HIGHLY LINEAR LOW NOISE AMPLIFIER

A Thesis

by

SIVAKUMAR GANESAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2006

Major Subject: Electrical Engineering

HIGHLY LINEAR LOW NOISE AMPLIFIER

A Thesis

by

SIVAKUMAR GANESAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Co-Chairs of Committee,	Edgar Sanchez-Sinencio
	Jose Silva-Martinez
Committee Members,	Aydin Karsilayan
	Aniruddha Datta
	Charles S. Lessard
Head of Department,	Costas Georghiades

May 2006

Major Subject: Electrical Engineering

ABSTRACT

Highly Linear Low Noise Amplifier. (May 2006)

Sivakumar Ganesan, B.E. (Hons.)

Birla Institute of Technology and Science, Pilani

Co-Chairs of Advisory Committee: Dr. Edgar Sanchez-Sinencio
Dr. Jose Silva-Martinez

The CDMA standard operating over the wireless environment along with various other wireless standards places stringent specifications on the RF Front end. Due to possible large interference signal tones at the receiver end along with the carrier, the Low Noise Amplifier (LNA) is expected to provide high linearity, thus preventing the inter-modulation tones created by the interference signal from corrupting the carrier signal.

The research focuses on designing a novel LNA which achieves high linearity without sacrificing any of its specifications of gain and Noise Figure (NF). The novel LNA proposed achieves high linearity by canceling the IM3 tones in the main transistor in both magnitude and phase using the IM3 tones generated by an auxiliary transistor. Extensive Volterra series analysis using the harmonic input method has been performed to prove the concept of third harmonic cancellation and a design methodology has been proposed. The LNA has been designed to operate at 900MHz in TSMC 0.35um CMOS technology. The LNA has been experimentally verified for its functionality. Linearity is usually measured in terms of IIP3 and the LNA has an IIP3 of +21dBm, with a gain of 11 dB, NF of 3.1 dB and power consumption of 22.5 mW.

DEDICATION

To my parents and sisters

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisors Dr. Edgar Sanchez-Sinencio and Dr. Jose Silva-Martinez for helping me out during my difficult times at TAMU both on technical and personal fronts. I thank them for all the knowledge that I have gained on analog circuits in the past two and half years and for having shaped me into what I am today.

I would like to thank my committee members Dr. Aydin Karsilayan, Dr. Aniruddha Datta and Dr. Charles S. Lessard for being on my committee and for patiently listening and signing on my numerous changes to my degree plan.

I would like to thank my amma, appa and my sisters Sudha and Bhuvani, for, without their advice I would have been designing digital circuits at Wipro Technologies without being exposed to the wonderful world of analog circuit design. They were highly supportive, both emotionally and financially during my stay at TAMU, encouraging me all the time and giving me courage to face any situation, however difficult it might have been.

I am grateful to my seniors Alberto, Chinmaya and Bharath for taking the time to answer my questions and clear my doubts in spite of their hectic schedules.

Radhika needs a special mention here for this thesis wouldn't have been possible without her support during the earlier stages of the project. I thank her for all that I have learned from all those heated discussions.

Life in the U.S. gets quite boring over the weekends. Though I had lots of fun watching every possible movie, I would like to thank my roommates Gopi, Vishnu and Kota for bearing and enjoying all those movies with me. I would also like to thank Ranga, Aluri, Ananth, Prakash, Nitin, Uday, Suganth, Bhavani, Preethi, ND and Ramya for the great time I had at TAMU.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 PROBLEM STATEMENT

Communication technology has progressed rapidly in the 21st century from wired technology to analog cellular and most recently to digital cellular technology. Ever increasing number of subscribers combined with increasing demand for high data rate applications like wireless video has resulted in various different standards spanned over closely spaced frequencies. In today's wireless environment, various standards coexist in the same geographical area, starting from 1G represented by the AMPS; 2G represented by GSM; 2.5G represented by GPRS and EDGE; and most recently 3G represented by UMTS, WCDMA. Table-1 below shows the frequency spectrum occupied by various standards currently used.

Table 1. Frequency spectrum of various communication standards

Standard	Frequency Spectrum
AMPS	800MHz – 900MHz
GSM	900MHz and 1.8GHz
UMTS	1.9GHz and 2.17GHz
WLAN	2.4GHz
Bluetooth	2.4GHz

From the Table-1, it can be seen that the frequency spectrum around 900MHz and 2.4GHz is crowded. Due to the limited spectrum allocated to each user, the signal is

---

This thesis follows the style of *IEEE Journal of Solid-State Circuits.*

subjected to interference from various out of channel signals operating within the band of interest and various out of band signals. This combined with the numerous other co-existing standards place stringent requirements on the RF receiver front end design. Thus the receiver should be able to sufficiently suppress the interference signals and process the desired channel of interest.

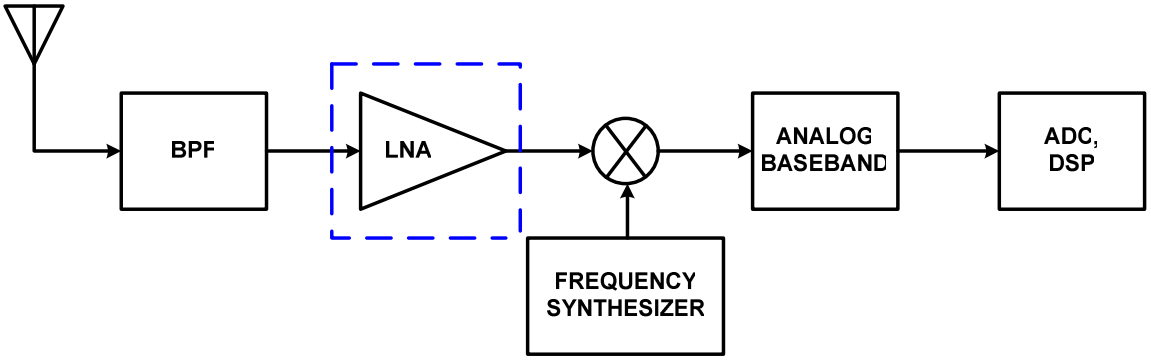


Fig. 1. Block diagram of a typical receiver.

The block diagram of a typical receiver is shown in Fig. 1. As shown in the figure, the Low Noise Amplifier (LNA) is usually preceded by a band-pass filter which filters the out of band signals while allowing the in-band signals to pass through. Hence the LNA forms the first block that amplifies the desired band of signals without adding significant noise to the signal. The LNA receives the entire in-band of signals with the out of band signals sufficiently suppressed. The LNA is a non-linear device and generates various frequency components few of which affect the input signal. This non-linear characteristic results in two important problems namely “Blocking” and “Intermodulation” which are explained in detail below.

In general, for a given input $x(t)$ to the LNA, the output $y(t)$ can be approximately represented as:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad (1)$$

Where α_1 represents the gain of fundamental signal and α_2, α_3 represent the second and third order non-linearities of the amplifier.

The problem involved with blocking of signal is explained below [1]. A weak input signal accompanied by a strong in-band interferer (neighbor channel for instance) tends to reduce the gain of LNA and desensitize the circuit. This characteristic is analyzed below. Let the input signal be represented as sum of desired signal ($A_1 \cos \omega_1 t$) and strong interferer ($A_2 \cos \omega_2 t$) given by $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, where $A_1 << A_2$. The output of the system represented by (1) is given by

$$y(t) \cong \left(\alpha_1 + \frac{3}{2} \alpha_3 A_2^2 \right) A_1 \cos \omega_1 t + ... \quad (2)$$

As shown in (2), if $\alpha_3 < 0$, which is usually the case, a large interferer might "block" the entire signal thus resulting in zero output signal at frequency ω_1.

Another interesting problem that occurs in non-linear circuits is "Intermodulation". When two strong in-band interferers appear at the input, the circuit non-linearities result in intermodulation components which fall on the signal of interest thus corrupting the input signal. Intermodulation is shown mathematically below. If the input interferer is given by $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, the output represented by (1) is given by

$$
\begin{aligned}
y(t) &= \alpha_1\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right) + \alpha_2\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^2 + \\
&\quad \alpha_3\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^3 \\
&= \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos\omega_1 t + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right)\cos\omega_2 t \\
&\quad + \alpha_2 A_1 A_2\cos(\omega_1+\omega_2)t + \alpha_2 A_1 A_2\cos(\omega_1-\omega_2)t \\
&\quad + \frac{3}{4}\alpha_3 A_1^2 A_2\cos(2\omega_1+\omega_2) + \frac{3}{4}\alpha_3 A_2^2 A_1\cos(2\omega_2+\omega_1) \\
&\quad + \frac{3}{4}\alpha_3 A_1^2 A_2\cos(2\omega_1-\omega_2) + \frac{3}{4}\alpha_3 A_2^2 A_1\cos(2\omega_2-\omega_1)
\end{aligned}
\tag{3}
$$

It can be seen from (3) that various frequency components are generated at the output. But the third order intermodulation components (IM3) located at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ are of particular interest as they fall in the frequency band of interest while the rest of the frequency components either fall at very high frequencies or can be filtered out.

These intermodulation components thus created tend to corrupt the signal and hence form a very important part of any RF system. Input third order intercept point (IIP3) is the figure of merit that is used to characterize an RF system for its non-linearity. This is usually measured by a two tone test for sufficiently low amplitudes 'A', in the linear region of operation of the system. As the input amplitude is increased, the fundamental components at the output increase proportional to 'A' while the third order intermodulation components increase proportional to 'A^3'. In theory, for sufficiently higher amplitudes, the intermodulation components become equal to the fundamental and the input amplitude 'A' at this point is defined as IIP3. But the amplifier output saturates at such high amplitudes and IIP3 is obtained by linearly extrapolating with the values for low input amplitudes as shown in Fig. 2.

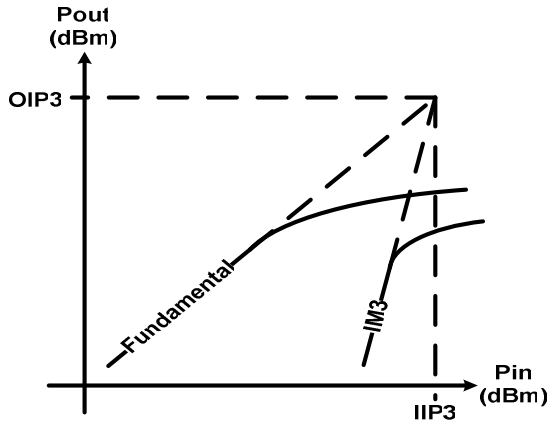


Fig. 2. IIP3 calculation.

In an RF system with different cascaded blocks, the IIP3 of the system is dominated by the IIP3 of the last stages as they encounter larger signal amplitudes while the noise figure (NF) of the system is dominated by the NF of the input stage. But in today's wireless environment, due to the problems involving interferers described above, the LNA should also be able to suppress the interferers without which the following mixer block encounters a much larger interferer and thus demanding much higher performance from it in terms of linearity and trading off on its other specifications like conversion gain. Thus an LNA that achieves high levels of linearity and consequently high IIP3 is desired. But the main function of an LNA is to achieve high gain without adding significant noise (less NF) to the signal. Thus any circuitry that is used in the LNA to achieve higher linearity shouldn't achieve that at the expense of gain and NF.

The objective of this thesis is to design a novel low noise amplifier that achieves high IIP3 in the order of 20dBm without sacrificing gain and NF. The next section describes some of the circuit topologies in the literature used to achieve high linearity in the LNA.

1.2 BACKGROUND

This section describes the various techniques used to achieve high linearity in an LNA and their advantages and drawbacks. The linearity techniques can be broadly classified into four different categories namely, optimum biasing, linear feedback, optimum out-of-band terminations and feedforward.

1.2.1 Optimum biasing

The non-linearity of a MOS transistor arises from its voltage to current (V-I) conversion. The drain current in a MOSFET can be modeled in terms of its gate-source voltage as given in (4).

$$i_d = g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + ... \quad (4)$$

Where g_{m1} is its transconductance, g_{m2} represents its second order non-linearity obtained by the second order derivative of FET transfer characteristics (Id-Vgs) and g_{m3} is its third order non-linearity obtained by the third order derivative of FET transfer characteristics. The IIP3 is given in the above-mentioned-terms as follows [2].

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \quad (5)$$

The I_d-V_{gs} transfer characteristics of a common source transistor along with g_{m1}, g_{m2}, g_{m3} are shown in Fig. 3 for the case of a transistor in 0.35µm CMOS process. It can be seen that in the region of moderate inversion, in-between weak inversion and strong inversion, the third order derivative (g_{m3}) becomes zero over a narrow region [3]. As shown in (5), it can be seen that IIP3 approaches infinity as g_{m3} becomes zero. Thus any transistor biased at this point can achieve high linearity. But the problem with this

mechanism is that the region over which this linearity boost can be obtained is very narrow and due to process variations this bias point is bound to change leading to a very sensitive and limited improvement. Also, the transistor has to be biased in moderate inversion at the "sweet spot" hence placing a restriction on the transconductance of the input stage. This restricts the maximum gain that can be obtained and thus affects the noise figure (NF) which is highly undesirable.

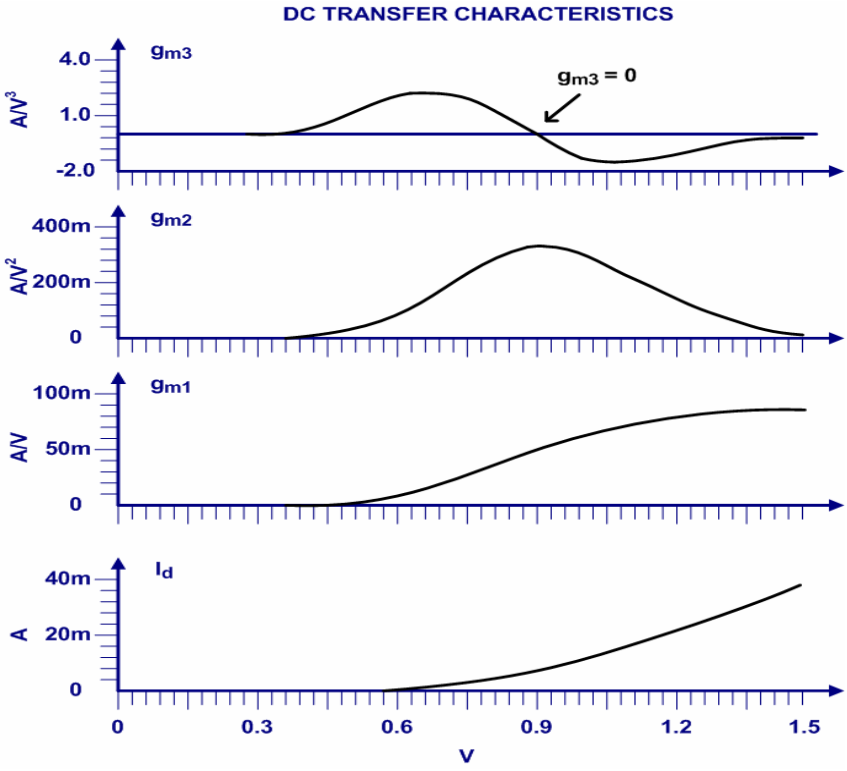


Fig. 3. MOSFET transfer characteristics.

Various bias circuit techniques have been proposed [4] where the input transistor can be optimally biased such that $g_{m3} = 0$. It has been proven that the actual point of bias at which high levels of IIP3 can be achieved is slightly offset from the bias point at which

g_{m3} is zero. But such a bias circuit is again prone to process variations resulting in poor linearity and would require fancy process to minimize the mismatch between transistors.

1.2.2 Feedback

The most popular technique in base-band circuits to obtain high linearity is through the use of negative feed back. Fig. 4 shows the configuration of a negative feedback non-linear amplifier with gain 'A' and a linear feedback factor 'β'.

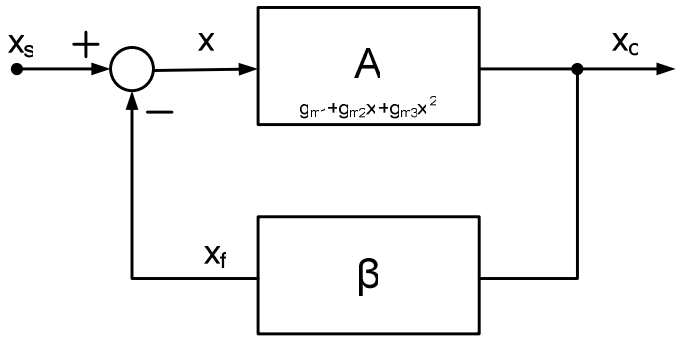


Fig. 4. Non-linear amplifier with linear feedback.

In the feedback method, a fraction of the output signal (x_o) is fed back to the input (x_s) through a linear feedback network (β) and is subtracted from the input to generate an error signal (x_i) which is fed to the amplifier (A). The amplifier transfer function is given as follows.

$$\begin{aligned} x_o(t) &= a_1 x_i(t) + a_2 x_i^2(t) + a_3 x_i^3(t) \\ x_i(t) &= x_s(t) - x_f(t) = x_s(t) - f x_o(t) \end{aligned} \tag{6}$$

The closed loop transfer function is given by

$$x_o(t) = b_1 x_s(t) + b_2 x_s^2(t) + b_3 x_s^3(t) + ... \tag{7}$$

The coefficients b_1, b_2, b_3 are calculated [5], and the third order intermodulation distortion can be given as follows.

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|(1+a_1 f)^3} \tag{8}$$

When compared to (5), it can be seen that IIP3 as shown in (8) has increased by a factor of $(1+a_1 f)^{3/2}$. Thus, feedback has improved the linearity at the expense of loss in the gain by a factor of approximately the loop gain ($T_o = a_1 f$). Further analysis without any approximations [5] leads to the following expression for IIP3.

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|\frac{(1+T_o)^3}{\left(1-\frac{2a_2^2}{a_1 a_3}\frac{T_o}{1+T_o}\right)}} \tag{9}$$

As shown in (9), it can be seen that the IIP3 is also affected by the second order non-linearity (a_2). In CMOS circuits which operate in strong inversion region, the co-efficients a_1 and a_3 are of opposite signs leading to further reduction in IIP3 than that shown in (8). In high frequency RF circuits, this phenomenon is further noticeable due to the parasitic capacitances which offer very small impedance at that frequency and hence are no longer negligible [6].

The traditional inductive source degenerated common-source LNA shown in Fig. 5, falls under the category of feedback linearization in which the source degeneration inductor acts as the feedback circuit. Though this LNA has been proven to give the best gain and noise performance for a given power [7], it suffers from poor linearity due to the second order non-linearity feedback effect described above. This is explained in detail in the

section on feedforward techniques. Further, the concept of negative feedback is not that compatible with RF circuits since the gain of the amplifier is in the order of 10-20dB as opposed to base band circuits where a gain of 60dB can be easily achieved.

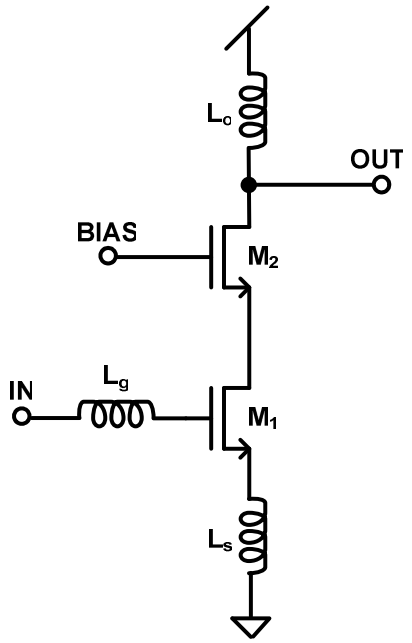


Fig. 5. Cascode LNA with source degeneration inductor.

1.2.3 Input impedance frequency termination

The feedback network discussed in the previous section was considered to be frequency independent which would be true in the case of pure resistive networks. But typical feedback networks involve frequency dependent passive elements like inductors and capacitors. This results in the frequency response of the feedback network affecting the linearity of the signal due to the frequency varying impedance it presents to the different harmonics generated by the input device. This process is explained with an example of source degenerated common-emitter transistor here.

The value of IM3 for a source degenerated common-emitter transistor shown in Fig. 6 is derived in [8] and is given below. The small signal model of the common-emitter transistor used to derive (10) is also shown in Fig. 6.

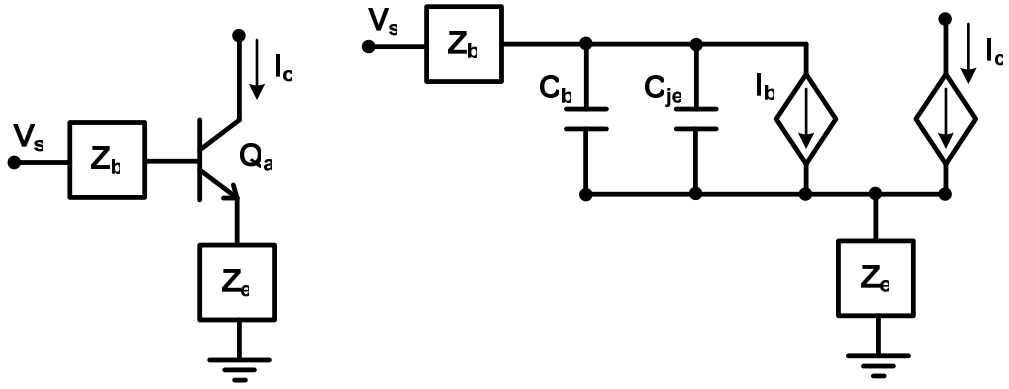


Fig. 6. Common emitter transistor with source degeneration.

$$|IM3| \approx \left|\frac{A_1(s)}{I_Q}\right|^3 \left|\frac{V_T}{4}\left[1+sC_{je}Z(s)\right]\left\{-1+\frac{A_1(\Delta s)}{g_m}\left[1+\Delta sC_{je}Z(\Delta s)\right]+\frac{A_1(2s)}{2g_m}\left[1+2sC_{je}Z(2s)\right]\right\}\right| |V_s|^2$$

where

$$\Delta s = (s_a - s_b) << s, \quad s_a = j2\pi f_a, \quad s_b = j2\pi f_b \qquad (10)$$

$$s \approx s_a \approx s_b,\ s_a > s_b$$

$$A_1(s) = \frac{g_m}{sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m \left.Z(s)\right/\beta_o + 1 + g_m Z_e(s)}$$

$$Z(s) = Z_b(s) + Z_e(s)$$

It can be seen from the IM3 expression given in (10) that the second order frequency components generated due to 2nd harmonic frequency ($2s$) and difference frequency (Δs) are fed back to the input which further get mixed with the fundamental components to generate third order inter-modulation components. In the case of inductive source degeneration, the impedance presented by the inductor at 2nd harmonic frequency is much higher than that presented at difference frequency. Hence the gain at 2nd harmonic

frequency is less than that at difference frequency. Hence the term $A_1(\Delta s)/g_m$ is significant and $A_1(2s)/2g_m$ can be neglected. The input can be terminated with low-frequency impedance which traps the difference frequency components fed back to the input. Fig. 7 shows the configuration of a trap network reported in [9].

In the circuit configuration shown in Fig. 7, the low frequency input trap network consisting of L_t and C_t are tuned to change the input impedance at the difference frequency so that the product associated with $A_1(\Delta s)/g_m$ in (10) cancels with the "-1", resulting in high IIP3 values. But the problem with such a circuit is that the required values of inductance would be huge thus forcing the use of off-chip inductors.

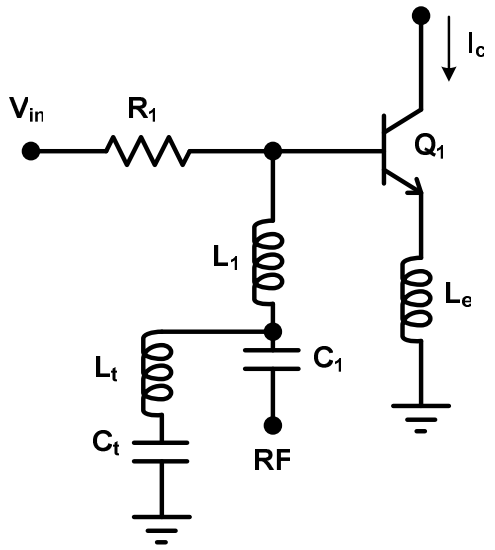


Fig. 7. Low frequency input impedance termination.

This concept of input termination has been applied in various other topologies. In [10], all the three terminals of a BJT are terminated with low frequency impedance thus resulting

in high IIP3. In [11], a current mirror with negative feedback is used to bias the LNA and provide low frequency input termination. In [12], the impact of terminating both input and output impedance in the case of CMOS circuits is experimentally shown.

1.2.4 Feedforward cancellation

In this technique, scaled versions of the input signal are fed to two different amplifiers whose outputs are added to obtain the final output. The input signals are scaled such that the third order distortion is eliminated at the final output.

This feedforward cancellation technique is used to achieve high linearity in [13] as described below. As shown in Fig. 8, output $y(t)$ is obtained by subtracting the output of the main amplifier ($y_{main}(t)$) from that of the auxiliary amplifier ($y_{aux}(t)$) whose inputs are x and βx ($\beta < 1$) respectively.

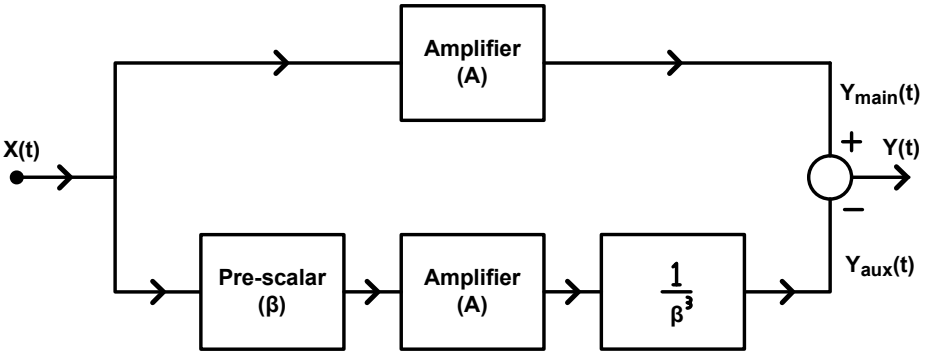


Fig. 8. Feedforward cancellation technique.

The equations given below show the complete cancellation of third order distortion.

$$
\begin{aligned}
y_{main}(t) &= A.x.(1+\alpha_2 x^2) \\
y_{aux}(t) &= A.\beta.x.(1+\alpha_2 \beta^2 x^2) \\
y(t) &= y_{main}(t) - \frac{1}{\beta^3} y_{aux}(t) \\
&= A\left(1-\frac{1}{\beta^2}\right).x
\end{aligned}
\tag{11}
$$

As shown in the equations above, the third harmonic can be cancelled to obtain high IIP3 by using two similar amplifier blocks (A) and scaling (β) their inputs appropriately.

But this technique has several disadvantages. The gain of the amplifier is reduced at the expense of canceling the third order distortion. Due to the reduced gain, the noise figure (NF) worsens. Further, more noise is added due to more active components in the circuit. This technique is highly sensitive to mismatch between the main and auxiliary gain stages and errors in the signal scaling factor. This configuration also consumes more power due to two amplifier stages being used.

A different approach to feedforward cancellation technique which uses the FET transfer characteristics to obtain high linearity is the "DS Method" [14]. This method addresses the problem of narrow range of values associated with optimum biasing technique for achieving high IIP3 and the problem of gain reduction associated with the feedforward technique described above.

As shown in the FET transfer characteristics in Fig. 3, the third order distortion component (g_{m3}) changes from positive to negative as V_{gs} is varied from weak inversion to strong inversion. Thus if the output currents of two transistors are added with the bias

points chosen at the positive and negative peaks of g_{m3} and the widths scaled such that the positive and negative peaks are equal in magnitude, the output current would result in zero g_{m3} and thus high linearity over a wide range of bias values. This configuration is shown in Fig. 9, where transistor M_A is biased in weak inversion and M_B is biased in strong inversion. The third order non-linearity DC-transfer characteristics for the strong and weak inversion transistors for the above configuration are shown in Fig. 10.

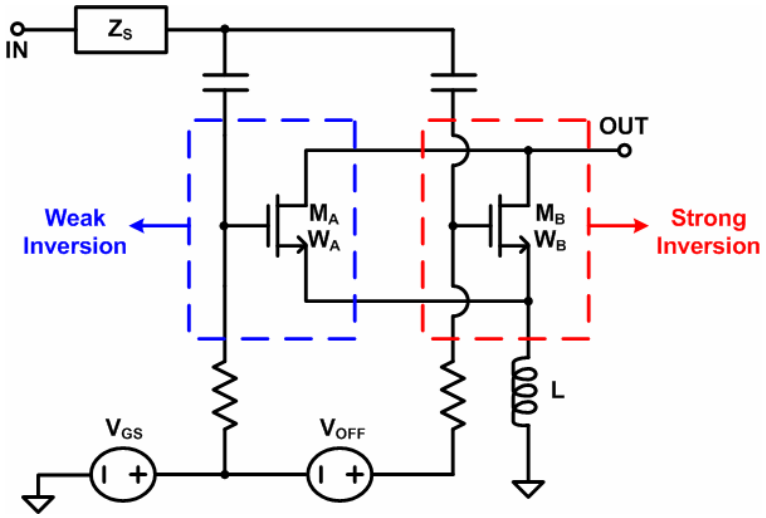


Fig. 9. DS method.

To obtain a much wider range of bias values over which g_{m3} is flat and close to zero, outputs of scaled and bias shifted transistors can be connected in parallel to the circuit shown in Fig. 9 such that the negative peak in the FET transfer characteristics of one cancels the positive peak if any, of the other. In [15-16], the same technique has been implemented using a multiple-gated transistor in which the gate width and gate bias of each transistor can be adjusted separately. In [17] this technique has been used with the auxiliary transistor implemented using a parasitic BJT. The BJT is biased in strong

inversion region as the g_{m3} in this case is positive thus achieving higher gain. In [18], the auxiliary transistor is implemented in triode region using the same technique.

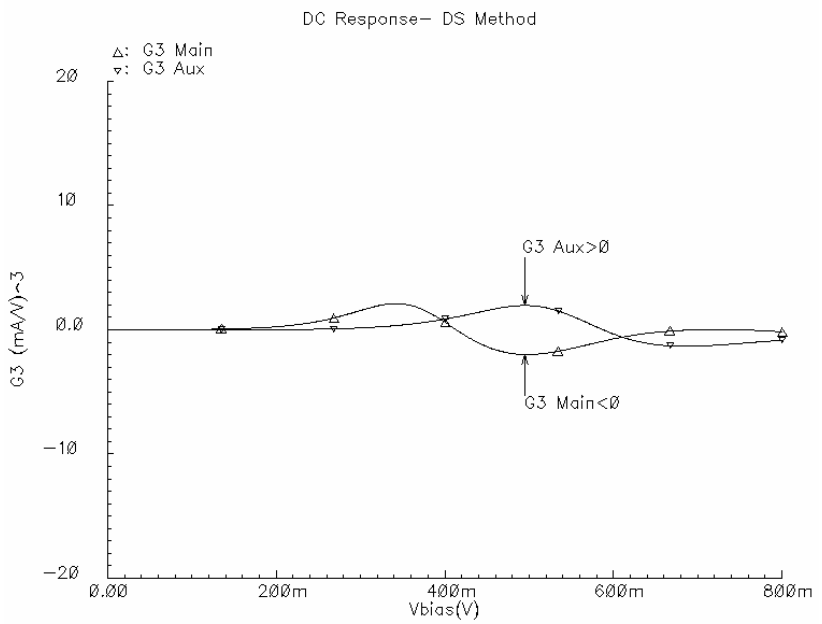


Fig. 10. Third order non-linearity transfer characteristics in DS method.

The drawback with DS-method is that it is valid only at very low frequencies at which the effect of circuit reactances is negligible. At high frequencies the source degeneration inductance creates a feedback path for the drain current i_d to the gate source voltage V_{gs} of M_B through the gate-source capacitance (C_{gs}). For example, the second harmonics ($2\omega_1, 2\omega_2, \pm\omega_1 \pm \omega_2$) generated are fed-back across the gate and source thus adding to the fundamental components. These spectral components along with the fundamental result in more IM3 components at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ due to the second order non-linearity. Thus, the second order non-linearity of i_d also contributes to IMD3.

Using the Volterra series, the exact expression for the IIP3 at RF frequencies is calculated in [4] and is given as follows.

$$IIP3 = \frac{4 g_{m1}^2 \omega^2 L C_{gs}}{3|\varepsilon|}$$

$$where, \qquad \varepsilon = g_{m3} - \frac{2 g_{m2}^2 / 3}{g_{m1} + \frac{1}{2 j \omega L} + 2 j \omega C_{gs} + Z_s(2\omega)\frac{C_{gs}}{L}} \tag{12}$$

As can be seen from (12), making g_{m3} zero as done in the DS method doesn't result in a large IIP3 due to the additional term in ε. This term, as stated above, represents the contribution of the second order non-linearity to generate IM3 components and it depends on the source degeneration inductor L. Thus at RF frequencies, the second order non-linearity component g_{m2} plays a major role in limiting the levels of IIP3 that can be obtained.

A "modified DS method" proposed in [19-20] addresses this issue of feed back of second order frequency components. In this method, the magnitude and phase of second order non-linearity contribution to IMD3 is tuned to cancel the third order non-linearity contribution to IMD3 thus resulting in an output current with zero IM3 component. As shown in Fig. 11, the transistor M_1 is biased in strong inversion region with negative g_{m3} while M_2 is biased in weak inversion with positive g_{m3}. The two source degeneration inductors L_1 and L_2 connected to the sources of the two transistors are used to tune the magnitude and phase of the IM3 components in each branch.

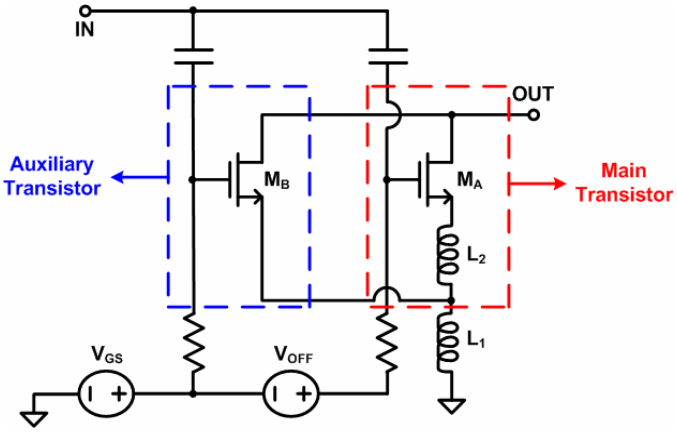


Fig. 11. Modified DS method.

There are primarily two disadvantages involved in any of these methods using the feedforward technique involving two or more transistors connected in parallel with one or more transistors operating in weak inversion region. The first and the most important problem is that the additional weak inversion transistors added to achieve linearity degrades the noise performance of an LNA. This can be explained as follows [19].

The most significant noise sources at RF frequencies are the drain current noise and the gate induced noise given by

$$i_{nd}^2 = 4kT\Delta f\gamma g_{d0}$$
$$i_{ng}^2 = 4kT\Delta f\delta \frac{\omega^2 C_{gs}^2}{5g_{d0}} \qquad (13)$$

Where, γ *and* δ are bias dependent noise coefficients and g_{d0} is the drain source conductance at zero V_{DS}. Since the drain current in weak inversion is due to diffusion, g_{d0} is given by I_{Dsat}/ϕ_t ; where ϕ_t is the thermal voltage (kT/q). Since the FET in weak

inversion draws a negligible drain current, its induced gate noise is inversely proportional to the drain current and, thus can be quite significant.

The other problem with this circuit configuration is that the weak inversion transistor loads the input node and adds extra capacitance thus affecting the input match and maximum frequency of operation. The increased capacitance would demand a larger source inductor to achieve 50Ω input matching. Further, the number of iterations required for optimization would be large as any changes to the weak inversion transistors to tune for linearity would result in the input match being affected and vice versa.

The proposed solution achieves high linearity without the problems involved with the above circuits and is discussed in the next section.

1.3 PROPOSED IDEA AND MAIN ACHIEVEMENTS

Any new technique for achieving high linearity in an LNA should be able to achieve it without sacrificing any of the important specifications of gain and noise figure (NF) and at the expense of minimal additional power. A novel highly linear LNA is presented in this work. The proposed solution uses the feedforward technique in which the magnitude and phase of the IM3 current components in each branch are tuned such that they are equal in magnitude and opposite in phase and effectively cancel each other at the output of LNA. The LNA is designed in TSMC 0.35µm CMOS technology and has been fabricated using the MOSIS facility and packaged using the MLF64 leadless package. The LNA is designed to operate at a frequency of 900MHz. It achieves an IIP3 of

+21dBm, with a gain of 19.3 dB, NF of 3.1 dB and power consumption of 15.1 mW in simulation. Two versions of the same technique will be discussed in the following sections.

1.4 THESIS GUIDE

This section gives a brief description of the organization of this thesis. This thesis has been divided into three sections.

Section 2 describes the problems that need to be addressed to achieve high linearity. The novel idea behind achieving high linearity is introduced and the circuit implementation of the same without sacrificing on any of the other specifications of the LNA is described. The problems involved with the solution are explained and an alternative circuit topology has been proposed. A detailed Volterra series analysis is performed and the MATLAB plots theoretically proving the concept of achieving high linearity using this circuit topology are shown. A design procedure to choose the inductor values is presented.

Section 3 presents the various simulation and experimental results achieved. The lab setup for measuring the IIP3 of the LNA is described. The results are compared with those of existing circuits and conclusions are drawn about the comparative performance of the circuit.

2. NOVEL LINEAR LNA

This section discusses the proposed novel linear LNA designed to operate at 900MHz. The principle behind achieving high linearity without losing out on gain or NF is explained in detail. The Volterra analysis is used to theoretically prove this concept and a design strategy has been presented.

2.1 INTRODUCTION

As illustrated in section 1.2.4, most the existing techniques for achieving high linearity in an LNA are not valid at RF frequencies due to the issue of feedback of second-order frequency components. Any improvement over the existing techniques is possible only if the proposed technique takes into consideration this feedback effect of second-order components. As explained in the previous section, the "modified DS method" takes a step in the right direction by canceling the IM3 components generated due to third order non-linearity with that generated by the feedback of second-order frequency components. This appears to be an ideal solution but for the problems associated with the increased noise figure (NF) due to the transistor operating in weak inversion region and the lack of flexibility offered by the design to be able to tune the transistor for input match and higher linearity independently. The input match and tuning of linearity depend on the same set of components leading to increased number of design steps to arrive at an optimized solution.

The following section describes the proposed phase cancellation technique for achieving high linearity without sacrificing the gain or the NF.

2.2 PHASE CANCELLATION TECHNIQUE

In all the proposed variants of feedforward technique, the input signal is fed both to the main amplifier and the auxiliary amplifier and the outputs are added to achieve high linearity. The auxiliary transistor connected in parallel to the main transistor is the reason for the problems associated with the existing solutions explained in the previous section. Hence, the first major step is to remove the auxiliary transistor connected to the gate of the main transistor. Further, it can be seen that the current in the main amplifier contains the information of all the frequency components generated by the input transistor. This can somehow be treated separately to achieve high linearity. This is explained in detail below.

The proposed solution uses the technique of phase cancellation as in the modified DS method to achieve high linearity. As stated above, the drain current in a simple cascode LNA configuration shown in Fig. 5, contains the IM3 components which are a result of IM3 components generated due to third order-nonlinearity and feedback of second order non-linearity components. If this information can somehow be used to generate an output current in an auxiliary amplifier with the IM3 components being equal in magnitude and out of phase with those in the main amplifier, the sum of these output currents would result in a zero IM3 component at the output of the LNA as shown in Fig. 12.

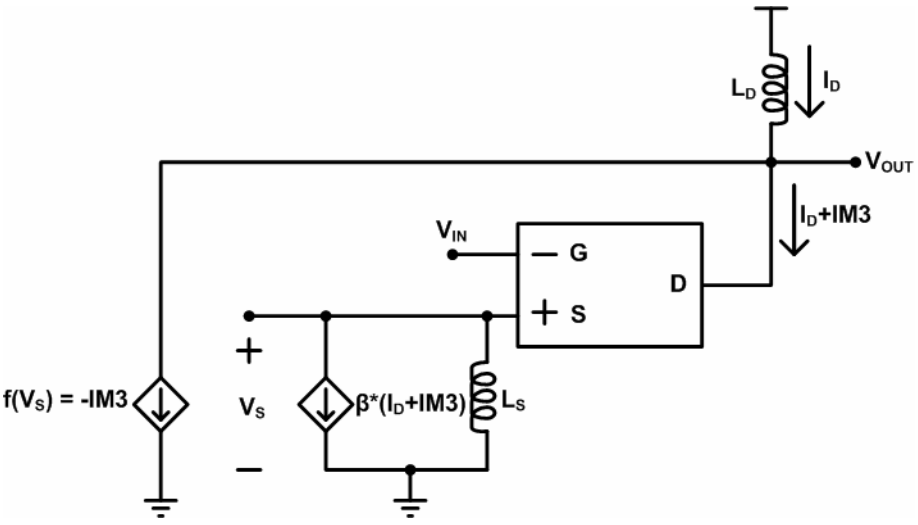


Fig. 12. Conceptual view of proposed solution.

The schematic of the realized circuit for the proposed solution is shown in Fig. 13. The transistors M_A and M_C form the basic cascode LNA with the inductors L_G and L_A for obtaining input match and the inductor L_O for resonating with the output capacitance to provide gain at the desired frequency. The transistor M_B forms the auxiliary transistor and is source degenerated with the inductor L_B and is used to tune the magnitude and phase of the IM3 components. The non-linearity information present in the drain current of the main transistor (M_A) is tapped as voltage at its source and forms the input to the auxiliary transistor. The transistor M_A is biased in strong inversion with negative g_{m3} and the transistor M_B is biased in weak inversion with a positive g_{m3}. The aspect ratio, bias voltage and the inductance value associated with the auxiliary amplifier are tuned to cancel the IM3 components generated by the main transistor. Though the signal at the source of main transistor is small, the auxiliary transistor operating in weak inversion region is highly non-linear with high g_{m3} and hence the magnitude of IM3 component

generated in the auxiliary should be able to match the magnitude of IM3 component in the main transistor.

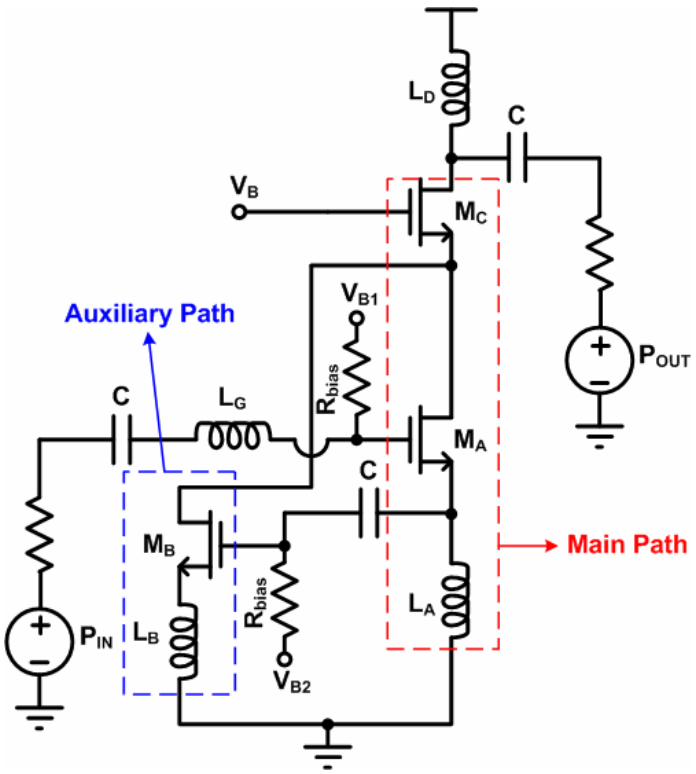


Fig. 13. Proposed solution.

2.3 THEORETICAL ANALYSIS AND DESIGN

To theoretically prove that the proposed circuit achieves high linearity, the equivalent small signal model of the circuit in Fig. 13 shown in Fig. 14 is analyzed. The effect of all parasitic capacitances other than the gate-source capacitance is neglected. The capacitances C_A and C_B shown are the gate-source capacitances of main and auxiliary transistors respectively. The inductors L_A and L_B are the source degeneration inductors for the main and auxiliary transistors respectively. The impedance Z_s is the input source impedance. The currents i_A and i_B are the currents through main and auxiliary transistors

respectively. The current i_{out} forms the output current which is a sum of both i_A and i_B. The expressions used for the above mentioned currents are given below.

$$
\begin{aligned}
i_A &= g_{1a}V_A + g_{2a}V_A^2 + g_{3a}V_A^3 \\
i_B &= g_{3b}V_B^3 \\
i_{out} &= i_A + i_B = C_1(s_1) * V_x + C_2(s_1, s_2) * V_x^2 + C_3(s_1, s_2, s_3) * V_x^3
\end{aligned}
\tag{14}
$$

Where g_{1a} represents the transconductance of the main amplifier and g_{2a} and g_{3a} represent the second and third order non-linearity co-efficients of the main transistor while g_{3b} represents the third order non-linearity of the auxiliary transistor. As shown in (14), g_{1b} and g_{2b} have been neglected since the auxiliary transistor is operating in weak inversion and they have very weak effect on the IM3 components. Volterra series is used to analyze the various coefficients of non-linearity associated with the output current for an input signal of amplitude 'A' and two tones at frequency ω_a and ω_b. The two tones are assumed to be closely spaced ($\omega_a \cong \omega_b$).

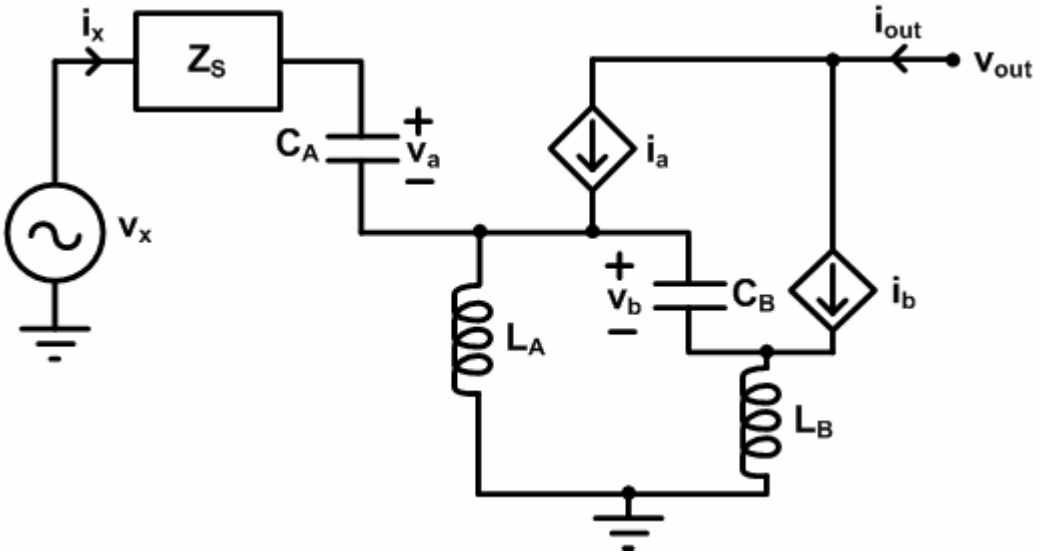


Fig. 14. Small signal model of proposed solution.

The detailed analysis using Volterra series is shown in Appendix A. The expression obtained for IIP3 is given below.

$$IIP_3 = \frac{1}{6\,\mathrm{Re}(Z_s(s))\left|A_1(s)\right|^2}\left\{\frac{g_{1a}}{\varepsilon}\right\}$$

$$where,\ \varepsilon = g_{3a} - \frac{g_{2a}^2}{3g_{1a}} + g_{3b}n(s)\left|n(s)\right|^2\frac{2+s^2L_BC_B}{2(1+s^2L_BC_B)} \qquad (15)$$

$$n(s) = \frac{sL_A(g_{1a}+sC_A)}{1+sC_B(sL_A+sL_B)}$$

The above expression shows the effect of various circuit components on IIP3. It can be seen that the second order non-linearity co-efficient (g_{2a}) appears in the expression due to the feedback effect discussed before. But it can be seen that the effect of g_{2a} on IIP3 has become independent of any circuit components thus resulting in a constant value. The value of g_{3b} can be tuned to obtain high IIP3 by choosing appropriate values for the inductors L_A and L_B. Fig. 15 shows the theoretical values of IIP3 that can be obtained for different values of L_A and L_B. This result is obtained from a MATLAB simulation for given values of $g_{1a}, g_{2a}, g_{3a}, g_{3b}, C_A, C_B$.

It can be seen from Fig. 15 that the value of IIP3 peaks for certain values of inductors L_A and L_B. The graph of IIP3 proves the theory of phase cancellation too. As shown in the graph, very large values of IIP3 can be obtained when the IM3 components in both main and auxiliary transistors cancel perfectly. The very high peaks in the graph are the points at which perfect cancellation and hence zero IM3 components at the output are obtained. Biasing the LNA at this particular point is very difficult and reasonable values of IIP3 in the order of 20-25dBm can be obtained over a range of values making the design reliable.

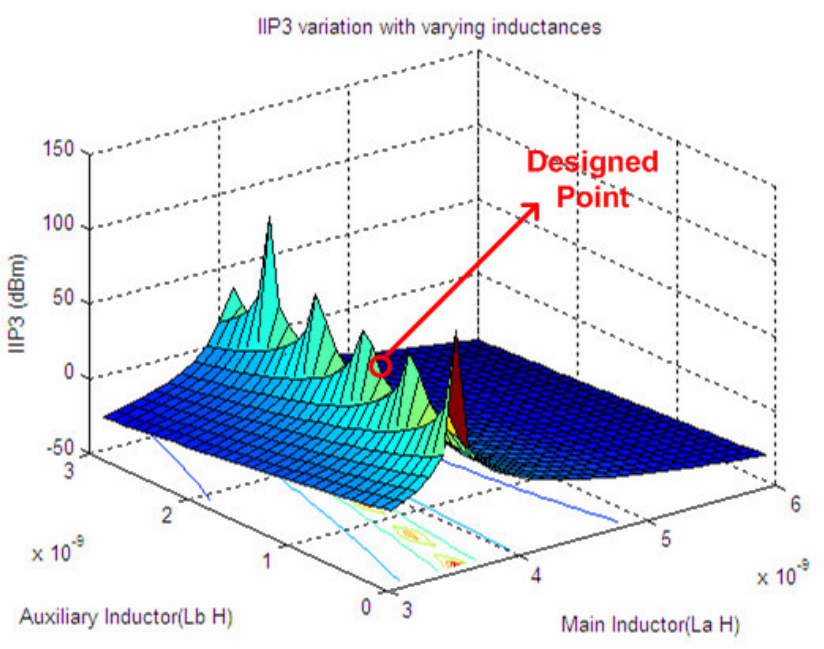


Fig. 15. Variation in IIP3 with source degeneration inductors.

For the initial design of Linear LNA, the aspect ratio of the auxiliary transistor can be assumed to be of same value as that of the main transistor of any given LNA, and biased in weak inversion region resulting in positive g_{3b}. The values of inductors required for the design can be selected from the graph drawn above. For any given cascode LNA, the values of g_{1a}, g_{2a}, g_{3a} can be obtained from the transistors transfer characteristics. For these given values the above mentioned plot can be drawn and the values of L_A and L_B can be selected as the points at which a peak in IIP3 can be observed over a broad range of values.

2.4 EFFECT ON OTHER SPECIFICATIONS OF LNA

The following section describes how the important specifications of input match, gain and noise figure of the LNA are affected due to the added auxiliary transistor.

2.4.1 Effect on input impedance matching

One of the major disadvantages in all of the feed-forward techniques is the inability to tune the circuit for good input match and good linearity independently. An ideal circuit block used to achieve high linearity should not affect the input match thus giving the designer flexibility to tune the circuit for good input match and hence good noise figure.

In this section, the input impedance of the proposed linear LNA is calculated to find the effect of the additional circuitry on the input match. In the small signal model shown in Fig. 16, the outputs are grounded and the input impedance given by $Z_{in} = V_{in} / I_{in}$ is calculated.

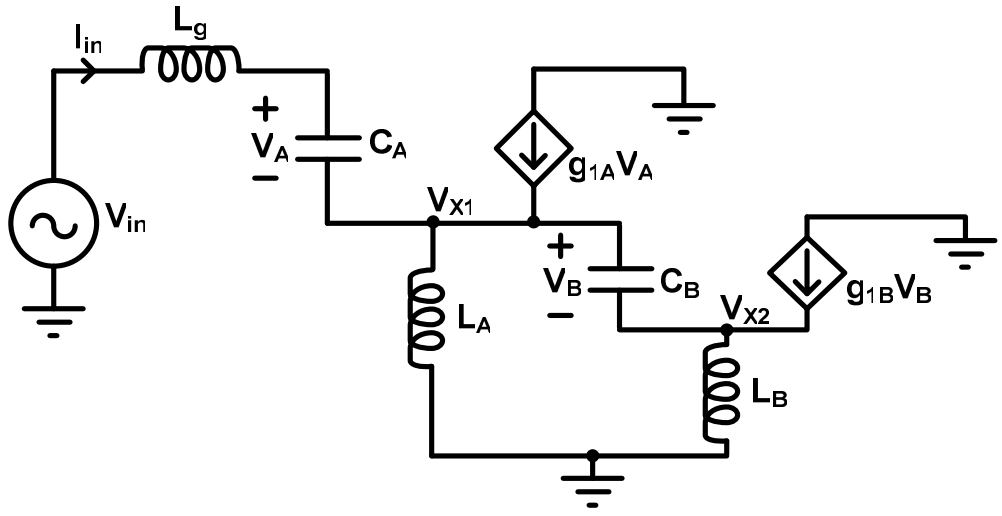


Fig. 16. Input impedance calculation.

The detailed calculation for the input impedance is given in Appendix B. The value of Z_{in} is found to be

$$Z_{in} = sL_G + \frac{1}{sC_A} + \left(sL_B\left(sC_B + g_{1b}\right)+1\right)\frac{\left(sL_A + \frac{g_{1a}L_A}{C_A}\right)}{\left(s^2 L_A C_B + sL_B\left(sC_B + g_{1b}\right)+1\right)} \tag{16}$$

If $\left|s^2 L_A C_B\right| << 1$, this term can be neglected and Z_{in} can be simplified as

$$Z_{in} = sL_G + \frac{1}{sC_A} + sL_A + \frac{g_{1a}L_A}{C_A} \tag{17}$$

It can be seen that the above equation is same as the input impedance of a regular cascode LNA [21]. Thus if the condition mentioned above is met, which is almost always the case at RF frequencies, the additional auxiliary circuit will not affect the input impedance and hence the input match, thus allowing independent tuning for perfect input match and high linearity.

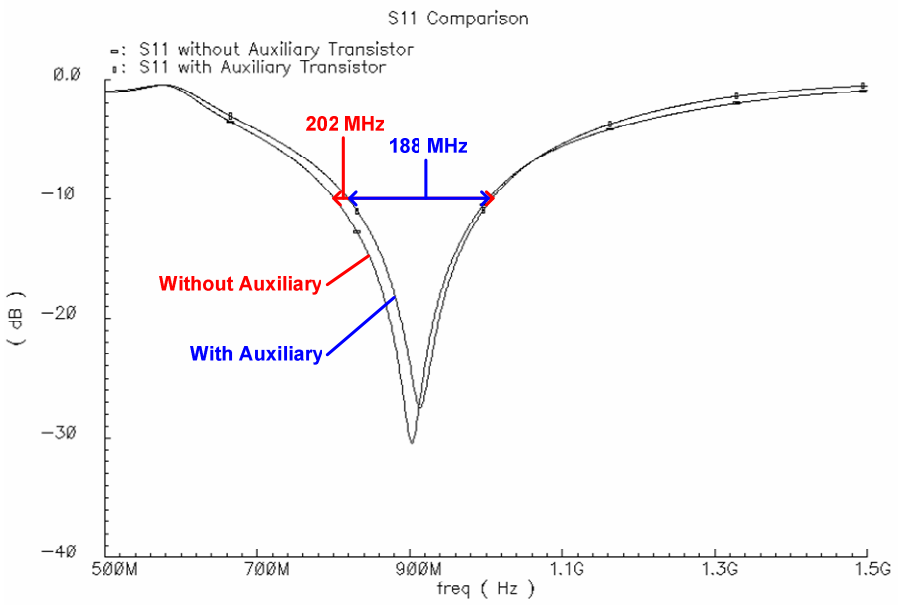


Fig. 17. Effect on input match.

Fig. 17 shows the effect of auxiliary circuit on input match. It can be seen from the figure that the change in the input match is negligible with added auxiliary transistor thus proving that the input impedance is unaffected as shown in (17).

2.4.2 Effect on gain and NF

In the proposed solution the main transistor (M_A) operates in strong inversion region while the auxiliary transistor (M_B) operates in weak inversion region. Since the current flowing through M_A is at least ten times larger than the current flowing through M_B, the transconductance (g_{1b}) of M_B is very less and hence its contribution to gain is very minimal. Also the additional power consumed due to the addition of the auxiliary transistor is less for the same reason.

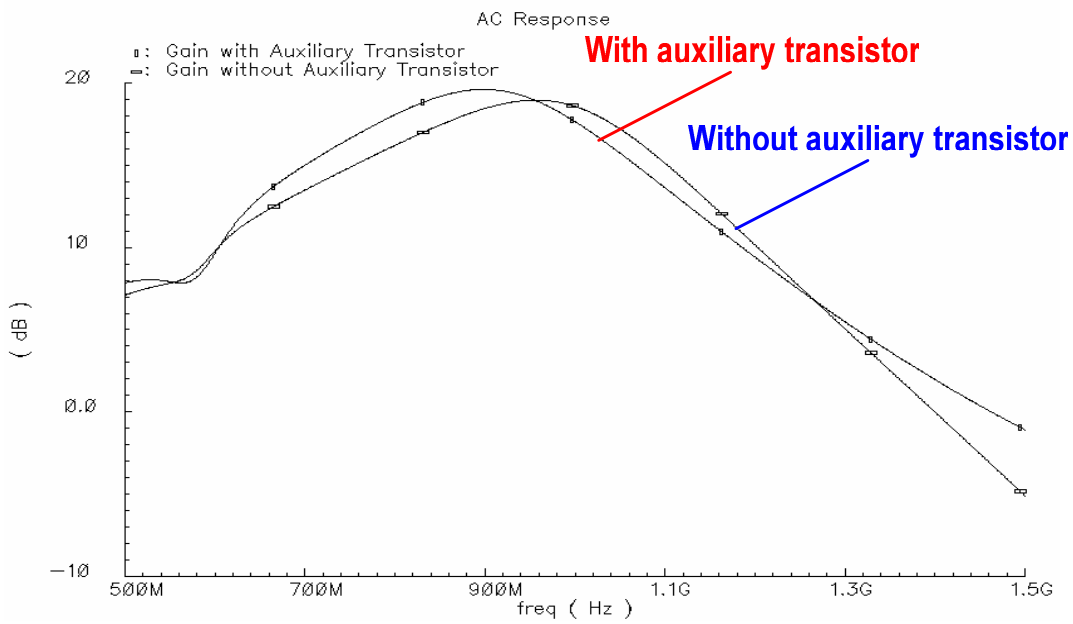


Fig. 18. Effect on gain.

Fig. 18 shows the gain of LNA with and without the auxiliary transistor. It can be seen from Fig. 18 that the auxiliary transistor has negligible effect on the gain. The small increase can be attributed due to the weak inversion transistor amplifying the fundamental by a small factor. The output peak has shifted to a slightly lower frequency due to output loading of the auxiliary transistor.

As explained in the previous section, the drain current noise in a weak inversion transistor is negligible as the drain current is very less, while the gate noise of a weak inversion transistor is inversely proportional to its drain current and hence it degrades the noise performance of an LNA as it directly gets added to the total noise at the input. In the proposed solution, as shown in Fig. 19, the gate noise of the weak inversion (auxiliary) transistor is large. But since the gate of the auxiliary transistor is connected to the source of the main transistor, the gate noise of the auxiliary transistor gets added to the drain noise of the main transistor which when reflected to the input gets divided by the gain of the LNA and hence resulting in a negligible effect on the overall noise figure.

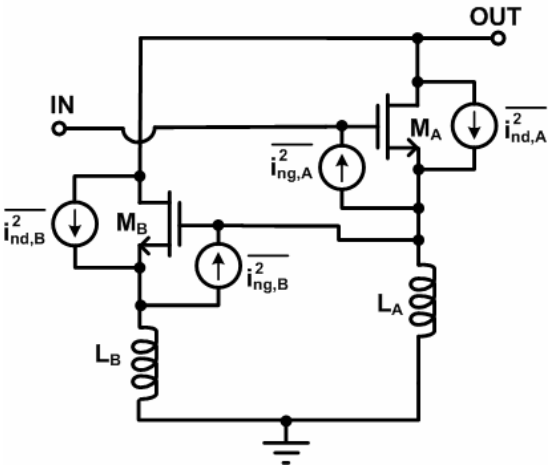


Fig. 19. Noise sources.

The effect on NF due to auxiliary transistor is simulated and shown in Fig. 20 below. It can be seen that the NF has degraded by 0.3 dB due to addition of auxiliary transistor. This drop can be attributed due to the lossy inductor L_B, and hence noise contribution due to the auxiliary transistor as explained in Fig. 19 is negligible.

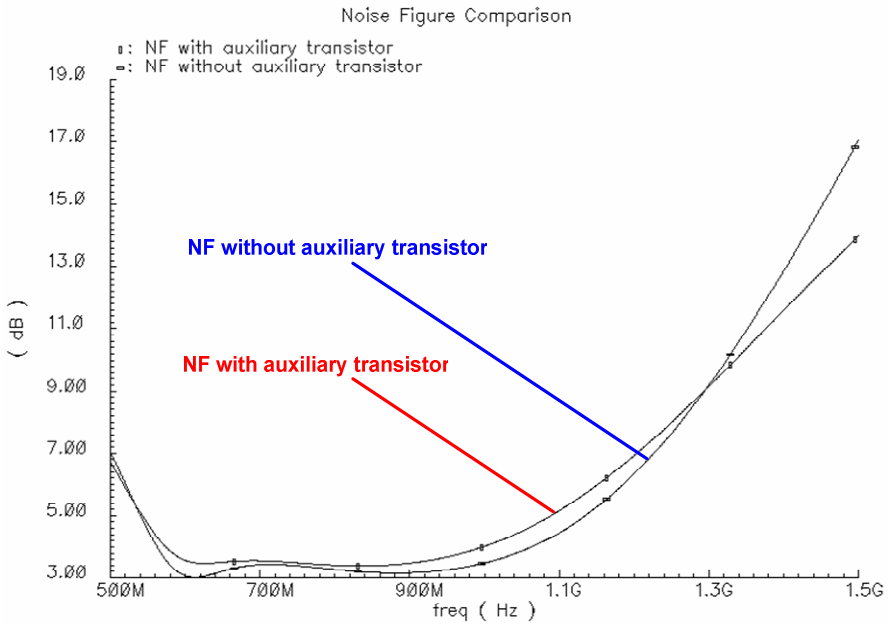


Fig. 20. Effect on NF.

As explained above, the proposed solution achieves high linearity without losing out on any of the specifications of gain, noise figure (NF) and at the expense of very minimal additional power.

2.5 BOTTLENECK FOR FURTHER IMPROVEMENT

In the proposed solution described in the previous section, the currents at the drain of the main input transistor and the auxiliary transistor are added to cancel the IM3 components.

This current flows through the cascode transistor before flowing into the output. Though the cascode transistor is ideally assumed to be a linear device, the parasitic capacitances at RF frequencies would result in a non-linear cascode transistor thus resulting in a slight degradation of linearity. An alternate topology in which the drain of the auxiliary transistor is directly connected to the drain of the cascode transistor thus canceling the IM3 components at the output is shown in Fig. 21.

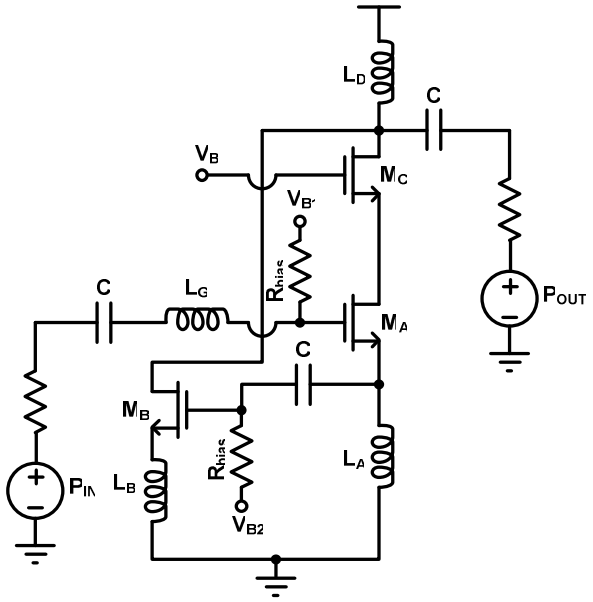


Fig. 21. Alternate proposed solution.

The topology described above cancels the non-linearity associated with the cascode transistor thus achieving even higher levels of linearity than that possible using the topology in which the drains of the main and auxiliary transistors are connected. But the disadvantage with such a topology is that since the auxiliary transistor is directly connected to the output, the signal swing across the gate and drain of the auxiliary transistor is very large. This results in a huge equivalent capacitor at the input of the

auxiliary transistor due to miller effect of the parasitic C_{gd} capacitor thus affecting the input matching. Hence, as the output impedance varies, the gain and the signal swing at the output vary, resulting in a different capacitor value at the input of auxiliary transistor due to the miller effect described above. This results in a different optimum linearity point. This problem might be solved by having a cascode transistor on top of the auxiliary transistor.

3. RESULTS

The proposed Linear LNA has been designed and simulated in the TSMC 0.35µm CMOS technology. All the inductors have been simulated using the ASITIC software and pi-model has been used to model the inductors.

Two circuits have fabricated in TSMC 0.35µm CMOS technology. The first version (LNA1) has the Linear LNA circuit alone and hence would be terminated with a 50Ω load of the port and hence an ideal platform to test the proposed cancellation technique. The second version (LNA2) has a buffer connected to the output of LNA and hence the LNA sees a high impedance load at its output. The buffer models a high impedance load to the LNA which is usually followed by a mixer in a receiver. This presents an ideal platform to test for linearity of LNA in realistic conditions with high gain. The following sections describe the various simulation and experimental results obtained in both the versions.

Section 3.1 describes the simulation results for the second version of LNA with an in-built buffer. It also describes how the LNA specifications are de-embedded from that of the LNA-Buffer combination. Section 3.2 and 3.3 described the simulation and experimental results respectively of the first version of stand alone LNA. A testing strategy to improve the gain of LNA is also discussed.

3.1 LINEAR LNA WITH BUFFER

This section describes the schematic and the simulation results of the Linear LNA with a buffer connected to its output.

3.1.1 Circuit setup

In a transmitter, the LNA is usually followed by a mixer and thus has a high impedance load at its output. To simulate the same effect, a buffer is connected to the output of LNA. If two gain stages are connected in series, the linearity of the second stage dictates the overall linearity performance. Hence the buffer is source degenerated with a 50Ω resistance to achieve higher linearity than the LNA so that the IIP3 of the LNA can be de-embedded from the overall IIP3. This results in a lossy buffer and the source degeneration resistor adds noise at the output. But these results can be easily de-embedded by having a stand alone buffer. The final schematic of the LNA used is shown in Fig. 22 below.

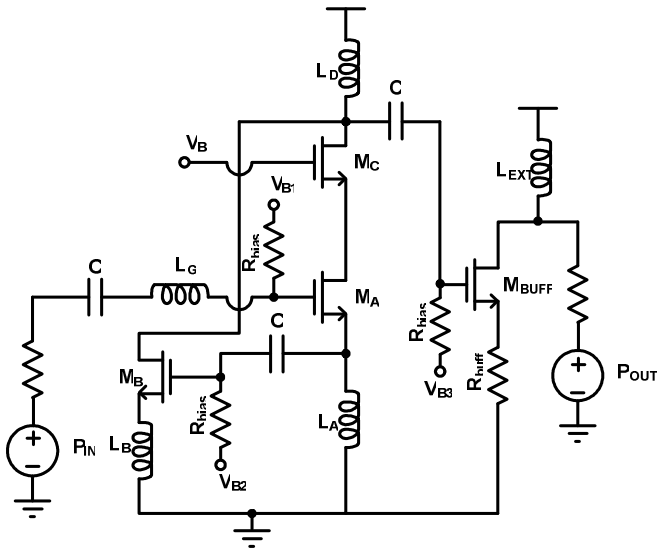


Fig. 22. Whole schematic of LNA with buffer.

The LNA has been tuned for high IIP3 performance using the plot shown in Fig. 15. Table-2 shows the final aspect ratios of different transistors and the values of inductors used for both LNA and buffer as shown in Fig. 22.

Table 2. Component design values of LNA with buffer

Component	Value
M_A	10 µm/0.4 µm, m=30
M_C	10 µm/0.4 µm, m=6
M_B	10 µm/0.4 µm, m=45
M_{Buff}	10 µm/0.4 µm, m=8
L_G	30 nH
L_A	4.65 nH
L_B	1.05 nH
L_D	10 nH
L_{EXT}	10 nH
R_{buff}	50 Ω
I_A	4.85mA
I_B	0.69mA
I_{buff}	8.84mA

3.1.2 Layout

The layout of the Linear LNA was drawn using the Virtuoso layout editor in CADENCE. The picture of the final layout is shown in Fig. 23. The following steps have been taken while drawing the layout. To minimize the parasitic capacitance added to the LNA, the drain of the input transistor which is shared with the source of the cascode transistor has been drawn without any contacts. Since no output is taken out of this node, the size of this node can be minimized in layout hence decreasing the capacitance added. The input transistor and the cascode transistor are inter-fingered with multiple fingers to minimize the process variations. The auxiliary transistor is drawn with multiple fingers with the

smallest transistor being the same size as that of the input transistor hence resulting in same values of parameters in both the cases.

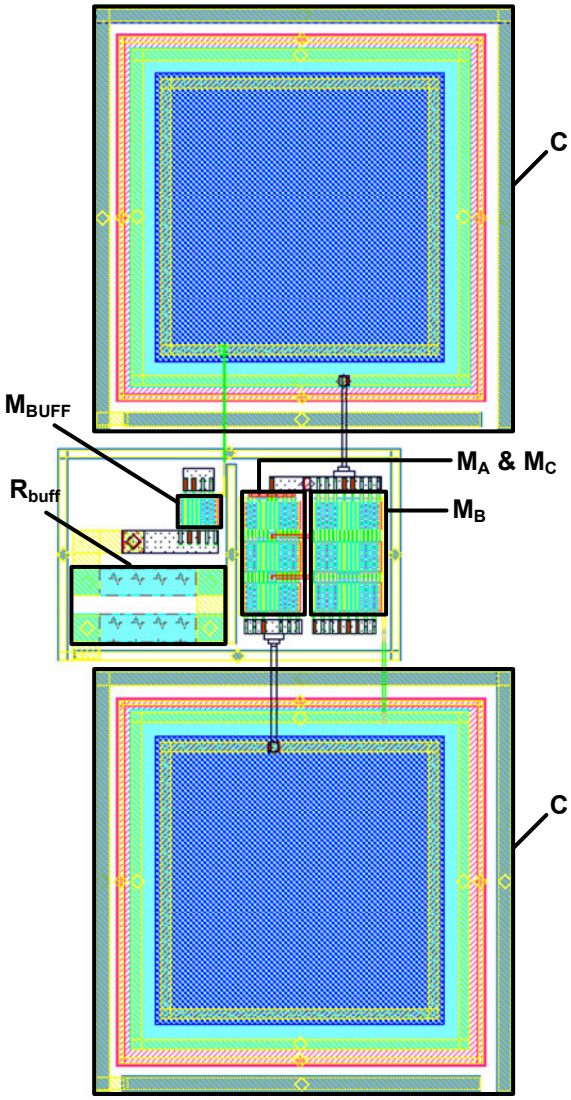


Fig. 23. Picture of layout.

The inductors are drawn using ASITIC and imported into CADENCE. The inductors are drawn in the topmost metal layer (metal4) to be far away from substrate and hence achieving higher Q. The inductors are shielded on all sides using broken segments of

both n-well and p-substrate contacts connected to supply and ground respectively to improve the inductor performance [22] as shown in Fig. 24. Fig. 24 also shows the inductor pi-model used for modeling the Q of the inductors and the losses to the substrate during simulations.

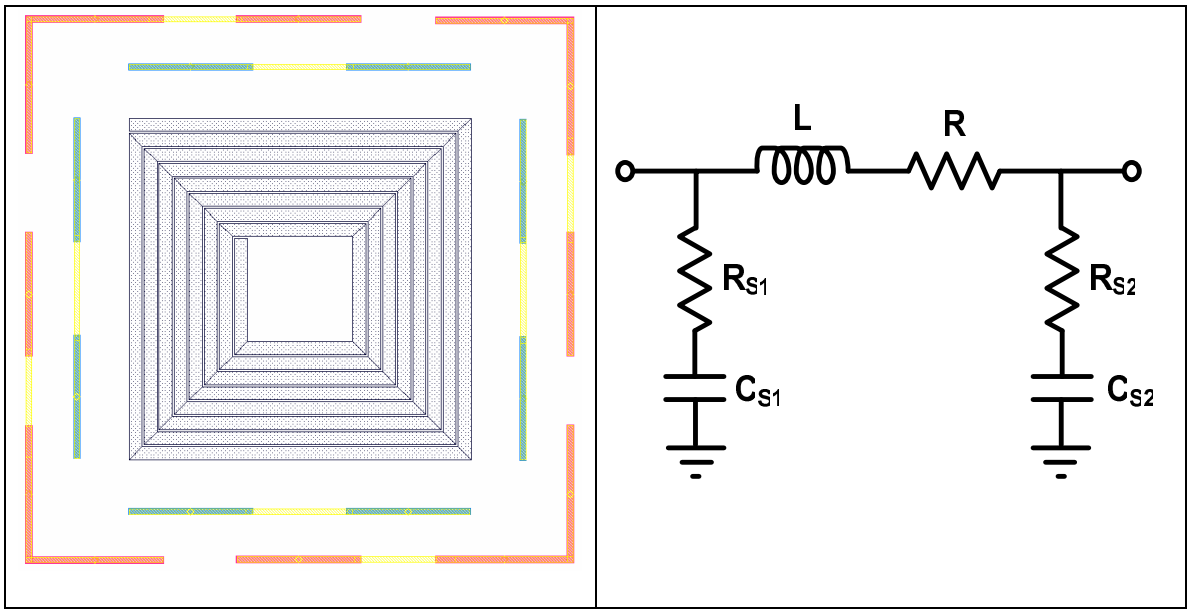


Fig. 24. Inductor layout and inductor model.

3.1.3 Simulation results

The post-layout simulation results of the Linear LNA with the buffer are shown in this section. The results of stand alone buffer are shown and the results of LNA are obtained from these results.

The input matching of the LNA is shown by the S_{11} plot and the power gain is shown by S_{21} plot. Matching is essential in an LNA so that maximum signal power gets to the input of LNA. An S_{11} less than -10dB at the frequency of interest is necessary for maximum

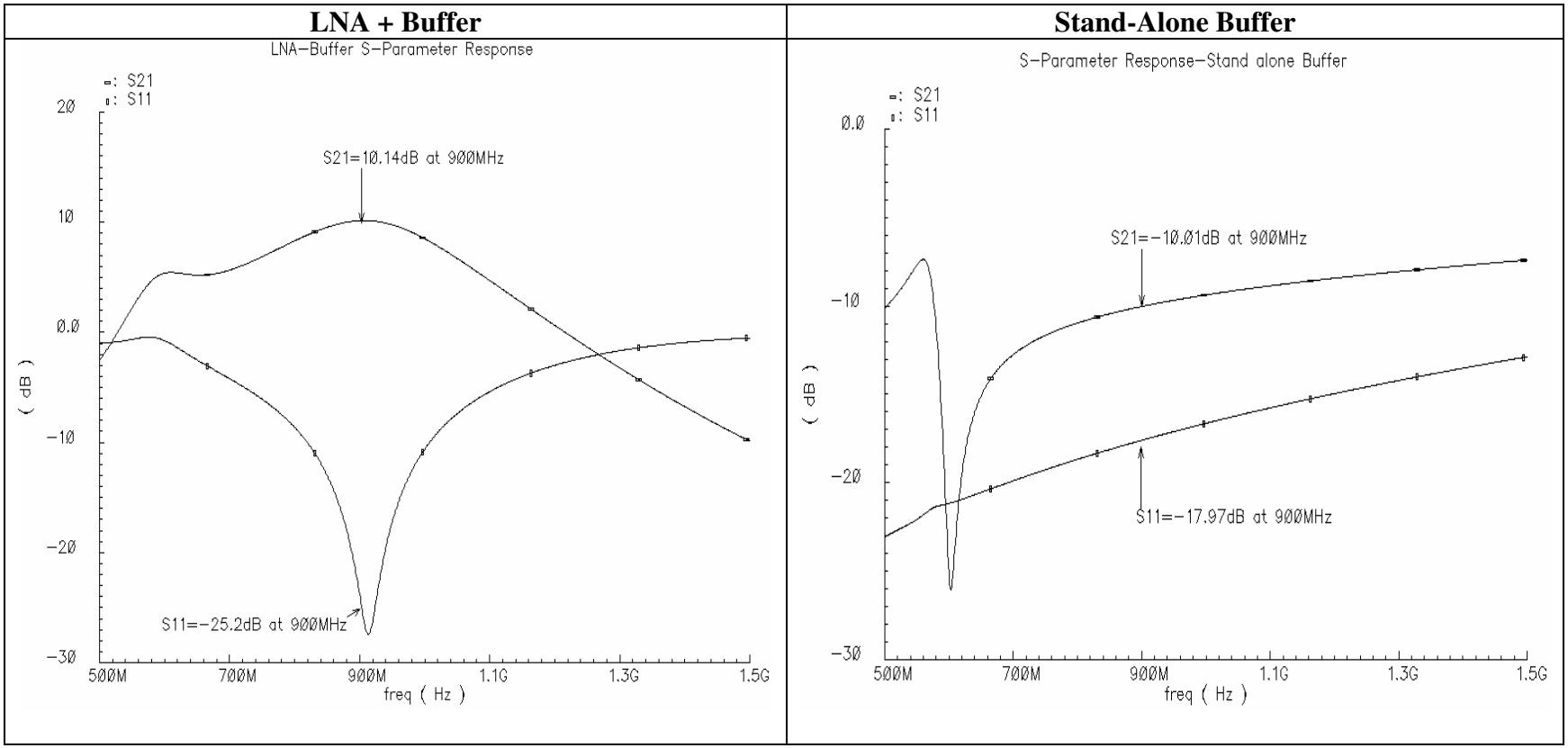


Fig. 25. Input match and power gain plots.

signal power at the input of LNA. Fig. 25 shows the matching and the power gain obtained in the case of LNA and buffer combination and the stand alone buffer.

The power gain of the LNA from the above plots is found to be 20.14dB at 900MHz. The AC voltage gain and the power gain are the same if both the input and output are properly matched to 50Ω. The following AC voltage gain plot shows the voltage signal at the input of LNA, output of LNA and at the output of buffer over a frequency range.

It can be seen from Fig. 26 that the voltage gain at 900MHz of the LNA alone is 19.9dB, the overall gain of LNA and buffer is 10.14dB and the loss due to buffer is 9.5dB which is close to the results predicted by the power gain proving that the matching is good enough.

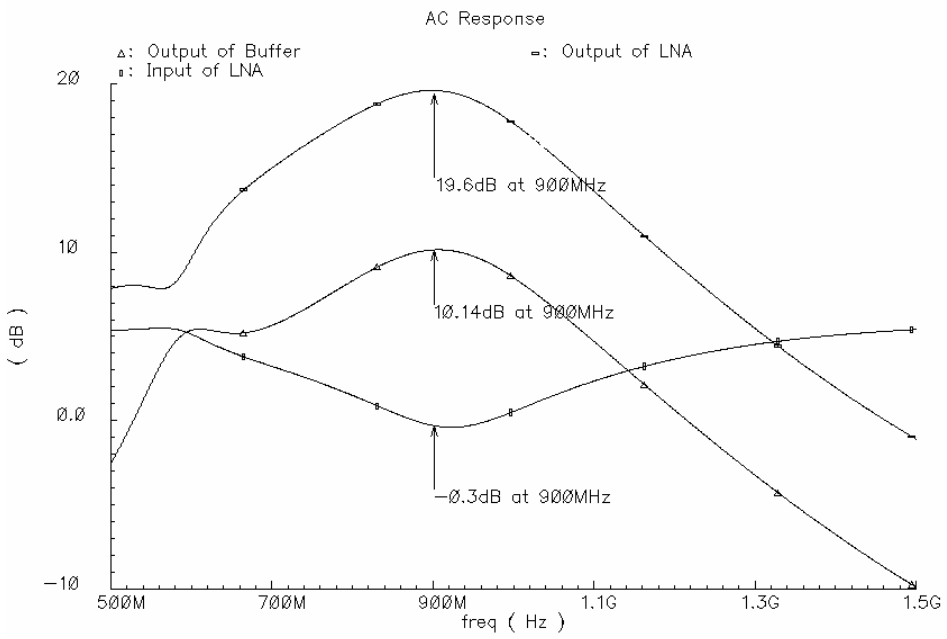


Fig. 26. AC voltage gain of LNA and buffer.

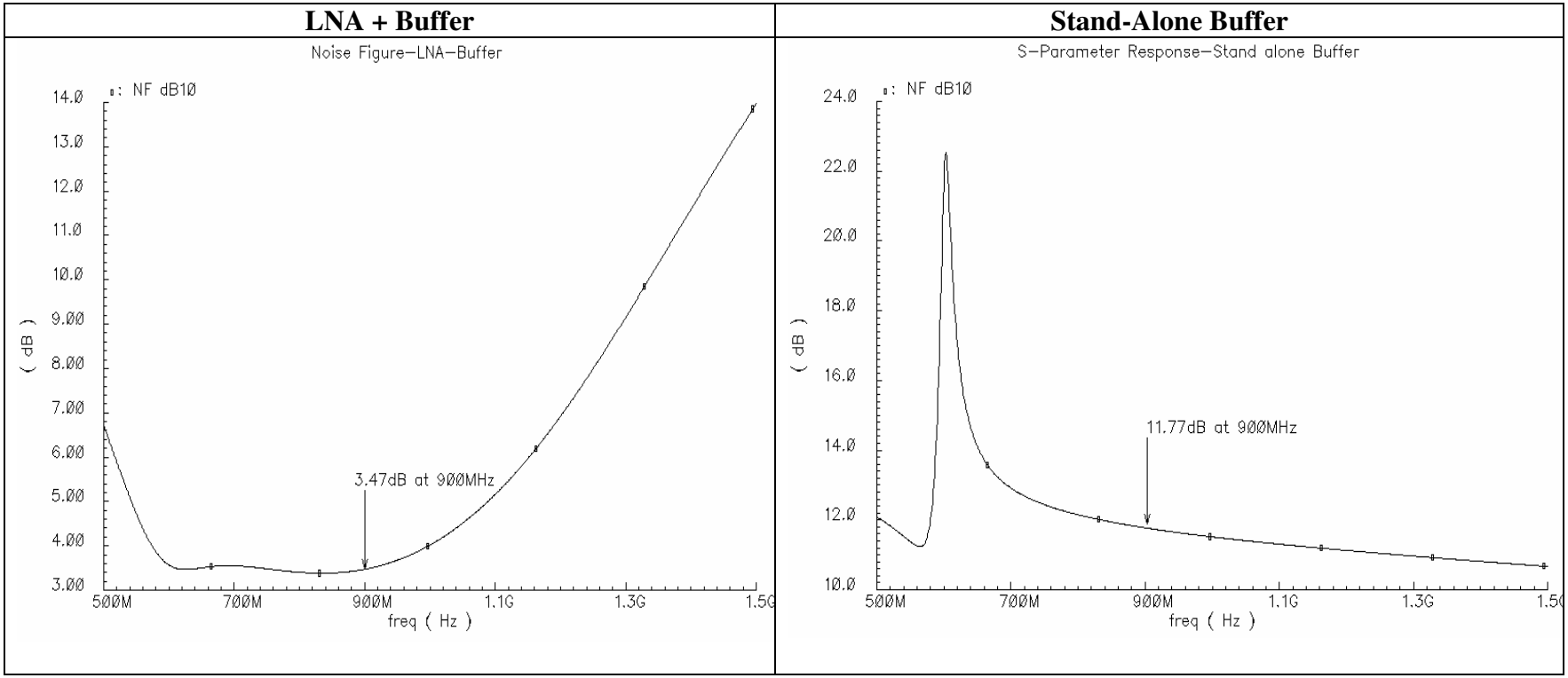


Fig. 27. NF plots.

Fig. 27 shows the noise performance of the LNA. The Noise Figure (NF) of an LNA is used to indicate the noise performance of an LNA.

As shown in Fig. 27, the NF of the stand alone buffer is very high due to the lossy nature of the buffer and more over the source degeneration resistor (50 Ω) adds lot of noise. The NF of the LNA and buffer together is 3.47dB at 900MHz. The NF of the stand alone LNA from the above results is found to be 2.07dB. The NF is high due to the poor performance of inductors in 0.35µm technology. The Q of inductors in 0.35µm technology is found to be in the order of 2.5 thus making the inductors quite lossy and noisy. The poor NF can be attributed to this factor.

The linearity of an LNA is measured in terms of its IIP3. As described in section 2, high linearity is achieved by canceling the IM3 component of current in the auxiliary transistor to be of same magnitude and opposite in phase with the IM3 component of current in main transistor. Fig. 28 shows the magnitude and phase of IM3 component currents in both main and auxiliary branches for input frequency tones at 895MHz and 905MHz. This generates IM3 components at 885MHz and 915MHz.

Fig. 28 shows the magnitude and phase of IM3 tones at 885MHz in both main and auxiliary branches. As shown in the figure, the IM3 tones in both the branches are equal in magnitude and opposite in phase over the input power range of -60dBm to -50dBm and thus are cancelled at the output.

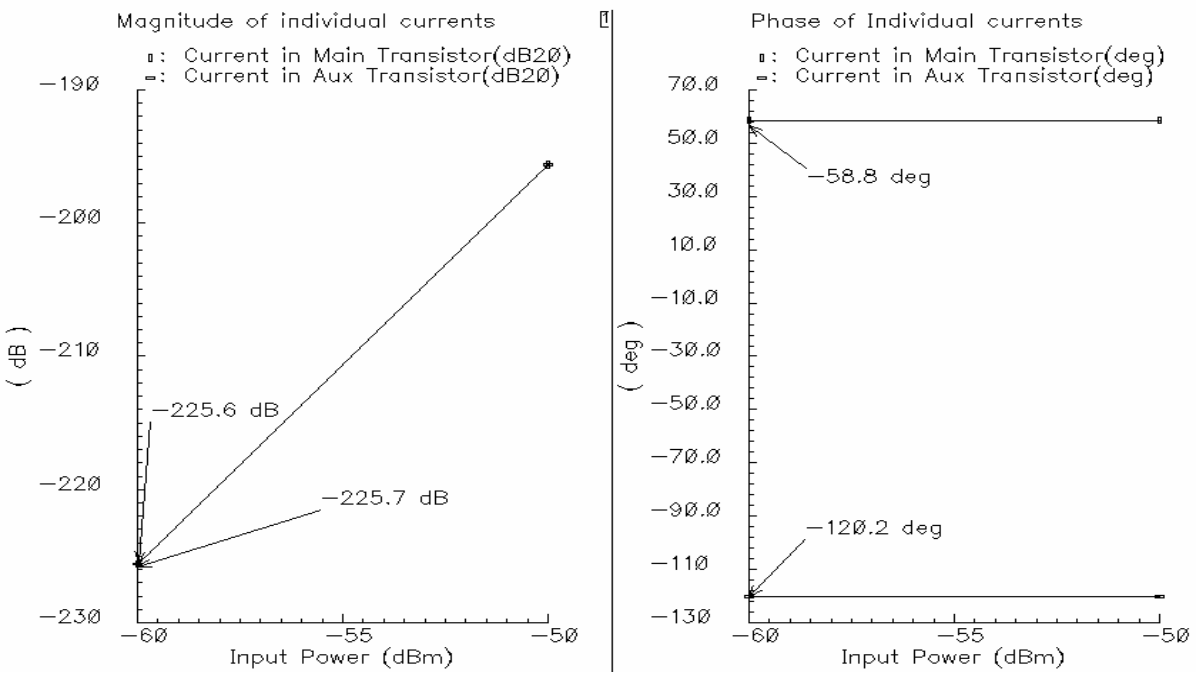


Fig. 28. Phase cancellation of IM3 currents.

Fig. 29 shows the magnitude of fundamental and IM3 tones at the output of LNA and at the output of stand-alone buffer. The IIP3 can be found from the above graph as follows [23].

$$IIP3(dBm) = P_{in} + \frac{P_f - P_{IM3}}{2}$$
$$where\ P_{in} = Total\ Signal\ Input\ Power \quad (18)$$
$$P_f = Total\ Signal\ Output\ Power$$
$$P_{IM3} = Total\ IM3\ tone\ Output\ Power$$

The IIP3 of LNA using (18) is found to be 19.6dBm and that of the stand-alone buffer to be 26.6dBm. Since the linearity of buffer is much higher than that of LNA, the IIP3 of LNA can be de-embedded from the LNA-Buffer combination.

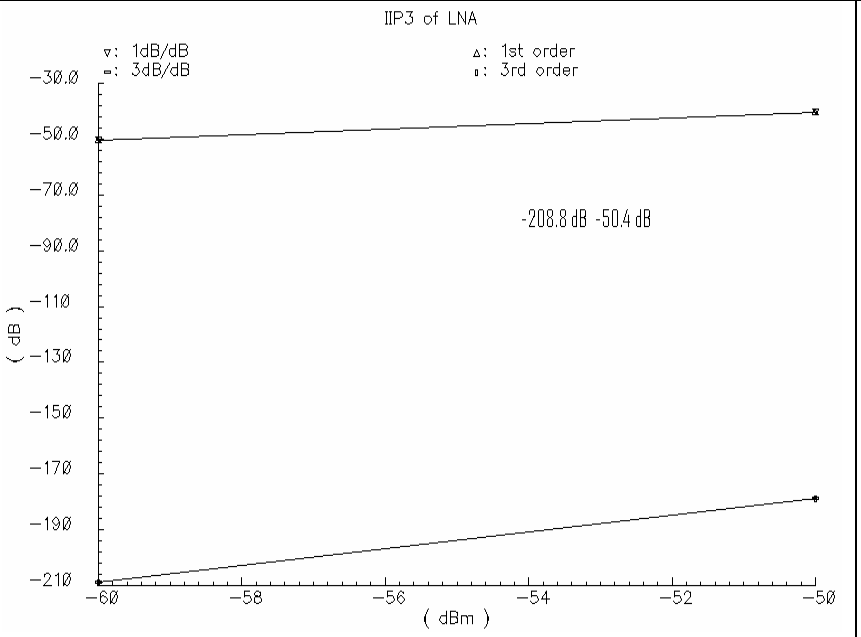
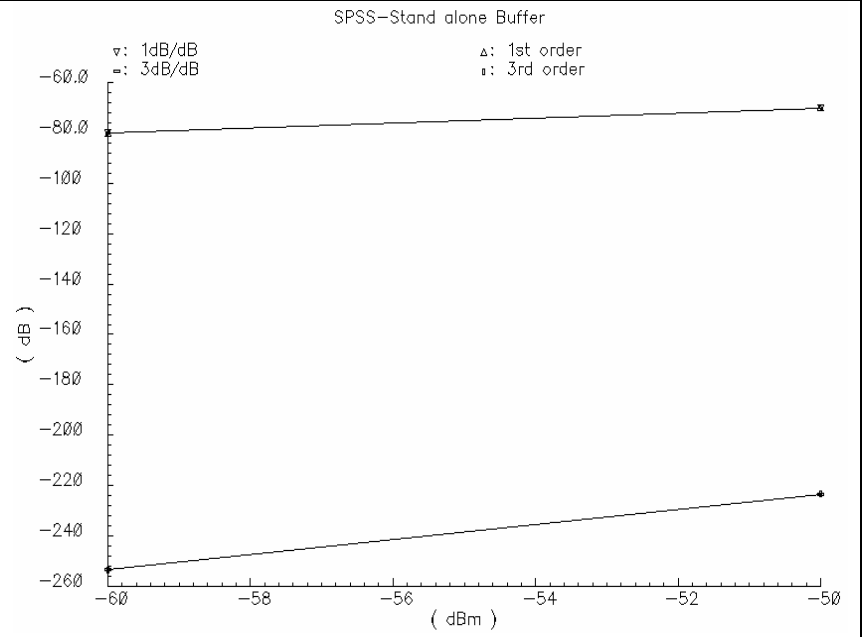
IIP3 of LNA	IIP3 of Stand-Alone Buffer
	

Fig. 29. IIP3 measurement.

Table-3 summarizes the simulation results of LNA and Buffer obtained.

Table 3. Summary of simulation results

Specification	LNA + Buffer	Buffer	LNA
IIP3 (dBm)	7.45	26.85	19.56
Gain (dB)	10.14	-10.01	19.9
NF (dB)	3.47	11.77	2.07
Power (mW)	35.92	22.09	13.83

3.2 LINEAR LNA WITHOUT BUFFER

This section describes the simulation results and a strategy to improve the gain of the stand alone LNA fabricated. In this case the LNA sees the output impedance of the port which is usually 50Ω.

3.2.1 Circuit setup

A stand alone LNA as shown in Fig. 30 was fabricated in TSMC 0.35µm CMOS technology. This circuit was fabricated to test the proposed linearization technique. In this case the LNA sees the output impedance of the port of 50Ω and hence the gain of LNA is reduced. The gain of LNA can be improved by increasing the impedance seen by the LNA by adding a resistor in series with the output port which is explained in the following sections.

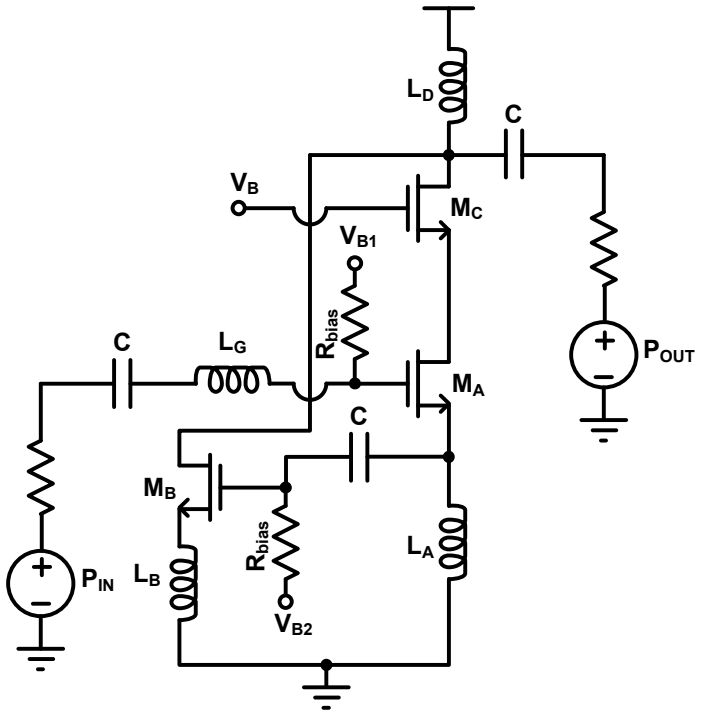


Fig. 30. Schematic of LNA without buffer.

The component values of the designed LNA shown in Fig. 30 are listed in Table 4.

Table 4. Component design values of LNA without buffer

Component	Value
M_A	24 µm/0.4 µm, m=16
M_C	24 µm/0.4 µm, m=16
M_B	24 µm/0.4 µm, m=36
L_G	30 nH
L_A	5 nH
L_B	1.05 nH
L_D	10 nH
I_{main}	4.68mA
I_{aux}	0.84mA

3.2.2 Layout

The layout of the schematic shown in Fig. 30 is shown in Fig. 31 below. The layout has been drawn using the VIRTUOSO tool in CADENCE. The capacitor shown in the layout is the coupling capacitor connected between the source of main transistor and the gate of auxiliary transistor. The main transistor and the cascode transistor have been inter-fingered. The auxiliary transistor is multi fingered with the minimum finger size to be same as that of the main transistor to minimize process variations.

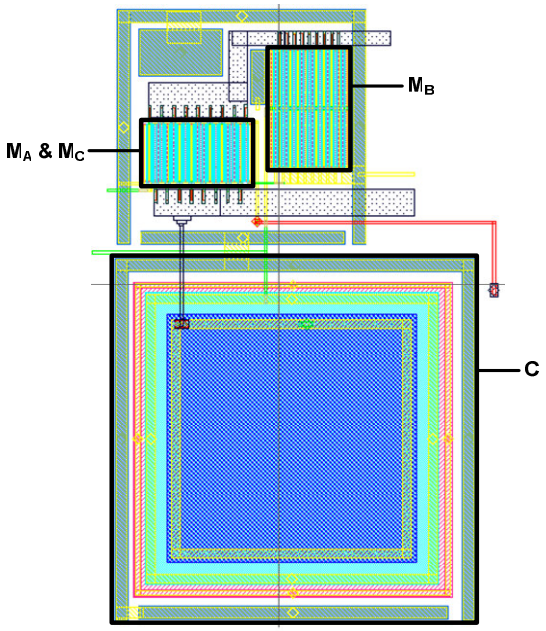


Fig. 31. Layout of LNA without Buffer.

3.2.3 Simulation results

The post layout simulation results of the LNA are shown below. The LNA has been simulated with the output terminated with the 50Ω impedance of the port. Fig. 32 shows the input match (S_{11}) and the power gain (S_{21}) obtained over various different

frequencies. S_{11}<-10dB is desired for maximum input power transfer. It can be seen from Fig. 32 that S_{11} is -25.77dB at 900MHz. The S_{21} obtained is 8.45dB mainly due to the 50Ω output termination.

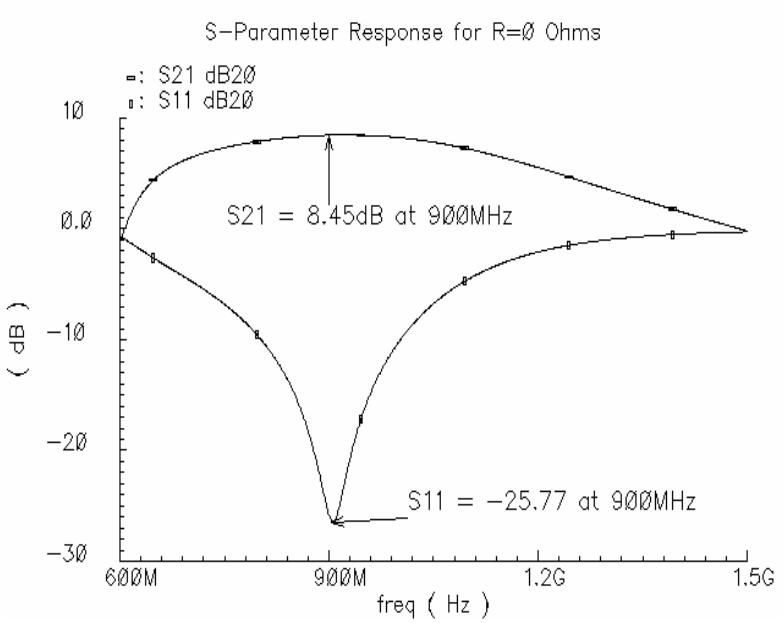


Fig. 32. S-parameter analysis of LNA.

Fig. 33 shows the plot of Noise Figure (NF) over different frequencies. It can be seen that the NF dips around 900MHz due to good input impedance matching at that frequency. A Noise Figure of 3.35dB is obtained at 900MHz. The NF obtained is high due to reduced gain in the LNA and also due to lossy inductors with high series resistance as explained in the previous section.

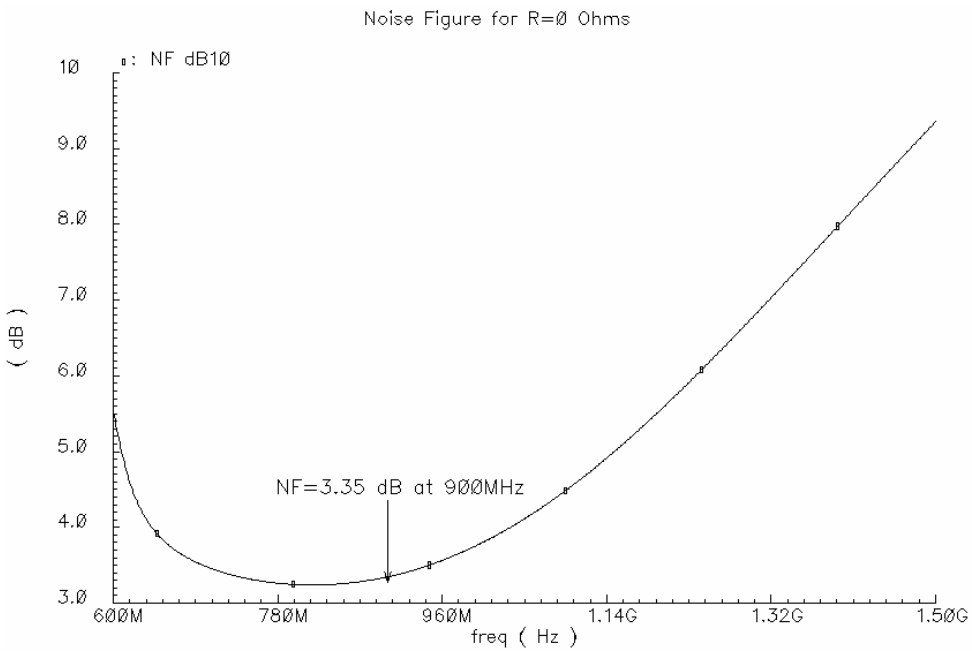


Fig. 33. NF measurement of LNA.

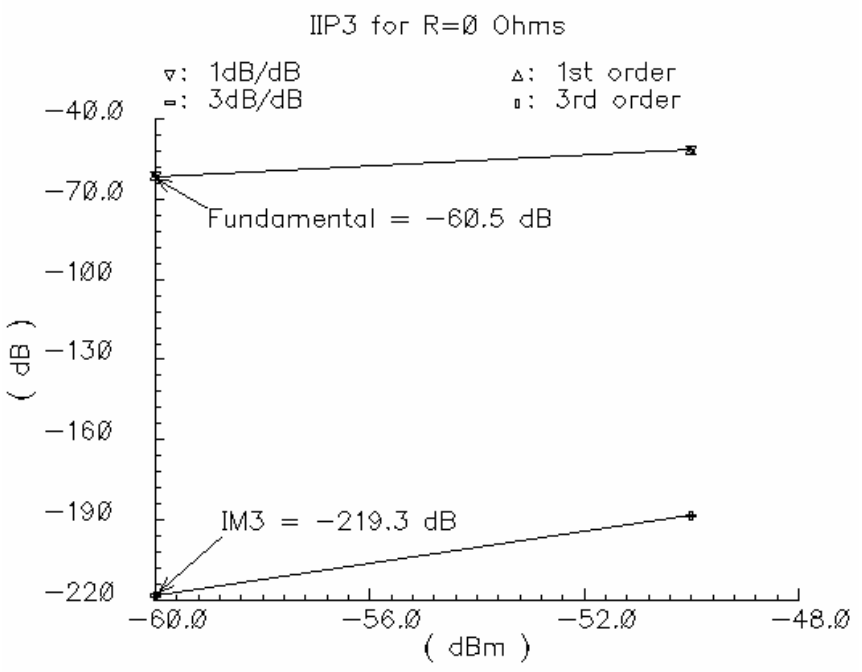


Fig. 34. IIP3 measurement of LNA.

Fig. 34 shows the linearity measurement of the LNA done with the two tone test. Since the LNA output peaks at 900MHz, the input to LNA consisted of two tones at 895MHz and 905MHz such that one of the IM3 tones generated due to the non-linearity of the LNA fall on the band of interest at 900MHz. The input power of the tones was swept from -60dBm to -50dBm and Fig. 34 shows the power of the fundamental tone (895MHz) and the IM3 component (900MHz) for different input powers. The IIP3 obtained can be calculated using (18) and is found to be 19.8dBm.

3.2.4 Strategy to improve LNA gain

The LNA shown in Fig. 30 sees the 50Ω impedance of the port leading to reduced gain. To increase the gain of the LNA, a resistor 'R' is placed in series with the decoupling capacitor and then connected to the output port as shown in Fig. 35. Here the LNA sees a total output impedance of (R+50) Ω, thus increasing the output impedance and hence increasing the gain at the output of LNA. But the signal at the output port (V_{out}) would be attenuated by 50/(R+50) times the original signal at the output of LNA. Hence assuming this resistance to be a linear component, the gain of the LNA can be extrapolated by adding the attenuation factor to the measured gain. The resistive divider stage being a linear element should not affect the linearity of the LNA. Also, since the internal nodes of LNA would see a large signal swing, this would also prove to be an ideal test for linearity.

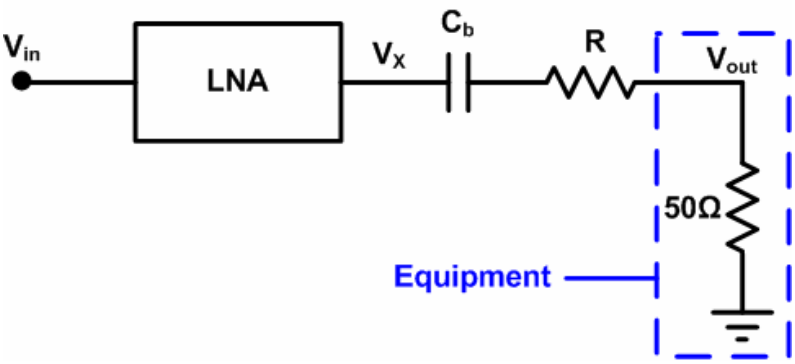


Fig. 35. LNA testing strategy to improve gain.

Table 5 summarizes the simulation results obtained for different values of resistance 'R' shown in Fig. 35. It can be seen that the LNA gain improves for higher values of R. But the gain saturates for large values of 'R' at which the impedance of the load inductor and parasitic capacitors are no longer negligible. There is no improvement in the NF of LNA even with increased gain. This is because of additional noise contribution of the resistance 'R' to the output. The degradation in IIP3 as mentioned above is very minimal and can be improved by slightly tuning the bias voltages.

Table 5. Summary of simulation results with different resistors

	R=0 Ω	R=25 Ω	R=50 Ω	R=75 Ω	R=100 Ω
S_{11} (dB20)	-25.77	-24.35	-23.1	-21.83	-20.87
S_{21} (dB20)	8.47	7.28	6.21	5.23	4.34
Gain (dB20)	8.47	10.97	12.49	13.5	14.24
IIP3 (dBm)	19.8	18.8	18.3	18	18
NF (dB)	3.35	3.41	3.47	3.52	3.58

3.3 EXPERIMENTAL RESULTS

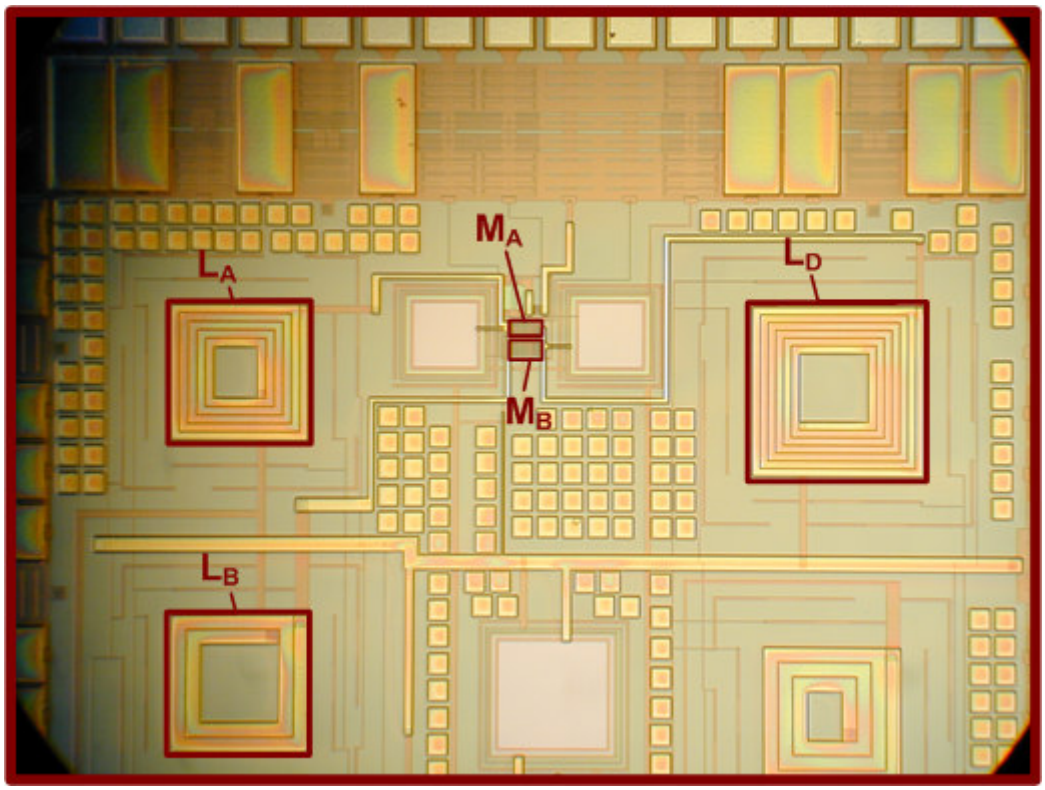


Fig. 36. LNA chip microphotograph.

The LNA described in section 3.2 has been experimentally verified for its functionality and the various results obtained are described below. The chip microphotograph of the LNA is shown in Fig. 36. It can be seen that all inductors other than the gate inductor are built on-chip.

The strategy described in section 3.2 to improve the gain of LNA has been incorporated during testing. The following sections describe the testing results obtained for different values of R of 0Ω, 75Ω and 100Ω.

3.3.1 Experimental results with R=0 Ω

Initial testing was carried with the output of LNA directly connected to the output port (R=0). As shown in Fig. 37, this resulted in S_{11} of -16dB at 950MHz and S_{21} of 4.5dB. The LNA was tested for linearity with two input tones at 940MHz and 945MHz and the IIP3 of 20dBm was obtained.

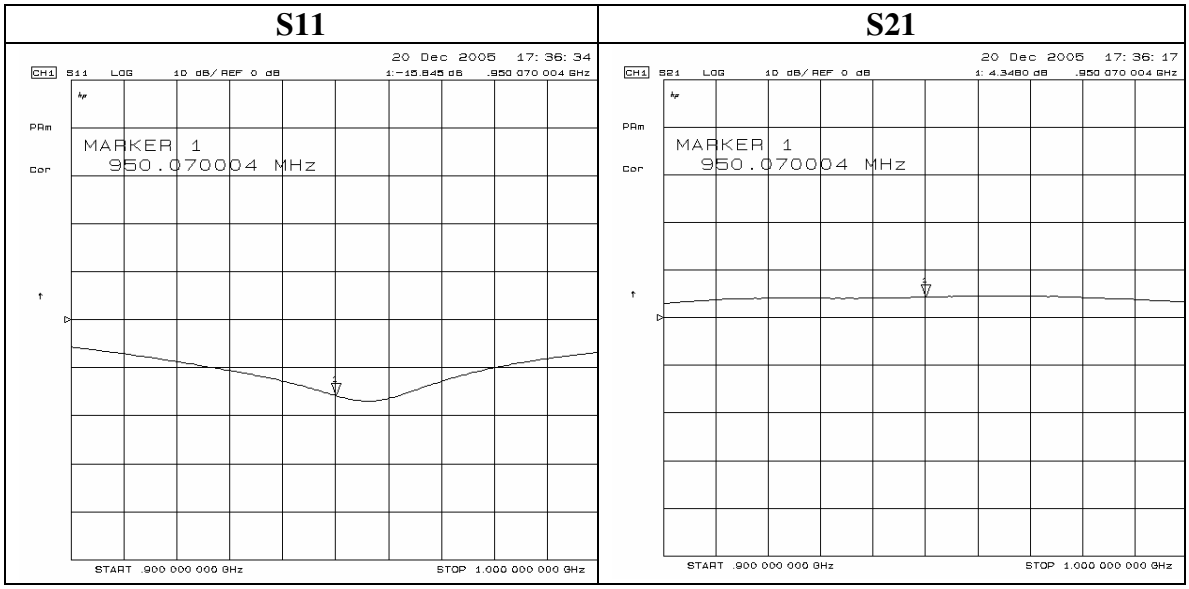


Fig. 37. S-Parameter measurement for R=0Ω.

3.3.2 Experimental results with R=75 Ω

The following experimental results are with a resistance R=75Ω in series with the output port. Fig. 38 shows the input impedance matching (S_{11}) obtained in this case. It can be seen that S_{11} is less than -10 dB over a range of frequencies from 925MHz to 955MHz. Fig. 38 also shows the S_{21} obtained at 50 ohms port. It can be seen that the measured gain after the voltage divider is approximately 1.5dB. Due to the 75Ω resistor, the signal at the output port is 0.4 times (50/(50+75)) the signal at the output of LNA as explained

before. Hence the attenuation is by 2.5 times which is 8dB. Hence the actual gain at the output of LNA would be 9.5dB.

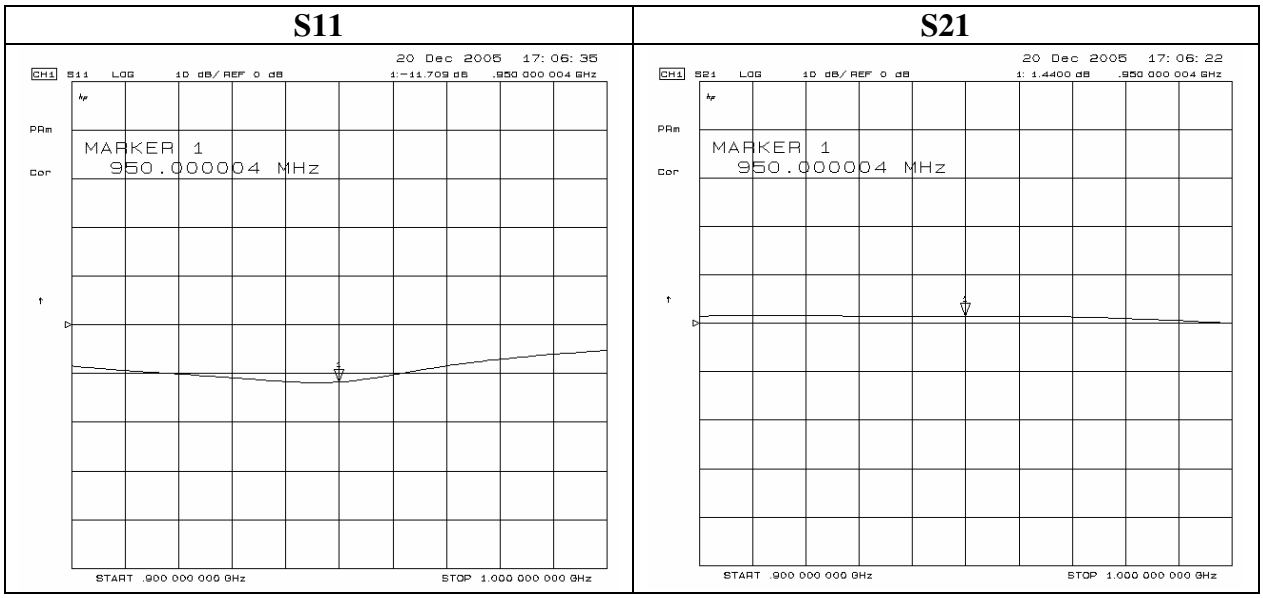


Fig. 38. S-Parameter measurement for R=75Ω.

Fig. 39 shows the power spectrum at the output of LNA for input tones at 940MHz and 945MHz of power -10dBm, which produces IM3 tones at 935MHz and 950MHz of which 950MHz falls on the band of interest. The frequency spectrum for the case described above with the tones at 945MHz and 950 MHz is shown in Fig. 39.

Using (19), the IIP3 can be calculated.

$$IIP3(dBm) = P_{in} + \frac{P_f - P_{IM3}}{2}$$
$$where\ P_{in} = Total\ Signal\ Input\ Power \tag{19}$$
$$P_f = Total\ Signal\ Output\ Power$$
$$P_{IM3} = Total\ IM3\ tone\ Output\ Power$$

From Fig. 39, the following values can be obtained.

P_{in}=-10dBm (Total signal power at the input of LNA)

P_f= -16.2dBm (Power of fundamental tone (945MHz) at the output port)

P_{IM3}=-78.07dBm (Power of IM3 tone (950MHz) at the output port).

For a total signal input power (P_{in}) of -10dBm at the input of LNA, using (18) the IIP3 for the above values is found to be 20.93dBm.

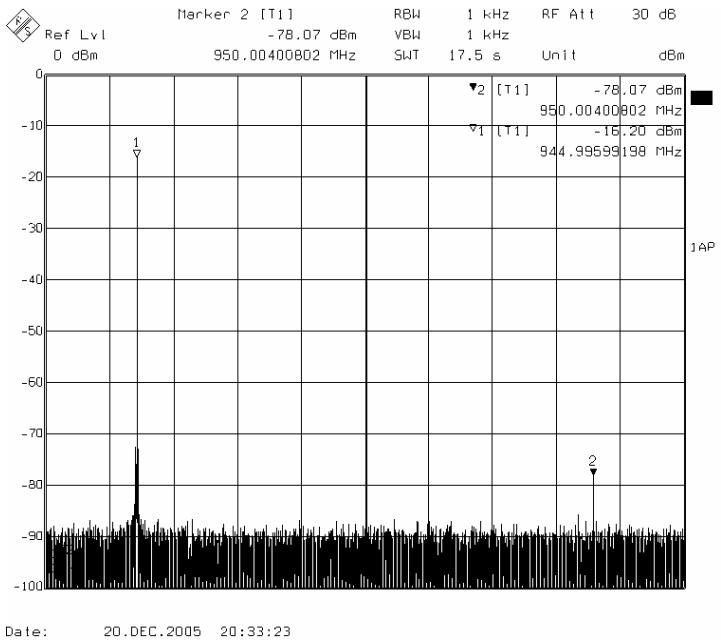


Fig. 39. IIP3 measurement for R=75Ω.

Fig. 40 shows the variation in the power of fundamental (945MHz) and IM3 tones (950MHz) at the output with varying input power. This plot is used to measure the IIP3 of the LNA.

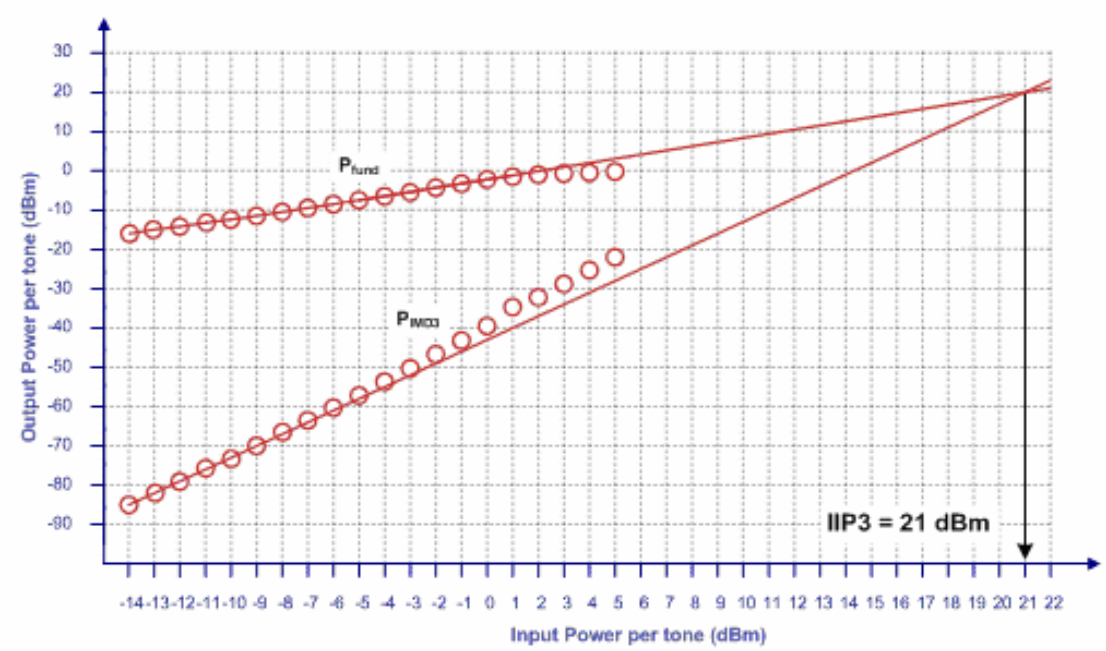


Fig. 40. Experimental IIP3 characterization R=75Ω.

3.3.3 Experimental results with R=100 Ω

The following experimental results are with a resistance R=100Ω in series with the output port.

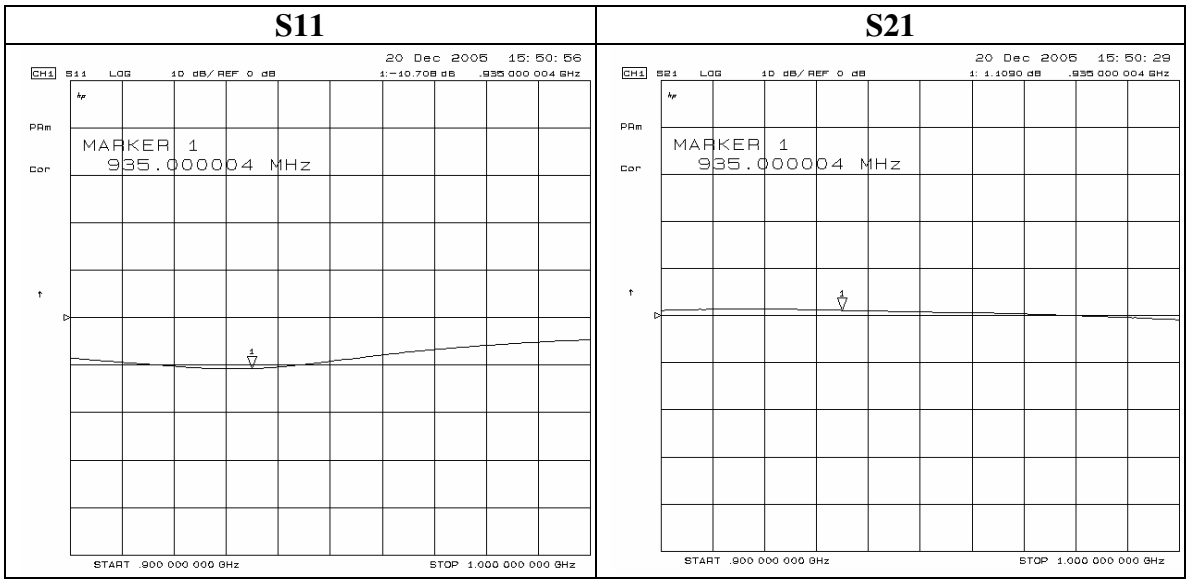


Fig. 41. S-Parameter measurement for R=100Ω.

It can be seen from Fig. 41 that an S_{11} of -10.7dB can be achieved with an S_{21} of 1.1dB. Due to the 100Ω resistor, the signal at the output port is 0.333 times the signal at the output of LNA as explained before. Hence the attenuation is by 3 times which is 9.5dB. Hence the actual gain at the output of LNA would be 10.6dB.

Fig. 42 shows the power spectrum at the output for two input tones at 940MHz and 945MHz. The power of both fundamental (940MHz) and IM3 (935MHz) tones is shown.

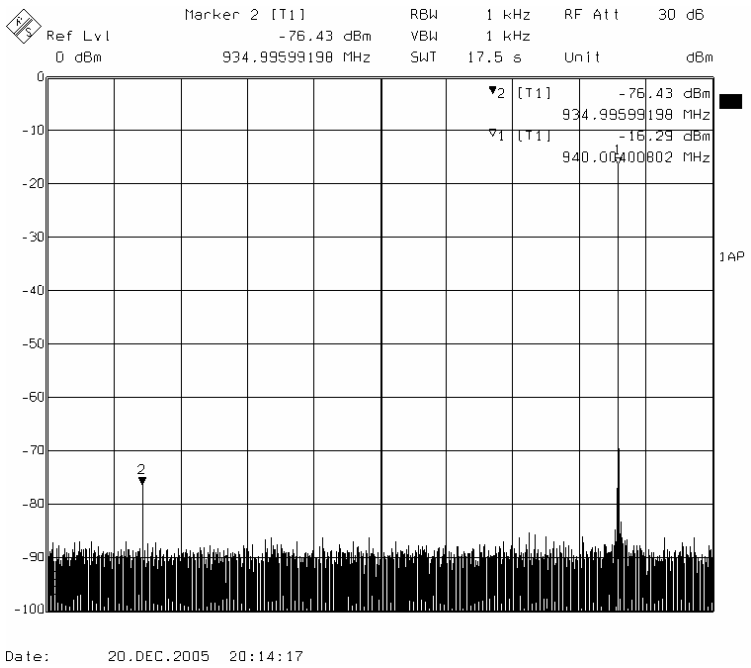


Fig. 42. IIP3 measurement for R=100Ω.

From Fig. 42, the following values can be obtained to calculate IIP3 using (19).

P_{in}=-10dBm (Total signal power at the input of LNA)

P_f= -16.29dBm (Power of fundamental tone (945MHz) at the output port)

P_{IM3}=-76.43dBm (Power of IM3 tone (950MHz) at the output port)

For a total signal input power (P_{in}) of -10dBm at the input of LNA, using (18) the IIP3 for the above values is found to be 20.2dBm.

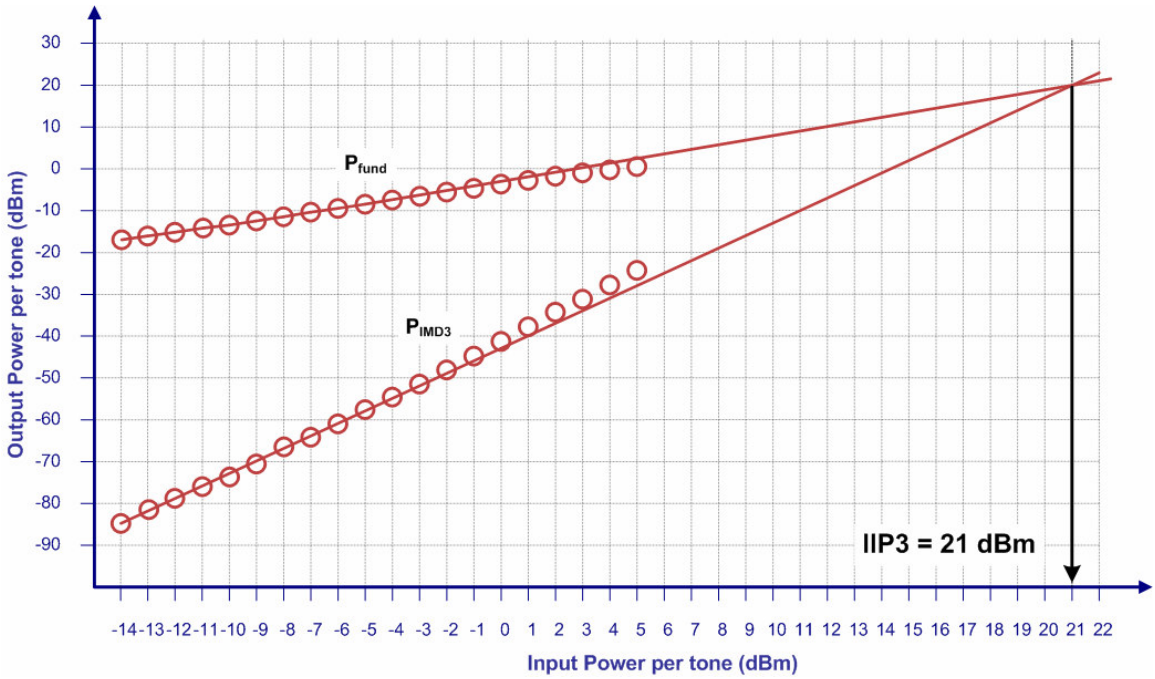


Fig. 43. Experimental IIP3 characterization for R=100Ω.

Fig. 43 shows the variation in the power of fundamental (945MHz) and IM3 tones (950MHz) at the output with varying input power. This plot is used to measure the IIP3 of the LNA.

The following table 6 summarizes the results obtained.

Table 6. Summary of experimental results for different values of R

R(Ω)	S11 (dB)	S21 (dB)	LNA Gain (dB)	IIP3 (dBm)
0	-15.85	4.4	4.4	20
75	-11.7	1.5	9.5	20.9
100	-10.7	1.1	10.6	21
150	-9.5	-0.5	11.5	20.5

It can be seen from the above table that with increasing values of ‘R’, the gain improvement in gain initially was significant and it saturates gradually due to the comparable impedance of load inductor in parallel with the resistive load. The IIP3 obtained was constant over different load impedances. Thus it can be concluded that the gain can be improved significantly by connecting a buffer load to the output and the value of IIP3 can be retained.

The following section compares the results obtained with other existing linearization techniques in the literature.

4. CONCLUSION

A novel highly linear Low Noise Amplifier (LNA) circuit has been proposed which uses the phase cancellation technique to achieve high linearity. The proposed solution uses an auxiliary transistor whose IM3 components are tuned to be equal in magnitude and opposite in phase to those in the main transistor. These two current components in the main and auxiliary branch are added to achieve high linearity. The circuit has been designed and fabricated in TSMC 0.35µm CMOS technology and experimentally verified. The circuit achieves an IIP3 of +21dBm with a gain of 11dB and power consumption of 9mA@2.5V. The table 7 shown below compares the results of the proposed solution to other existing topologies.

Table 7. Comparison of experimental results

Work	**Technology**	**Freq GHz**	**S21 dB**	**NF dB**	**IIP3 dBm**	**P_{dc} mW**
This Work	0.35um CMOS	0.95	11	2.95	21	22.5
[17]	0.18um RF CMOS	3	6.5	1.9	15	8.9
[19]	0.25um CMOS	0.9	15.5	1.65	22	24.2
[4]	0.25um CMOS	0.9	14.6	1.8	10.5	5.4
[11]	0.5um SiGe BiCMOS	0.88	15.7	1.4	11.7	11.7
[18]	0.25um CMOS	2.2	14.9	3	16.1	23.5
[16]	0.35um CMOS	0.9	10	2.8	15.6	21.1
[13]	0.35um CMOS	0.9	2.5	2.8	18	45

REFERENCES

[1] R. Meyer and A. Wong, "Blocking and Desensitization in RF Amplifier," *IEEE Journal of Solid-State Circuits,* vol.30, no. 8, pp. 944-946, Aug. 1995.

[2] D. Johns and K. Martin, *Analog Integrated Circuit Design*, New York, Wiley, 1997.

[3] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Trans. Circ. & Sys. I*, vol. 51, no. 2, pp. 319-328, Feb. 2004.

[4] V. Aparin, G. Brown, and L. E. Larson "Linearization of CMOS LNAs via optimum gate biasing,"*IEEE International Symposium on Circuits and Systems*, vol. IV, Vancouver, Canada, May 2004, pp. 748-751.

[5] G. Palumbo and S. Pennisi, "Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain," *Electronics Circuits and Systems*, 2001, vol. 1, 2-5 Sept. 2001, pp. 209 – 212.

[6] D.R. Webster, A.E. Parker, D.G. Haigh, and P.M. Radmore, "Device circuit interaction in the common source amplifier**,"** *IEEE International Symposium on Circuits and Systems*, 1994, vol. 5, London, UK, 30 May-2 June 1994, pp. 241 – 244.

[7] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[8] K.L. Fong and R.G. Meyer, "High-frequency nonlinearity analysis of common – emitter and differential-pair transconductance stages," *IEEE Journal of Solid-State Circuits*, vol. 33, issue 4, pp. 548 – 555, April 1998.

[9] K. L. Fong, "High-frequency analysis of linearity improvement technique of common-emitter trans-conductance stage using a low-frequency trap network," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1249-1252, Aug. 2000.

[10] P. Shah, P. Gazzerro, V. Aparin, R. Sridhara, and C. Narathong, "A 2GHz lowdistortion low-noise two-stage LNA employing low-impedance bias terminations and optimum inter-stage match for linearity," *Europ. Solid-State Circ. Conf.*, Stockholm, Sweden, Sept. 2000, pp. 213-216.

[11] V. Aparin and L.E. Larson, **"**Linearization of monolithic LNAs using low-frequency low-impedance input termination," *European Solid-State Circuits Conference*, 2003, Lissabon, Portugal, 16-18 Sept. 2003, pp.137 – 140.

[12] J.S. Fairbanks and L.E. Larson, "Analysis of optimized input and output harmonic termination on the linearity of 5 GHz CMOS radio frequency amplifiers**,"** *Radio and Wireless Conference*, Boston, MA, 10-13 Aug. 2003, pp. 293 – 296.

[13] Y.Ding and R.Harjani, "A +18dBm IIP3 LNA in 0.35um CMOS", *IEEE ISSCC*, Digest of Technical Papers, San Francisco, CA, pp. 162-163, Feb. 2001.

[14] D.R.Webster, D.G.Haigh, J.B.Scott and A.E.Parker, "Derivative Superposition – a linearization technique for ultra broadband systems," in IEE Colloq. On Wideband Circuits Modeling & Techniques, May 1996, pp. 3/1-3/14.

[15] B.Kim, J.S.Ko, and K.Lee, "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," IEEE Microwave & Guided Wave Letters, vol. 10, no. 9, pp. 371-373, Sept. 2000.

[16] T.W. Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 223-229, Jan. 2004.

[17] C. Xin, E. Sanchez-Sinencio, "A linearization technique for RF low noise amplifier", *IEEE International Symposium on Circuits and Systems*, vol. IV, Vancouver, Canada, May 2004, pp. 313-316.

[18] Y.S. Youn, J.H. Chang, K.J. Koh, Y.J. Lee and H.K. Yu, "A 2 GHz 16 dBm IIP3 low noise amplifier in 0.25 um CMOS technology," presented at the *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, February 2003, pp 25.7.

[19] V.Aparin, and L.E.Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers." In IEEE Transactions on Microwave Theory and Techniques., vol .53, no .2, pp. 571 – 581, February 2005.

[20] V Aparin, "Linearization of CDMA receiver front-ends", Chapter 1,2 of PhD Dissertation, University of California, San Diego, pp 1 - 35, 2005.

[21] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, U.K.: Cambridge Univ. Press, 1998.

[22] A.M. Niknejad and R.G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RFICs," *IEEE Journal of Solid-State Circuits*, vol. 33, issue 10, pp. 1470 – 1481, Oct. 1998.

[23] B. Razavi, *RF Microelectronics,* First Edition, Upper Saddle River, NJ, Prentice-Hall, 1997.

[24] J.C. Pedro and N.B. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits,* Norwood, MA, Artech House Publishers, 2003.

APPENDIX A

The IIP3 of the proposed Linear LNA is derived below using Volterra series analysis. The small signal model of the circuit is given in Fig. 14. The first and second order non-linearity co-efficients in the weak inversion transistor are neglected.

As shown in the Fig. 14, V_A and V_B are considered to be the gate-source voltages of transistors M_A and M_B respectively. The currents in the main and auxiliary transistors (i_A and i_B) are given in terms of their gate-source voltages as follows.

$$\begin{aligned} i_A &= g_{1a}V_A + g_{2a}V_A^2 + g_{3a}V_A^3 \\ i_B &= g_{3b}V_B^3 \\ i_{out} &= i_A + i_B = C_1(s_1)*V_x + C_2(s_1,s_2)*V_x^2 + C_3(s_1,s_2,s_3)*V_x^3 \end{aligned} \tag{A1}$$

The gate-source voltages of main and auxiliary transistors can be given in terms of the input voltage (V_x) as follows.

$$\begin{aligned} V_A &= A_1(s_1)*V_x + A_2(s_1,s_2)*V_x^2 + A_3(s_1,s_2,s_3)*V_x^3 \\ V_B &= B_1(s_1)*V_x + B_2(s_1,s_2)*V_x^2 + B_3(s_1,s_2,s_3)*V_x^3 \end{aligned} \tag{A2}$$

Thus the currents i_A and i_B can be represented in terms of the input voltage (V_x) from the above expressions as follows.

$$\begin{aligned} i_A &= g_{1a}A_1(s)*V_x + \left[g_{1a}A_2(s_1,s_2) + g_{2a}A_1(s_1)A_1(s_2)\right]*V_x^2 + \\ &\quad \left[g_{1a}A_3(s_1,s_2,s_3) + 2g_{2a}\overline{A_1(s_1)A_2(s_1s_2)} + g_{3a}A_1(s_1)A_1(s_2)A_1(s_3)\right]*V_x^3 \\ i_B &= g_{3b}B_1(s_1)B_1(s_2)B_1(s_3)*V_x^3 \end{aligned} \tag{A3}$$

Using Kirchhoff's laws in the small signal model give above, the following equations can be derived

$$
\begin{aligned}
&V_1 - V_2 = V_A \\
&V_2 - V_3 = V_B \\
&\frac{V_x - V_1}{Z_s} = sC_A V_A \\
&i_B + sC_B V_B = \frac{V_3}{sL_B} \\
&i_A + sC_A V_A = \frac{V_2}{sL_A} + sC_B V_B
\end{aligned}
\tag{A4}
$$

From the above equations, solving for V_A and V_B gives the following.

$$
\begin{aligned}
&V_A = V_1 - V_2 = \frac{-i_A * sL_A(1 + s^2 L_B C_B) - i_B * s^3 L_A L_B C_B + V_x * Z_2}{Z_1 Z_2 - s^4 L_A^2 C_A C_B} \\
&V_B = V_2 - V_3 = \frac{i_A * sL_A(1 + sC_A Z_s) - i_B * sL_B Z_1 + V_x * s^2 L_A C_A}{Z_1 Z_2 - s^4 L_A^2 C_A C_B} \\
&where\ Z_1 = 1 + sC_A Z_s + s^2 L_A C_A, Z_2 = 1 + s^2 L_A C_B + s^2 L_B C_B
\end{aligned}
\tag{A5}
$$

$$
Let\ a(s) = sL_A, b(s) = sL_B,\ c(s) = sC_B, d(s) = 1 + sC_A Z_s, e(s) = s^2 L_A C_A \tag{A6}
$$

Using the above convention (A6), V_A and V_B can be expressed as follows.

$$
\begin{aligned}
&V_A = \frac{1}{Z_0}\left[-i_A * a(s)\big(1 + b(s)c(s)\big) - i_B * a(s)b(s)c(s) + V_x * \big(1 + c(s)\{a(s) + b(s)\}\big)\right] \\
&V_B = \frac{1}{Z_0}\left[i_A * a(s)d(s) - i_B * b(s)\big(d(s) + e(s)\big) + V_x * e(s)\right] \\
&Z_0 = Z_1 Z_2 - s^4 L_A^2 C_A C_B \\
&\quad = (1 + sC_A Z_s)(1 + s^2 L_A C_B + s^2 L_B C_B) + s^2 L_A C_A (1 + s^2 L_B C_B) \\
&\quad = d(s)\big(1 + c(s)\big(a(s) + b(s)\big)\big) + e(s)\big(1 + b(s)c(s)\big)
\end{aligned}
\tag{A7}
$$

Using the Harmonic Input method [24] to find out the first, second and third order non-linearity coefficients A(s) and B(s) of the gate-source voltages of main and auxiliary transistor.

Step-I:

To find $A_1(s)$ *and* $B_1(s)$ substitute $V_x = e^{st}$ in (A7) and compare the coefficients of e^{st} on both sides.

$$\begin{aligned} A_1(s) &= \frac{1}{Z_0(s)}\left[-g_{1a}A_1(s) * a(s)\{1+b(s)c(s)\}+1+c(s)\{a(s)+b(s)\}\right] \\ &= \frac{1+c(s)\{a(s)+b(s)\}}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}} \end{aligned} \tag{A8}$$

$$B_1(s) = \frac{1}{Z_0(s)}\left[g_{1a}A_1(s) * a(s)d(s)+e(s)\right] \tag{A9}$$

$$B_1(s) = n(s)A_1(s)$$

$$where\ \ n(s) = \frac{g_{1a}a(s)+e(s)}{1+c(s)\{a(s)+b(s)\}} \tag{A10}$$

Step-II:

To find $A_2(s_1, s_2)$ substitute $V_x = e^{s_1 t} + e^{s_2 t}$ in (A7) and compare the coefficients of $e^{(s_1+s_2)t}$ on both sides.

$$\begin{aligned} A_2(s_1,s_2) &= \frac{1}{Z_0(s)}\left[-\left(g_{1a}A_2(s_1,s_2)+g_{2a}A_1(s_1)A_1(s_2)\right)a(s)\{1+b(s)c(s)\}\right] \\ A_2(s_1,s_2) &= \frac{-g_{2a}a(s)\{1+b(s)c(s)\}}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}}A_1(s_1)A_1(s_2) \end{aligned} \tag{A11}$$

Step-III:

To find $A_3(s_1, s_2, s_3)$ substitute $V_x = e^{s_1 t} + e^{s_2 t} + e^{s_3 t}$ in (A7) and compare the coefficients of $e^{(s_1+s_2+s_3)t}$ on both sides.

$$A_3(s_1,s_2,s_3)=\frac{1}{Z_0(s)}\left[\begin{matrix}-\left(g_{1a}A_3(s_1,s_2,s_3)+2g_{2a}\,\overline{A_1(s_1)A_2(s_1,s_2)}+g_{3a}A_1(s_1)A_1(s_2)A_1(s_3)\right)*\\ a(s)\{1+b(s)c(s)\}-\left(g_{3b}B_1(s_1)B_1(s_2)B_1(s_3)\right)*a(s)b(s)c(s)\end{matrix}\right]$$

$$A_3(s_1,s_2,s_3)=\frac{-1}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}}*\left\{\begin{matrix}\left(2g_{2a}\,\overline{A_1(s_1)A_2(s_1,s_2)}+g_{3a}A_1(s_1)A_1(s_2)A_1(s_3)\right)a(s)\{1+b(s)c(s)\}\\ +\left(g_{3b}B_1(s_1)B_1(s_2)B_1(s_3)\right)*a(s)b(s)c(s)\end{matrix}\right\} \quad \text{(A12)}$$

IMD$_3$ at $2\omega_b-\omega_a$ can be found by setting $s_1=s_2=s_b$ and $s_3=-s_a$. Assuming closely spaced frequencies, (i.e.) $s_a\cong s_b\cong s$, (A12) can be simplified as follows.

$$A_3(s_b,s_b,-s_a)=\frac{-1}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}}*\left\{\begin{matrix}\left(2g_{2a}\,\overline{A_1(s_b)A_2(s_b,-s_a)}+g_{3a}A_1(s)\left|A_1(s)\right|^2\right)a(s)\{1+b(s)c(s)\}\\ +g_{3b}B_1(s)\left|B_1(s)\right|^2*a(s)b(s)c(s)\end{matrix}\right\} \quad \text{(A13)}$$

Where $\overline{A_1(s_b)A_2(s_b,-s_a)}=\frac{1}{3}\left[2A_1(s_b)A_2(s_b,-s_a)+A_1(-s_a)A_2(s_b,s_b)\right]$

$$=\frac{-g_{2a}}{3}A_1(s_b)^2A_1(-s_a)*\left[\frac{a(\Delta s)\{1+b(\Delta s)c(\Delta s)\}}{Z_0(\Delta s)+g_{1a}a(\Delta s)\{1+b(\Delta s)c(\Delta s)\}}+\frac{a(2s)\{1+b(2s)c(2s)\}}{Z_0(2s)+g_{1a}a(2s)\{1+b(2s)c(2s)\}}\right] \quad \text{(A14)}$$

Since the two input frequency tones are closely spaced, the difference frequency would be located at almost zero frequency.

$\Delta s=s_b-s_a;\ s_b\cong s_a\Rightarrow\Delta s=0\Rightarrow a(\Delta s)=b(\Delta s)=c(\Delta s)\cong 0$

Hence (A14) can be simplified as given in (A15).

$$\therefore\ \overline{A_1(s_b)A_2(s_b,-s_{a)}}=\frac{-g_{2a}}{3}A_1(s_b)^2A_1(-s_a)\left[\frac{a(2s)\{1+b(2s)c(2s)\}}{Z_0(2s)+g_{1a}a(2s)\{1+b(2s)c(2s)\}}\right] \quad \text{(A15)}$$

Substituting (A8), (A10), (A11) and (A14) in (A13) gives

$$A_3(s_b,s_b,-s_a)=\frac{-a(s)A_1(s)\left|A_1(s)\right|^2}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}}*$$
$$\left[g_{3b}n(s)\left|n(s)\right|^2b(s)c(s)+\left(g_{3a}-\frac{2g_{2a}^2}{3}\frac{a(2s)\{1+b(2s)c(2s)\}}{Z_0(2s)+g_{1a}a(2s)\{1+b(2s)c(2s)\}}\right)(1+b(s)c(s))\right] \quad \text{(A16)}$$

Step-IV:

The non-linearity co-efficients of output current (i_{out}) are calculated in terms of co-efficients of currents i_A and i_B calculated above.

$$i_{out}=C_1(s_1)*V_x+C_2(s_1,s_2)*V_x^2+C_3(s_1,s_2,s_3)*V_x^3 \quad \text{(A17)}$$

$$where\ C_1(s)=g_{1a}A_1(s)$$
$$C_3(s_1,s_2,s_3)=$$
$$g_{3b}B_1(s_1)B_1(s_2)B_1(s_3)+g_{1a}A_3(s_1,s_2,s_3)+2g_{2a}\overline{A_1(s_1)A_2(s_1,s_2)}+g_{3a}A_1(s_1)A_1(s_2)A_1(s_3)$$

Substituting all the terms calculated in steps I-III in (A17) and simplifying gives the following expression.

$$C_3(s_b,s_b,-s_a)=\frac{A_1(s)\left|A_1(s)\right|^2}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}}*$$
$$\left\{\begin{array}{l} g_{3b}n(s)\left|n(s)\right|^2\left(Z_0(s)+g_{1a}a(s)\right)+g_{3a}Z_0(s)- \\ \frac{2g_{2a}^2}{3}\frac{a(2s)\{1+b(2s)c(2s)\}}{Z_0(2s)+g_{1a}a(2s)\{1+b(2s)c(2s)\}}Z_0(2s) \end{array}\right\} \quad \text{(A18)}$$

The expression for $C_3(s_b,s_b,-s_a)$ given in (A18) can be further simplified by considering conjugate matched input impedance ($Z_s(s)$ and hence $Z_s(s)=Z_{in}(-s)$.

Input impedance (Z_{in}) is calculated with a test voltage V_x applied at the input. The current in the auxiliary transistor is neglected as it is operating in weak inversion region. The input impedance is found to be follows for the schematic shown in Fig. 14.

$$\begin{aligned} Z_{in}(s) &= \frac{1+sC_B(sL_A+sL_B)+sL_A(g_{1a}+sC_A)(1+s^2L_BC_B)}{sC_A(1+sC_B(sL_A+sL_B))} \\ Z_s(s) &= Z_{in}(-s) \\ &= \frac{1+sC_B(sL_A+sL_B)-sL_A(g_{1a}-sC_A)(1+s^2L_BC_B)}{-sC_A(1+sC_B(sL_A+sL_B))} \end{aligned} \tag{A19}$$

Substituting the above value in expression for $Z_0(s)$ given in (A7) gives the follows.

$$\begin{aligned} Z_0(s) &= (1+sC_AZ_s)(1+sC_B(sL_A+sL_B))+s^2L_AC_A(1+s^2L_BC_B) \\ &= g_{1a}sL_A(1+s^2L_BC_B) \end{aligned} \tag{A20}$$

Calculating various other terms in the expression of $C_3(s_b, s_b, -s_a)$ given in (A18).

$$Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\} = 2g_{1a}sL_A(1+s^2L_BC_B) \tag{A21}$$

$$n(s) = \frac{g_{1a}a(s)+e(s)}{1+c(s)\{a(s)+b(s)\}} = \frac{sL_A(g_{1a}+sC_A)}{1+sC_B(sL_A+sL_B)} \tag{A22}$$

$$\frac{a(2s)\{1+b(2s)c(2s)\}}{Z_0(2s)+g_{1a}a(2s)\{1+b(2s)c(2s)\}} = \frac{1}{2g_{1a}} \tag{A23}$$

$$A_1(s) = \frac{1+s^2C_B(L_A+L_B)}{2s^2L_AC_A(1+s^2L_BC_B)} \tag{A24}$$

$$\frac{Z_0(s)}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}} = \frac{1}{2} \tag{A25}$$

$$\frac{Z_0(s)+g_{1a}a(s)}{Z_0(s)+g_{1a}a(s)\{1+b(s)c(s)\}} = \frac{2+s^2L_BC_B}{1+s^2L_BC_B} \tag{A26}$$

The value of IIP3 at the output, in terms of co-efficients of non-linearity of the output current can be given as follows.

$$IIP_3 = \frac{1}{6\,\mathrm{Re}\left(Z_s(s)\right)}\left|\frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)}\right| \tag{A27}$$

Substituting all the above calculated values in $C_1(s_a)$ *and* $C_3(s_b, s_b, -s_a)$ gives

$$IIP_3 = \frac{1}{6\,\mathrm{Re}\left(Z_s(s)\right)\left|A_1(s)\right|^2}\left\{\frac{g_{1a}}{\varepsilon}\right\}$$

where

$$\varepsilon = \frac{1}{Z_0(s) + g_{1a}a(s)\{1 + b(s)c(s)\}}\left[\begin{array}{l} g_{3b}n(s)\left|n(s)\right|^2\left(Z_0(s) + g_{1a}a(s)\right) + g_{3a}Z_0(s) - \\ \frac{2g_{2a}^2}{3}\frac{a(2s)(1 + b(2s)c(2s))}{Z_0(2s) + g_{1a}a(2s)(1 + b(2s)c)(2s))}Z_0(2s) \end{array}\right] \tag{A28}$$

$$= g_{3a} - \frac{g_{2a}^2}{3g_{1a}} + g_{3b}n(s)\left|n(s)\right|^2\frac{2 + s^2L_BC_B}{2(1 + s^2L_BC_B)}$$

APPENDIX B

The input impedance of the "Linear LNA" is calculated here. KCL and KVL equations for the circuit shown in Fig. 16 are given below.

$$I_{in} = sC_A V_A \tag{B1}$$

KCL at node V_{x1}

$$I_{in} - \frac{V_{x1}}{sL_A} + g_{1a} V_A - sC_B V_B = 0 \tag{B2}$$

KCL at node V_{x2}

$$sC_B V_B + g_{1b} V_B - \frac{V_{x2}}{sL_B} = 0 \tag{B3}$$

From (B3)

$$V_{x2} = sL_B (sC_B + g_{m2}) V_B \tag{B4}$$

$$\begin{aligned} \textit{Now, } V_{x1} &= V_B + V_{x2} \\ &= V_B + sL_B (sC_B + g_{1b}) V_B \\ &= V_B \left(sL_B \left(sC_B + g_{1b} \right) + 1 \right) \end{aligned} \tag{B5}$$

Substituting $(B5)$ *in* $(B2)$

$$I_{in} - \frac{\left(sL_B \left(sC_B + g_{1b} \right) + 1 \right)}{sL_A} V_B + g_{1a} \frac{I_{in}}{sC_A} - sC_B V_B = 0$$

$$I_{in} \left(1 + \frac{g_{1a}}{sC_A} \right) = V_B \left(sC_B + \frac{sL_B \left(sC_B + g_{1b} \right) + 1}{sL_A} \right) \tag{B6}$$

$$V_B = \frac{\left(1 + \frac{g_{1a}}{sC_A} \right)}{\left(sC_B + \frac{sL_B \left(sC_B + g_{1b} \right) + 1}{sL_A} \right)} I_{in}$$

Substituting $(B6)$ *in* $(B5)$ *gives*

$$V_{x1} = \left(sL_B \left(sC_B + g_{1b} \right) + 1 \right) \frac{\left(1 + \frac{g_{1a}}{sC_A} \right)}{\left(sC_B + \frac{sL_B \left(sC_B + g_{1b} \right) + 1}{sL_A} \right)} I_{in} \tag{B7}$$

$$V_{in} = sL_g I_{in} + V_A + V_{x1}$$

$$= sL_g I_{in} + \frac{I_{in}}{sC_A} + \left(sL_B\left(sC_B + g_{1b}\right)+1\right)\frac{\left(1+\frac{g_{1a}}{sC_A}\right)}{\left(sC_B + \frac{sL_B\left(sC_B + g_{1b}\right)+1}{sL_A}\right)} I_{in} \tag{B8}$$

$$Therefore\ Z_{in} = \frac{V_{in}}{I_{in}}$$

$$= sL_g + \frac{1}{sC_A} + \left(sL_B\left(sC_B + g_{1b}\right)+1\right)\frac{\left(sL_A + \frac{g_{1a}L_A}{C_A}\right)}{\left(s^2 L_A C_B + sL_B\left(sC_B + g_{1b}\right)+1\right)} \tag{B9}$$

VITA

Sivakumar Ganesan

Department of Electrical and Computer Engineering
Texas A&M University
College Station, TX 77843
sivakumar@neo.tamu.edu

B.E. (Hons.) Electrical and Electronics, 2003
Birla Institute of Technology and Science
Pilani, India.

M.S. Electrical Engineering, 2006
Texas A&M University
College Station, TX, USA