DESIGN AND IMPLEMENTATION OF A FREQUENCY SYNTHESIZER FOR AN IEEE 802.15.4/ZIGBEE TRANSCEIVER

A Thesis

by

RANGAKRISHNAN SRINIVASAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2006

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Design and Implementation of a Frequency Synthesizer for an

IEEE 802.15.4/Zigbee Transceiver. (May 2006)

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The frequency synthesizer, which performs the main role of carrier generation for the down-conversion/up-conversion operations, is a key building block in radio transceiver front-ends. The design of a synthesizer for a 2.4 GHz IEEE 802.15.4/Zigbee transceiver forms the core of this work. This thesis provides a step-by-step procedure for the design of a frequency synthesizer in a transceiver environment, from the mapping of standard-specifications to its integrated circuit implementation in a CMOS technology.

The results show that careful system level planning leads to high-performance realizations of the synthesizer. A strategy of using different supply voltages to enhance the performance of each building block is discussed. A section is presented on layout and board level issues, especially for radio-frequency systems, and their effect on synthesizer performance. The synthesizer consumes 15.5 mW and meets the specifications of the 2.4 GHz IEEE 802.15.4/Zigbee standard. It is capable of 5 GHz operation with a VCO sensitivity of 135 MHz/V and a tuning range of 700 MHz. It can be seen that the adopted methodology can be used for the design of high-performance frequency synthesizers for any narrow-band wireless standard.

DEDICATED TO

Raga Bhairavi – Mother Goddess

Music of Baba Ali Akbar Khan

My Gurus

Amma, Appa and Chinna

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So many people come into our lives to provide valuable lessons, only to proceed in their own ways. I am fortunate and blessed to have had a highly enriching graduate study experience at Texas A&M University. The varied mutual planes of interactions and the deepest of resonance with a select few made my life at Texas A&M all the more special.

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My *amma, apppa* and *chinna* have been my pillars of strength by providing me with their unconditional love and support. Last but not the least; I am deeply indebted to the Divine. I am an insignificant speck in this universe which is a wonderful creation of His/Hers. The beautiful things in the world – arts, music, books, nature, people, philosophy, etc. are a great source of joy, bliss, inspiration and solace. I thank them all.

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1. INTRODUCTION

1.1 Background and Motivation

The need for ubiquitous mobile computing and networking has lead to the development of various wireless standards by the Institute of Electrical and Electronics Engineers (IEEE) in consortium with the industry over the last decade. The development of such standards has lead to a complete revolution in the wireless segment by spurring on an exponential growth in the semiconductor and communications industry. Examples of such standards include Bluetooth, IEEE 802.11 a/b/g, Ultra wide-band (UWB), etc. It merits mention that each standard caters to a different application and has an altogether different design focus.

The IEEE 802.15.4/Zigbee standard [1] has been recently developed (released in December 2004) to cater to the needs of low cost, low power, low data rate, and short range wireless networks. This new standard is specifically intended for applications pertaining to data monitoring, industrial control and sensor networks. The thesis focuses on the design of a frequency synthesizer for a 2.4 GHz IEEE 802.15.4/Zigbee transceiver.

The design of a monolithic solution of a low power, high-performance frequency synthesizer in CMOS is the main challenge. Implementation of the synthesizer in a transceiver environment leads to additional design considerations and evaluation of non-idealities. It is shown that careful planning at the system level of the synthesizer can lead to high-performance realizations.

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits.*

The frequency planning of the transceiver also plays a key role in the development of the synthesizer. Further, it can be seen that a similar design approach be followed for the implementation of synthesizers for other wireless transceivers.

1.2 Organization

Section 2 begins with the need for the IEEE 802.15.4/Zigbee standard and a comparative study with the existing standards of Bluetooth, IEEE 802.11a/b/g and UWB. The architecture of the entire transceiver is given and the important specifications for the synthesizer have been derived from the standard. The architecture chosen for the particular implementation of this synthesizer in a transceiver environment is provided.

Moreover, a detailed system level design procedure with stability and settling time considerations aids in understanding the system level issues of the synthesizer better. A literature survey of synthesizer implementations for transceivers in general (at both 5 GHz and 2.4 GHz) is provided. The section ends with a discussion of the salient features of the synthesizers. The survey helps us in understanding the bottlenecks and performance oriented goals for a successful design better.

Section 3 forms the crux of this thesis and deals with the practical design and implementation of a frequency synthesizer in a plain CMOS technology. It provides a practical solution to the development of the synthesizer after the system level progress in Section 2. Salient considerations affecting the performance of the synthesizer and germane issues specific to the integrated circuit implementation are discussed here.

Further, a section on layout and board level issues highlights their importance and affect on the synthesizer performance. The testing and measurement results of the silicon prototype; both for the synthesizer and the VCO are provided in this section. Moreover,

the key features of the synthesizer are highlighted and a judicious comparative analysis made with existing synthesizers reported in the literature (mentioned in Section 2).

Section 4 is dedicated to the design and implementation of the Voltage Controlled Oscillator (VCO), one of the key radio-frequency (RF) blocks in the synthesizer. Various architectures are considered and the final realization is justified. The passive RF components play a crucial role in a VCO. Hence, a treatment of the varactors and inductors; and their effects on the overall performance is necessary. The design procedure provides a better understanding of the tightly coupled design space.

Finally, Section 5 concludes with a summary of the work done as part of this research. Further the future scope of work and open-ended problems for research treatment are given.

1.3 Zigbee in Literature

The PHY layer of the standard had been prepared in 2003 by the IEEE and the Zigbee Alliance; and the standard had been officially released in December 2004. Since then, the design of Zigbee related products has been one of the main focuses in the industry, especially among members of the Zigbee Alliance. Publications in the literature related to academic research are limited.

A low-coin sized transceiver for a preliminary IEEE 802.15.4 standard is reported in [2]. Reference [3] reports one of the first 2.4 GHz Zigbee-ready IEEE 802.15.4 compliant radio-transceiver. Recently, a complete system-on-chip solution for a 2.4 GHz transceiver developed in the industry is reported in [4]. References [5] and [6] are stand-alone frequency synthesizers reported for 2.4 GHz Zigbee applications.

2. ZIGBEE FREQUENCY SYNTHESIZER

In this section, the need for the Zigbee standard is addressed and the specifications for the frequency synthesizer for application in a 2.4 GHz transceiver are derived. The architecture development of the synthesizer and the system level design issues are discussed here. The frequency synthesizer, which performs the main role of career generation for the down-conversion/ up-conversion, is a key building block in radio front-ends. Despite not being directly involved in the signal path, the performance of the synthesizer affects the overall performance of the transceiver. A detailed treatment of the frequency synthesizer is beyond the scope of the thesis and the reader is encouraged to refer to [7-13] for a better understanding of important concepts.

2.1 Wireless Standards

The 21st century has lead to the dawn and revolution of a new information technology era marked by the emergence of various wireless standards. Internetworking technologies have lead to a high connectivity to information, be it data, voice, audio, or video. The need for ubiquitous mobile computing and networking is more so felt now than ever before. Various standards have been developed over the last decade to cater to different needs and applications.

Examples of such standards include Bluetooth, 802.11a/b/g, ultra wideband, 802.15.4/Zigbee, GSM, GPS, DECT-1800, DECT-1900, etc. It merits mention that certain standards like the GPS were mainly developed for military applications, only to be released in the commercial market too. Moreover, the technological advances, especially, in the field of integrated circuits has accelerated this revolution. Complete low-area, low-cost, monolithic integrated transceiver solutions are now in vogue.

The IEEE 802.15.4/ Zigbee standard has been recently developed (officially released for commercial applications in December 2004) to cater to the needs of low cost, low power, low data rate, and short range wireless networks [1]. *The Zigbee Alliance is responsible for the Zigbee wireless technology, which defines network, security and application layers upon the IEEE 802.15.4 PHY and MAC layers [1]*. Henceforth, for reasons of brevity, the IEEE 802.15.4/ Zigbee standard will be termed Zigbee.

It has been realized that already existing short-range wireless standards like Bluetooth and 802.11a/b/g have relatively high data rates when compared to the actual data rate required for certain applications. For e.g. the use of a Bluetooth transceiver, with a data rate of 1 Mbps, in applications involving the communication of data in the form of simple text, leads to sheer wastage of resources. Networks involving machine-to-machine (M2M) communication for monitoring and quality control purposes do not need a high data rate.

The standard addresses the need of network applications requiring high density of transceivers with low data-rate. Such transceivers need to have a long battery life and should be highly economical in cost. They are an attractive option for applications pertaining to low-data industrial monitoring and control, sensor based network systems, home automation, gaming, medical and automotive solutions. Further, it can theoretically support upto 65,000 nodes in the network [1].

The important design considerations from the paradigm of a transceiver design are frequency band, the data rate, the required range of wireless transmission, sensitivity at the receiver end, modulation scheme, transmitted output power, settling time for frequency hopping, adjacent and alternate channel interferers etc. These specifications

influence the choice of technology, the choice of architecture and the choice of the standard.

Table I gives a comparison between the popular wireless standards – IEEE 802.11.a/b/g [14-16], Bluetooth [17], and ultra wideband [18] with the Zigbee standard [1]. It can be seen that Zigbee is the only standard that is tailored for low data-rate systems. Further, it can be inferred that prior to the Zigbee standard, more importance had been given to the development of high data-rate, multimedia friendly standards.

TABLE I
WIRELESS STANDARDS

	Zigbee	*Bluetooth*	*802.11b*	*802.11g*	*802.11a*	*UWB*
Data Rate	250 Kbps	1 Mbps	11 Mbps	54 Mbs	24 Mbps	500 Mbps
Band	2.4 GHz ISM	2.4 GHz ISM	2.4 GHz ISM	2.4 GHz ISM	5 GHz UNII	3.1-10.6 GHz
Range	10m	10m	100m	100m	50m	10m
Channel Bandwidth	5 MHz	1 MHz	25 MHz	25 MHz	20 MHz	500 MHz-7.5GHz
Sensitivity	-85 dBm	-70 dBm	-76 dBm	-76 to -74 dBm	-82 to -65 dBm	-70 dBm
Modulation	O-QPSK	GFSK	11Mbaud QPSK	OFDM 64+	COFDM BPSK	BPSK/ QPSK
Output Power	-5 to 3 dBm	0 to 20 dBm	30 dBm	30 dBm	50mW; 250 mW	-41.3 dBm/MHz
Settling time	192 μs	259 μs	224 μs	224 μs	224 μs	10ns

2.2 Zigbee Transceiver

The design and implementation of the RF front-end of the 2.4 GHz Zigbee transceiver is a collaborative effort of five graduate students (four Ph.D. and one M.S.). The responsibilities of the author included derivation of frequency synthesizer specifications from the standard, architecture development of the frequency synthesizer, phase-locked loop design based on settling time and stability paradigms (Section 2); and the design and implementation of certain building blocks (Sections 3 and 4) of the

synthesizer. The main design focus of this transceiver implementation is design for low power consumption and high integrability in a low cost technology.

The TSMC 0.18 μm CMOS technology is used for the design of the transceiver. Two popular radio transceiver architectures exist – the low-IF architecture and Direct Conversion. Both the architectures have their merits and drawbacks. The architecture development of a complete transceiver depends on a multitude of parameters like Noise Figure, Linearity, Power Consumption, SNR-BER, implementation challenges, injection pulling, PA load pulling, Coherent and Non-coherent demodulation, Choice of modulation scheme, Gain Planning and Frequency Planning.

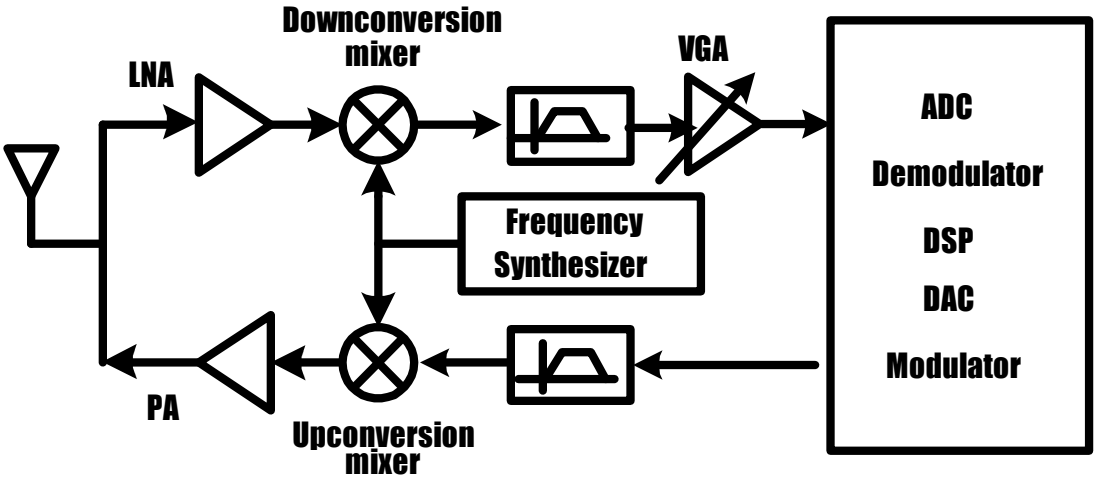


Fig. 2.1 Zigbee Transceiver Architecture

The transceiver architecture is given in Fig. 2.1. The circuit implementation of the important building blocks in the transceiver such as the Low Noise Amplifier, Downconversion mixer, Power Amplifier, Upconversion mixer in the direct signal path and the Frequency Synthesizer introduce non-idealities. A thorough approach to system

design is essential and an involved discussion on radio transceivers is beyond the scope of the thesis. The reader is encouraged to read [12] and [13] for a treatment of the issues in a transceiver.

TABLE II
SPECIFICATIONS OF THE 2450 MHZ IEEE 802.15.4 PHY LAYER

Performance Metrics	*Specifications*
Carrier	2400 MHz
Spectrum	2400-2483.5 MHz
Modulation	O-QPSK using DSSS
Channel Bandwidth	3 MHz
Channel Spacing	5 MHz
No. of Channels	16 (11-26 of the PHY layer)
Sensitivity	- 85 dBm
FER	5e-5
SNR	2 dB
Settling Accuracy	$\pm$ 40 ppm (96 KHz)
Alternate Channel Rejection	30 dB at 10 MHz offset
Adjacent Channel Rejection	0 dB at 5 MHz offset
Output Transmitted Power	-5 to 3 dBm

The important specifications of the PHY layer from the 2.4 GHz IEEE 802.15.4 standard are given in Table II. The overall transceiver needs to meet these specifications, irrespective of their implementation scheme. The general design methodology for the design of a frequency synthesizer is summarized in Table III. Moreover, the relevant sections in the thesis are given along side for the sake of completeness.

TABLE III
GENERAL DESIGN METHODOLOGY FOR PLL-BASED FREQUENCY SYNTHESIZERS

Step	*Procedure*	*Relevant Section*
I	Transceiver Considerations	2.2
II	Synthesizer Specifications from Standard	2.3
III	Architecture Development	2.4
IV	Phase Locked Loop Design	2.5
V	Integrated Circuit Implementation	3, 4

2.3 Synthesizer Specifications from Standard

The IEEE 802.15.4 standard gives the communication protocol for the prototype transceiver implementation and the specifications for the transceiver and the synthesizer need to be derived from this standard. The mapping of the specifications from the standard is an important pre-design process. This section highlights the one-to-one correspondence between the standard and the key performance metrics of the synthesizer. The key specifications from the standard that are used for the estimation of the synthesizer performance metrics is explained figuratively using Fig. 2.2.

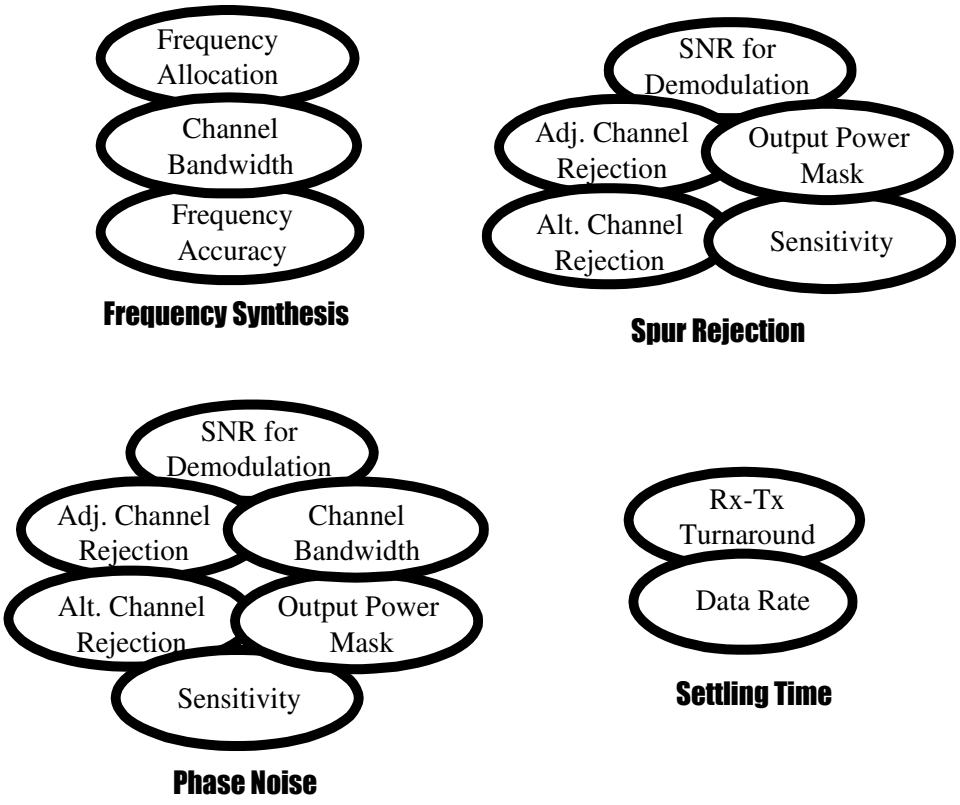


Fig. 2.2. Mapping Standard to Key Synthesizer Specifications

2.3.1 Frequency Synthesis

The 2.4 GHz Zigbee standard has 16 channels, spaced 5 MHz apart, from 2405 MHz to 2480 MHz. The synthesizer needs to synthesize these 16 channel selection clock frequencies with 40-ppm frequency accuracy. This performance metric is essential for the selection of the architecture and the design of the divide ratio for the divider. Since 16 channels need to be synthesized with a spacing of 5 MHz, it is natural to assume a clock reference of 5 MHz for an integer-N PLL based synthesizer scheme.

2.3.2 Phase Noise

Typical wireless systems employ the concept of time division multiple access or frequency division multiple access to increase the throughput and capacity of the system. Hence, it becomes necessary to switch from one channel to another in time. With this multiple access approach, the signal actually seeps into the other channels and contributes to channel interference. In the Zigbee PHY layer, the maximum contribution to co-channel interference is from the adjacent and alternate channels, spaced 5 MHz and 10 MHz apart from the channel of interest.

Fundamentally, the LO spectrum is not a pure single frequency tone in real-life implementations. The mechanisms of phase noise lead to the “skirt” behavior in the LO spectrum of the VCO or the synthesizer. The time domain manifestation of phase noise is jitter. Jitter can be defined as the variations in the zero crossings of the signal. These variations can be both random and deterministic. The various sources of jitter are reference, charge pump mismatch, spurs in the control line of the VCO, thermal noise of the loop filter, supply noise, phase noise of the VCO, phase mismatch in the dividers, etc. [19-21].

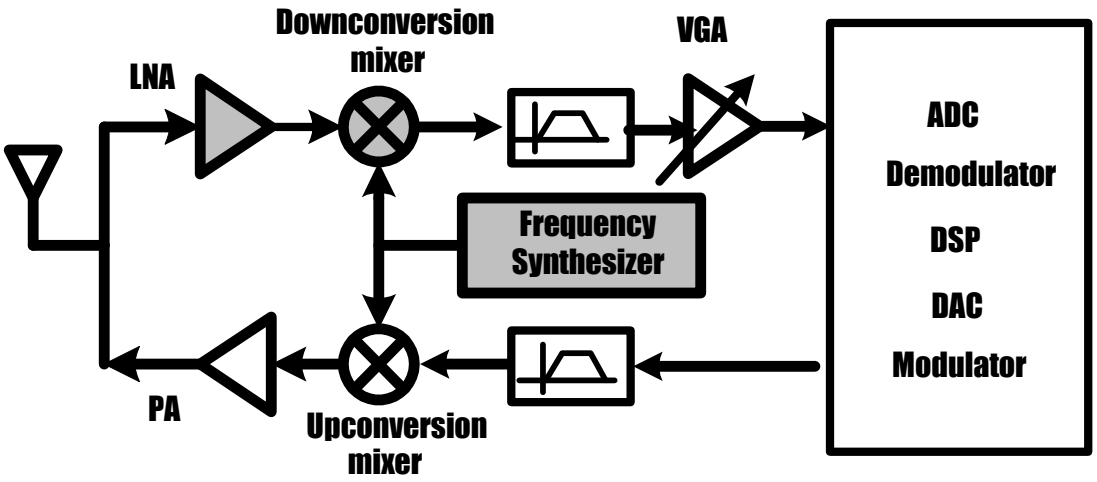


Fig. 2.3 Downconversion in a Transceiver

Thus, the phase noise of the LO for a particular channel, contributes to co-channel interference due to the mechanism of downconversion. In typical wireless systems, signal processing is performed in two steps (as shown in Fig. 2.3) – downconversion of the RF signal following "low-noise" amplification by the LNA to the baseband domain; and subsequent baseband processing. Thus, downconversion is inevitable and most phase noise specifications are derived from adjacent channel rejection requirements of the standard.

The phase noise of the adjacent channel LO frequency tone creates interference for the channel of interest. From Fig. 2.4, it can be seen that the Signal to Noise Ratio required at the input of the IF section (say, following downconversion) is given as

$$SNR = (P_{sig} + P_{LO}) - (PN + P_{\text{int}} + P_{BW}) > SNR_{\min} \qquad (2.1)$$

where P_{sig} is the power content of the carrier

P_{LO} is the power content of the LO

PN is the phase noise contribution of the LO

P_{int} is the power content of the interferer

P_{BW} is the power content of the signal across the channel bandwidth

SNR_{min} is the required SNR at the input of the IF section following downconversion for the given demodulation scheme and tolerable bit error rate.

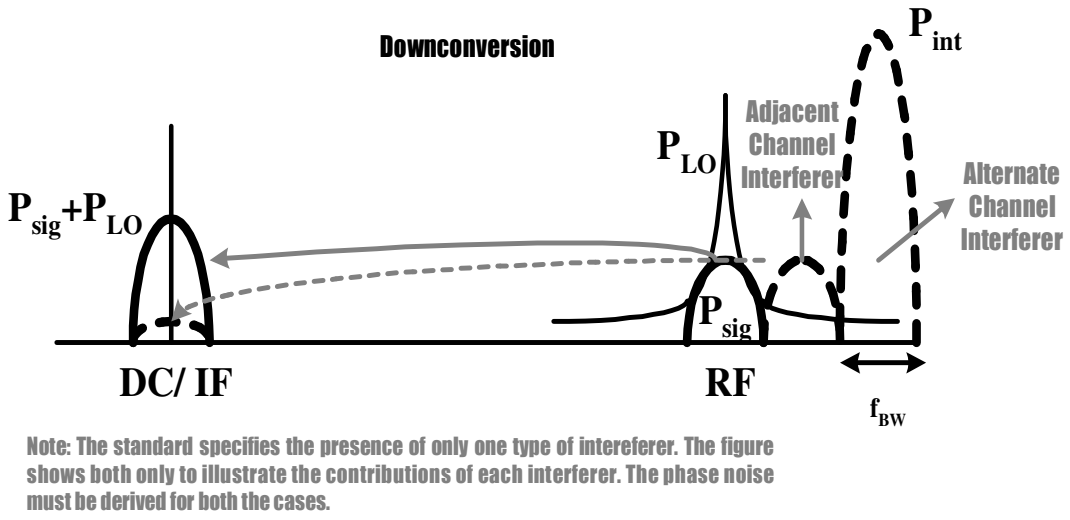


Fig. 2.4 Phase Noise Contribution to SNR at Input of IF Section

Careful gain planning gives us a minimum SNR requirement at the input of the IF section. To support a minimum SNR requirement of 2 dB at the input of the demodulator in the receiver path, the SNR requirement at the input of the IF section can be calculated as 8 dB. The signal (P_{sig}) is downconverted to IF or DC by LO (P_{LO}) provided by the synthesizer. The channel spacing is 5 MHz. There would be a guard band on either side of the channel to prevent aliasing and minimize co-channel interference. The actual

bandwidth of the channel would therefore be less than 5 MHz. However, for purposes of hand calculations, we can assume that the bandwidth is 5 MHz. Equation 2.1 can be rearranged to give

$$PN - P_{LO} < (P_{sig} - P_{\text{int}}) - P_{BW} - SNR_{\min} \tag{2.2}$$

From the above equation, the phase noise specifications for the synthesizer can be calculated as

$$\left(PN - P_{LO}\right)_{5MHz} = (0-0) - 10\log(5\cdot 10^{6}) - 8 = -75 dBc/Hz \tag{2.3}$$

$$\left(PN - P_{LO}\right)_{10MHz} = (0-30) - 10\log(5\cdot 10^{6}) - 8 = -105 dBc/Hz \tag{2.4}$$

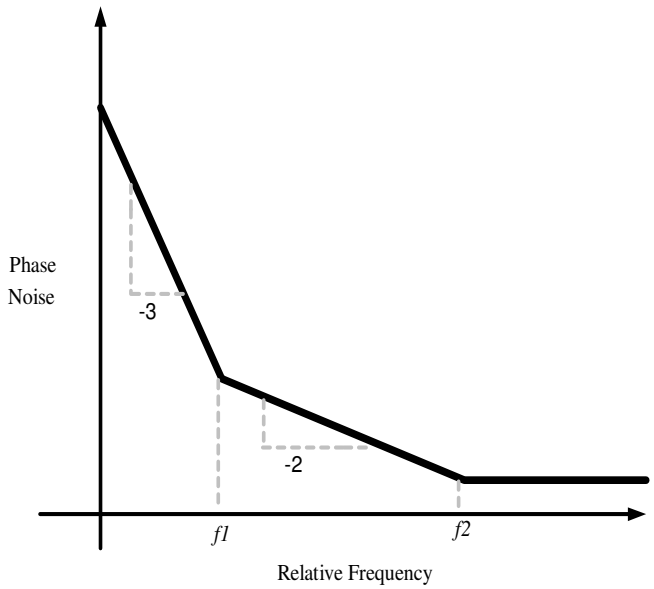


Fig. 2.5 Leeson Phase Noise Model

Assuming a margin of 5 dB in SNR to model the non-idealities of the system, the phase noise specification can be taken as –110 dBc/Hz at an offset of 10 MHz from the carrier. The Leeson model of phase noise provides a good approximation. Typically at

frequency offsets in the range of 1 MHz (beyond the knee frequency f_1, given by flicker noise upconversion limitations), the "skirt" assumes a -20 dBc/decade roll-off behavior (Refer Fig. 2.5). Thus it can be seen that the 10 MHz specification is tighter to meet. Therefore meeting the phase noise specifications at 10 MHz implies that the specification at 5 MHz is met, but not vice-versa.

Additionally, the power spectral mask requirements for the transmitter require a phase noise of –103 dBc/Hz at an offset frequency of 3.5 MHz.

2.3.3 Spur Rejection

The reference spurs appear at the output of the VCO spectrum in any PLL based system. If the integer-N PLL based synthesizer scheme is implemented, reference spurs appear at an offset of 5 MHz, equal to the channel spacing. The downconverted spur contributes to the interference and worsens the SNR at the input of the IF section. The Zigbee standard specifies the adjacent channel interference of 0 dB at an offset of 5 MHz. Here, the spur is considered as a single tone and not as an integrated noise.

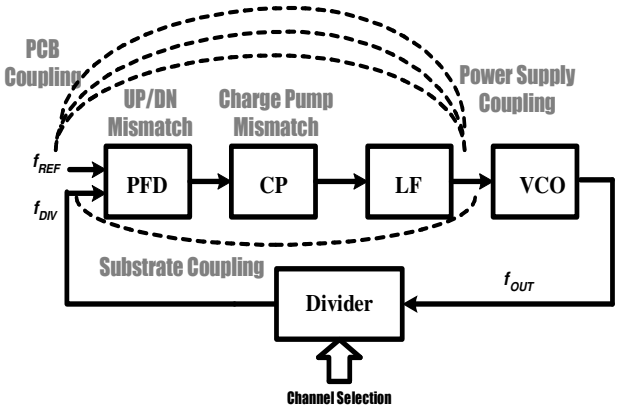


Fig. 2.6 Sources of Reference Spur in an Integer-N PLL based Synthesizer

The various sources of reference spur in a practical implementation of an integer-N synthesizer are discussed in Section 3. Further, the importance of PCB level issues on the spur performance of a synthesizer is highlighted. The modulation of the control voltage of the VCO leads to spurs in the output spectrum of the VCO and the synthesizer. Various sources exist for the modulation of this control line of the VCO. The important sources are the PCB coupling, substrate coupling, charge pump mismatch, and the power supply noise and are given in Fig. 2.6.

From Fig. 2.7, the Signal to Noise Ratio required at the input of the IF section (say, following downconversion) can be obtained as

$$SNR = (P_{sig} + P_{LO}) - (P_{Spurs} + P_{\text{int}}) > SNR_{\min} \tag{2.5}$$

$$P_{Spurs} - P_{LO} < (P_{sig} - P_{\text{int}}) - SNR_{\min} \tag{2.6}$$

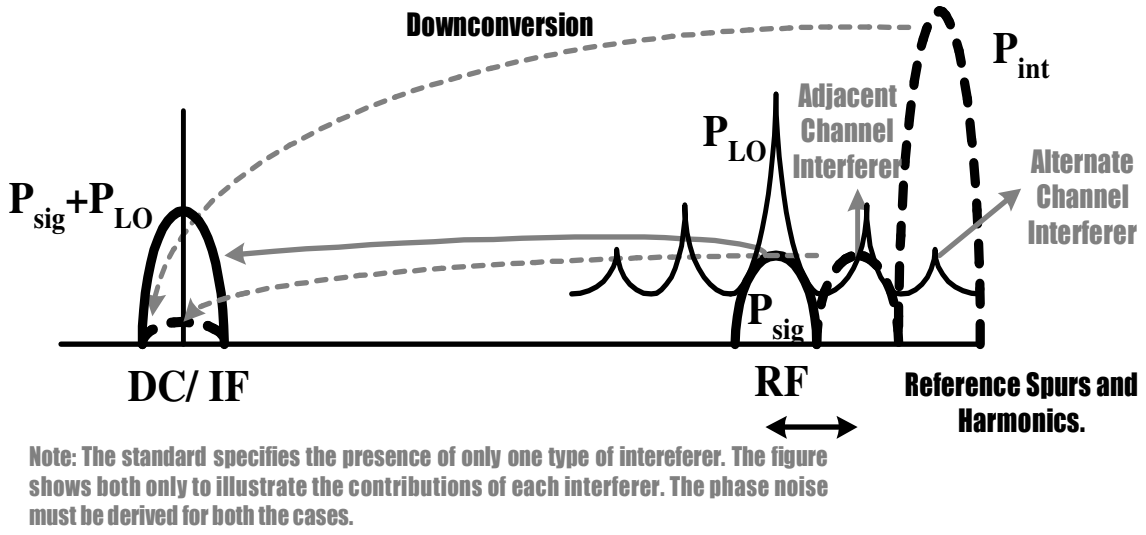


Fig. 2.7 Effect of Spurs on SNR at Input of IF Section

Thus the spur suppression requirement for the synthesizer can be calculated as

$$P_{Spurs} - P_{LO} = (0-0) - 8 = -8dBc \quad (2.7)$$

Moreover, the fundamental reference spur is at 5 MHz. Harmonics of the reference spur occur at 10 MHz, 15 MHz, etc. The differential mode of operation should ideally give only odd-harmonics. However, realistic environments give finite even-order components. Thus, the spur suppression specification at an offset frequency of 10 MHz, where the alternate channel interferer is present can be calculated as

$$P_{Spurs} - P_{LO} = (0-30) - 8 = -38dBc \quad (2.8)$$

Assuming a margin of 5 dB in SNR to model the non-idealities of the system, the Spur Suppression Specifications can be taken as –13 dBc and –43 dBc at offset frequencies of 5 MHz and 10 MHz respectively.

2.3.4 Settling Time

The standard supports a data rate of 250 Kbps. Each symbol is a word, consisting of 4 bits. Thus, the supported symbol rate is 62.5 Ksymbols/ sec. The maximum RX-TX or TX-RX turnaround time is given as 12 symbol periods, which is equivalent to 192 μs. This gives an estimate of the worst case settling time for the synthesizer for extreme switching from Channel 1 to Channel 16.

The settling time for the synthesizer is equivalent to the locking time for the PLL. The loop settles to a new frequency output based on the channel selection configuration. For e.g. the transceiver is operating in the receive mode at 2.405 GHz. In the next scheme

of operation, it needs to operate in the transmit mode at 2.48 GHz. The synthesizer now synthesizes 2.48 GHz. The time taken by the synthesizer to settle to the new frequency can be seen as the frequency response time of the loop.

TABLE IV
SPECIFICATIONS FOR THE SYNTHESIZER DERIVED FROM THE STANDARD

Performance Metric	*Value*
Frequency Synthesis	2405-2480 MHz in steps of 5 MHz
Phase Noise	-110 dBc at 10 MHz
	- 102 dBc at 3.5 MHz
Spur Rejection	-13 dBc at 5 MHz
	-43 dBc at 10 MHz
Settling time	192 μs

The important frequency synthesizer specifications derived from the standard are given in Table IV. The specifications, derived from first-order hand calculations, are found to be match closely with the ones derived by the system designer for the transceiver.

2.4 Synthesizer Architecture

The synthesizer needs to synthesize channels in steps of 5 MHz from 2405-2480 MHz. The frequencies to be synthesized are integer multiples of the channel spacing. Hence, integer-N PLL based synthesizer architecture will be best suited for this application. Since the phase noise and spur rejection specifications are relaxed, the integer-N PLL based solution gives the best performance in terms of power consumption and ease of integrability. Other synthesizer architectures exist, namely the Fractional-N synthesizer and Direct Digital Synthesizer [12, 13].

The fractional synthesizer uses a fractional divider scheme with sigma-delta modulator for dithering mechanism and noise shaping in the divider section. This architecture is particularly useful in applications requiring very high frequency resolution. For e.g., in typical read channel applications, the synthesizer works from 1 GHz to 2 GHz with a frequency resolution of 1.5%. The fractional-N synthesizer is not the best scheme for 2.4 GHz Zigbee applications.

The direct digital synthesizer doesn't make use of a feedback mechanism and is known to provide frequency synthesis with fast settling times. However, the frequency of application is limited due to the inherent digital nature of the synthesizer. It makes use of an accumulator, read only memory (ROM), digital-analog converter (DAC) and low pass filter (LPF). It is difficult to obtain ROM's working at 4.8 GHz for 2.4 GHz synthesizers. Thus, this approach is not suitable for 2.4 GHz Zigbee applications.

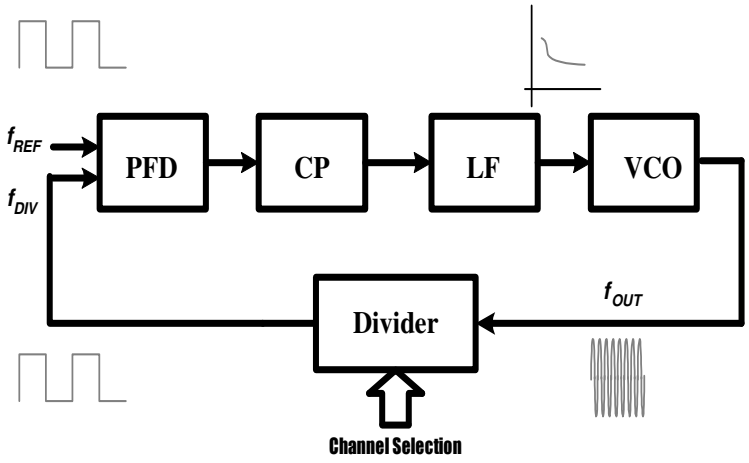


Fig. 2.8 Integer-N PLL Based Synthesizer

$$f_{OUT} = N.f_{REF} \tag{2.9}$$

The integer-N PLL based synthesizer architecture is given in Fig. 2.8. It consists of a phase frequency detector that compares the reference with the feedback signal obtained from the dividers to translate into time-level information. The charge pump along with the loop filter converts the critical time-level information into voltage. This voltage is effectively the control voltage of the VCO. Based on the behavior of the control voltage, the VCO changes its frequency. The PLL finally settles to a new frequency based on the channel select configuration. The dividers provide programmability to the synthesizer.

The synthesizer implementation, given above, is a complex discrete-time system and involves a non-linear control theory approach. However, for purposes of gaining insight into the operation of the PLL control structure, the continuous time approximation can be made, provided the Gardener's Stability limit is taken into consideration [22]. This approximation helps us in understanding the loop stability and dynamics better.

2.5 System Level Design

2.5.1 Theory

The charge-pump based PLL architecture [22] is given with the respective transfer functions of each block in Fig. 2.9. The oscillator and the charge pump-loop filter contribute to two poles at the origin (Figure on Page 22). For purposes of stability, a zero is placed appropriately to ensure sufficient phase margin. The loop filter introduces a pole and a zero in the system. If C_2 were absent, the control voltage experiences sharp transitions every time charge is injected into the R_1-C_1.

Eqn. 2.10 gives the overall open loop transfer function as

$$H_{open}(s) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{K_{vco} I_{cp}}{2\pi N C_1} \cdot \frac{(1 + s/\omega_{z1})}{s^2 (1 + s/\omega_{p1})} \tag{2.10}$$

where $\omega_{z1} = \frac{1}{R_1 C_1}$ and $\omega_{p1} = \frac{1}{R_1 C_2}$

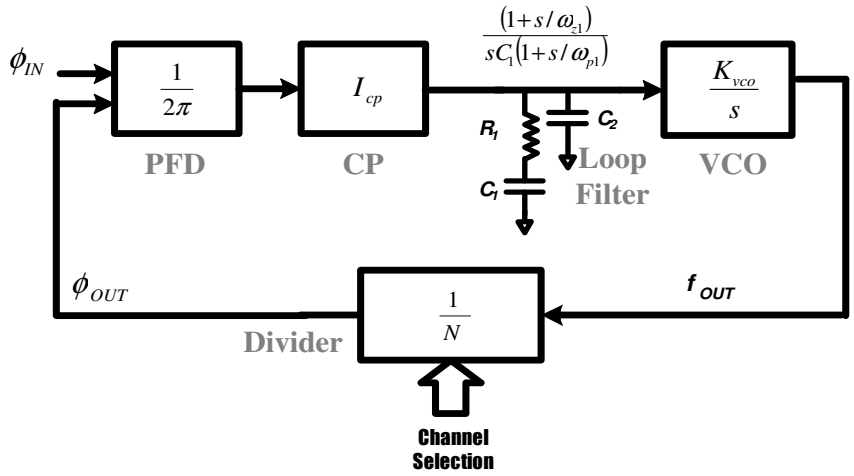


Fig. 2.9 Charge Pump PLL

The closed loop transfer function can be obtained as

$$H_{closed}(s) = \frac{H_{open}(s)}{1 + H_{open}(s)} = \frac{\left(\frac{K_{vco} I_{cp}}{2\pi N C_1}\right)(1 + s/\omega_{z1})}{\frac{s^3}{\omega_{p1}} + s^2 + \left(\frac{K_{vco} I_{cp}}{2\pi N C_1}\right)\frac{s}{\omega_{z1}} + \left(\frac{K_{vco} I_{cp}}{2\pi N C_1}\right)} \tag{2.11}$$

Normally, the pole ω_{p1} is placed beyond the natural frequency ω_n of the system. Therefore, Eqn. 2.11 reduces to a second order system given by Eqn. 2.12.

$$H_{closed}(s) = \frac{\left(\frac{K_{vco} I_{cp}}{2\pi N C_1}\right)(1 + sR_1 C_1)}{s^2 + \left(\frac{K_{vco} I_{cp} R_1}{2\pi N_1}\right)s + \left(\frac{K_{vco} I_{cp}}{2\pi N C_1}\right)} \tag{2.12}$$

This can be compared with the classical second order equation given by Eqn. 2.13

$$H_{II}(s) = \frac{\omega_n^{\,2}}{s^2 + (2\xi\omega_n)s + \omega_n^{\,2}} \tag{2.13}$$

to obtain the critical design parameters given by Eqns. (2.14-16).

$$\omega_n = \sqrt{\frac{K_{vco} I_{cp}}{2\pi N C_1}} \tag{2.14}$$

$$\omega_c = (2\xi\omega_n) = \frac{K_{vco} I_{cp} R_1}{2\pi N} \tag{2.15}$$

$$\xi = \frac{R_1}{2}\sqrt{\frac{K_{vco} I_{cp} C_1}{2\pi N}} \tag{2.16}$$

From Fig 2.10, it can be seen that the exact location of the pole ω_{p1} and the zero ω_{z1} affects the transient dynamics of the entire closed loop. From control theory [23], if

$$\omega_{z1} = \frac{\omega_c}{\alpha^2} \tag{2.17}$$

$$\omega_{p1} = \omega_c \cdot \alpha^2 \tag{2.18}$$

then, $\alpha = 2$ yields $\xi = 1$; the case for critical damping in a II order system. Critical damping leads to a fair compromise between settling time and overshoot.

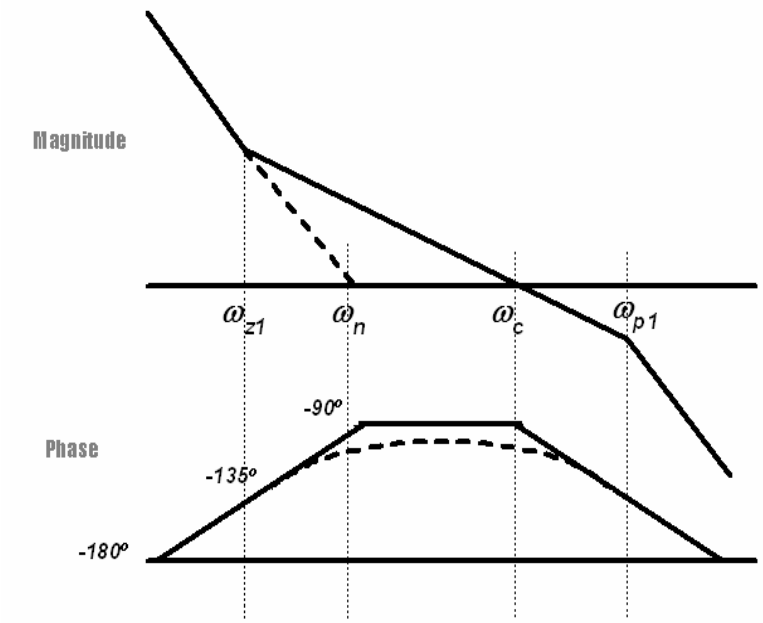


Fig. 2.10 Pole-Zero Placement

2.5.2 Design Procedure

The design procedure followed is optimized after several iterations. The initial set of assumptions are I_{cp}=20 μA and K_{vco}=150 MHz/V. There is a limit on how low the I_{cp} can be set. The leakage from the devices into the critical control line needs to be minimized. A lower current in the charge pump helps in increasing the output impedance of the charge pump.

A low sensitivity of the VCO helps in improving the spectral purity of the VCO by providing low gain to the ripples in the control voltage. It merits mention that the tuning range would be affected with the low sensitivity. Section 4 discusses this issue in detail. Moreover, the desired pole-zero placement technique in the loop filter outlined in the previous sub-section requires $\xi = 1$.

1. Loop Stability

The channel reference frequency is 5 MHz. For the continuous time approximation to be valid, Gardener's stability limit [22] is given by

$$\omega^2{}_n < \frac{\omega^2{}_{ref}}{\pi(\pi + \omega_{ref}/\omega_{z1})} \tag{2.19}$$

For a critically damped system, $\omega_c \approx \frac{\omega^2{}_n}{\omega_{z1}}$. Therefore, the Gardener's stability limit is now given by

$$\omega_c < \frac{\omega_{ref}}{\pi(1 + \pi\omega_{z1}/\omega_{ref})} \tag{2.20}$$

A low loop bandwidth improves the spur attenuation and minimizes the noise bandwidth at the expense of a high settling time. It is related to the natural frequency of the PLL system by

$$\omega_n = \frac{\omega_c}{2\xi} \tag{2.21}$$

A natural frequency of 15 KHz is a good starting point in the design. This gives the loop bandwidth to be

$$\omega_c = 2\xi\omega_n = 2\pi \cdot 30 Krps \tag{2.22}$$

The pole and zero placement technique for critical damping gives

$$\omega_{z1} = \frac{\omega_c}{2^2} = 2\pi \cdot (7.5) Krps \tag{2.23}$$

$$\omega_{p1} = \omega_c \cdot 2^2 = 2\pi \cdot 120 Krps \tag{2.24}$$

The phase margin is given as

$$PM = \tan^{-1}\left(\frac{\omega_c}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p1}}\right) = \tan^{-1}(4) - \tan^{-1}\left(\frac{1}{4}\right) = 61.92^0 \tag{2.25}$$

Using the above values, from Gardener's stability limit, we obtain

$$\omega_c < \frac{\omega_{ref}}{\pi(1+\pi\omega_{z1}/\omega_{ref})} \approx \frac{\omega_{ref}}{\pi} \tag{2.26}$$

Thus, the minimum value of the loop bandwidth to satisfy the continuous time approximation is $2\pi \cdot (1.584) Mrps$. Thus, the actual loop bandwidth is around 52 times lower than the one stipulated by Gardener's stability limit.

2. Loop Filter Parameters

The natural frequency is given as

$$\omega_n = \sqrt{\frac{I_{cp} K_{vco}}{2\pi N C_1}} \Rightarrow C_1 = \frac{I_{cp} K_{vco}}{2\pi N \omega^2_n} \tag{2.27}$$

$$\therefore C_1 = \frac{\left(20\times10^{-6}\right)\times\left(2\pi\times150\times10^6\right)}{2\pi\times(976)\times\left(2\pi\times15\times10^3\right)^2} = 346 pF \tag{2.28}$$

N is taken as an average of 960-992. It will be explained in Section 3 about the need for doubling the divide ratios.

$$\omega_{z1} = \frac{1}{R_1 C_1} \Rightarrow R_1 = 61.33 K\Omega \tag{2.29}$$

$$\omega_{p1} = \frac{1}{R_1 C_2} \Rightarrow C_2 = 21.625\,pF \tag{2.30}$$

It can be seen that $\frac{C_1}{C_2} = 16$.

3. Settling time

For critically damped case, the settling time is given by [24-25]

$$t_{lock} = \frac{1}{\xi\omega_n} \ln\left(\frac{\Delta f}{\alpha f_0}\right) \tag{2.31}$$

where Δf is the maximum frequency switching, here 160 MHz

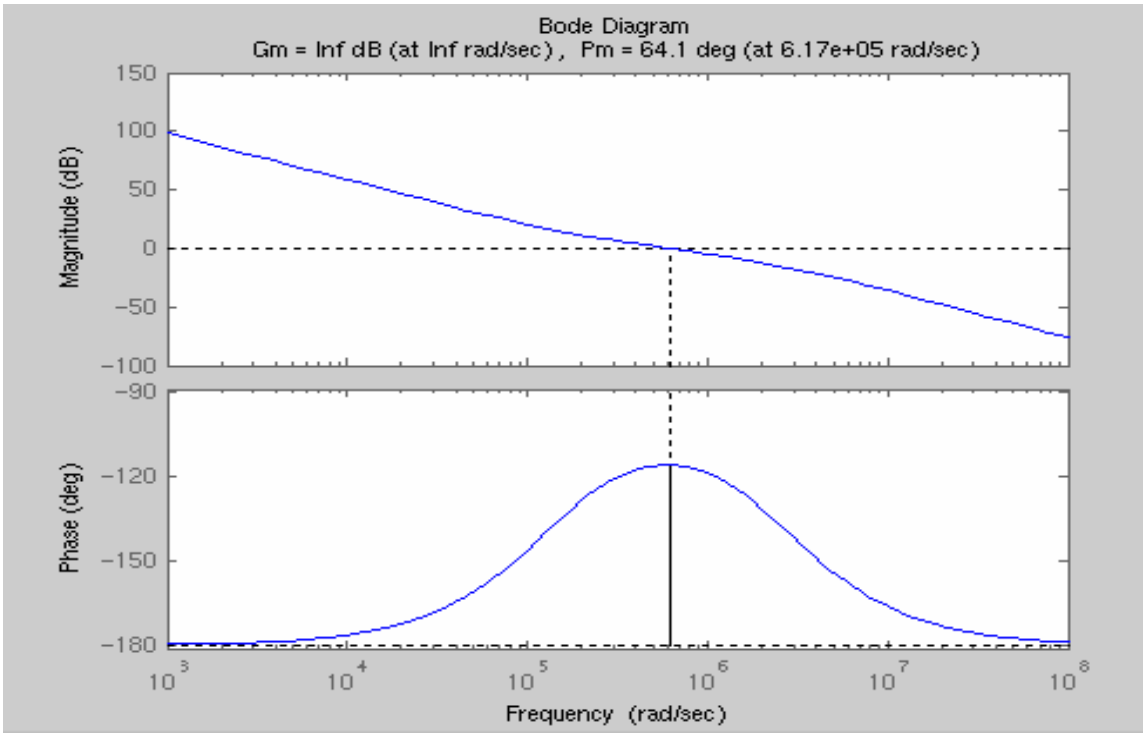
α is the desired frequency accuracy, here 40 ppm

It is found that t_{lock} is 71.4 μs, which is 37% of the actual specification. It must be remembered that the settling time equation is only approximate, and over-designing for the settling time is necessary.

2.5.3 System Level Verification

The above design is verified using MATLAB and SystemView. The open loop transfer function is given by

$$A_{OL} = \frac{K_{vco} I_{cp}}{2\pi C_1 N \cdot s^2}\left(\frac{\omega_{p1}}{\omega_{z1}}\right)\left\{\frac{s+\omega_{z1}}{s+\omega_{p1}}\right\} = \frac{1.61\times10^{12}}{s^2}\left\{\frac{s+137\times10^6}{s+2.6\times10^6}\right\} \tag{2.32}$$



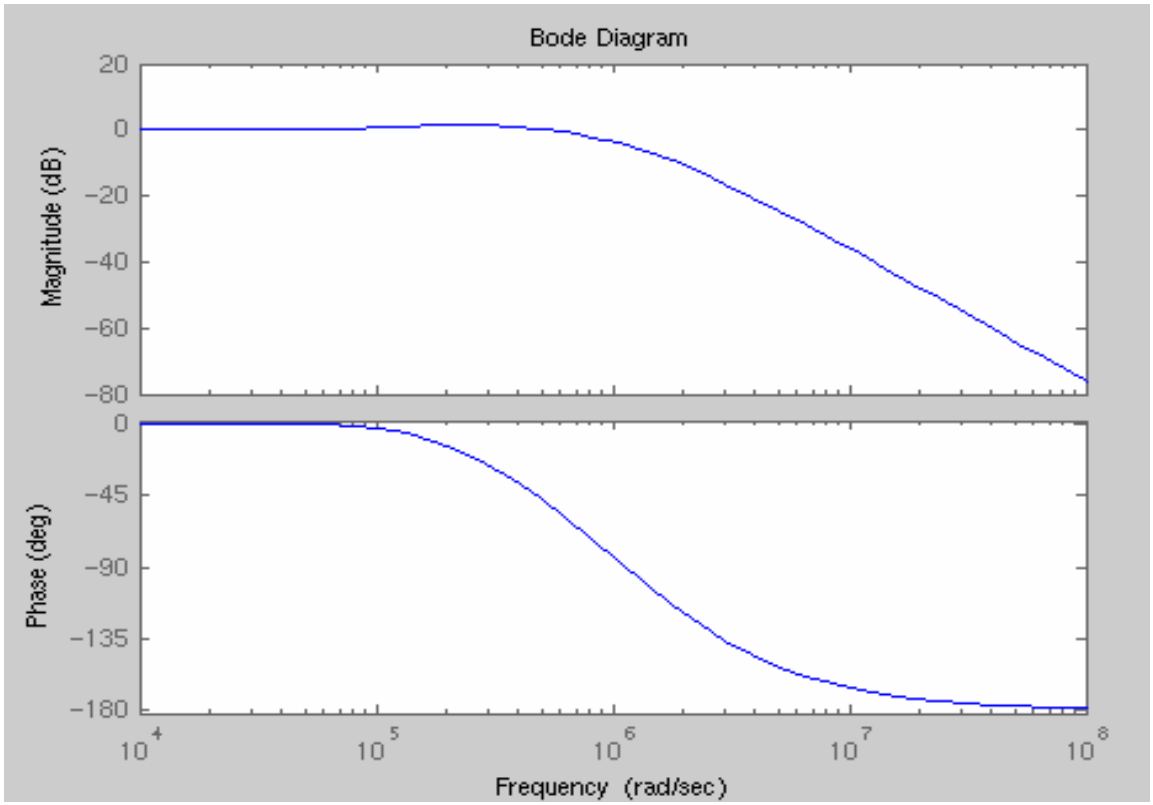


Fig. 2.11. Bode Plots (a) Open Loop (b) Closed Loop for the PLL

The MATLAB Bode plots for the open loop and the closed loop of the designed PLL is are given in Fig. 2.11. The phase margin is found to be in agreement with the hand calculations. Further, it can be seen that the Bode plot of the error transfer function of the closed loop is as expected.

Transient response for impulse, step and ramp inputs can be obtained using MATLAB. However, the approximations behind Eqn. (2.32) must be remembered. This analysis gives a good starting point in the design.

The SystemView setup is given in Fig. 2.12. Based on the loop filter parameters calculated in the previous sub-section and the assumed variables I_{cp} and K_{vco}, the given setup is simulated for settling behavior.

Token 0 provides the reference of 5 MHz for the PLL while token 1 is for the Phase/ Frequency detect operation. The charge pump is emulated using tokens 2, 4 and 5. Token 7 accounts for the loop filter in the design. The VCO is modeled using a frequency modulator with the given sensitivity and free running frequency using token 3. The dividers is modeled using token 6 and varies from 962-992 for the Zigbee operation. Token 13 is to tap the control voltage of the VCO to monitor the settling behavior of the PLL.

As per the setup given in Fig. 2.12, the VCO is initially operating at 4.6 GHz. The divide ratio is 960 and the reference is 5 MHz. The PLL now needs to lock to 4.8 GHz. Fig. 2.13 provides the transient response of the PLL by showing the control voltage settling behavior.

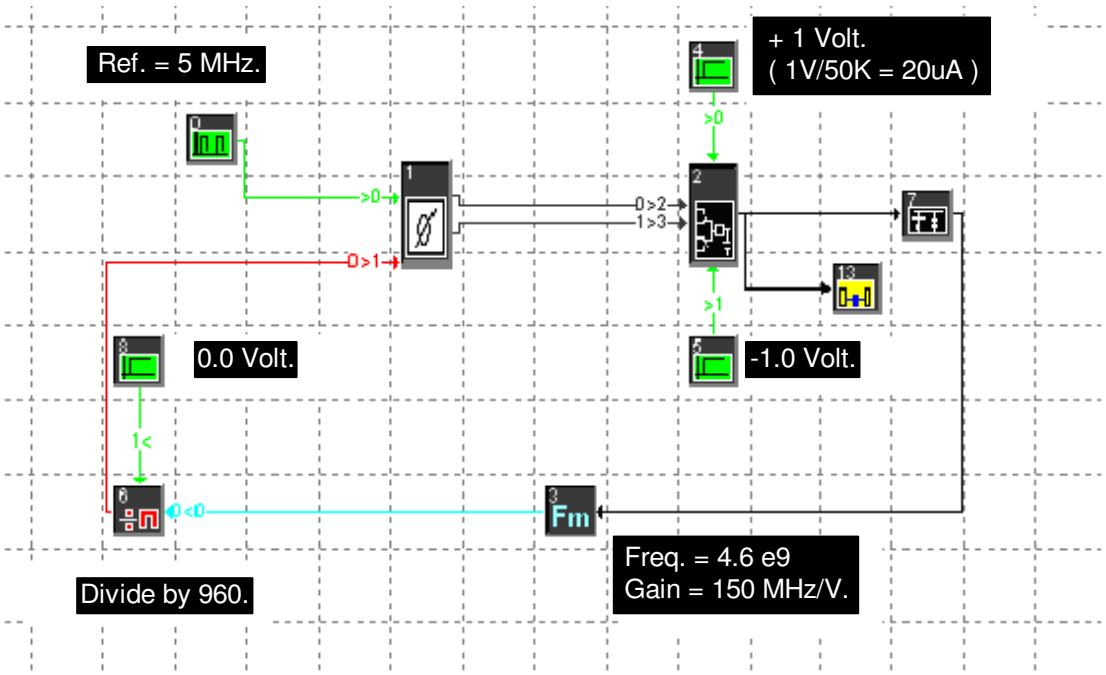


Fig. 2.12. SystemView Setup for PLL Design Verification

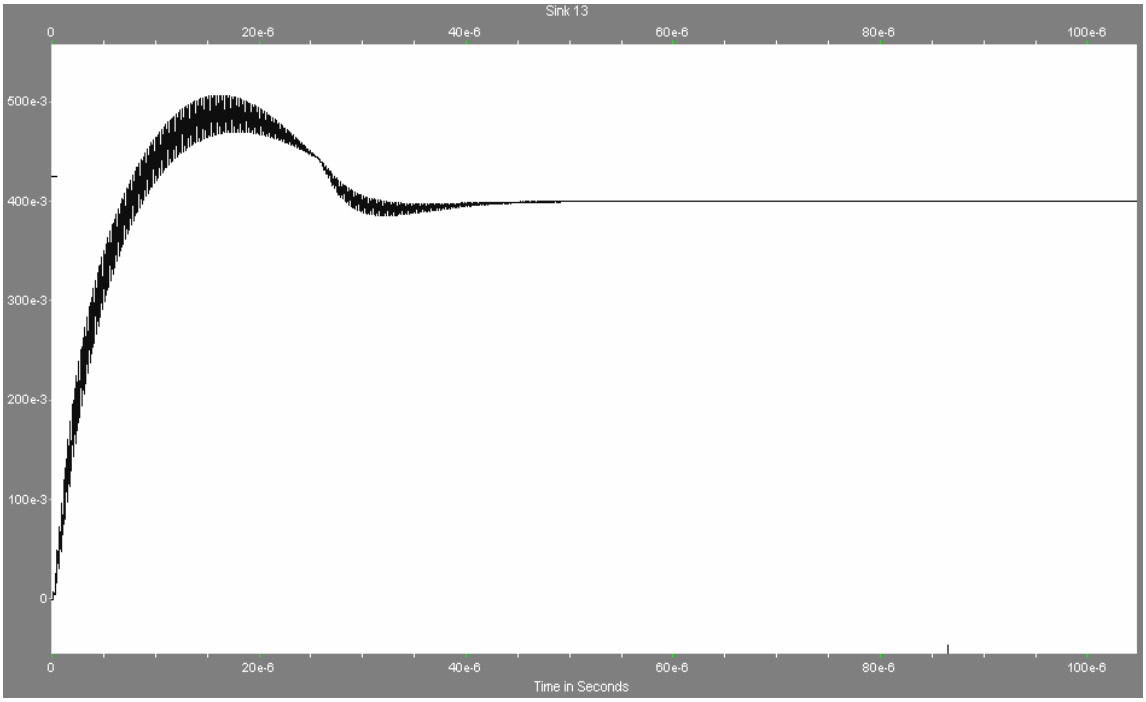


Fig. 2.13 Transient Settling Behavior for the PLL Using SystemView

It merits mention that the system level verification methods used do not account for the discrete nature of the PLL. The actual integrated circuit implementation needs to take into account various parasitic and non-ideal effects and are discussed where relevant in the subsequent sections. At the same time, the importance of the system level design needs to be emphasized.

This section lays the foundation for the actual practical implementation for the PLL based synthesizer. Other methods for system level simulations exist – Cadence based simulations using Verilog and ideal models, and Analog verilog coding. Non-idealities can also be introduced into the existing holistic models used in MATLAB and SystemView.

2.6 Literature Survey

The frequency synthesizer is one of the crucial blocks of the transceiver. The entire translation in frequency is dependent on the LO provided by the synthesizer in the transceiver. It is one of the power-hungry blocks of the transceiver. Most synthesizers are implemented as integer-N or fractional-N PLL applications [24-29]. The locked tone of the PLL is used to synthesize multiple frequencies [30]. Further, injection locking phenomena is used for frequency synthesis [31].

The high-frequency blocks VCO and dividers have received special attention over the recent years [20, 21, 31-34]. Fast settling time [35-36], spur suppression [5, 37], and low jitter [38], spectral purity [39] have been important bottlenecks in the design of synthesizers. Dual-loop architectures for fast settling time are also popular [40-41]. Reference spur optimization techniques heavily depend on superior charge pump

performance and excellent power routing and isolation from substrate noise. Spurs and phase noise are crucial in high-performance systems [27, 39].

The requirements for the synthesizer vary from one standard to another. Usually, in wireless systems, power consumption is a very critical issue, as it is always desired to have a long battery life. However, for systems that require high spectral purity, high power consumption in the VCO becomes inevitable to achieve such stringent phase noise specification [27, 39]. It has been shown that injection-locking phenomena can be used to achieve improved phase noise PLL systems [42]. Synthesizers in multi-standard transceiver applications have also been reported [43-44]. Thus, it can be seen that the synthesizer has been a research topic of constant focus and attention.

With the advent of technology scaling, supply voltages have decreased. The effect of scaling is pronounced in the design of high-performance synthesizers in wireless transceivers. On the other hand, technology scaling has increased the f_T of the devices, benefiting the design of high-performance of 2.4 GHz and 5 GHz systems. A complete integrated solution of a synthesizer with high spectral purity, spur suppression and low power consumption is a challenge in high f_T technologies.

Moreover, scaling reduces the tuning control voltage range of the VCO; thereby demanding a high VCO sensitivity [11]. On-chip voltage doubler is used to increase the tuning control voltage range in [45]. In charge-pump based PLL systems, the locking range is often limited by the tuning control voltage range [7]. Hence, for broadband synthesizers, it is important to achieve high tuning range [46].

Reference [3] reports a synthesizer for a low-data rate standard, similar to Zigbee. The use of true single phase clocking scheme in the prescaler is explored in [47]. An 802.11a synthesizer based on the principle of transformer coupling achieves a power

consumption of 9.7 mW in [48]. Low-voltage design techniques have been incorporated in the design of a 1-V frequency synthesizer in [49]. Recently, a Zigbee frequency synthesizer has been reported with a power consumption of 22 mW in 0.18 μm technology (based on simulation results) [5].

This work successfully explores the application of low sensitivity VCOs with a high tuning range using a TSMC 0.18 μm CMOS process in a 5 GHz frequency synthesizer. It is also intended for applications in a 2.4 GHz Zigbee transceiver, requiring a low-power, low-cost complete integrated solution.

3. FREQUENCY SYNTHESIZER DESIGN

This section forms the crux of this thesis and deals with the practical design and implementation of a frequency synthesizer in a plain CMOS technology. It provides a practical solution to the development of the synthesizer after the system level progress made in Section 3. The architecture is given here, for the sake of completeness, and in more detail. The individual building blocks along with the germane implementation issues are discussed in this section. The VCO is discussed in more detail in the next section. The important layout and board-level issues are given along with the measurement results of the silicon prototype.

3.1 Synthesizer Architecture

The integer-N PLL based synthesizer circuit implementation with all the building blocks is given in Fig. 3.1. As discussed in Section 2, the synthesizer can be broadly classified into three sub-systems for the purpose of design and efficient simulations. The three systems are (i) core analog system consisting of the phase/ frequency detector, charge pump, loop filter, loop filter buffer (ii) RF system of the voltage controlled oscillator and the CML divide-by-2 (iii) digital system consisting of the prescaler and pulse/ swallow counters. It merits mention that the three sub-systems have different power supplies. It is usually a good practice to isolate the power supplies of the analog and the digital sections to minimize noise interactions through the medium of the substrate.

For purposes of measuring settling time and control voltage during the lock state of the PLL, the output voltage node of the charge pump is tapped. Open-drain buffers are

used to “tap” the high frequency outputs of the VCO (4.8 GHz) and the CML divide-by-2 (2.4 GHz). It merits mention that the main purpose of a synthesizer is the generation of I and Q components of the LO for upconversion/ downconversion at the mixer. For the worst case scenario of the synthesizer failing to lock to the required channel frequency, we need to ensure that the mixer still gets the LO input. Therefore, an additional CML divide-by-2 is provided to generate I and Q components from an external source for it is difficult to obtain them directly from the instrument.

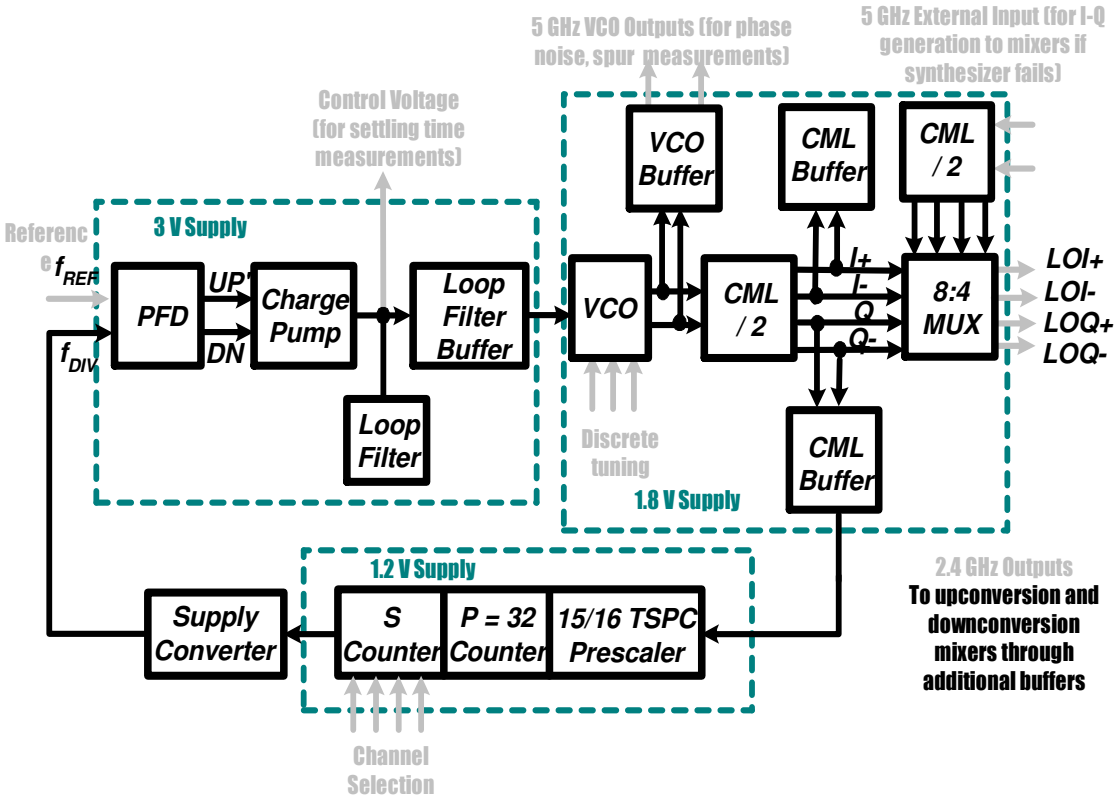


Fig. 3.1 Architecture of the Frequency Synthesizer

The output of the CML divide-by-2 used in the synthesizer loop is multiplexed with the output of the CML divide-by-2 for test purposes. Additionally, this test CML

divide-by-2 can be used for the characterization of a stand-alone CML divide-by-2. The power consumption of the frequency synthesizer need not include the test CML divide-by-2, the VCO output buffer for test purposes, the portion of the multiplexer driving the test CML divide-by-2.

3.2 Phase/Frequency Detector

3.2.1 Topology

A *nand*-based tri-state Phase/Frequency Detector (PFD) is used to perform the role of phase/ frequency detection in the synthesizer. The PFD compares the divider output with that of the reference clock. It is capable of frequency detection during the coarse acquisition phase and phase detection during the fine acquisition phase. Other topologies exist for phase/ frequency detection.

The implemented scheme is capable of performing both frequency and phase detections. The only drawback of this approach is the frequency limitation determined by the static CMOS implementation (typically 500 MHz). We would be operating at 5 MHz and this architecture is best suited for such synthesizer applications. The selection of the scheme is entirely dependent on the typical application.

This principle of phase/ frequency detection fails in a clock and data recovery (CDR) environment. For high frequency phase detection for random data in CDR circuits, Hogge detectors are used [50-51, 11-12]. Gilbert cell based mixers and XOR gates are used for high frequency phase detectors in synthesizers [10].

The PFD generates two important signals, namely the *UP* and *DN*, which represent the difference in phase/ frequency of the two inputs. The two signals are named figuratively. The *UP* signal is used as an indicator for increasing the VCO frequency

(which is made possible by an increase in the control voltage). Similarly, the *DN* signal is used for decreasing the VCO frequency. The reader is encouraged to refer to the literature for a detailed analysis of the PFD [52].

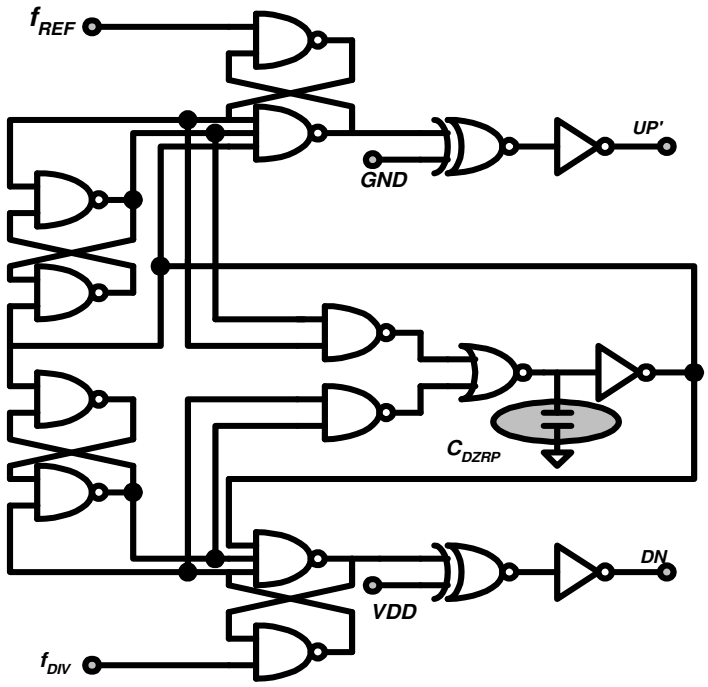


Fig. 3.2 Topology of the Phase/ Frequency Detector

We need a method that converts the critical phase/ frequency difference information in the *UP* and *DN* signals to useful voltage related information. The charge pump along with the loop filter performs this operation. It is seen that the final optimization be done with the three blocks in cascade. These three blocks need to be considered together using the tool of transient analysis. Usually, $\overline{UP}$ and *DN* are connected to the PMOS and NMOS transistors of the charge pump. The timing mismatch

between $\overline{UP}$ and DN needs to be minimized. This is done by the use of EXOR gates, keeping these Boolean identities in mind:

$$X \oplus 1 = \overline{X} \text{ and } X \oplus 0 = X \qquad (3.1, 3.2)$$

Further, these individual gates must be laid out in a symmetric fashion to minimize the timing delays. Fig. 3.2 gives the gate level schematic of the PFD.

3.2.2 Dead zone

Dead zone is one of the crucial aspects of the PFD design and is elaborately discussed in [10]. It can be briefly summarized as that region of operation of the PFD where the PLL loop fails to respond to the phase error at the input. Thus, the critical VCO output is allowed to drift away in open loop. In practical integrated circuit implementations, the dead zone is alleviated by the dead-zone removal pulse (DZRP). When both UP and DN is ON, the reset path becomes active and forces them to the OFF states. The finite gate delays in the reset path are responsible for τ_{DZRP}. The DZRP has its own merit and drawback in the overall synthesizer; hence τ_{DZRP} must be judiciously set.

When the PLL is in the locked state, the divider output and the reference phase are identical in frequency with a possible constant phase error between them. In the absence of any DZRP, the system is in open loop. The PFD-Charge Pump fails to track the drift in the VCO. Consider the hypothetical situation where UP is ON and DN is OFF. Then, DN is becoming ON. For a small τ_{DZRP}, there is unequal charge injection into the loop filter through the charge pump. This leads to ripples in the control voltage and spurs at the output. If the charge injected is high, the system might be temporarily out of lock.

If τ_{DZRP} is appropriately sized, the UP and DN conduct equally. Ideally, no charge is injected into the loop filter. However, during this time, the critical control voltage is susceptible to the noise and supply variations from the power rails. Hence, a high τ_{DZRP} is not desirable; in direct contradiction to the requirement from a current matching point of view. It merits mention that DZRP forces the system to be in closed loop during the locked state. Thus, the phase comparison during each reference prevents the excessive drifting of the VCO [11].

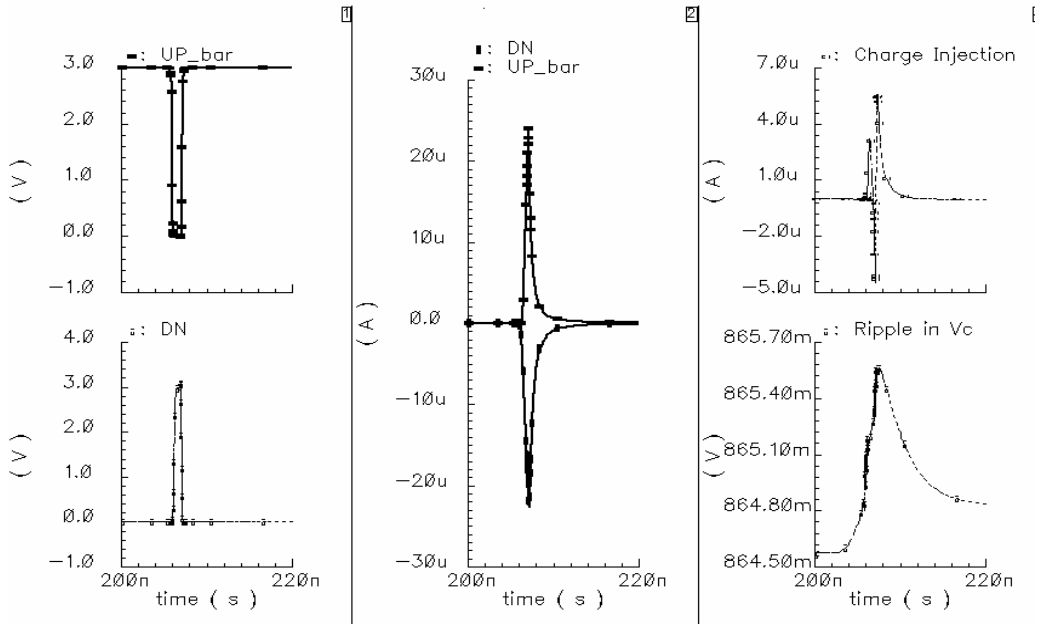


Fig. 3.3 Ripples in the Control Voltage

Fig. 3.3 gives the post-layout transient simulation results of the core analog system consisting of the PFD, charge pump and loop filter. This design uses τ_{DZRP} of 2ns, which translates to 1% of the total reference time. The capacitor C_{DZRP} (equal to 60fF)

placed on purpose in the delay path helps in sizing the DZRP. τ_{DZRP} varies with the process corners and the worst case is during the fast corner, where it is around 1.4 ns.

A small τ_{DZRP} requires a high charging time for the UP and DN switches of the charge pump, thereby imposing added performance requirements. Further it can be seen from Fig. 3.3 that current mismatch is inevitable due to realistic charging times for the switches of the charge pump. The unequal charge injection leads to ripples in the control voltage line. These ripples are responsible for the appearance of reference spurs at the VCO spectrum.

TABLE V
PHASE FREQUENCY DETECTOR – SPECIFICATIONS

Performance Metric	*Value*
Gain	1/2π
Reference Input Frequency	5 MHz
τ_{DZRP}	2 ns.
Timing Mismatch between UP' and DN	Minimum
Supply Voltage	3 V

In the next section, we will discuss the non-ideal effects of the charge pump, especially during τ_{DZRP}. The non-ideal effects further deteriorate the performance of the charge pump during DZRP. Finally, the phase frequency detector specifications are summarized in Table V.

3.3 Charge Pump

Functionally, a charge pump transforms the time domain information present in the UP and DN pulses of the PFD to voltage related information by pumping/ extracting

charge into/ from the loop filter. The simplest charge pump topology is given in Fig. 3.4(a). It consists of a capacitive load C_1 that contributes to a pole at the origin (Eqn. 3.3). Thus, if one of the signals were to be absent at the input of the PFD, the infinite gain at DC will make the control voltage hit the supply rails. Fig. 3.4(b) gives an accurate charge pump model with a realistic loop filter. As seen from Eqn. 3.4, the premise of a pole at the origin continues to hold true [11].

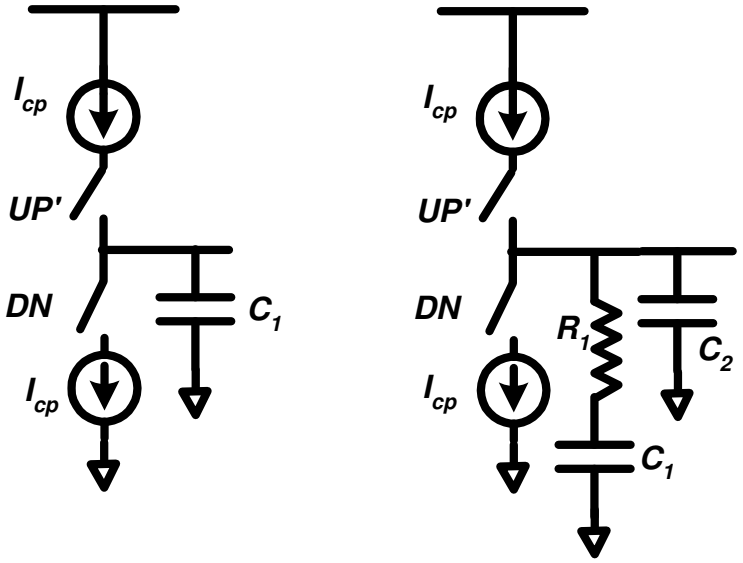


Fig. 3.4 Charge Pump Model with the Loop Filter (a) Conceptual (b) Actual

$$K_{cp} = \frac{I_{cp}}{2\pi\left(sC_1\right)} \tag{3.3}$$

$$K_{cp} = \frac{I_{cp}}{2\pi}\left(\left\{R_1 + \frac{1}{sC_1}\right\}\middle\|\frac{1}{sC_2}\right) \approx \frac{I_{cp}}{2\pi s}\frac{\left(1+s/\omega_{z1}\right)}{\left(1+s/\omega_{p1}\right)} \tag{3.4}$$

The most important characteristic of a charge-pump is its immunity to variations at its output node, which is the control voltage of the synthesizer. Conventional charge

pumps suffer from the issues of high sensitivity to the output node voltage and charge sharing. Moreover, for accurate current matching during the UP and DN stages, it is best to use low-voltage cascode current mirrors. As discussed in the previous section, accurate current matching is very critical during τ_{DZRP}. It becomes extremely important to have the behavior of the UP and DN current sources immune to the variations in the output node (the control voltage of the VCO). The synthesizer operation makes the variation in the output node of the charge pump essential [11].

For purposes of obtaining a reasonable tuning range at low sensitivity for the VCO, we need to have a high tuning control voltage range. In a charge pump design at 1.8V, it will be impossible to obtain a tuning control voltage range of 1.5V as desired. Thus to achieve a good tuning control voltage range and current matching, the charge pump is implemented in a 3V domain using 3V devices. The choice of 3V supply is justified because of the improved performance at the cost of a minimal increase in the power consumption. From the system level design procedure in Section 2, the charge pump current is taken as 20 μA.

The charge pump is responsible for the reference spurs seen at the output of the VCO. An accurate well-designed charge pump is essential for minimizing spurs at the output. The spurs appear at the output of the synthesizer at an offset frequency equal to that of the reference. When the PLL is in locked condition, the DZRP appears at a frequency equal to the reference. The two currents related to UP and DN need to be matched very well.

From Fig. 3.3, it can be seen that realistic circuit implementations have a finite mismatch because of difference in charging and discharging of the PMOS and NMOS

devices. This finite mismatch leads to ripples in the control voltage. The ripples modulate the control voltage, which leads to the spurs at the output spectrum. Thus, the presence of reference spurs is an inherent drawback of the PFD-CP based PLL.

Fig. 3.5 gives the circuit implementation of the charge pump [53]. The charge pump operates with a supply voltage of 3V. It is important to note the range of output control voltages allowable for the charge pump. We would like to minimize the dependence of the UP and DN currents on the output node voltage. Low-voltage cascode mirrors are used to minimize the headroom and improve the matching between the UP and DN transistors.

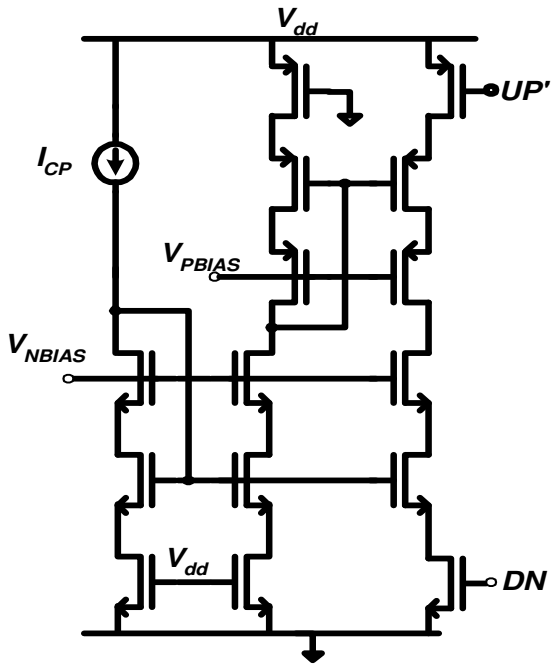


Fig. 3.5 Charge Pump – Topology

The devices are sized iteratively based on transient simulation results. It is important to have long devices so as to improve their output impedance. Post layout

simulations show that the charge pump operates with minimal dependence on the output node voltage ranging from 0.5 to 2.5V. This translates to the allowable tuning control voltage range for the VCO. The headroom of the PMOS and NMOS low-voltage cascode mirrors limits this output voltage range.

TABLE VI
CHARGE PUMP – SPECIFICATIONS

Performance Metric	*Value*
Gain	20 μA
τ_{DZRP}	2 ns.
Dynamic Range	0.5 to 2.5 V
Output Impedance	High
Supply Voltage	3 V

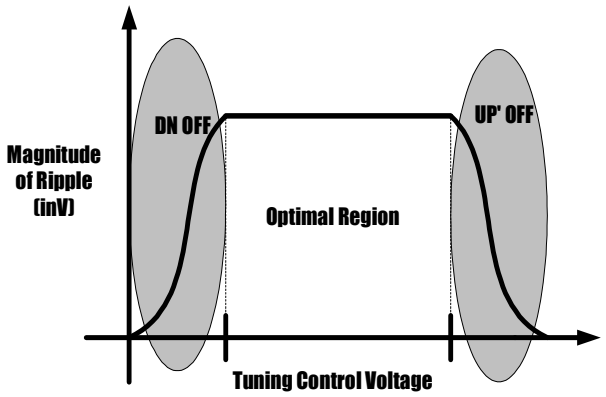


Fig. 3.6 Charge Pump Behavior with Varying Output Voltage

Fig. 3.6 graphically describes the charge pump behavior with varying control voltage of the synthesizer. For voltages below 0.5V, the NMOS cascode current source fails to accurately match the charge pump current of 20 μA. Similarly mismatch beyond 2.5V increases due to the PMOS cascode current source. The increase in mismatch

between the UP' and DN current sources leads to increased ripples in the control voltage; leading to higher reference spurs. The charge pump specifications are given in Table VI.

3.4 Loop Filter

Section 2 deals with the loop filter design at the system level. After considering the settling time and stability paradigms, the loop filter parameters can be obtained as R_1=62K, C_1=346 pF, C_2=21.625 pF. An on-chip implementation is necessary for the complete monolithic integrated solution of the transceiver. The conceptual representation of the loop filter is given in Fig. 3.7.

From Section 2, it can be seen that the loop filter parameters are responsible for settling time, damping ratio, pole-zero locations, phase margin, etc. of the overall synthesizer loop. It is therefore extremely important to ensure robustness of the loop filter for an on-chip implementation. This necessitates that the overall system be tested across all process corners. The process variations can be taken as ± 30 % for purposes of system level simulations using Matlab or SystemView.

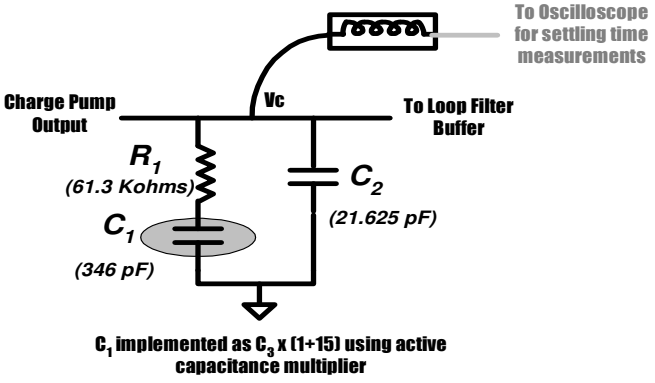


Fig. 3.7 Loop Filter – Conceptual Diagram with Parameters

The resistor R_1 is implemented using poly. The area occupied by this resistor implementation is low due to the high resistivity of the material. The capacitor implementation is not as straightforward. Among the various types of capacitors available, the metal-insulator-metal (MIM) capacitors have the highest accuracy and least sensitivity to process variations. It merits mention that the variation can still be as high as 20%. Moreover, the MIM implementations suffer from an extremely low density. Approximately, a 0.9pF capacitor occupies an area of 30µm by 30µm. The area occupied by C_1 is 560µm by 560µm. With the active emulation technique, the area occupied by "C_1" is 250 µm by 325 µm.

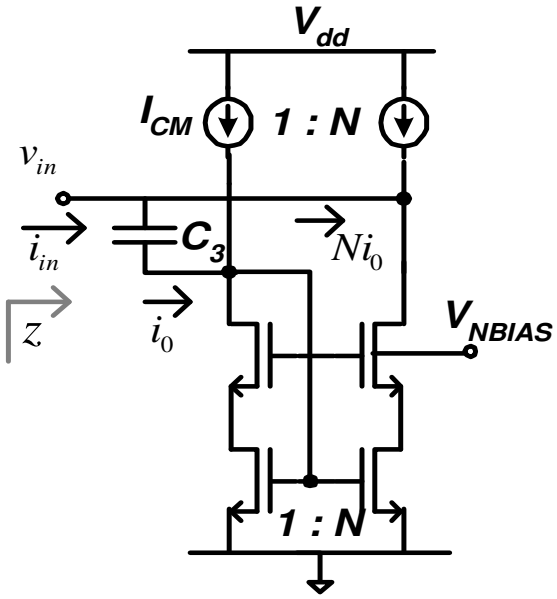


Fig. 3.8 Capacitance Emulation of C_1=346 pF

To have a large spur attenuation, low bandwidth and stability of the PLL feedback system, a high capacitance value for C_1 is desired [8, 11]. However, on-chip implementations have the constraint of area too. An active capacitance emulation

technique [54, 28] can be used to minimize the area. The reader is encouraged to read [54, 28, and 24] for a complete understanding of the emulation, the frequency limitations thereof and the design considerations. From Fig. 3.8, it can be seen that the small signal current (i_0) flowing through the capacitor C, is mirrored N times; and the total current being extracted from the node A is $(1+N)\, i_0$. Thus the effective impedance at A is given as

$$z = \frac{1}{sC_3(1+N)} = \frac{1}{sC_1} \tag{3.5}$$

The bias current I_{B1} is taken as 5μA. The overall power consumption of the active capacitance multiplier is in the μW range. The loop filter needs to be capable of sustaining the charge being injected/ extracted during τ_{DZRP}. This poses a constraint on the minimum bias current. Further, a high bias current reduces the output impedance of the current mirrors. This reduces the finite output resistance of the capacitance multiplier and increases the leakage current.

TABLE VII
LOOP FILTER – SPECIFICATIONS

Performance Metric	*Value*
R_1	61.33 KΩ
C_1	346 pF ($16C_2$)
C_2	21.625 pF
Leakage Current	Minimum
Capacitance Multiplier	N=15
Current Bias in Multiplier	5 μA
Supply Voltage	3 V

It can be seen that $C_3=C_2$, when N=15. Thus, layout techniques such as common centroid can be employed to minimize mismatch between C2 and C3. The layout of the loop filter is given in Fig. 3.9. The area occupied is 325 µm by 250 µm. The filter specifications are summarized in Table VII.

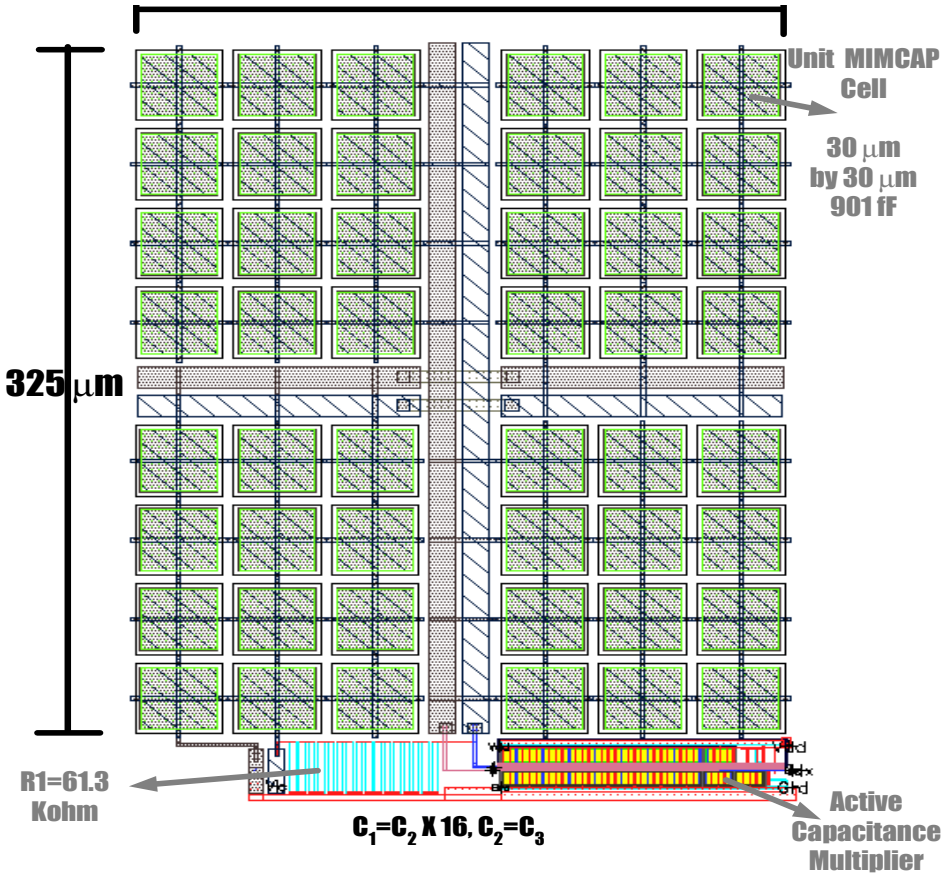


Fig. 3.9 Layout of the Loop Filter

3.5 Loop Filter Buffer

A loop filter buffer is placed between the loop filter and the VCO to improve the reverse isolation from the high amplitude-oscillating node. The varactors are leaky and have finite impedance to the high frequency signal. Thus, there is a high frequency

component at the output of the charge pump (input of the loop filter buffer). The VCO has a distinctive band pass nature given by the Q of the tank. When the VCO is operating at 5 GHz, the common mode oscillation at the control voltage is 10 GHz. Thus, the effect of a 10 GHz component at the control voltage might not be detrimental to the VCO.

The buffer is implemented using a differential pair in unity gain feedback as shown in Fig. 3.10. It consumes a portion of the permissible control voltage range of the VCO to ensure its own safe operation. With the buffer, the tuning control voltage range becomes 1-2.5 V, a clear reduction of 0.5V. Thus, the loop filter buffer might not be essential for this case.

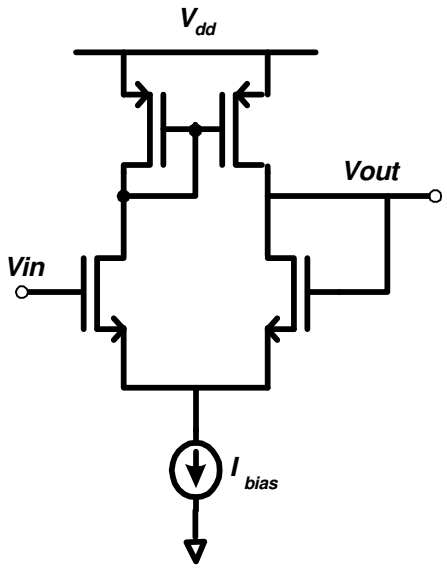


Fig. 3.10 Loop Filter Buffer

However, it merits mention that the *Gm-*C_{load} implementation of the buffer gives rise to an additional pole in the loop filter. It improves the spur attenuation by an additional –20 dB. The thermal noise of the transistors in the buffer will affect the performance of the VCO, and the devices are sized with large gate lengths to minimize

the flicker noise. This method is superior to an R-C filter system if the noise introduces happens to be less than that of R. The buffer specifications are summarized in Table VIII.

TABLE VIII
LOOP FILTER BUFFER– SPECIFICATIONS

Performance Metric	*Value*
Gm/C_{load}	> 1.25 MHz
Dynamic Range	1 to 2.5V
Reverse Isolation	- 20 dB
Power Consumption	Minimum
Supply Voltage	3 V

3.6 Voltage Controlled Oscillator

The voltage-controlled oscillator is one of the most crucial blocks of the synthesizer. A complete treatment of the issues in a VCO is necessary and the next section is dedicated to the VCO. The VCO has a tuning range of 685 MHz from 4580-5275 MHz with an average sensitivity of 135 MHz/V. Thus, the VCO designed in Section 4 meets the requirements of the VCO for the synthesizer. A brief summary of the VCO specifications is provided in Table IX.

Due to process variations, if the VCO is to operate at lower or higher frequencies than the desired range from 4800-4960 MHz, the discrete tuning mechanism will shift the entire VCO tuning band to the desired range. It needs to be mentioned that the broadband nature of the VCO can be observed by the use of discrete tuning range steps. Since the tuning range of the VCO normally limits the locking range of a synthesizer, the VCO can be used in any 5 GHz synthesizer environment to provide frequencies spanning across the observed broadband tuning range from 4580-5275 MHz.

Further, it merits mention that the VCO amplitude and the sensitivity vary for each discrete tuning control case. An amplitude control mechanism is given in [55].

TABLE IX
VOLTAGE CONTROLLED OSCILLATOR– SPECIFICATIONS

Performance Metric	*Value*
VCO Sensitivity	150 MHz/V
Tuning Frequency Range	4600-5200 MHz
Tuning Control Voltage Range	1-2.5 V
Phase Noise	- 113 dBc at 10 MHz offset
Supply Voltage	1.8 V

3.7 Frequency Divider[††]

The frequency divider is mainly responsible for the translation of GHz range frequencies obtained from the output of the VCO to MHz range frequencies for phase/ frequency comparison at PFD. Typical PFD architectures work till 150 MHz-200 MHz. Hence, frequency division is inevitable in GHz synthesizer systems. The divider is implemented using prescaler based pulse-swallow architecture [13] and is given in Fig. 3.11. The initial divide by 2 operations needed for I and Q generation gives us a frequency range from 2405-2480 MHz.

The divide ratios vary from 481-496 to obtain the 16 channels of the synthesizer. These ratios can be implemented using 15/16 prescaler, P=32 counter, S=1-16 counter. The first divide-by-2 is implemented using Current Mode Logic and uses a 1.8 supply. The prescaler is implemented using True Single Phase Clocking Logic. It merits mention that the prescaler is single ended while the divide by 2 is of differential nature. This leads to unequal loading at the output of the divide by 2. This affects the I-Q mismatch properties of the divide by 2 and is a critical concern in the design.

[††] The subsection on the divider is being written for the sake of completeness. The author acknowledges the permission obtained from his colleague, Ms. Didem Zeliha Turker.

The P and S counters are in standard CMOS static logic. The prescaler and the counters operate on a 1.2 supply. There is a supply converter from 1.2V to 3V to ensure a 3V-feedback signal from the divider at the input of the PFD. The use of different power supplies is justified because we can assume that there is one on-chip-regulated supply and that these supplies are derived from the single supply.

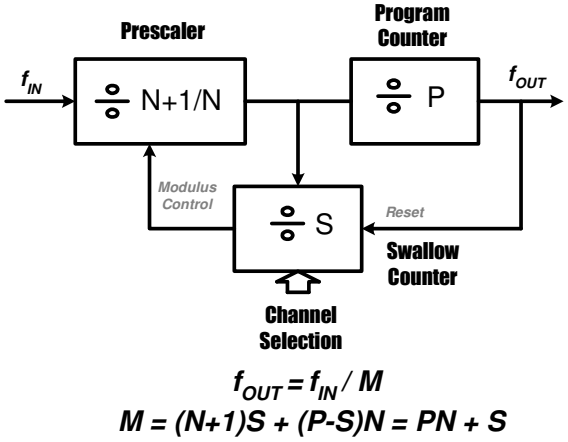


Fig. 3.11 Frequency Divider – Topology

TABLE X
FREQUENCY DIVIDER– SPECIFICATIONS

Performance Metric	*Value*
Divide Ratio	960-992
I-Q Mismatch from divide by 2	$< 5^{o}$
Power Consumption	Minimum
Supply Voltage	1.8 V, 1.2V, 3V

Moreover, the use of different supplies helps us in minimizing the power consumption of the synthesizer. Additionally, the analog section of PFD-CP-LF-LFB is separated from the digital sections of the prescaler and counters for improved noise isolation. The specifications are summarized in Table X.

3.8 Layout Issues

3.8.1 Floor Plan

The layout of the entire taped out chip is given in Fig. 3.12. The chip is designed in the six metal TSMC 0.18 μm process. The die size is 2.5 mm by 2.5 mm and the chip is packaged in a TQFP64 technology. Post layout simulations are performed after taking into consideration the effect of bond-wires and realistic supplies. The entire chip consists of four sections; namely the standalone synthesizer, VCO with its load, prescaler and the on-chip power supply capacitors.

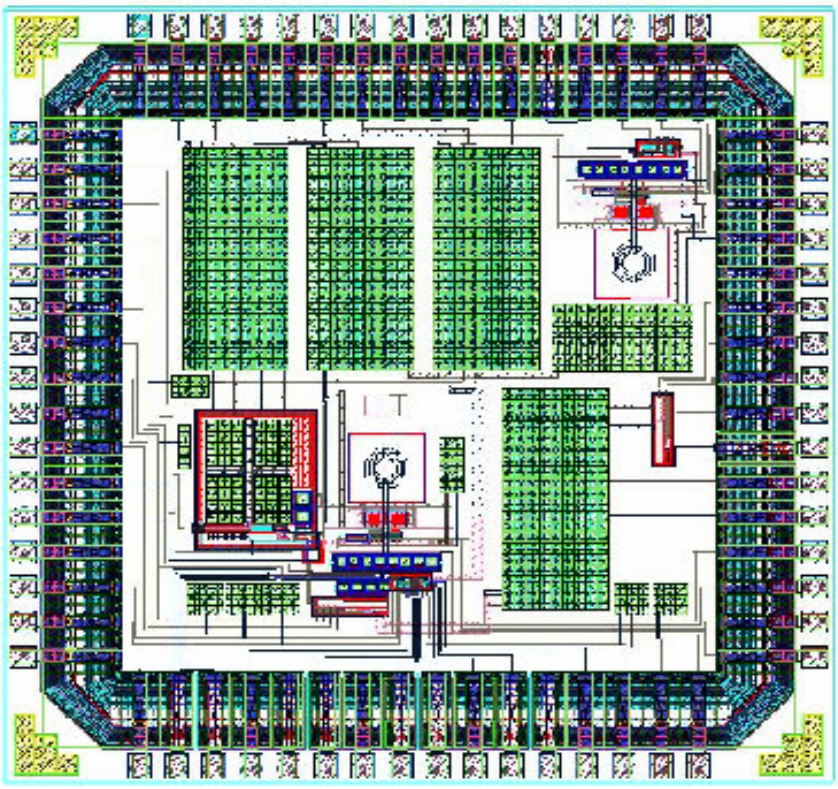


Fig. 3.12 Frequency Synthesizer Layout with the Frame

Floor planning and power supply routing is an important design step for synthesizers. Floor planning becomes crucial during routing of RF signals. The sub-section on RF routing highlights certain relevant issues. For high-performance realizations of synthesizers, reference spur suppression is a critical issue. Efficient and good power supply routing helps in minimizing the ripples in the control line of the VCO. The floor plan for the entire chip is given in Fig. 3.13.

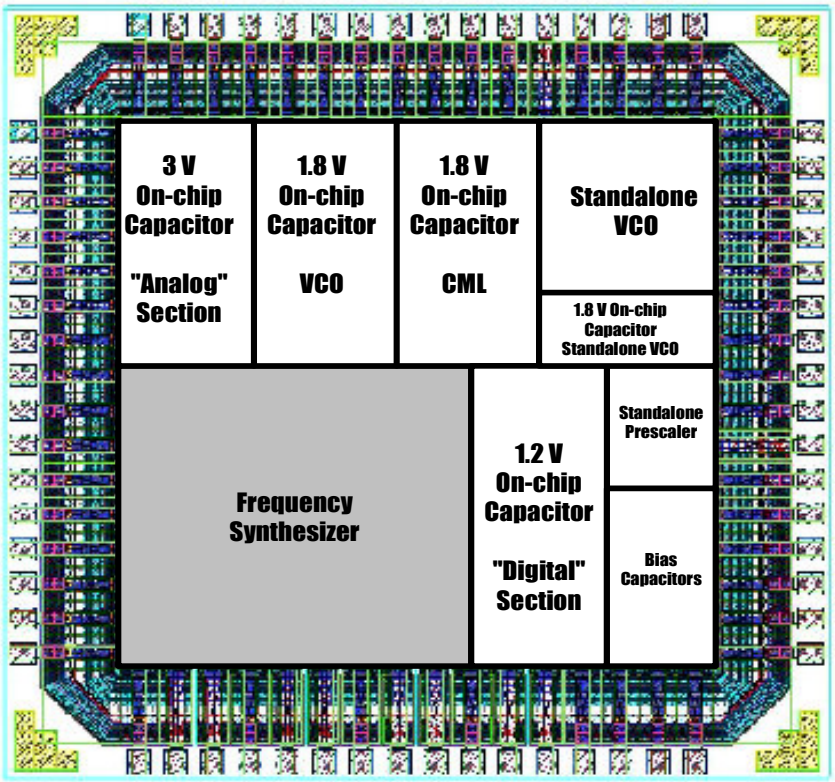


Fig. 3.13 Frequency Synthesizer - Floor Plan

3.8.2 Supply Biasing Capacitors

The bond-wire inductance leads to transient voltage jumps due to *Ldi/dt*. The use of four different power supplies mandates the need of four huge capacitors to minimize the voltage difference between the respective *Vdd's* and *Gnd's*. On-chip capacitors of 200pF are realized for this purpose and MIM realization is used for metal density purposes (Fig. 3.14). The ground bouncing needs to be minimized in all the circuits due to the high sensitive nature of the VCO. The prescaler section has the highest ground bouncing due to its inherent digital and rail-to-rail nature.

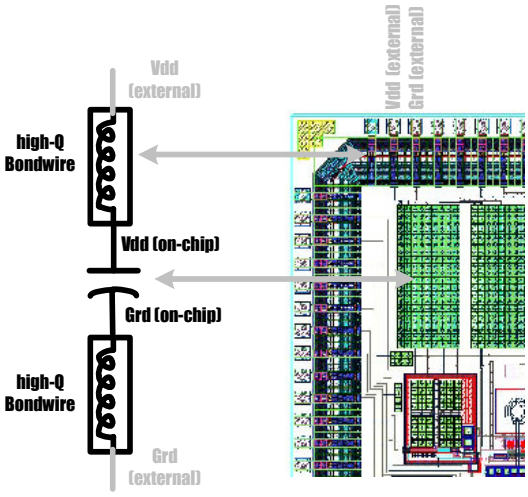


Fig. 3.14 On-chip Capacitor to Minimize Ground Bouncing

3.8.3 Guard Ring for Substrate Isolation

Since there is one underlying uniform substrate, the use of different supplies might not locally help with substrate isolation. This necessitates the use of guard rings to improve noise rejection and substrate isolation. The technology doesn't provide with a deep trench. Hence, the analog section, digital section and the CML divide by 2 sections

have their individual guard rings. As will be explained in Section 4, the VCO section doesn't need a guard ring.

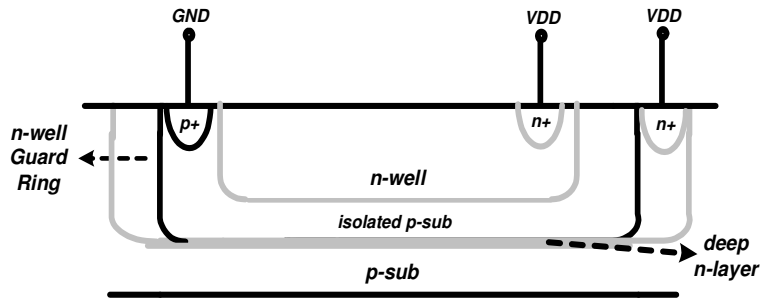


Fig. 3.15 Conceptual Idea of the Guard Ring

The guard ring can be considered as a tub of a different p-substrate (tied to a clean and separate Vdd) surrounded by a thick wall of n-layer (tied to appropriate Gnd) from the sides and a deep n-well layer at the bottom. Thus, the isolation between the p-substrate within the tub and the universal substrate improves. This layout technique greatly improves the performance of RF systems by providing additional isolation of almost 20 dB (Refer Fig. 3.15) [56].

3.8.4 Pin Placements

1. Supply Pins

While dedicating separate power supplies to analog and digital sections reduces the noise on the analog supply, some noise may still couple to sensitive signals through the mutual inductance of bond wires and package traces [57]. Careful pin assignment can minimize these mutual inductances. For two wires

carry equal and opposite currents, the mutual inductance between them is minimized. Thus, the *Vdd* and *Gnd* pins can be placed next to each other. (Refer Fig. 3.16).

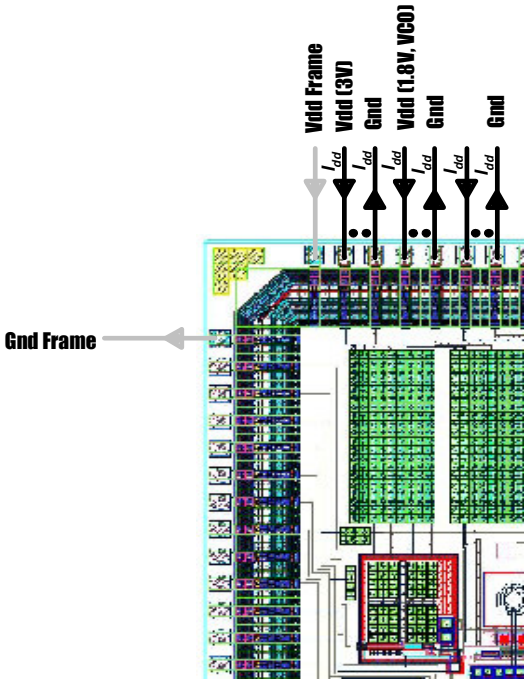


Fig. 3.16 Power Supply Pin Placement

2. RF Pins

Most of the RF inputs or outputs are for testing purposes. Since, we would be interested in the frequency content of the signal, amplitude of the obtained output is not critical. However, we would need to meet the minimum amplitude requirements for the equipments used during testing. It is a good practice to minimize the RF routing as the interconnect capacitances deteriorate the strength of the RF signals. Moreover, the signals were shielded by using *Gnd* routes on either side.

3. *Vc* Pin

The control voltage of the VCO prior to the loop filter buffer is tapped out for measuring the settling time of the synthesizer. The reference for the PFD is a strong signal from the external environment. Due to substrate coupling, the reference affects the control line of the synthesizer. This leads to increased spurs at the output of the VCO. It is a good practice to isolate the two signal paths during layout. More details on substrate coupling and effects on spurs is discussed in the next section on board-level issues.

3.8.5 RF Routing

The VCO and the divider sections need to be placed as close as possible. The high frequency signal loss because of the capacitive nature of the interconnects needs to be taken into account. M6 or M5 are used for high frequency signal routing. They offer the lowest resistivity to high frequency signals. Moreover, their parasitic capacitance to the substrate (fringe capacitance) is minimal. The inductors need to be placed at least a diameter apart to minimize mutual coupling and radiation effects. The stand-alone VCO for test purposes is placed appropriately.

3.9 Printed Circuit Board Design

3.9.1 Chip Fabrication

The chip was fabricated using the TMSC 0.18 μm CMOS process and sponsored by Silicon Laboratories, Austin, TX. Fig. 3.17 shows the die photo of the entire synthesizer. Provisions are made to test the complete synthesizer, the VCO, the CML

divide-by-2, and the prescaler section. The overall power consumption of the synthesizer is 15.5 mW. It merits mention that each section, as discussed in Section A of this section, is operating at different supply voltages. The loop filter is on-chip and a capacitance of 346 pF is implemented using the capacitance multiplier technique.

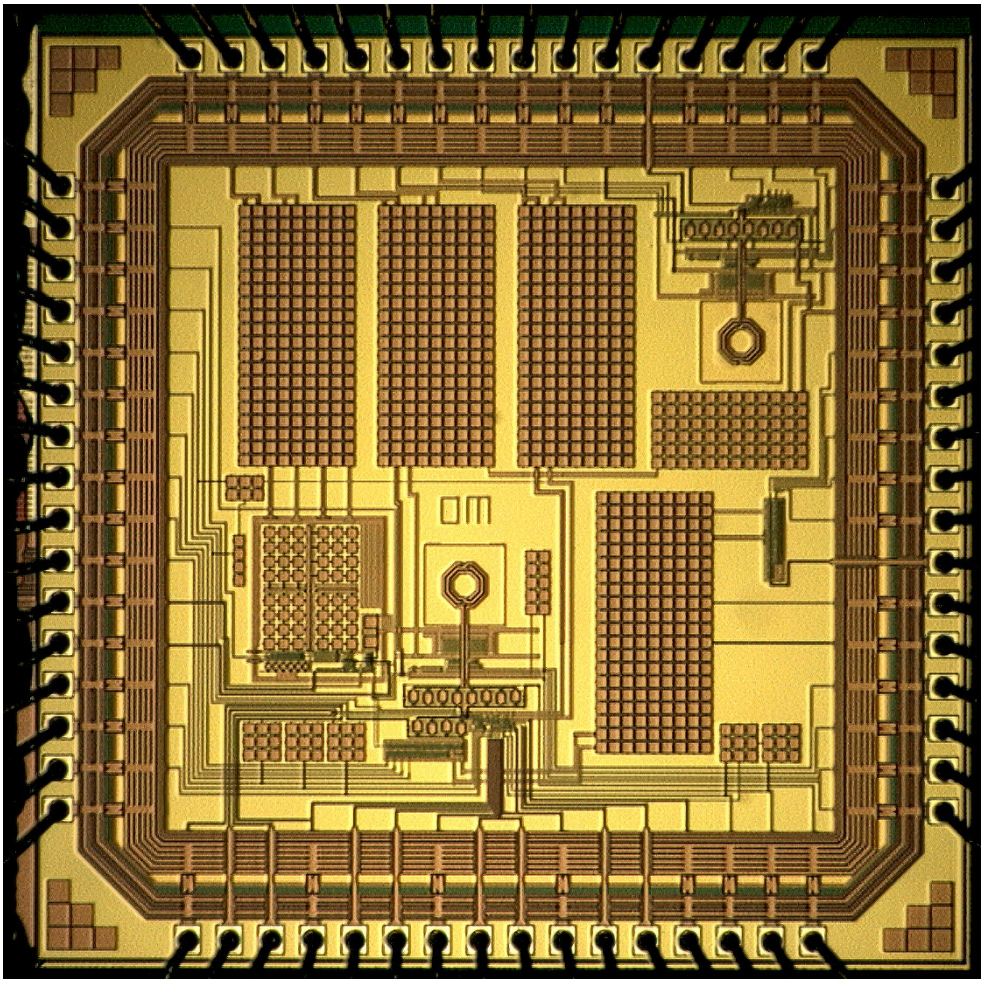


Fig. 3.17 Die Photo of the Frequency Synthesizer

The frequency synthesizer needs to be functionally verified for the synthesis of channel select frequencies. Initially, the VCO and the dividers are characterized separately on two different PCBs for their functionality. The VCO results are given in Section 4. Finally, the synthesizer needs to be characterized for phase noise, spurs, and settling time.

3.9.2 Board Level Issues

Protel software is used to design the PCB and the in-house PCB manufacturing equipment is used to manufacture the PCB on a copper plated FR-4 substrate. During the chip testing and characterization phase, five PCB's were manufactured. Table XI provides a summary of the characteristics of the PCB's. PCB's #1, #2, and #3 were for the purpose of test for functionality of the high frequency blocks – VCO and dividers; and the complete synthesizer.

PCB #4 included provisions for the complete characterization of the synthesizer. PCB #5 is a refinement of PCB #4 design and was manufactured using PCB Express. PCB #4 and #5 are used as design prototypes to highlight the various board level issues in the design. Testing results are provided in the next sub-section for these two PCB's. The fabricated PCB #4 used for measurements is given in Fig. 3.18 along with the PCB floor plan layout in Fig. 3.19.

TABLE XI
CHARACTERISTICS OF THE PCB'S USED FOR TESTING

PCB #	*Purpose*
1	Test for functionality of the VCO
2	Test for functionality of the dividers
3	Test for functionality of the synthesizer
4	Characterization of the synthesizer
5	Characterization of the synthesizer

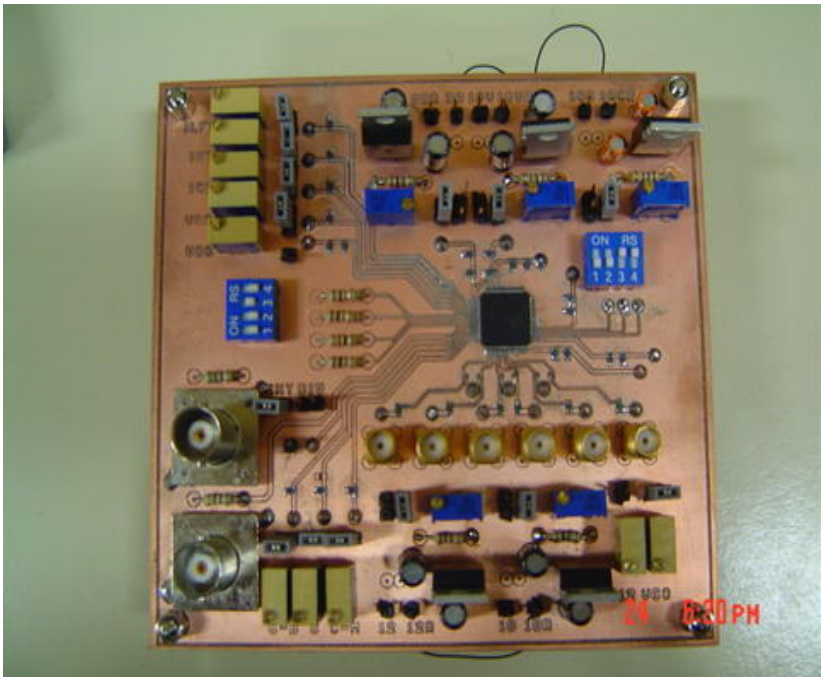


Fig. 3.18 PCB #4 for Testing the Synthesizer

1. Settling Time

For the purposes of settling time measurements, provision is made to clock the channel selection switches from an external reference. A BNC connector is used to provide the low frequency clock (500 kHz to 2 MHz). The reference is matched to $50\,\Omega$.

2. Grounding Scheme

It is extremely important to have a proper grounding scheme in the PCB. With the judicious selection of clearance width constraint and proper placement of the external PCB components, the stray floating islands can be reduced. Importantly, the use of a ground plane helps in minimizing the parasitic impedances in the RF signal paths.

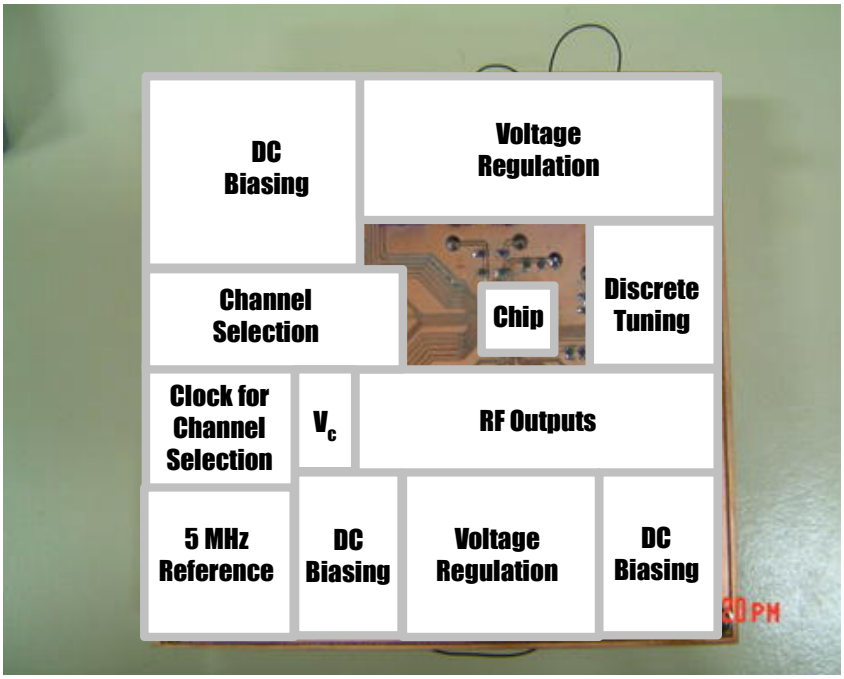


Fig. 3.19 Floor Plan Layout of PCB for Testing the Synthesizer (Fig. 3.18)

3. Power Supply Routing

Power Supply routing is important in RF boards. The system performance of the synthesizer is affected by corruption in the power lines. The control voltage of the VCO is extremely sensitive to power supply variations. The VCO lacks good supply rejection. Regulation of supply voltages helps in improving the performance of the overall synthesizer by minimizing the effect of noise injection in the analog and VCO sections.

Moreover, current flows in a loop, both inside and outside the chip. Such current flowing loops are inductive in nature. It is best to minimize the parasitic inductances from such loops. These parasitic inductors could couple with the inductance of the VCO, leading to deteriorated performance.

The supply power lines are susceptible to the high-frequency noise from the environment. Before entering the chip, the noise is filtered using a parallel bank of surface mount capacitors with high self-resonant frequencies. It must be remembered that the PCB trace and vias have resistive and inductive elements.

4. Reference

The reference clock of 5 MHz is obtained from a signal generator, instead of a dedicated crystal. It must be remembered that the accuracy of the clock determines the overall accuracy of the synthesized frequency. The PLL loop is low-pass in nature for jitter at the input of the PLL. Most of the low jitter is transmitted to the output without any attenuation. Hence, it is important to have a dedicated crystal with high accuracy for practical solutions. However, for the purpose of testing, the reference from a signal generator would suffice. The reference is matched to $50\,\Omega$.

5. Channel Selection and Discrete Tuning

Two DIP switches are used to accommodate discrete tuning and channel selection in the synthesizer. While one terminal of the switch is connected to the corresponding power supply, the other terminal is connected to the ground through a resistance of $1\mathrm{K}\,\Omega$. The current drawn by these resistors needs to be taken into account while calculating the actual power consumption of the synthesizer.

6. RF Buffers

The SMA connectors are used to tap RF outputs at 4.8 GHz and 2.4 GHz. The buffer is an open-drain configuration. The RF output from the die is in the form a current. The off-chip inductive load provides certain impedance to the current at that frequency, which is in parallel to the port impedance of $50\,\Omega$. As can be seen in Fig. 3.20, the small signal current high frequency current is collected through the capacitor and converted to a voltage at the port. The attenuation of the buffer is not an important consideration as long as it is above the minimum power levels of the spectrum analyzer. This is so because; we are interested in the frequency content of the RF output.

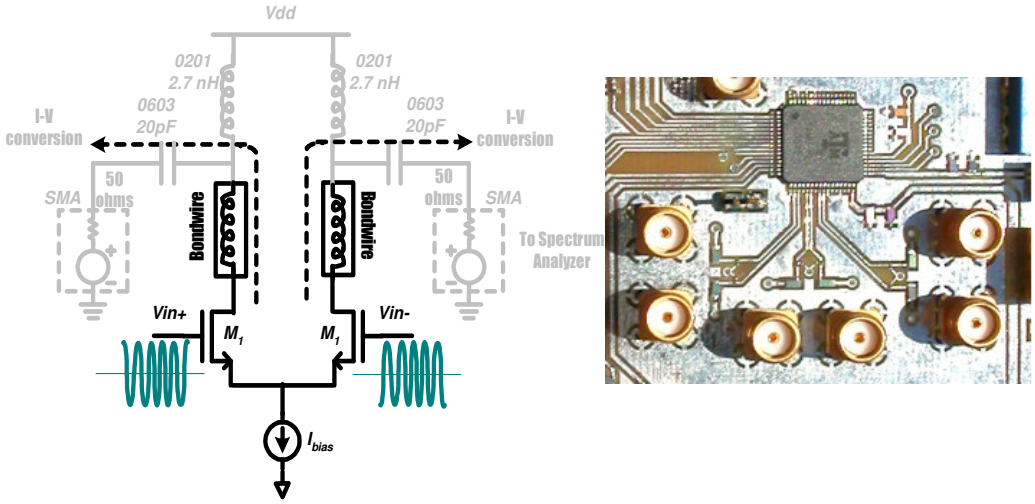


Fig. 3.20 Tapping Buffered RF Output Using Off-chip Components in the PCB

The selection of the L and C off-chip components in the PCB is important. The inductor used had a footprint of 0201 and a self-resonant frequency of 10 GHz. At RF frequencies, an inductor need not always behave as an inductor. It

tends to be capacitive in nature for frequencies well beyond the self-resonant frequency of the inductor. The capacitors used had a footprint of 0603. The RF outputs are tapped as close as possible to the chip. Long RF traces will result in significant signal loss, for they act as transmission lines at such frequencies. A wide-band passive balun can be used to obtain differential-single ended conversion of the RF outputs.

7. Biasing

The power supplies are regulated using the LM317 and its associated circuitry. They are used in the adjustable mode so as to obtain supplies of 3V, 1.8V, 1.8V and 1.5V respectively for the analog section, VCO section, CML section and prescaler section respectively from a single 6V supply. The DC current biasing for the various building blocks is implemented using 25-trim potentiometers.

Jumpers are provided in the path for purposes of current measurement. The DC voltage biasing is provided using 25-trim potentiometers for purposes of flexibility in testing. Shunt capacitors are provided for important signal/ bias traces so as to minimize bouncing at the corresponding input pin of the die. As an example, it is extremely important to ensure a clean VCO bias.

8. PCB coupling to control line

The reference is usually a strong signal with amplitude from 0 to 3V. The digital nature of the PFD allows for using a lower amplitude swing depending on the trip voltage of the gates. PCB #4 suffers from high PCB coupling to the

control line. From Fig. 3.21(a) it can be seen that the control voltage trace and the reference trace travel for a couple of inches in the PCB. This increases the level of coupling between the two traces. With this strong coupling, the spurs obtained at the output of the VCO are extremely poor. Thus, even a good potential high-performance design can have poor spur suppression due to the dominating nature of the external coupling.

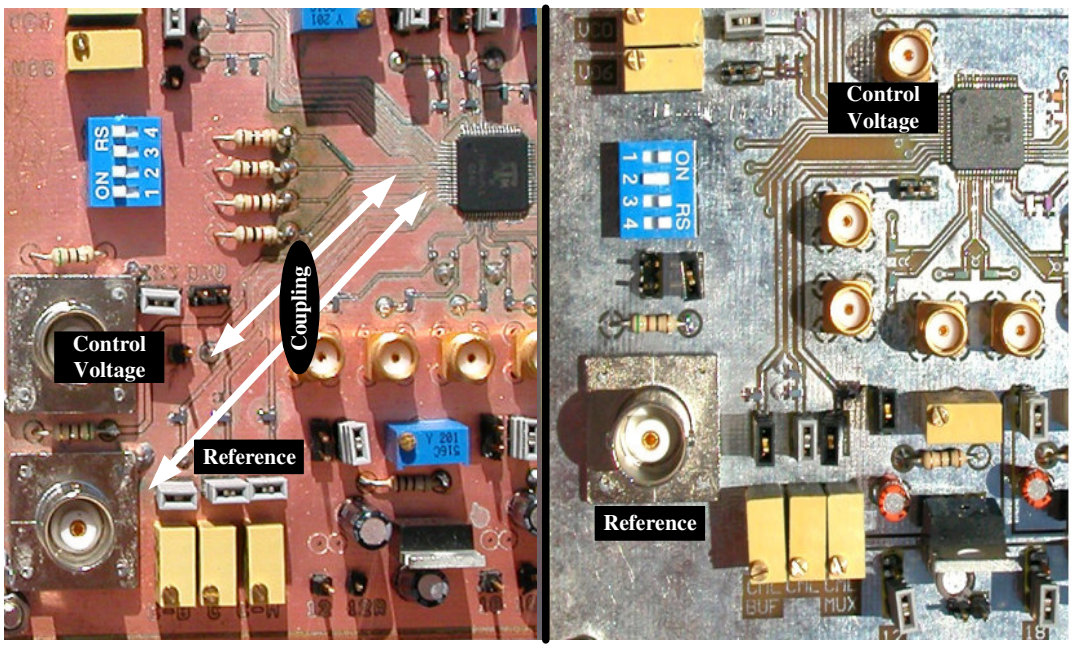


Fig. 3.21 (a) Coupling in the PCB to the Control Voltage of the VCO (b) Refinement in PCB #5

PCB #5, a refinement of PCB #4, takes this factor into account and is given in Fig. 3.21(b). The control voltage pin is tapped as closely as possible to the chip. The floor plan of the new PCB #5 is similar to the one shown in Fig. 3.19 and PCB #5 is given in Fig. 3.22.

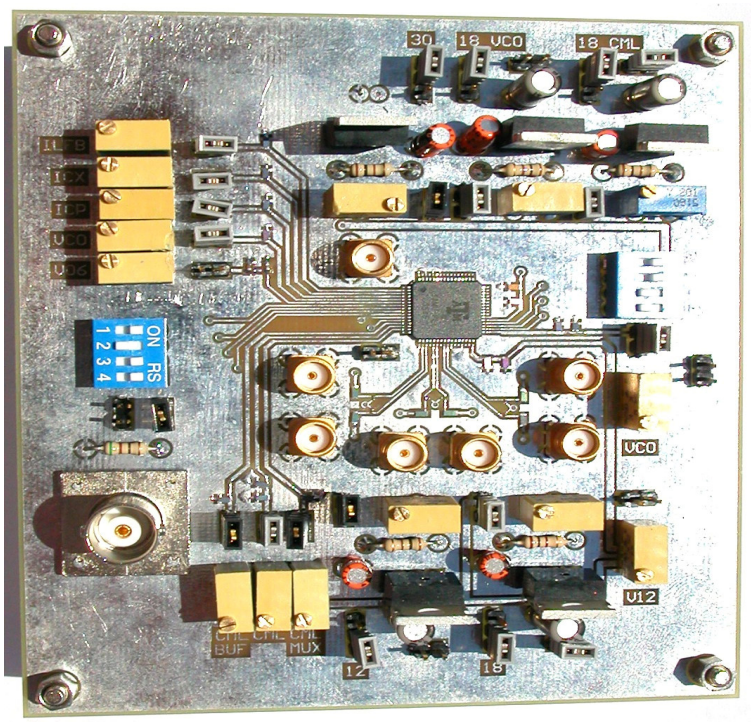


Fig. 3.22 PCB #5 for Testing the Synthesizer

3.10 Testing and Measurement

3.10.1 Testing Setup

The equipments used for testing the synthesizer are given in Table XII. It merits mention that the synthesizer was tested at three different labs – AMSC Testing Lab, TI and Wiquest; at different points of time using different equipments.

TABLE XII
EQUIPMENT USED FOR TESTING

Equipment Used	*Purpose*
Agilent 33250A Function Generator	5 MHz Reference
HP 33120A Function Generator	1.5 KHz channel switching clock for settling time measurements
3Hz – 13.2 GHz Agilent E445A PSA Series Spectrum Analyzer	Output Spectrum for VCO and CML outputs
Agilent Infiniium Oscilloscope	Settling time measurement
Agilent E3631A Power Supply	6 V supply to the input of the four regulators to provide regulated supply to four sections of the chip

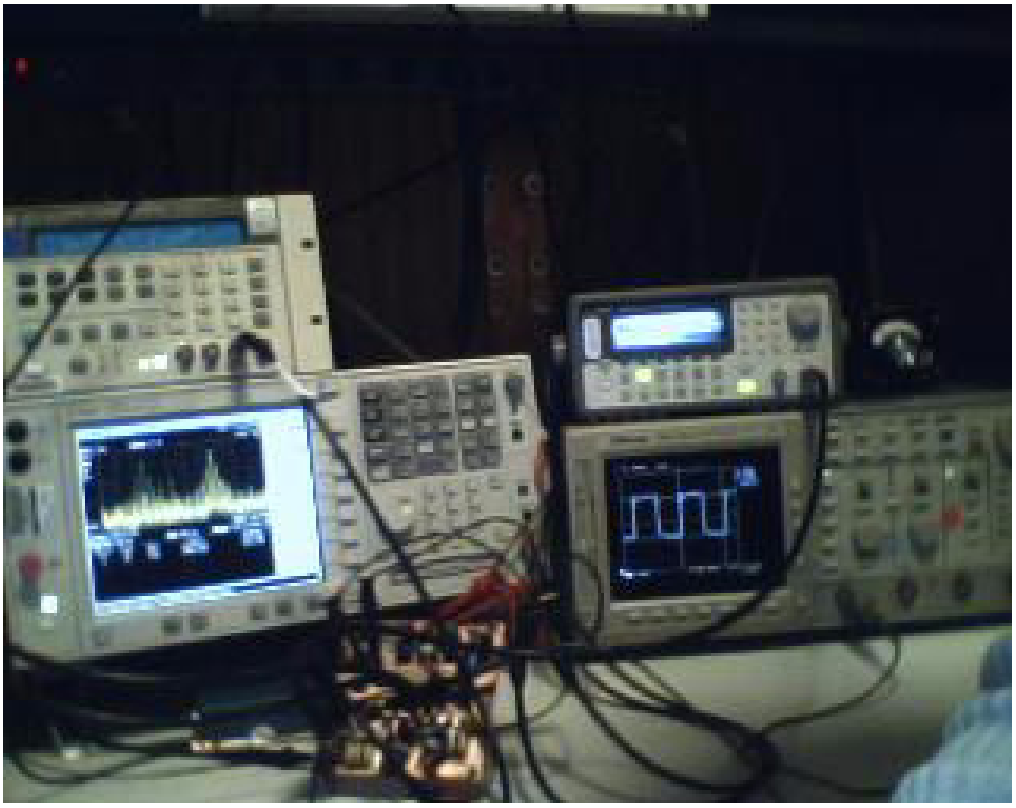


Fig. 3.23 Testing Bench Setup

Fig. 3.23 gives the testing bench setup. It shows the case of extreme switching from 2.405 to 2.48 GHz and vice versa. The key equipments used are the 3Hz – 13.2 GHz Agilent E445A PSA Series Spectrum Analyzer and the Tektronix TDS740 500 MHz oscilloscope apart from the two random signal generators and power supplies. The settling behavior of the synthesizer is evident in the oscilloscope.

For phase noise measurement, FSE-K4 software is used in the AMSC testing facility. The output of the Rohde & Schwarz Spectrum Analyzer is connected to a PC through a GPIB cable. The 3Hz – 13.2 GHz Agilent E445A PSA Series Spectrum Analyzer has in-built phase noise measuring capabilities. The I-Q mismatch could not be measured due to the lack of availability of high sampling oscilloscopes.

3.10.2 Measurement Results

1. Frequency Synthesis

The synthesizer is first tested for its basic functionality – generation of the 16 channel select frequencies. The presence of reference spurs in the output power spectrum of the VCO output and the CML divide-by-2 output proves that the synthesizer is in locked state of operation. The low sensitivity of the VCO helps in reducing the "jumpiness" of the output tone, thereby making it stable.

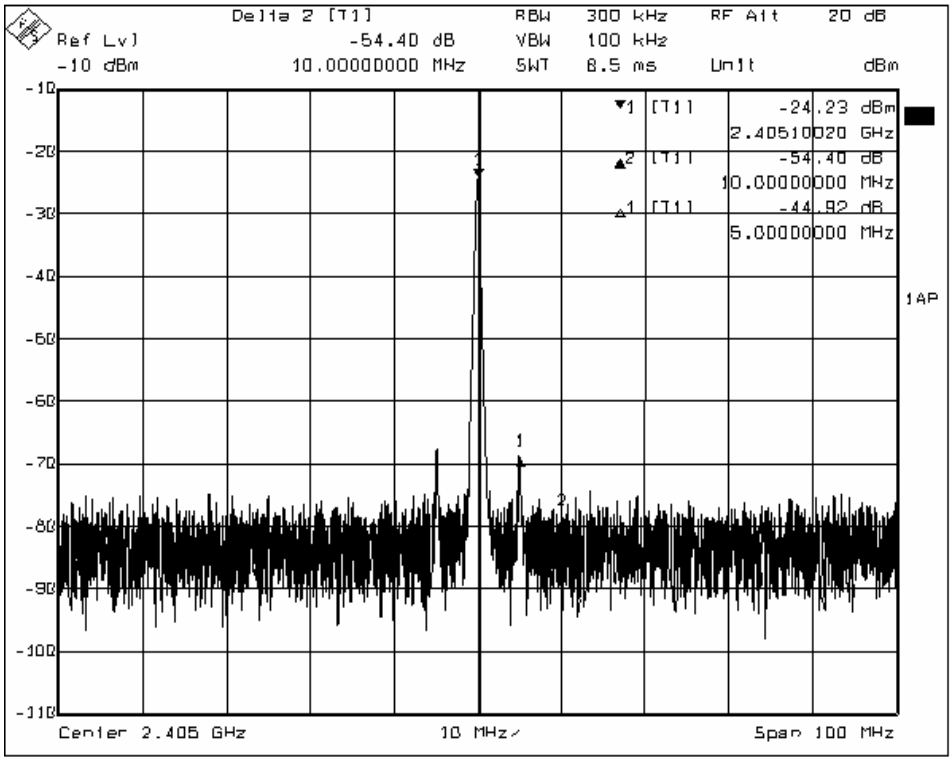


Fig. 3.24 Frequency Synthesis of Channel 1 for Zigbee Applications

Fig. 3.24 gives the output spectra of the synthesizer for channels 1. The divide-by-2 output spectrum has a 6-dB improvement in spurs due to the divide

operation [25]. The VCO has a tuning range from 4580-5275 MHz, with an average sensitivity of 135 MHz/V for a tuning control voltage range from 1-2.5V. Thus, we can see that the entire 2.4 GHz Zigbee band can be covered and all channel select frequencies synthesized. Fig 3.25 gives the output spectrum for the 16th channel for Zigbee applications.

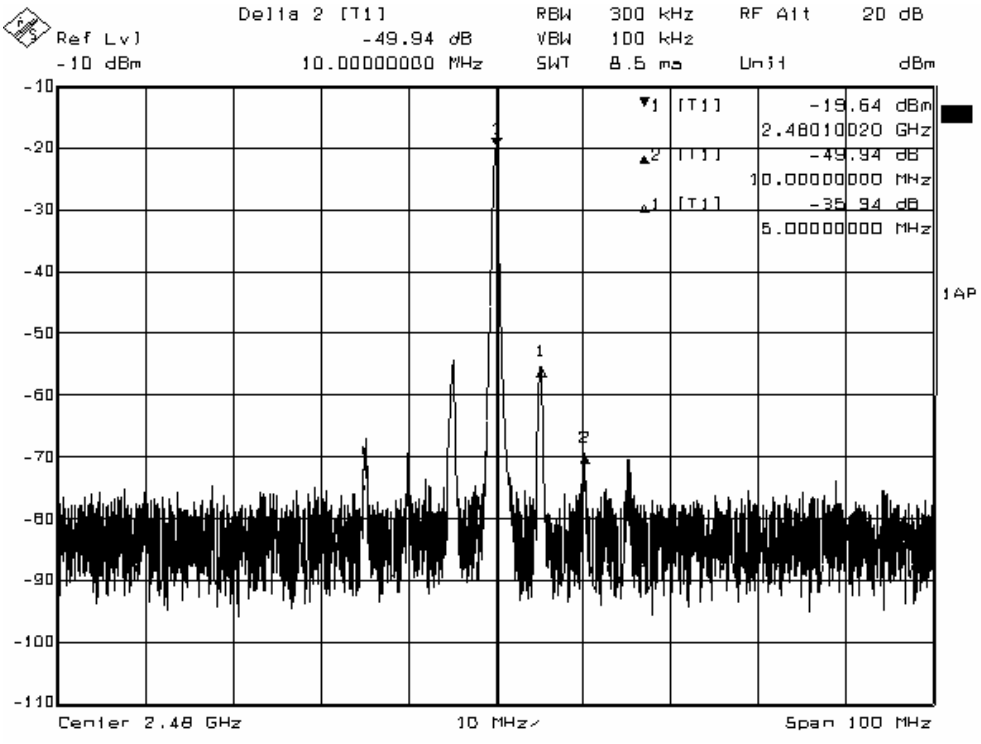


Fig. 3.25 Frequency Synthesis of Channel 16 for Zigbee Applications

2. Settling time

For settling time measurements, the channel selection switches are clocked with a 0.5 KHz frequency. The DIP switches are in ON state. Thus, the settling time is measured for the extreme switching case, from 2.405 GHz to 2.480 GHz.

Fig. 3.26 gives the oscilloscope plot for the settling time measurement for the synthesizer. The settling time is found to be 55 µs.

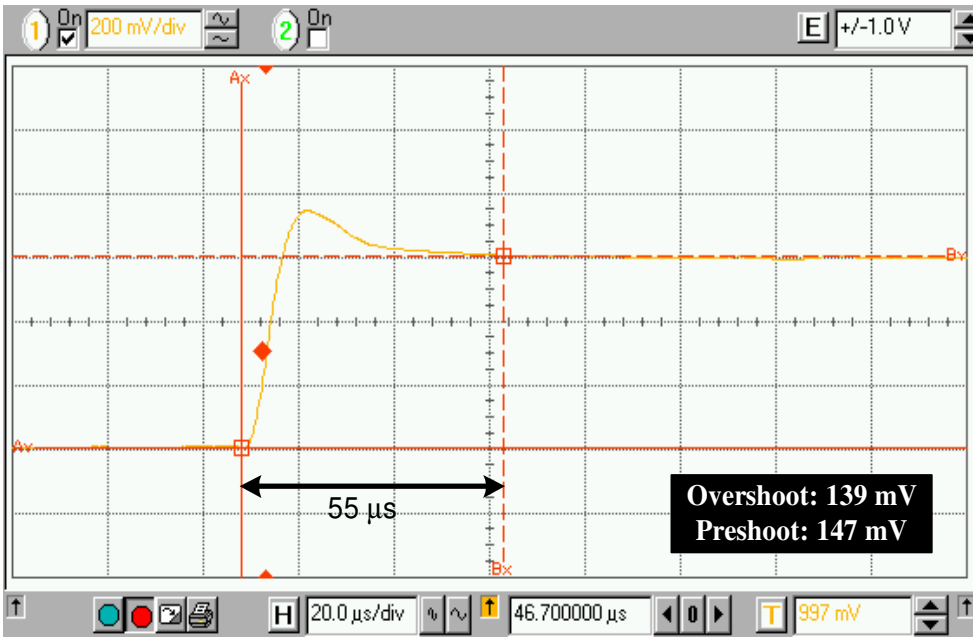


Fig. 3.26 Settling Time Measurement for the Extreme Switching of the Synthesizer

Fig. 3.27 gives the settling time measurement for the synthesizer when a 100pF 0603 load capacitor is placed on purpose at the control voltage node externally in the PCB. By adding a 100pF capacitor on purpose, the loop dynamics would change. It will be compromise between spur suppression and the settling time for the synthesizer. Moreover, the damping factor for the system changes. In this case, it happens to be stable too.

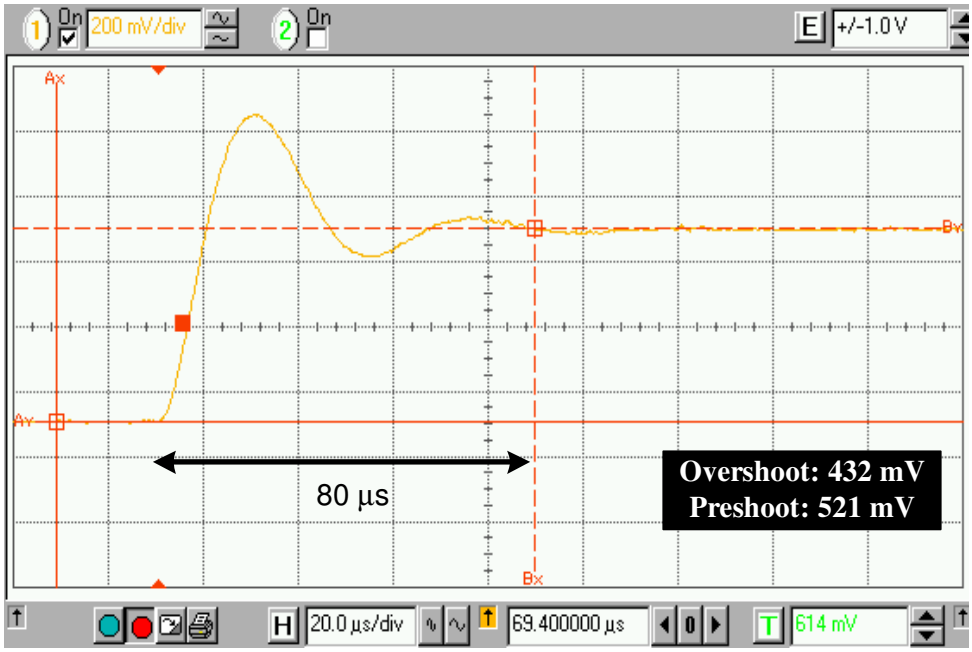


Fig. 3.27 Settling Time Measurement for the Extreme Switching of the Synthesizer with a 100pF Capacitor at the Control Voltage Node (Placed Externally)

3. Spur Suppression

Reference spur is a phenomenon that is characteristic of integer-N charge pump PLL based systems. The various sources of reference spurs are given in Table XIII along with the methods to minimize them. It can be seen that the board-level and the layout issues are as important as the design itself. The frequency synthesizer testing in a real environment opens up a plethora of feasibilities in improving the spurs.

Apart from the methods listed in Table XIII, the VCO sensitivity plays an important role. The methods listed affect the critical control line of the VCO. The sensitivity of the VCO is discussed in detail in the next section. For a 150 MHz/V gain, a 1 mV ripple leads to a variation of 150 KHz. Thus, the design of

a low sensitivity VCO with a high tuning range becomes extremely important for the realization of high-performance synthesizers.

TABLE XIII
SOURCES OF REFERENCE SPURS AND THEIR ALLEVIATION METHODS

Sources of Reference Spur	*Alleviation Methods*
PCB Coupling	Minimize the trace length of control voltage; Minimize the "interaction" between the reference and the control line
Reference	Use lower amplitude signal (the PFD responds to the edge transitions); Use of sinusoidal reference source helps in improving the 10 MHz (second harmonic) spurs.
Substrate Coupling	Minimize the "interaction" between the reference and the control line by appropriate pin placement.
Power Supply Variations	Use regulated supplies in the PCB; place off-chip 0603 capacitors to filter the high-frequency noise
Charge Pump Mismatch	Use of 3V low-voltage cascode charge pump; improving the current mismatch; sizing the dead zone removal pulse appropriately

TABLE XIV
SPUR SUPPRESSION FOR VARIOUS TEST SCENARIOS AT 2.48 GHZ (REFERENCE AMP., BIAS, WAVE TYPE)

Scenario				*PCB*	*Spur at 5 MHz offset*	*Spur at 10 MHz offset*
Amp.	*Bias*	*Wave*	*V_c cap*			
3 V_{p-p}	1.5 V	square	-	#4	-3.2 dBc	-11.2 dBc
3 V_{p-p}	1.5 V	sine	-	#4	- 6 dBc	-19 dBc
1.6 V_{p-p}	**1.5 V**	**square**	**-**	**#4**	**-10 dBc**	**-24.5 dBc**
1.6 V_{p-p}	1.5 V	sine	-	#4	- 12 dBc	-30.5 dBc
3 V_{p-p}	1.5 V	square	-	#5	-15.5 dBc	-30.6 dBc
3 V_{p-p}	1.5 V	sine	-	#5	-18.5 dBc	- 36.5 dBc
1.7 V_{p-p}	1.5 V	square	-	#5	- 22 dBc	-36 dBc
1.7 V_{p-p}	1.5 V	sine	-	#5	-26 dBc	-38 dBc
3 V_{p-p}	1.5 V	square	100 pF	#5	- 32 dBc	-50 dBc
3 V_{p-p}	1.5 V	square	100 pF	#5	- 36 dBc	-52 dBc
1.7 V_{p-p}	1.5 V	sine	100 pF	#5	-38 dBc	-51 dBc
1.7 V_{p-p}	**1.5 V**	**square**	**100 pF**	**#5**	**- 39 dBc**	**-49 dBc**
1.0 V_{p-p}	1.3 V	sine	100 pF	#5	-52 dBc	-52 dBc
1.0 V_{p-p}	1.3 V	sine	-	#5	-40 dBc	-48 dBc

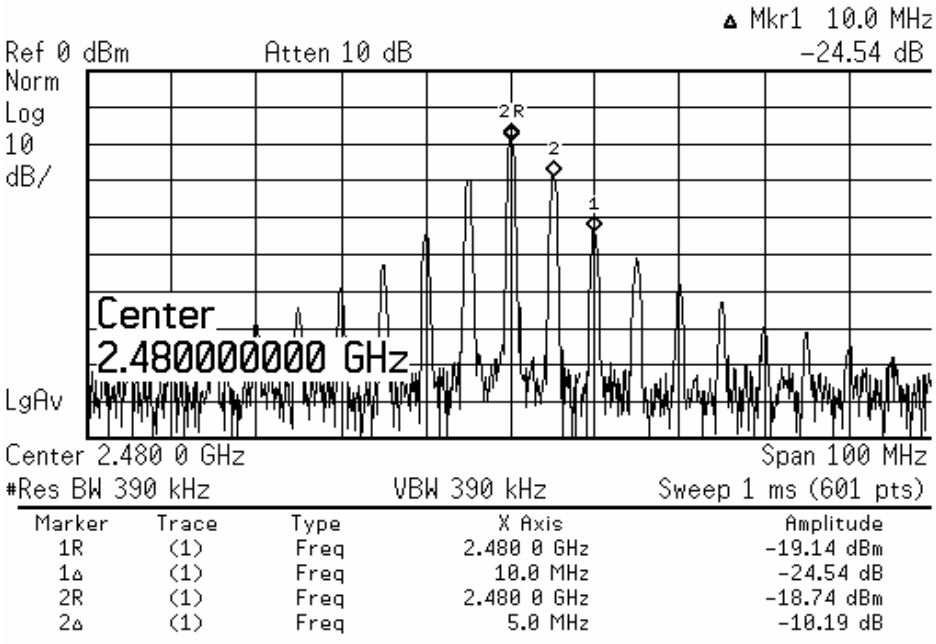


Fig. 3.28 Spur Suppression for 1.6Vpp, 1.5V, Square, PCB#4 Case

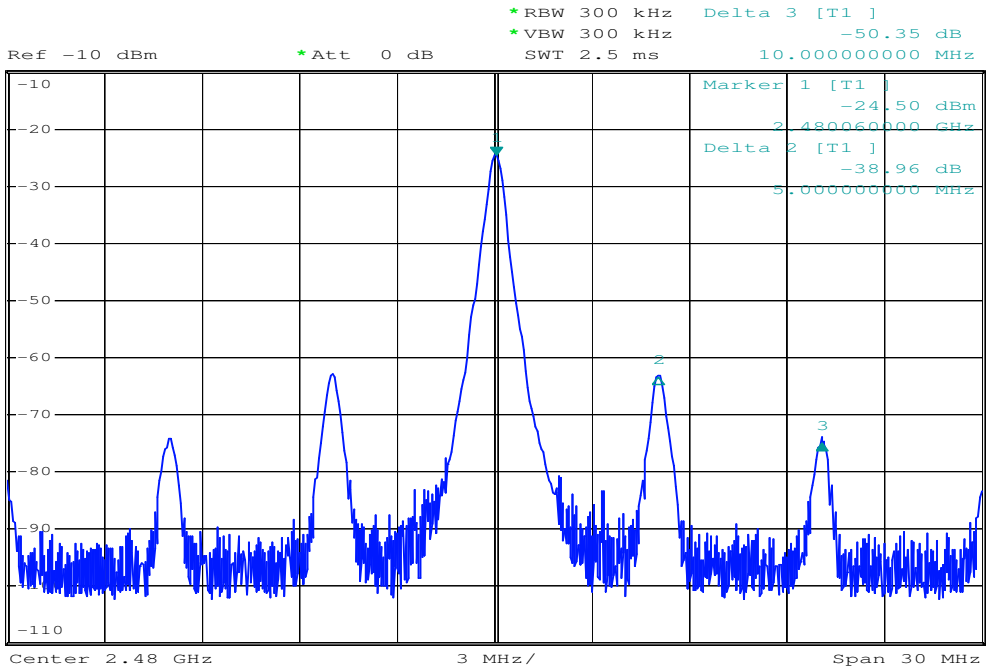


Fig. 3.29 Spur Suppression for 1.7Vpp, 1.5V, Square, 100pF, PCB#5 Case

From Table XIV, it can be inferred that the spur performance improves with PCB #5. Further, a lower amplitude reference and sinusoidal reference helps in achieving higher spur suppression. Placing an external capacitor of 100 pF alters the loop dynamics and thereby the settling time. Figs. 3.28 and 3.29 give the synthesizer spectrum for the highlighted scenarios in Table XIV.

4. Phase Noise

The measured phase noise spectrum is given in Fig. 3.30. It can be seen that the phase noise at an offset of 10 MHz from the center frequency is –130 dBc/Hz. This corroborates with the open loop synthesizer phase noise obtained mostly from the VCO. The phase noise spectrum for the synthesizer in the locked state gives an idea of the reference spurs too. The presence of the spurs in the phase noise spectrum is a true test for locking of the synthesizer.

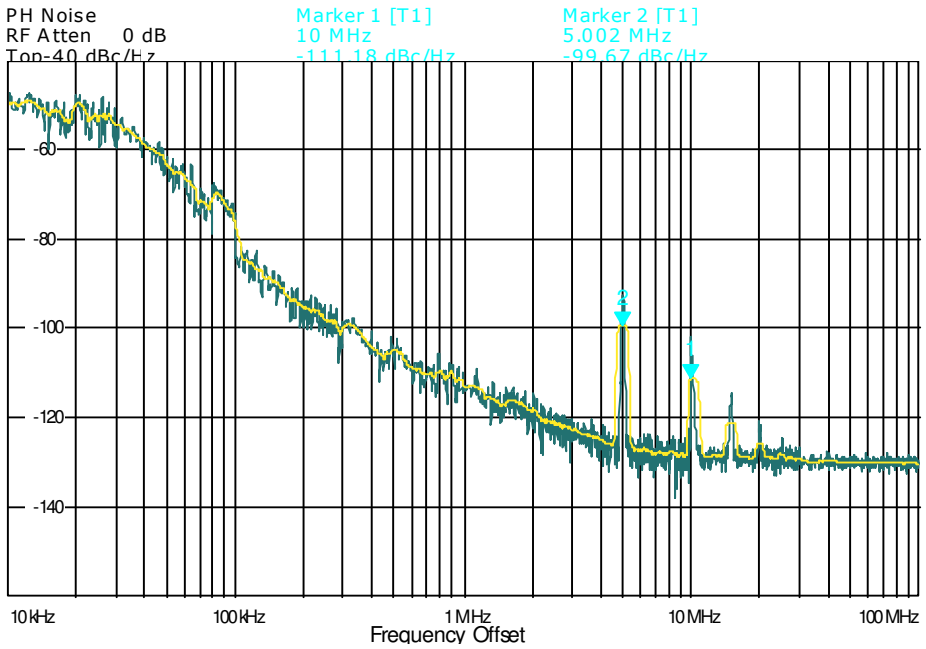


Fig. 3.30 Phase Noise for Synthesizer Spectrum with Reference Spurs

The phase noise spectrum also includes the deterministic spurs, although normalized by the resolution bandwidth. Fig. 3.31 gives the open loop phase noise response for the synthesizer. It merits mention that the dividers were fully functional. The spur from the dividers can be seen. The reference signal is absent. Hence, the synthesizer is in open loop.

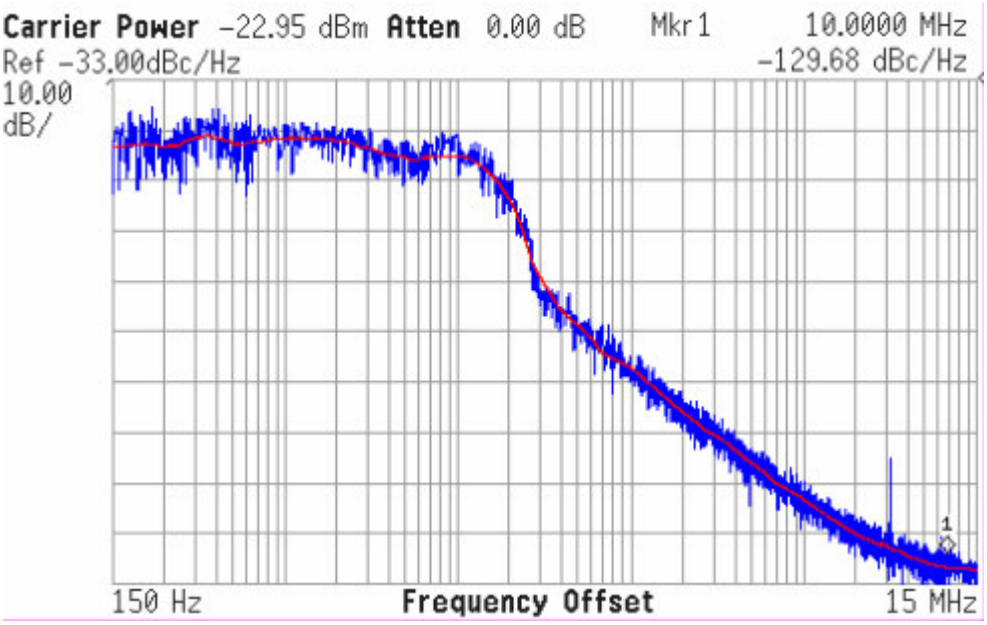


Fig. 3.31 Phase Noise Spectrum of the Synthesizer in Open Loop

3.10.3 Performance Summary

The measurement results are summarized in Table XV along with the original specifications derived in Section 2. It can be seen that all the specifications for the 2.4 GHz standard are met.

TABLE XV
PERFORMANCE SUMMARY OF THE FREQUENCY SYNTHESIZER

Metric	*Specification*	*Implementation*
Frequency synthesis	2405-2480 MHz	2405-2480 MHz
Spurs	- 13 dBc at 5 MHz	- 40 dBc at 5 MHz
	- 43 dBc at 10 MHz	- 48 dBc at 10 MHz
Settling Time	192 µs	55 µs
Phase Noise	-110 dBc/Hz at 10 MHz	- 130 dBc/Hz at 10 MHz
Power Consumption	Minimum	15.5 mW

The overall power consumption is found to be 15.5 mW. Fig. 3.32 gives the pie-diagram for the total power consumption of the synthesizer.

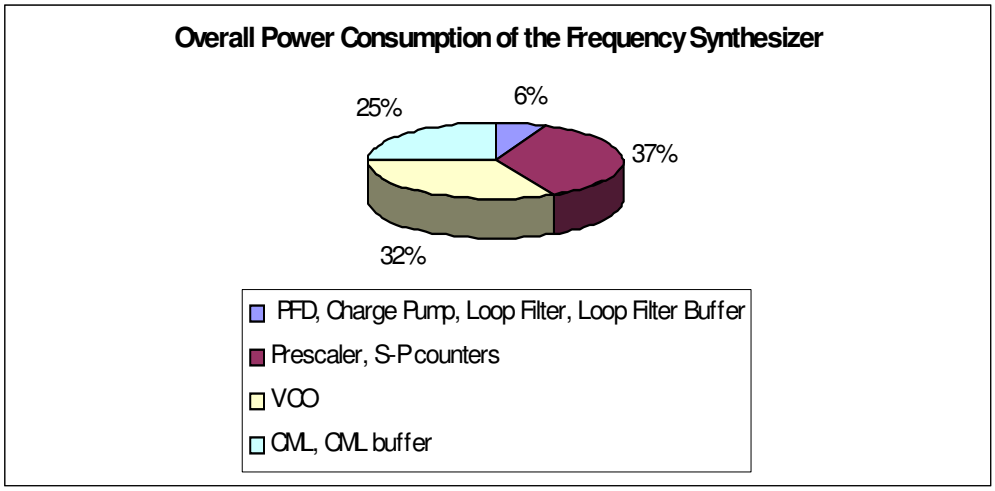


Fig. 3.32 Power Consumption of the Frequency Synthesizer – Pie Diagram

3.10.4 Comparison with Other Zigbee Synthesizers

Table XVI gives a comparison with the other frequency synthesizers that have been reported so far in the literature.

TABLE XVI
COMPARISON WITH OTHER SYNTHESIZERS FOR ZIGBEE APPLICATIONS

Performance Metric	*[2] (Silicon)*	*[3] (Silicon)*	*[5] (Simulation)*	*[6] (Silicon)*	*This work (Silicon)*
Frequency Synthesis	2.4 GHz, 8 channels with 3 MHz spacing	2.4 GHz, 16 channels with 5 MHz spacing	2.4 GHz, 16 channels with 5 MHz spacing	2.4 GHz, 160 channels with 1 MHz spacing	2.4 GHz, 16 channels with 5 MHz spacing
Phase Noise	-	-	-	-110 dBc at 1 MHz offset	-130 dBc at 10 MHz offset
Settling Time	< 150 µs	-	300 µs	-	55 µs
Spur Suppression	-	-	-	-55 dBc at 1 MHz offset	-40 dBc at 5 MHz offset; -48 dBc at 10 MHz offset
Power Consumption	12 mW	-	22 mW	18 mW	15.5 mW
Technology	TSMC 0.18 µm CMOS	-	TSMC 0.18 µm CMOS	TSMC 0.18 µm CMOS	TSMC 0.18 µm CMOS

4. VOLTAGE CONTROLLED OSCILLATOR DESIGN

The Voltage Controlled Oscillator (VCO) is one of the crucial blocks of the frequency synthesizer. It is responsible for the one-to-one correspondence of the control voltage (containing useful feedback information) to the output frequency. The performance metrics of the VCO plays a crucial role in the overall Phase-Locked Loop (PLL) based synthesizer design. Further, the transceiver environment imposes additional constraints on the VCO.

The architecture for the VCO is developed in the next section. Following this, the important specifications of the VCO are given. These two sections help us develop our understanding of the VCO and lead us to the actual implementation of the selected scheme. However, it merits mention that the concepts of injection pulling [58-59, 42] phase noise [19-21, 60], etc. are beyond the scope of the thesis work.

4.1 Architecture

4.1.1 VCO in a Transceiver Environment

The 2.4 GHz Zigbee transceiver needs 16 frequencies from 2405-2480 MHz so as to perform up-conversion or down-conversion of the appropriate channel of the spectrum. However, the transceiver environment imposes additional constraints. Consider this hypothetical situation where the VCO is running at ω_0 (2440 MHz) and the RF signal is modulated at ω_n (2480 MHz) in the receive mode. Here, for the VCO, the RF signal is equivalent to “noise” and with increasing signal strength; the VCO might lock to 2480 MHz (Fig. 4.1). There always exists feedback due to the presence of parasitics and a strict unilateral mode of operation, though desirable, is not pragmatic [12-13].

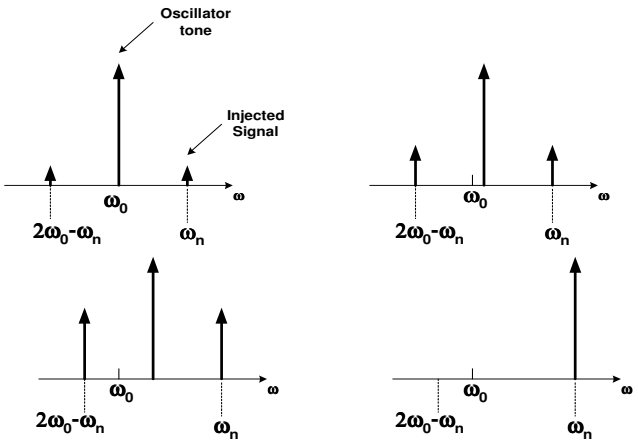


Fig. 4.1 Injection Pulling of an Oscillator as the Noise Amplitude Increases [13]

Moreover, the Zigbee transceiver needs to consume low power. It is therefore desirable to turn-off the PA when in receive (Rx) mode. This additional switching of the PA might interfere with the VCO performance (Fig. 4.2). Thus, the issues of PA load pushing and injection pulling force us to seek an alternative solution for the VCO. It merits mention that these issues are more crucial in a transceiver environment than a receiver environment, as the synthesizer provides the local oscillator (LO) signal to both up-conversion and down-conversion mixers in the receive (Rx) and transmit (Tx) path.

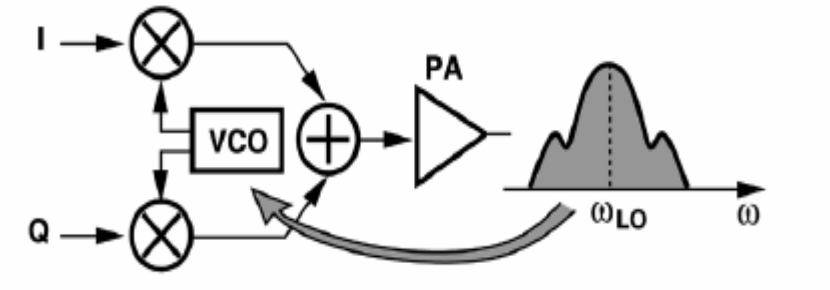


Fig. 4.2 PA Load Pulling in a Transceiver [42]

4.1.2 I- Q Generation

The overall architecture of the transceiver for a direct-conversion or low-IF scheme is given in Section 2. It can be seen that the architecture demands the presence of in-phase and quadrature components for the LO. These two components need to be out of phase strictly by 90 degrees and need to have the same amplitude level. However, real-world solutions have certain amplitude and phase mismatch factor. It is a good practice to consider these mismatches into account while performing the system level simulations for the entire transceiver. To support the given BER, the SNR requirement at the demodulator end of the receiver is higher due to the non-idealities in the I and Q components.

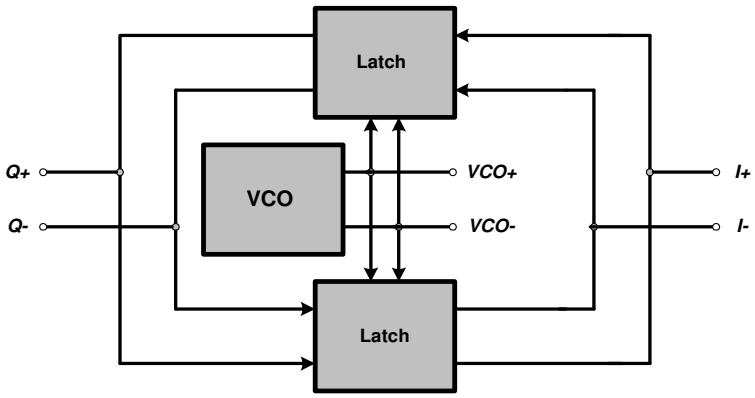


Fig. 4.3 VCO-Divide by 2 Network for I-Q Generation

The most accurate method for I-Q generation is by doubling the frequency and then using a divide-by-2, which can give the two components with minimal amplitude and phase mismatch (given in Fig. 4.3)[13]. As has been mentioned in the previous sub-section, the VCO needs to be at a different frequency when compared to the RF signal

frequencies. It is therefore justified to have the VCO running from 4800-4960 MHz, and then dividing by 2 to obtain the LO. However, we still need to ensure that this is not an expensive solution in terms of power consumption of the circuit. For this approach, the L-C based VCO at 5 GHz with subsequent division by 2 using current mode logic is the best solution.

A quadrature VCO can also be used for I-Q generation [61, 11]. However, the topology in Fig. 4.4 makes use of two L-C tanks, thereby doubling the power consumption and area occupied by the inductors. The R-C, C-R based approach for I-Q generation is conceptually the simplest. However, this scheme suffers from high amplitude mismatch and has a strong dependence on passives, which are known to have high susceptibility to process variations [12-13]. The main drawback of these two mentioned schemes is that the oscillator would be running at 2.4 GHz.

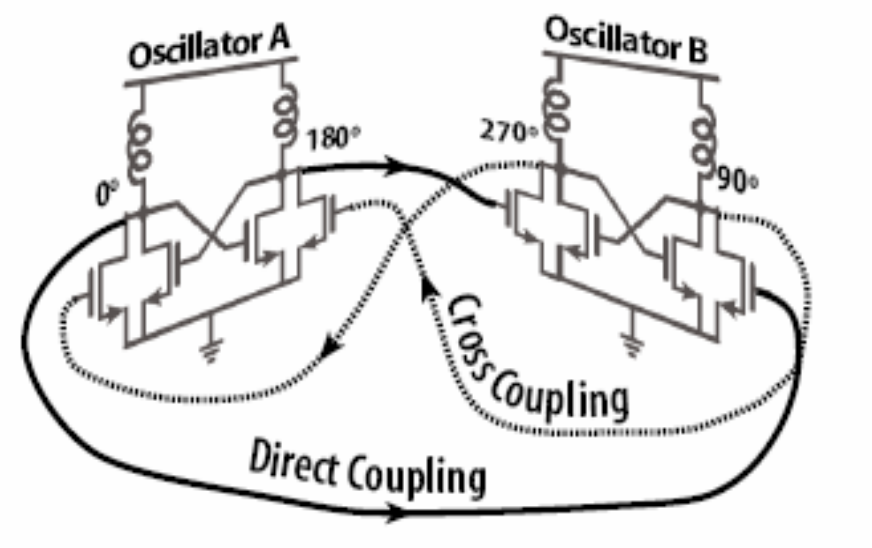


Fig. 4.4 Quadrature VCO [61]

Further, it needs to be mentioned that the R-C, C-R based scheme can be employed for narrow-band architectures only. It might be the preferred solution if the technology happens to limit the maximum frequency of oscillation for the VCO. Since the VCO output is at 5 GHz, which is feasible in this technology, this approach is not preferred in the design. For the hypothetical situation, wherein we are interested in generating I and Q components at 10 GHz, we need to have the VCO running at 20 GHz. Certain calibration techniques can be employed to minimize the I-Q mismatch [24].

TABLE XVII
I-Q GENERATION

Approach	*Comment*	*Drawback*
L-C based, frequency doubling and division by 2	Most accurate I-Q generation; Minimizes injection pulling and PA pulling effects	Additional power-hungry divider
L-C based, quadrature VCO	High frequency I-Q possible	Power consumption and area occupied by inductors doubled.
L-C based, R-C, C-R	High frequency I-Q possible	High mismatch, narrow-band operation only
Ring oscillator based	Inherent I-Q present in the "ring"	High power consumption, poor phase noise

The ring oscillator topology (Fig. 4.5) can give the I-Q components directly due to its "ring" nature [11]. However, at 2.4 GHz, this solution is expensive in terms of power consumption and phase noise performance. Moreover, quadrature generation schemes at 2.4 GHz have poor performance in a transceiver environment. Hence, the L-C based VCO at 5 GHz to be subsequently followed by a divide-by-2 is the best solution. The four cases are given in Table XVII along with their drawbacks.

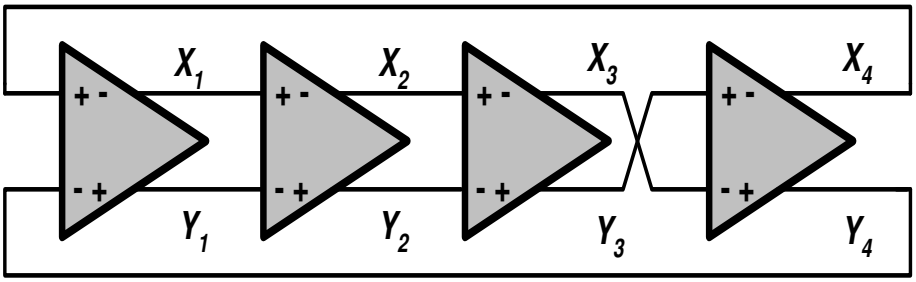


Fig. 4.5 Ring Oscillator

4.1.3 5-GHz L-C VCO

From the previous two subsections, it can be seen that the 5 GHz L-C based oscillator scheme provides the best solution while keeping the issues of injection pulling and I-Q generation in mind. As will be seen in the next section, this affects the tuning range and sensitivity requirements of the VCO. Thus, the selection of the scheme plays an important role in the overall synthesizer design too.

Within the category of L-C VCO's, there exist schemes that differ based on the way the negative transconductor is implemented. The CMOS approach is given in Fig. 4.6 and makes use of both PMOS and NMOS transistors to achieve the $-G_m$. A higher transconductance is possible for the same power consumption as the NMOS only or PMOS only case. However, the effect of parasitic capacitances is more pronounced in the CMOS topology due to the contribution from both the NMOS and PMOS devices. The frequency of oscillation in an L-C based oscillator is given by

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

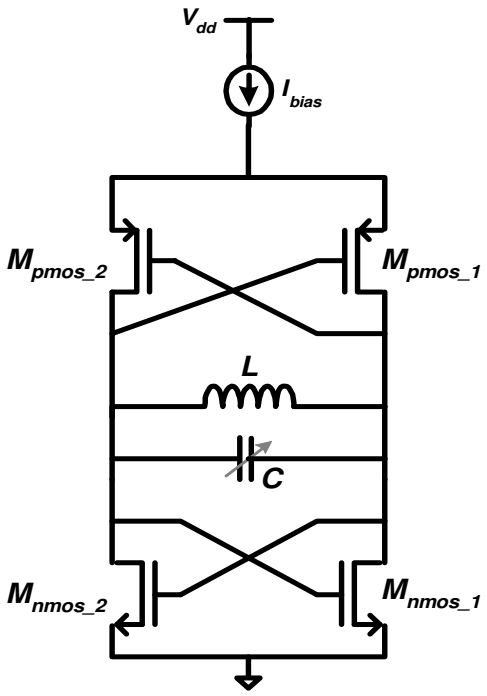


Fig. 4.6 CMOS VCO - Topology

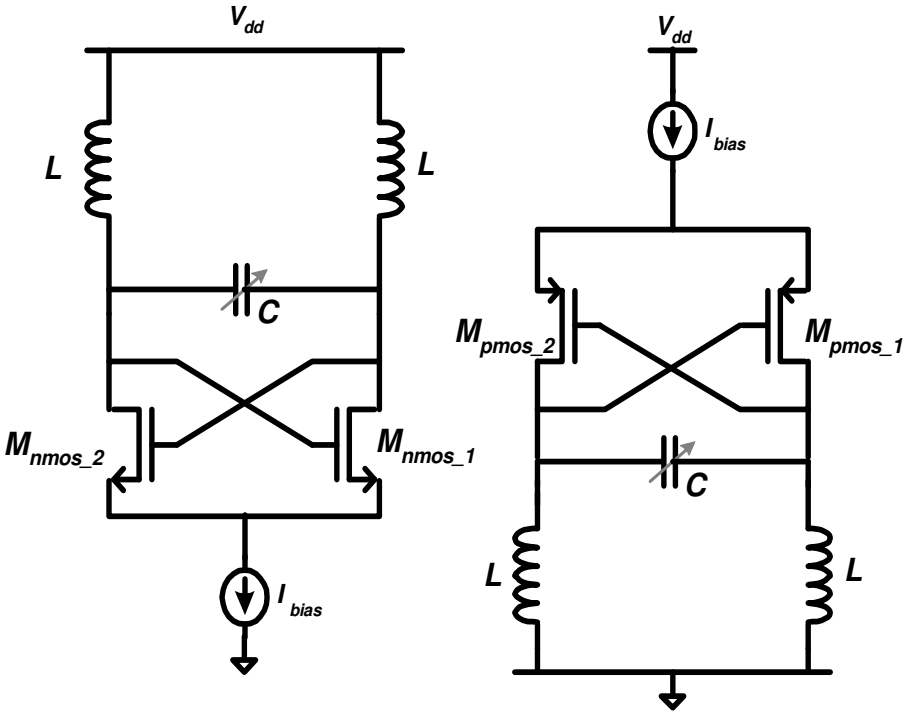


Fig. 4.7 L-C based VCO Topology (a) NMOS Only (b) PMOS Only

Thus, a lower value of inductance is required to ensure the frequency of oscillations. This leads to a decrease in Q and the output voltage amplitude and poorer phase noise performance. Thus, there exists a tight and heavily constrained design space in a VCO making optimization difficult and technology dependent (RF passives – inductor and varactor). Moreover, a differential symmetric inductor with center-tap can be used in the CMOS approach. The differential inductors have a higher Q, implying a better phase noise performance, at the benefit of lower silicon area.

The PMOS only case (as given in Fig. 4.7(b)) needs bulky transistors to achieve the required $-G_m$ despite having lower flicker noise up-conversion. The higher parasitic capacitances affect the tuning range, sensitivity and the output voltage swing of the VCO. The design procedure given in the following sections validates this statement. A parallel topology is the NMOS only case, which is given in Fig 4.7(a). To ensure sustained oscillations, it is a good practice to over design the required $-G_m$. It merits mention that the achieved negative G_m for a given current budget is lower in both of these two cases.

TABLE XVIII
L-C VCO SCHEMES

Approach	*Comment*
CMOS	Higher –Gm possible for same power consumption, improved phase noise, higher output voltage swing, higher parasitic capacitance and lower value of inductance needed for resonance
NMOS only	Limits tuning range, sensitivity and output voltage swing; two spiral inductors
PMOS only	Low flicker noise up-conversion, limits tuning range, sensitivity and output voltage swing; two spiral inductors

Moreover, these topologies require two spiral inductors as against one differential inductor in the CMOS case. This leads to an increased area due to two reasons (i) inductors are known to occupy significant silicon area (ii) the inductors need to be spaced a diameter apart to minimize mutual inductances and coupling. Table XVIII gives a summary of the topologies discussed in this section.

4.2 Passives

The design of an L-C VCO is heavily dependent on the technology. Usually, reasonable models of the passives are available 2-3 years after the original release of technology [62]. Passive characterization continues to be an area of active research and becomes more important, particularly for mm-wave IC design [63-64]. Realization of high-Q inductors and varactors continues to be a bottleneck for the design of high-performance communication circuit systems.

The TSMC 0.18 μm kit makes available inductor and varactor models. In this research, passives were not custom-made and characterized prior to their application in the VCO. The passives available from the kit were used. Nevertheless, a judicious selection of the passives is necessary and this section deals with the different types before zeroing in onto the specific type.

4.2.1 Inductors

The TSMC 0.18 μm has six metal layers M1-M6. The inductors made available through the kit use the highest metal M6 for the spirals. An NTN and a substrate contact layer surround the inductor. Two different types of inductors are available in this

technology, namely the spiral and differential inductor. Prior to their use in the VCO, the two inductors are characterized for their Q. For reasons cited in the previous section, the frequency of oscillation is around 5 GHz.

The CMOS nature makes the two output nodes strictly differential. The VCO is seen as a high-potential tank, wherein the two nodes are slashing back and forth with the current. The pure differential nature of the employed VCO scheme makes possible the use of differential or symmetric inductors with center tap. By their very construction and realization, differential inductors have a higher Q [13].

A high Q is necessary for higher output voltage swing and improved phase noise performance. For systems with low Q, the only method to increase the output voltage swing will be an act of desperation – the increase of power consumption. The high Q nature of the inductor proves to be extremely beneficial in this case, for we will like to minimize the power consumption of the VCO, one of the major contributors in the synthesizer.

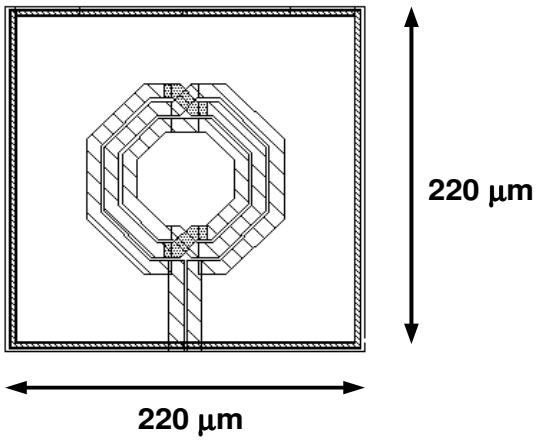


Fig. 4.8 Layout of the Differential Inductor Used in the VCO Design

Additionally, in a CMOS VCO, only one differential inductor needs to be used if employed. This leads to a significant reduction in silicon area. It must be noted that the area occupied by the used differential inductor is around 220µm by 220µm (Refer Fig. 4.8). For architectures, employing two spiral inductors, the silicon area is higher due to the use of two inductors. It merits mention that the two inductors need to be placed a diameter apart to minimize mutual inductance and coupling. Fig. 4.9 gives the Q of the differential inductor used in the VCO as a function of frequency. It is advisable to operate in a region not too close to the frequency where the Q peaks.

Usually, operating at a lower Q, say 40% away from the peak makes the system robust to process variations. If the VCO is designed with an inductor whose Q is at the peak, then with process variations, the actual realized Q might be lesser. This could be of concern, as the original design would have been done using a different Q. A hypothetical situation will be – the power is optimized because of the high Q of the inductor. A high Q implies a lower negative Gm compensation. In reality, the lower Q will be catastrophic. The compensation might not be enough to ensure sustained oscillations.

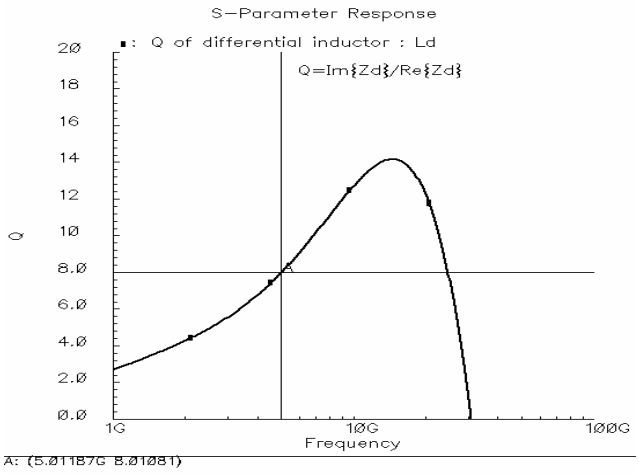


Fig. 4.9 Q of the Differential Inductor Used in the VCO Design

The dimensions of the differential inductor used are given in Table XIX. The Q of the inductor is around 8 at 4.8 GHz (a typical frequency of operation).

TABLE XIX
PARAMETERS OF THE DIFFERENTIAL INDUCTOR

Parameter	*Value*
Model name	spiral_s2_std
Approximate inductance	902.283p H
Inductor width (m)	6µ
Inductor spacing (m)	2µ
Inner radius (m)	30µ
Number of turns	2.5

4.2.2 Varactors

In an L-C based VCO, the exact tuning mechanism is offered by the variable capacitor, known as the varactor. It is very difficult to change the physical value of the inductor used. Various types of varactors are available and a judicious selection of the varactor is extremely crucial for the implementation of the VCO. It is important to have a high Q for the varactors. The TSMC 0.18 µm process makes available the NMOS accumulation mode varactor and the p-n junction based varactor. PMOS inversion mode varactors can also be implemented. A description of these varactors is essential at this juncture.

The voltage dependent capacitor varying nature of the PMOS transistor can be explained using its three modes of operation as follows [65]:

1. Accumulation Mode ($V_{BG}<0$)

   The gate is biased at a higher potential when compared to the bulk. The positive charge at the gate attracts negative charge at its surface. Electrons are

accumulated beneath the surface of the gate. The effective capacitance is now equal to C_{ox}. Refer Fig. 4.10.

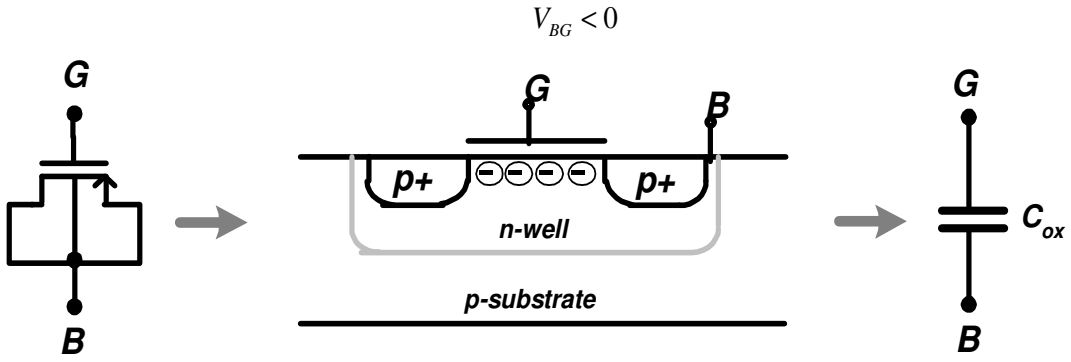


Fig. 4.10 Accumulation Mode of a PMOS Transistor

2. Depletion Mode ($0 < V_{BG} < V_{th}$)

As V_{BG} increases, the density of electrons at the interface reduces, and the device enters weak inversion region. A depletion layer is formed and the effective capacitance of the device is the gate capacitance in series with the depletion layer capacitance, i.e. $C_{ox} \parallel C_d$. Refer Fig. 4.11.

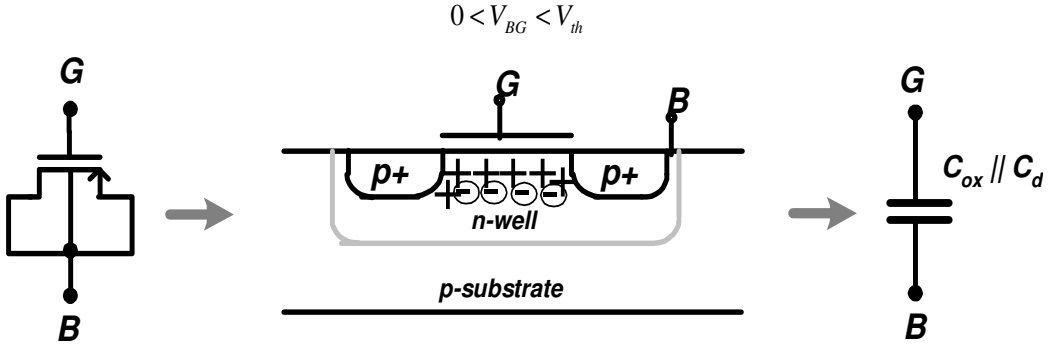


Fig. 4.11 Depletion Mode of a PMOS Transistor

3. Inversion Mode ($V_{BG}>V_{th}$)

In this bias condition, an inverted channel is created and holes flow from the source to the drain. This channel now acts as the positive plate of the capacitor. The effective capacitance is now equal to C_{ox}. Refer Fig. 4.12.

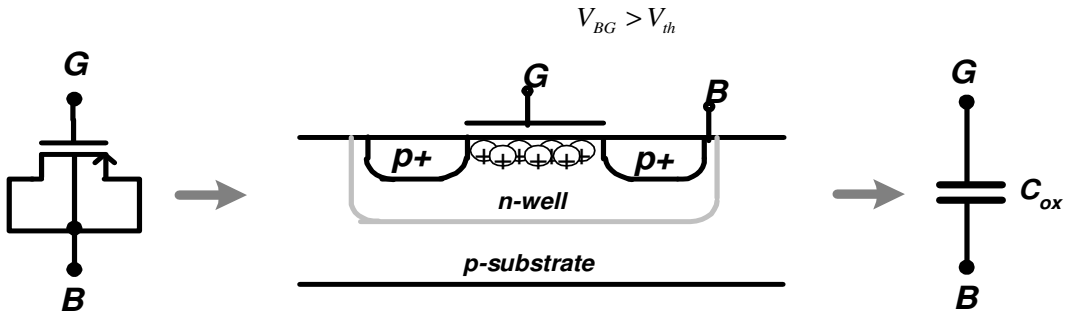


Fig. 4.12 Inversion Mode of a PMOS Transistor

It can be seen from Fig. 4.13 that the slopes are different and the capacitance variation is not monotonic in nature too. The use of a PMOS transistor as a varactor is limited because of this. It will not be possible for the VCO to react in the right manner to the feedback in a PLL. Two methods exist to overcome the non-monotonic nature.

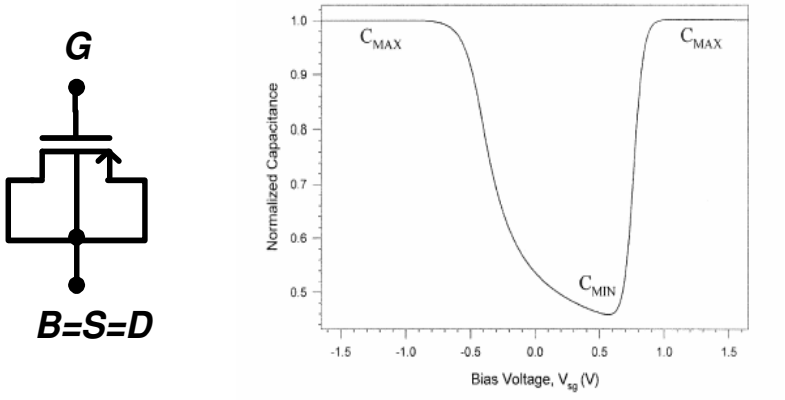


Fig. 4.13 C-V characteristic of a PMOS Device (B=S=D) [66]

1. NMOS Accumulation Mode Varactor

In a PMOS transistor, the S/D regions are p+ and located in an n-well. The NMOS accumulation mode varactor solves the problem of the non-monotonic nature of the PMOS transistor by employing n+ S/D regions in an n-well (Fig. 4.14). For negative gate voltages, it now becomes impossible to invert because of the absence of a p+ region. For gate voltages < V_{th}, the "transistor" is in the depletion mode of operation. For voltages > V_{th}, the "transistor" operates in the accumulation mode.

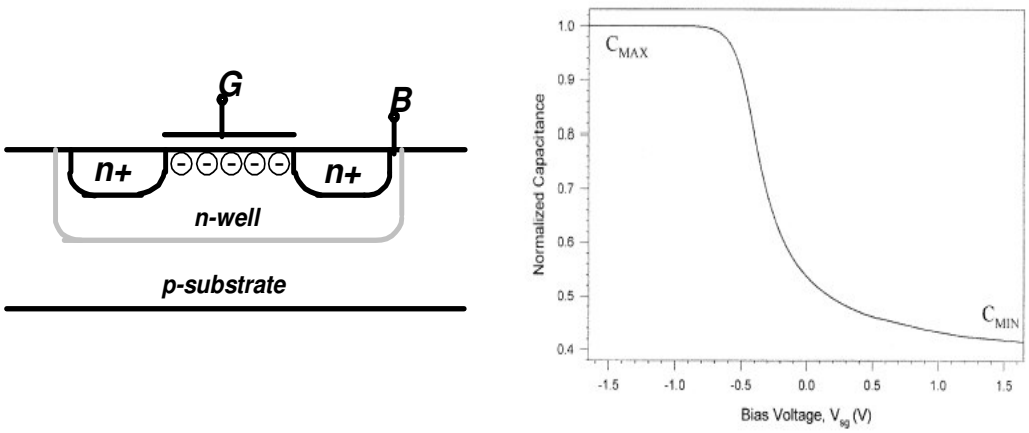


Fig. 4.14 NMOS Accumulation Mode Varactor and Its Characteristic [66]

2. PMOS Inversion Mode Varactor

The bulk terminal is tied to the highest potential Vdd. The gate voltage can never exceed the bulk in this case, and the accumulation mode of operation is not possible. The transistor is now in the inversion mode or depletion mode of operation. Fig. 4.15 gives the characteristic of this varactor.

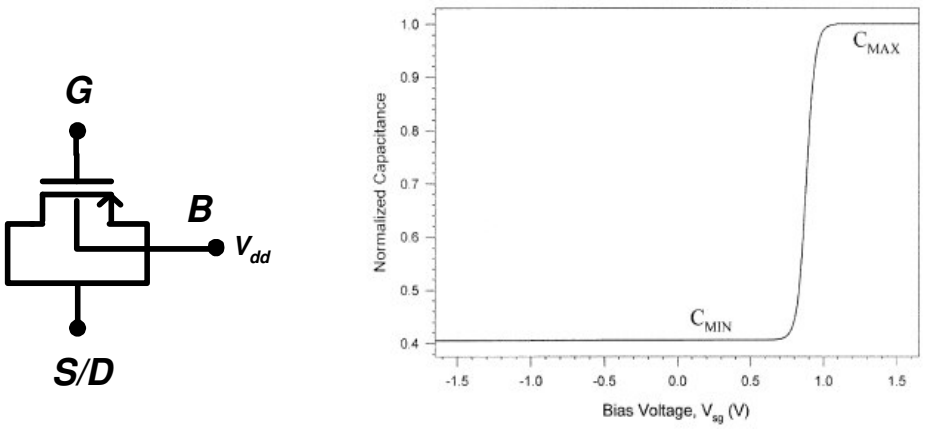


Fig. 4.15 PMOS Inversion Mode Varactor and Its Characteristic [66]

4.3 Specifications

The important performance metrics for a VCO are tuning range, phase noise, sensitivity, and output voltage swing. It merits mention that power consumption of the VCO needs to be minimized and that the VCO is one of the "power-hungry" blocks of the synthesizer. It can be seen that the specifications play an important role in the development of the VCO architecture itself. The VCO design is a complex octagon and is given in the Fig. 4.16.

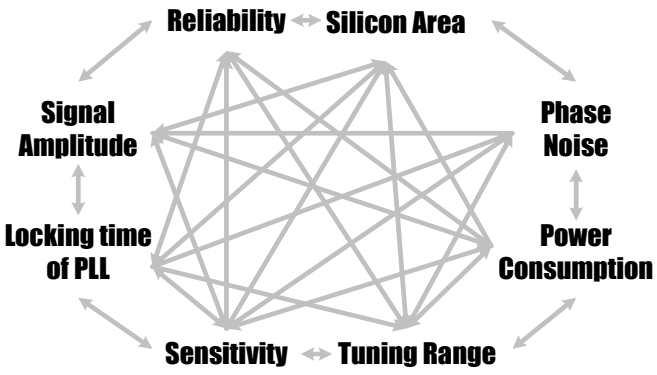


Fig. 4.16 VCO Design Octagon

4.3.1 Tuning Range

The synthesizer needs to synthesize channels in the spectrum of 2400-2480 MHz. However, for reasons elucidated in the preceding sections, we are operating at twice the frequency. Thus, the minimum required tuning range for the VCO is 160 MHz from 4800-4960 MHz. The variations in "L" are negligible as the dimensions are much larger when compared to the minimum feature size.

More than the exact value, the quality factor of the inductor is more susceptible to process variations. On the other hand, the capacitors and varactors vary by almost 20% with process and the VCO needs to be designed for a higher tuning range. We must cover the required tuning range irrespective of the process corner and temperature variations.

Assuming that the technology models for the varactors are fairly accurate, and that the variations due to process can be modeled as γ with a range from 0.9 to 1.1, the new frequency of oscillation is given by

$$f_{osc} = \frac{1}{2\pi\sqrt{L(\gamma C)}} \tag{4.2}$$

The above assumption is justified for advanced technologies like TSMC 0.18 μm, IBM SiGe processes, etc. With this assumption, the tuning range needs to take into account a 5% variation at both ends. Thus, the required tuning range can be taken as 4560-5200 MHz.

4.3.2 Phase Noise

The VCO phase noise is the main contributor of the high frequency phase noise of the overall synthesizer [11]. It is reasonable to assume that the specification for the phase noise of the VCO is the same as that of the synthesizer. Section II gives the derivation for the phase noise of the synthesizer from the standard. Hence, the specification for the phase noise of the VCO can be taken as -110 dBc/Hz at an offset of 10 MHz. When compared to other standards, the specification is relaxed. This proves useful in limiting the current budget for the VCO.

Two popular models exist for the phase noise of an oscillator. Leeson model [19] gives a practical insight into the phase noise characteristic of a real oscillator. An accurate treatment for phase noise is given in [21] by taking into account the non-linear time-varying nature of the oscillator. A detailed analysis and treatment of phase noise is beyond the scope of the thesis. A method for optimization of VCO in the limited design space is given in [32].

4.3.3 Sensitivity

The sensitivity of the VCO plays a crucial role in the PLL loop design. From Section 2, it can be seen as to how this metric of the VCO affects the dynamic response and stability of the control system. Further, the sensitivity of the VCO is the actual gain of the VCO and all of the AM-PM conversion. The ripples at the control voltage of the VCO (primarily due to the charge pump action, explained in Section 3) modulate the control voltage and appear as spurs at the output of the VCO. A high sensitivity leads to high spurs and inferior performance at the transceiver system level.

There exists a clear trade-off between the sensitivity of the VCO and the tuning range. Nowadays, in the event of supply voltage scaling, it is difficult to have a high tuning range due to the limitation in the tuning control voltage range. This makes it necessary to increase the sensitivity of the VCO. This is usually at the cost of spectral performance of the synthesizer. Thus, it is extremely important to determine the required sensitivity of the VCO *a priori* due to its crucial role in the entire loop design.

In the preceding sub-section, the required tuning range of the VCO is 4560-5200 MHz, around 650 MHz. The previous discussion highlighted the importance of having a low sensitivity. With a sensitivity of 150 MHz/V, the required tuning voltage range is around 4.3 V, which is impossible. We therefore need to look for methods to attain this tuning voltage range with an average sensitivity of 150 MHz/V. The next section deals with this issue.

4.3.4 Output Voltage Swing

The output voltage signal strength is an important performance metric for the VCO. The VCO drives the divide by 2, the first block running at 5 GHz in this technology. The VCO and the divider need to work together, in sync with each other, for all possible process variations. Ideally, the negative Gm compensates for the loss in the topology.

However, the usual practice is to over-design the –Gm, to ensure sustained oscillations. Hence there exists a certain finite Q (ideally infinity) of the entire tank consisting of the passives and the –Gm. The Q of the VCO varies across process and frequency, which changes the output amplitude of the VCO. An amplitude control

mechanism can be employed as a solution [55]. Importantly, the output amplitude is a salient parameter in the expression for phase noise.

Table XX gives a summary of the VCO specifications.

TABLE XX
SPECIFICATIONS FOR THE VCO

Performance Metric	*Value*
Frequency Range	4800-4960 MHz
Tuning Range	4560-5200 MHz
Phase Noise	-110 dBc at 10 MHz
Output Voltage Swing	$600mV_{peak}$
Sensitivity	150 MHz/V

4.4 Tuning in a VCO

The transceiver environment and purposes of I-Q generation lead to the doubling of frequency and a minimum tuning range requirement from 4800-4960 MHz. The need for robustness in a VCO required a tuning range of 4560-5200 MHz. It is desired to keep the sensitivity low for better spur performance. With the limited tuning voltage range constraint, it is difficult to achieve such low sensitivities. Further, it merits mention that in a charge pump based PLL scheme, the locking range is limited by the tuning range of the VCO [11].

The "broadband" tuning range for the VCO can be achieved by employing the discrete tuning mechanism (Fig. 4.17). A set of externally tunable varactors can be used to tune the frequency range of operation in a coarse manner. These varactors are not in the main PLL loop. The varactor for fine-tuning the VCO (using the feedback voltage information) needs to have a low sensitivity. Due to process variations, the VCO could

then be working from 4600-4800 MHz. Using the discrete tuning mechanism; we can shift the VCO to 4800-4960 MHz and then synthesize the 16 channels as desired.

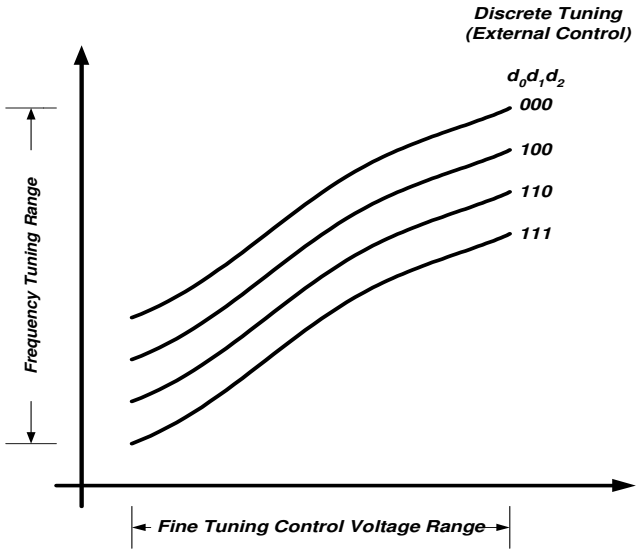


Fig. 4.17 Broadband Tuning Range Using Discrete Tuning Mechanism

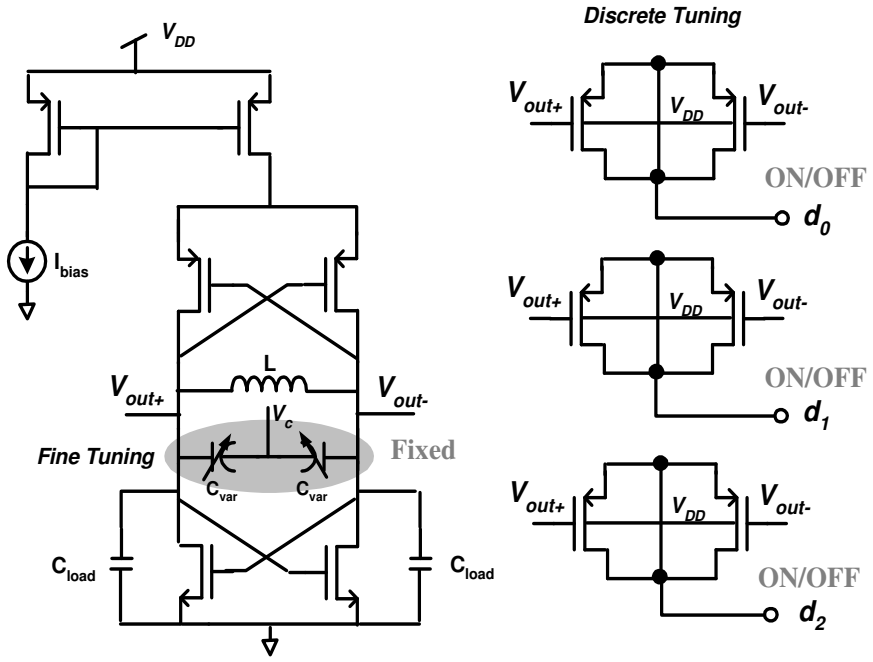


Fig. 4.18 CMOS VCO with Discrete Tuning - Topology

The PMOS inversion varactors are used for coarse tuning and the junction varactor is used for fine tuning the VCO. The selection of a 3V supply in the preceding stage helps us achieve a tuning voltage range from 0.5-2.5V. Thus, we need to use varactors that can operate safely till 3V. The NMOS accumulation varactor and the PMOS inversion varactors saturate beyond 1.8V and show very low gain at these voltages. Thus, junction varactors provide us the best choice. The use of junction varactors requires that sufficient care be taken to prevent them from going into a deep forward bias region of operation [11].

The junction varactors further have a low gain and a monotonically increasing characteristic. However, they cannot be used for discrete tuning because of their low gain. The very feature that made them the only solution for fine-tuning proves to be detrimental here. We will not have a sufficient tuning range when junction varactors are used. To have a high tuning range (achieved by coarse tuning), the varactors need to show significant frequency shifts. It is proposed to use a bank of three PMOS inversion mode varactor array as shown in the Fig. 4.18 All three of them are identical, and this leads to four different tuning ranges, based on their ON/OFF status.

TABLE XXI
CAUSE-AFFECT RELATION IN A CMOS VCO

Cause	*Affected Performance Metric*	*Action*
Injection Pulling, PA pushing, accurate I-Q generation	Frequency of oscillation, Tuning Range	4800-4960 MHz tuning range; VCO design at 5 GHz
High sensitivity to process variations and need for robustness	Tuning Range, Sensitivity	Tuning range is 4560-5200 MHz; sensitivity fixed at 150 MHz/V
Low sensitivity and a tuning control voltage range from 0.5-2.5V	Output voltage swing, Phase Noise	Junction varactors used for the fine control tuning mechanism; Deep forward bias region of operation is not permissible.
High tuning range required at low sensitivity	Output voltage swing, Phase Noise	Use of discrete tuning; and bank of varactors. Careful layout techniques to improve the effective Q of the tank.

The use of discrete tuning mechanism has the disadvantage of increasing the "capacitive" load of the VCO. This forces us to have a lower inductance value, which in turn relates to the output voltage swing of the VCO. The output voltage of the VCO is given by [32]

$$V_{osc} = I_{tail} R_{L\_parallel} \text{ for current-limited regime} \tag{4.3}$$

$$V_{osc} = V_{\max} \text{ for voltage-limited regime} \tag{4.4}$$

Here, R_p is the parallel equivalent of R_s, and is related to the Q of the inductor by

$$R_{L\_parallel} = Q^2 R_L = \frac{\omega^2 L^2}{R_L}, \text{ where } Q = \frac{\omega L}{R_L} \tag{4.5}$$

From Eqn. 4.5, it is clearly seen that the use of a lower value of L reduces the Q of the overall tank, leading to a lower output voltage swing. Further, the phase noise of the VCO, which is given as a function of the output voltage amplitude in Eqn. 4.6, deteriorates.

$$PN = f\left(\frac{L^2 I_{tail}}{V^2_{osc}}\right) \tag{4.6}$$

Thus, the design of a VCO is severely constrained by a host of conflicting parameters and requirements. Table XXI gives the cause-effect relationship in a VCO.

4.5 Design Procedure

The design procedure in a VCO is iterative in nature. A good starting point is given by the procedure outlined below.

4.5.1 Bias Current

The bias current is an important design parameter. It controls the output voltage swing and thereby the phase noise of the VCO. For the CMOS version,

$$V_{osc} = I_{tail} R_{L\_parallel} \text{ where } R_{L\_parallel} = Q_L^2 R_L \quad (4.7)$$

The –Gm needed might be high, necessitating the use of bulky transistors for low tail currents. The bulky transistors decrease the tuning range and the sensitivity too, because of the increase in the parasitic capacitances. As a starting point, the current is taken as 3 mA for a supply voltage of 1.8V. We need to minimize the current consumption of the VCO, one of the major contributors to the overall power consumption of the synthesizer.

4.5.2 Inductor

The inductor value is extremely crucial as it has a direct role to play in the phase noise, output voltage swing, tuning range, sensitivity of the VCO. A high inductor value will lead to a high output voltage swing and improved phase noise performance. However, this is at the expense of the tuning range. The capacitor variation required becomes very small, making it difficult to achieve the sensitivity for the VCO. It merits

mention that the ratio of the varactor capacitance to the total capacitance in the tank is a measure of the sensitivity of the VCO. Eq. 4.7 can be written as Eq. 4.8.

$$\text{Tuning Range} = \frac{1}{2\pi\sqrt{L}}\left(\frac{1}{\sqrt{C_{tot\_\min}}} - \frac{1}{\sqrt{C_{tot\_\max}}}\right) \tag{4.8}$$

$$V_{osc} = I_{tail} R_{L\_parallel} \text{ where } R_{L\_parallel} = Q_L{}^2 R_L = \left(\frac{\omega L}{R_L}\right)^2 R_L \tag{4.9}$$

L needs to be minimum for tuning range considerations; and maximum for output voltage swing and phase noise considerations. Thus, there exists a clear trade-off in the inductor value.

Using discrete tuning mechanism, we will ensure that the VCO covers the required band from 4800-4960 MHz. For purposes of hand calculation, we assume that the VCO needs to cover 4750-5000 MHz. To achieve a fine tuning range of 250 MHz, and a sensitivity of 150 MHz, we need a control voltage range of

$$\Delta V_{control} = \frac{Fine\_tuning\_range}{Sensitivity} = 1.67V \tag{4.10}$$

The use of 3V supply in the preceding section makes this control voltage range a permissible and achievable one.

As a starting point, the inductor value is assumed to be 1nH. With post layout simulations, the final value might need to be tweaked. For a 1nH differential inductor, the Q was found to be 8 at 5 GHz (Fig. 4.9).

$$R_L = \frac{\omega L}{Q_L} = \frac{2\pi \cdot 5 \cdot 10^9 \cdot 1 \cdot 10^{-9}}{8} = 1.25\pi \approx 4\Omega \tag{4.11}$$

$$R_{L\_parallel} = Q_L{}^2 R_L = 8^2 \cdot 4 = 256\Omega \tag{4.12}$$

$$V_{osc} = I_{tail} R_{L\_parallel} = 3 \cdot 10^{-3} \cdot 256 = 0.768V \tag{4.13}$$

This gives peak-to-peak signal amplitude of 0.768 V for the oscillator. For purposes of hand calculations, this is a healthy value in the design. Higher peak-to-peak signal amplitude implies improved phase noise performance.

4.5.3 Varactor

We need a sensitivity of 150 MHz and a tuning range from 4750-5000 MHz. Further the inductance value was taken as 1 nH in the previous section. In the CMOS topology of the L-C VCO, the total capacitance at each output end is given as

$$C_{tot} = C_{fine\_\mathrm{var}} + C_{disc\_\mathrm{var}} + C_{p\_NMOS} + C_{p\_PMOS} + C_{Load} \tag{4.14}$$

where C_p's are the parasitic capacitances of the NMOS and PMOS transistors used for – Gm implementation. The discrete tuning varactors used for robustness to process variations consume a significant part of the overall total allowable capacitance. The CMOS nature almost doubles the parasitic capacitances. C_{Load} is the input capacitance of the load, which includes the VCO buffer (used for test purposes and characterization of the phase noise and spurs) and the following divide-by-2 for I-Q generation.

Thus, we can see that there is very little room for optimization and that the sensitivity of the VCO can be given as a function of

$$Sensitivity = f\left(\frac{C_{fine\_\mathrm{var}}}{C_{fine\_\mathrm{var}} + C_{disc\_\mathrm{var}} + C_{p\_NMOS} + C_{p\_PMOS} + C_{Load}}\right) \tag{4.15}$$

To achieve the fine tuning range, the total capacitance variation is from 1.122pF to 1.013 pF. Since, we will need a fine tuning control voltage range from 1-2.5 V, for application in the synthesizer, a junction varactor is used. We need to ensure that the junction varactor is never in deep forward bias region of operation (Fig. 4.19).

From our design calculations, the output single-ended peak-to-peak amplitude is 0.768V (approximated to 0.8V). The DC bias for the output can be assumed to be slightly less than $V_{dd}/2$, so as to leave sufficient margin for the PMOS current mirror for biasing. Assuming a V_{DS} of 300mV, the DC bias at the output can be assumed to be 0.75V. The output voltage swing (DC+AC) varies from 0.35V to 1.15V. This is the p-terminal of the junction varactor. The n-terminal of the junction varactor (control voltage) varies from 1V to 2.5V. The worst-case forward-bias voltage drop across the junction varactor is 150mV. Thus, we ensure that the varactor is never in deep forward bias condition.

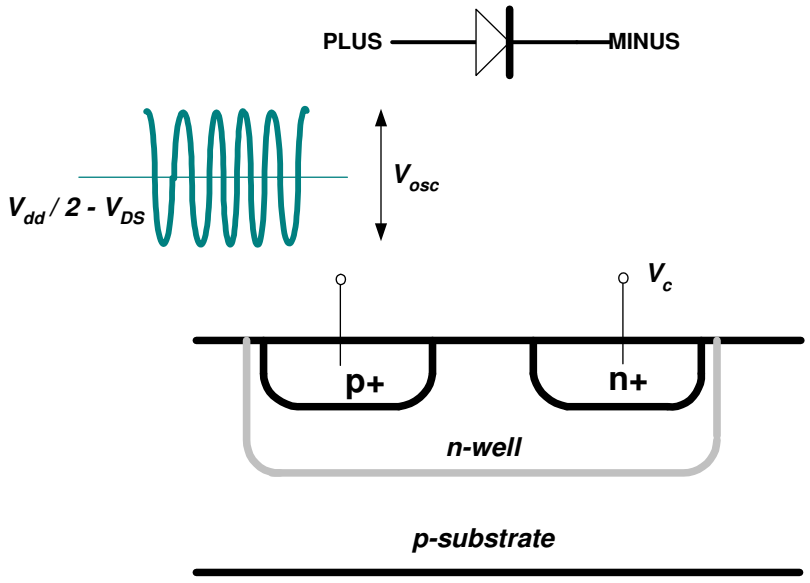


Fig. 4.19 Issue of Forward Bias in a Junction Varactor

4.5.4 CMOS Drivers

The architecture is based on the compensation of the loss in the VCO using –Gm obtained from the cross-coupled NMOS and PMOS transistors. The elements of loss in the VCO include the finite Q of the inductors and varactors; and the output impedances of the cross-coupled transistors and are given in Fig. 4.20. These elements are modeled as R_L, R_V, r_{on}, r_{op}. It merits mention that R_L, R_V are in series to the inductor and varactor elements. R_m takes into account the miscellaneous loss elements in the VCO not modeled.

$$\text{Now, } R_{L\_parallel} = Q_L{}^2 R_L = \frac{\omega^2 L^2}{R_L} \tag{4.16}$$

$$\text{Similarly, } R_{V\_parallel} = Q_V{}^2 R_V = \frac{1}{\omega^2 C^2 R_V} \tag{4.17}$$

For oscillations,

$$\left|G_m\right| = \left[\frac{1}{r_{on} \left\| r_{op}\right.} + \frac{1}{R_m} + \frac{1}{R_{V\_parallel}} + \frac{1}{R_{L\_parallel}}\right] \tag{4.18}$$

It is difficult to predict all the loss elements in an accurate fashion. Hence, it is advisable to over-design for the –Gm so as to ensure oscillations. The limited supply voltage "amplitude limits" the oscillations.

For sustained oscillations,

$$\left|G_m\right| = \alpha_{\min}\left[\frac{1}{r_{on} \left\| r_{op}\right.} + \frac{1}{R_m} + \frac{1}{R_{V\_parallel}} + \frac{1}{R_{L\_parallel}}\right] \tag{4.19}$$

where $\alpha_{\min}$ is the minimum excess loop gain to ensure startup in the worst case condition and can be taken as 3 [32]. In Eqn. 4.19, the contribution of the output impedances and the miscellaneous "resistor" can be assumed to be negligible. Eqn. 4.19 can be further simplified as

$$|G_m| = 3\left(\frac{1}{Q_V{}^2 R_V} + \frac{1}{Q_L{}^2 R_L}\right) \tag{4.20}$$

The inductor losses are more dominant than the varactor losses. Hence, for the purpose of hand calculation, it is reasonable to assume that

$$|G_m| \approx 3\left(\frac{1}{Q_V{}^2 R_V}\right) = 11.7mA/V \tag{4.21}$$

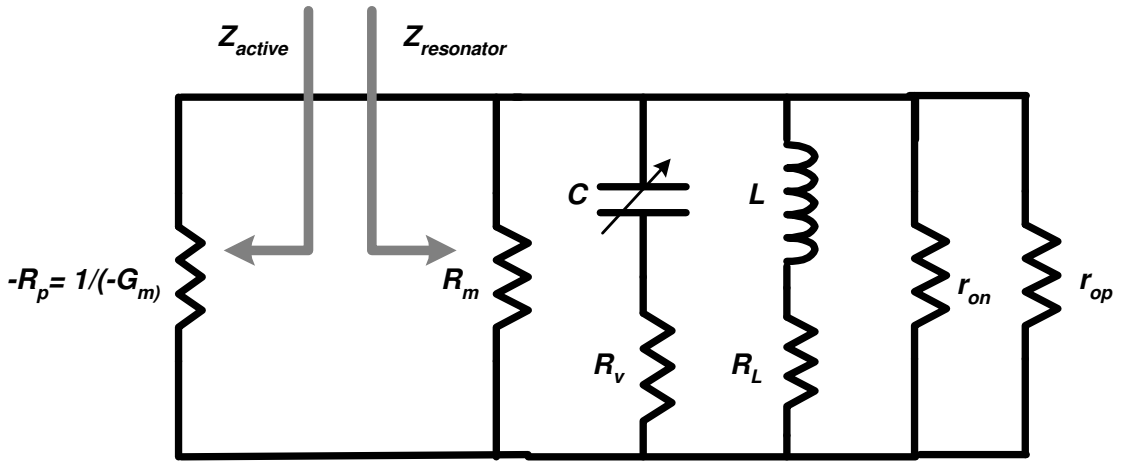


Fig. 4.20 Elements of Loss in an L-C VCO Using the One-Port Model

4.6 Layout Issues

Careful layout techniques greatly improve the performance of the VCO during post-layout simulations. The ASSURA extractor takes the parasitic resistors and capacitors to substrate into account. For high frequency simulations, the results will be closer to reality with the use of this extractor. However, it needs to be mentioned that complete reliance on the extractor might prove detrimental. It is always a good practice to analyze why things happen as they happen.

From the elaborate design procedure given in the previous section, the importance of a high-Q system is highlighted. The discrete tuning varactors are realized using PMOS inversion mode varactors that are essentially PMOS devices with a certain W/L. It is advisable to use multipliers so as to avoid large values of W that increases the gate resistance [57]. Moreover, the technology offers us a choice of 6 metal layers. The high frequency signal lines are routed in M5 or M6. These metals offer a lower resistivity and thereby, help improve on the Q of the varactors. Post-layout simulation results revealed an increase of almost 50% from 600mV peak single-ended signal swings to 900mV peak.

The CMOS VCO is a truly symmetric VCO, with identical set of CMOS drivers and varactors at both ends of the output. It is extremely important to maintain the symmetric nature of the VCO in the layout stage. Fig. 4.21 shows the line of symmetry and the carefully drawn layout for the VCO. The differential inductor with center tap is a symmetric device too.

Usually, for high frequency applications, it is recommended to use the RF transistor models. Each RF transistor comes with its own localized guard-ring and shield. As a result, they occupy more area than the regular transistors. The use of RF transistors in the VCO increases the area and length of the interconnects, connecting the output lines

to the transistors. This is not beneficial for RF circuits. Hence, in such situations, it is the practice to have localized shields or guard rings.

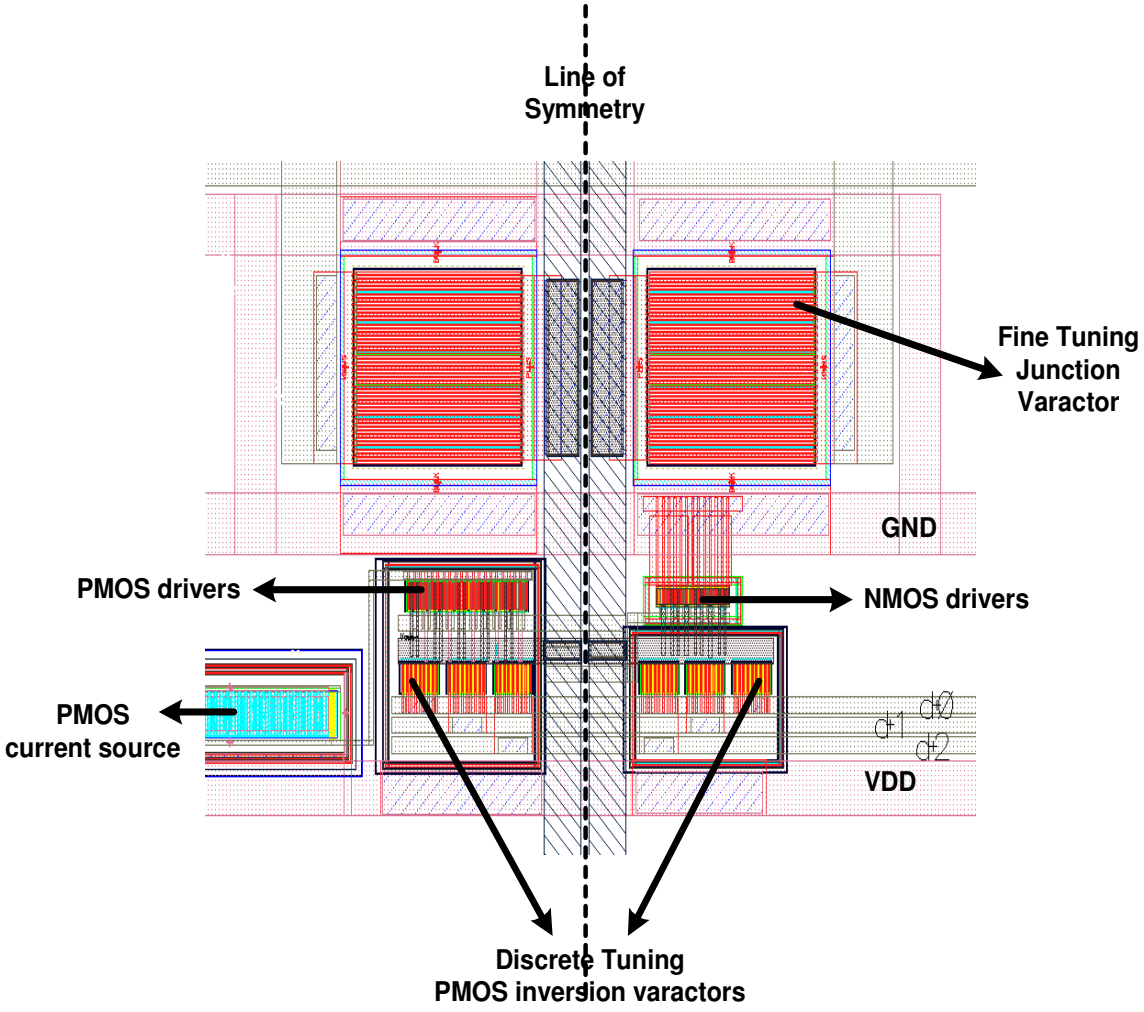


Fig. 4.21 Layout of the VCO – CMOS Drivers and the Varactors

The NMOS devices (namely the drivers) have their own substrate contact ring, connected to the most positive supply for reverse bias. Similarly, the PMOS devices (the drivers and the inversion mode varactors) are encased in an N-well contact ring, which is

connected to the ground. This helps improve the isolation. The inductor, which is encased in its own substrate ring, is spaced appropriately so as to minimize the effect of radiation to the surroundings.

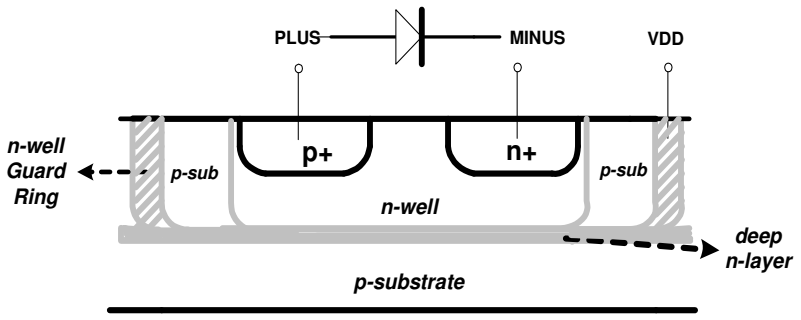


Fig. 4.22 Problem of Guard Ring around the Junction Varactor

The use of guard-rings improves isolation and substrate noise rejection [56]. In this case, a guard ring can be used, but care should be taken so as not to encase the junction varactors. This is because the control voltage (the n-side of the junction) is shorted to the n-well through the deep *n* layer. It must be remembered that the n-well of the guard ring is connected to the highest possible supply, in this case *Vdd*, so as to prevent forward bias. From this, it can be seen that with the guard ring encasing the junction varactors, the control voltage is always connected to *Vdd*. (Fig 4.22).

The VCO fails to work as a “voltage-controlled” oscillator. It will give a fixed tone at the output. It will obviously fail, in the synthesizer system. Further, the inductor doesn’t allow any layer beneath the M6 and above the substrate. Hence, the guard ring cannot cover the inductor too. In this specific case, the guard ring for the VCO can be avoided, provided there is localized shielding.

TABLE XXII
TUNING RANGE WITH PROCESS VARIATIONS

Tuning Voltage	*Post Layout Simulation*		
	SS corner (MHz)	*TT corner (MHz)*	*FF corner (MHz)*
1-2.5 V, 000	4836-5073	5020-5236	5184-5381
1-2.5 V, 100	4698-4914	4874-5070	5030-5210
1-2.5 V, 110	4570-4770	4737-4910	4890-5050
1-2.5 V, 111	4450-4633	4610-4780	4756-4910
Tuning Range	623	626	625

The post-layout results for the four tuning cases are given in the Fig. 4.23. We can see that the VCO has a tuning range from 4610-5236 MHz with an average sensitivity of 135 MHz/V, as per the “tt” corner simulations. Since the VCO is highly dependent on passives and sensitive to process variations, the VCO needs to be optimized across process corners too. We must ensure that the required band from 4800-4960 MHz is covered, irrespective of the process and temperature variations. From Table XXII, it can be seen that the “111” tuning case for the “ff” corner and the “000” tuning case for the “ss” corner covers the required band.

The corners model the process variations in the IC design tool. It is a good practice to simulate the design in post-layout across all corners. The “ss” corner is the slow-slow corner; where the devices operate slower than expected. Similarly, “tt” and “ff” are to model the typical-typical and fast-fast scenarios for the NMOS and PMOS devices.

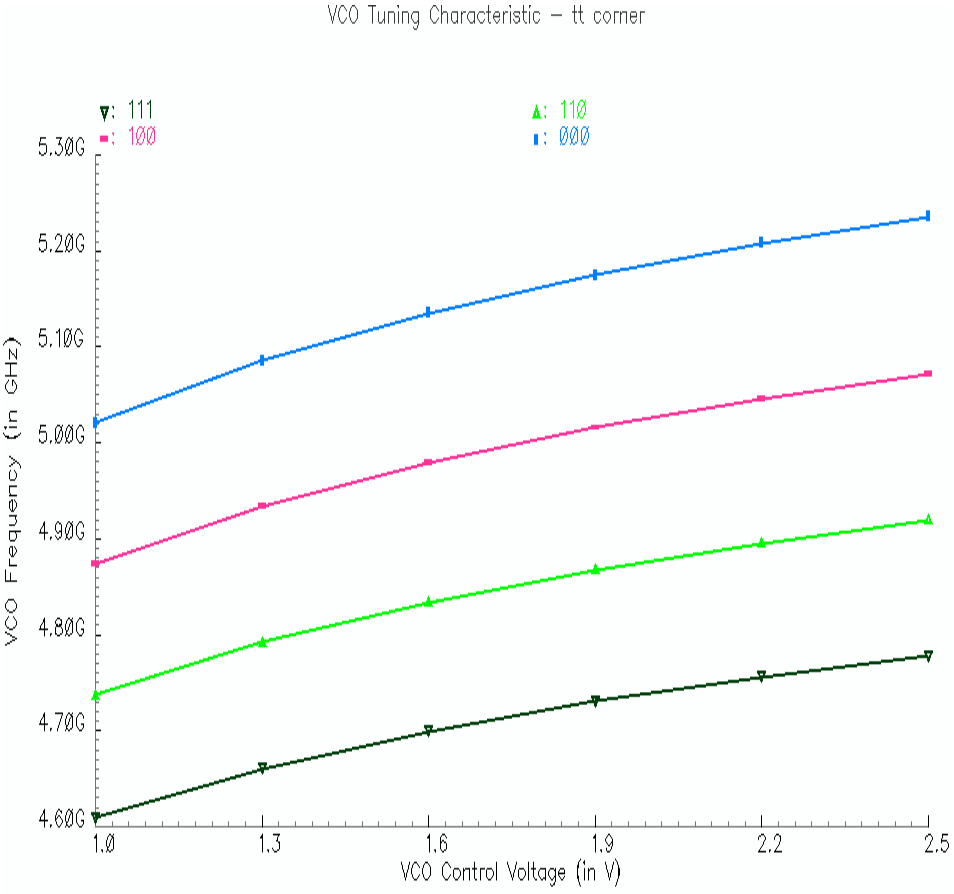


Fig. 4.23 Post Layout Results of the VCO– "TT" Corner

The layout of the VCO is given in Fig. 4.24.

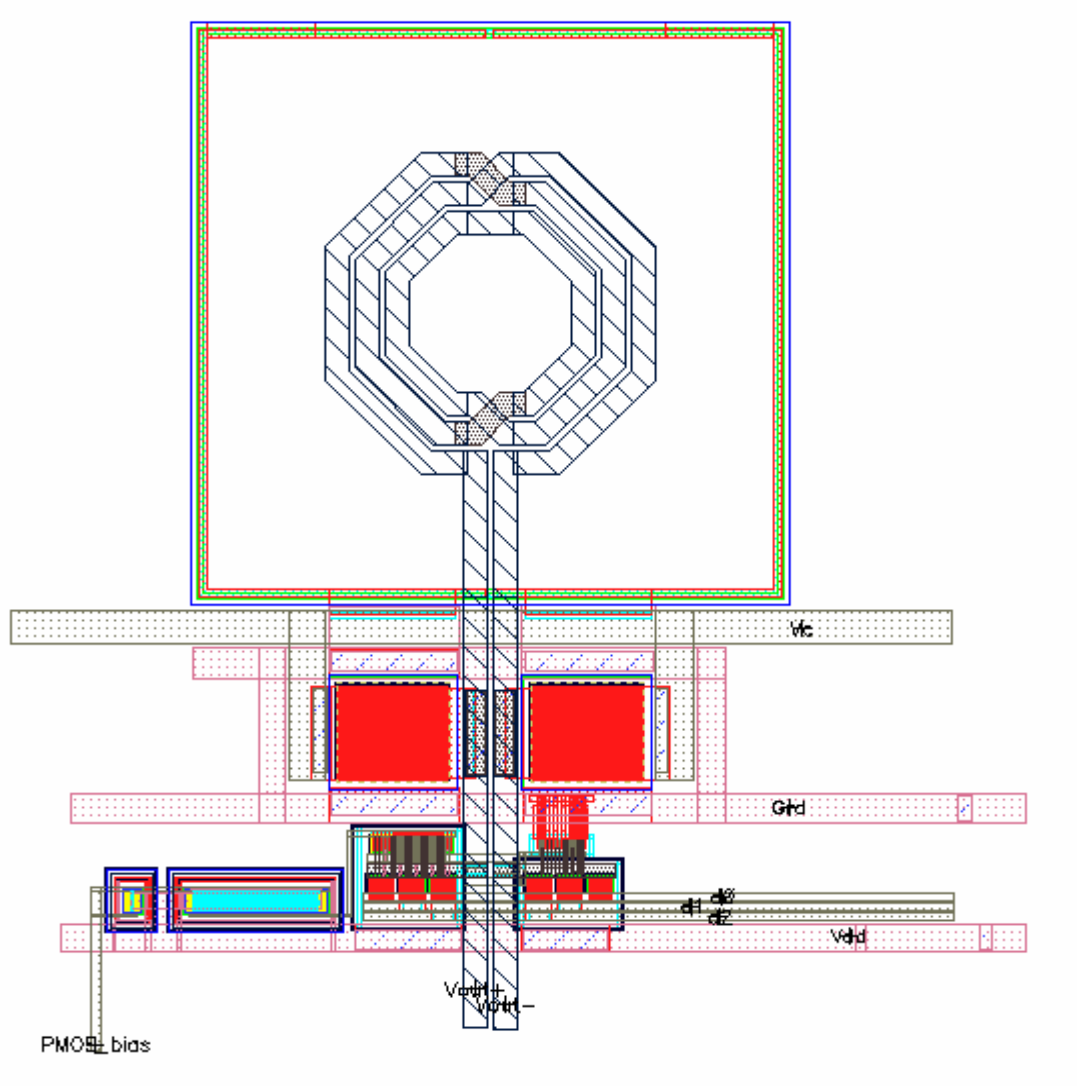


Fig. 4.24 Layout of the VCO

4.7 Testing and Measurement

The issues of testing bench setup and board-level considerations for the VCO characterization are given in the Section 3. A printed circuit board (PCB) dedicated for VCO characterization was prepared to check for functionality and tuning range of the VCO. The synthesizer PCB can be used for VCO characterization in the open loop by not powering on the rest of the circuitry. The output spectrum of the VCO and the tuning

range of the VCO is given here for the sake of completeness. In the open loop characterization of the VCO, there is absence of reference spurs. In Fig. 4.25, the spur at an offset of 4 MHz is due to the dividers. The synthesizer is tested in open loop by not providing the reference.

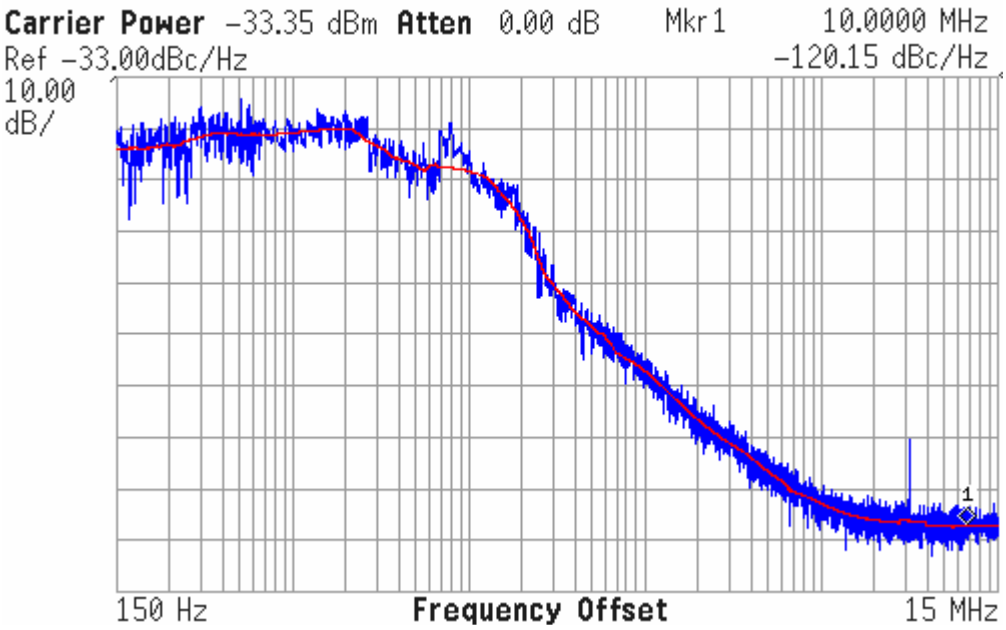


Fig. 4.25 Phase Noise of the VCO Output

The VCO tuning characteristic is given in Fig. 4.26. We can see that the VCO has a broad tuning range from 4580-5275 MHz with an average sensitivity of 135 MHz/V. Thus, this VCO can be used in a 2.4 GHz Zigbee synthesizer environment. Since the locking range of a charge-pump based PLL is limited by the tuning range of the VCO, the VCO can also be applied to other 5 GHz systems to generate frequencies in the range of 4580-5275 MHz. The discrete tuning technique is also a neat way of achieving a broadband VCO.

TABLE XXIII
TUNING RANGE WITH PROCESS VARIATIONS AND MEASUREMENT RESULTS

Tuning Voltage	*Post Layout Simulation*			*Measurement (MHz)*
	SS corner (MHz)	*TT corner (MHz)*	*FF corner (MHz)*	
1-2.5 V, 000	4836-5073	**5020-5236**	5184-5381	**5051.1-5275.5**
1-2.5 V, 100	4698-4914	**4874-5070**	5030-5210	**4880.7-5082.1**
1-2.5 V, 110	4570-4770	**4737-4910**	4890-5050	**4726.5-4910.2**
1-2.5 V, 111	4450-4633	**4610-4780**	4756-4910	**4589.2-4758.5**
Tuning Range	623	**626**	625	**686.3**

Table XXIII gives a comparison between the post-layout results and the test measurement results. Thus, we can see that the measurement results are in close agreement with the "tt" corner post-layout simulation results.

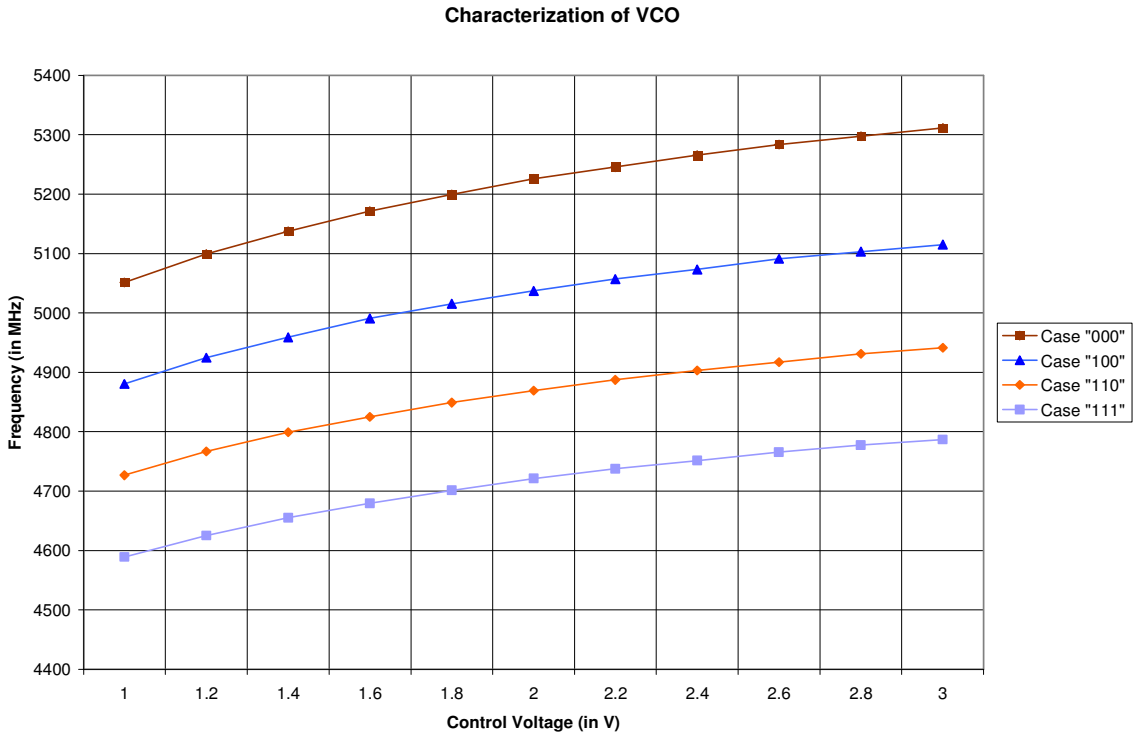


Fig. 4.26 Measurement Results – VCO with CML Load

5. CONCLUSIONS

This thesis dealt with a complete step-by-step procedure from interpreting the Zigbee standard to the derivation of the important specifications to the design and implementation of an integer-N PLL based frequency synthesizer. The application of the synthesizer in a transceiver environment was an important paradigm that required constant attention. A system design procedure was developed for the PLL keeping the settling time and stability considerations in mind.

Certain system level strategies were followed that enabled the realization of a high-performance charge pump and a low sensitivity for the VCO. The sensitivity of the VCO was measured to be around 135 MHz/V with broadband tuning range from 4580-5275 MHz. Four different supplies were used to isolate the critical RF and analog sections from the noisy environment of the dividers.

The synthesizer solution was a complete on-chip implementation and was fabricated in a TSMC 0.18 μm CMOS technology. It was found to consume 15.5 mW and able to meet the specifications of the Zigbee standard. The analog section and the VCO contributed to 38% of the total power. The phase noise was obtained to be -130 dBc/Hz at 10 MHz offset; and the spur suppression was found to be -40 dBc at 5 MHz offset. Test measurement results were in corroboration with the post-layout results.

The design of high-performance synthesizers in the wake of supply scaling and optimization for spurs will be an interesting problem to pursue. The power consumption of the present synthesizer can be reduced further. The CML divider drives the TSPC prescaler through a CML buffer, which consumes substantial power (close to 5 mW). Other dynamic styles that do not require a high input signal swing could be used.

We showed that low sensitivity VCOs could be realized at 5 GHz by the use of discrete tuning. Further, the sixteen channels were synthesized as per the Zigbee specifications. It was also seen that the procedure followed from the very beginning to the end was generic and applicable to any standard. The clock reference and the channel selection counters, characterize the Zigbee flavor. The digital counters do not consume much power. Most of the power is consumed by the RF blocks of the VCO, CML, Prescaler and associated circuitry. Hence, it is justifiable to conclude that the power consumption of the synthesizer for a wireless standard is totally determined by the high-frequency blocks.

The quality of the passives and the stringent spectral purity requirements determines the power consumption of the VCO. Thus, we can show that the overall power consumption of the synthesizer for this integer-N PLL based scheme will be dependent on the specifications. With specifications being similar, the power consumption will be on similar lines. An appropriate change in the digital counters and the clock reference, provided the loop is stable, will result in frequency synthesis for other standards. It can also be claimed that the synthesizer can also function as a 5 GHz synthesizer with a locking range limited by the tuning range of the VCO.

The supremacy of the integer-N PLL based scheme is the feasibility of complete monolithic CMOS implementations with minimal cost, area and power overheads.

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