A LOW POWER, HIGH DYNAMIC RANGE, BROADBAND VARIABLE GAIN AMPLIFIER FOR AN ULTRA WIDEBAND RECEIVER

A Thesis

by

LIN CHEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2006

Major Subject: Electrical Engineering

A LOW POWER, HIGH DYNAMIC RANGE, BROADBAND VARIABLE GAIN AMPLIFIER FOR AN ULTRA WIDEBAND RECEIVER

A Thesis

by

LIN CHEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Laszlo Kish
	Charles S. Lessard
Head of Department,	Costas Georghiades

May 2006

Major Subject: Electrical Engineering

ABSTRACT

A Low Power, High Dynamic Range, Broadband Variable Gain Amplifier for an Ultra Wideband Receiver.

(May 2006)

Lin Chen, B.E., Tsinghua University; M.E., Cornell University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

A fully differential Complementary Metal-Oxide Semiconductor (CMOS) Variable Gain Amplifier (VGA) consisting of complementary differential pairs with source degeneration, a current gain stage with programmable current mirror, and resistor loads is designed for high frequency and low power communication applications, such as an Ultra Wideband (UWB) receiver system. The gain can be programmed from 0dB to 42dB in 2dB increments with -3dB bandwidth greater than 425MHz for the entire range of gain. The 3rd-order intercept point (IIP3) is above -13.6dBm for 1Vpp differential input and output voltages. These low distortion broadband features benefit from the large linear range of the differential pair with source degeneration and the low impedance internal nodes in the current gain stages. In addition, common-mode feedback is not required because of these low impedance nodes. Due to the power efficient complementary differential pairs in the input stage, power consumption is minimized (9.5mW) for all gain steps. The gain control scheme includes fine tuning (2dB/step) by changing the bias voltage of the proposed programmable current mirror, and coarse tuning (14dB/step) by switching on/off the source

degeneration resistors in the differential pairs. A capacitive frequency compensation scheme is used to further extend the VGA bandwidth.

DEDICATION

To my parents and my sister for their unconditional support and love

ACKNOWLEDGEMENTS

I would like to express many thanks and much appreciation to Dr. Jose Silva-Martinez, for his kindly guidance and attention to details throughout my study. I am also grateful to my thesis committee members, Dr. Edgar Sanchez-Sinencio, Dr. Laszlo Kish and Dr. Charles Lessard, for providing additional insight throughout this process. I would also like to thank Johnny Lee, Jun He, Jason Wardlaw, Xiaohua Fan, and Haitao Tong for their help on proofreading my thesis draft. My gratitude goes to all of the faculty and students of the Analog and Mixed Signal group who have raised my level of, and enthusiasm for, knowledge, and have aided me in reaching my goals. Most of all, I would like to thank my parents and my sister for their unconditional support, trust, encouragement and love through the years.

TABLE OF CONTENTS

CHAPTER Page

LIST OF FIGURES

Page

Page

Page

Page

LIST OF TABLES

Page

Page

CHAPTER I

INTRODUCTION

A Variable Gain Amplifier (VGA) is needed in many baseband circuits for communication applications. For example, in a RF receiver, it is required to use a VGA between the filter and the analog to digital converter (ADC), to adjust the output signals from the filter to the required input signal level of the ADC; hence, providing the largest signal-to-noise ratio to the ADC stage and improving the overall dynamic range of the receiver.

A Multi-Band Orthogonal-Frequency-Division-Multiplexing (MB-OFDM) based Ultra-Wideband (UWB) receiver system is widely adapted in the industry. The analog baseband of the receiver consists of a VGA between the low pass filter and the ADC (VGA2 as shown in Fig 1.1). This VGA must attain a wide bandwidth (250MHz) with minimum noise and power consumption. In addition, due to the characteristics of the OFDM communication system, the receiver's group delay variation within the band of interest should be reduced as much as possible. Since the VGA is used before the ADC, bandwidth and linearity requirements should be comparable with those of the ADC; otherwise, the performance of the ADC will be degraded. The specifications of this VGA are shown in Table 1.1.

Style and format follow *IEEE Journal of Solid-State Circuits.*

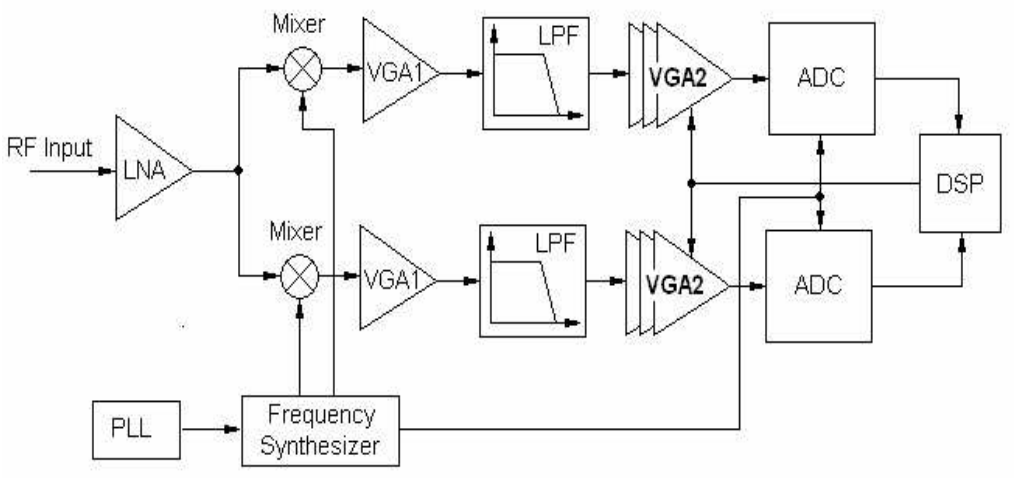


Fig 1.1 Proposed UWB receiver architecture

Table 1.1 VGA design specifications

Technology	Gain Range (dB)	Bandwidth (MHz)		Linearity IIP3 (dBm)	Noise Figure (dB)	Group Delay Variation (pS)	Power (mW)
		f_{-1dB}	f_{-3dB}				
IBM6HP 0.25um CMOS	0 ~ 42	>264	>350	>-15	<25	<200	<20

The proposed VGA uses a CMOS fully differential architecture. It includes complementary differential pairs with source degeneration as its input transconductor to convert the input voltage into current, then a programmable current mirror as its current gain stage to further amplify the current, and fixed load resistors to provide the linear current-to-voltage conversion at the output of the VGA. Due to the power efficient complementary differential pairs as the input stage, the power consumption is minimized to a very low level (<10mW) for all gain steps. The gain control scheme consists of fine

tuning (2dB/step) by changing the bias current voltage of the proposed programmable current mirror, and coarse tuning (14dB/step) by connecting/disconnecting the source degeneration resistors in the complementary differential pairs. Capacitive frequency compensation scheme is used to further extend the VGA bandwidth. The DC offset cancellation is implemented to eliminate the offset voltage and fix the DC voltage level at the output of VGA.

This thesis is organized as follows. In Chapter II, several VGA basic architectures are discussed. Since the proposed architecture is based on a programmable current mirror, DC and AC characteristics of the simple current mirror and the programmable current mirror are analyzed in Chapter III. The proposed VGA is presented in Chapter IV, and Chapter V contains the simulation and experimental results of the VGA. Finally, some conclusions are given in the last chapter.

CHAPTER II

BASIC VGA STRUCTURES

This chapter starts with an introduction of the commonly used VGA structures. The gain control schemes, the linearization techniques, and the power consumption of each structure have been discussed and their advantages and drawbacks are compared. The study suggests that a new approach must be introduced because some requirements for the UWB system, such as low power consumption and very wide bandwidth, cannot be achieved with the current structures.

II.1 VGA structures

There are several commonly used VGA structures: (1) differential pair with diode-connected loads; (2) analog multiplier; (3) differential pair with source degeneration.

The performance of each structure is studied in the following sessions.

II.1.1 Differential pair with diode-connected loads

Amplifiers based on differential pair with diode-connected loads have been used for the design of VGAs [1]-[2]. As shown in Fig 2.1, the input voltage signal is converted into current using a non-linear differential pair, and converted back into voltage using a load based on another differential pair with a smaller transconductance.

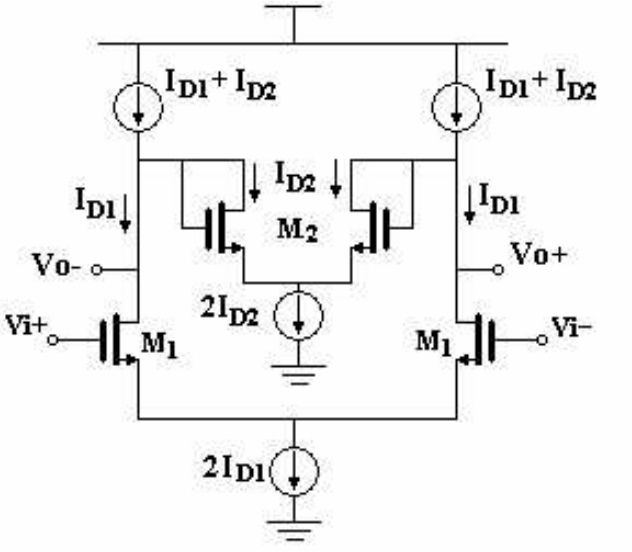


Fig 2.1 Differential pair with diode-connected loads

The DC voltage gain $A_v(0)$ of this topology is given by

$$A_V(0) = -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{\left(\frac{W}{L}\right)_1 \frac{I_{D1}}{2}}\sqrt{1-\frac{1}{4}\left(\frac{V_{in}}{V_{DSAT1}}\right)^2}}{\sqrt{\left(\frac{W}{L}\right)_2 \frac{I_{D2}}{2}}\sqrt{1-\frac{1}{4}\left(\frac{V_{out}}{V_{DSAT2}}\right)^2}} \tag{2.1}$$

where V_{DSAT1} and V_{DSAT2} are the saturation voltages ($V_{DSAT} = V_{GS} - V_{th}$) for M_1 and M_2 respectively, and $(W/L)_1$ and $(W/L)_2$ are the aspect ratios of M_1 and M_2 respectively.

If $\frac{1}{4}\left(\frac{V_{in}}{V_{DSAT1}}\right)^2$ and $\frac{1}{4}\left(\frac{V_{out}}{V_{DSAT2}}\right)^2$ <<1, from equation 2.1, yields

$$A_V(0) = -\frac{\sqrt{\left(\frac{W}{L}\right)_1 I_{D1}}}{\sqrt{\left(\frac{W}{L}\right)_2 I_{D2}}} \tag{2.2}$$

Equation 2.2 indicates that the gain can be changed by using different bias currents I_{D1} and I_{D2} for M_1 and M_2. If I_{D1} exactly matches I_{D2}, equation 2.2 is reduced to

$$A_V(0) = -\frac{\sqrt{W_1 / L_1}}{\sqrt{W_2 / L_2}} \tag{2.3}$$

Equation 2.3 shows that the voltage gain is linear and independent of the bias currents of the transistors, which also makes it insensitive to the process and the temperature variations. When M_1 and M_2 operate in the saturation region, their drain-source currents are given by

$$I_{D1} = I_{D2} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 V_{DSAT\,1}{}^2 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 V_{DSAT\,2}{}^2 \tag{2.4}$$

Combining equation 2.2 with 2.4 yields

$$A_V(0) = -\frac{V_{DSAT2}}{V_{DSAT1}} \tag{2.5}$$

Equation 2.5 indicates that large gain factors require large V_{DSAT2}, but the gain is limited by the supply voltage. Next, through the analysis on frequency response and linear range of this structure, its limitations are shown.

(1) Frequency response

The parasitic capacitance and the resistance at the output node generate the dominant pole in this structure, which determines its -3dB bandwidth (Fig 2.2).

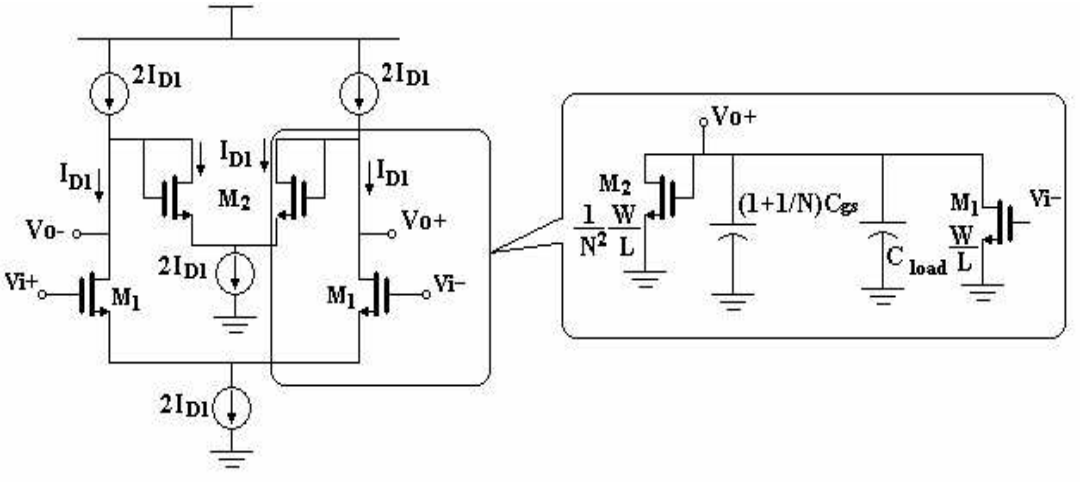


Fig 2.2 Pole location of the differential pair with diode-connected loads

For a DC voltage gain of N, the small signal gain of this structure is given by

$$A_V(s) = \frac{A_V(0)}{1+\frac{s}{\omega_P}} = -\frac{N}{1+\frac{s}{\omega_P}} \tag{2.6}$$

where $\omega_P = \dfrac{\frac{g_{m1}}{N}}{C_{gs1}(1+\frac{1}{N^2})+C_{load}} = \dfrac{g_{m1}}{C_{gs1}(N+\frac{1}{N})+C_{load}}$

Assume $C_{gs1}(N+\frac{1}{N}) >> C_{load}$, then

$$\omega_P \approx \frac{\frac{g_{m1}}{N}}{C_{gs1}(1+\frac{1}{N^2})} \tag{2.7}$$

Define "unity gain frequency" as $\omega_t = g_{m1}/C_{gs1}$, then

$$\omega_P = \frac{\omega_t}{N+\frac{1}{N}} \tag{2.8}$$

This structure is a one-pole system, so its -3dB bandwidth (f_{-3dB}) is determined by

$$f_{-3dB} = \frac{\omega_P}{2\pi} \approx \frac{\frac{g_{m1}}{N}}{2\pi C_{gs1}(1+\frac{1}{N^2})} \tag{2.9}$$

Define the gain-bandwidth-product (GBW) as the product of its DC voltage gain and -3dB frequency :

$$GBW = A_V(0) \times f_{-3dB} \approx N \times \frac{\frac{g_{m1}}{N}}{2\pi C_{gs1}(1+\frac{1}{N^2})} \approx \frac{g_{m1}}{2\pi C_{gs1}} \text{(If N >>1)} \tag{2.10}$$

Therefore, we observe that the VGA based on the differential pair with diode-connected loads has a constant gain-bandwidth-product. In other words, there is a trade-off associated with the gain and bandwidth. When gain increases, its bandwidth drops to lower frequency. For example, suppose $f_t = \frac{\omega_t}{2\pi}$ =10GHz for the above circuit. Then a plot of pole location vs. different voltage gains can be generated as in Fig 2.3, which shows the reduction of the pole frequency with the increasing gain. Compared to bandwidth requirement of this design, an almost constant bandwidth regardless of gain changing is desired. Thus, this structure is not suitable for this design.

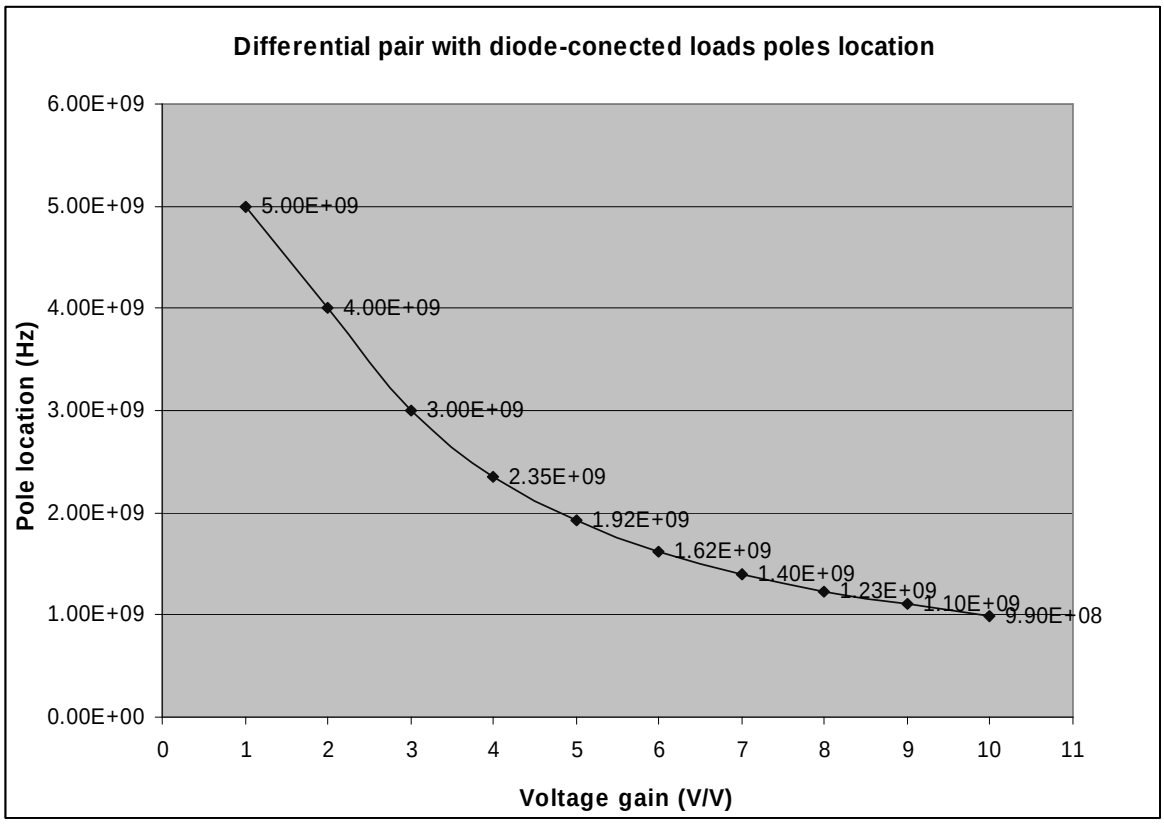


Fig 2.3 Differential pair with diode-connected loads pole location vs. voltage gain

(2) Linear range limitation

In this VGA design, the output signal is fixed to be $1V_{pp}$ with 2.5V power supply, to meet the full scale of the ADC. Thus, the suitable VGA topology for this design has to provide at least $1V_{pp}$ linear range with large variable gain range (42dB). The linear range of the differential pair with diode-connected loads is limited by the voltage headroom occupied by the gate source voltage of M_2, the saturation voltage of the NMOS transistor to generate the tail current for the differential pair, and the saturation voltage of the PMOS bias transistor to generate $2I_{D1}$. (See Fig 2.4)

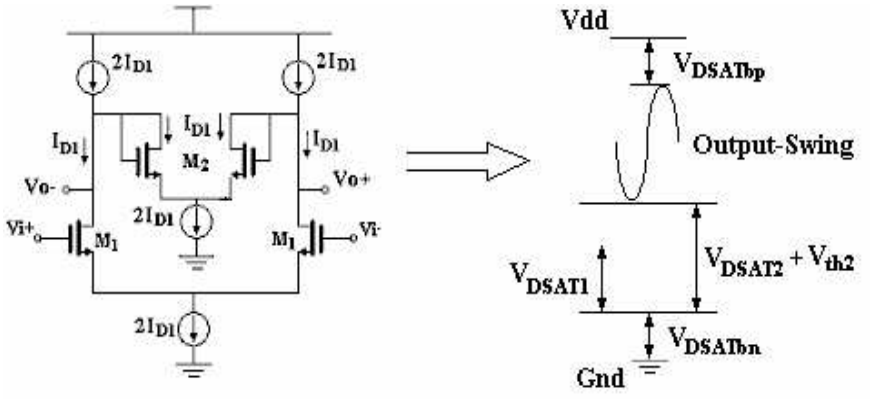


Fig 2.4 Linear range of differential pair with diode-connected loads

As shown in Fig 2.4, the linear range of differential pair with diode-connected loads is given by

$$V_{linear-range} = \frac{1}{2}\left[V_{dd} - V_{DSATbp} - (V_{DSAT2} + V_{thn}) - V_{DSATbn}\right] \tag{2.11}$$

where V_{DSATbp} is the saturation voltage of the PMOS bias transistor to generate $2I_{D1}$ current; V_{DSAT2} is the saturation voltage of M_2; V_{thn} is the threshold voltage of M_2; V_{DSATbn} is the saturation voltage of the NMOS transistor generating the tail current for M_2. If the DC voltage gain = N, with equation 2.4, we have

$$V_{DSAT2} = N \times V_{DSAT1}$$

Also if $V_{DSATbp} \sim V_{DSATbn} \sim V_{DSAT1}$, from equation 2.11, we have

$$V_{linear-range} \approx 0.5\left(V_{dd} - V_{DSAT1} - NV_{DSAT1} - V_{thn} - V_{DSAT1}\right) = 0.5\left[V_{dd} - V_{thn} - (N+2)V_{DSAT1}\right] \tag{2.12}$$

From equation 2.12, it is observed that as the DC gain increases, the linear range drops proportionally.

In this design, V_{dd} = 2.5V, $V_{thn} \sim$ 0.6V. Substitute them into equation 2.12 yields

$$V_{linear-range} \approx 0.95V - 0.5(N+2)V_{DSATn} \quad (2.13)$$

Suppose V_{DSATn} = 0.1V, to achieve 0.5V amplitude of the linear range required in this design, the gain is limited to be less than 7. Thus, in low voltage applications, the linear range of differential pair with diode-connected loads limits its maximum achievable gain range.

(3) Summary of the VGA based on differential pair with diode-connected loads

The VGA based-on differential pair with diode-connected loads has the following characteristics:

a) For small signal, its voltage gain is linear and independent of the bias currents of the transistors, which makes it insensitive to the process variations.

b) The gain-bandwidth-product of this structure is a constant, so the bandwidth trades off with the gain, which is not desired in this design.

c) Its linear range linearly decreases as gain increases, which prevents it from being used in the low voltage applications

In summary, differential pair with diode-connected loads-based VGA is not suitable for this design, because it cannot simultaneously satisfy the required specifications of large bandwidth, large variable gain range, and large linear range ($1V_{pp}$).

II.1.2 Analog multiplier

Another commonly used approach to implement a VGA is based on the analog multiplier [3]- [4]. The multiplier can be used as a linearized transconductor if one of the inputs is a DC signal as shown in Fig 2.5.

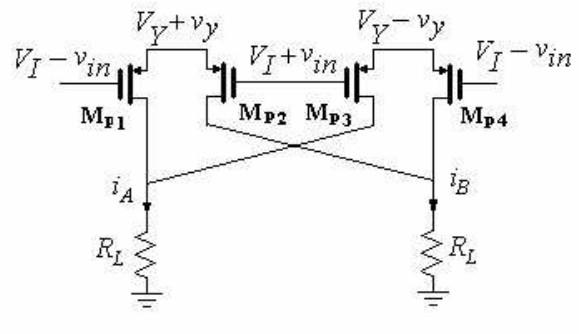


Fig 2.5 Analog multiplier used as VGA

In Fig 2.5, V_I and V_Y are the common-mode levels for the input signal v_{in} and the DC voltage v_y, respectively. Assuming that all transistors operate in saturation region, the multiplier transconductance becomes,

$$G_m = 2\mu_p C_{OX}\left(\frac{W}{L}\right)v_y \tag{2.14}$$

Neglecting the second order effects and the transistors mismatches, the transconductance of the multiplier is linear. The DC voltage gain of a multiplier and load resistor is given by

$$A_V(0) = \left(2\mu_n C_{OX}(\frac{W}{L})v_y\right)R_L \tag{2.15}$$

Thus the voltage gain can be varied by changing the control voltage level v_y. There is flexibility in controlling the gain because the control voltage is an analog signal.

Next the analysis on the linear range and the power consumption of multiplier will be given to show its advantages and drawbacks.

(1) Linear range

The linear range of the multiplier-based VGA depends on the control voltage level v_y. Hence, when the DC voltage gain increases, the linear range of this structure is reduced linearly. It can be justified as follows. The load for the multiplier can be a current mirror (Fig 2.6) [3].

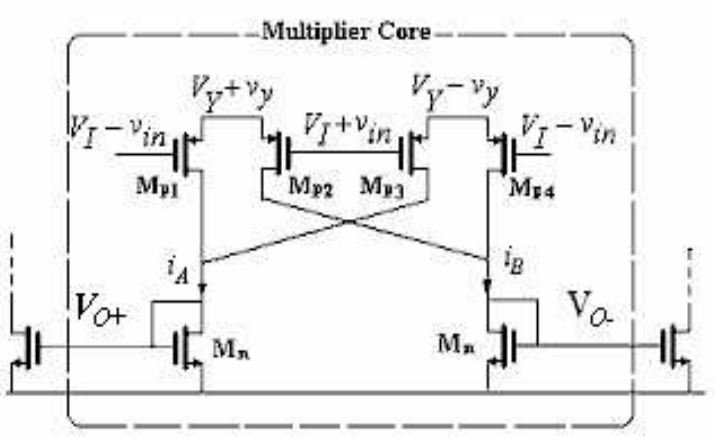


Fig 2.6 Multiplier with current mirror load [3]

The linear range of this multiplier is given by

$$V_{linear-range} = \frac{1}{2}\left(V_{dd} - V_{DSATbp} - V_{DSATp} - V_{DSATn} - V_{thn}\right) \tag{2.16}$$

where V_{DSATbp} is the saturation voltage of the PMOS bias transistor; V_{DSATp} is the saturation voltage of the PMOS drivers M_{pi}, and V_{DSATn} is the overdrive voltage of the NMOS transistor M_n.

Because $V_{DSATp} = V_Y + v_y - V_I$, so the output voltage swing is given by

$$V_{linear-range} = \frac{1}{2}\left(V_{dd} - V_{DSATbp} - \left(V_Y + v_y - V_I\right) - V_{DSATn} - V_{thn}\right) \tag{2.17}$$

Also, from equation 2.16 $\Rightarrow v_y = \dfrac{A_V(0)}{2\mu_n C_{OX}\dfrac{W}{L}R_L}$

Substitute the above result into equation 2.16, we have

$$V_{linear-range} = \frac{1}{2}\left(V_{dd} - V_{DSATbp} - V_Y + V_I - V_{DSATn} - V_{thn} - \frac{A_V(0)}{2\mu_n C_{OX}\dfrac{W}{L}R_L}\right) \tag{2.18}$$

Equation 2.18 indicates that, as $A_V(0)$ increases, the linear range drops proportionally. In other words, for large variable gain range, the linear range of the multiplier-based VGA is limited.

(2) Power consumption

In this design, low power consumption is a must. However, it will be shown that the multiplier-based VGA is not power efficient. Referring to Fig 2.5, the multiplier is equivalent to the cross-coupled outputs of two differential pairs M_{P1} and M_{P2}, M_{P3} and M_{P4} as shown in Fig 2.7.

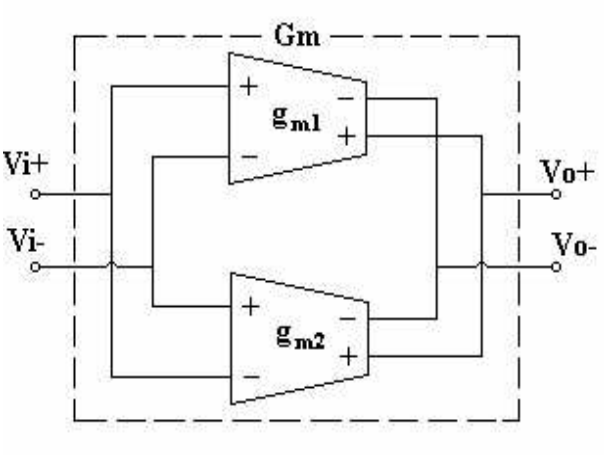


Fig 2.7 Block diagram of cross-coupled transconductors multiplier

The overall transconductance is given by

$$G_{m,eff} = g_{mp1} - g_{mp2} = 2\mu_p C_{OX} \frac{W}{L} v_y \tag{2.19}$$

$$g_{mp1} = \mu_p C_{OX} (\frac{W}{L})(V_Y + v_y - V_I); \quad g_{mp2} = \mu_p C_{OX} (\frac{W}{L})(V_Y - v_y - V_I) \tag{2.20}$$

where g_{mp1} and g_{mp2} are the transconductance of the differential pair consisting M_{P1} and M_{P2}, and the one consisting of M_{P3} and M_{P4} respectively.

By varying v_y , g_{mp1} and g_{mp2} are changed in the opposite directions by the same amount, and the effective transconductance $G_{m,eff}$ will be doubled by that amount. So, the tuning range of the transconductance is large. However, this scheme is not power-efficient. This is because, in low gain cases, v_y is small, g_{mp1} and g_{mp2} are quite close, and only a small portion of g_{mp1} is delivered to the output while most of it is cancelled out by g_{mp2}. Thus a lot of power is wasted in this case. For the high gain cases, v_y is

large, g_{mp1} is much larger than g_{mp2}, but still only part of g_{mp1} is delivered to the output. As a result, the multiplier-based VGA is not suitable for low power applications.

(3) Summary of analog-multiplier-based VGA

In summary, the multiplier-based VGA has good linearity and large gain tuning range, but it is not power efficient because the effective transconductance $G_{m,eff}$ is generated by the subtraction between g_{mp1} and g_{mp2}. And hence, it is not suitable for low-power VGA design.

II.1.3 Differential pair with source degeneration

Another commonly used VGA topology is the differential pair with source degeneration [5]- [6], as shown in Fig 2.8. It will be shown that good linearity can be achieved in this structure with large source degeneration factors; but the transconductance is attenuated a lot at the same time.

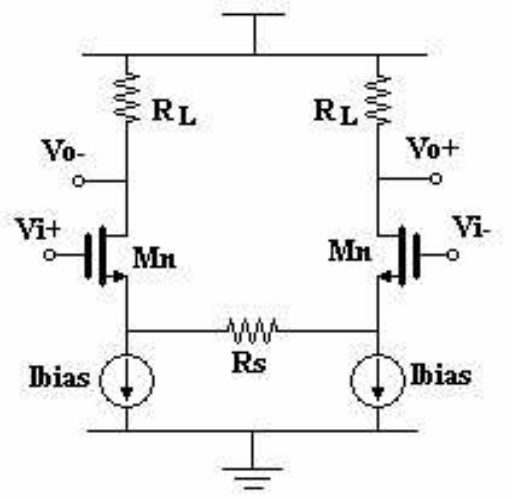


Fig 2.8 Differential pair with source degeneration

The transconductance of the differential pair with source degeneration is determined by

$$Gm = \frac{g_m}{1 + \frac{g_m R_S}{2}} \tag{2.21}$$

where R_s is the source degeneration resistor, and $\frac{g_m R_S}{2}$ is the source degeneration factor.

If the source degeneration factor ($\frac{g_m R_S}{2}$) >>1, equation 2.21 yields $G_m \approx \frac{2}{R_S}$. Under this condition, the transconductance of this configuration is simply determined by the source degeneration resistor. By changing the value of R_s, the amplifier gain can be tuned. Compared to the transconductance of simple differential pair, effective G_m of differential pairs with source degeneration is only 1/(N+1) times that of the simple differential pair. This motivates us to find an approach to boost effective transconductance of differential pairs with source degeneration.

II.1.4 Complementary differential pairs with source degeneration

To boost the effective transconductance of differential pairs with source degeneration while still achieving the similar linearity level, the complementary differential pair with source degeneration scheme can be used [7] (see Fig 2.9). In this structure, the drain of a PMOS differential pair and a NMOS differential pair are connected together such that the current converted by each differential pair are delivered

together to the next stage. In each differential pair, source degeneration resistors are used to improve their linearity.

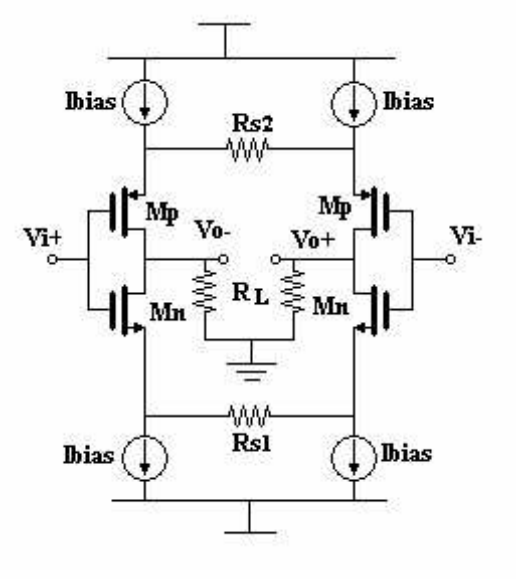


Fig 2.9 Complementary differential pairs with source degeneration

The effective transconductance of this structure is given by

$$G_m = \frac{g_{mn}}{1+\frac{g_{mn}R_{s1}}{2}} + \frac{g_{mp}}{1+\frac{g_{mp}R_{s2}}{2}} \tag{2.22}$$

A special case of it is to set $g_{mn}R_{S1} = g_{mp}R_{S2}$, then equation 2.21 becomes

$$G_m = \frac{g_{mn} + g_{mp}}{1+\frac{g_{mn}R_{s1}}{2}} \tag{2.23}$$

Both differential pairs are biased with the same DC current. Compared with the single differential pair case, the power consumption is the same for both topologies. But the complementary configuration has a larger effective transconductance, because the

effective transconductance is the summation of the transconductances of NMOS and PMOS transconductors. It can be shown that with the complementary differential pairs, the effective transconductance can be boosted by 60% compared to that of the single differential pair [7].

(1) Linear range

The linear range of complementary differential pairs with source degeneration is limited by the V_{dsat} of M_p and $M_{n,}$ and those of their bias transistors M_{bp} and M_{bn} altogether. So the linear range for it is given by

$$V_{OUTPUT-SWING} = \frac{1}{2}\left(V_{dd} - V_{DSATbp} - V_{DSATp} - V_{DSATn} - V_{DSATbn}\right) \quad (2.24)$$

Notice that the DC voltage gain variation is achieved by changing the source degeneration resistor, which will not affect the terms in equation 2.24. Therefore, regardless of the change in the voltage gain, the linear range of complementary differential pairs with source degeneration is fixed. On comparison with the differential pair with diode-connected loads, where the linear range is reduced linearly if gain is increasing, it can be justified that, in low voltage applications, the complementary differential pairs with source degeneration structure can achieve larger variable gain range than that of the differential pair with diode-connected loads structure.

(2) Summary of VGA based on complementary differential pairs with source degeneration

Complementary differential pairs with source degeneration have better power efficiency than that of differential pair with source degeneration. The former boosts the transconductance while consuming the same power and has similar linearity performance as that of the latter. The linear range of the complementary differential pairs with source degeneration is independent of gain variations, which enables it to obtain large variable gain ranges under low supply voltage.

II.2 Comparison of the commonly used VGA structures

The design requirements impose challenges on low power consumption, very large bandwidth, large variable gain range, and very small group delay variation.

A differential pair can be linearized with diode-connected loads. But in large gain cases, the linear range and bandwidth are limited.

A multiplier has good linearity and flexible tunablity. However, due to the subtraction of two transconductances in this type of multiplier, the power is wasted when generating total transconductance. So for low power applications, a multiplier may not be a suitable candidate.

The linearity of the differential pair with source degeneration is dependent on the g_mR_S and V_{DSAT}. By increasing these values, its linear range becomes comparable with the multiplier's linearity. But at the same time, the effective transconductance is attenuated dramatically.

Currently available VGA structures cannot meet all these requirements. A new approach has to be proposed, in which, the following aspects should be emphasized:

(1) An approach with better power efficiency while maintaining enough linearity is needed.

(2) To obtain large bandwidth, current amplification is preferred to voltage amplification due to its low impedance internal nodes.

Starting with differential pairs with source degeneration, a complementary differential pairs with source degeneration configuration is proposed. Its effective transconductance can be boosted up by 60% as compared to a single NMOS differential pairs with source degeneration while maintaining the same power consumption. It also has large variable gain range and large linear range. Therefore it will be a suitable choice for this design.

CHAPTER III

PROGRAMMABLE CURRENT MIRROR

In this chapter, the simple current mirror is briefly reviewed. Its AC response and non-idealities are studied. Based on the design requirements, a programmable current mirror is proposed to improve frequency response and programmability. A performance comparison between the simple current mirror and the proposed programmable current mirror is given.

III.1 Review of simple current mirror

Because of its low-impedance internal node, the current mirror is used in many high-frequency VGA designs [1].

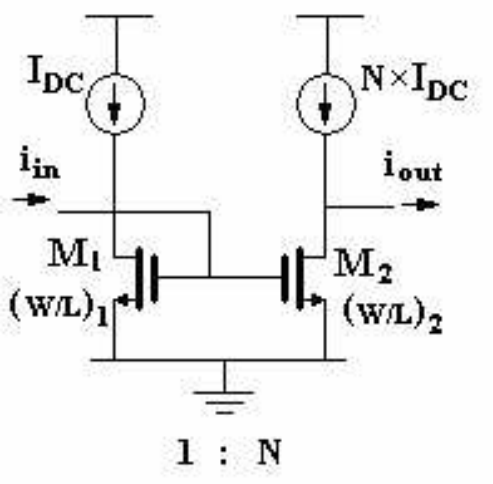


Fig 3.1 Simple current mirror

Neglecting the mismatch and the channel-length modulation effects, the DC current gain for the simple current mirror shown in Fig 3.1 is given by:

$$\frac{i_{out}}{i_{in}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \tag{3.1}$$

In the simple current mirror, the parasitic capacitance and the resistance at the diode-connected node generate an internal pole. It has been shown in [3] that the short circuit transfer function of the simple current mirror in Fig 3.1(a) is given by:

$$\frac{i_{out}}{i_{in}} = -\frac{\frac{g_{m2}}{(N+1)C_{gs}}}{s + \frac{g_{m2}}{(N+1)C_{gs}}} \times N \tag{3.2}$$

where N is the DC current gain, and C_{gs} is the gate-source capacitance of the input transistor.

The pole at the diode-connected node is given by

$$\omega_P = \frac{g_{m2}}{(N+1)C_{gs}} \tag{3.3}$$

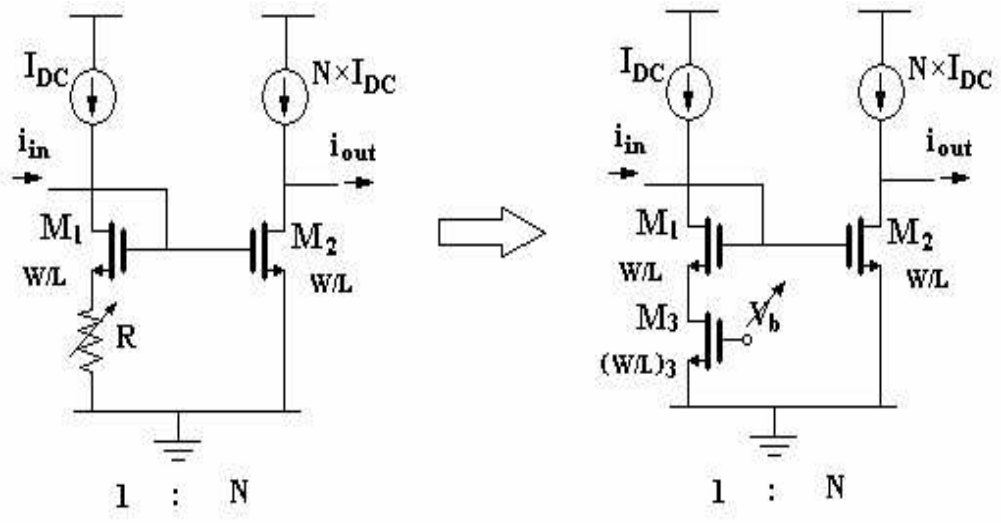
From equation 3.3, with a DC current gain of N, the gate dimension of the output transistor in simple current mirror is N times larger than its input transistor, so is its parasitic capacitance. This implies that the pole location will drop to a lower frequency. While the current gain still can be changed with an alternate method, if we can find a way with fixed input/output transistor dimensions, the frequency response of the current mirror can be improved.

III.2 Proposed programmable current mirror

As just mentioned, we can try to fix the dimensions of the input/output transistor in the current mirror but change the current gain through alternate means. In the simple current mirror, the DC current gain is given by

$$\frac{i_{out}}{i_{in}} = \frac{\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{th})^2}{\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{th})^2} \tag{3.4}$$

From equation 3.4, if $\left(\frac{W}{L}\right)_2$ and $\left(\frac{W}{L}\right)_1$ are fixed, changing V_{GS2} or V_{GS1} can vary the current gain too. One solution to vary V_{GS} is to insert a variable resistor between the source and the ground of the input transistor; V_{GS1} is adjusted by varying the resistor. Fig 3.2 shows the proposed programmable current mirror.



(a) Simple resistor model (b) Linear region transistor replaces resistor

Fig 3.2 Programmable current mirror

As illustrated in Fig 3.2 (a), M_1 and M_2 are identical, and the DC current gain of the programmable current mirror is given by

$$\frac{i_{out}}{i_{in}} = \frac{(V_{GS2} - V_{th})^2}{(V_{GS2} - R \times I_{DC} - V_{th})^2} \tag{3.5}$$

For the implementation of a variable resistor, a MOS transistor operating in triode region can be used. Its resistance is then linearly controlled by its gate-source bias voltage. How to generate V_b to control the current gain of the programmable current mirror accurately will be discussed next.

The proposed bias circuit is shown in Fig 3.3. By rearranging equation 3.5, we obtain

$$\frac{i_{out}}{i_{in}} = \frac{1}{\left(1 - \frac{R \times I_{DC}}{V_{GS2} - V_{th}}\right)^2} \tag{3.6}$$

If $R \times I_{DC} \propto (V_{GS2} - V_{th})$, then equation 3.6 indicates that the current gain can be accurately controlled. This inspires the circuit shown in Fig 3.3. The diode-connected transistor M_b is used to convert the DC reference current, I_{DC}, into a bias voltage, V_b, to bias M_3. It will be shown that the current gain is determined by the aspect ratios of M_1 (M_2), M_3, M_b, and the ratio between the I_{ref} and I_{DC}.

From equation 3.6, we have

$$\Rightarrow \frac{i_{out}}{i_{in}} = \frac{1}{\left(1 - \frac{V_{DS3}}{V_{GS2} - V_{th}}\right)^2} \tag{3.7}$$

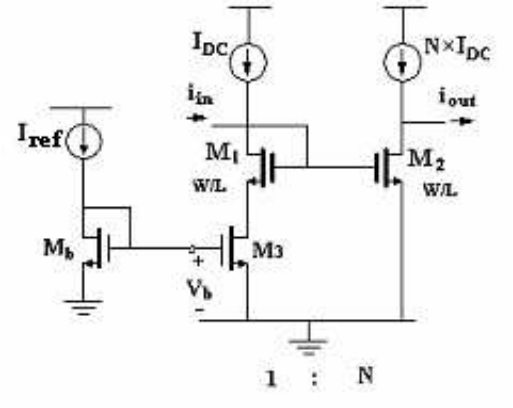


Fig 3.3 V_b generation for programmable current mirror

If M_3 operates in the linear region, then $I_{D3} \approx \beta_3 (V_{GS3} - V_{th}) V_{DS3}$. By rearranging this, we obtain,

$$V_{DS3} \approx \frac{I_{D3}}{\beta_3 (V_{GS3} - V_{th})} \tag{3.8}$$

M_b operates in the saturation region yields

$$I_{ref} = I_{D3} \approx \frac{1}{2} \beta_b (V_{GS3} - V_{th})^2 \tag{3.9}$$

where $\beta_i = \mu_n C_{OX} \left(\frac{W}{L} \right)_i$.

If we substitute equations 3.8 and 3.9 into equation 3.7, we have

$$\frac{i_{out}}{i_{in}} = \frac{1}{\left(1 - \frac{\beta_b (V_{GS3} - V_{th})^2}{2\beta_3 (V_{GS3} - V_{th})(V_{GS2} - V_{th})} \right)^2} = \frac{1}{\left(1 - \frac{\beta_b V_{DSAT3}}{2\beta_3 V_{DSAT2}} \right)^2} \tag{3.10}$$

So, if $\beta_b = 2\beta_3$, then

$$\frac{i_{Out}}{i_{In}} = \frac{1}{\left(1 - V_{DSAT3} / V_{DSAT2}\right)^2} \tag{3.11}$$

Equation 3.11, based on the special case of $I_{ref} = I_{D3}$, indicates that V_{DSAT3} and V_{DSAT2} can be related by the dimensions and bias currents of the transistors in the current mirror, and therefore the current gain can be related to them as well. In general cases, we have $I_{ref} = K \times I_{D3}$ (where K is a constant). The expression of current gain as a function of the aspect ratios of M_1 (M_2), M_3, M_b, and the ratio between the I_{ref} and I_{DC} is obtained in Appendix A; the result is as follows:

$$\frac{i_{out}}{i_{in}} = \left(\sqrt{NK} + 1 - \sqrt{NK - M}\right)^2 \tag{3.12}$$

where $M = \frac{(W/L)_1}{(W/L)_3}$ $\quad N = \frac{(W/L)_1}{(W/L)_b}$ $\quad K = \frac{I_{ref}}{I_{DC}}$

First, notice that in equation 3.12, the product of NK has to be larger than M. If NK = M, then, M_3 will operate in the saturation region. Even though the drain current equation for M_3 is not valid any more, equation 3.12 is still valid and reduces into equation 3.13,

$$\frac{i_{out}}{i_{in}} = \left(\sqrt{M} + 1\right)^2 = \left(\sqrt{NK} + 1\right)^2 \tag{3.13}$$

However, if M_3 operates in the saturation region, its output resistance is almost constant and only varies subtly due to the channel length modulation effects. Therefore, it is not suitable as a variable resistor.

Equation 3.12 also shows that by increasing M, or decreasing K or N, the current gain can be increased. To minimize the power consumption for the bias control voltage,

we should avoid using large K to keep I_{ref} at a minimum. Also, according to the real implementation of the programmable current mirror, M cannot be varied, which leaves K and N to be varied. Changing K to obtain different current gain ratios unavoidably requires a large range of K variation, as it is square-root proportional to the current gain, which results in wasting power at large K cases. However, if variable current gain is obtained by varying N, it is only needed to implement a bank of diode-connected transistors with different dimensions and bias with an optimal current ($I_{ref} = K_{optimal} \times I_{D3}$). By connecting or disconnecting them to the gate of M_3, different gain can be obtained. Thus, restricted by the low power requirement, this approach is adapted to implement the programmable current mirror. Furthermore, as K is fixed, the variables left in equation 3.12 are M and N. As they are both related to the dimensions of M_1, their ratio, which is the aspect ratio between M_b and M_3, can be a variable to determine the current gain.

To obtain 14dB of variable gain range, and include the consideration of the trade-off mentioned previously, K = 2 and M = 2 are selected. With this combination, the maximum gain is approximately 14 dB for N = 1. The simulated dimensions of the transistors are listed in Table 3.1. W_b is the total equivalent transistor width of the bias control circuit, $W_b = \sum_{i=1}^{N} W_{bi}$. Therefore, the individual transistor width can be calculated as shown in Table 3.1. The corresponding bias control circuit with programmable current mirror is shown in Fig 3.4.

Table 3.1 Dimensions of the bias circuits

(L = 0.24μm)

N	1.01	1.05	1.2	1.4	1.8	3	5.6
Current Gain	14dB	12dB	10dB	8dB	6dB	4dB	2dB
W_b	23.6	21.6	16.8	12	7.2	2.4	0.72
	M_{b1}	M_{b2}	M_{b3}	M_{b4}	M_{b5}	M_{b6}	M_{b7}
W	2μm	4.8 μm	4.8 μm	4.8 μm	4.8 μm	1.68 μm	0.72 μm

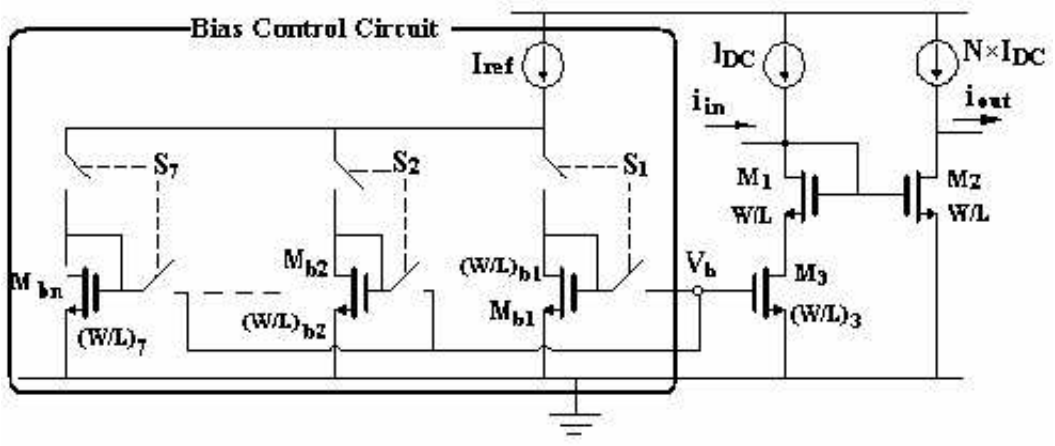


Fig 3.4 Dimensions of the bias circuits bias transistors to generate seven gain steps for programmable current mirror

III.2.1 AC response of programmable current mirror

When the programmable current mirror operates at a low frequency, M_3 is equivalent to a variable resistor R and its parasitic capacitance can be ignored. M_1, connected to the variable resistor R, converts the input current, i_{in}, into voltage. This

voltage at node C is then converted back to current (i_{out}) through M_2. As shown in Fig 3.5, the DC current gain is given by

$$\frac{i_{out}}{i_{in}} = g_{m2}\left(R + \frac{1}{g_{m1}}\right) \tag{3.14}$$

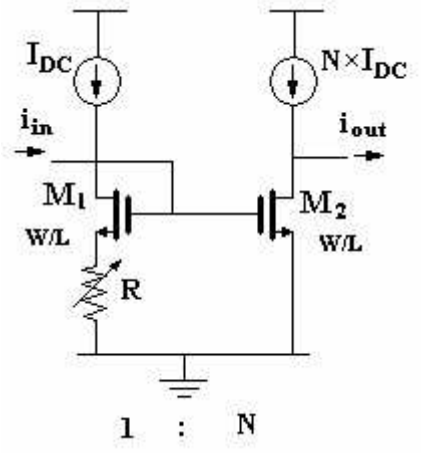


Fig 3.5 Programmable current mirror low frequency model

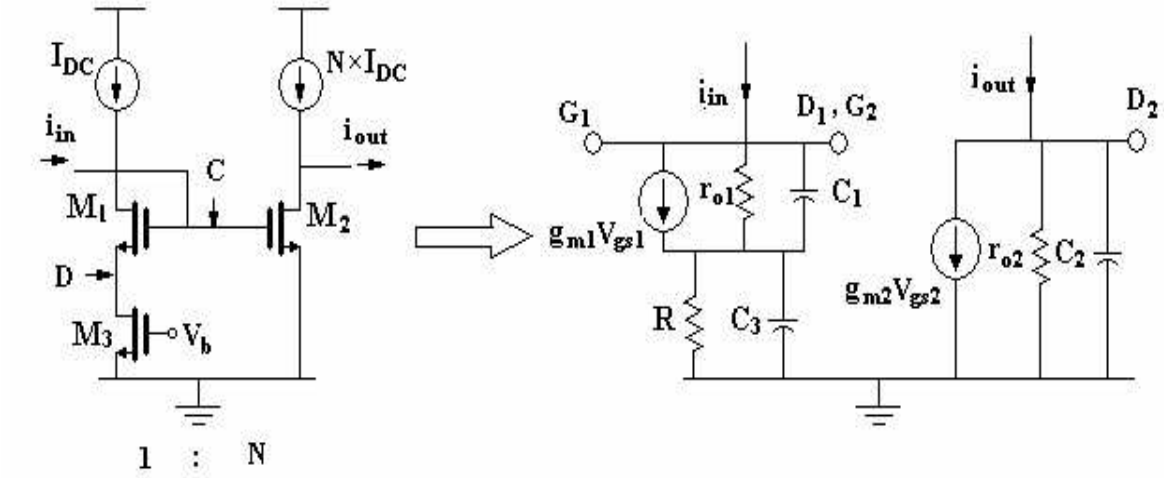
At high frequencies, the parasitic capacitance at node C and D must be taken into account (Fig 3.6). Assuming that the gate-source capacitance of M_1 and M_2 are equal, the current gain computation yields

$$\frac{i_{out}}{i_{in}} \cong \frac{g_{m1}\left(R+\frac{1}{g_{m1}}\right)(C_1+C_3)}{C_1(2C_1+C_3)} \frac{s+\frac{g_{m1}+\frac{1}{R}}{C_1+C_3}}{\left(s+\frac{g_{m1}}{2C_1}\right)\left(s+\frac{1}{R(C_1+0.5C_3)}\right)}$$

When DC current gain = N $\Rightarrow$ $R = \dfrac{N-1}{g_{m1}}$

$$\Rightarrow \frac{i_{out}}{i_{in}} \cong \frac{N(C_1+C_3)}{C_1(2C_1+C_3)} \frac{s+\dfrac{\left(1+\dfrac{1}{N-1}\right)g_{m1}}{C_1+C_3}}{\left(s+\dfrac{g_{m1}}{2C_1}\right)\left(s+\dfrac{g_{m1}}{(N-1)(C_1+0.5C_3)}\right)}$$

$$\Rightarrow \frac{i_{out}}{i_{in}} \cong \frac{N(C_1+C_3)}{C_1(2C_1+C_3)} \frac{s+\dfrac{\left(1+\dfrac{1}{N-1}\right)g_{m1}}{C_1+C_3}}{\left(s+\dfrac{g_{m1}}{2C_1}\right)\left(s+\dfrac{g_{m1}}{(N-1)(C_1+0.5C_3)}\right)} \qquad (3.15)$$



(a) Nodes C and D (b) Small signal model

Fig 3.6 Programmable current mirror high frequency operation model

Equation 3.15 indicates that there are two poles and one zero in the programmable current mirror, which are:

$$\omega_{P1} = \frac{g_{m1}}{2C_1}, \quad \omega_{P2} = \frac{g_{m1}}{(N-1)(C_1 + 0.5C_3)}, \quad \omega_Z = \frac{g_{m1}\left(1 + \frac{1}{N-1}\right)}{C_1 + C_3} \tag{3.16}$$

The dominant pole in the programmable current mirror is

$$\text{Dominant Pole}: \omega_{P2} = \frac{g_{m1}}{(N-1)(C_1 + 0.5C_3)} \tag{3.17}$$

The dominant pole frequency of the programmable current mirror with that of the simple current mirror is compared as shown in Table 3.3.

Table 3.2 Dominant poles comparison between programmable and simple current mirror

	Simple Current Mirror	Programmable Current Mirror
Dominant pole	$\frac{g_{m1}}{(N+1)C_1}$	$\frac{g_{m1}}{(N+1)C_1 + 0.5C_3(N-1) - 2C_1}$

From Table 3.3, if $0.5C_3(N-1) - 2C_1 < 0$, then the dominant pole of the programmable current mirror is at higher frequency than that of the simple current mirror. Further, C_1 (the gate-source parasitic capacitance of M_1) and C_3 (the drain-bulk capacitance combined with the drain source parasitic capacitance of M_3) are also comparable. Thus, from the expression of the non-dominant pole and zero of the programmable current mirror, when N>>1,

$$\omega_Z \approx \frac{g_{m1}}{C_1 + C_3} \approx \frac{g_{m1}}{2C_1} = \omega_{P1} (\text{N>>1}) \tag{3.18}$$

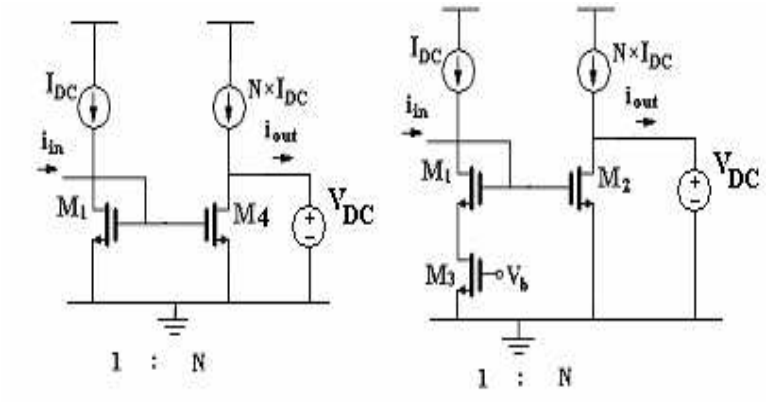
Therefore, at large gain cases in which N>>1, the zero of the programmable current mirror will cancel out its non-dominant pole and hence its -3dB frequency will be only determined by its dominant pole frequency.

Overall, to achieve an improved frequency response from the programmable current mirror when compared to the simple current mirror, we have to guarantee that at DC current gain of N,

$$0.5C_3(N-1) - 2C_1 < 0 \tag{3.19}$$

The result from equation 3.19 is very critical, since at high gain cases, it can be used to determine whether the programmable current mirror has improved the frequency response when compared to the simple current mirror and determine how much improvement we can get.

Using the Cadence simulator, a comparison of f_{-3dB} of the programmable current mirror vs. that of the simple current mirror under different current gain levels can be obtained. The simulation setup is shown in Fig. 3.7; transistors dimensions are given in Table 3.3.



(a) Simple current mirror (b) programmable current mirror

Fig 3.7 Setup for testing f_{-3dB} of the current mirror

In Fig 3.7, the same DC bias current I_{DC} is provided for both current mirrors. In the simple current mirror, for different current gain N, M_4 is split into N fingers each with the same dimension as M_1. Further, a DC voltage is provided at the output to fix the drain-source voltage of M_4 to be the same as that of M_1. This will avoid the current mismatch caused by the channel-length modulation effects. For the case of the programmable current mirror, the bias voltage (V_b) is changed to obtain different current gains.

Table 3.3 Current mirror's f_{-3dB} testing setup

	M_1	M_2	M_3	M_4
W/L (μm)	24/0.24	24/0.24	24/0.24	24×N/0.24
I_{DC} (μA)	i_{in} (μA)	N		
100	25	2, 3, …, 10		

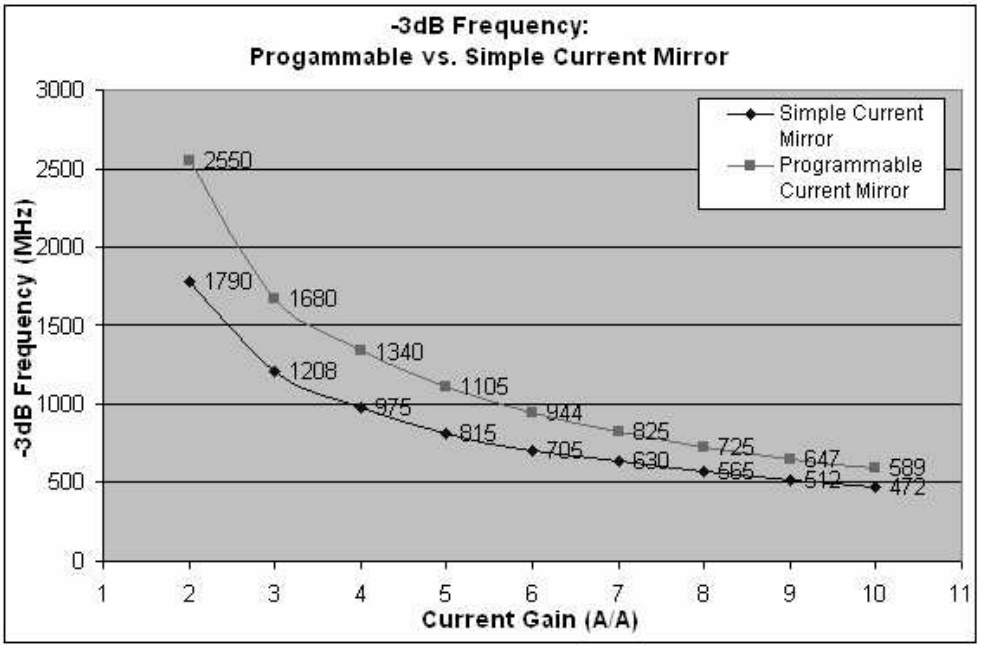


Fig 3.8 f_{-3dB} of the simple current mirror vs. that of the programmable current mirror

According to Fig 3.8, with the programmable current mirror, we can improve the f_{-3dB} in a certain current gain range, but this improvement is reduced as the gain increases, and eventually at very high current gain cases, in which equation 3.19 is not satisfied any more, or say, $0.5C_3(N-1)-2C_1$ is larger than zero, the programmable current mirror will have even smaller f_{-3dB} and worse frequency response than those of the simple current mirror.

III.2.2 Programmability of the programmable current mirror

Another advantage of using the programmable current mirror is its good programmability. To change current gain in the simple current mirror, we need several transistors with different dimensions connected to the input transistor with switches.

This circuit is shown in Fig 3.9. There are some effects on the circuit's performance caused by these connections. The on-resistance of the switches combined with the parasitic capacitance at the current mirror internal node (dominated by the gate-source parasitic capacitance of the transistors) generates a RC network. This network is along the signal path of the current mirror, and thus the high-frequency signal will be attenuated and delayed by the RC time constant from this RC network.

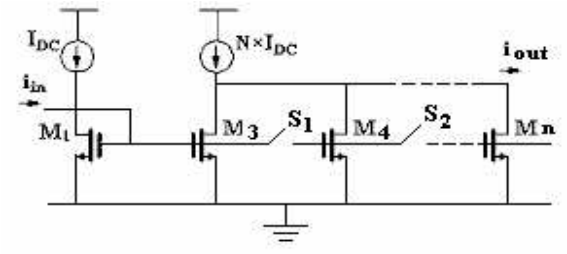


Fig 3.9 Simple current mirror to implement different current gain

For the case of the programmable current mirror, the gain control is achieved by the bias control circuit. Even though there are switches in this bias circuit, none of them are in the signal path, implying that there will be no additional time constants, as in the simple current mirror. So, more gain steps with larger overall variable gain ranges can be implemented in the programmable current mirror than that of the simple current mirror.

III.3 Conclusions

A comparison between the simple current mirror and the proposed programmable current mirror is listed in Table 3.4.

Table 3.4 Current mirror comparison

	simple current mirror	programmable current mirror
R_{out}	r_{ds2}	r_{ds2}
Frequency response	$\omega_P = \frac{g_{m2}}{(N+1)C_{gs}}$	$\omega_{P1} = \frac{g_{m1}}{2C_1}, \omega_{P2} = \frac{1}{R(C_1 + 0.5C_3)}, \omega_Z = \frac{g_{m_1} + \frac{1}{R}}{C_1 + C_3}$ It is justified in section III.2.1 that It has improved frequency response than simple current mirror if $0.5C_3(N-1) - 2C_1 < 0$ is satisfied.
Programmability	Poor (as explained in section 3.2(2))	Good (as explained in section 3.2(2))

The proposed programmable current mirror avoids changing the output transistor's dimension to change current gain, which improves frequency response and provides larger bandwidth than that of simple current mirror in a certain gain range as long as equation 3.19 is valid. Also, as explained in 3.2(2), it has better programmability than that of the simple current mirror. The current gain variation in the programmable current mirror is obtained by changing the bias voltage, V_b, for M_3 in Fig 3.6. With the proposed bias control circuit, the current gain of the programmable current mirror becomes a function of the aspect ratios of M_1, M_3, M_{bi}, and their bias current ratio. By properly selecting these parameters, a large current gain tuning range can be achieved.

CHAPTER IV

DESIGN CONSIDERATIONS OF THE PROPOSED VGA

In this chapter, VGA design challenges are summarized, and the motivations for the new approach are addressed. Following an overview of the system-level considerations, the individual building blocks of the proposed VGA are introduced. Each building block is explained and analyzed. Finally, detailed calculations for the proposed VGA are given in the Appendix B.

IV.1 VGA design challenges and motivations

In this design, we want to achieve large bandwidth, large variable gain range with low power consumption and small group delay variation. Also, the VGA should maintain good linearity and low noise performance for all gain steps; its design specifications are given in Table 4.1.

Table 4.1 VGA specifications

Technology	Gain range (dB)	Bandwidth (MHz)		Linearity IIP3 (dBm)	Noise figure (dB)	Group delay variation (pS)	Power (mW)
		f_{-1dB}	f_{-3dB}				
IBM 0.25um CMOS	0 ~ 42	>264	>350	-15	<25	<200	<20

IV.2 System-level overview of the proposed VGA

IV.2.1 System-level design of the proposed VGA

From the system-level point of view, this design can be divided into three categories:

1) Gain amplification schemes

2) Variable gain control schemes

3) Other auxiliary schemes

For the first category, the 42dB gain range is distributed into two amplification stages: first with a transconductance stage to convert the input voltage signal into current, and then use a current mirror to further amplify the current. With fixed resistors at the output, the current is converted back into voltage. With the combination of the two gain stages, a large variable gain range is obtained.

For the variable-gain-control scheme, coarse tuning at the transconductance stage and fine tuning at the current mirror stage are implemented respectively.

Besides the previously mentioned two categories in the VGA, frequency compensation and DC offset cancellation are implemented as well. These functions will be explained in the following sections.

Overall, the system-level architecture of the proposed VGA is shown in Fig 4.1, and an explanation of each block follows.

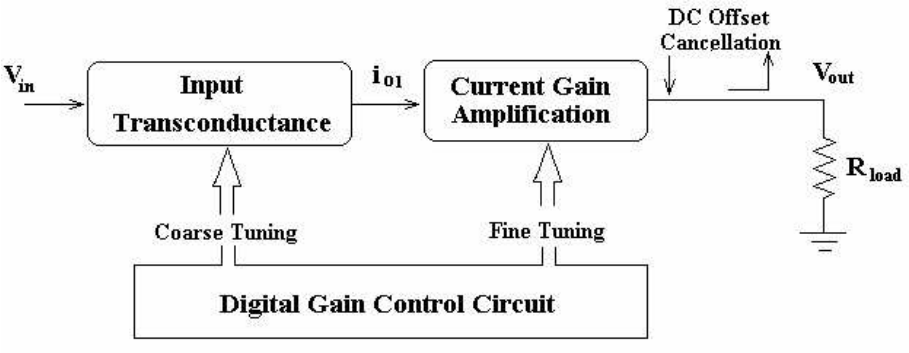


Fig 4.1 System-level architecture of the proposed VGA

IV.2.2 Introduction of the building blocks of the proposed VGA

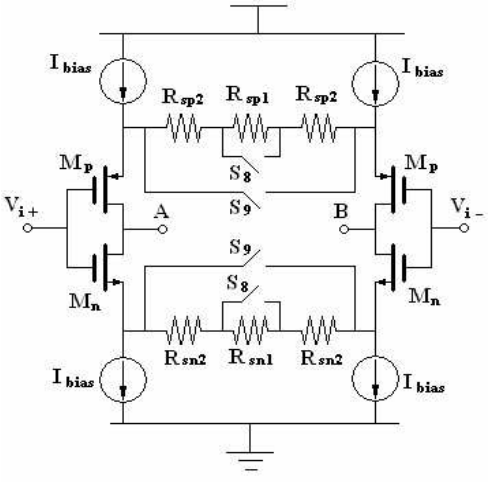
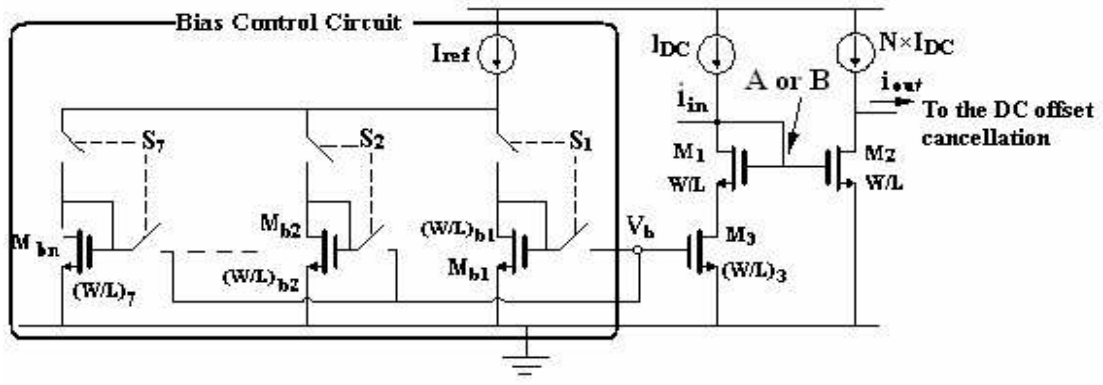


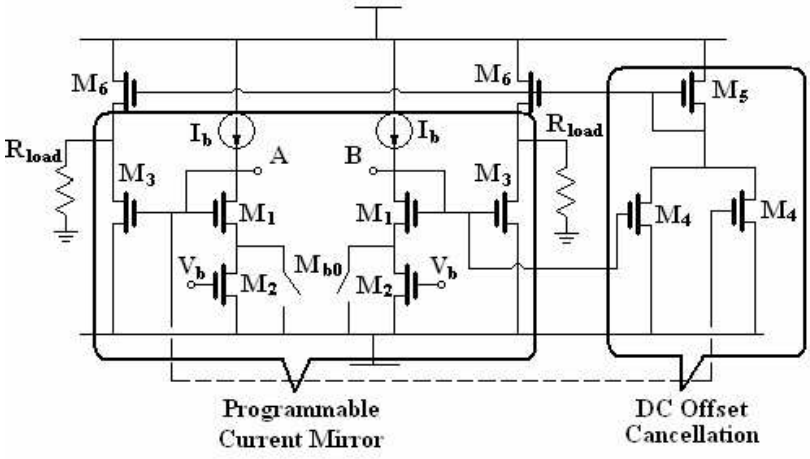
Fig 4.2 Complementary differential pairs with source degeneration

Based on the system-level VGA structure discussed previously, the building blocks can be constructed to meet the system needs. First, a power-efficient transconductor is required as the input stage. From the comparison conducted in Chapter II, the complementary differential pairs with source degeneration boosts

transconductance while consumes the same power as the simple differential pair with source degeneration. Thus, it is used as the input stage (Fig 4.2). As for the current amplification stage, according to the studies in Chapter III, the programmable current mirror shows the good frequency response and gain programmability. Thus, it is used as the current amplification stage (Fig 4.3).



(a) Programmable current mirror



(b) DC offset cancellation

Fig 4.3 Programmable current mirror and DC offset cancellation

Nodes A and B in Fig 4.2and in Fig 4.3 are the same nodes.

Secondly, for the gain-control scheme, the coarse tuning is implemented by changing the source degeneration resistor in the input stage (Fig 4.2). Fine tuning is obtained by changing the dimensions of the transistors in the bias control circuit of the programmable current mirror (Fig 4.3). Both gain varying schemes are then programmed with digital gain control.

For the auxiliary circuits, a capacitive frequency-compensation scheme is used to further extend the bandwidth of the VGA (Fig 4.4), and a DC offset cancellation output stage is used to fix the DC voltage level, regardless of the offset introduced by mismatch or process variations (Fig 4.3).

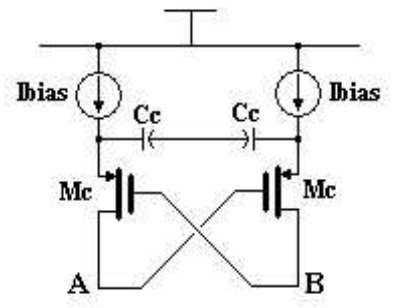


Fig 4.4 Capacitive frequency compensation (A and B are the same in Fig 4.3)

Overall, the building blocks in the proposed VGA are shown in Fig 4.5.

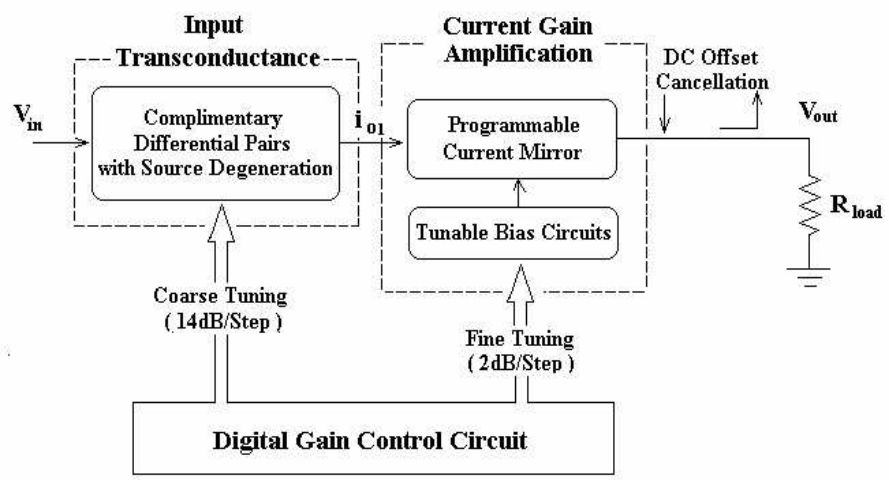


Fig 4.5 Block diagram of the proposed VGA

IV.3 Detailed discussion of the VGA building blocks

IV.3.1 Gain-control scheme

In this VGA, the gain range is from 0 dB to 42dB with 2dB/step and it is divided into coarse tuning (varying the source degeneration resistor) and fine tuning (the varying current gain of the current mirror). There are tradeoffs in allocating the tuning range for coarse and fine tuning. First, consider how many steps can be allocated in the coarse tuning without causing a severe mismatch between the source degeneration resistors. To maintain symmetry and achieve good matching, the resistors and switches should be connected as shown in Fig 4.6.

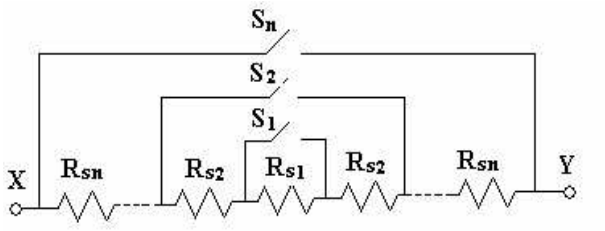


Fig 4.6 Source degeneration resistors and controlling switches configuration

X and Y are connected between the sources of the driver transistors in differential pairs in Fig 4.2. The relation between the number of coarse tuning steps and the corresponding number of resistors/switches required are demonstrated in Table 4.2.

Table 4.2 Coarse tuning steps vs. number of resistors/switches required

	2-step	3-step	4-step	5-step	…	N-step
Number of controlling switches	1	2	3	4	…	N-1
Number of Resistors	1	3	5	7	…	2N-3

According to Table 4.2, to realize N steps of coarse tuning, (2N – 3) source degeneration resistors and (N – 1) switches are required. As the number of resistors increases, it is more difficult to match them because of process parameter variations. Also, MOS transistors operating in the linear region are used to implement the switch, which introduces some nonlinearity. The more switches in the circuit, the more nonlinearity. Thus, with the above concerns, 3-step coarse tuning to cover the entire

42dB gain range is more practical. This leads to each coarse tuning step having 14dB gain range.

On the other hand, the fine tuning is achieved by the programmable current mirror. As illustrated in Chapter III, Fig 3.6, the current gain is set to be less than 10 in this design to ensure enough bandwidth. With 3-step coarse tuning, the fine tuning range of the current mirror will be 14dB, which is within the current gain range to ensure enough bandwidth. Gain step size in fine tuning is determined by the UWB receiver system design, which requires 2dB/step. Therefore, 8 steps of fine tuning are needed to cover the 14dB gain range.

As a result, with the nonlinearity concerns of the MOS switches, the mismatch of resistors in the source degeneration, and the limitation of the maximum gain range of the current mirror, 3-step coarse tuning (14dB each) and 8-step fine tuning (2dB each) are chosen as shown in Table 4.3.

Table 4.3 Coarse/fine tuning combinations

Coarse tuning (dB)	Fine tuning (dB)							
	0	2	4	6	8	10	12	14
0	0	2	4	6	8	10	12	14
14	NA	16	18	20	22	24	26	28
28	NA	30	32	34	36	38	40	42

(1) Coarse tuning

Coarse tuning is obtained by switching on/off the resistor R_{sni} and R_{spi} in Fig 4.2.

The high gain range (28dB to 42dB) requires the lowest linearity level because the input signal levels are very small (10 ~ 20mV_{pp}). Thus, source degeneration is not needed for the differential pairs. Hence, R_{sn1} (R_{sp1}) and R_{Sn2} (R_{sp2}) are disconnected by switching on S_8 and S_9.

In the middle gain range (14dB to 26dB), the input signal is increased compared to the high gain case. To achieve the same linearity level, source degeneration should be included. By switching on S_8 and switching off S_9, R_{Sn2} (R_{sp2}) is connected to the circuit to be the source degeneration resistor.

In the low gain range (0dB to 12dB), the VGA experiences the largest input signal. To maintain the similar linearity level, more source degeneration should be used. So, by switching off both S_8 and S_9, R_{sn1} (R_{sp1}) and R_{Sn2} (R_{sp2}) are connected in series as source degeneration.

The detailed calculation of source degeneration resistor values is derived in Appendix B.

(2) Fine tuning

Fine tuning is obtained by changing the dimensions of the transistors in the bias control circuit of the programmable current mirror. Details about this relation can be found in Chapter III. In our design, 0 ~ 14dB with 2dB/step needed in the fine tuning. So, we implement seven transistors in the bias control circuit to realize 2dB to 14dB.

Also, another switch S_8 is used to short M_3 when 0dB is required as shown in Fig 4.3. Table 4.4 shows the sequence to generate the gain steps.

Table 4.4 Gain vs. bias transistor mapping

Transistors turn-on	Gain steps
M_{b1}	2dB
$M_{b1} + M_{b2}$	4dB
…	…
$M_{b1} + M_{b2} + \ldots + M_{b7}$	14dB

IV.3.2 Input stage complementary differential pairs with source degeneration

Chapter II shows that the VGA based on complementary differential pairs with source degeneration boosts the transconductance while consuming the same power and maintains a similar linearity level as those of the simple differential pair with source degeneration. It is also more power efficient than the multiplier-based VGA and has a larger linear range than the differential pairs with the diode-connected loads-based VGA. Thus, it is used as the input-stage (Fig 4.2).

Also shown in Chapter II, the overall transconductance of this configuration is given by

$$Gm = \frac{g_{mn}}{1+N_n} + \frac{g_{mp}}{1+N_p} \tag{4.1}$$

where we define the source degeneration factor N as: $N_n = g_{mn} \times R_{sn} / 2$ and $N_p = g_{mp} \times R_{sp} / 2$

To select the transconductance of differential pairs, two approaches can be followed [8].

I) The saturation voltage (V_{DSAT}) and the source degeneration factors of both differential pairs can be made equal. This approach provides good linearity, since the saturation voltages of both differential pairs can be maximized. Following this approach, it yields

$$V_{DSAT,n} = V_{DSAT,p} \text{ and } I_{bias,n} = I_{bias,p} \Rightarrow \frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n} \tag{4.2}$$

In IBM 6HP CMOS technology, $\mu_n / \mu_p = 4.5$, then $(W/L)_p = 4.5\ (W/L)_n$. So, the PMOS differential pair will have large dimensions and hence large parasitic capacitance, which will limit the bandwidth of the VGA. This is a major drawback of this approach. The overall transconductance of this approach is given by

$$G_m = \frac{2g_{mp}}{1+N_n} \tag{4.3}$$

II) Use the same dimensions for both differential pairs and also let $N_n = N_p$. Under this condition, $V_{DSATp} = 2.1V_{DSATn}$; so, the harmonic distortion components are dominated by the nonlinearities of the NMOS differential pair. With this approach, the overall transconductance is

$$G_m = \frac{g_{mp}\left(1+\sqrt{\mu_n / \mu_p}\right)}{1+N_n} = \frac{3.13 g_{mp}}{1+N_n} \tag{4.4}$$

For approach I, the V_{DSAT} of both differential pairs can be maximized together as they are equal; for approach II, $V_{DSATp} = 2.1V_{DSATn}$, then V_{DSATp} should be maximized to the desired value, and then V_{DSATn} can be determined accordingly. Thus, V_{DSATp} is the same for both approaches.

To avoid the large parasitic due to the large size of PMOS differential pair, we use approach II in this design instead of approach I to design the complementary differential pairs, which use the same dimension for both differential pairs and the same degeneration factor $N_n = N_p$.

IV.3.3 Current gain stage—programmable current mirror

The current amplification stage is implemented with the programmable current mirror, as it improves frequency response and achieves larger bandwidth than those of the simple current mirror.

In [2] and [3], multi-stage amplification is used. With one programmable current mirror, its current gain is given by (3.10). Thus, with m identical cascade stages, its overall current gain is given by:

$$\frac{i_{out}}{i_{in}} \cong \left[\frac{g_{m2}(C_1 + C_3)}{C_1(2C_1 + C_3)} \frac{s + \dfrac{g_{m1} + \dfrac{1}{R}}{C_1 + C_3}}{\left(s + \dfrac{g_{m1}}{2C_1}\right)\left(s + \dfrac{1}{R(C_1 + 0.5C_3)}\right)} \right]^m \tag{4.5}$$

With the Cadence simulation, the f_{-3dB} of the multi-stage programmable current mirror vs. the current gain can be plotted as shown in Fig 4.8. The simulation setup is shown in Fig 4.7. The dimensions and the bias current values are the same as listed in

Table 3.3. Notice that for an M-stage programmable current mirror to obtain a total current gain of L, each current gain $N = \sqrt[M]{L}$.

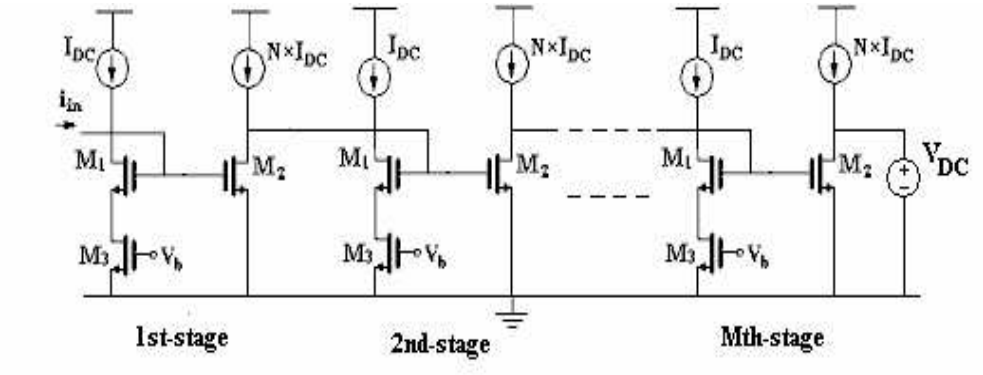


Fig 4.7 Simulation setup for multi-stage programmable current mirror

Fig 4.8 shows that with two or more programmable current mirror stages, to implement current gain of 5 A/A, their f_{-3dB} all drop to less than 700MHz. Including the parasitic capacitance from the input stage which is also connected to the diode-connected node of the programmable current mirror, the overall f_{-3dB} of the VGA may fall below the design requirement (>350MHz). Thus, to ensure enough bandwidth at a large gain variation, only one-stage programmable current mirror is chosen in this design. The details about the programmable current mirror are given in Chapter III.

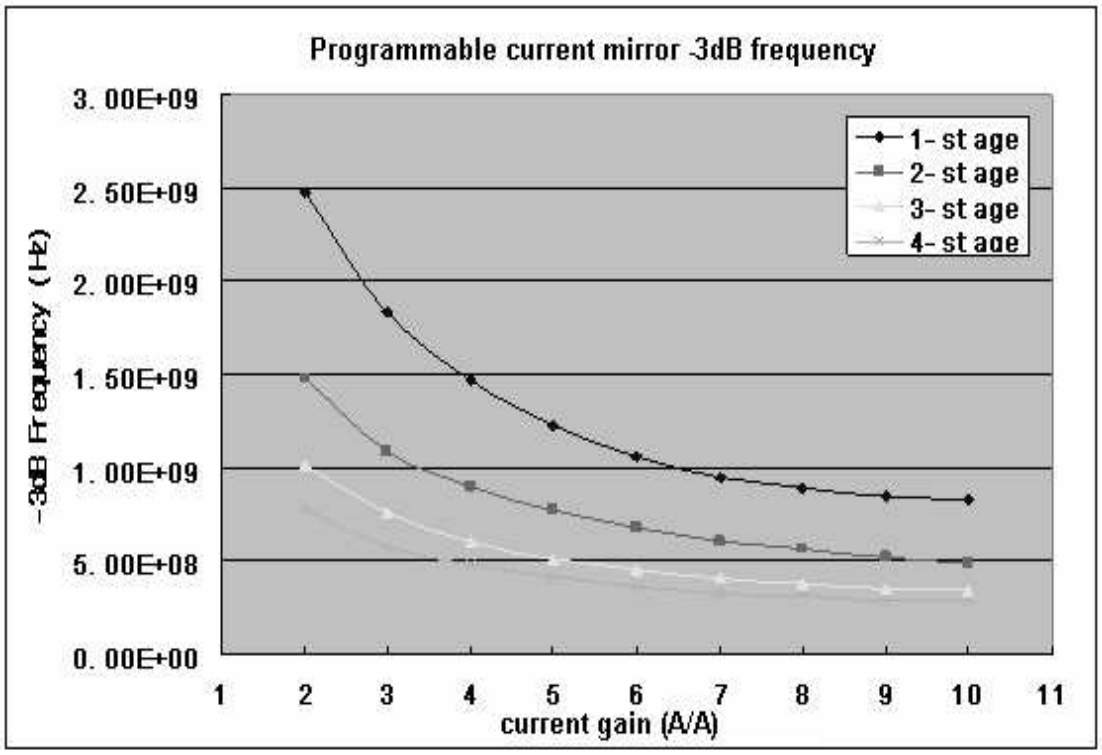


Fig 4.8 f_{-3dB} of the multi-stage programmable current mirror

vs. current gain

IV.3.4 Frequency-compensation scheme

To ensure that even with all parasitic included the overall bandwidth of the VGA is still enough to meet the requirement, the frequency compensation is implemented. To explain the concept of this compensation and its effectiveness, we refer to the programmable current mirror in Fig 4.9.

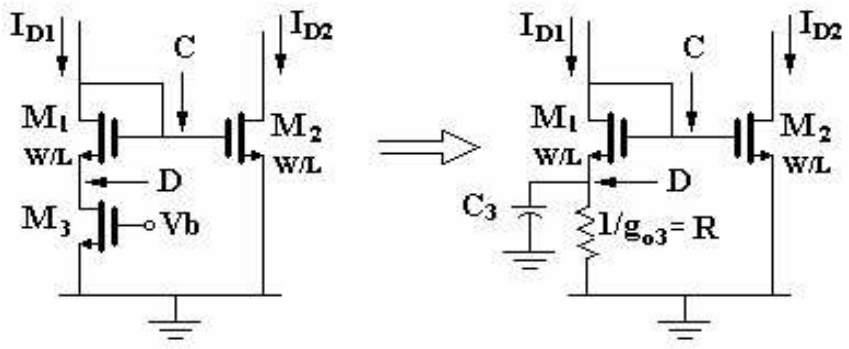


Fig 4.9 Simplified schematic of the programmable current mirror

From equation 3.15, and there are two poles in the programmable current mirror:

$$\omega_{P1} = \frac{g_{m1}}{2C_1}(\text{at node } C), \quad \omega_{P2} = \frac{1}{R(C_1 + 0.5C_3)}(\text{at node } D).$$

where $2C_1 = C_{GS1} + C_{GD1} + C_{DB1} + C_{GS2} + C_{GD2}$ and $C_3 = C_{GD3} + C_{DB3} + C_{GS1} + C_{SB1}$

We can cancel some parasitic capacitance at node C. The capacitive frequency compensation is shown in Fig 4.9. At node V_o, ignoring the output resistance of compensation transistor:

$$I_o + g_m(V_X - V_{in}) + C_m s V_X = 0 \text{ and } I_o = C_C s V_X$$
$$\Rightarrow G_m = \frac{I_o}{V_{in}} = -\frac{g_m C_C s}{g_m + (C_C + C_m)s} \approx -\frac{g_m s}{s + \frac{g_m}{C_C}} \quad (4.6)$$

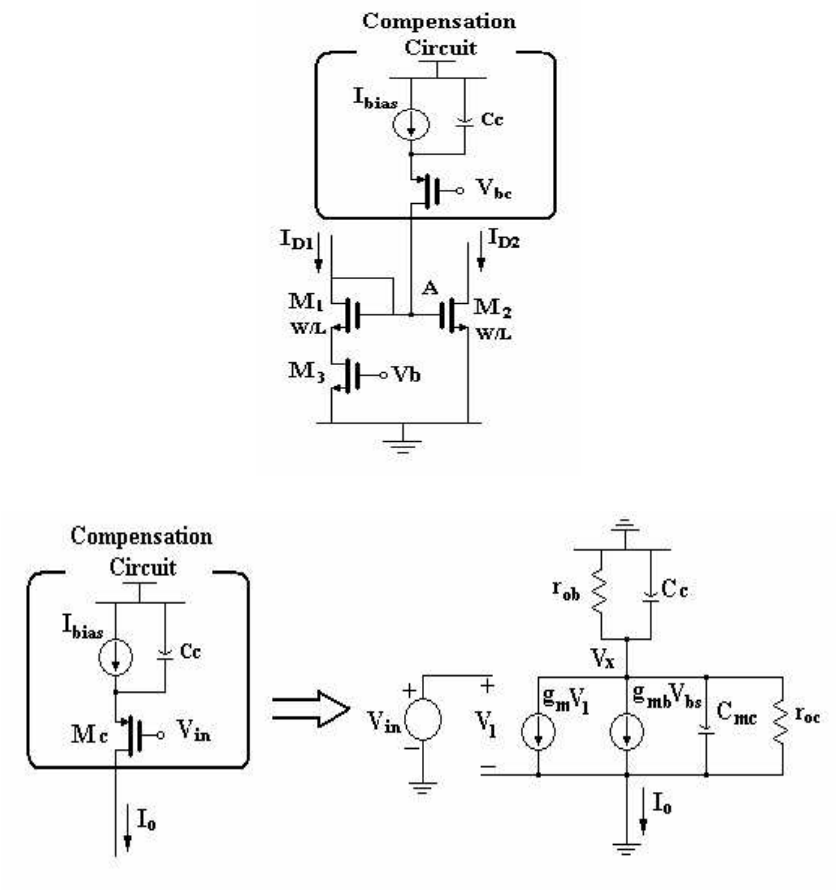
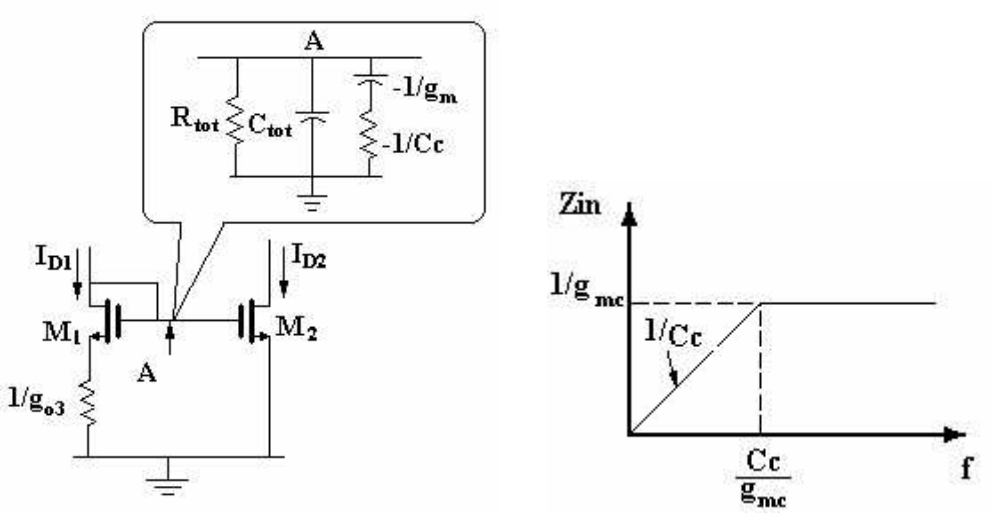


Fig 4.10 Single-ended version of the compensation circuit and its small signal model

So this is equivalent to a negative capacitor ($-C_C$) and a negative resistor ($-1/g_m$) connected in series to node C. This gives us a high-pass characteristic as shown in Fig 4.11.



(a) (b)

Fig 4.11 Compensation effects on the current mirror

As illustrated in Fig 4.11 (b), there exists a corner frequency g_m / C_C. If the corner frequency is higher than the frequency of the pole at node C, we should move this corner frequency to lower frequency to compensate the poles in our VGA. To reduce it, we can either increase C_C or reduce g_{mc}. In Figs 4.12 and 4.13, it is shown that increasing Cc and reducing g_{mc} in a certain range, the bandwidth of the VGA is extended to higher frequency. But if we further reduce the corner frequency of the compensation to lower than the frequency of the pole at node C, the overall capacitance at that node becomes negative. It results in large peaking and extremely large group delay variation. So, the negative capacitance effects from our compensation scheme should not over-compensate the positive parasitic capacitance there.

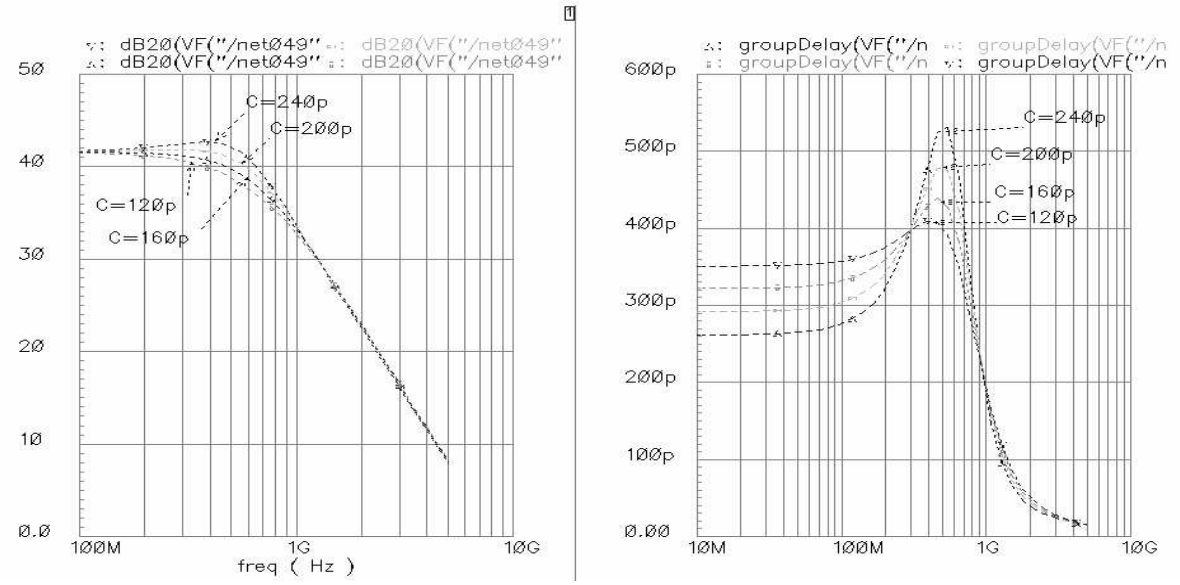


Fig 4.12 Capacitance variation effects on frequency response

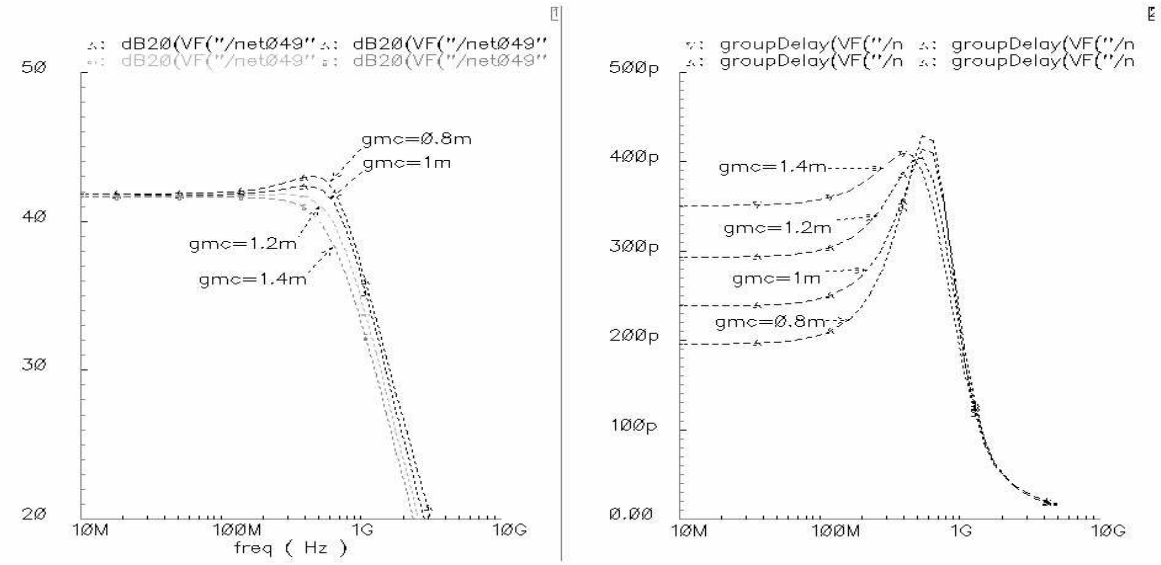


Fig 4.13 g_{mc} variation effects on frequency response

Fig 4.12 shows that by increasing compensation capacitor values from 120 to 240pF, the bandwidth of the VGA is extended. When the capacitor value reaches beyond 200pF, the group delay variation is larger than 200pS which is not tolerable by our design requirement. Therefore, the compensation capacitor should not be increased above certain level, and this level is restricted by the group delay variation requirement. Fig 4.13 indicates that by decreasing the transconductance of the transistor Mc, the bandwidth of the VGA can be extended. However, by further decreasing it to under a certain level, the group delay variation will be intolerable too as shown in Fig 4.12. Therefore, observe from Figs 4.12 and 4.13 that restricting by the group delay variation requirement (<200pS), the compensation will extend the f_{-3dB} by approximately 50%.

Because our VGA is in fully differential style, the capacitive frequency compensation is implemented in a differential version as well (see Fig 4.14 and Table 4.5).

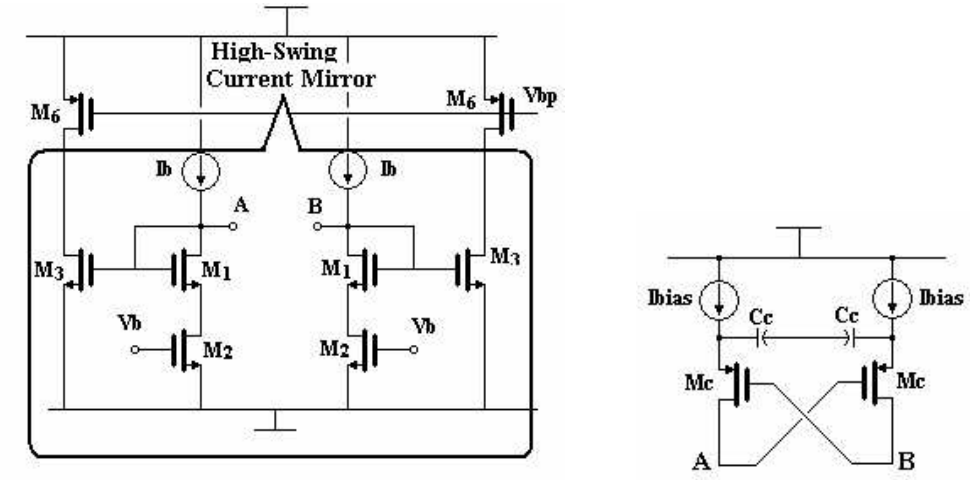


Fig 4.14 Implementation of the capacitive frequency compensation

Table 4.5 Dimension of the capacitive frequency compensation

I_{bias}	W_{Mc}	C_C
220μA	12μm	160fF

IV.3.5 DC offset cancellation

To fix the DC operating point at the output between M_3 and M_6, and to cancel out common-mode offset, an offset-cancellation circuit is used, as illustrated in Fig 4.3. M_4 is half of the size of M_3, $(W/L)_{M4} = 1/2(W/L)_{M3}$, and M_5 and M_6 are identical. So the AC signals at A and B are cancelled, and only their common-mode DC values are left and are feedback to M_6 and M_3. Because of the size used here, the feedback DC current is exactly the amount needed to correct the operating point of M_6 and M_3 to its ideal level. Through this approach, disregarding how the DC bias current changes in the input stage, the output DC level is fixed.

IV.3.6. Digital control circuit

According to the discussion in the gain control scheme, there are 3 steps of coarse tuning and 8 steps of fine tuning. Hence, we can use 2-bit digital control for the coarse tuning and 3-bit digital control for the fine tuning, as illustrated in Fig 4.4. From Table 3.2, the digital gain control for the bias voltage of M_2 in Fig 3.4 is identical to the thermometer code, the logic for which is given as:

$$s_0 = \overline{b_0 b_1 b_2} \quad s_1 = \overline{b_1 b_2} \quad s_2 = \overline{(b_0 + b_1) b_2} \quad s_3 = b_3$$
$$s_4 = \overline{b_0 b_1 + b_2} \quad s_5 = \overline{b_1 + b_2} \quad s_6 = \overline{b_0 + b_1 + b_2} \tag{4.7}$$

Then, the digital control circuit is implemented, as in Fig 4.15.

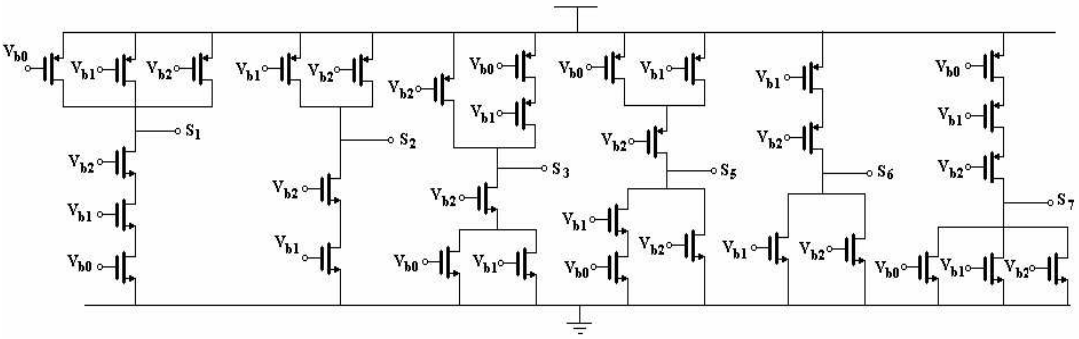


Fig 4.15 Digital control circuit

IV.3.7 The dimension and bias current for the VGA

The nominations of the components in the VGA are illustrated in Figs 4.2 and 4.3. The corresponding dimensions and bias currents for the VGA are shown in Tables 4.6 and 4.7. Please refer to Appendix B for the calculation details.

Table 4.6 Dimensions and bias currents of the components of the VGA in the signal path

W_{Mp}	W_{Mn}	R_{s1}	R_{s2}	R_{load}
78um	78um	3K ohm (R_{sn1}) 4.5K ohm (R_{sn1})	300 ohm (R_{sn2}) 450 ohm(R_{sn2})	1.5K ohm
I_{bias}	I_b	W_{M1}	W_{M2}	W_{M3}
400µA	220µA	24µm	16µm	24µm
L = 0.24um for all transistors				

Table 4.7 Dimensions for the transistors in the bias control circuit (Fig 4.3)

W_{Mb1}	W_{Mb2}	W_{Mb3}	W_{Mb4}	W_{Mb5}	W_{Mb6}	W_{Mb7}
2μm	4.8μm	4.8μm	4.8μm	4.8μm	1.68μm	0.72μm

IV.4 Conclusion

In this chapter, the design challenges and motivations of this VGA design are summarized. Complementary differential pairs with source degeneration are used as the input stage to achieve the good power-efficiency and maintain enough linearity. The programmable current mirror is proposed as the current amplification to further amplify the current, which has good programmability and frequency response. To cover the large variable gain range, gain tuning is further divided into coarse and fine tuning. Coarse tuning is obtained by changing the source degeneration resistor in the input stage; while fine tuning is achieved by varying the transistor dimension in the bias control circuit and hence changing the current amplification ratio. Both schemes are programmed by the digital gain control. Capacitive frequency compensation is adapted to further extend the bandwidth of the VGA, and a DC offset cancellation is used to fix the DC output voltage level and cancel out the offset voltage due to gain changing or mismatch effects. Overall, the proposed VGA structure is able to achieve large variable gain rang, very large bandwidth with very low power consumption, and very small group delay variation. The simulation result of this design will be given in the next chapter to justify the performance of this VGA.

CHAPTER V

SUMMARY OF RESULTS

The VGA has been designed in the IBM 6HP 0.25μm CMOS process. Simulation results are included in this chapter. The experimental results for the prototype fabricated in the same process are presented.

V.1 Design summary

The design specifications for the VGA are summarized in Table 5.1.

Table 5.1 Design specifications for VGA

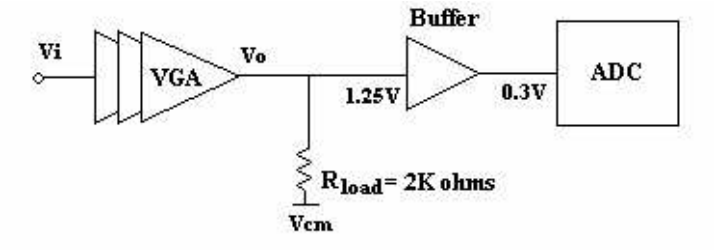
Technology	IBM6HP 0.25μm CMOS process
Variable gain range	0 ~ 42dB, 2dB/step
Bandwidth (f_{-1dB})	> 264MHz
Linearity (IIP3)	> -15dBm
Noise (Noise Figure)	< 25dB
Group delay variation	< 200pS
Power consumption	< 20mW

V.2. Simulation setup

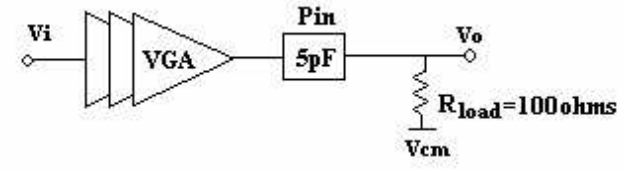
Two simulation setups are performed, these are:

1) Use a buffer to provide the voltage level shift for the ADC's 0.3V input DC voltage level. In this case, the load resistors are still chosen as the previous design value which is 2KΩ.

2) Without using a buffer to ADC while the VGA output is directly connected to the output pads which have large capacitance (about 5pF). The load resistors are external resistors outside the chip, and to ensure VGA's bandwidth will not get degraded by the pole from the resistance from the load and the large parasitic capacitance of the pads, the load resistors are intentionally made accordingly smaller—100 ohm for this case .



(a) With buffer to ADC stage (R_{load} = 2K ohm)



(b) Without buffer to ADC stage (R_{load} = 100 ohm)

Fig 5.1 Simulation setup

Comparing these two setups, we realize that the maximum DC gain from the second setup will be 16dB instead of 42dB because its load resistor is 20 times smaller than that of the first case. However, it can be still verified the functionality of the VGA based on the second setup, as the VGA current amplification range in both setups is the equal, just the load resistor plays a multification factor to determine the final absolute value of the gain. These two setups are shown in Fig 5.1.

The dimensions of the VGAs used in the different setups are listed in Table 5.2 as shown.

Table 5.2 Dimensions of the VGAs for different setups

With buffer to ADC stage							
M_p	M_n	R_{s1}	R_{s2}	R_{load}	M_1	M_2	M_3
78/0.24 (µm)	78/0.24 (µm)	3K ohm 4.5K ohm	300 ohm 450 ohm	2K ohm	24/0.24 (µm)	16/0.24 (µm)	24/0.24 (µm)
I_{biasn}*	I_{biasp}*						
910µA	1040µA						
M_{b1}	M_{b2}	M_{b3}	M_{b4}	M_{b5}	M_{b6}	M_{b7}	
2/0.24 (µm)	4.8/0.24 (µm)	4.8/0.24 (µm)	4.8/0.24 (µm)	4.8/0.24 (µm)	1.68/0.24 (µm)	0.72/0.24 (µm)	

Without buffer while directly connected to the output pads								
M_p	M_n	R_{s1}	R_{s2}	R_{load}	M_1	M_2	M_3	
78/0.24 (µm)	78/0.24 (µm)	3KΩ 4.5KΩ	300Ω 450Ω	100Ω	As the same as the case with buffer to ADC			
I_{biasn}*	I_{biasp}*	M_{b1}	M_{b2}	M_{b3}	M_{b4}	M_{b5}	M_{b6}	M_{b7}
1170 µA	1040µA	As the same as the case with buffer to ADC						

In the following sections, the post-layout simulation results of these two setups will be shown and discussed.

V.3 Simulation results

V.3.1 Explanation of simulation terminologies

The simulation results provided are collected from the post-layout simulations, in which all the parasitic capacitors are extracted except for the well-to-subtract parasitic capacitance. Measurement setting and simulated terms are defined as follows.

(1) -1dB bandwidth (f_{-1dB})

This is the bandwidth in which the voltage gain is 1dB below the DC gain. It indicates the gain flatness of the VGA within the useful bandwidth.

(2) -3dB bandwidth (f_{-3dB})

This is the bandwidth in which the voltage gain is 3dB below the DC gain, and it is commonly used as a critical specification in many VGA designs.

(3) Linearity and distortion

Consider a nonlinear system described by

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{5.1}$$

where y (t) and x (t) are the output and input of the system respectively.

Consider $x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$, where ω_1 and ω_2 are two frequencies very closed to each others around the frequency of interest, substitute this into equation 5.1 yields

$$y(t) = \left(a_0 + a_2 A^2\right) + \left(a_1 A + \frac{9a_3 A^2}{4}\right)\cos(\omega_1 t) + \left(a_1 A + \frac{9a_3 A^2}{4}\right)\cos(\omega_2 t) +$$
$$\left(\frac{a_2 A^2}{2}\right)\cos(2\omega_1 t) + \left(\frac{a_2 A^2}{2}\right)\cos(2\omega_2 t) + \left(a_2 A^2\right)\cos[(\omega_1 + \omega_2)t] +$$
$$\left(a_2 A^2\right)\cos[(\omega_1 - \omega_2)t] + \left(\frac{3a_3 A^3}{4}\right)\cos[(2\omega_1 - \omega_2)t] + \left(\frac{3a_3 A^3}{4}\right)\cos[(2\omega_2 - \omega_1)t] + \quad (5.2)$$
$$\left(\frac{3a_3 A^3}{4}\right)\cos[(2\omega_1 + \omega_2)t] + \left(\frac{3a_3 A^3}{4}\right)\cos[(2\omega_2 + \omega_1)t] +$$
$$\left(\frac{3a_3 A^3}{4}\right)\cos(3\omega_1 t) + \left(\frac{3a_3 A^3}{4}\right)\cos(3\omega_2 t)$$

The third-order intercept point (IIP3): It is defined as the input signal power level at which the fundamental component intercepts with the third-order intermodulation component. From equation 5.2,

$$\left(a_1 A_{IIP3}\right) = \left(\frac{3a_3 A_{IIP3}^3}{4}\right) \Rightarrow A_{IIP3} = \sqrt{\frac{4|a_1|}{3|a_3|}} \quad (5.3)$$

Also, the third-order intermodulation distortion IM3 is defined as

$$IM\ 3 = \frac{3|a_3|}{4|a_1|} A^2 \quad (5.4)$$

Comparing equation 5.3 and 5.4, we can relate IIP3 with IM3 as follows,

$$A_{IIP3}{}^2 = A^2 / \left(\frac{3|a_3|}{4|a_1|} A^2\right) = A^2 / IM_3 \Rightarrow 20\log\left(A_{IIP3}{}^2\right) = 20\log A^2 - 20\log(IM_3) \quad (5.5)$$
$$\Rightarrow A_{IIP3}(dBm) = A(dBm) - \frac{IM_3(dB)}{2}$$

where A is the input signal magnitude in dBm unit.

By measuring IM3 at a certain input signal level, IIP3 can be obtained accordingly.

(4) Input referred integrated noise

Input referred noise is the noise collected from the VGA output divided by the gain of the VGA. In this simulation, the input referred integrated noise is integrated from DC to 250MHz.

(5) Signal-to-Noise-Ratio (SNR)

Low noise is an important concern if the input signal is very small and the bandwidth of interest is very wide. Since we are interested in a very high frequency, the contribution from the 1/f noise at a lower frequency can be neglected. Signal-to-Noise-Ratio is

$$SNR = 10\log\frac{V_{in,rms}^2}{V_{n,in}^2} \tag{5.6}$$

where $V_{in,rms}$ is the root-mean-square value of the input signal, and $V_{n,in}$ is the equivalent input referred noise voltage.

(6) Noise Figure (NF)

The most commonly accepted definition of Noise Figure is given in equation 5.7.

$$Noise\ Figure = \frac{SNR_{in}}{SNR_{out}} \tag{5.7}$$

Noise Figure is a measure of how much the SNR degrades as the signal passes through a system. And it can be written as:

$$NF = 10 \cdot \log\left(1 + \frac{IN^2}{4kTR_s \cdot BW}\right) \tag{5.8}$$

where IN is short for integrated input referred noise voltage.

For $R_s = 50\ \text{ohm}$ and BW = 250MHz, $4kTR_s \cdot BW = 1.96 \times 10^{-10} V^2$

(7) Group Delay

The Group Delay is defined as the rate of change of the total phase shift with respect to the angular frequency:

$$\text{Group Delay} = \frac{\partial \theta}{\partial \omega} \tag{5.9}$$

It also is the time delay through the system for a sine wave pulse. If the group delay is non-uniform and varies with the sine-wave frequency, the time-domain response to a sharp input-signal change may show overshoot or ringing. Thus, a perfectly uniform group delay is equivalent to a perfectly linear phase response.

(8) Figure of Merit (FOM)

A Figure of Merit (FOM) is defined such that this VGA's performance can be compared with other VGA designs fairly. Based on the design requirements, the FOM should include the maximum DC voltage gain ($A_{V,MAX}(0)$), the -3dB frequency bandwidth (f_{-3dB}), the technology, the power consumption, and the silicon area of the VGA. With concerns of linearity and noise, the Signal to Noise Ratio should be included in the FOM as well, which indicates the ratio between the input signal level (under sufficient linearity level) and the input referred noise voltage. Thus, the FOM can be defined as

$$FOM = \frac{A_{V,MAX}(0) \times f_{-3dB} \times \text{SNR} \times \text{Technology}}{\text{Power} \times \text{Area}} \tag{5.10}$$

Next, the post-layout simulation results are presented in detail.

V.3.2 Layout

The VGA is laid out for I/Q channels, and includes analog and digital parts as shown in Fig 5.2.

Each VGA occupies silicon area of $140\mu\text{m} \times 110\mu\text{m} = 15400\mu\text{m}^2 = 0.0154\text{mm}^2$, and the total area of I/Q channels is approximately 0.03mm^2.

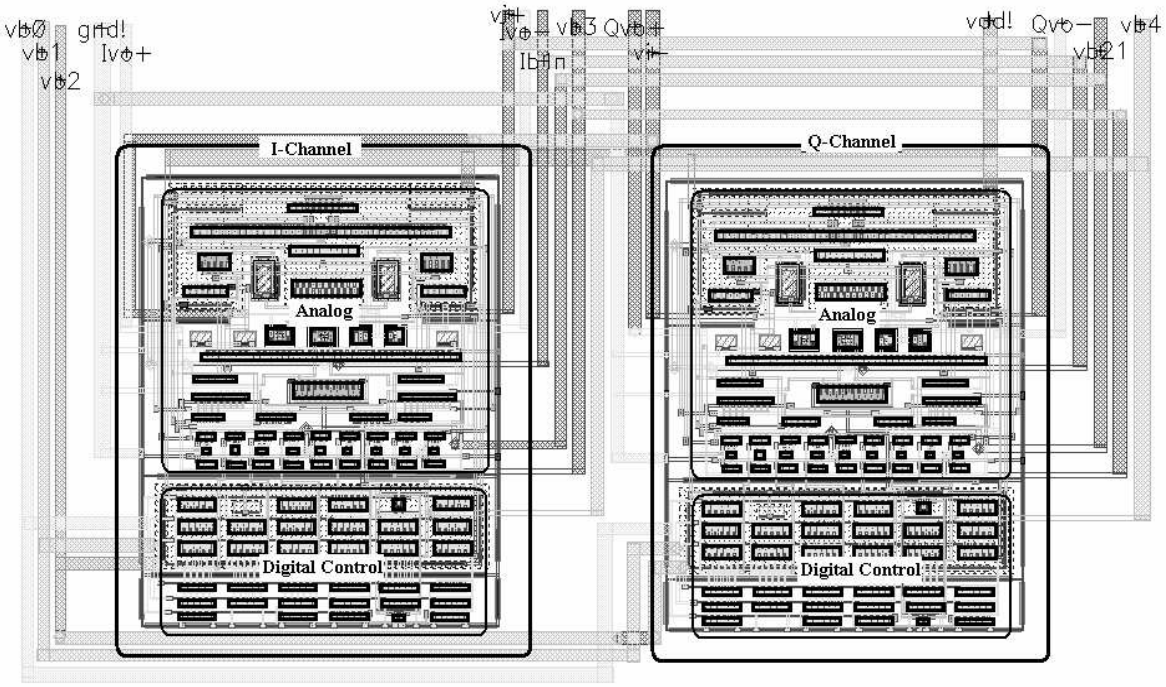


Fig 5.2 Layout view of the I/Q channels of the VGA

V.3.3 AC response

The VGA post-layout simulation results of the AC response are shown in Figs 5.3 through 5.8d. It achieves 0 to 42dB with 2dB/step for this VGA with both simulation setups (one with a buffer to ADC and the other without). For the setup with a buffer to ADC, it achieves $f_{-1dB} > 321MHz$ ($f_{-3dB}= 474MHz$), and the group delay for all cases is less than 150 pS. As for the setup without a buffer with the VGA output directly tied to the pads, it achieves $f_{-1dB} > 290MHz$ ($f_{-3dB}= 411MHz$), and the group delay for all cases is less than 110 pS for all gain cases. Therefore, all results meet the requirements, as summarized in Tables 5.3 and 5.4.

Table 5.3 Post-layout AC response simulation results vs. system requirements

With buffer to ADC	Gain Range (dB)	Bandwidth (MHz)	Group Delay(pS)
Post-Layout Simulations	0 ~ 42dB 2dB/Step	321[f_{-1dB}] (474[f_{-3dB}])	146
System Requirements		>264 [f_{-1dB}]	<200
Without buffer to ADC	Gain Range (dB)	Bandwidth (MHz)	Group Delay(pS)
Post-Layout Simulations	0 ~ 42dB 2dB/Step	311[f_{-1dB}] (290[f_{-3dB}])	108
System Requirements		>264 [f_{-1dB}]	<200

Table 5.4 AC response

a. With Buffer to ADC (R_{load} = 2K ohm)

2dB/Step, 0 ~ 42dB			
Ideal Gain (dB)	Real Gain (dB)	f_{-3dB} (MHz)	Group Delay(pS)
42	42.65	474 (321[f_{-3dB}])	45
36	35.9	492	86
30	30.14	512	110
24	24.3	528	102
18	18.14	540	131
12	11.92	548	136
6	6.1	562	139
0	0.368	580	146

b. Without buffer to ADC (R_{load} = 100 ohm)

Ideal Gain (dB)	Real Gain (dB)	f_{-3dB} (MHz)	Group Delay(pS)
16	16.65	411(290 [f_{-3dB}])	39
10	10.8	432	44
4	4.3	459	67
-2	-1.4	489	93
-8	-7.3	490	89
-14	-13.9	496	96
-20	-20.4	512	102
-26	-26.3	520	108

(1) Frequency response based on VGA setup with buffer to ADC

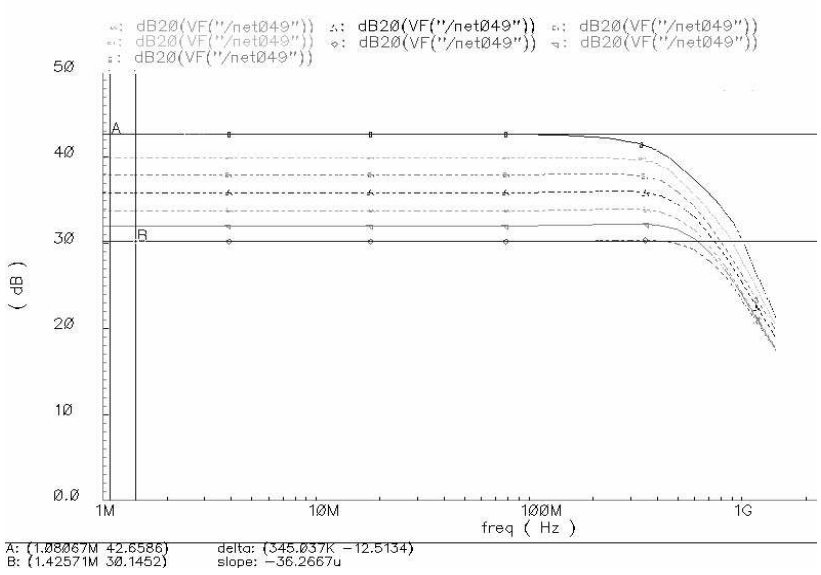


Fig 5.3 Gain steps from 30dB to 42dB

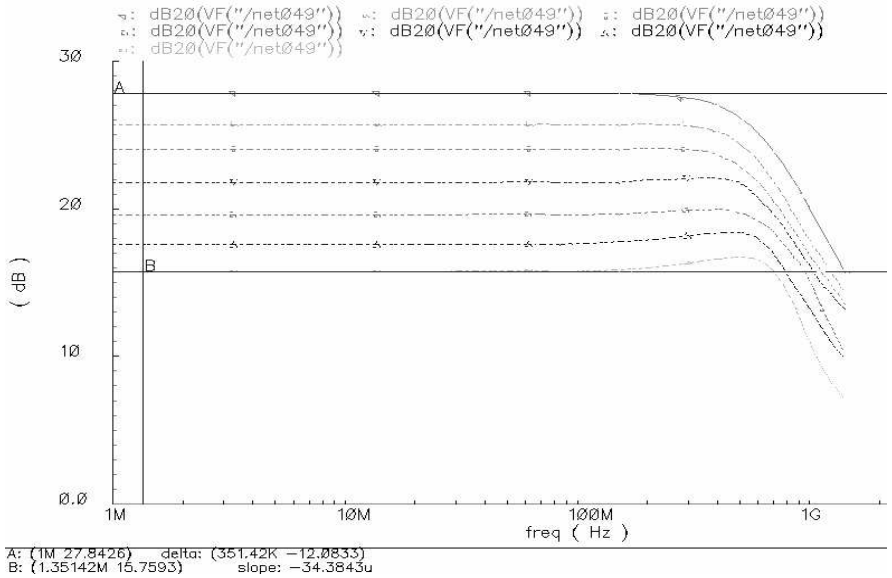


Fig 5.4 Gain steps from 16dB to 28dB

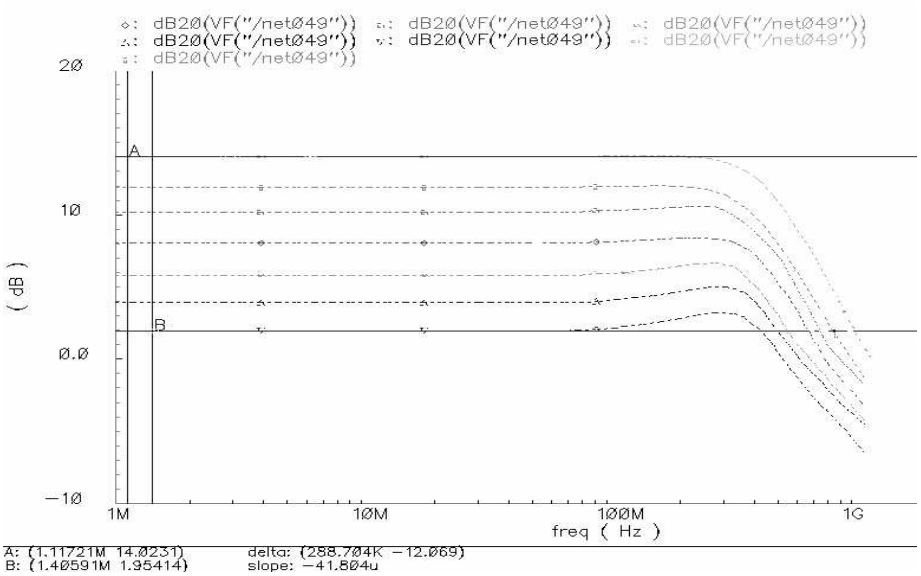


Fig 5.5 Gain steps from 0dB to 14dB

(2) Frequency response based on VGA setup without buffer to ADC

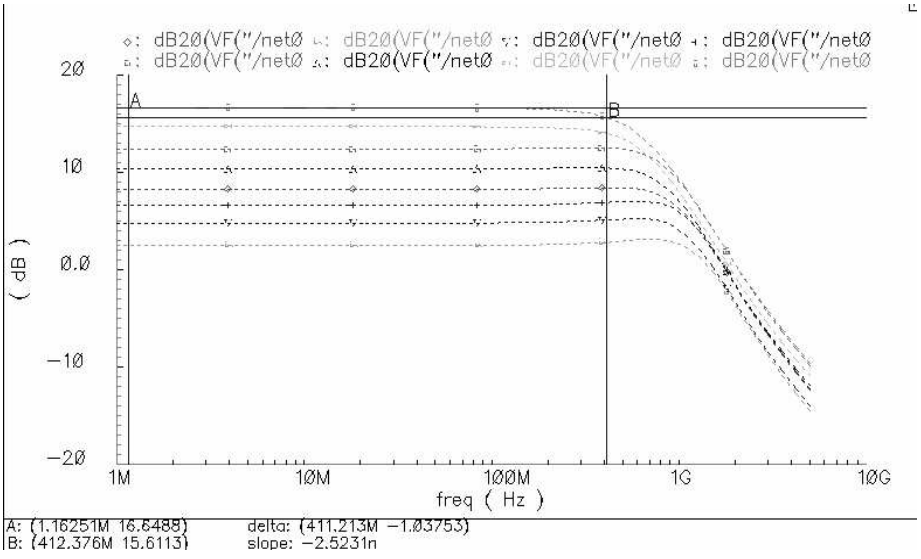


Fig 5.6 Gain steps from 2dB to 16dB

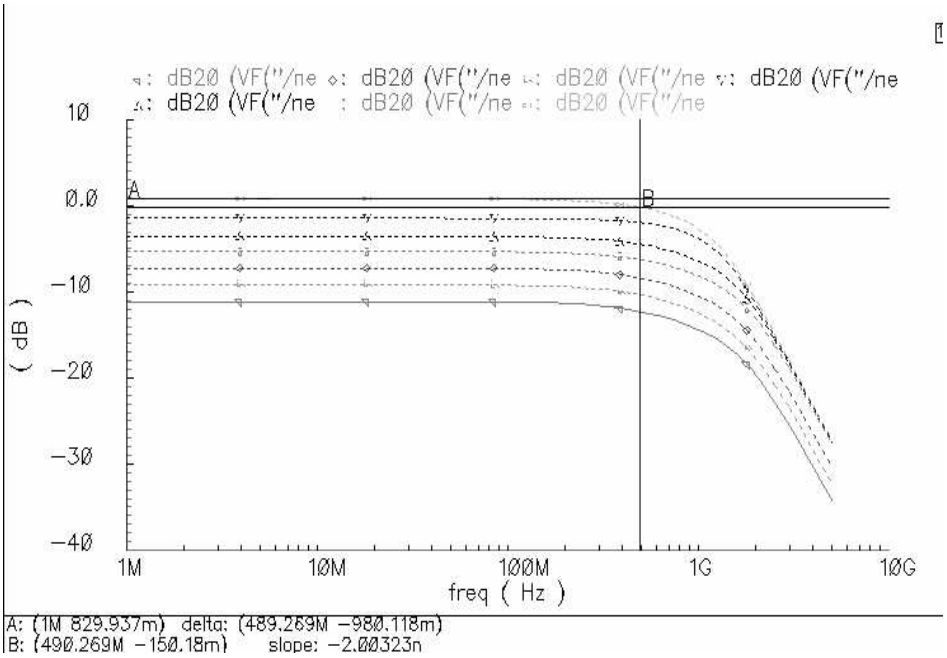


Fig 5.7 Gain steps from -12dB to 0dB

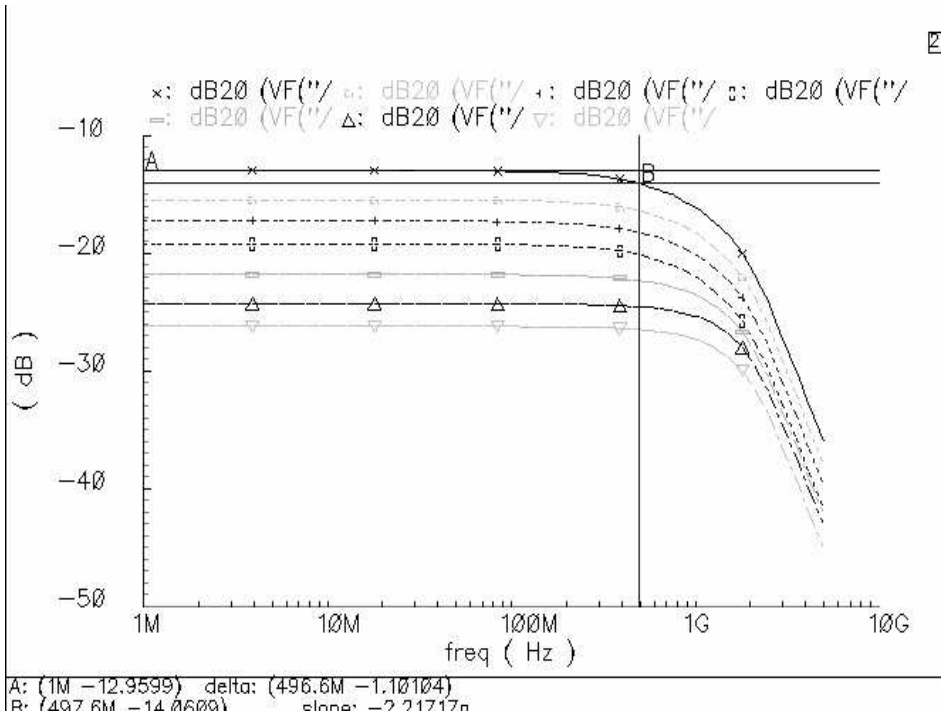


Fig 5.8 Gain steps from -26dB to -14dB

V.3.4 Noise

(1) SNR

The Signal-to-Noise-Ratio (SNR) is defined previously in equation 5.6 as the ratio between the root-mean-square values of the input signal to the corresponding equivalent input-referred noise voltage.

$$SNR = 10\log\frac{V_{in,rms}^2}{V_{n,in}^2} \tag{5.6}$$

where $V_{in,rms}$ is the root-mean-square value of the input signal, and $V_{n,in}$ is the equivalent input referred noise voltage.

VGA with maximum gain setting has the smallest input signal. Therefore, noise at a 42dB gain setting is characterized at this section. As the differential output-signal level of the VGA is fixed to $1V_{pp}$, and the equivalent input referred noise power ($V_{n,in}^2$) is $3.6\times10^{-9}V^2/Hz$ at 42dB gain, so the SNR is given as

$$SNR = 10\log\frac{V_{in,rms}^2}{V_{n,in}^2} = 10\log\frac{\left(\frac{1}{2\sqrt{2}\cdot10^{\frac{42}{20}}}\right)^2}{3.6\cdot10^{-9}} = 33.4\text{dB}$$

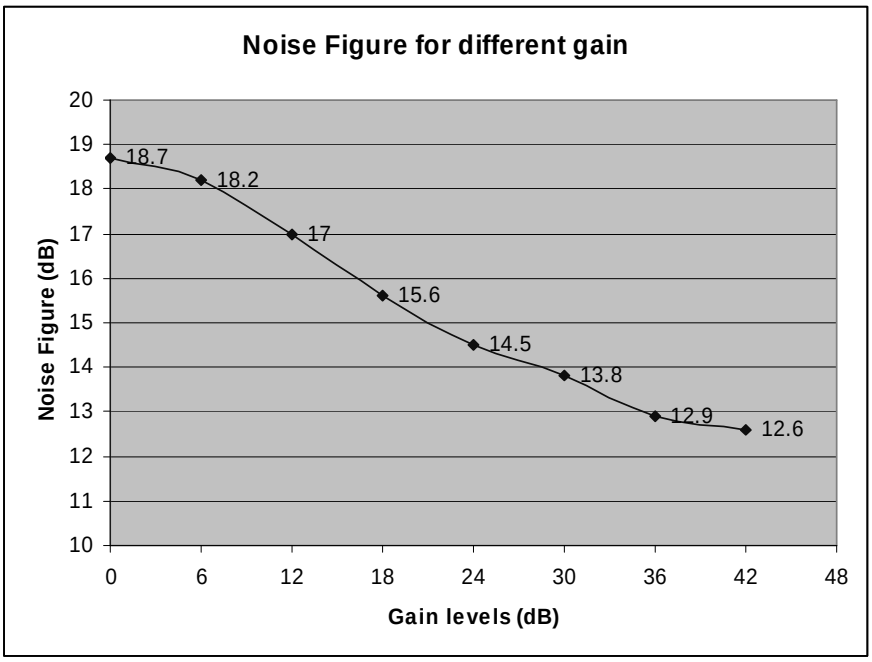
(2) Noise Figure

The Noise Figure (NF) can be written as:

$$NF = 10\cdot\log\left(1+\frac{IN^2}{4kTR_s\cdot BW}\right) \tag{5.8}$$

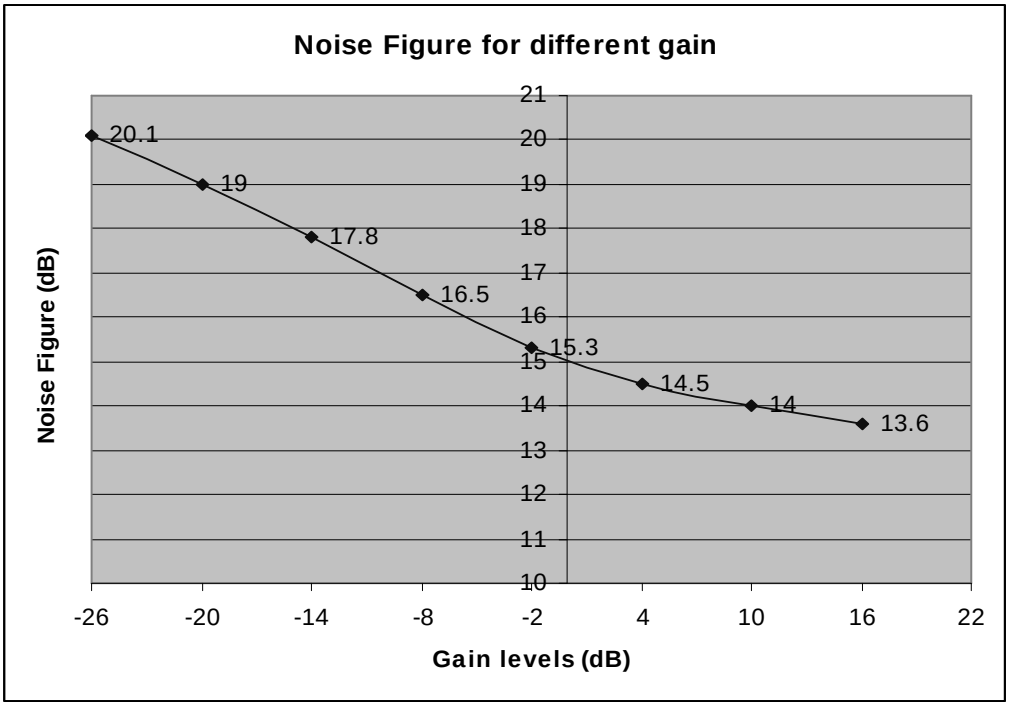
where IN is short for Integrated Input Referred Noise Voltage.

For R_S=50 ohm and BW = 250MHz, $4kTR_S \cdot BW = 1.96\times10^{-10}V^2$. Thus, we calculate the Noise Figure based on IN as shown in Fig 5.9. As expected, the Noise Figure degraded from high-gain to low-gain cases as shown in Fig 5.9. The worst Noise Figure for the VGA with a buffer to ADC is 18.7dB; while for the case without a buffer, it gives 20.1dB for the worst case. So, both cases meet the system specification which requires the Noise Figure to be less than 25dB for all gain steps.



(a) With buffer to ADC (R_{load} = 2KΩ)

Fig 5.9 Noise Figure for different gain levels



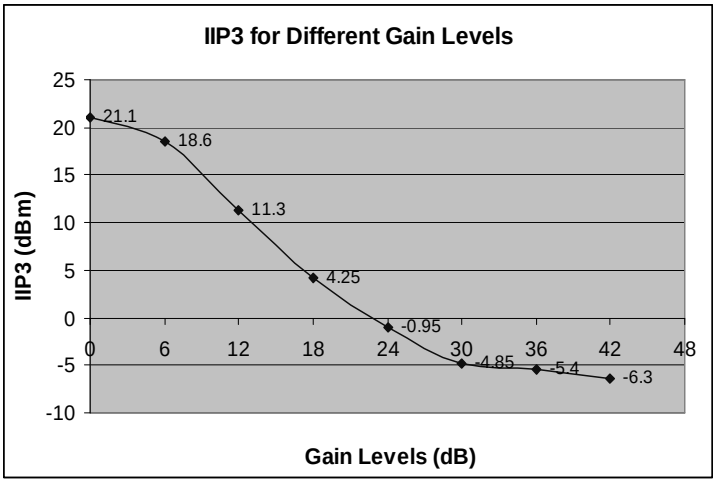
(b) Without buffer to ADC (R_{load} = 100Ω)

Fig 5.9 Continued

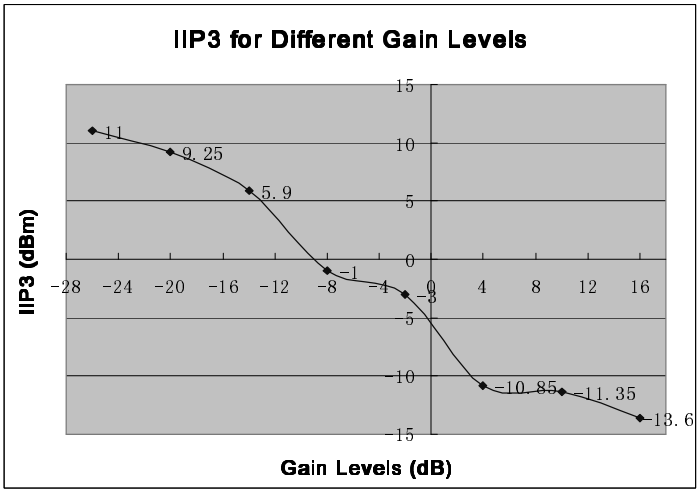
V.3.5 Linearity

Because the output signal level is fixed by the VGA, increasing the gain in the VGA corresponds to lower input signal level, which relaxes the linearity requirement of the VGA. In other words, the most critical case to ensure good linearity in the VGA should be the lowest gain case, which corresponds to the largest input signal level. Therefore, the VGA should be designed to posses improving linearity when gain is reduced; that is the reason more source degeneration resistance in the lower gain case are

turned on. IIP3 for different gain settings is plotted in Fig 5.10. As expected, the better linearity is achieved in lower gain cases. The worst case for IIP3 is at 42dB, which is -6.3dBm, and is better than the required -15dBm.



(a) With buffer to ADC (R_{load} = 2K ohm)



(b) Without buffer to ADC (R_{load} = 100 ohm)

Fig 5.10 IIP3 for different gain levels

V.3.6 Power consumption

The maximum power consumption happens at the highest gain case—42dB, which only consumes 9.5mW and is way below the 20mW required by the system as shown in Fig 5.11, because the power efficient complementary differential pairs are used as the input stage.

signal	OP("v105" "??")
i	-3.793m
pwr	-9.482m
v	2.5

Fig 5.11 Power consumption

V.4 Experimental results

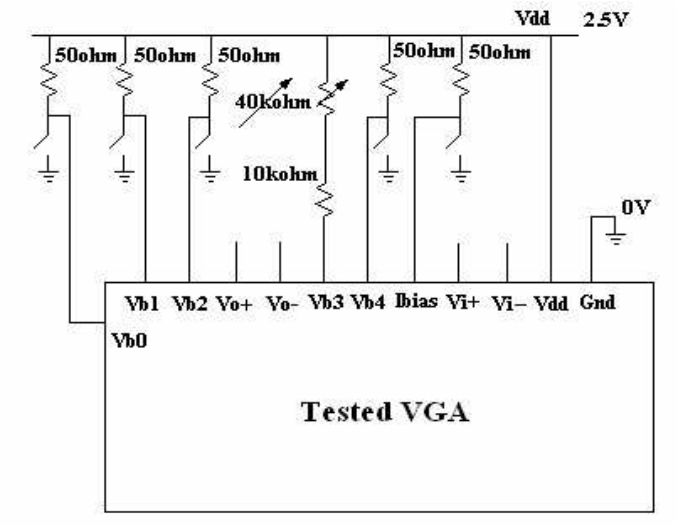


Fig 5.12 VGA testing pins arrangement

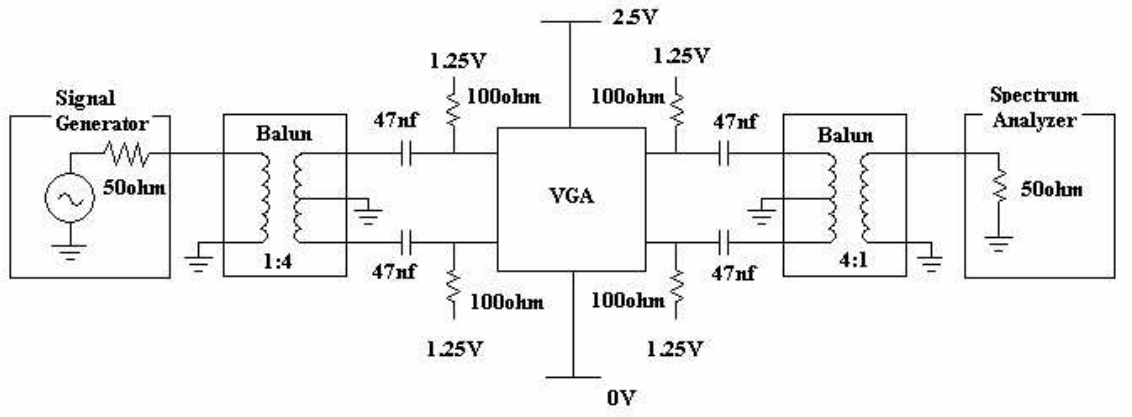


Fig 5.13 VGA input/output testing setup

The testing setup is shown in Figs 5.12 and 5.13. The VGA is fabricated in IBM 6HP 0.25μm CMOS technology. To convert single-ended input signal from the signal generator to the differential inputs for the VGA, balun (an abbreviation for balanced to unbalanced) is used. The ratio of the number of balun turns from single end to the differential ports is 1:4. Because broadband matching is required, only resistive instead of impedance-matching networks are used to match the output impedance of the signal generator. To convert the differential output signal from the VGA into the single-ended signal required by the measurement of the spectrum analyzer, a 4:1 balun is used at the output of the VGA. The 47pF capacitors are used for the AC coupling so that the input common-monde voltage is set by the input common-mode voltage level which is 1.25V for this design, and the output common-mode voltage is fixed at the middle of the power supply voltage to maximize the output voltage swing. For the measurement, a spectrum

analyzer with 50 ohm input impedance is used to measure the frequency response. The supply voltage is 0 to 2.5V.

The testing shows a gain variation from -18dB to 14dB, with a 2dB/step. Including the gain loss of approximately 2dB from the balun (transformer), the maximum gain is as we expected as the post-layout simulation of 16dB for maximum gain with a 100 ohm load resistor (with 2K ohm, it will be 42dB). The -1dB frequency is from 266 to 293MHz, all above 264MHz, but a little bit short than the post-layout simulation (288~ 315MHz). The IIP3 are closed to the post-layout simulation results too.

V.4.1 Experimental results for the AC response of the VGA

The results are listed and illustrated in Table 5.5 and the remaining figures in the chapter. As mentioned previously, to avoid the bandwidth reduction caused by the pole from the large parasitic capacitance of the pad and the load resistor, a 100 ohm resistor is used as the load instead of 2K ohm. With this test setting, the experimental results show a gain range from -18dB to 14dB with the 100 ohm load resistor. Including the gain loss from the balun which is about 2dB, the above gain range corresponds to a gain range of 10 to 42dB with 2K ohm load resistor. We can also compare the DC gain of the testing results with the ideal DC gain steps desired to get an idea of the accuracy of the gain steps. In Table 5.5, it shows that, regarding the gain step accuracy, the worst case has a 0.73dB deviation from the ideal case (at -2dB ideal case, the experimental result shows -1.2783dB). Thus, we can conclude that the deviations of gain-step from our desired values are all within the 1dB range. This further justifies that the programmable current

mirror proposed in this design can be accurately controlled to provide the desired gain variation at least to 2dB/step.

As for the bandwidth, the -1 dB bandwidth (f_{-1dB}) is defined previously to ensure the gain flatness within the useful bandwidth. Hence, we desired to have f_{-1dB} at least larger than 264MHz for all cases to cover the entire band of interest. Among all the gain steps, the smallest f_{-1dB} is about 266MHz and the largest is about 293MHz. These results verify that this design has enough bandwidth to cover the desired band and that the bandwidth is relatively constant along the whole gain range. The large and constant bandwidth is benefit from the good frequency response of the programmable current mirror and the capacitive frequency compensation, as demonstrated in Chapter IV.

Besides, comparing to the post-layout simulation results, it can be also observed that the deviations of the gain steps between the post-layout simulation and the experimental results are all within the 2dB range, which indicates that the IBM 6HP design-kit includes relatively accurate models of parasitic effects of the components and thus provides designers a close estimation between the simulation results and the real performance of the design on the silicon.

Table 5.5 Testing results for VGA AC response

Gain steps (dB)	Post-layout simulation		Testing	
	DC Gain (dB)	f_{-1dB} (MHz)	DC Gain (dB)	f_{-1dB} (MHz)
-18	-18.3	315	-18.687	291.15
-16	-15.92	310	-16.095	284.06
-14	-13.9	304	-14.273	282.4
-12	-12.1	320	-12.2	291.9
-10	-9.9	316	-10.068	291.105
-8	-7.3	305	-7.27	281
-6	-5.92	310	-5.6832	281.875
-4	-4.05	307	-4.168	288.56
-2	-1.4	298	-1.2783	276.68
0	0.24	303	-0.595	288.2
2	2.1	307	2.3413	293.57
4	4.3	305	4.2174	283.67
6	5.95	302	6.011	270
8	8.02	302	7.9052	267.87
10	10.8	294	9.108	270.48
12	11.78	299	11.492	270.22
14	13.85	288	13.561	266.7

The measurement results of the frequency response of the gain settings of 14, 12, 10, 8, and 6dB with a 100 ohm load resistor is shown in Fig 5.14. Including the loss from the balun, which is about 2dB, this group of gain settings correspond to 42, 40, 38, 36, and 34dB with the 2K ohm load resistor. Because we are considering the whole

VGA gain range, this group of gains is high gain stages, the -1dB frequency of this group of gain settings is between 266 to 270MHz as illustrated in Table 5.5 previously and are relatively low compared to other low gain cases. Table 5.5 also shows that the gain accuracy of this group of gains is below 0.9dB derivation from the ideal DC gain values. This gain derivation is still tolerable because it is less than the minimum gain step (2dB/step) of the VGA.

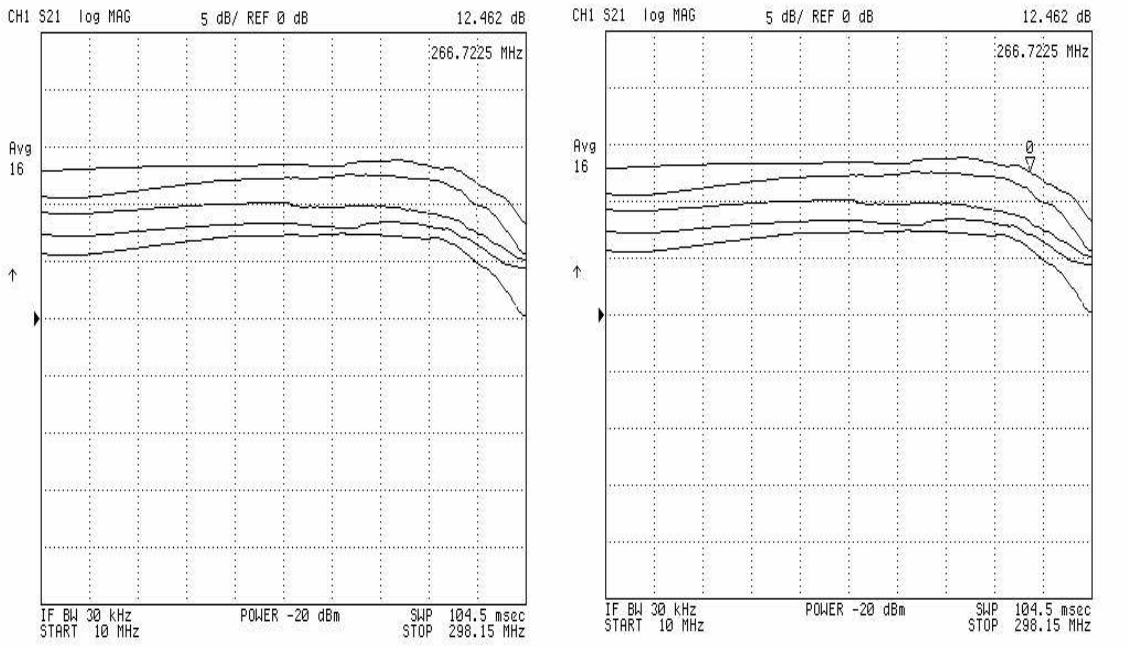


Fig 5.14 Frequency response of gain settings of 14, 12, 10, 8, and 6dB

The measurement results of the frequency response of the gain settings of 4, 2, 0, -2, -4, and -6dB with a 100 ohm load resistor are shown in Fig 5.15, and correspond to 32, 30, 28, 26, 24, and 22dB with the 2K ohm load resistor. The -1dB frequency of this

group of gain settings are between 298 to 310MHz. The gain accuracy of this group of gains is all below 0.73dB derivation from the ideal DC gain values, and this is tolerable because it is still fall below the minimum gain step (2dB/step) of the VGA.

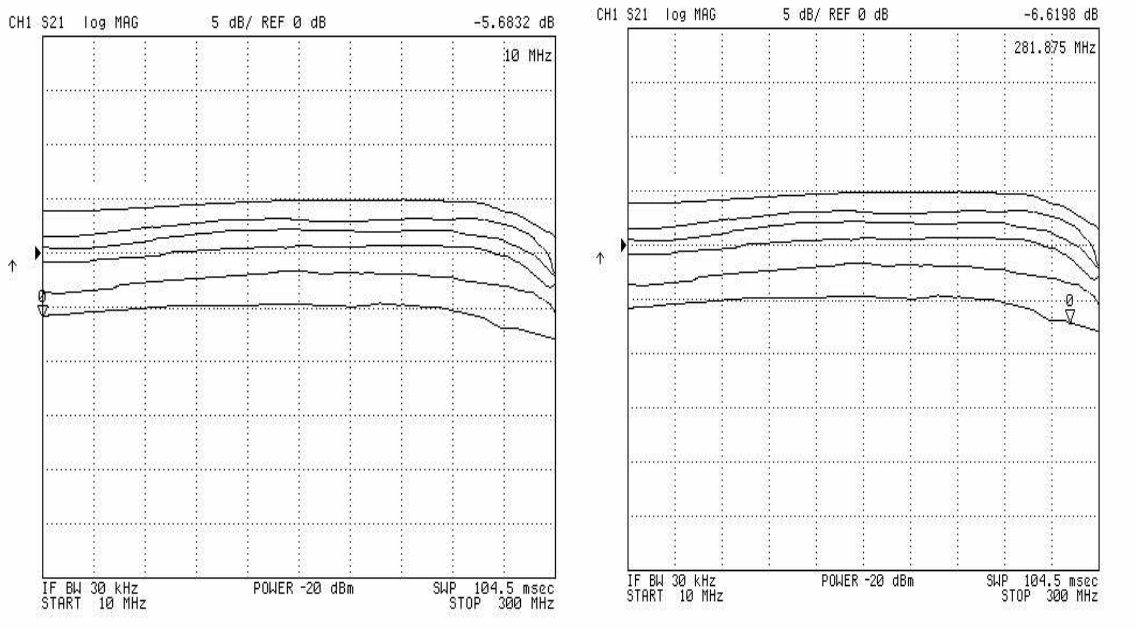


Fig 5.15 Gain setting of 4, 2, 0, -2, -4, and -6dB

The measurement results from the frequency response with the gain settings of -8, -10, -12, -14, -16, and -18dB with a 100 ohm load resistor are shown in Fig 5.16, and they correspond to 20, 18, 16, 14, 12, and 10dB with the 2K ohm load resistor. Their f_{-1dB} frequency of this group of gain settings is between 305 to 315MHz, which is higher than the rest gain settings because this is a low gain-stage group. Table 5.5 also shows that the gain accuracy is below the 0.7dB derivation from the ideal DC gain values, which is higher than the rest of the gain settings because this is a low gain-stage group.

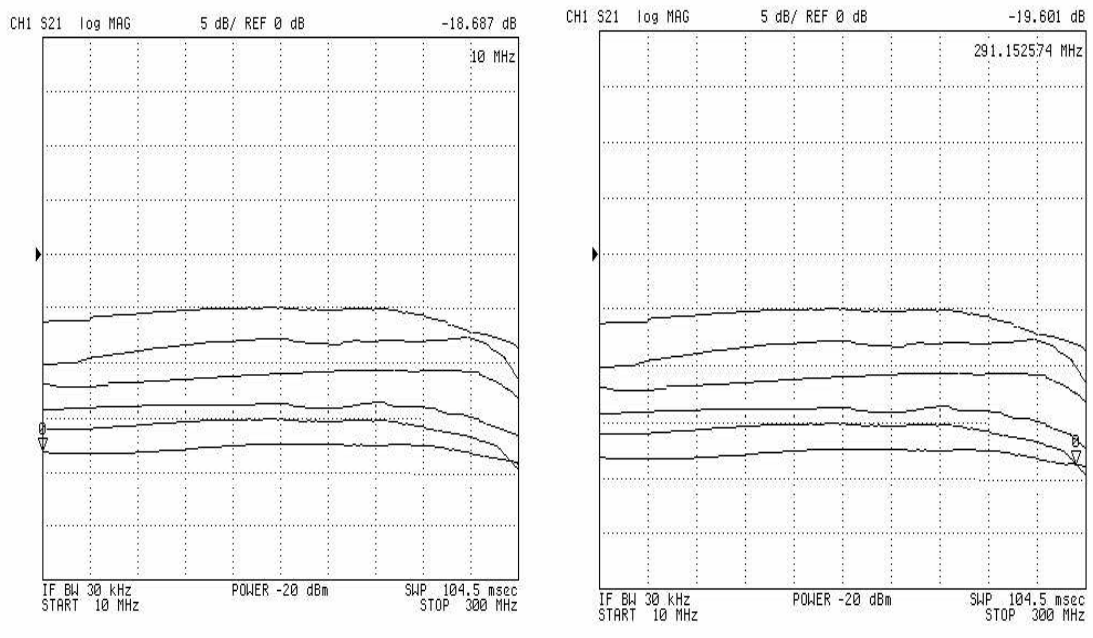


Fig 5.16 Gain setting of -8, -10, -12, -14, -16, and -18dB

We couldn't accurately measure the rest of the gain settings between -26 to -20dB with a load resistor 100 ohm, which correspond to 0 to 8dB with load resistor of 2K ohm. One reason is that the chip included this VGA design has a malfunction in its ESD protection pins, its ESD_VDD and ESD_GND are shorted together. This mistake severely limits the control voltage range of the digital control circuit to be less than two times the diode's forward bias voltage (about 1.4V). In a result, some of gain stages may miss if the digital circuit can not be fully turned on or off.

The measured frequency response of the maximum and minimum gain steps are shown in Figs 5.17 and 5.18 respectively.

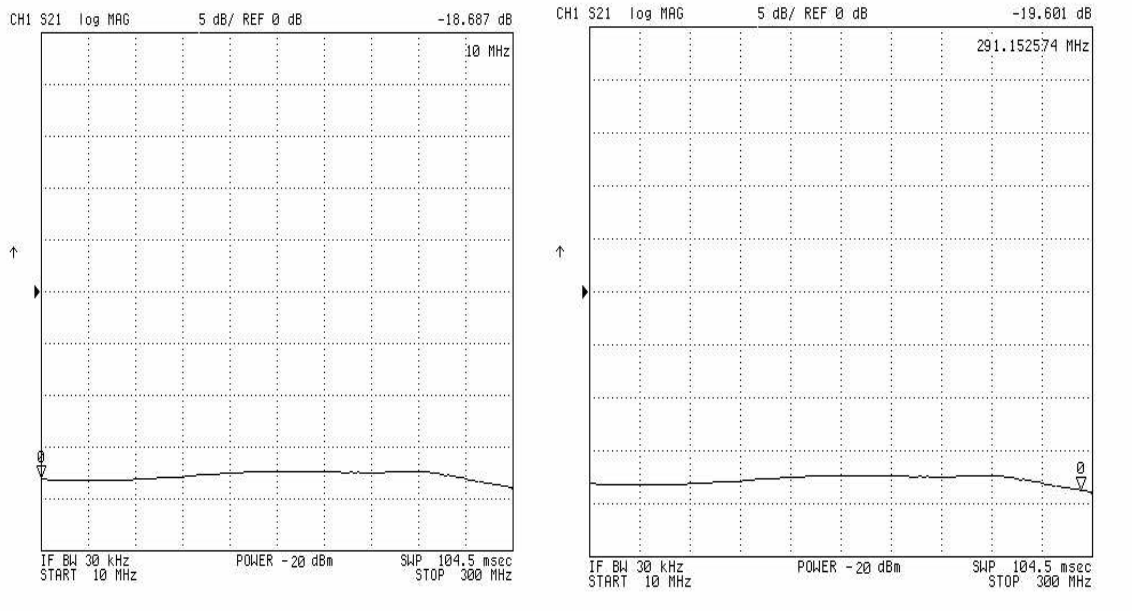


Fig 5.17 Gain setting of -18dB: Av(0) = -18.687dB, f_{-1dB} = 291.15MHz

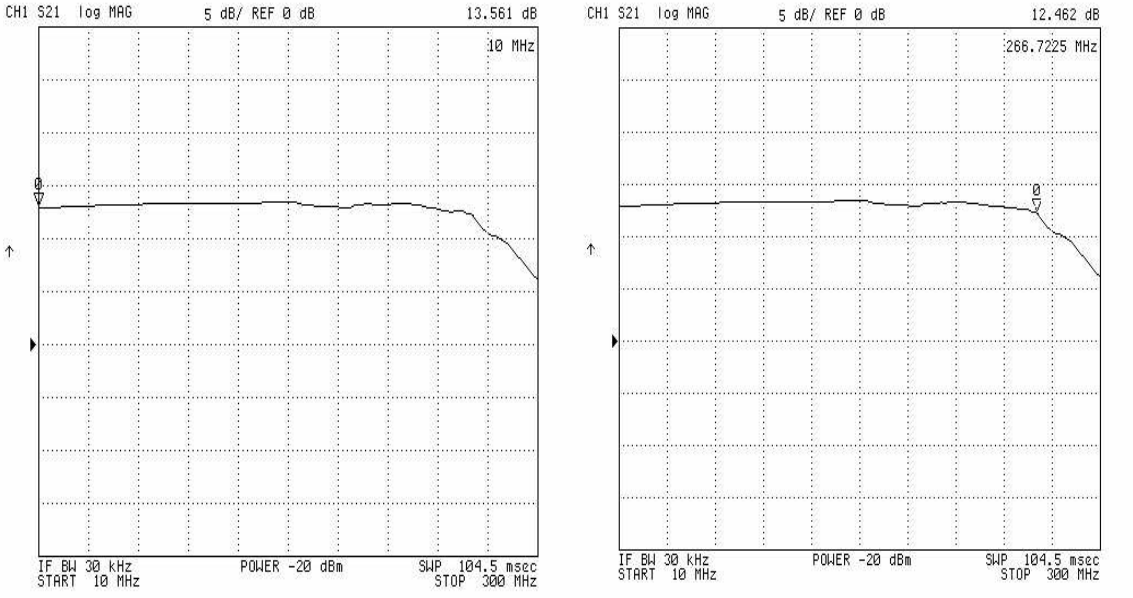


Fig 5.18 Gain setting of 14dB: Av(0) = 13.561dB, f_{-1dB} = 266.7MHz

V.4.2 Experimental results of the IIP3

To measure the IIP3, the two-tone test is performed with one tone at 240MHz and the other at 260MHz. By sweeping the input signal's power level, two sets of data are recorded. One set of data is for the output power level of the fundamental tone (at 240 and 260MHz), and the other set of data is for the output power level of the third harmonic (at 220 and 280MHz) due to the intermodulation of the input two tones. By recording several of those data at different input power level, the curve of the power levels of the fundamental tones and the third harmonic tones changing along the varied input signals can be obtained. Hence, using a straight line to interpolate these two curves, the intersection point of the two curves can be found. The corresponding input signal power level is the IIP3. The whole procedure is illustrated in Fig 5.19.

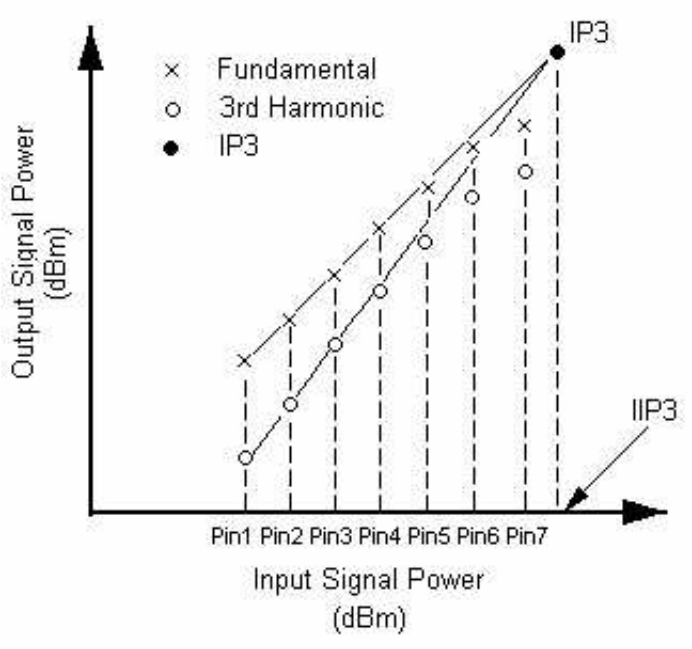


Fig 5.19 Measure IIP3 with interpolation

According to this measurement procedure, the IIP3 of different gain stages are obtained as shown in Fig.5.19. The measured IIP3 of the maximum and minimum gain steps are summarized in Table 5.6. Notice that, the balun (transformer) loss is about 2dB, and the loss from the wire and connectors of the spectrum analyzer is about 6dB, so the total loss is 8dB. We need to deduct this amount from IIP3 calculation. The post-layout simulation results are shown in Fig 5.20 to compare with the experimental results.

Table 5.6 IIP3 testing results

Pin(dBm)	-10	-8	-6	-4	-2	0	IIP3(dBm)	Gain(dB)
1st	-36	-33.7	-31.8	-30	-28.3	-26.7	8	-18
3rd	-72	-66	-60.1	-54.8	-49.2	-44.8		
Pin(dBm)	-24	-22	-18	-16	-14	-12	IIP3(dBm)	Gain(dB)
1st	-18.7	-16.89	-14.9	-13	-11.2	-9.5	-12.5	14
3rd	-41.77	-35.85	-29.9	-24.1	-19.4	-14.9		

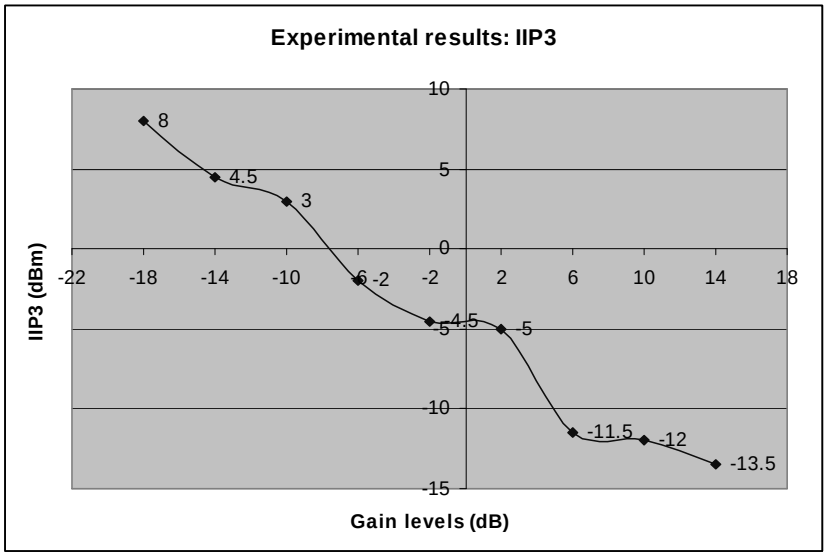


Fig 5.20 Testing results of IIP3 vs. gain levels

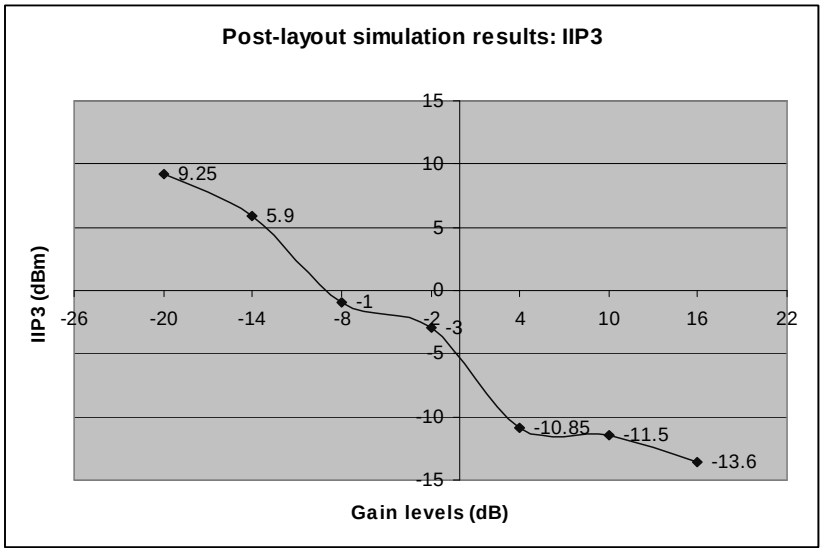


Fig 5.21 Post-layout results of IIP3 vs. gain levels

For the VGA gain range from -18 to 14dB, the IIP3 is from 8 to -13.5dBm, as illustrated in Fig 5.21. Comparing Figs 5.20 and 5.21, the experimental results show that there are about 1 ~ 2dBm loss in IIP3 from its post-layout simulation results. Overall, for all gain steps, their IIP3s are all above -14dBm, which is enough for the system requirement of IIP3 > -15dBm for all gain steps.

V.4.3 Noise characterization

Low noise is an important concern if the input signal is very small and the bandwidth of interest is very wide. Since we are interested in a very high frequency (up to 250MHz), the contribution from the 1/f noise at a lower frequency can be neglected. In this measurement, the spectrum analyzer collects the noise power within the Resolution Bandwidth (RBW). The noise power per Hz at the output, $\overline{v}_{no}^{2}$, is obtained by

dividing the noise power on the spectrum analyzer, $\bar{v}^2_{n,spectrum}$, by the RBW; hence the noise power per Hz is

$$\bar{v}^2_{no} = \frac{\bar{v}^2_{n,spectrum}}{RBW} \tag{5.11}$$

In a further step, the Noise Figure can be calculated in equation 5.8 as demonstrated in previously,

$$NF = 10 \cdot \log\left(1 + \frac{IN^2}{4kTR_s \cdot BW}\right) \tag{5.8}$$

where IN is short for Integrated Input Referred Noise Voltage

Given that in the measurement, RBW = 1MHz, and with equation 5.11, it yields

$$IN^2 = \frac{\bar{v}^2_{no} \times BW}{A_v(0)^2} = \frac{\left(\frac{\bar{v}^2_{n,spectrum}}{1MHz}\right) \times 250MHz}{A_v(0)^2} \tag{5.12}$$

Also, it can be also found that, with Rs = 50Ω, BW = 250MHz, 4kTRs×BW = 1.96×10^{-10} V^2. Substitute this result into equation 5.12 yields

$$NF = 10 \cdot \log\left(1 + \frac{\bar{v}^2_{n,spectrum} \times 250}{A_v(0)^2 \times 1.96 \times 10^{-10}}\right) \tag{5.13}$$

With equation 5.12, the Noise Figure for each gain stage based on the noise power output measurement result from the spectrum analyzer can be obtained. The measured output noise power from the spectrum analyzer of the maximum and minimum gain steps are shown in Figs 5.22 and 5.23.

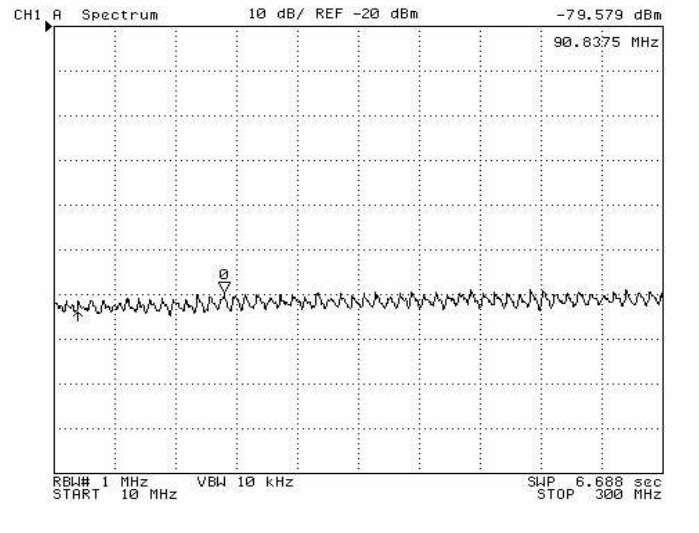


Fig 5.22 $A_v(0)$ = 14dB, equivalent output noise level = -79.6dBm, NF = 14.8dB

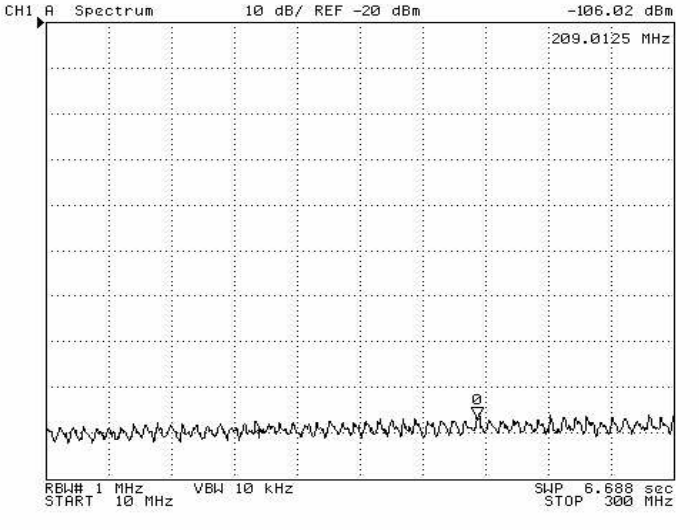


Fig 5.23 $A_v(0)$ = -18dB, equivalent output noise level = -106dBm, NF = 20.53dB

With the output noise power for different gain stages measured, using equation 5.13, the Noise Figure for different gain settings can be calculated. A comparison of

Noise Figure results from the measurement with those from the post-layout simulation is shown in Fig 5.24.

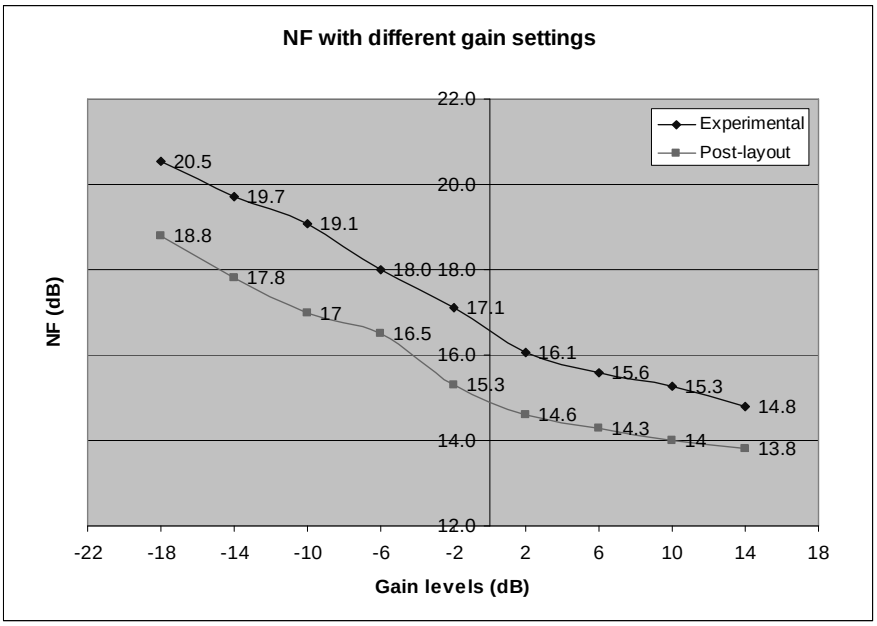


Fig 5.24 Noise Figure (NF): experimental result vs. post-layout simulation results

As seen in Fig 5.24, the Noise Figure varies from 14.8dB to 20.5dB for all gain settings, and they all fall in the required range of the system design specifications, which is less than 25dB for all gain cases. Because the noise performance is a more important concern in the very small input signal cases as mentioned before, the noise figure at the maximum gain setting—14dB—should be guaranteed to be lower than the requirement. The testing results show that the noise figure at the maximum gain is much below the requirement of NF < 25dB. For the lower gain cases, even though the noise figure is degraded, and the VGA introduces more noise into the signal it processing, the input

signal levels are relatively higher and are more immune to the noise than the very small signal level at the high gain cases. So, from the system design point of view, as long as they are all below the required noise level, the degradation of noise performance in the lower gain cases is still tolerable,.

Comparing the experimental results with post-layout simulation results, the experimental results deviate from the simulation by about 1 ~ 2dB, which again indicates the IBM 6HP design-kit has a relatively accurate model on the noise performance of the circuit.

V.5 Summary of results and comparison

As mentioned, comparing the Figure of Merit (FOM) of all the references with this work is a more fair approach to compare the overall performance of these VGAs because it includes the maximum gain range, -3dB bandwidth, signal-to-noise-ratio (SNR) and the power consumption performance altogether.

$$FOM = \frac{A_{V,MAX}(0) \times f_{-3dB} \times \text{SNR} \times \text{Technology}}{\text{Power} \times \text{Area}} \tag{5.10}$$

Notice that the commonly used units for each specification are different from the International Standard Unit, for example, $A_{V,MAX}(0)$'s unit is dB. So, when calculating the FOM, all the specifications are converted into the International Standard Unit. Finally, as the FOM will be a very large number if it is still in the International Standard Unit, it can be expressed in dB instead. Table 5.7 and Figure 5.25 illustrate the results.

Table 5.7 Figure of Merit (FOM) comparison

	$A_{V,MAX}(0)$ (dB)	f-3dB (MHz)	SNR (dB)	Power (mW)	Technology	Area (mm^2)	FOM (dB)
[4]	40	495	12.65	54	0.35µm CMOS	0.15	259
[8]	11	380	35	64	0.25 µm CMOS	2	223
[9]	34	2000	35	40	0.18 µm CMOS	0.7	271
This work	42	425	30	9.5	0.25 µm CMOS	0.015	310

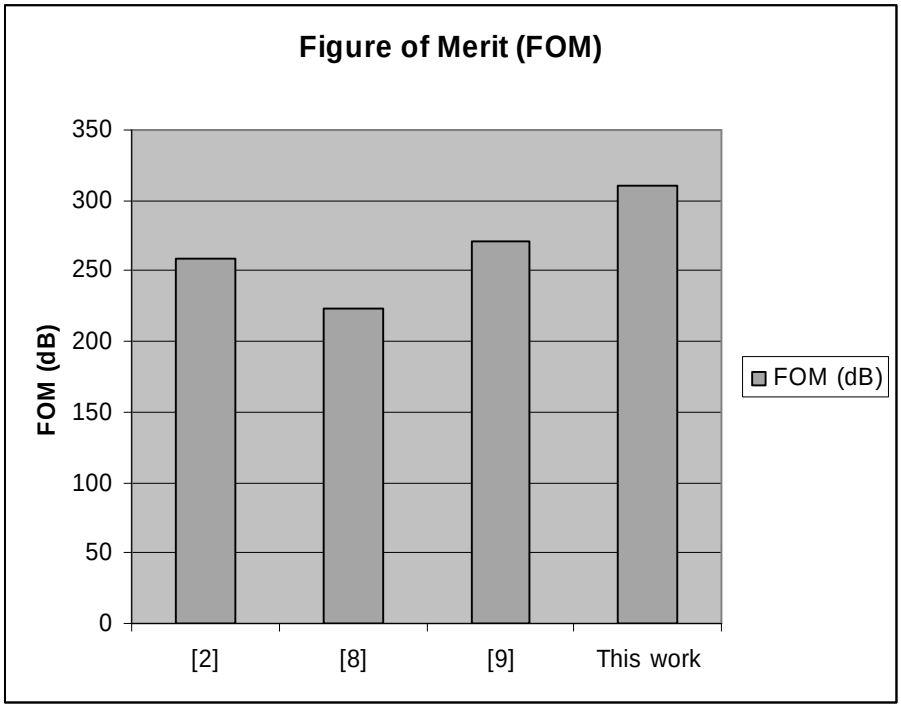


Fig 5.25 Figure of Merit (FOM) comparison

Fig 5.25 shows that this work has the highest Figure of Merit, mainly due to the highest maximum gain, largest bandwidth, and lowest power consumption among the VGAs in that comparison.

In summary, from the experimental results and comparing with the state-of-the-art VGA designs in the literature, the proposed VGA posses: (1) Comparable gain variable range and the smallest gain steps; (2) Comparable bandwidth with other designs; (3) Occupies the smallest area; (4) Has the best power consumption among all designs; (5) Comparable or better than other designs in linearity and noise performance.

CHAPTER VI

CONCLUSION

A fully differential CMOS Variable Gain Amplifier (VGA) consisting of complementary differential pairs with source degeneration, current gain stage with programmable current mirror, and resistor loads is designed for high frequency and low power communication applications, such as UWB receiver system. The gain can be programmed from 0 to 42dB of 2dB/step with -3dB bandwidth greater than 425MHz for all range of gain. The Third-Order Input Intercept Point (IIP3) is above -7dBm for $1V_{pp}$ differential input and output voltages. These low distortion broadband features are benefited from the large linear range of the differential pair with source degeneration and the low impedance internal nodes in the current gain stages. In addition, common-mode feedback is not required because of these low impedance nodes. Due to the power efficient complementary differential pairs as input stage, the power consumption is minimized (9.5mW) for all gain steps. The gain-control scheme includes of fine tuning (2dB/step) by changing the bias voltage of the proposed programmable current mirror, and coarse tuning (14dB/step) by switching on/off the source degeneration resistors in the differential pairs. Capacitive frequency compensation scheme is used to further extend the VGA bandwidth.

The VGA has been designed in the IBM 6HP 0.25μm CMOS processes. Experimental results demonstrated closed results as the post-layout simulation as expected.

This VGA topology, benefiting from its features such as ultra-low power consumption, small die area, large gain range and bandwidth, low distortions, can be broadly adopted into other immerging communication systems as well.

REFERENCES

[1] R. Gomez and A. A. Abidi, “A 50 MHz CMOS Variable Gain Amplifier for magnetic Data Storage Systems,” *IEEE Journal of Solid-State Circuits*, vol.35, no.6, pp.935-939, Jun. 1992.

[2] R. Gomez and A. A. Abidi, “A 50 MHz Variable Gain Amplifier Cell in 2μm CMOS,” in *Proc. IEEE Custom IC Conference*, May 1991, pp.9.4.1-9.4.4.

[3] T.-W. Pan and A. A. Abidi, “A 50dB Variable Gain Amplifier Using Parasitic Bipolar Transistors in CMOS,” *IEEE Journal of Solid-State Circuits*, vol.24, no.4, pp.951-961, Aug. 1989.

[4] S.T Tan, and J. Silva-Martinez, “A 270 MHz, 1Vpk-pk, Low-Distortion Variable Gain Amplifier in 0.35μm CMOS Process,” *Analog Integrated Circuits and Signal Processing*, vol.38, no.2, pp.307-310, Feb.2004.

[5] Y. Zheng, J. Yan, and Y. Xu, “A CMOS dB-Linear VGA with Pre-Distortion Compensation for Wireless Communication Applications,” in *Proc. International Symposium on Circuits and Systems*, May 2004, vol.1, pp.813-816.

[6] A. Thanachayanont and P. Naktongkul, “Low-Voltage Wideband Compact CMOS Variable Gain Amplifier,” *Electronics Letters*, vol. 41, no. 2, pp.51-52, Jan. 2005.

[7] J. Silva-Martinez, J. Adut, J. M. Rocha-Perez, M. Robinson and S. Rokhsaz, “A 60mW 200 MHz Continuous-Time Seventh-Order Linear Phase Filter with On-Chip

Automatic Tuning System," *IEEE Journal of Solid-State Circuits*, vol. 38, no.2, pp.216-225, Feb. 2003.

[8] O. Watanabe, S. Otaka, M.Ashida, and T. Itakura, "A 380MHz CMOS Linear-in-dB Signal-Summing Variable Gain Amplifier with Gain Compensation Techniques for CDMA Systems," in *VLSI Circuits Digest of Technical Papers*, Jun. 2002, pp.136-139.

[9] C.-H. Wu, C.-S. Liu and S.-L. Liu, "A 2 GHz CMOS Variable Gain Amplifier with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet," in *IEEE International Solid-State Circuits Conference*, vol. 1, Feb. 2004, pp.584-541.

APPENDIX A

DETERMINE THE DIMENSIONS FOR THE PROGRAMMABLE CURRENT MIRROR

In this appendix, it will be shown how equation (3.12) is obtained.

Let us make some assumptions and observations (as shown in Fig 3.4.)

(1) Assume, M_1 and M_2 have identical dimensions while that of M_3 is $W/(ML)$

(2) Make an equivalent transistor for all the transistors turned on in the bias control circuit, call it M_b with dimension $W/(NL)$.

(3) Assume that the bias current for the bias control circuit is correlated to that of the programmable current mirror. Set I_{bias} for the current mirror, then $I_{ref} = K \times I_{bias}$ in the bias control circuit, where K is a constant current gain factor.

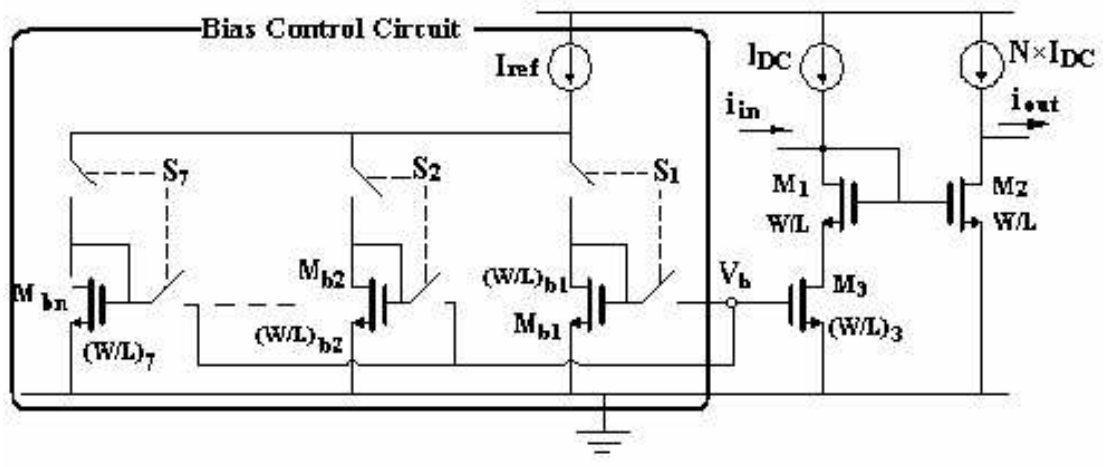


Fig A.1 Bias Transistors to generate seven gain steps for programmable current mirror

First, notice that $V_{GS1} + V_{DS3} = V_{GS2}$ then $V_{DSAT1} + V_{DS3} = V_{DSAT2}$, where $V_{DSAT} = V_{GS} - V_{th}$. Since M_1 and M_b operate in the saturation region while M_3 operates in the triode region, their drain-source currents are given by

$$\begin{aligned} I_{D1} &= \frac{1}{2}\mu_n C_{OX} \frac{W}{L} V_{DSAT\,1}{}^2 \left[1 + \lambda (V_{DS\,1} - V_{DSAT\,1})\right] \\ I_{D3} &= \mu_n C_{OX} \frac{W}{ML}\left(V_{DSAT\,3} V_{DS\,3} - \frac{V_{DS\,3}{}^2}{2}\right) \\ I_{ref} &= \frac{1}{2}\mu_n C_{OX} \frac{W}{NL} V_{DSATb}{}^2 \left[1 + \lambda (V_{DSb} - V_{DSATb})\right] \end{aligned} \tag{A.1}$$

From Fig 3.9,

$$\because V_{DS1} - V_{DSAT1} = V_{DS1} - V_{GS1} + V_{th} = V_{th} \quad \therefore I_{D1} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{DSAT2} - V_{DS3})^2 [1 + \lambda V_{th}] \tag{A.2}$$

$$\because V_{DSAT\,3} = V_{DSATb} \ \therefore I_{ref} = \frac{1}{2}\mu_n C_{OX} \frac{W}{NL} V_{DSAT\,3}{}^2 \left[1 + \lambda V_{th}\right] \tag{A.3}$$

$$I_{ref} = K * I_{D1} = K * I_{D3} \tag{A.4}$$

Combining equation A3.1, A3.3, and A3.4, we obtain

$$\begin{aligned} &\frac{K}{M}\left(V_{DSAT3} V_{DS3} - \frac{V_{DS3}{}^2}{2}\right) = \frac{1}{2N} V_{DSAT3}{}^2 \Rightarrow V_{DS3}{}^2 - 2V_{DSAT3} V_{DS3} + \frac{M}{NK} V_{DSAT3}{}^2 = 0 \\ &\Rightarrow V_{DS3} = V_{DSAT3}\left(1 - \sqrt{\frac{N - (M/K)}{N}}\right) \end{aligned} \tag{A.5}$$

Combining equation A3.2, A3.3, and A3.4, we obtain

$$K(V_{DSAT\,2} - V_{DS\,3})^2 = \frac{1}{N} V_{DSAT\,3}{}^2 \Rightarrow V_{DSAT\,2} - V_{DS\,3} = \frac{1}{\sqrt{NK}} V_{DSAT\,3} \tag{A.6}$$

Substituting equation A3.5 into A3.6, we have

$$V_{DSAT\,2} = V_{DSAT\,3}\left(1 + \frac{1}{\sqrt{KN}} - \sqrt{\frac{N - (M/K)}{N}}\right) \tag{A.7}$$

The low frequency current gain of programmable current mirror is given by

$$\frac{i_{out}}{i_{in}} = \frac{V_{DSAT\ 2}{}^{2}}{\left(V_{DSAT\ 2} - V_{DS\ 3}\right)^{2}} \tag{A.8}$$

Substituting equation A3.6 and A3.7 into A3.8, yields

$$\frac{i_{out}}{i_{in}} = \left(\sqrt{NK} + 1 - \sqrt{NK - M}\right)^{2} \tag{3.12}$$

Where $M = \frac{(W/L)_1}{(W/L)_3}$, $N = \frac{(W/L)_1}{(W/L)_b}$, $K = \frac{I_{ref}}{I_{bias}}$

Therefore, the low frequency current gain of the programmable current mirror is a function of the aspect ratios of M_1, M_3 and M_b, and the ratio between I_{ref} and I_{bias}. In the approach used in this design, $(W/L)_1, (W/L)_3, I_{ref}/I_{bias}$ are all fixed. By varying $(W/L)_b$, different current gains can be obtained.

APPENDIX B

THE DIMENSIONS AND CURRENT BIAS FOR THE VGA

1) Calculation of the load resistance

As -3dB frequency (f_{-3dB})>350MHz, to leave some margin, choose f_{-3dB} = 400MHz. From this, we can estimate the output resistance we need. $f_{-3dB} = 1/(R_{out}C_{out})$. As we use current mirror connecting to the output resistor, their parasitic capacitor determines C_{out}, which would be quite small. Assuming the maximum parasitic is $0.2pF$, and then we can find R_{out} as

$R_{out} = 1/(2\pi \times 4 \times 10^{8} \times 0.2 \times 10^{-12}) = 1.99K\Omega$, so choose R_{out} =1 .5KΩ.

2) Calculation of the source degeneration resistance Ω

Because we need 14dB between adjacent coarse tuning steps, which corresponds to 5 times of amplification, we can calculate the maximum transconductance of input stage as

$G_{m,\max} \times 5 \times 1.5K = 42dB = 126 \quad \Rightarrow G_{m,\max} = 16.8m$

Then connect the source degeneration resistor to get a $14dB$ lower gain than the maximum gain. From equation 4.5

$$G_m = \frac{g_{mn}(1+\sqrt{\mu_p/\mu_n})}{1+0.5R_{sn}g_{mn}} = \frac{16.8m}{5} = \frac{1.4g_{mn}}{1+0.5R_{sn}g_{mn}}$$

Also $g_{mn}/g_{mp} = \sqrt{\mu_n/\mu_p}$ and $R_{sn}g_{mn} = R_{sp}g_{mp}$

$$\Rightarrow R_{sn} \approx 600\Omega,\ R_{sp} \approx 900\Omega \qquad \text{(B.1)}$$

$$\Rightarrow 2R_{sn2} = 600\Omega,\ \ 2R_{sp2} = 900\Omega$$

$$\Rightarrow R_{sn2} = 300\Omega,\ R_{sp2} = 450\Omega$$

Finally for the last coarse tuning steps, another 14dB gain reduction is needed.

$$G_m = \frac{g_{mn}(1+\sqrt{\mu_p/\mu_n})}{1+0.5R_{sn}g_{mn}} = \frac{16.8m}{5\times 5} = \frac{1.4g_{mn}}{1+0.5R_{sn}g_{mn}}$$

Also $g_{mn}/g_{mp} = \sqrt{\mu_n/\mu_p}$ and $R_{sn}g_{mn} = R_{sp}g_{mp}$

$$\Rightarrow R_{sn} \approx 3.6K\Omega,\ R_{sp} \approx 5.4K\Omega \qquad \text{(B.2)}$$

$$\Rightarrow 2R_{sn2} + R_{sn1} = 3.6K\Omega, 2R_{sp2} + R_{sp1} = 5.4K\Omega$$

$$\Rightarrow R_{sn1} = 3K\Omega,\ R_{sp1} = 4.5K\Omega,$$

3) Calculation of the dimensions and bias current of the input stage

Because we adapt Approach II as mentioned previously to choose the same dimensions for both differential pairs, the overall transconductance is given by

$$G_m = \frac{g_{mn}\left(1+\sqrt{\mu_p/\mu_n}\right)}{1+N_n} = \frac{1.4g_{mn}}{1+N_n} \qquad \text{(B.3)}$$

For the maximum gain setting, equation G_m reduces into

$$G_m = g_{mn}\left(1+\sqrt{\frac{\mu_p}{\mu_n}}\right) = 1.4g_{mn} = 16.8m \quad \Rightarrow g_{mn} = 12m$$

To further calculate the dimension and bias current of the input stage, we have to determine $V_{DSAT,\ Mn}$, $V_{DSAT,\ Mp}$. And this has to meet three different cases V_{DSAT} requirements, a) high gain range (28 ~ 42*dB*), b) middle gain range (14 ~ 26*dB*), and c) low gain range (0 ~ 12*dB*).

a) 28 ~ 42dB

To accommodate the $1V_{pp}$ differential output signal requirement, with 28*dB* gain, it corresponds to a $39.9mV_{pp}$ input signal. So in this case, we have to make V_{DSAT} >40*mV*.

b) 14 ~ 26dB

With 14dB gain, $1V_{pp}$ differential output signal corresponds to a $200mV_{pp}$ input signal. As the source degeneration resistor is included, which relaxes V_{DSAT} by (1+*N*) times, *N* = 4, so the V_{DSAT} requirement will be $200mV_{pp}/(1+4) = 40mV$.

c) 0 ~ 12dB

With 0dB gain, the required output signal corresponds to a $1V_{pp}$ input signal. With source degeneration, N = 24 in this case, so the V_{DSAT} requirement will be $1V_{pp}/(1+24) = 40mV$

Overall, from the above three cases, with some margin, we set $V_{DSAT,Mn}$= 150mV

$$g_{mn} = 2I_{bias} / V_{DSAT,Mn} = 12m, V_{DSAT,Mn} = 150mV \Rightarrow I_{bias} = 400uA$$

$$\text{Alsobecause } g_{mn} = \mu_n C_{OX} (W/L)_n V_{DSAT,Mn}, \text{ for IBM6HP technology, } \mu_n C_{OX} \approx 232uA/V^2$$

$$\Rightarrow (W/L)_n = (W/L)_p = 345, L = 0.24um$$

$$\Rightarrow W_n = W_p = 78um$$

4) Calculation of the Dimensions of the Programmable Current Mirror

Because the VGA is needed to handle a $1V_{pp}$ differential output signal, the single-ended signal at the output will be $0.5V_{pp}$. With 1.5K load resistor, the AC current

at output will be 0.5/1500 = 0.33mA. As a rule of thumb, to accommodate this AC current, we must have 3 times larger DC current, which is 1mA. With maximum current gain of 5, the single ended DC current at the input of the current mirror will be 1mA/5 =0.2mA. Choose 220μA to leave some margin.

For the V_{DSAT} of the current mirrors, choose V_{DSAT} = 150mV to prevent linearity degradation from the current mirror stage. Now we can calculate the dimensions of the current mirrors

$$I_{bias} = 220uA, V_{DSAT} = 150mV$$

$$I_{bias} = \frac{1}{2}\mu_n C_{OX} (W/L)_n V_{DSAT,Mn}{}^2$$

for IBM6HP 0.25um Technology, $\mu_n C_{OX} \approx 232uA/V^2$

$$\Rightarrow (W/L)_n = (W/L)_p = 100, L = 0.24um$$

$$\Rightarrow W_n = W_p = 24um$$

The dimensions of the programmable current mirror are given in Table B.1.

Table B.1 Dimension of the bias circuits

N	1.01	1.05	1.2	1.4	1.8	3	5.6
Current Gain (dB)	14	12	10	8	6	4	2
W_b (W_1=24μm)	23.6	21.6	16.8	12	7.2	2.4	0.72
	M_{b1}	M_{b2}	M_{b3}	M_{b4}	M_{b5}	M_{b6}	M_{b7}
W	2 μm	4.8 μm	4.8 μm	4.8 μm	4.8 μm	1.68 μm	0.72 μm
L	0.24 μm						

At the end, we can roughly calculate the power consumption of this VGA.

VITA

Lin Chen

Texas Instruments,
MS 8749
12500 TI Blvd,
Dallas, Texas 75243

Education
M.E. in Mechanical Engineering, Cornell University, Ithaca, New York, May 2001
B.E. in Automotive Engineering, Tsinghua University, Beijing, China, July 2000