# AN ANALOG APPROACH TO INTERFERENCE SUPPRESSION IN ULTRA-WIDEBAND RECEIVERS

A Dissertation

by

TIMOTHY W. FISCHER

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2007

Major Subject: Electrical Engineering

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# ABSTRACT

An Analog Approach to Interference Suppression in Ultra-Wideband Receivers.

(May 2007)

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Chair of Advisory Committee: Dr. Aydın Karşılayan

Because of the huge bandwidth of Ultra-Wideband (UWB) systems, in-band narrowband interference may hinder receiver performance. In this dissertation, sources of potential narrowband interference that lie within the IEEE 802.15.3a UWB bandwidth are presented, and a solution is proposed. To combat interference in Multi-Band OFDM (MB-OFDM) UWB systems, an analog notch filter is designed to be included in the UWB receive chain. The architecture of the filter is based on feed-forward subtraction of the interference, and includes a Least Means Squared (LMS) tuning scheme to maximize attenuation. The filter uses the Fast Fourier Transform (FFT) result for interference detection and discrete center frequency tuning of the filter. It was fabricated in a 0.18 $\mu$m process, and experimental results are provided. This is the first study of potential in-band interference sources for UWB. The proposed filter offers a practical means for ensuring reliable UWB communication in the presense of such interference.

The Operational Transconductance Amplifier (OTA) is the predominant building block in the design of the notch filter. In many cases, OTAs must handle input signals with large common mode swings. A new scheme for achieving rail-to-rail input to an OTA is introduced. Constant $g_m$ is obtained by using tunable level shifters and a single differential pair. Feedback circuitry controls the level shifters in a manner that fixes the common mode input of the differential pair, resulting in

consistent and stable operation for rail-to-rail inputs. As the new technique avoids using complimentary input differential pairs, this method overcomes problems such as Common Mode Rejection Ratio (CMRR) and Gain Bandwidth (GBW) product degradation that exist in many other designs. The circuit was fabricated in a $0.5\mu m$ process. The resulting differential pair had a constant transconductance that varied by only $\pm 0.35\%$ for rail-to-rail input common mode levels. The input common mode range extended well past the supply levels of $\pm 1.5$V, resulting in only $\pm 1\%$ fluctuation in $g_m$ for input common modes from -2V to 2V.

To Tiffany, Dylan, and those yet to be named

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# CHAPTER I

# INTRODUCTION

## A. Background

In 2003, the FCC opened the 3.1–10.6 GHz frequency band for ultra-wideband UWB communication under the restriction that the average transmit power does not exceed $-41.3$ dBm/MHz, which is the existing limit set for unintentional radiation of class-B electronic devices [1]. In response, the IEEE formed the 802.15.3a working group and began accepting proposals on how to best utilize this bandwidth. Two modulation formats emerged as the leading candidates for becoming the 802.15.3a standard. One of these is Direct-Sequence Code Division Multiple Access (DS-CDMA) [2], and is based on technology similar to PCS cellular systems. The second is Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) [3], and is an extension to the modulation format used in Asynchronous Digital Subscriber Lines (ADSL) and 802.11a Wireless Local Area Networks (WLAN). MB-OFDM seems to be the more popular of the two modulation formats, and has nearly gained the 75% industry approval required for becoming the 802.15.3a standard. This work is thus based on MB-OFDM, although it could be extended to any wideband modulation format.

### 1. OFDM Basics

Orthogonal Frequency Division Multiplexing (OFDM) [4–6] provides an efficient solution to wideband modulation. The entire allocated bandwidth, $B$, is divided into $N$ subchannels. Data is transmitted on these subchannels in parallel using a 2-Dimensional M-ary modulation format. Figure 1 displays the spectral content of an

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The journal model is *IEEE Transactions on Automatic Control*.

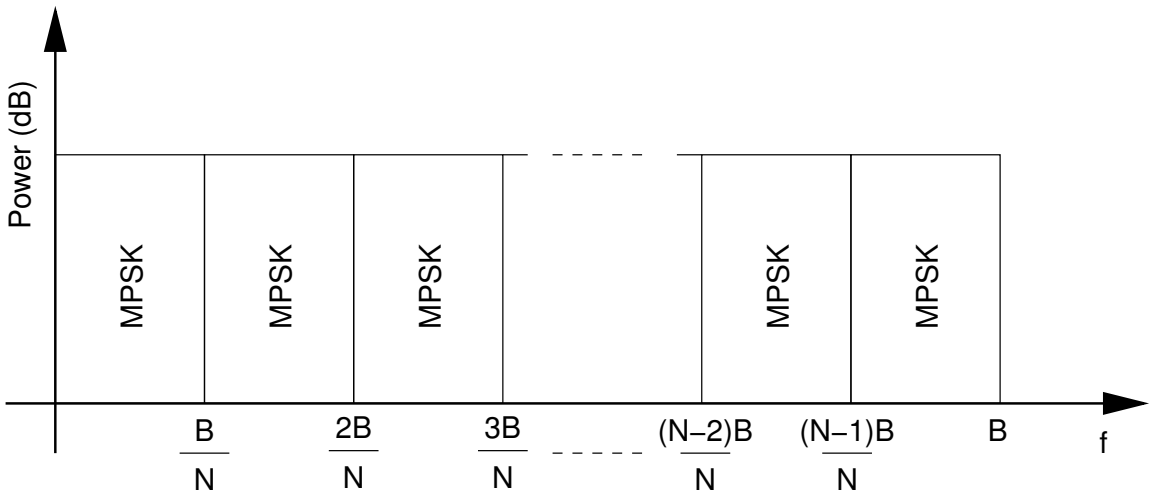



Fig. 1. OFDM using MPSK on N parallel subchannels.

OFDM system using M-ary Phase Shift Keying (PSK).

OFDM is spectrally encoded, and then converted to the time domain with an inverse Fast Fourier Transfer (iFFT) processor. Decoding is then performed with a Fast Fourier Transfer (FFT) processor.

## 2. MB-OFDM: Time and Frequency Interleaved OFDM

MB-OFDM is a method of extending OFDM to larger bandwidths. This is done by dividing the bandwidth into subbands, and then using OFDM modulation sequentially on each subband. Only one subband is active at any given time. The MB-OFDM proposal indicates that in the first phase, three subbands will be used with center frequencies 3432 MHz, 3960 MHz, and 4488 MHz [3]. Illustrated in Fig. 2, each subband will be active for the symbol period of 312.5 ns, after which a 9.5 ns guard interval will be allotted for the receiver to switch to the next subband, which then becomes active for the next symbol period. The entire MB-OFDM bandwidth is thus 1.584 GHz, but the instantaneous bandwidth is only 528 MHz. Since any one subband is only active for every third symbol, the transmit power can be three times

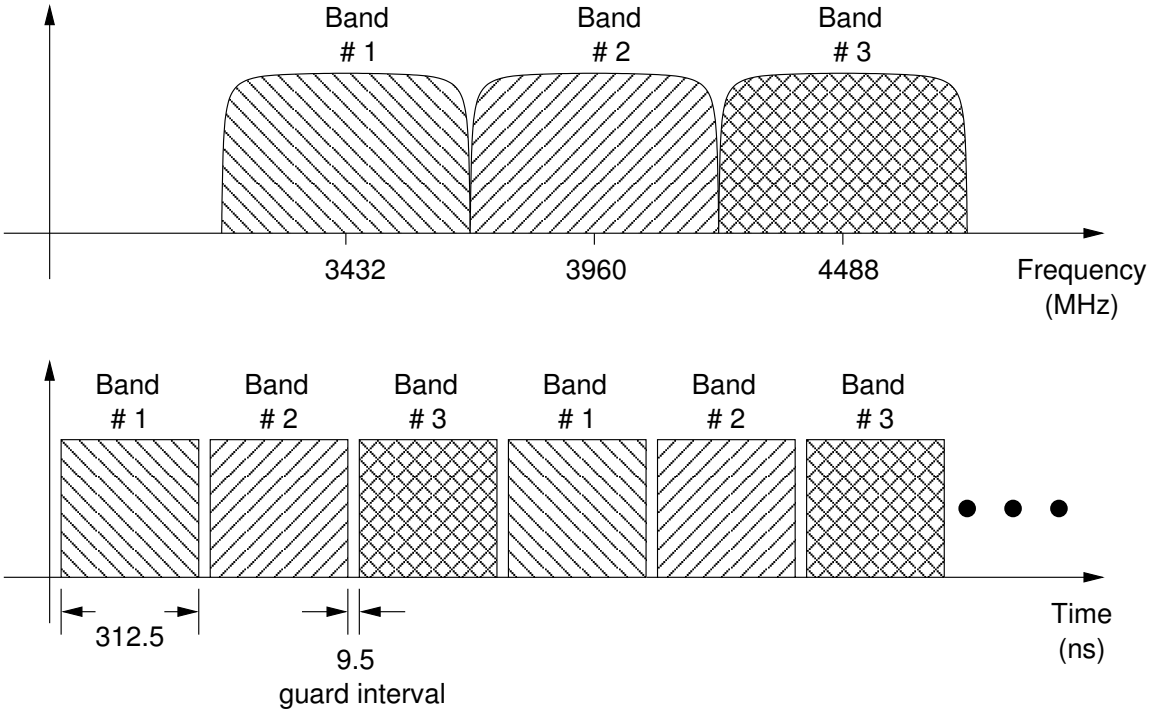



Fig. 2. MB-OFDM for 802.15.3a sequentially modulates OFDM on different RF carrier frequencies.

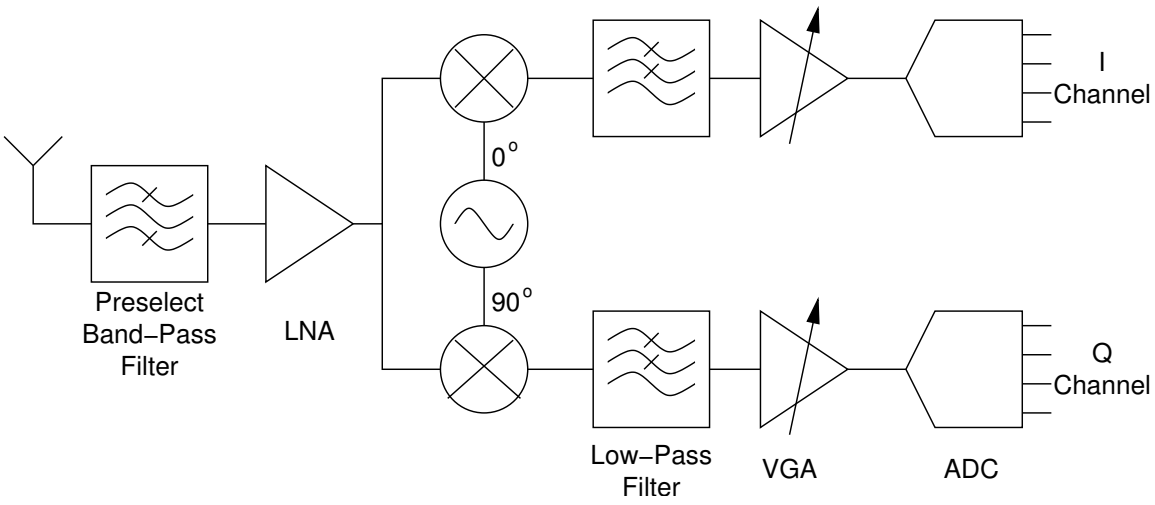



Fig. 3. Analog front end of a typical receiver.

larger while still satisfying the FCC regulations. An example analog front-end for an MB-OFDM receiver is shown in Fig. 3.

## B. Interference in UWB

Due to the huge bandwidth and low transmit power of UWB systems, radio interference could degrade receiver performance. Interference in UWB can be divided into two categories, out-of-band (OOB) and in-band. OOB interference sources include microwave ovens and existing communication standards, such as WLAN and WiFi. Because the frequencies of these interference sources are not in the UWB bandwidth they can be attenuated with RF surface acoustic wave (SAW) and baseband lowpass filtering without affecting the UWB data. On the other hand, the problem of in-band interference is not as well defined. This is partially due to the fact that sources of in-band interference have not been explored to the extent of the OOB interference sources. Since in-band narrow-band interference (NBI) has not been fully demonstrated as a problem, even less research has been focused on a solution.

## C. Research Goals

The aim of this work is twofold. First, a comprehensive collection of potential in-band NBI sources is provided, and an analysis is made on the effect of NBI on UWB systems. From this, it is evident that in-band NBI is a pressing problem in UWB systems that, if left ignored, could hinder transceiver performance. Second, a solution to this problem is provided. An adaptive analog notch filter is designed to reduce the effect NBI will have on UWB systems. The center frequency of the filter is controllable from near DC up to a few hundred megahertz. It employs an analog least mean square (LMS) tuning to maximize the attenuation. The complete design

procedure is provided, from specification development through device fabrication and experimental verification.

Furthermore, a scheme for achieving rail-to-rail input to an operational amplifier is presented. Constant $g_m$ is obtained by using tunable level shifters and a single differential pair. Feedback circuitry controls the level shifters in a manner that fixes the common mode input of the differential pair, resulting in consistent and stable operation for rail-to-rail inputs. As the new technique avoids using complimentary input differential pairs, this method overcomes problems such as CMRR and GBW degradation that exist in many other designs. The circuit was fabricated in AMI's $0.5\mu m$ process. The resulting differential pair had a constant transconductance that varied by only $\pm 0.35\%$ for rail-to-rail input common mode levels. The input common mode range extended well past the supply levels of $\pm 1.5$V, resulting in only $\pm 1\%$ fluctuation in $g_m$ for input common modes from -2V to 2V.

# CHAPTER II

# NARROWBAND INTERFERENCE: A PROBLEM FOR UWB

MB-OFDM for UWB communication was developed to coexist with current narrowband communication standards. The OFDM sub-bands are located such that interferences from IEEE 802.15.1, 802.11b, 802.11a, and 802.15.4 are out of band interferences, and can be adequately suppressed by the SAW and lowpass filters. However, interferences due to unintentional radiation of electronic devices may lie within the UWB bandwidth. There exist many potential interference sources that could hinder UWB communication. These range from computer components to common household devices such as electric shavers and hair dryers [7–9]. While the emission levels of any class-B compatible electronic device could legally have power levels of up to -41.3 dBm/MHz, those that reside closer to a potential UWB receiver, such as computer components, possess a higher probability for degrading UWB receiver performance. In this chapter, potential interference sources are explored, and their effect on MB-OFDM is analyzed.

## A. Potential In-band NBI Sources

Electro-magnetic compatibility (EMC) reports submitted to the FCC provide good sources for finding out what types of interference a UWB receiver might expect. For instance, in an EMC report provided to the FCC in 2004, measured radiation levels of a Local Area Network (LAN) Network Interface Card (NIC) indicate emissions of -49.8 dBm at 3.75 GHz [7]. In a separate report, emission levels of -44.3 dBm at 3.75 GHz were measured for a LAN switch [8]. The former is a PCI card for a personal computer (PC) that could reside within a few centimeters of a UWB

transceiver antenna. The latter is self-enclosed, but could still likely be placed near a PC, and hence, near a receiver. The center frequency in both cases is 3.75 GHz, which lies directly within the UWB bandwidth.

In a report to the FCC discussing potential interference sources for UWB communications, one of the examined devices was a computer motherboard [9]. Measured emissions indicate a tone around 1.9 GHz with a peak power of -36.7 dBm, and an average power of -42.7 dBm. Though this does not fall inside the UWB frequency band, it is close enough to cause concern. This report was created in 1999, and computers have only gotten faster. Thus, it is probable that today's motherboards radiate tones within the UWB spectrum, and with power very close to the FCC limit.

No EMC reports were found that provide emission levels for central processing units (CPUs). However, these also give rise to concern due to their clock rates. Current CPUs clock as fast as 3.8 GHz. In the cases of LAN NICs, LAN switches, and motherboards, the radiations are likely due to harmonics of the operating frequency. In the case of CPUs, however, the fundamental frequency lies directly within the UWB spectrum and could be expected to provide high emission levels.

Beyond personal computers, it also becomes necessary to examine the radiation levels of consumer electronics which may house a UWB transceiver, such as digital cameras, cell phones, and PDAs. In a smartphone currently on the market, a -43.9 dBm tone was measured at 1.87 GHz [10]. Though this is outside the UWB band, the measurements were only reported up to 2 GHz. Both the second and third harmonics of this tone exist in the UWB bandwidth, with unreported levels. Table I provides a summary of some of the potential interference sources found in EMC test reports provided to the FCC.

Furthermore, the above emission measurements were taken with the device under test inside a shielded PC chassis. Typical casings are known to attenuate emissions

Table I. Potential interference sources

| **Source** | $f_{int}$ | $P_{int}$ |
|---|---|---|
| LAN NIC [7] | 3.75 GHz | -49.8 dBm |
| LAN Switch [8] | 3.75 GHz | -44.3 dBm |
| Motherboard [9] | 1.9 GHz | -42.7 dBm |
| PDA [10] | 1.87 GHz | -43.9 dBm |

by greater than 25 dB [11]. This indicates power levels inside the chassis could exceed -16.3 dBm. Assuming one implementation of a UWB transceiver is marketed as a PCI peripheral, which is located inside the PC tower, these signals will couple to the receiver through the UWB packaging and circuit board.

## B. Power Levels of NBI at the Receiver

The MB-OFDM proposal provides some indication as to acceptable narrowband interference power levels. It states that reliable communication can occur as long as the SIR is greater than -8 dB for a generic in-band tone interferer [3]. Furthermore, the minimum received power of the UWB data signal is $P_{uwb}$ =-77.5 dBm, which is 6 dB above the sensitivity level for the 55 Mb/s data rate and is the measurement standard of the 802.15.3a working group [12]. This indicates that the maximum tolerable received interference power for this case is $P_{rint}$ =-69.5 dBm.

It is evident that some electronic devices radiate within the UWB bandwidth, and at power levels near the FCC limit. However, the power of the interference once it reaches the UWB antenna will have been attenuated due to path loss. The IEEE

802.15.3a channel modeling committee has provided a path loss model of :

$$P_L\left(f_g, d\right) = 20\log_{10}\left(\frac{4\pi f_g d}{c}\right), \tag{2.1}$$

where $P_L$ is the path loss in dB, $d$ is the distance from the source in meters, $c \approx 3 * 10^8$ m/s is the speed of light, and $f_g$ is the geometric average of the lower and upper corner frequencies [13]. In the case of NBI, $f_g$ can be approximated by the center frequency of the interference, $f_{int}$. The smallest path loss will occur at the lower end of the UWB spectrum, and is thus the case considered in the following analysis. As an example, consider the case where an interference source is radiating at 3.168 GHz with power at the FCC limit of $-41.3$ dBm. Furthermore, assume that a UWB receiver is operating at 55 MB/s with a received UWB signal power of -77.5 dBm. To achieve $SIR \geq -8$ dB, according to Eq. 2.1, the receive antenna would need to be at least 19.4 cm from the interference source. This may not be plausible considering the UWB receiver in many cases will be housed within the same device as the interference source.

Alternatively, consider the case above again, only fix the distance between the UWB antenna and the interference source to 5 cm, and let the power of the interference at its source vary. For $SIR \geq -8$ dB, the maximum tolerable radiated power of the interference would be -53 dBm. This is well below the legal limit set by the FCC. If an interference source is radiating at -41.3 dBm at a distance 5 cm from the UWB antenna, SIR would be -19.76 dB. In this case, the interference must be attenuated by more than 10 dB before reliable communication can occur.

## C. Effect of NBI on MB-OFDM

By examining emission reports for various electronic devices, it has been shown that it is quite possible for NBI to exist within the UWB bandwidth with power levels at or near the FCC limits. It now becomes necessary to determine the effect that NBI will have on the reliability of UWB communication. The threat that NBI poses to is two-fold. The first problem exists even for ideal receivers using floating point arithmetic and infinite full scale range and is a result of spectral leakage of the interference onto multiple OFDM tones in the FFT output. The second problem is a result of nonidealities in the receiver. For large interference, in order to prevent saturation of the ADC, the VGA gain is required to be set according to the interference power, which may leave the information signal buried under the quantization noise of the ADC.

### 1. Spectral Leakage of Interference onto Neighboring OFDM Tones

The effects of interference spectral leakage on MB-OFDB must be evaluated for both the case of a single tone interference and a narrow-band interference. The effects will be different depending on the frequency of the interference. The case with the least spectral leakage is when the interference falls directly on one of the OFDM sub-carriers. In this case, a single tone interference will display no spectral leakage. An interference with non-zero bandwidth, however, will contain some frequency components that are not directly on an OFDM sub-carrier, and leakage will occur. To verify this, two interference signals were created in Matlab. The first was a single tone with power -41.3 dBM, and with a frequency of 103.125 MHz after downconversion. This frequency corresponds to the $25^{th}$ OFDM sub-carrier. The second was a noise signal with the same average power and a 1 MHz bandwidth, modulated at the same

frequency. A plot of the FFTs of these signals, with their power levels referred back to the receiver input can be found in Fig. 4. Also drawn on this plot is the spectral density of the received UWB data signal when the receiver is operating at 6 dB above its sensitivity level. As expected, the single tone interference exhibits no spectral leakage, and thus frequency excision of this single tone would provide sufficiently reliable communication. The band-limited modulated noise interference, however, does display considerable spectral leakage. In fact, for interference power near the FCC limit of -41.3 dBm/MHz, the leakage power would exceed the sensitivity signal power for every OFDM sub-carrier. Thus, frequency excision of the single sub-carrier would not be sufficient.

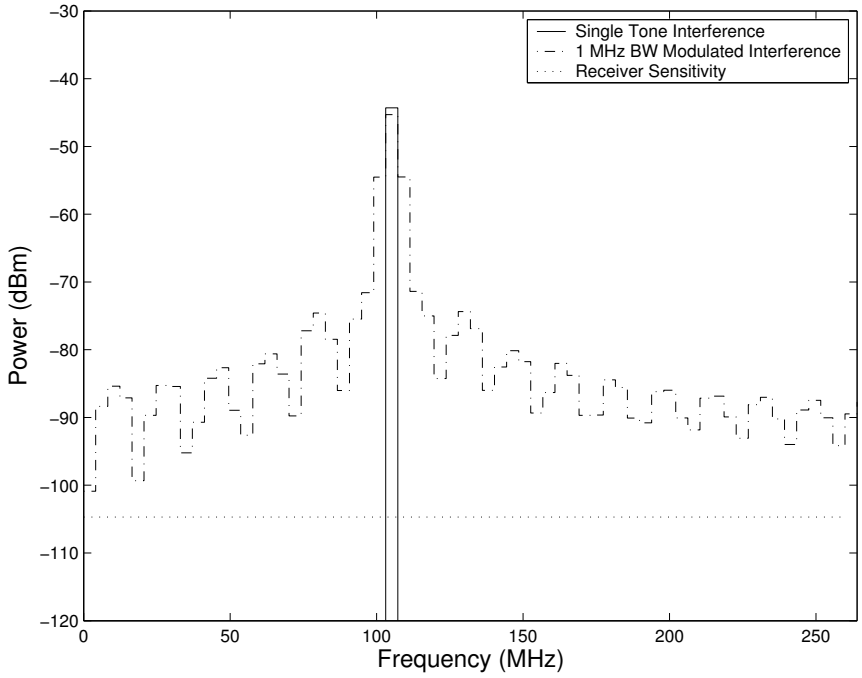



Fig. 4. FFT of maximum power single tone and non-zero bandwidth interference signals with frequency equal to that of the $25^{th}$ sub-carrier. Power levels are referred back to the input.

The worst case for spectral leakage occurs when the frequency of the interference

lies directly between two OFDM sub-carriers. Changing the downconverted interference frequency for both the single tone and modulated noise interferers to 105.1875 MHz, which is in between the $25^{th}$ and $26^{th}$ OFDM sub-carriers, spectral leakage should occur even for the single tone interference. As shown in Fig. 5, the spectral leakage for the single tone interference in this case is worse than that of the modulated noise interference. Now, in both cases, the spectral density of the leakage power exceeds that of the receiver sensitivity.

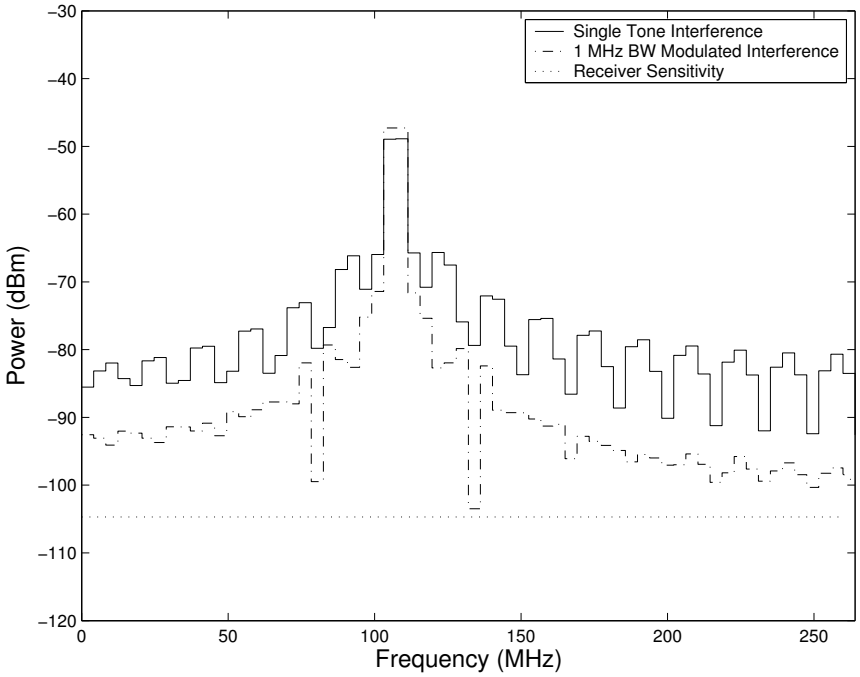



Fig. 5. FFT of maximum power single tone and non-zero bandwidth interference signals with frequency between the $25^{th}$ and $26^{th}$ OFDM subcarriers. Power levels are referred back to the input.

To provide some indication as to the tolerable limits of interference, the interference power was set to -69.5 dBm, with the frequency 105.1875 MHz. This corresponds to SIR=-8 dB, which, based on the MB-OFDM proposal, is the maximum interference power for a single tone interferer such that reliable communication will occur when

the receiver is operating at 6 dB above sensitivity [3]. Figure 6 displays the input referred FFT of the single tone and non-zero bandwidth interferences. Most of the subcarriers now have information power greater than the power of the interference spectral leakage.

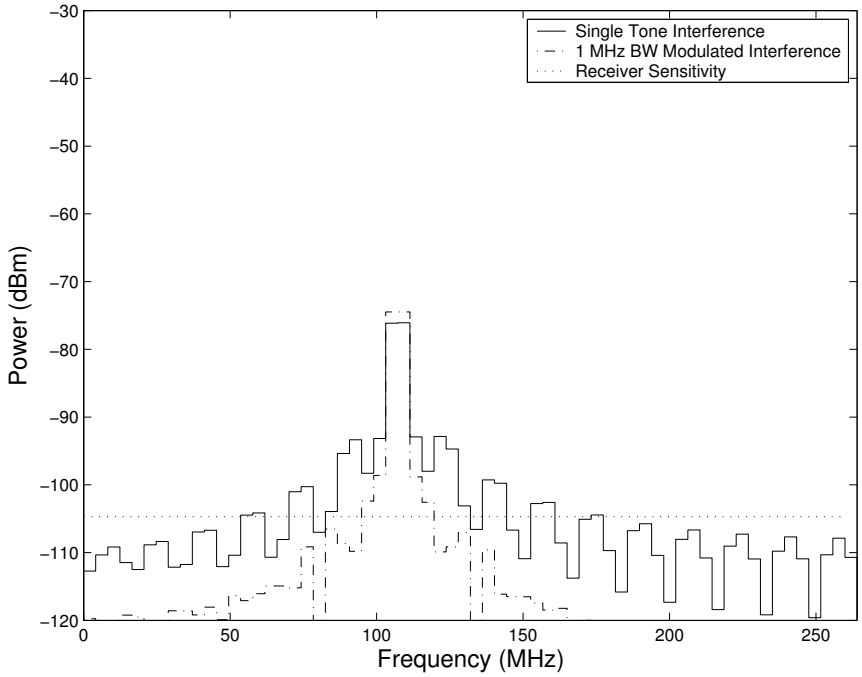



Fig. 6. FFT of single tone and non-zero bandwidth interference signals with frequency between the $25^{th}$ and $26^{th}$ OFDM subcarriers with SIR=-8dB. Power levels are referred back to the input.

### 2. Effect of NBI on Quantization Noise

Next, the effect NBI has on the signal to quantization noise (SQNR) is considered. A similar approach is taken to gain insight into this problem. In these simulations, a four bit quantizer was used prior to computing the FFT. The quantization levels were set according to the interference power. The frequency of the interference is set to exactly align with the $25^{th}$ sub-carrier to ensure that only quantization noise

power and no spectral leakage exists for the remaining FFT bins. For the maximum interference power of -41.3 dBm, the resulting input referred FFT is plotted in Fig. 7. The quantization noise spectral density exceeds that of the information, and communication would be unreliable. The interference power is again set to -68.5 dBm, corresponding to SIR=-9 dB. Figure 8 displays the input referred result of the FFT. Other than the FFT bin corresponding to the interference frequency, the information spectral density is greater than that of the ADC quantization noise. This indicated that spectral leakage of interference onto neighboring OFDM sub-channels poses a greater threat to reliable communication than the effect of interference on SQNR.

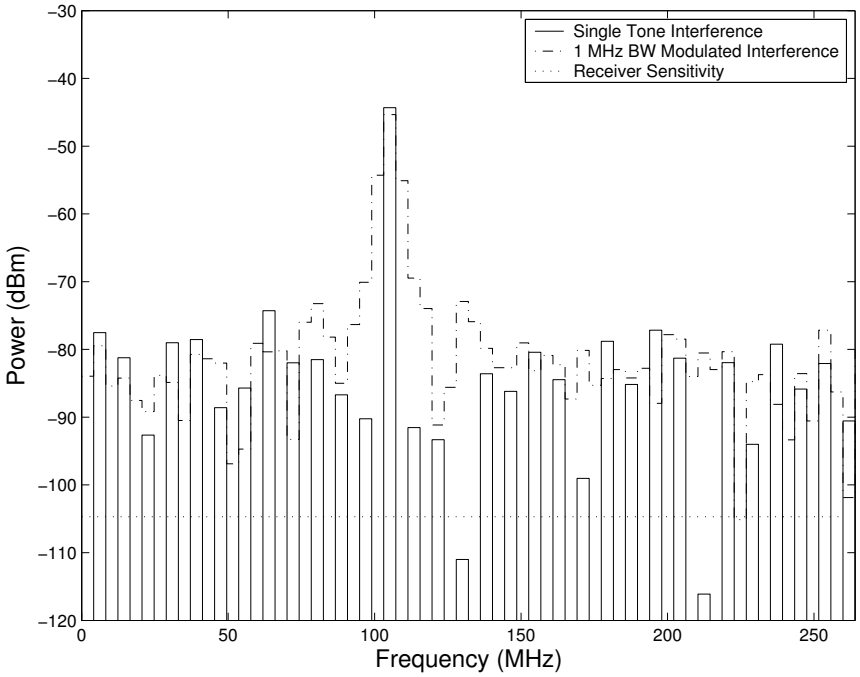



Fig. 7. FFT of single tone and non-zero bandwidth interference signals with frequency equal to the $25^{th}$ OFDM sub-carrier with power levels at the FCC limit of -41,3 dBm. A four bit quantizer was used before the FFT was computed. Power levels are referred back to the input.

As mentioned in Section B, assuming the receiver is operating at sensitivity, the maximum tolerable received interference power such that digital mitigation could

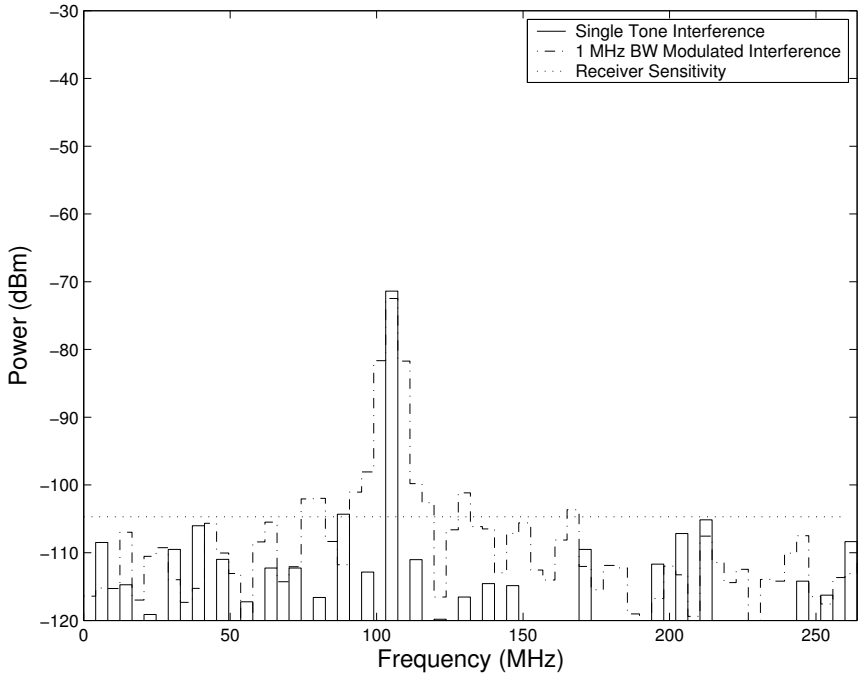



Fig. 8. FFT of single tone and non-zero bandwidth interference signals with frequency equal to the $25^{th}$ OFDM sub-carrier with SIR=-9dB. A four bit quantizer was used before the FFT was computed. Power levels are referred back to the input.

sufficiently handle interference is -69.5 $dBm$ for a single tone interferer, or -70.5 dBm for a modulated narrow band interferer (The additional 1 dB of allowable power for the modulated interferer is evident based on the lower spectral leakage associated with that case). Thus, reliable communication is only ensured when the received interference power is nearly 30 $dB$ less than the limit set forth by the FCC. Including path loss, it is evident that the NBI must be attenuated by at least 12 dB before digital mitigation techniques are applied to the signal in order to ensure reliable communication. One solution is to include an analog notch filter in the receive chain to attenuate the interference before the received signal enters the digital domain. Figure 9 displays the input referred FFT of an interference with frequency between the $25^{th}$ and $26^{th}$ OFDM subcarriers. The power of the interference is -57.3 dBm,

corresponding to a maximum power interference at 5cm separation from the antenna. This is the maximum interference power that might be expected at the receiver. Since the spectral leakage of the interference has higher power density than the received signal, communication will fail. Figure 10 shows the input referred FFT of the same signal after the inclusion of an analog notch filter in the receive chain. The -3 dB bandwidth of the notch filter was set to 24 MHz. By attenuating the interference, both the SQNR is increased and the spectral leakage is reduced to a level that is close to the unfiltered interference with SIR=-9 dB. Reliable communication is now possible for SIR as low as -20 dB.

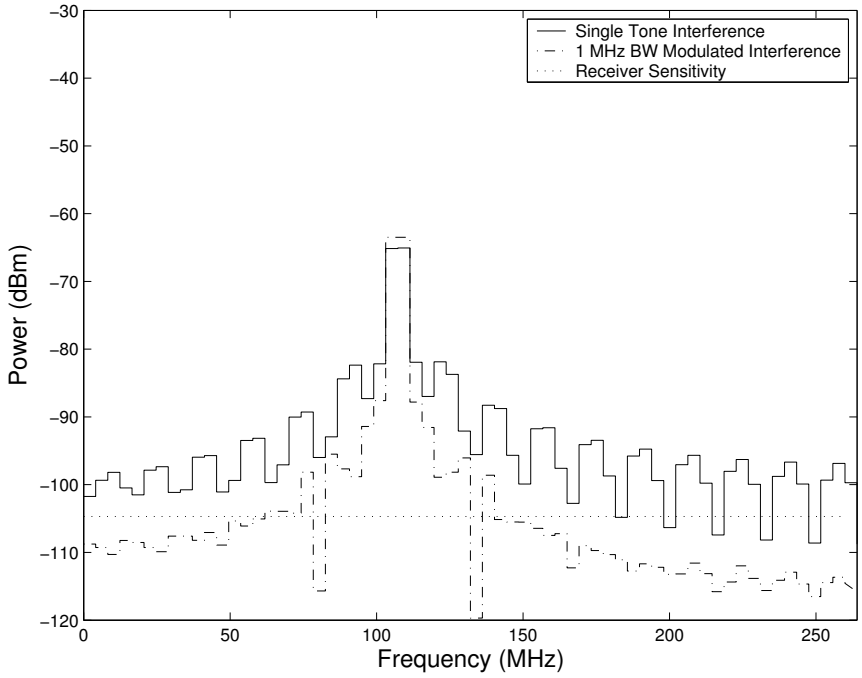



Fig. 9. FFT of single tone and non-zero bandwidth interference signals with frequency in between the $25^{th}$ and $26^{th}$ OFDM sub-carriers. The power levels are set to -57.3 dBm, assuming the interference power is -41.3 dBm with 5cm separation from the antenna. A four bit quantizer was used before the FFT was computed. Power levels are referred back to the input.

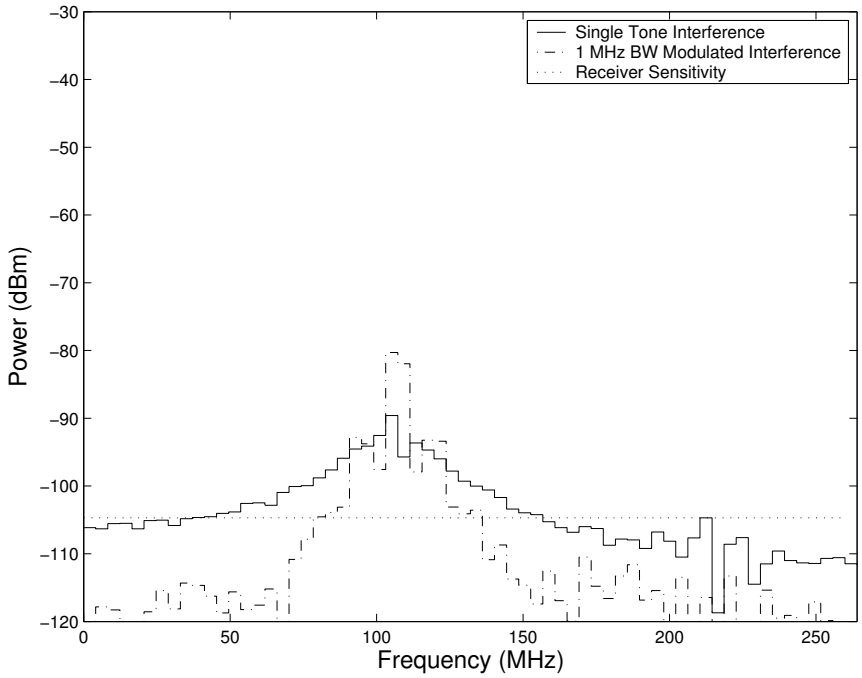



Fig. 10. FFT after analog notch filtering of single tone and non-zero bandwidth interference signals with frequency in between the $25^{th}$ and $26^{th}$ OFDM sub-carriers. The power levels are set to -57.3 dBm, assuming the interference power is -41.3 dBm with 5cm separation from the antenna. A four bit quantizer was used before the FFT was computed. Power levels are referred back to the input.

# CHAPTER III

## ANALOG FILTERING OF NARROWBAND INTERFERENCE

It has been shown that narrowband interference could be a problem for UWB communication. It thus becomes necessary to develop methods for handling NBI. In existing systems that use wideband modulation formats, such as spread-spectrum CDMA, digital techniques are used to reduce interference [14, 15]. In [16], a digital least squares estimation technique is used specifically for frequency hopping systems. Unfortunately, as discussed in Chapter II, part of the problem is due to nonidealities in the analog front end. These include amplitude clipping due to finite dynamic range and decreased SQNR due to finite precision of the ADC. To reduce these effects, interference needs to be reduced before the signal enters the digital domain. In [17], a UWB receiver based on analog filter banks was proposed to suppress NBI. However, the analog power consumption and complexity of such a system are very high. As many as 16 parallel filters and data converters were used in that work.

In this work, a single, programmable analog notch filter is included in the baseband receive chain to reduce NBI before the signal is quantized. The filter is optimally placed after the baseband lowpass filter (LPF), and before the variable gain amplifier (VGA), as depicted in Fig. 11. Placing the notch filter after the LPF reduces its need to handle out of band interference, and placing it before the VGA reduces its linearity requirement. Filtering at radio frequencies would be an attractive option from a system level perspective, however it is not practical in modern day CMOS technologies. Consider the case where NBI occurs at 4.75 GHz, which is the upper edge of the UWB spectrum. An analog notch filter centered around the NBI frequency with a 20 MHz -3 dB bandwidth would have a $Q = 4.75e9/20e6 = 237.5$. If the $Q$ of the filter

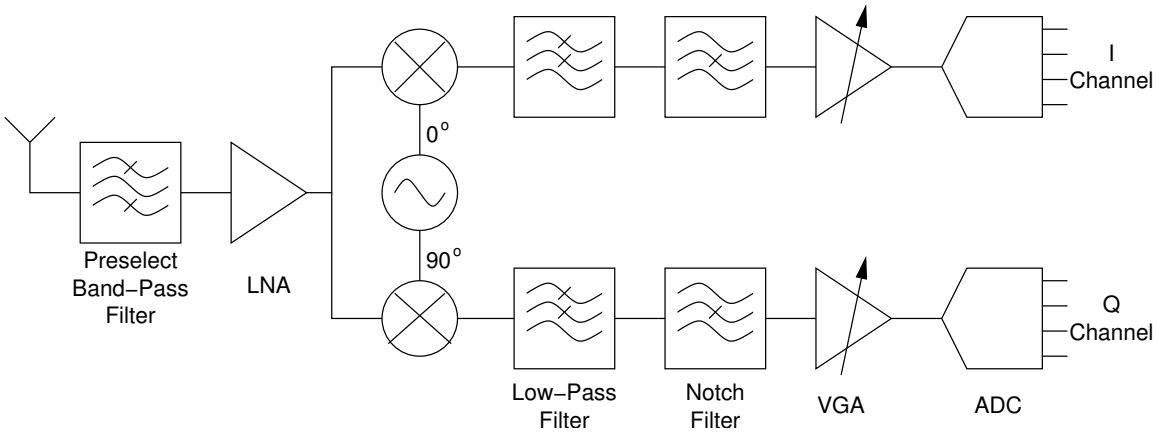



Fig. 11. Modified UWB receiver analog front end with the inclusion of an analog notch filter.

is reduced to the more reasonable value of 20, the bandwidth of the filter becomes 228.5 MHz. Thus, in addition to filtering the interference, nearly half of the UWB data would be filtered out as well. In this chapter, the specifications for the notch filter are obtained, and the design is discussed.

## A. Filter Specifications

Consider a second order notch filter, whose transfer function is:

$$H_{BR} = \frac{s^2 + \frac{1}{\alpha_0}\omega_{bw}s + \omega_0^2}{s^2 + \omega_{bw}s + \omega_0^2}, \tag{3.1}$$

where $\omega_0$ is the center frequency in Rad/s, $\omega_{bw}$ is the -3 dB bandwidth in Rad/s, and $\alpha_0$ is the steady state attenuation at the center frequency. After downconversion, interference could occupy any frequency within the continuous UWB baseband, which is 0–264 MHz. Most direct conversion receivers will have a high pass filter (HPF) to remove DC offsets after the mixer. The HPF will attenuate interferences that downconvert to frequencies near DC. The problematic interferences thus have frequencies from a few MHz up to 264 MHz. The notch filter's center frequency should accord-

ingly be adjustable throughout this range, and a method should exist for adaptively changing $\omega_0$ to match the interference frequency.

In typical OFDM systems, it would be desirable to set the notch filter's bandwidth equal to that of one OFDM sub-channel, which in the case of the current proposal is 4.125 MHz [3]. However, since MB-OFDM is a frequency hopping system, interference will only appear in the baseband periodically. If the current proposal is accepted, interference will appear for 312.5 ns every 966 ns. This presents two potential problems. First, the notch filter will need to settle on every period, and the settling time is inversely proportional to the filter's bandwidth. Secondly, the subsequent MB-OFDM symbol will be affected by the interference due to the ringing behavior of the filter. Figure 12 illustrates these problems. A typical downconverted interference in an MB-OFDM system is provided to the input of a second order notch filter with a bandwidth of 4.125 MHz. At this bandwidth, it takes nearly the entire symbol duration for the filter to settle. The problem of the filter ringing during the subsequent symbol can be solved by bypassing the filter during the symbols that contain no interference. The settling time can be controlled by optimizing the filter's bandwidth.

The specifications for the filter's -3 dB bandwidth, $\omega_{bw}$, and steady state attenuation, $\alpha_0$, can be developed together. A filter with infinite steady state attenuation will still have some interference at its output during the symbol period due to the settling behavior. If the input to the notch filter is $v_i = A_i \sin(\omega_0 t)$, for $\omega_0 \gg \omega_{bw}$, the filter output can be approximated by:

$$v_o \approx A_i \sin(\omega_0 t) \left[ \frac{1}{\alpha_0} + \frac{\alpha_0 - 1}{\alpha_0} e^{-\frac{\omega_{bw}}{2} t} \right] \tag{3.2}$$

If $\alpha_0 = \infty$, the 2% settling time is computed by setting the exponential term of

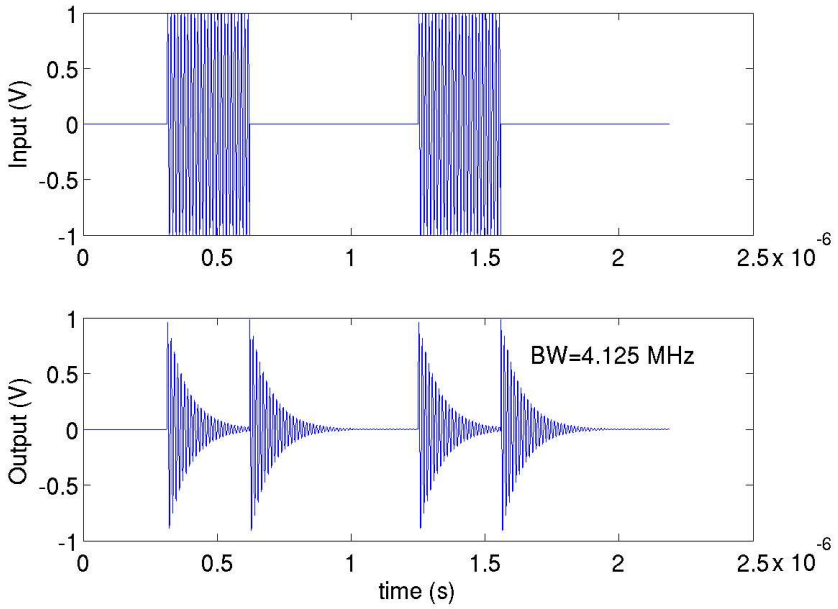



Fig. 12. Time domain input and output of a second order 4.125 MHz bandwidth notch filter for interference in the time and frequency interleaved MB-OFDM system.

Eq. 3.2 equal to 0.02. The solution is found to be:

$$t_s = \frac{7.82}{\omega_{bw}} \tag{3.3}$$

The settling time of the filter is thus only a function of the filter bandwidth, and not the center frequency. To illustrate this point, Fig. 13 displays the output of the filter for two different center frequencies, but with the same -3 dB bandwidth. The settling time for both cases is the same. Alternatively, Fig. 14 displays the output of the filter for two different bandwidths, but with the same center frequency. As expected, the filter with $\omega_{bw} = 2\pi 20$ Mrad/s settles in about half the time as the filter with $\omega_{bw} = 2\pi 10$ Mrad/s.

This result indicates that settling time can be reduced by increasing $\omega_{bw}$. The bandwidth cannot be increased indefinitely, however, because the UWB data signal will also be lost due to the filtering. One way to determine proper values for $\omega_{bw}$ and $\alpha_0$

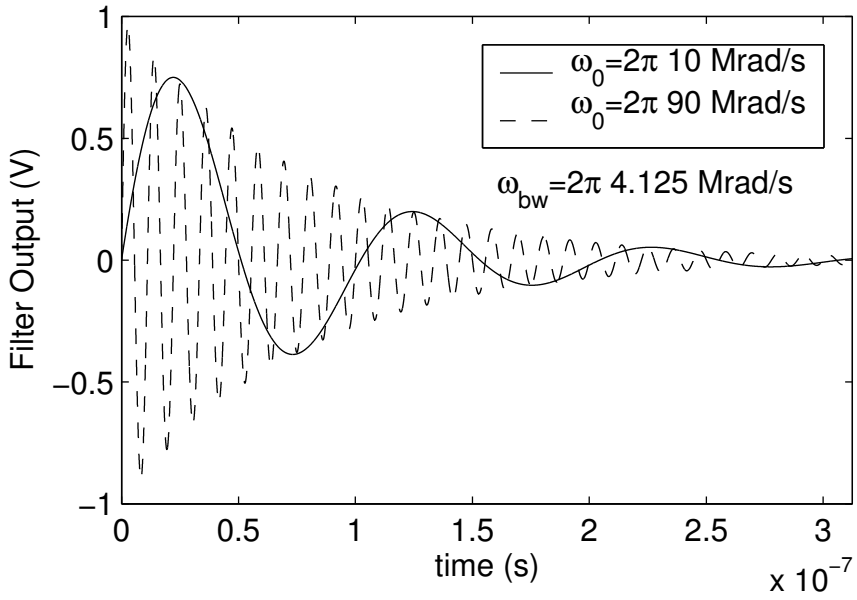



Fig. 13. Time domain output of a second order 4.125 MHz bandwidth notch filter for two different center frequencies. The settling time of the filter remains constant.

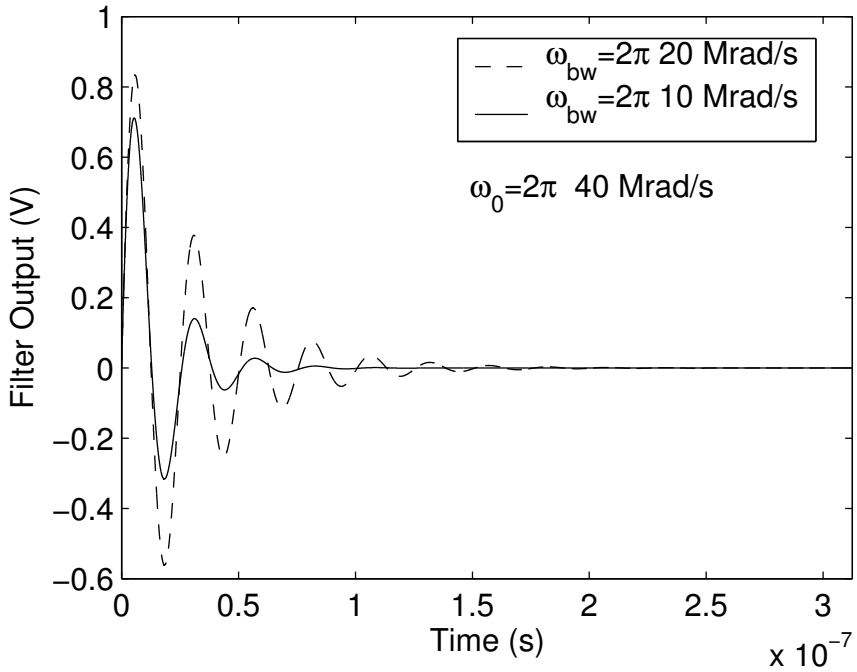



Fig. 14. Time domain output of a second order notch filter for two different bandwidths. The settling time of the filter decreases for larger bandwidths.

is to use the root mean squared (RMS) value of the interference at the filter's output. The RMS level of the output can be calculated from Eq. 3.2 assuming a symbol period of 312.5 ns, which is in accordance with the current MB-OFDM proposal [3]. The actual attenuation provided by the filter will then be the ratio of the output RMS to the input RMS. Assuming the input interference is a single tone located at the center frequency of the filter, the resulting attenuation in RMS,$\alpha_{RMS}$, is calculated as:

$$\alpha_{RMS} = \sqrt{2}\sqrt{\int_0^{312.5ns} v_o^2 dt} \tag{3.4}$$

Figure 15 displays the attenuation in the RMS of the interference, $\alpha_{RMS}$, versus $\omega_{bw}$ for different values of $\alpha_0$. For large $\omega_{bw}$, the RMS attenuation approaches the steady state attenuation, $\alpha_0$. For reasonable bandwidths, $\omega_{bw}$ between 10 and 40 MHz, not much improvement in $\alpha_{RMS}$ is seen when increasing $\alpha_0$ beyond 20 dB. As discussed in Section B, at least 10 dB attenuation in the interference is required. A reasonable option is then to select $\omega_{bw} \approx 20$ MHz, and $\alpha_0 = 20$ dB. These specifications should provide almost 15 dB in the RMS of the interference.

Using a higher order notch filter to suppress the interference has the benefit of sharper rolloffs in the stopband, which will allow for higher selectivity and thus less filtering of the UWB data signal. However, the settling times of the notch filter types increase with filter order. Figures 16, 17, 18, and 19 respectively display the settling behavior for Butterworth, Chebyshev, Elliptical, and Bessel type notch filters.

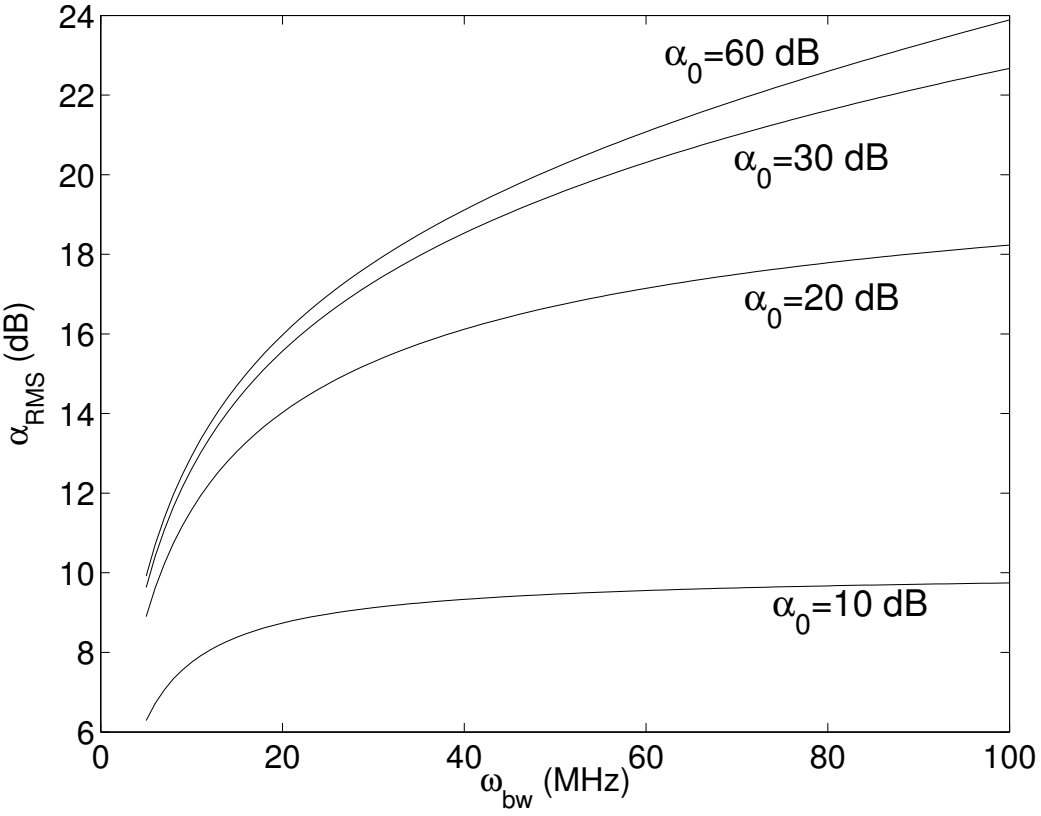



Fig. 15. Attenuation in the RMS level of the interference at the filter's output versus the filter's -3 dB bandwidth, $\omega_{bw}$, for different values of the filter's steady state attenuation, $\alpha_0$, assuming an OFDM symbol period of 312.5 ns.

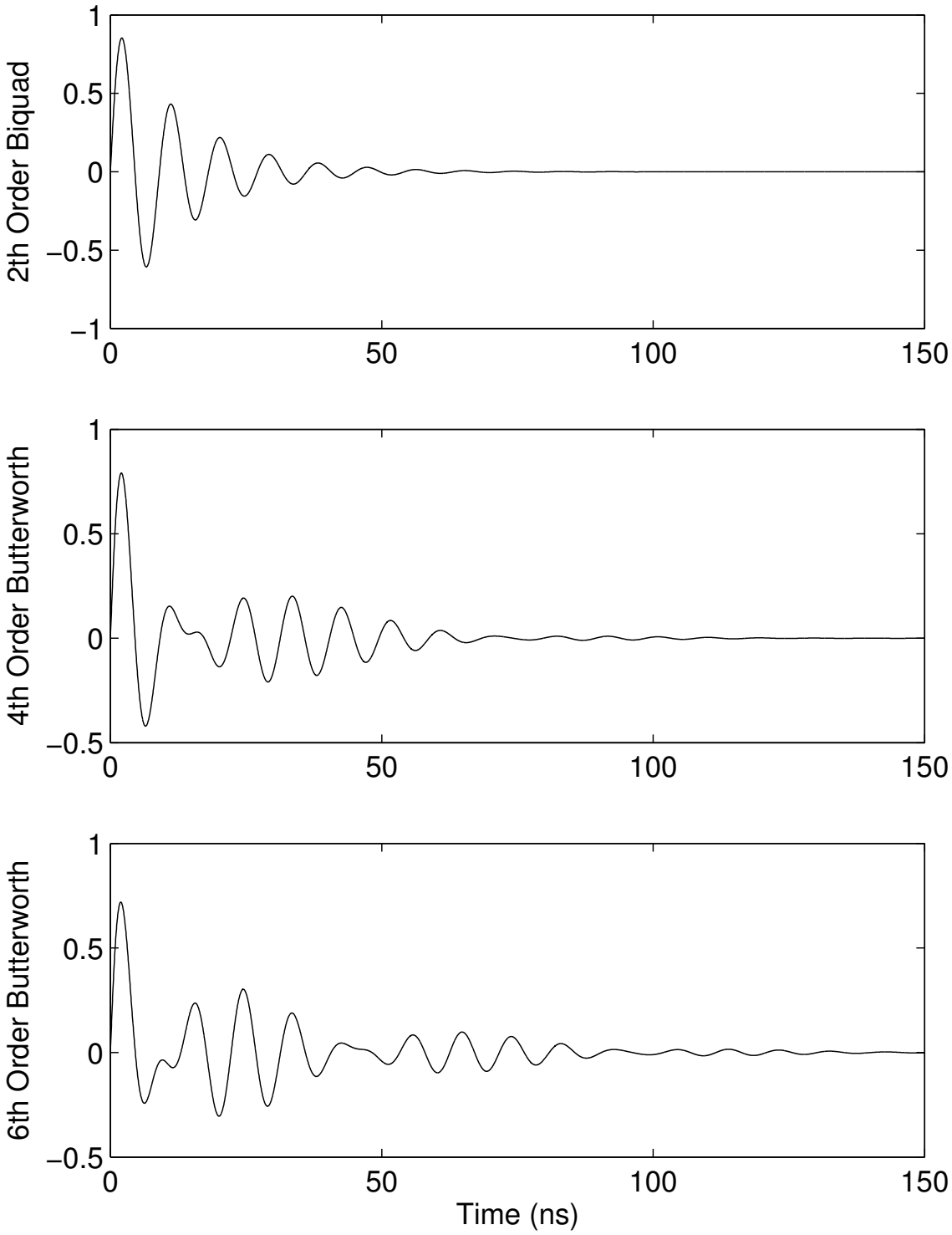



Fig. 16. Settling behavior of Butterworth type notch filters.

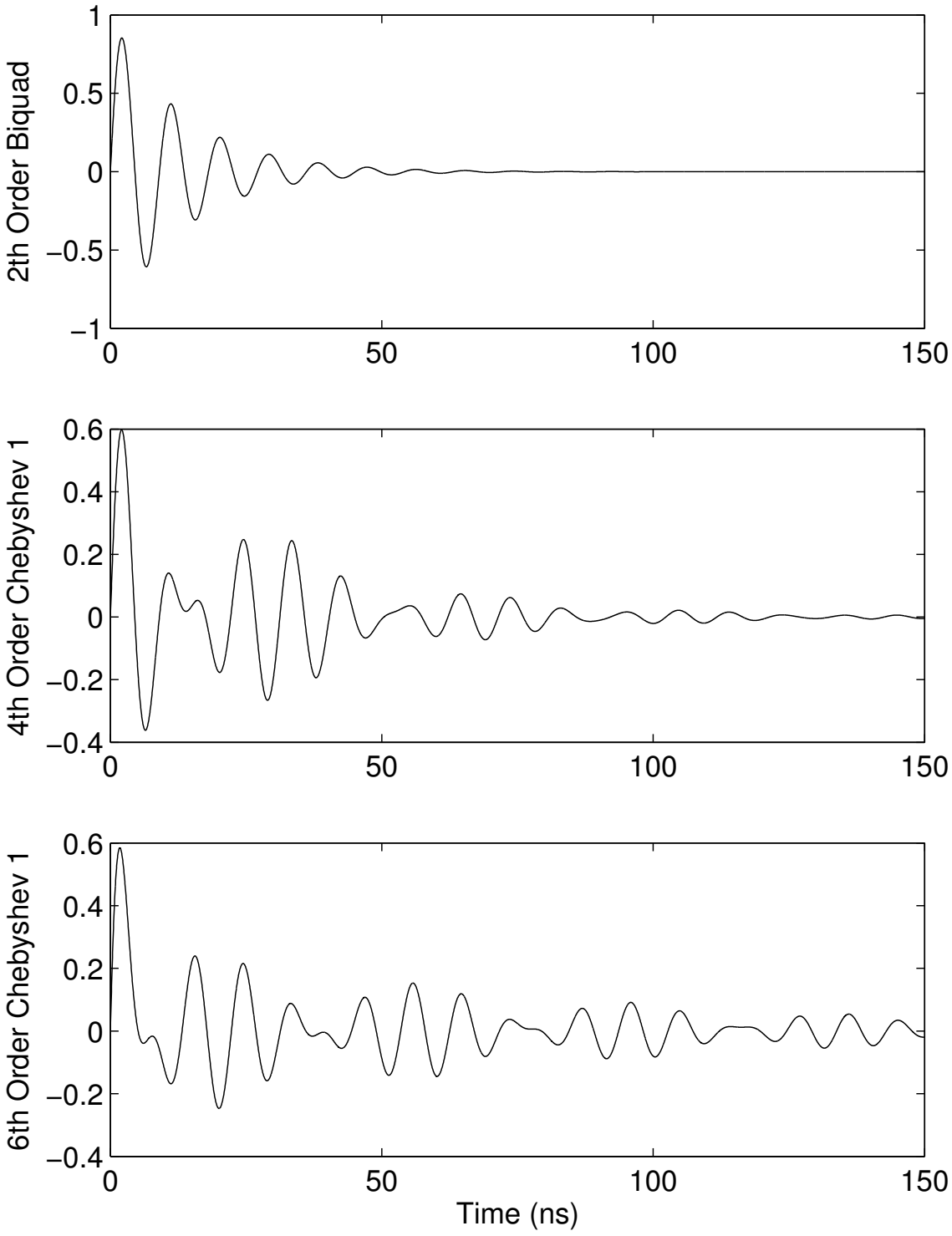



Fig. 17. Settling behavior of Chebyshev type 1 notch filters.

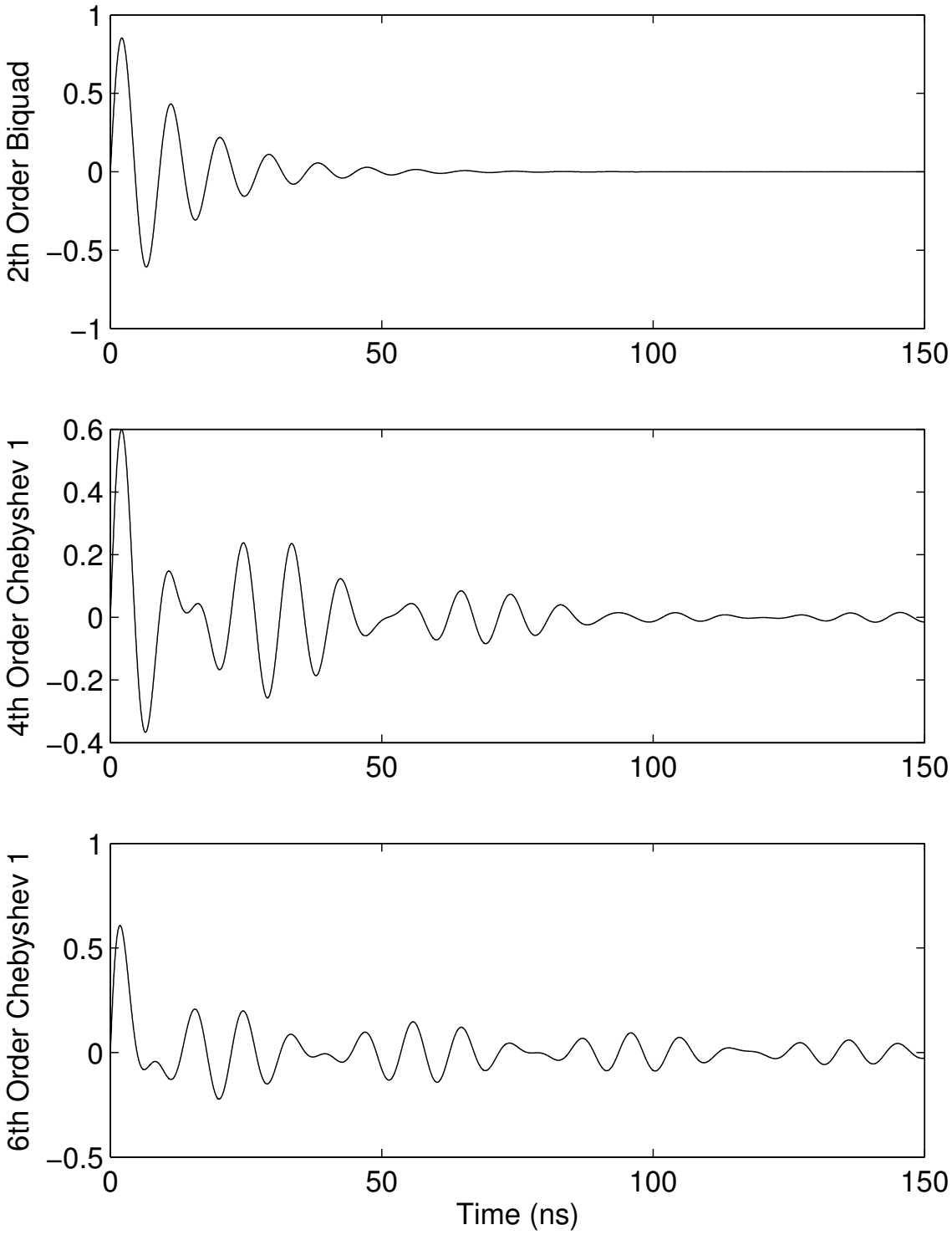



Fig. 18. Settling behavior of elliptic type notch filters.

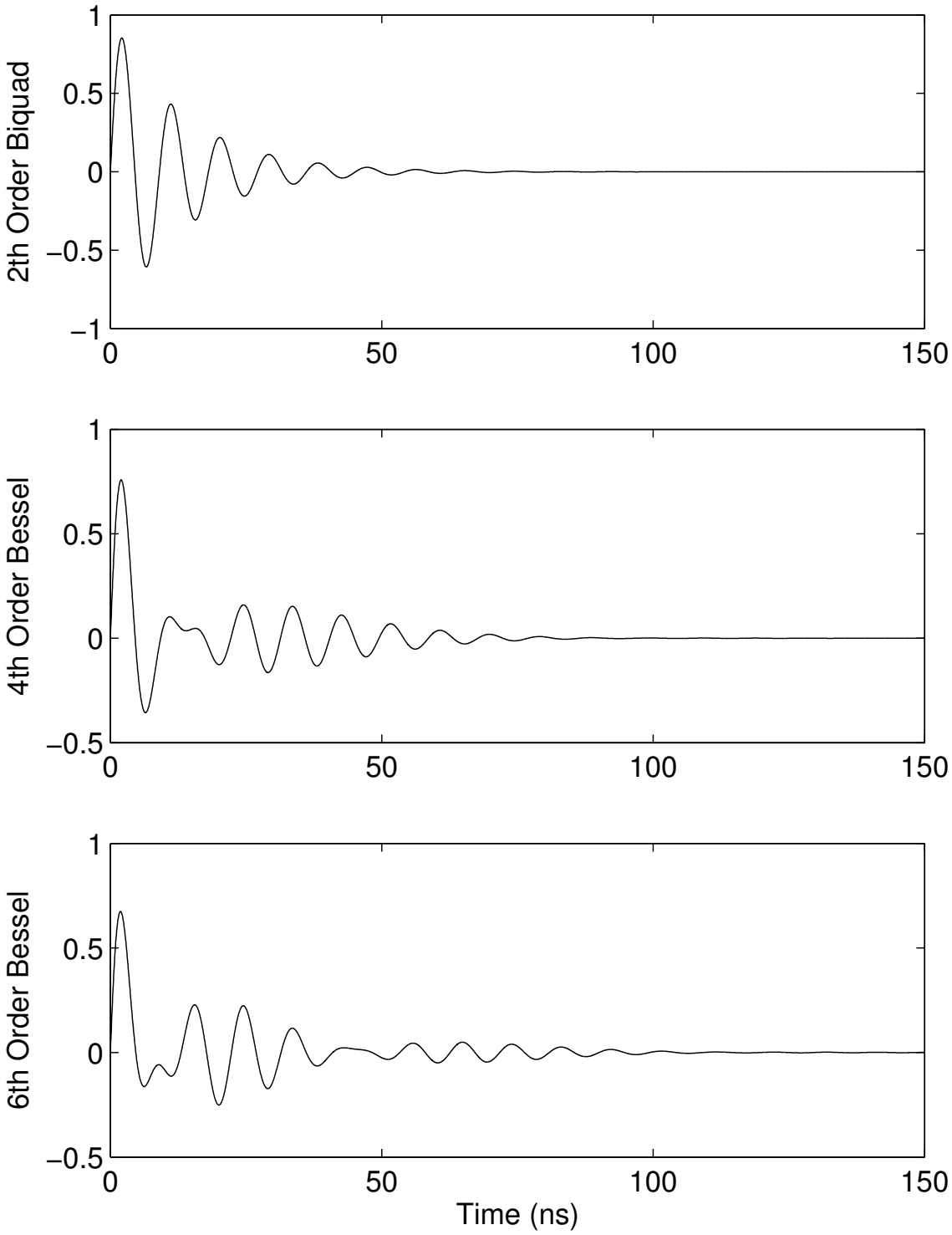



Fig. 19. Settling behavior of Bessel type notch filters.

Table II. Settling behavior for various notch filter types and orders

| **Filter Type** | **Order** | **2% Settling Time** | $\alpha_{RMS}$ |
|---|---|---|---|
| Biquad | 2 | 51.9 ns | 16.7 dB |
| Butterworth | 4 | 66.0 ns | 18.2 dB |
| Butterworth | 6 | 88.8 ns | 18.5 dB |
| Chebyshev I | 4 | 105.2 ns | 19.3 dB |
| Chebyshev I | 6 | 212.0 ns | 19.8 dB |
| Elliptic | 4 | 88.8 ns | 19.3 dB |
| Elliptic | 6 | 221.3 ns | 19.9 dB |
| Bessel | 4 | 66.3 ns | 19.1 dB |
| Bessel | 6 | 84.1 ns | 19.9 dB |

Table II provides a summary of the 2% settling times and attenuation in RMS of the interference for each type. Of the higher order filter types, Butterworth and Bessel approximations offer the best settling times. However, since settling time degrades and $\alpha_{RMS}$ is only moderately better for higher order filters compared to a second order biquad, it may not be worth the increased area, power consumption. Furthermore, tuning of higher order filters becomes a challenging task considering the large tuning range required for the center frequency. With all aspects considered, a second order notch filter seems to be the best option. A summary of the critical filter specifications is provided in Table III.

Table III. Desired notch filter characteristics

| **Specification** | **Value** |
|---|---|
| Filter Order | 2 |
| $\omega_0$ Tuning Range | $\omega_{0min} \leq 2\pi 2$ MRad/s $\omega_{0max} \geq 2\pi 264$ MRad/s |
| $\omega_{bw}$ | $\approx 2\pi 20$ MRad/s |
| $\alpha_0$ | $\geq 20$ dB |

## B. Filter Design

The notch filter architecture, as depicted in Fig. 20 is based on feedforward subtraction of a bandpass filtered signal. One implementation of the notch filter is to use an OTA-C biquad as the bandpass filter, and cross coupled OTAs as the subtracter, as shown in Fig. 21. $g_b$, $g_l$, and $g_s$ are parasitic conductances where $g_b = g_{o1} + g_{o2} + g_{o5}$, $g_l = g_{o3}$, and $g_s = 2g_{o5} + g_{o6}$. The transfer function of the notch filter, including these parasitic conductances, is derived to be:

$$\frac{V_o}{V_i} = \frac{g_{m5}}{g_{m6} + g_s} \times \frac{s^2 + \left[\frac{g_{m2} + g_b - g_{m1}}{C_1} + \frac{g_l}{C_2}\right] s + \frac{(g_{m2} + g_b + g_{m1})g_l + g_{m3}g_{m4}}{C_1 C_2}}{s^2 + \left[\frac{g_{m2} + g_b}{C_1} + \frac{g_l}{C_2}\right] s + \frac{(g_{m2} + g_b)g_l + g_{m3}g_{m4}}{C_1 C_2}} \tag{3.5}$$

For low center frequencies, output conductances can be neglected. At high center frequencies, the following assumptions are made to simplify the analysis:

$$g_{m3} \gg g_{o3} \gg g_{o1}, g_{o2} \tag{3.6}$$

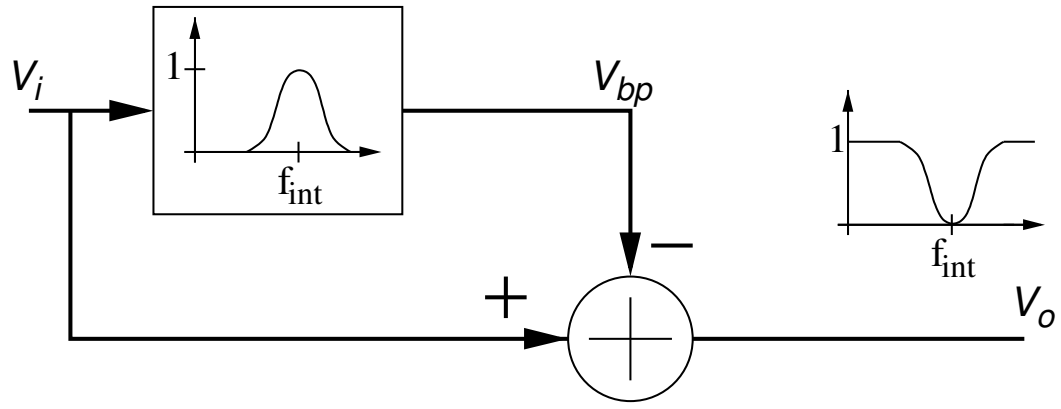



Fig. 20. Notch filter architecture based on feedforward subtraction of a bandpass filtered signal.

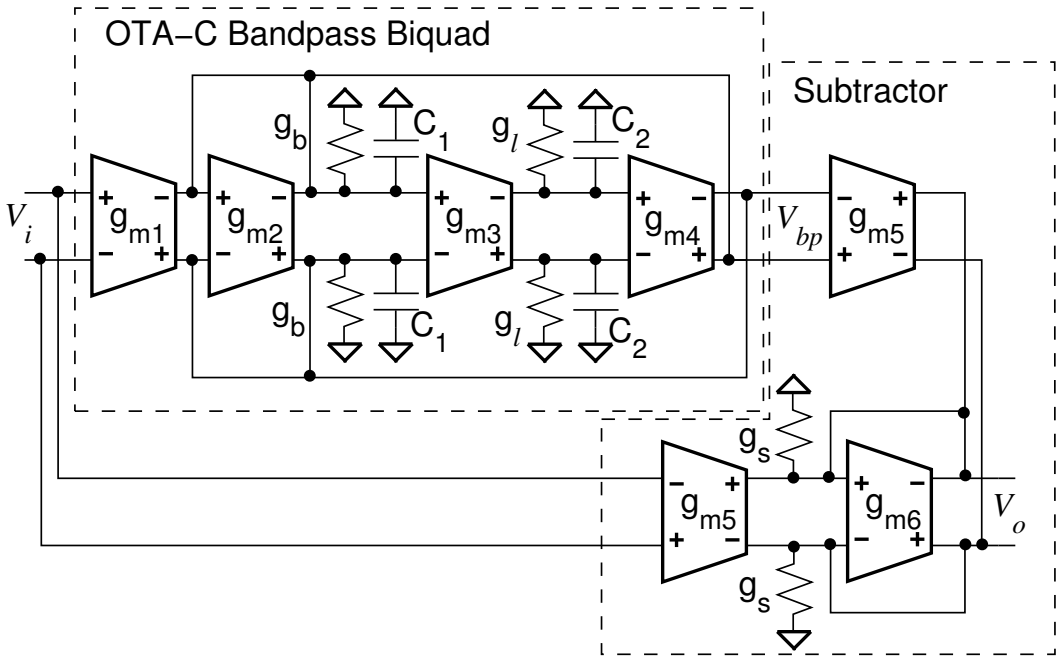



Fig. 21. Notch filter architecture utilizing an OTA-C bandpass filter.

$$g_{m6} \gg g_s \tag{3.7}$$

Assuming the OTAs are designed with sufficient DC voltage gain, the transconductance of a given OTA will be significantly larger than its output conductance. Furthermore, since at high center frequencies $g_{m3}$ will be large compared to $g_{m1}$ and $g_{m2}$, the output conductance, $g_{o3}$, should also be much larger than $g_{o1}$ and $g_{o2}$. Letting $C_1 = C_2 = C$, and $g_{m4} = g_{m3}$, Eq. 3.5 can now be approximated by:

$$\frac{V_o}{V_i} \approx \frac{g_{m5}}{g_{m6}} \frac{s^2 + \frac{g_{m2} + 2g_{o3} - g_{m1}}{C} s + \frac{g_{m3}^2}{C^2}}{s^2 + \frac{g_{m2} + 2g_{o3}}{C} s + \frac{g_{m3}^2}{C^2}} \tag{3.8}$$

The relevant characteristics of Eq. 3.8 are:

$$\omega_0 = \frac{g_{m3}}{C} \tag{3.9}$$

$$\omega_{bw} = \frac{g_{m2} + 2g_{o3}}{C} \tag{3.10}$$

$$\alpha_0 = \frac{g_{m6}}{g_{m5}} \frac{g_{m2} + 2g_{o3}}{g_{m2} + 2g_{o3} - g_{m1}} \tag{3.11}$$

### 1. Discrete Center Frequency Control

Interference can appear anywhere within the continuous UWB basebandwidth. Detecting the existence and location of the interference would be a challenging task in the analog domain, but becomes relatively straightforward with the use of an FFT. Since MB-OFDM modulation already uses FFT to decode the UWB data, interference detection can be done with minimal additional overhead. If digital interference detection via FFT is used, for simplicity it follows that the notch filter's center frequency should have digital controls.

The new block diagram of the filter with the center frequency control included is displayed in Fig. 22. The digital word, $W_{fo}$ is used to discretely control the center

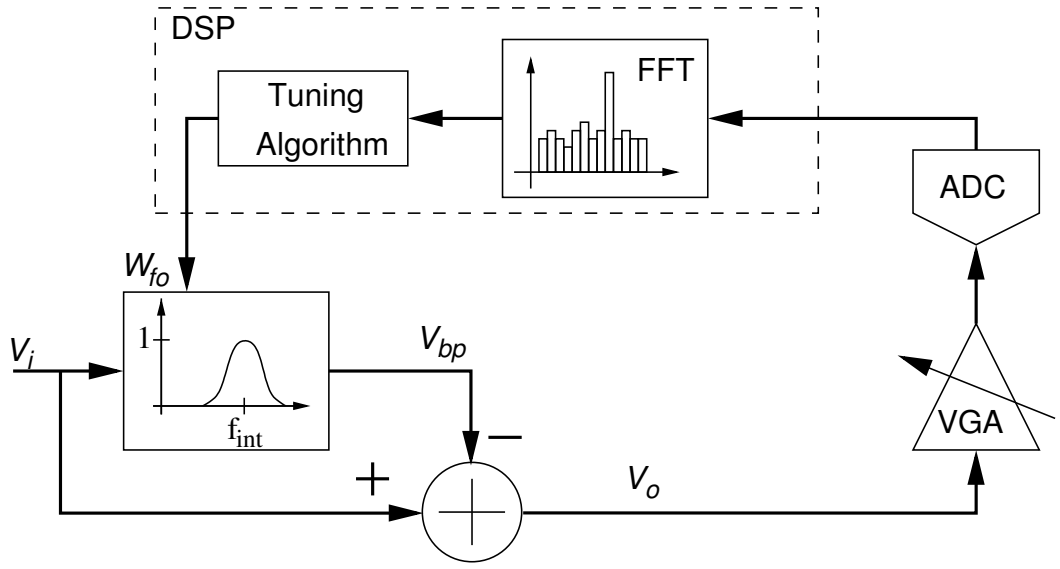



Fig. 22. Notch filter utilizing the DSP's FFT block for interference detection and center frequency tuning of the notch filter.

frequency of the filter, such that:

$$\omega_o = \rho W_{fo}, \tag{3.12}$$

where $\rho$ is the step size in Hz between adjacent frequency settings of the filter. Since $\omega_o$ is controllable only in discrete frequency steps, and the range of potential interference frequencies is continuous, $\rho$ should be carefully selected. The center frequencies for two adjacent settings of $W_{fo}$ should be close enough together that sufficient attenuation is achieved where their magnitude responses overlap. The proper value of $\rho$ can be determined from the specifications of the filter. To ensure an attenuation of at least $\alpha_{min}$, $\rho$ should be limited to:

$$\rho \leq \frac{\omega_{bw}}{\alpha_{min}} \tag{3.13}$$

The number of required discrete frequency steps, N, can then be determined by:

$$N \geq \frac{\omega_{max}}{\rho} \tag{3.14}$$

where $\omega_{max}$ is the maximum interference frequency. For the case of a MB-OFDM receiver with a basebandwidth of $\omega_{max} = 2\pi 264$ Mrad/s and utilizing a notch filter with $\omega_{bw} = 2\pi 20$ Mrad/s and $\alpha_0 \geq 20$ dB, Eq. 3.13 yields $\rho = 2\pi 2$ Mrad/s and Eq. 3.14 yields $N \geq 160$. To accommodate process and temperature variations, in this work, an 8-bit $W_{fo}$ with length $N = 256$ was used, and $\omega_{max}$ was over-designed to $\omega_{max} = 2\pi 320$ Mrad/s.

Based on Eq. 3.9, to discretely adjust $\omega_0$, either $g_{m3}$, $C$, or some combination of both need to be switchable. In this case, it is best to have $\omega_0$ change linearly with $W_{fo}$ so that the entire UWB baseband can be covered equally by the filter. This leads to utilizing a bank of OTAs for digitally controlling $g_{m3}$ and $g_{m4}$. Thermometer coded unit OTAs were used to prevent large center frequency steps due to mismatch when one of the most significant bits of $W_{fo}$ changes. If unit OTAs with transconductance $g_{mu}$ are used, it follows that $g_{m3}$ and $g_{m4}$ from Fig. 21 are equivalent to:

$$g_{m3} = g_{m4} = W_{fo} g_{mu} \tag{3.15}$$

Constant bandwidth regardless of center frequency is desirable. However, according to Eq. 3.10, $\omega_{bw}$ depends on the output conductance of $g_{m3}$, which for large values of $W_{fo}$ may be comparable to $g_{m2}$. To compensate for the increase in conductance, a bank of OTAs was also used for $g_{m2}$. However, only 16 unit OTAs were needed because $g_{o3}$ does not change strongly with $W_{fo}$. The digital control for $g_{m2}$, $W_{bw}$ can be derived from $W_{fo}$, and is equal to:

$$W_{bw} = 16 - \left\lfloor \frac{W_{fo}}{16} \right\rfloor \tag{3.16}$$

If the same unit OTA, $g_{mu}$, is used $g_{m2}$ from Fig. 21 becomes:

$$g_{m2} = W_{bw} g_{mu} \tag{3.17}$$

For unity passband gain of the notch filter, $g_{m5}$ and $g_{m6}$ were set equal, such that:

$$g_{m5} = g_{m6} = g_s \tag{3.18}$$

Substituting Eqs. 3.15, 3.17, and 3.18 into Eq. 3.8, the resulting transfer function in terms of the discrete control becomes:

$$\frac{V_o}{V_i} \approx \frac{s^2 + \dfrac{W_{bw} g_{mu} + 2W_{fo} g_{ou} - g_{m1}}{C} s + \dfrac{W_{fo}^2 g_{mu}^2}{C^2}}{s^2 + \dfrac{W_{bw} g_{mu} + 2W_{fo} g_{ou}}{C} s + \dfrac{W_{fo}^2 g_{mu}^2}{C^2}} \tag{3.19}$$

of which the relevant characteristics are:

$$\omega_0 = W_{fo} \frac{g_{mu}}{C} \tag{3.20}$$

$$\omega_{bw} = \frac{W_{bw} g_{mu} + 2W_{fo} g_{ou}}{C} \tag{3.21}$$

$$\alpha_0 = \frac{W_{bw} g_{mu} + 2W_{fo} g_{ou}}{W_{bw} g_{mu} + 2W_{fo} g_{ou} - g_{m1}} \tag{3.22}$$

For maximum attenuation, the denominator of Eq. 3.11 is set equal to 0, and the result is $g_{m1} = g_{m2} + 2g_{o3}$. Due to mismatch and changes in $g_{m2}$ and $g_{o3}$ as $W_{fo}$ increases, the transconductance of $g_{m1}$ should be tunable. A technique for controlling its value is discussed later, in Chapter IV. Including the digital control, a schematic of the notch filter is provided in Fig. 23. For unity passband gain of the notch filter, $g_{m5}$ and $g_{m6}$ were set equal, such that $g_{m5} = g_{m6} = g_s$. $V_{att}$ is an analog voltage used for controlling the transconductance $g_{m1}$, which in turn controls $\alpha_0$. $W_{on}$ is a single bit control which turns on/off the feedforward path of the bandpass filter. $W_{on}$ should be set to 0 during the symbol periods when there is no interference. By only

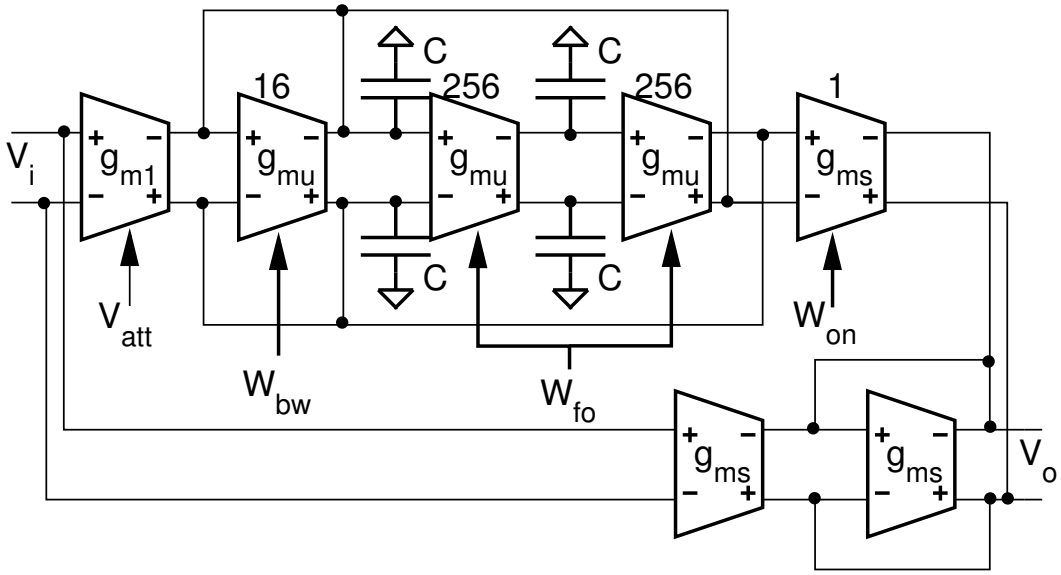



Fig. 23. Notch filter schematic with digital controls $W_{fo}$, $W_{bw}$, and $W_{on}$ and analog control $V_{att}$. The numbers above the OTAs represent the quantity of unit OTAs in the digitally controlled bank of OTAs.

turning on the feedforward path during the symbol period when interference exists, the ringing behavior of the filter is eliminated during the adjacent symbol.

## C. Filter Linearity Requirements

Linearity is an important aspect of many analog circuit designs. Since interference can be large, linearity is an aspect of this design that deserves some attention. For a large interference, harmonics could leak onto neighboring data tones, corrupting the information found in those tones. The UWB baseband spectrum when a high power interferer at SIR=-20 dB is present is displayed in Fig. 24. If a feedforward cancellation technique is used, as in this design, the spectrum at the bandpass filter output, $V_{bp}$ from Fig. 22, will contain the interference as well as its harmonics, as displayed in Fig. 25. After subtraction, the fundamental frequency of the interference will be subtracted out, however, the harmonic frequencies will be passed on to the

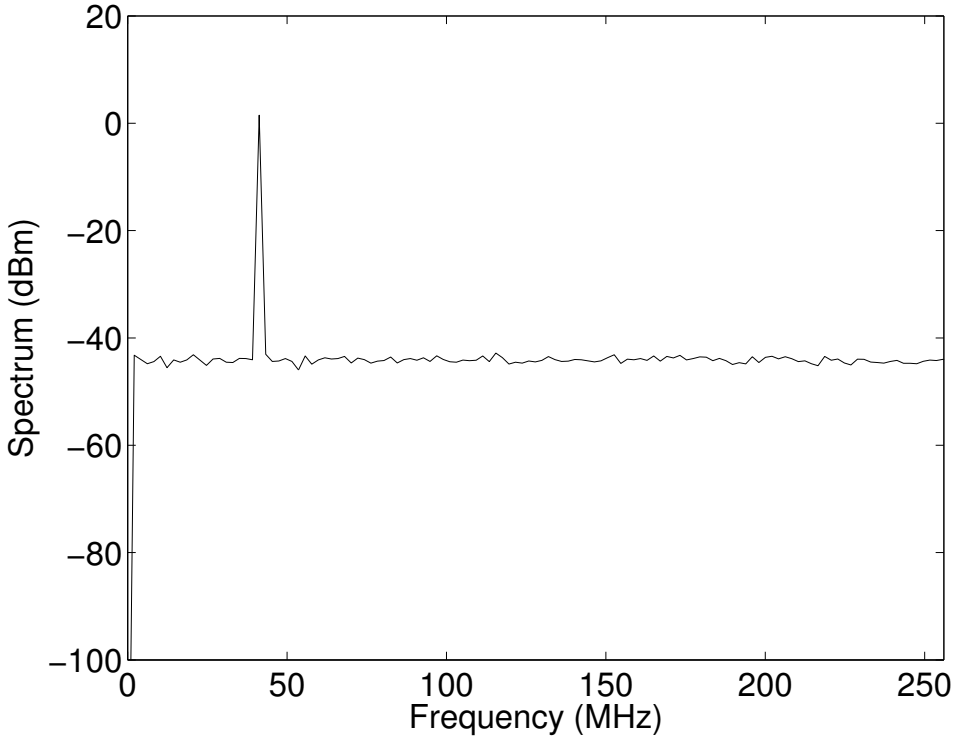



Fig. 24. Spectrum at the filter input, node $V_i$ from Fig. 22, for a high power interference at SIR=-20dB.

output, as shown in Fig. 26. In order for the bandpass filter's nonlinearity to not affect the receiver performance, its harmonics should have power lower than the spectral density of the data tones. At SIR=-20dB, the ratio of the interference power to the data spectral density is 45dB. The HD3 of the bandpass filter should thus be less than -45 dB.

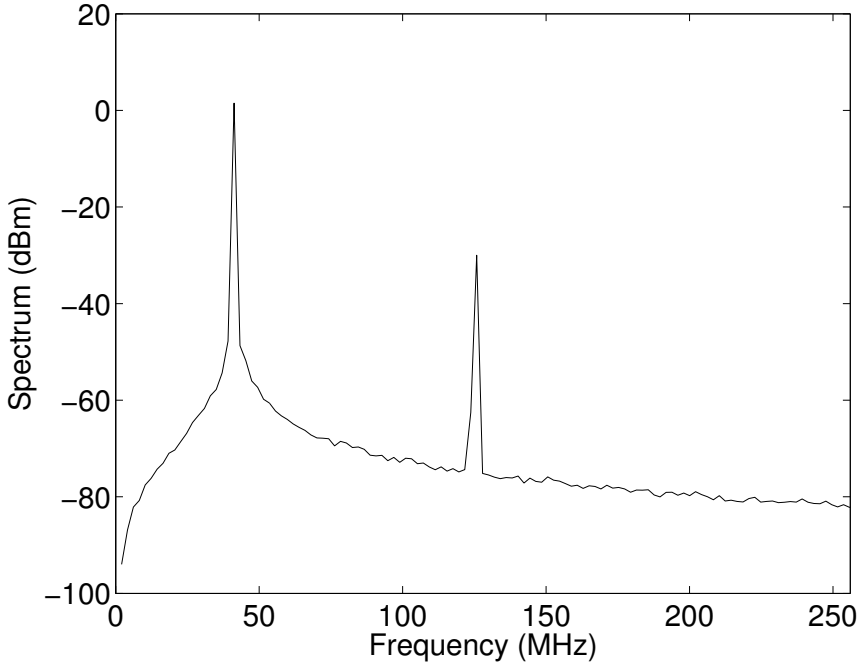



Fig. 25. Spectrum at the bandpass filter output, node $V_{bp}$ from Fig. 22, for a high power interference at SIR=-20dB.

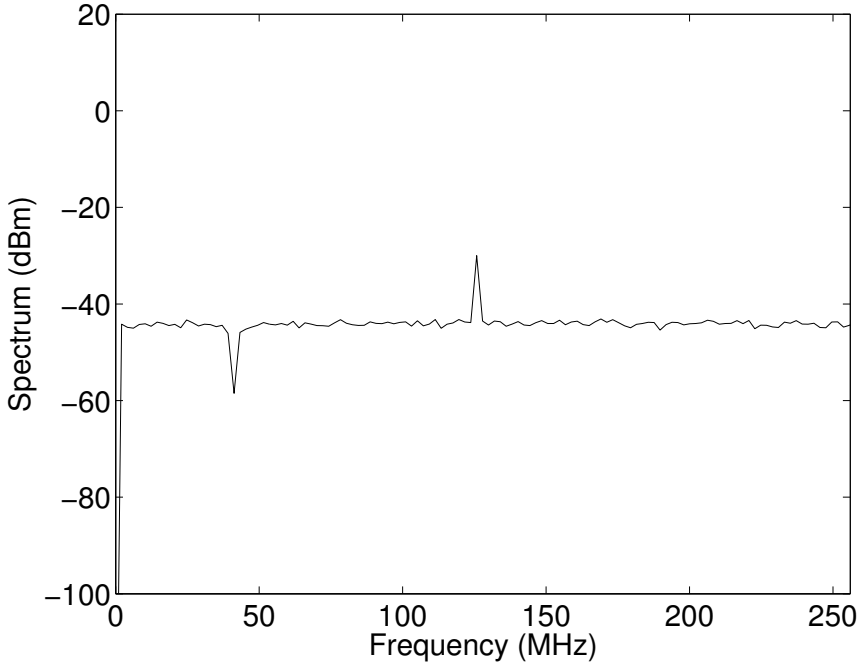



Fig. 26. Spectrum at the filter input, node $V_o$ from Fig. 22, for a high power interference at SIR=-20dB.

# CHAPTER IV

# FILTER TUNING

## A. Center Frequency Tuning

Since the interference frequency could appear anywhere within the UWB baseband at any time, a method must exist for interference detection and center frequency tuning. The `Tuning Algorithm` block from Fig. 22 is completely in software and can thus be tailored to the designer's preference. One potential algorithm for adjusting the filter's center frequency is a guess and search outward algorithm (GSO). A flowchart of the GSO algorithm is provided in Fig. 27. Interference can be detected at the FFT output by comparing the peak FFT bin amplitude to the average. If this difference is above some threshold, this FFT bin is considered interference, and the notch filter is turned on. The control word, $W_{f0}$, is initially set to $W_{f0} = f_{int}/\rho$. The value of the slope, $\rho$, may be adaptively learned, and is initially set to the expected value from simulations. After the filter has settled, the FFT is taken again. If the interference was sufficiently attenuated, the filter is considered tuned, and the algorithm is complete. In all likelihood, due to process and temperature variations, the interference will still exist in the FFT output. If this is the case, $W_{f0}$ is decreased by one, and the FFT is taken again. If the interference still exists, $W_{f0}$ is increased by 2, and pending an incorrect control, will be decreased by 3 such that on the $k$th attempt, the control word will be:

$$W_{f0}[k] = W_{f0}[k-1] + (-1)^{k-1}(k-1) \tag{4.1}$$

This outward search will continue until the interference is sufficiently attenuated in the output of the FFT. Once the filter has been properly adjusted, a new value can be computed for the slope, according to $\rho = W_{f0}/f_{int}$. This will be used for the slope

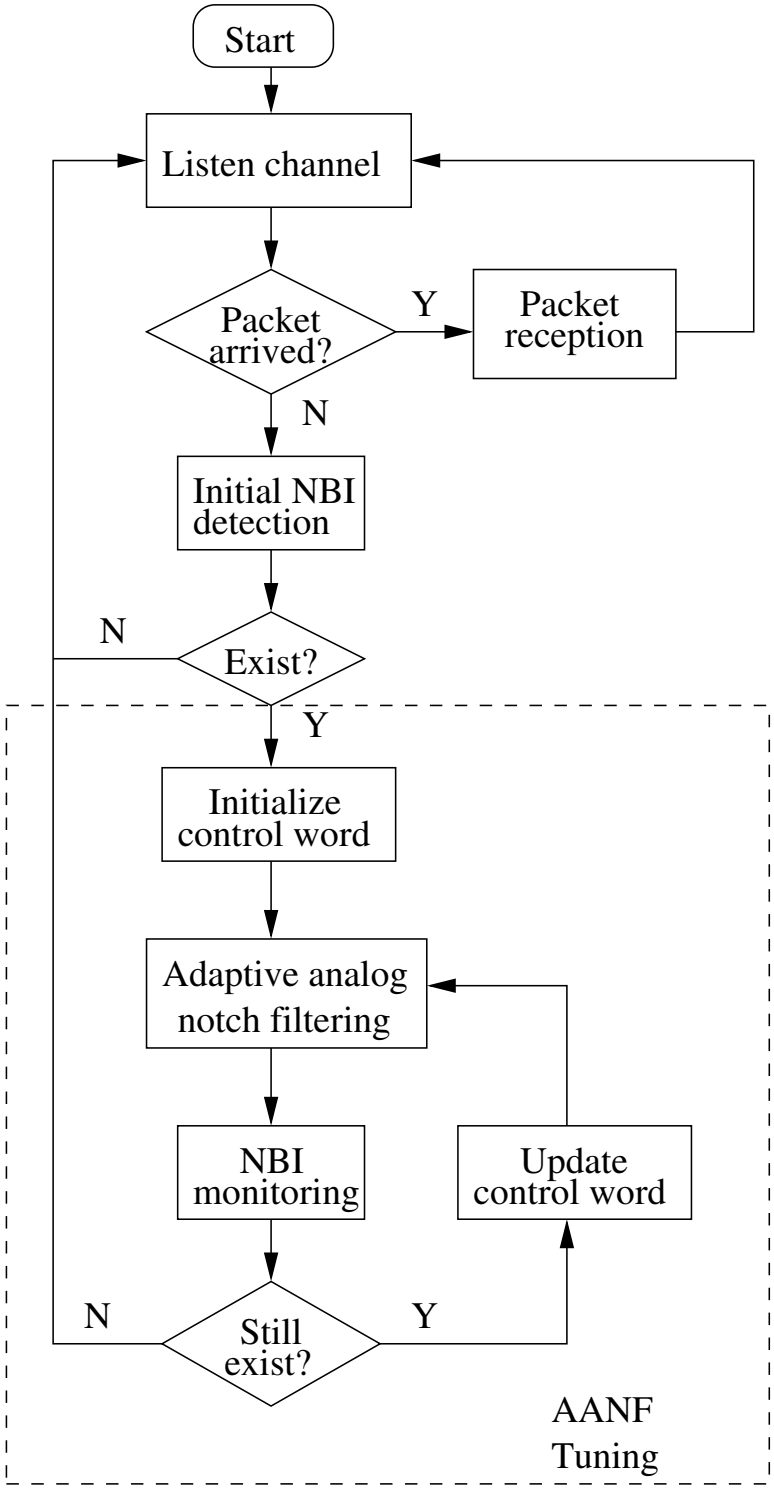



Fig. 27. Flowchart for GSO algorithm used for center frequency tuning.

the next time an interference is detected. By adaptively changing $\rho$, the time required for convergence will be reduced for subsequent interference because the control of the filter is effectively learned by the algorithm.

## B. LMS Gain Control

In the presence of process variations, temperature variations, and mismatch, the design of a bandpass filter with precisely unity passband gain becomes a challenging task. The fact that the filter's center frequency may change from a few MHz to 264 MHz further increases the challenge because unity passband gain needs to be ensured for all filter settings. To address this issue, an analog Least Means Squared (LMS) tuning technique can be applied to the filter. In [18], analog LMS was used to filter meter pulses from subscriber line systems. In [19], LMS was used for filtering co-site interference in military applications. These techniques require the inclusion of multiple instances of analog integrators, summers, and multipliers. However, it is desirable to develop a method which requires the addition of only a few components. In [20], an analog LMS technique was used for Q-Tuning of bandpass filters. This technique can be modified to tune the passband gain of a filter, and requires the addition of only one multiplier and one integrator to the existing filter architecture of Fig. 23. The block level schematic of the notch filter with LMS feedback is displayed in Fig. 28.

Assuming the bandpass filter is properly tuned with center frequency equal to the interference frequency, and noting that $V_o = V_i - V_{bp}$ from Fig. 28, it is seen that:

$$V_{att} = M \int V_{bp}(V_i - V_{bp}) = M \int V_{bp}V_i - V_{bp}^2, \tag{4.2}$$

where $M$ is the conversion gain of the multiplier, $V_{att}$ controls the passband gain of

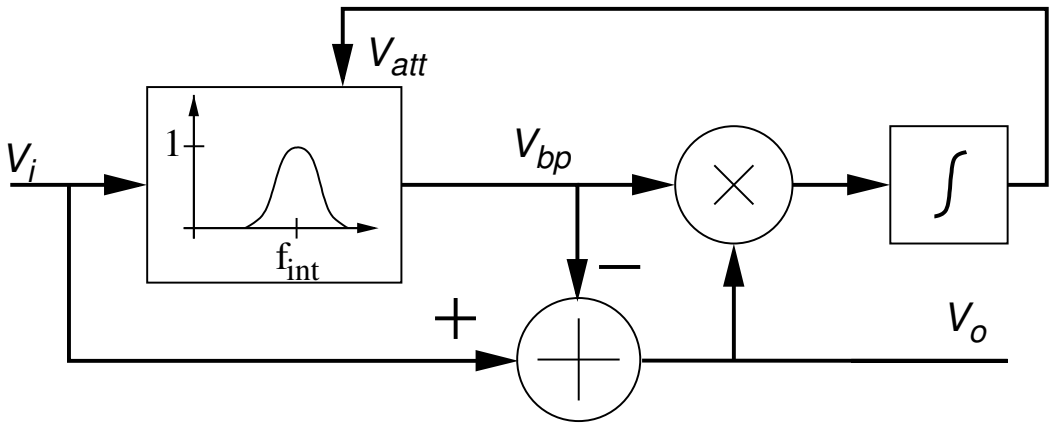



Fig. 28. LMS gain control for the notch filter.

the filter, and accordingly, $\alpha_0$. If the gain of the bandpass filter is less than unity, $|V_{bp}|$ will be less than $|V_i|$, and the interference component of $V_o$ will be in phase with $V_{bp}$. Integration of their positive product will result in increasing $V_{att}$. On the other hand, if the gain of the bandpass filter is greater than unity, the interference component of $V_o$ will be 180° out of phase with $V_{bp}$. Their product will thus be negative, and integration will result in decreasing $V_{att}$, and in turn, the gain of the bandpass filter. Only when the gain of the bandpass filter is precisely unity will the product of $V_o$ and $V_{bp}$ equal zero, and thus no change in $V_{att}$ will occur.

### 1. Limitations of LMS Gain Control

The accuracy of LMS feedback techniques can be sensitive to loop gain, amplitude mismatch, and phase mismatch. Further analysis demonstrates the extent to which these non-idealities affect the gain control loop in Fig. 28.

Assuming the the conversion gain from $V_{att}$ to the amplitude of $V_{bp}$ is $C$, and substituting $V_{bp} = CV_{att}V_i$, $V_{att}$ can be written as:

$$V_{att} = M \int CV_{att}V_i^2 \left(1 - CV_{att}\right) dt \tag{4.3}$$

If $V_i$ is a sinusoidal interferer, such that $V_i = A\sin(\omega_i t)$, then

$$V_{att} = M \int CV_{att}A^2 \left(1 - CV_{att}\right) \left(\frac{1 - \cos(2\omega_i t)}{2}\right) dt \tag{4.4}$$

Computing the average value of the integral, the result is:

$$\bar{V_{att}} = \frac{MCA^2 - 2}{MC^2A^2} \tag{4.5}$$

The output, $V_o$ now becomes:

$$V_o = -\sin(\omega_i t) \left(\frac{2}{MCA}\right) \tag{4.6}$$

Finally, dividing the input by the output, the attenuation is:

$$\alpha_0 = \frac{MCA^2}{2} \tag{4.7}$$

The result of Eq. 4.7 indicates that the attenuation achieved by the LMS loop depends on the square of the interference amplitude itself. Thus, this technique may not be suitable for filtering signals with small amplitudes. However, since in this application the filter is used to mitigate large interference signals, this is not a big constraint on the filter design.

The previous analysis assumes perfect matching between the two forward paths of the design. However, this is not a practical assumption due to transistor mismatch in CMOS processes. The following analysis assumes a mismatch factor, $\delta_{mm}$, in the subtracter, such that $v_o = v_i - (1 - \delta_{mm})v_{bp}$. Now, $V_{att}$ can be written as:

$$V_{att} = M \int \left(V_i V_{bp} - (1 - \delta_{mm})V_{bp}^2\right) \tag{4.8}$$

Rewriting $V_{bp}$ as $V_{bp} = CV_{att}V_i$,

$$V_{att} = M \int CV_{att}V_i^2(1 - CV_{att})(1 - \delta_{mm})dt \tag{4.9}$$

Substituting $V_i = A\sin(\omega_i t)$,

$$V_{att} = M \int CV_{att}A^2(1 - CV_{att})(1 - \delta_{mm}) \left( \frac{1 - \cos(2\omega_i t)}{2} \right) dt \tag{4.10}$$

The average value of the integral becomes:

$$\bar{V_{att}} = \frac{MCA^2 - 2}{MC^2A^2(1 - \delta_{mm})} \tag{4.11}$$

The resulting output voltage is:

$$V_o = -\sin(\omega_i t) \left( -A \frac{\delta_m m}{1 - \delta_{mm}} \frac{2}{MCA} (1 - \delta_{mm}) \right) \tag{4.12}$$

For large enough loop gain and signal amplitude, the mismatch will be the dominant nonideality, and the achieved attenuation can be approximated by:

$$\alpha_0 \approx \frac{1 - \delta_{mm}}{\delta_{mm}} \tag{4.13}$$

Thus for $\alpha_0$ greater than 20dB, the mismatch, $\delta_{mm}$ must be limited to $\delta_{mm} < 9.1\%$. This amount of mismatch is feasible in today's CMOS technologies, thus, mismatch should not keep the filter from performing to specification.

Finally, phase mismatch between the two forward paths could also degrade the filter's performance. For this analysis, assume that the bandpass filter phase shifts the input, such that $V_{bp} = V_i e^{j\theta}$. This could either be due to mismatch or inexact center frequency tuning in the bandpass filter. The output of the notch filter now becomes:

$$V_o = V_i - V_{bp} = A\sin(\omega t) - A\sin(\omega t + \theta) \tag{4.14}$$

which is trigonometrically equivalent to

$$V_o = A\sqrt{2(1 - \cos(\theta))}\sin(\omega t + \theta) \tag{4.15}$$

The attenuation thus becomes:

$$\alpha_0 = \frac{1}{\sqrt{2(1-\cos(\theta))}} \tag{4.16}$$

To obtain $\alpha_0 > 20dB$, it is required that $\theta < 5.7°$. To see if this is a problem in this design, the phase difference between two adjacent center frequency steps must be calculated. If that difference is less that 5.7°, then phase errors are not a limiting factor in the filter performance. The transfer function of the bandpass biquad is known to be:

$$\frac{V_o}{V_i} = \frac{\omega_{bw} s}{s^2 + \omega_{bw} s + \omega_o^2} \tag{4.17}$$

The phase at frequency $\omega$ is calculated to be:

$$\theta\left(\frac{V_o}{V_i}\right) = -\tan^{-1}\left(\frac{\omega_o^2 - \omega^2}{\omega_{bw}\omega}\right) \tag{4.18}$$

In the worst case, the interference will occur directly in between two adjacent center frequency steps, such that $\omega = \omega_o + \rho/2$. Where $\rho$ is the frequency step. The worst case phase error caused by the filter is derived to be:

$$\theta_{max}\left(\frac{V_o}{V_i}\right) = -\tan^{-1}\left(\frac{\omega_o\rho + \rho^2/4}{\omega_{bw}(\omega_o + \rho/2)}\right) \approx -\tan^{-1}\left(\frac{\rho}{\omega_{bw}}\right) \tag{4.19}$$

In this design, $\rho$ was designed to be $2\pi 1.3$ Mrad/s. The maximum phase error is thus $\theta_{max} < 2°$. This is less than the requirement of 5.7°. If the phase at the node $V_{bp}$ from Fig. 28 is too high or low, the center frequency of the filter can be adjusted to compensate for the error.

# CHAPTER V

## TRANSISTOR LEVEL DESIGN AND SIMULATION RESULTS

Based on the filter's architecture and specifications outlined in the previous chapter, the analog building blocks were designed at the transistor level. Since many of the controls of the filter are discrete, some digital building blocks were also designed. Once these blocks were created and simulated, simulations were performed on the entire notch filter. The design was performed in Cadence using TSMC's 0.18 $\mu$m design kit.

### A. Analog Building Blocks

There are three major analog building blocks used in the design of the notch filter. The first is the unit OTA used in the implementation of the bandpass biquad. The second is the OTA used in the subtracter design. Finally, a multiplier is designed for use in the LMS gain control tuning scheme.

#### 1. OTAs Used in the Bandpass Biquad

The small signal operation of the unit OTA from the bandpass biquad can be developed based on the biquad's specifications. The desired DC voltage gain of the OTA is determined from the bandwidth requirement. It is desired that the bandwidth remain nearly constant regardless of $W_{fo}$. Substituting Eq. 3.16 into Eq. 3.21, and setting the derivative with respect to $W_{fo}$ equal to 0 yields:

$$\frac{d\omega_{bw}}{dW_{fo}} = 2g_{ou} - \frac{g_{mu}}{16} = 0, \tag{5.1}$$

from which it is determined that the DC voltage gain of the OTA, $A_{vu}$, should be $A_{vu} = g_{mu}/g_{ou} = 32$ V/V= 30.1 dB.

A schematic of the switchable unit OTA used in this design is displayed in Fig. 29. $V_B$ is a DC bias generated from the current reference formed with $I_{ref}$ and $M_{ref}$. $V_{CMFB}$ is generated from a common mode feedback circuit. The OTA's switching operation is as follows. If $D_1D_0 = 00$, the gates of the biasing transistors $M_{2a}$ and $M_{2b}$ are switched to ground, and the gates of the common mode feedback transistors, $M_{3a,b}$ and $M_{4a,b}$ are switched to $V_{DD}$. This effectively turns off the OTA by driving no bias current through the driver transistors, $M_{1a}$ and $M_{1b}$. When $D_1D_0 = 01$, the gate voltage of $M_{2a}$ becomes $V_B$, forming a current mirror with $M_{ref}$ and the OTA is biased with a current equal to $I_{ref}$. The gates of $M_{3a}$ and $M_{3b}$ are tied to $V_{CMFB}$ supplying the common mode feedback current to the OTA. Finally, if $D_1D_0 = 11$, transistors $M_{2b}$, $M_{4a}$, and $M_{4b}$ turn on, and the OTA is biased with a current equal to $2I_{ref}$. Because there are three unique states to this OTA, $D_1D_0 \in [00, 01, 11]$, one of these OTA building blocks represent two unit OTAs, $g_{mu}$ from Fig. 23. Note that $D_1D_0 = 01$ is the same as $D_1D_0 = 10$ because $D_1$ and $D_0$ control transistors with equal sizes. The simulated characteristics of the OTA are provided in Table IV. The unit transconductance is calculated to be $g_{mu} = 30.2$ $\mu$A/V and is found by dividing the transconductance when $W_{fo}$ is at its maximum by $W_{fo}$. From Eq. 3.20, $C$ is determined to be $C = 3.85$ pF, resulting in $\omega_{bw} \approx 2\pi 20$Mrad/s. A plot of the simulated transconductance and OTA gains are provided in Figs. 30 and 31, respectively.

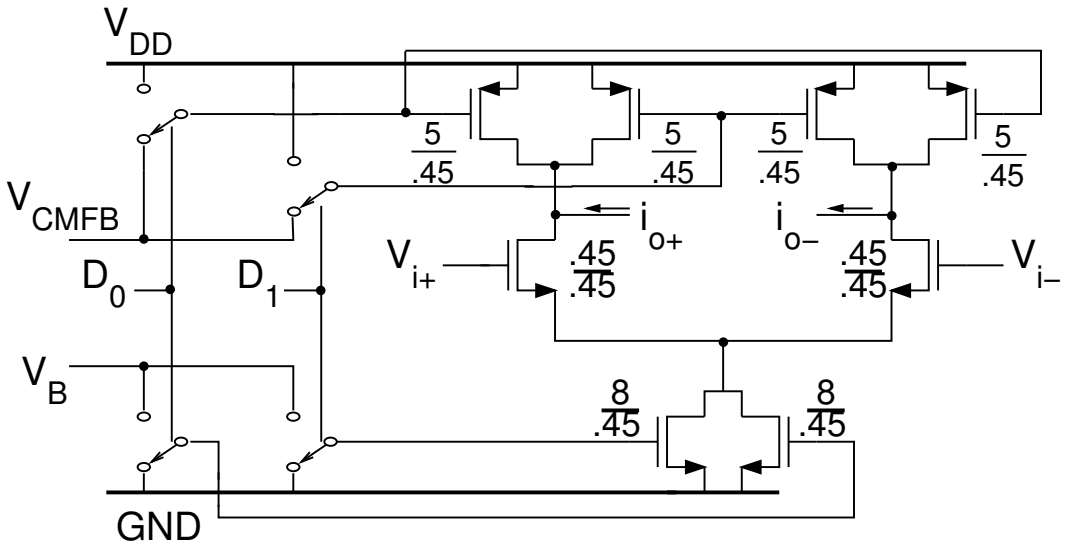



Fig. 29. Switchable unit OTA used in the notch filter.

Table IV. Simulated switchable unit OTA characteristics

| **State** $D_1D_0$ | $g_m$ ($\mu$A/V) | $A_{vu}$ (dB) |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 41.8 | 30.9 |
| 11 | 60.4 | 29.5 |

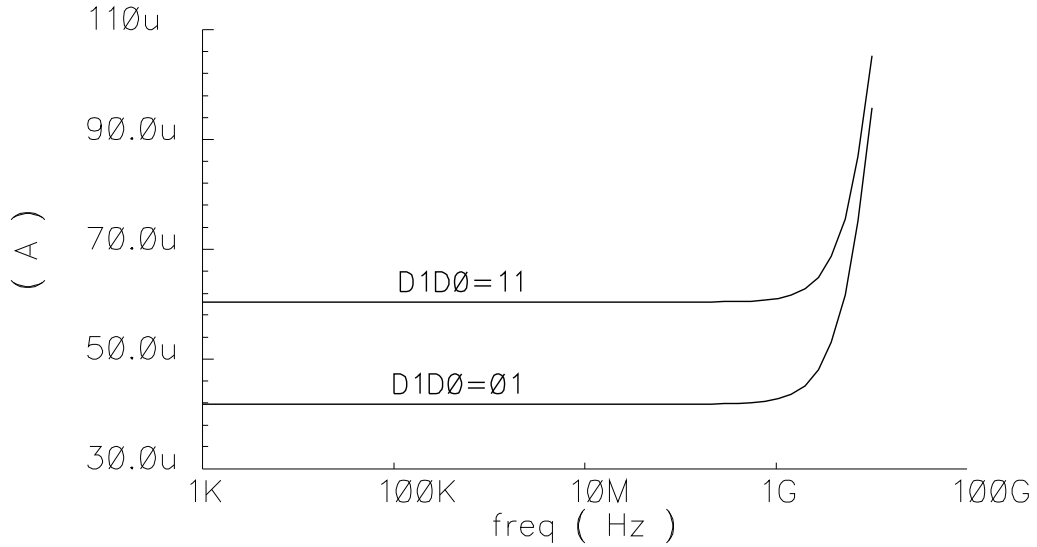



Fig. 30. Simulated transconductance vs. frequency for the switchable OTA used in the bandpass biquad.

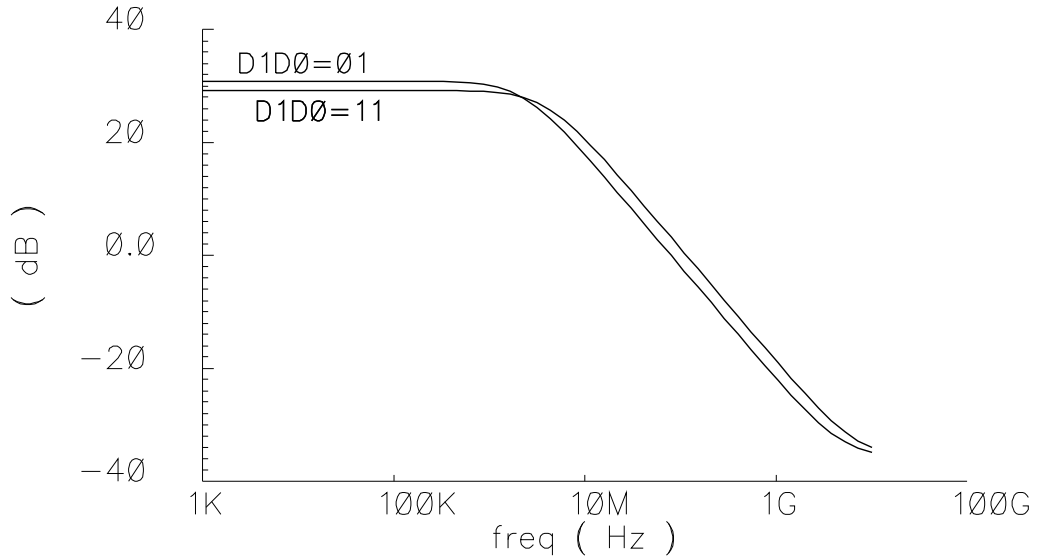



Fig. 31. Simulated voltage gain vs. frequency for the switchable OTA used in the bandpass biquad.

Table V. Simulated subtracter OTA characteristics

| **Parameter** | **Value** |
|---|---|
| Transconductance | 6.72 mA/V |
| DC Voltage Gain | 21.1 dB |
| Integrated Noise | $5.3nV^2$ |
| HD3 | $-69.9$ dB |

2. OTAs Used in the Subtracter

Since the requirements of the OTAs used in the subtracter, $g_{ms}$ from Fig. 23, are different from those used in the bandpass biquad, the performance requirements are also different. The noise, linearity, and speed of these OTAs are the important parameters. This is because the forward path OTA and the OTA used in the active resistor configuration, respectively $g_{m5}$ and $g_{m6}$ from Fig. 21, are always on, even when the notch filter is turned off. A schematic of the OTA utilized for the subtracter is displayed in Fig. 32. The simulated transconductance, voltage gain, and input referred noise spectrum are provided in Figs. 33, 34, and 35, respectively. The resulting FFT of the output current in response to a 400mV amplitude, 70MHz sinusoid is displayed in Fig. 36. A summary of the results from these simulations is given in Table V.

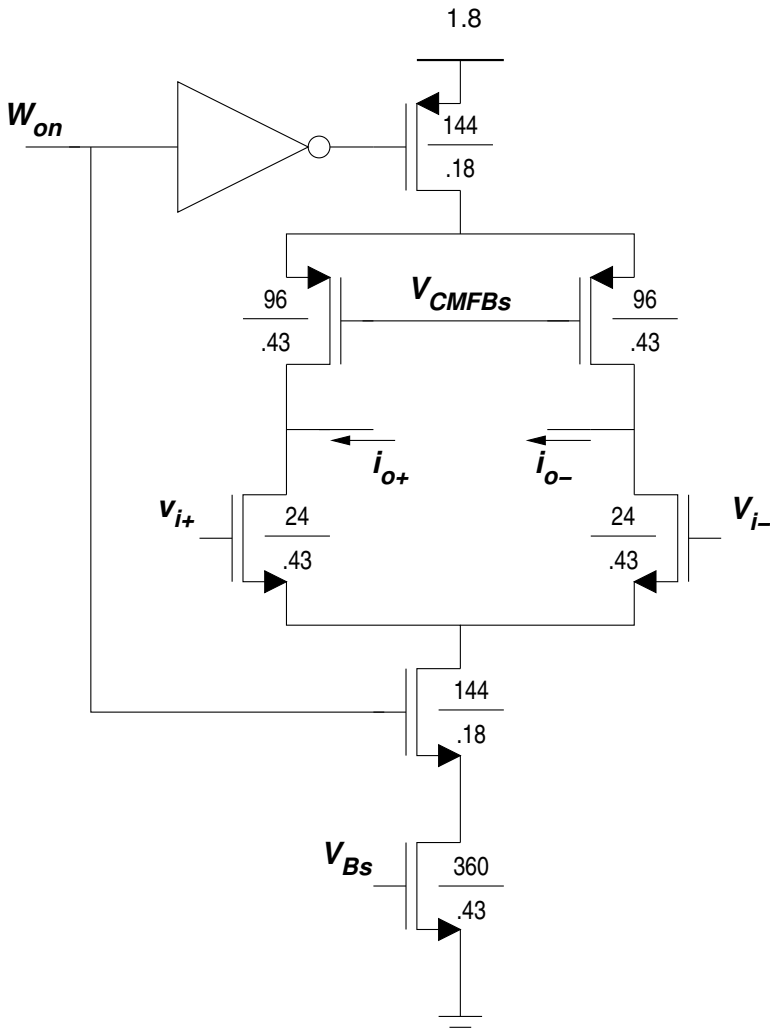



Fig. 32. Switchable OTA used in the subtracter.

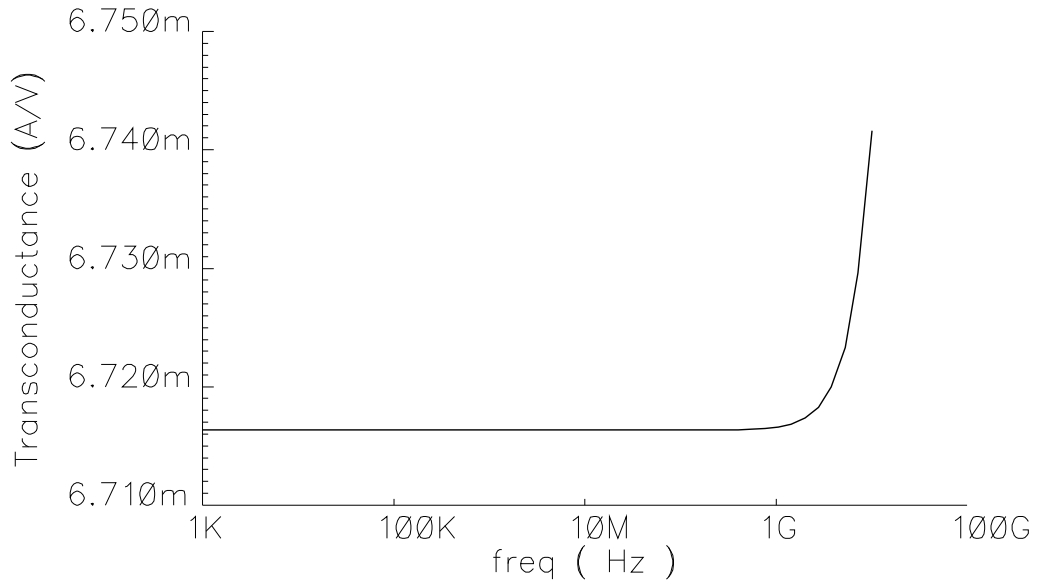



Fig. 33. Simulated transconductance vs. frequency for the OTA used in the subtracter.

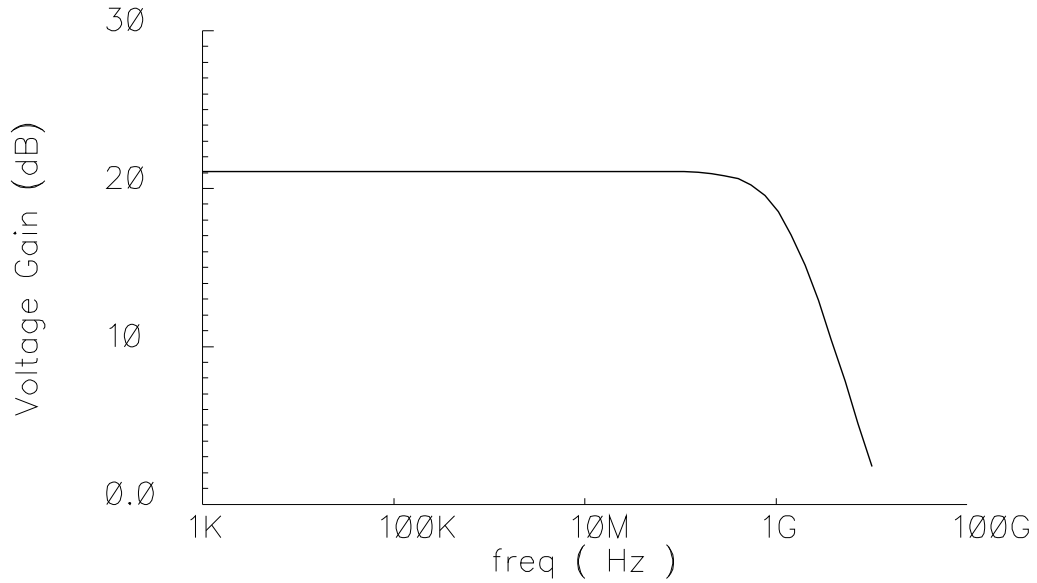



Fig. 34. Simulated voltage gain vs. frequency for the OTA used in the subtracter.

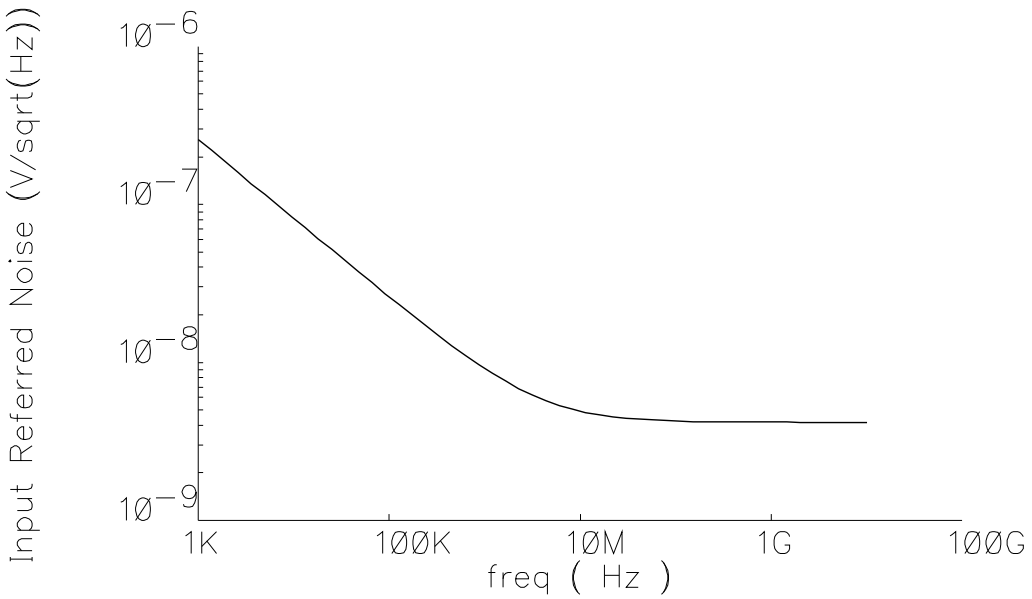



Fig. 35. Simulated input referred noise vs. frequency for the OTA used in the subtracter.

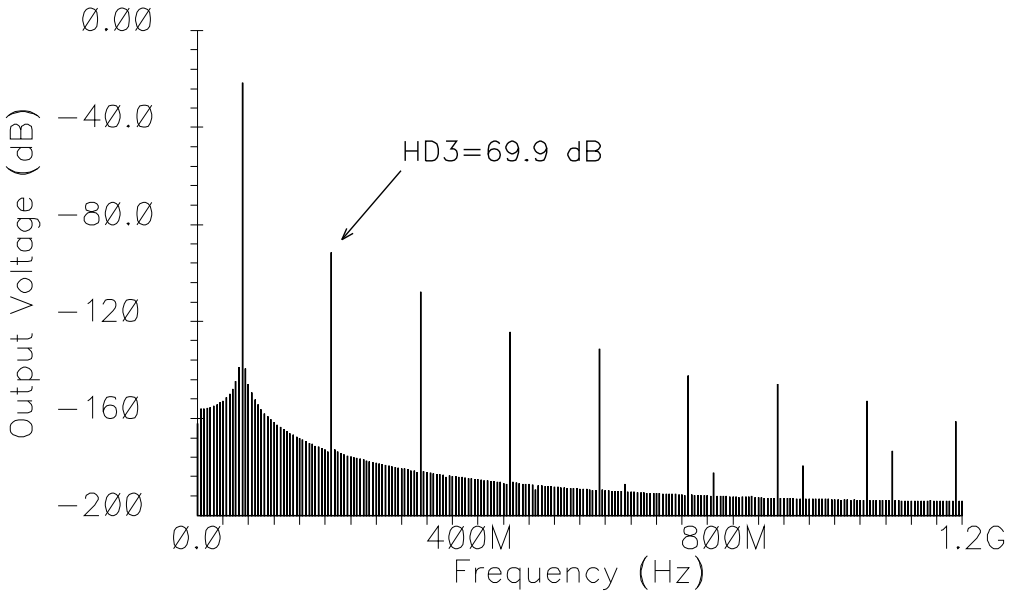



Fig. 36. FFT of output current for the OTA used in the subtracter when $v_{in} = 0.4sin(2\pi 70M)$.

### 3. Multiplier

Multipliers based on transconductance cells are an attractive option for implementing the multiplier because their output is a current. The integrator cell from Fig. 28 can thus be implemented by simply adding a capacitor to the output of the mixer. Many transconductance multipliers exist in the literature [21]. In this work, the multiplier from [22] was used because it accepts inputs with the same common-mode voltages without needing any level shifting circuitry. A CMOS schematic of the multiplier is provided in Fig. 37. $V_P$ and $V_{CM}$ are DC biasing voltages generated from a current reference. $V_{CMFBn}$ is generated from a common-mode feedback circuit. $W_{on}$ is the same digital control that was used in Fig. 23. During symbol periods where there is no interference, $W_{on} = 0$, and $V_{att}$ will be stored on the integrating capacitor. When the symbol period that contains the interference becomes active again, $V_{att}$ will already be near the correct value, and $W_{on} = 1$ to resume the LMS convergence. $V_{bp}$, $V_o$, and $V_{att}$ are connected to their respective nodes from Fig. 28.

The multiplier was independently simulated to verify its operation. Figure 38 displays the resulting output voltage due to a DC sweep of its inputs. Figures 39 and 40 respectively show the transient and frequency response of the multiplier for input frequencies of 200MHz and 220MHz. As expected, the output voltage has been mixed down to the modulated frequency of 20MHz.

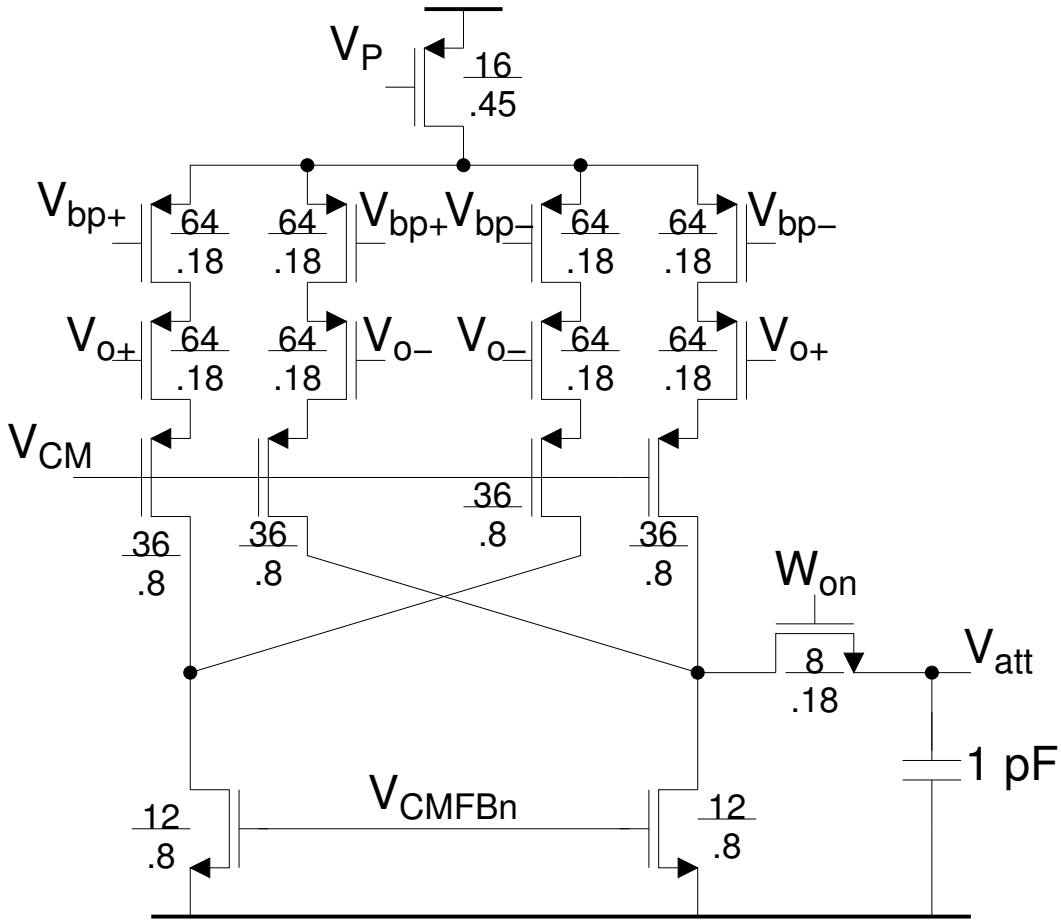



Fig. 37. Schematic of the multiplier/integrator.

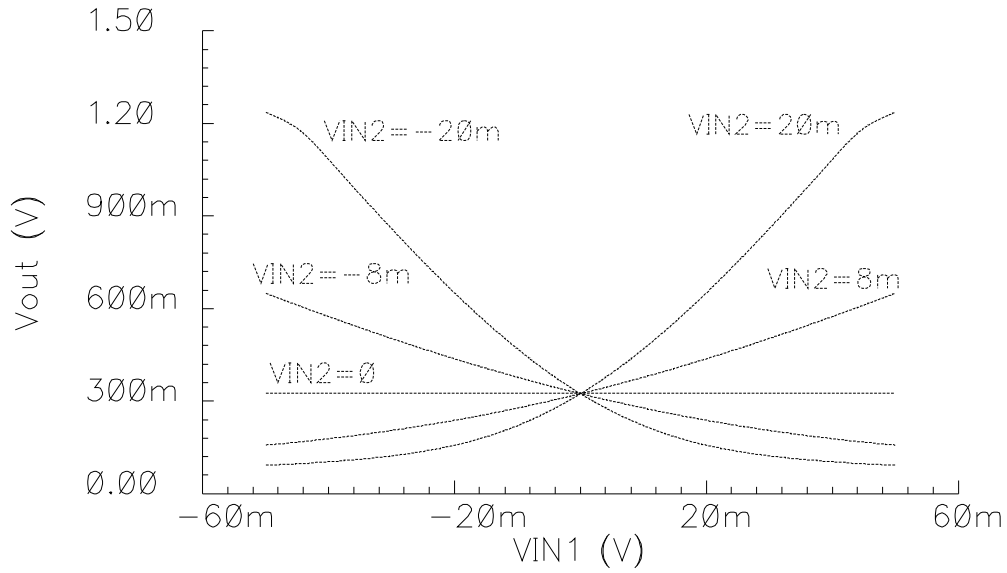



Fig. 38. DC response of the multiplier.

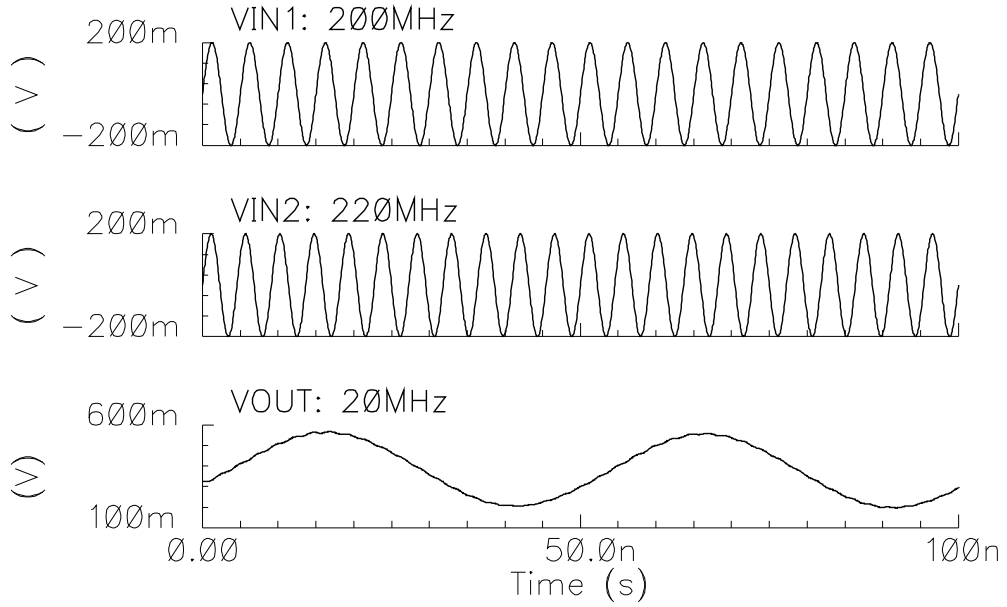



Fig. 39. Transient response of the multiplier. When multiplied together, the input frequencies of 200MHz and 220MHz are mixed down to 20MHz.

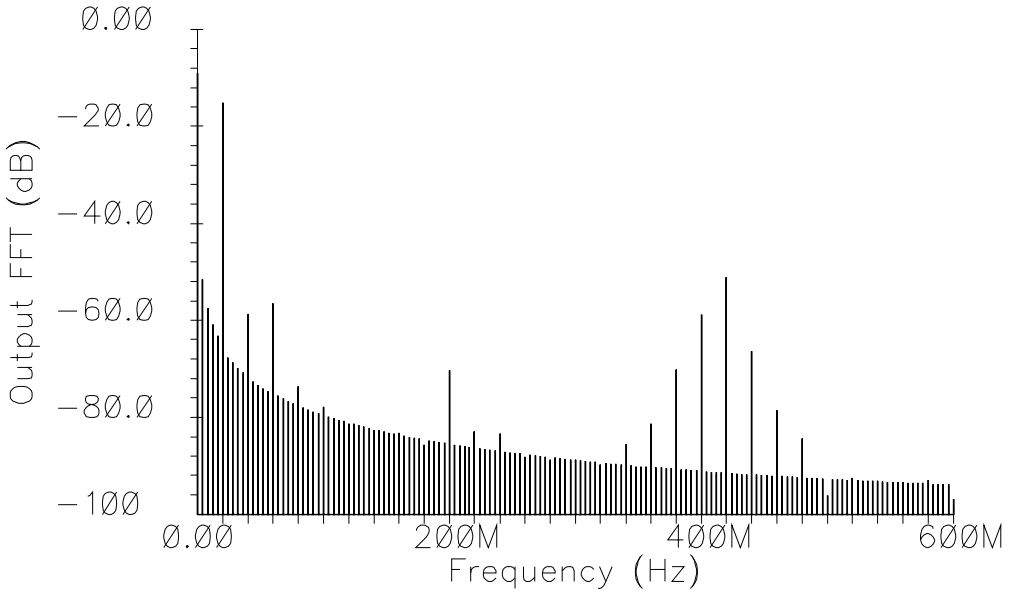



Fig. 40. FFT of the mixer output for inputs with frequencies 200MHz and 220MHz. The dominant tone in the output is at 20MHz.

## B. Digital Building Blocks

### 1. Binary to Thermometer Code Converter

Due to mismatch, a binary coded programmable OTA could leave large gaps in the achievable notch frequencies, resulting in the inability to filter certain interferences. Usually, this would occur when the MSB of the control flips (ie. W goes from 01111111 to 10000000). To prevent this from occurring, the OTAs were designed to be thermometer coded. However, directly controlling 8 bits of thermometer coded data requires 255 controls, which is too many for practical design of the controlling circuitry. Thus, an 8 bit binary to thermometer code converter was designed. The design was performed in Verilog HDL, and was synthesized using a digital library.

### 2. Filter Select

It has been shown that the notch filter should only be turned on during the times that the subband with interference is active. This prevents the residual settling of the filter from impacting the data during the next time interval. Figure 41 displays the gate level logic used for this purpose. Only when the clock signal for one of the frequency bands and the select signal for the same band are high will the filter be enabled.

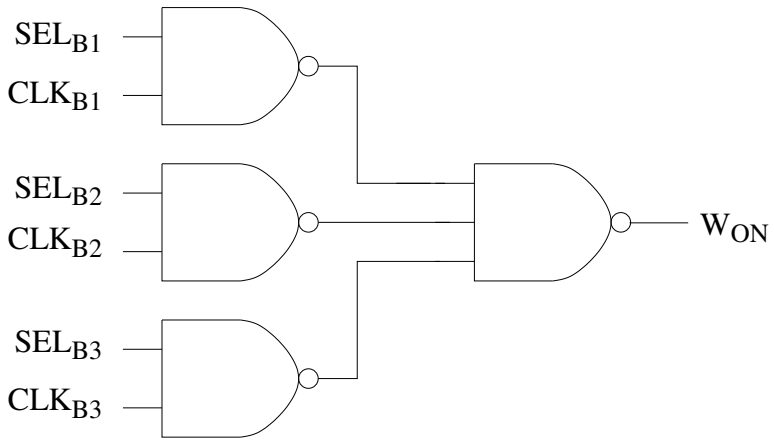



Fig. 41. Digital logic for controlling the enable signal, $W_{ON}$.

## C. Filter Simulations

To predict the filter's performance, both AC and transient simulations were run.

### 1. AC Simulations

The control word, $W_{fo}$, was swept from 0 to 255, and the resulting current consumption, center frequency, and -3 dB bandwidth are plotted in Fig. 42. As expected, the current consumption and center frequency increase linearly with $W_{fo}$. The simulation indicates that the center frequency of the filter has a tuning range from 1.4 MHz to 291 MHz. The simulations also indicate that the filter's -3 dB bandwidth remains nearly constant, only varying from 20.5 Mhz to 24.7 Mhz across the tuning range. Figure 43 displays the AC magnitude response of the filter for $W_{fo}$ values 1–5. Alternatively, Fig. 44 provides the AC magnitude response for $W_{fo}$ values of 170–175. From these plots, it is evident that the intersection of any two adjacent plots occurs below -20 dB. The resulting conclusion is that any frequency could thus be attenuated by at least -20 dB, even if it does not fall exactly on one of the discrete tuning frequency steps. .

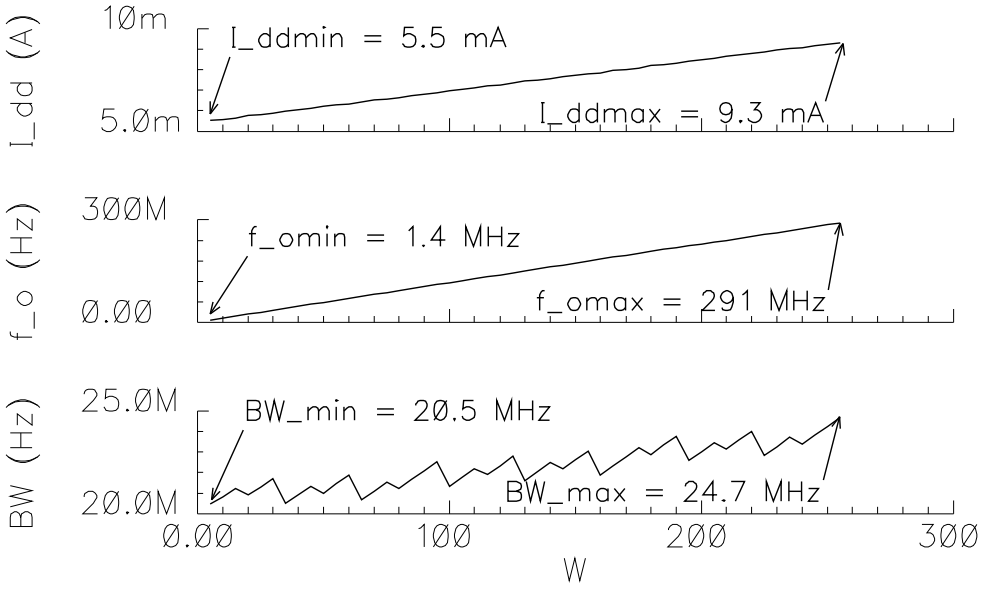



Fig. 42. Notch filter's current consumption, center frequency, and -3 dB bandwidth for different values of the control word, $W_{fo}$.

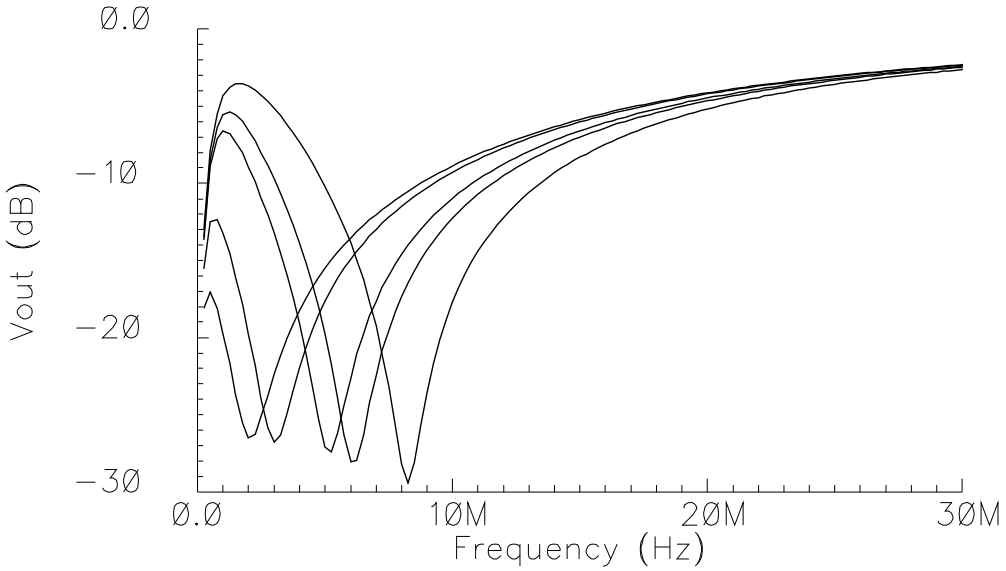



Fig. 43. AC magnitude response for $W_{fo}$ settings 1 through 5.

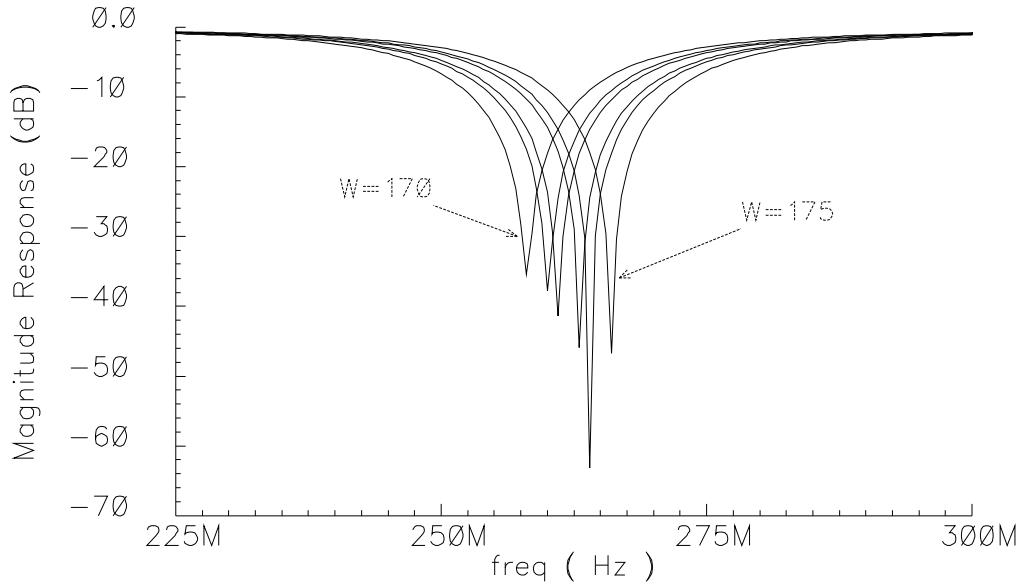



Fig. 44. AC magnitude response for $W_{fo}$ settings 170 through 175.

### 2. Transient Simulations

Figure 45 displays the filter input, output, and the LMS gain control, $V_{tune}$, for $V_i = 0.15\sin(2\pi 250e6) + S_{uwb}$, where $S_{uwb}$ is a representation of an actual UWB signal, when the receiver is operating at the sensitivity level. During the time interval that interference does not exist, the voltage $V_{tune}$ holds its value. This is due to switching the control $W_{on}$ in Fig. 37, causing the integrating capacitor to hold its charge while the tuning circuitry is not active. This helps reduce the settling time the next time interference appears. The desired result would be for the output signal to still contain the $S_{uwb}$ signal while removing the interference sinusoid. The actual result shows a greatly reduced interference on $V_o$. The interference is still too large to tell how the UWB signal was affected by the filtering just by looking at the time domain waveform. Taking the FFT of the signals and looking at the frequency domain behavior should provide more insight into this. Figure 46 displays the resulting FFT of the input

and output signals from Fig. 45. Observing the FFT of $V_i$, it is clear that there exists a single tone interference on top of UWB signal that is white across the UWB bandwidth. The output signal shows the interference attenuated by over 20 dB, with little affect on the amplitude of the UWB data signals.

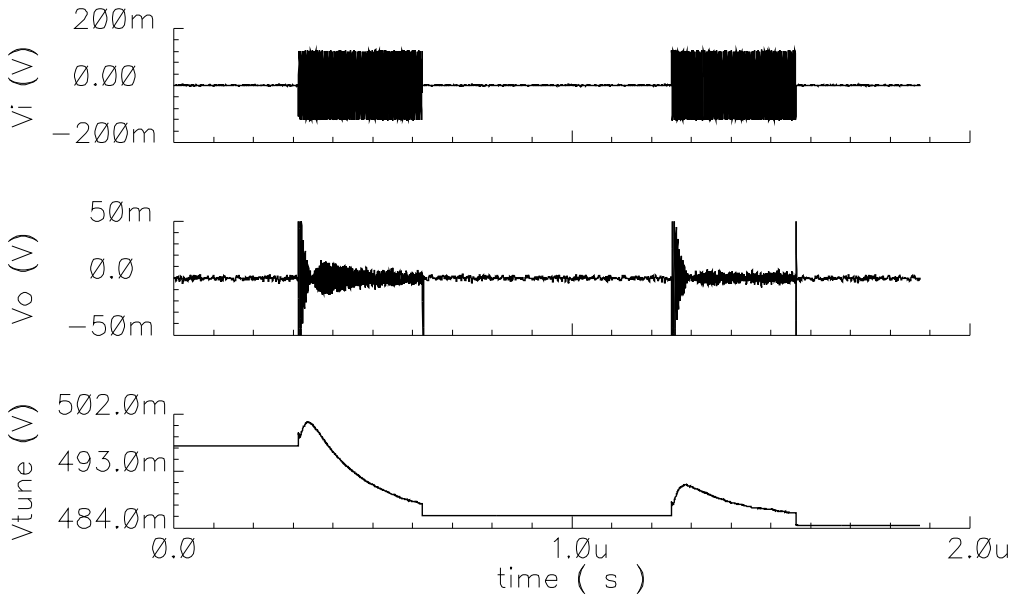



Fig. 45. Simulated transient behavior of filter input, output, and LMS control.

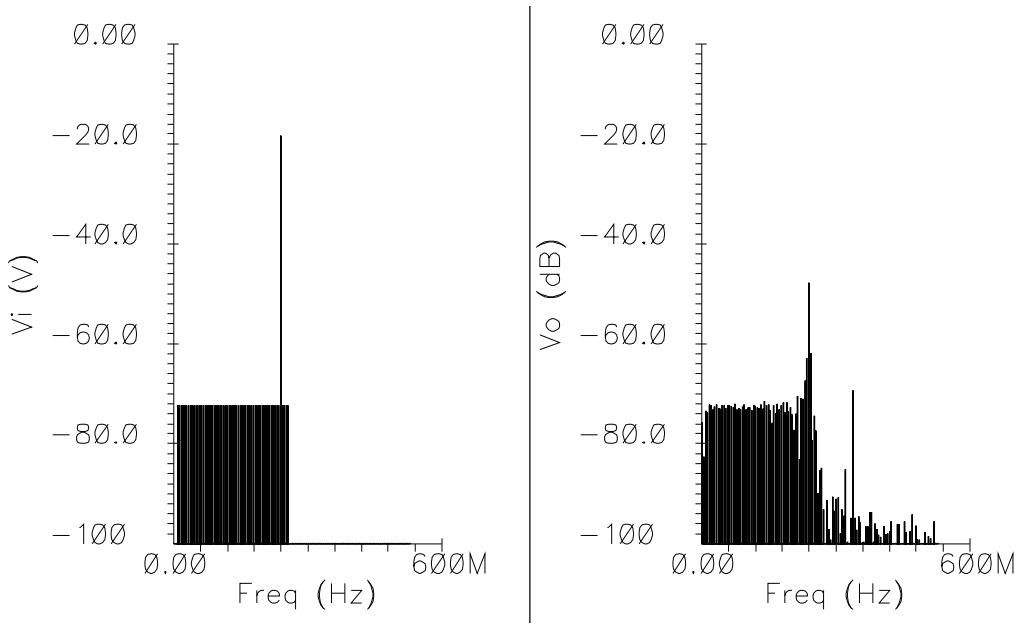



Fig. 46. FFT results of transient simulation from Fig. 45.

# CHAPTER VI

# FILTER LAYOUT

Because the filter uses an 8-bit thermometer coded bank of OTAs, the physical design lends itself to a modular, repetitive layout. In such a large design, this is important so that small changes in the design do not take too long to change in the layout. For this design, the filter was built using blocks of eight OTAs, each with its own common mode feedback. In this section, the development of the layout hierarchy is described..

## A. Layout of the OTAs Used in the Filter

### 1. Developing the Building Block Cell

All of the OTAs in the filter were developed such that the same building block cell was used in their design. A schematic of a single OTA is displayed in Fig. 47. The building block cell used for the layout consists of eight of these single OTAs combined with one of the common mode feedback cells, whose schematic is provided in Fig. 48.

Figure 49 displays the physical design of the building block cell. The labeling corresponds to that of Fig. 47. The wide metal trace around the block are power and ground lines. The signal routing is laid out in between the NMOS drivers and the PMOS load. These lines span the entire width of the layout so that cascading multiple cells horizontally maintains their continuity. At this point, connections are not made to the signal routing because their connections will depend on which OTA the cell is being used in. Figure 50 displays how the single OTAs and CMFB circuitry are combined to form the building block cell. The latter is placed on the outside of the cell to match better the single OTAs, which are horizontally cascaded in the cell's interior.

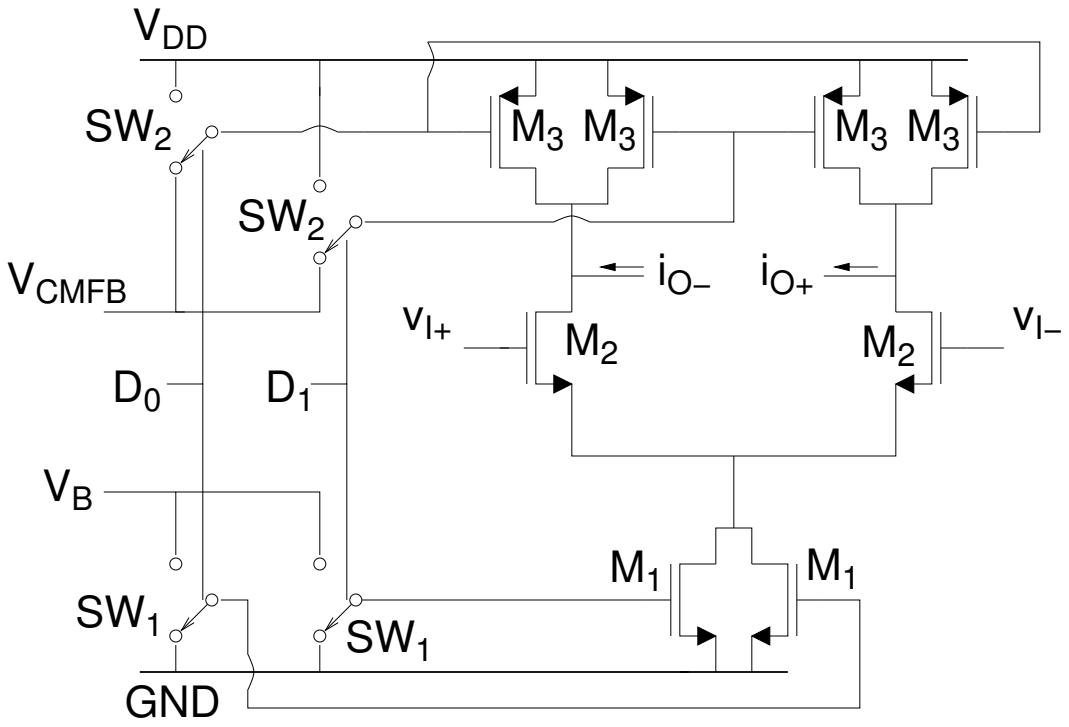



Fig. 47. Schematic of the OTA used in the bandpass filter.

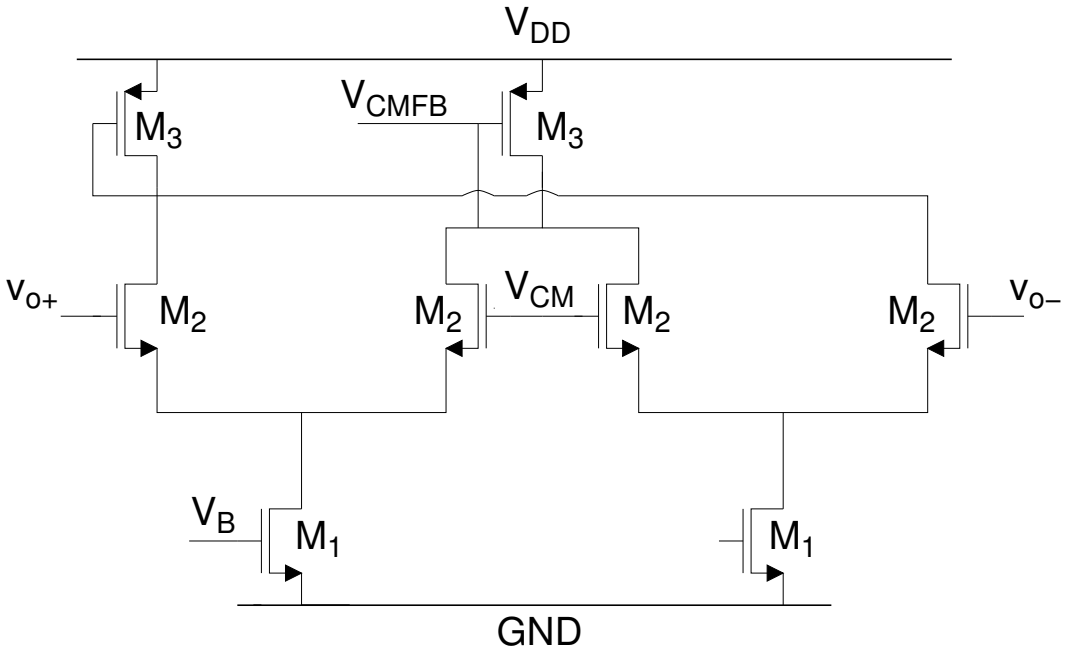



Fig. 48. Schematic of the common mode feedback circuitry used in the bandpass filter.

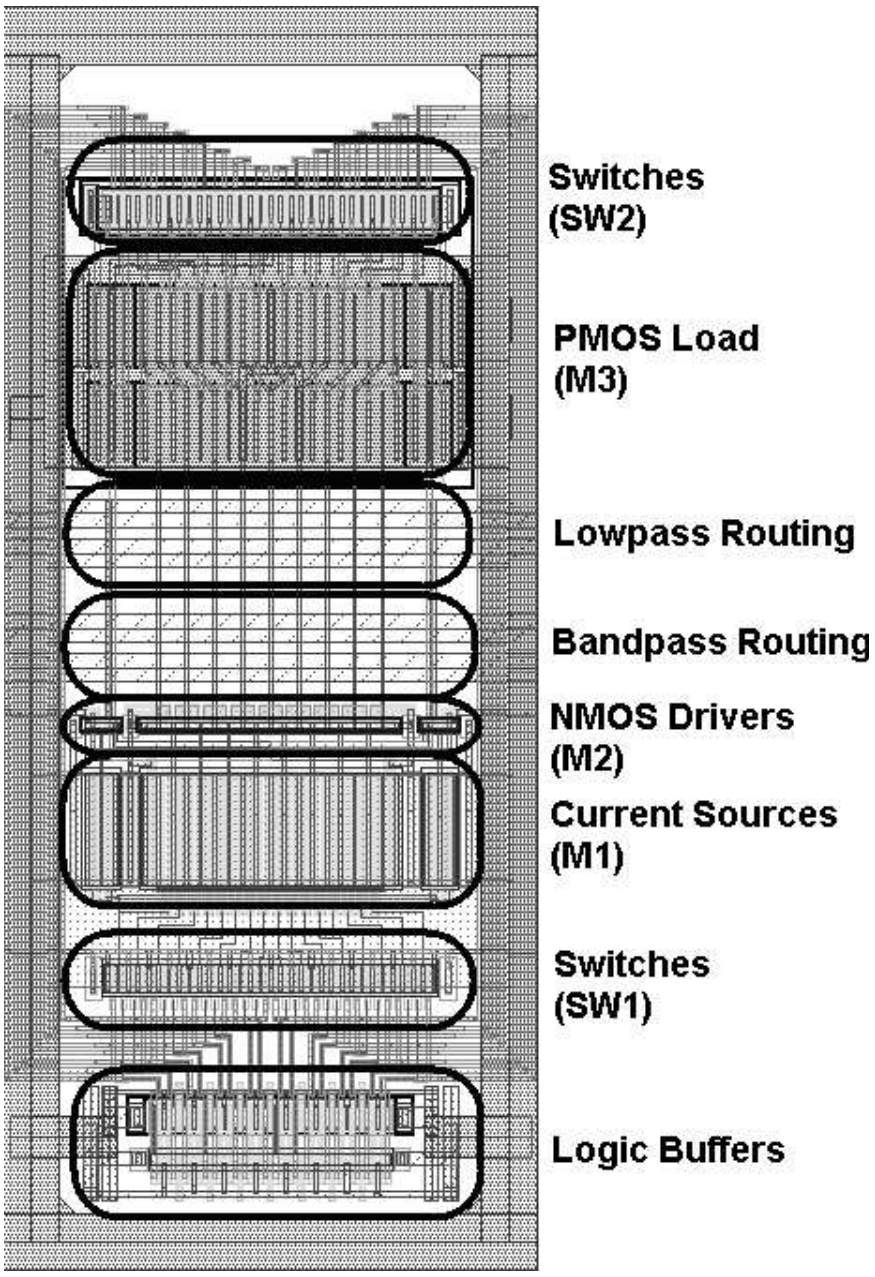



Fig. 49. Building block layout for OTAs in the bandpass filter. The location of the devices are labeled.

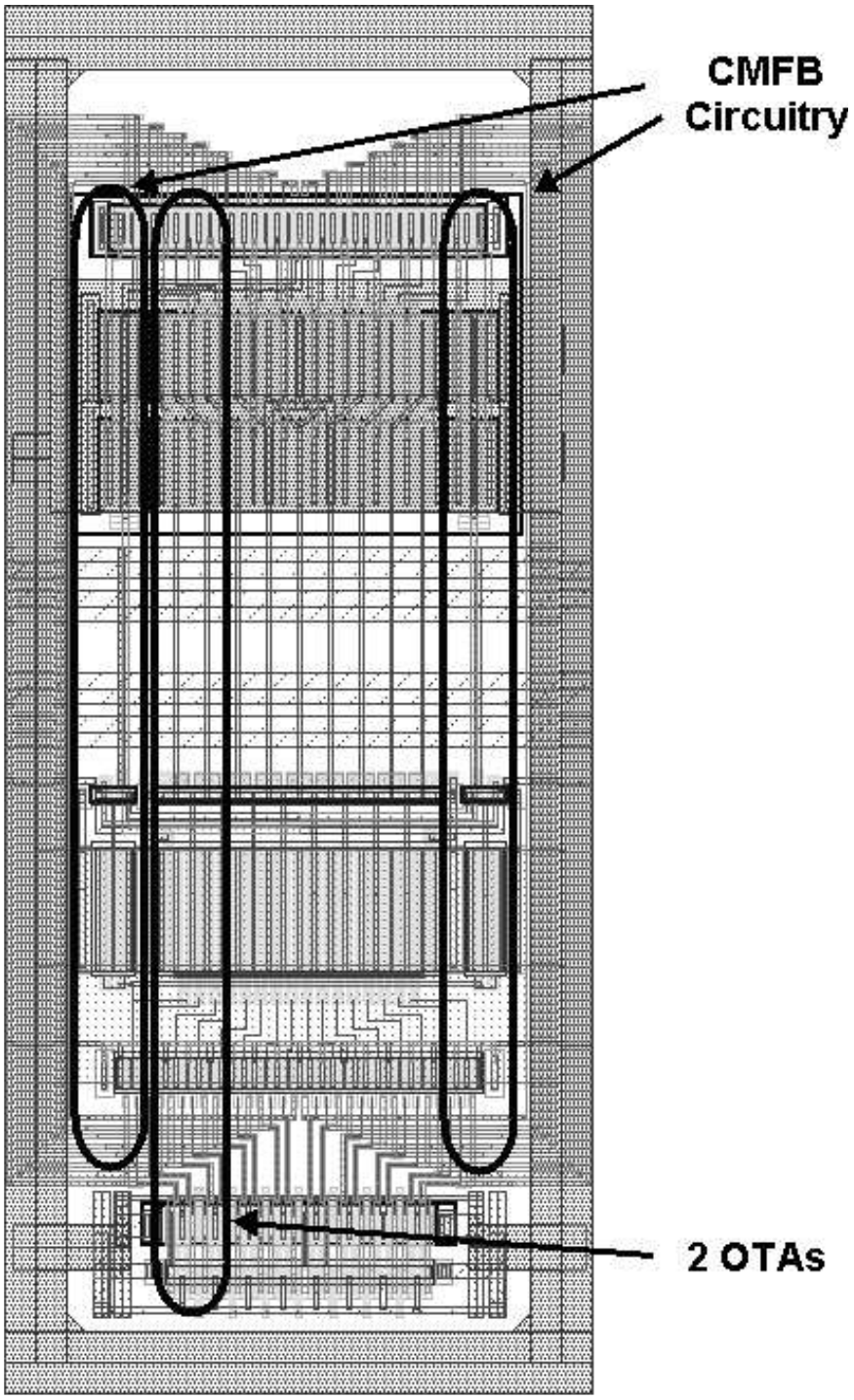



Fig. 50. Building block layout for OTAs in the bandpass filter. The orientation of the OTAs and CMFB circuitry are labeled.

## 2. Layout of Each OTA Using the Building Block Cell

Now that the building block cell has been developed, it can be used in the layout of each OTA in the bandpass filter. A schematic of the filter is displayed in Fig. 51. There are three primary signals in the filter. $V_{in}$ is the filter's input, $V_{BP}$ is the bandpass node of the filter, and $V_{LP}$ is the lowpass node. In the physical design, the OTAs are distinguished by which of these nodes their inputs and outputs connect to. Referring back to Figs. 49 and 50, the inputs to the building block cell are the gates of transistor M2. These are routed in metal layer 1 vertically across the signal routings. The outputs are at the drains of M2 and M3, and are routed in metal layer 3, also vertically across the signals. Now it becomes very easy to make the connections based on the OTA. To connect from a signal line to an OTA input, a Metal 1 to Metal 2 Via is dropped where the gate routing and the signal routing cross. Alternatively, to connect the signal line to an OTA output, a Metal 2 to Metal 3 Via is placed where the signal routing crosses the drain routing. The following pages provide illustrations of each OTAs layout, labeled with descriptions of the connections made. Figures 52, 53, 54, and 55 are respectfully the layouts of OTAs $g_{m1}$, $g_{m2}$, $g_{m3}$, and $g_{m4}$ from Fig. 51.

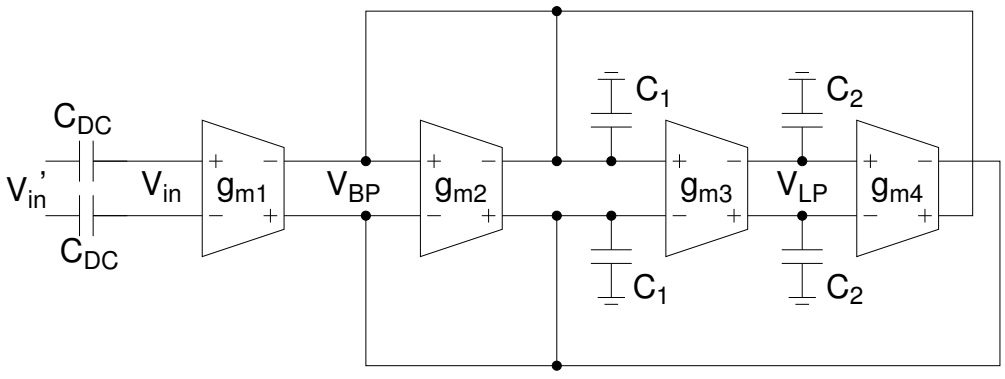



Fig. 51. OTA-C biquadratic filter schematic.

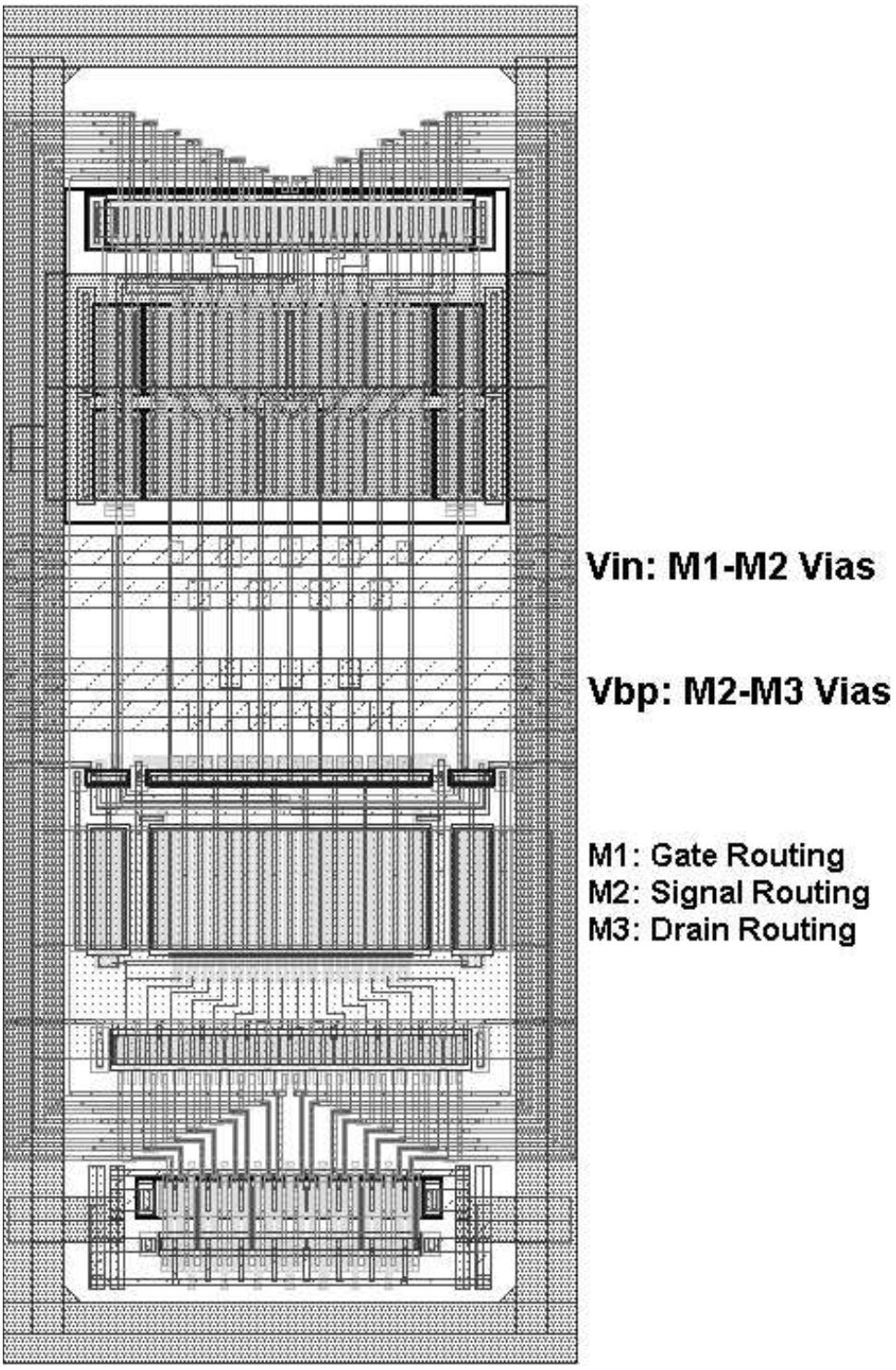



Fig. 52. Layout of the OTA $g_{m1}$ from Fig. 51.

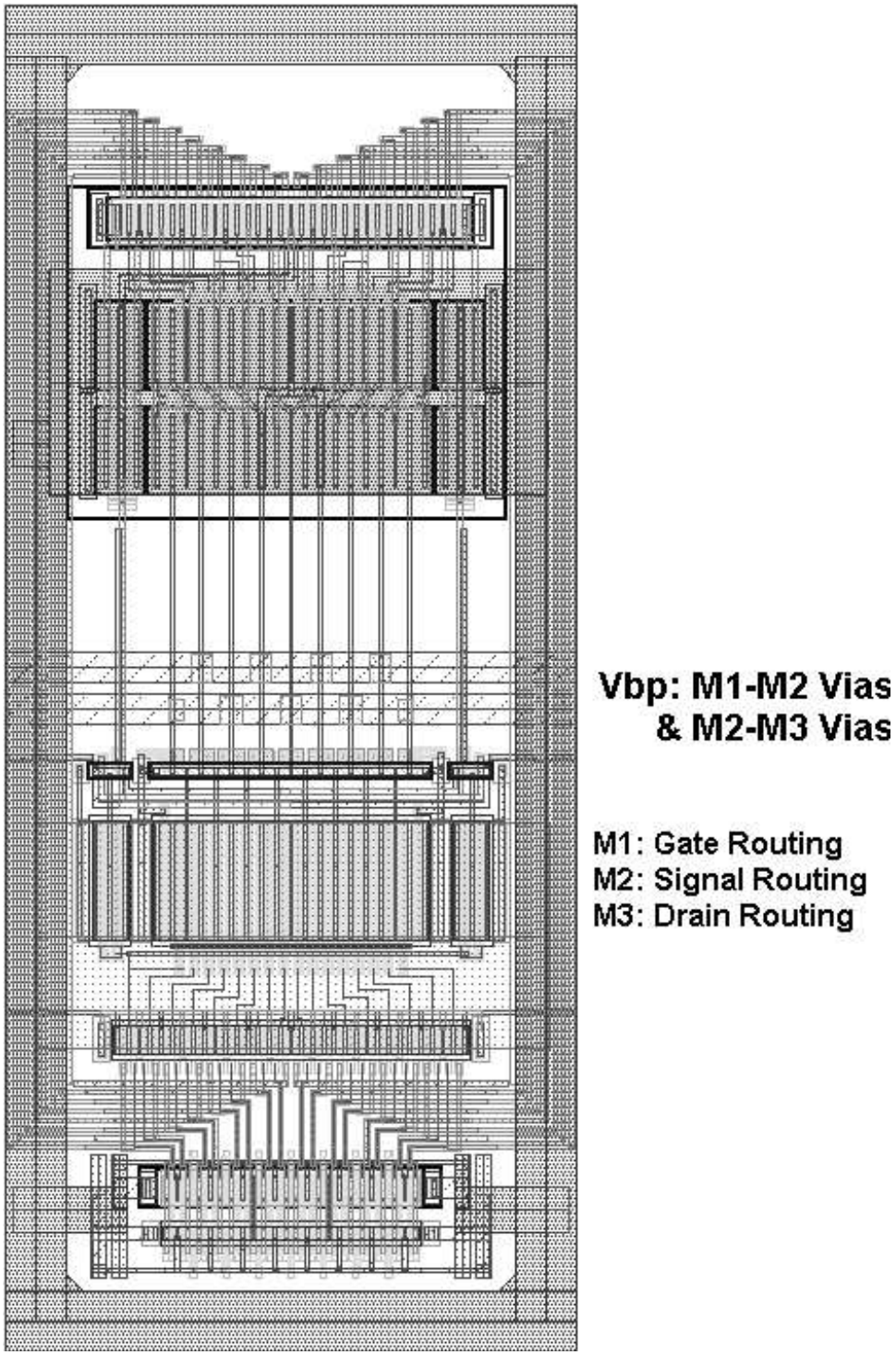



Fig. 53. Layout of the OTA $g_{m2}$ from Fig. 51.

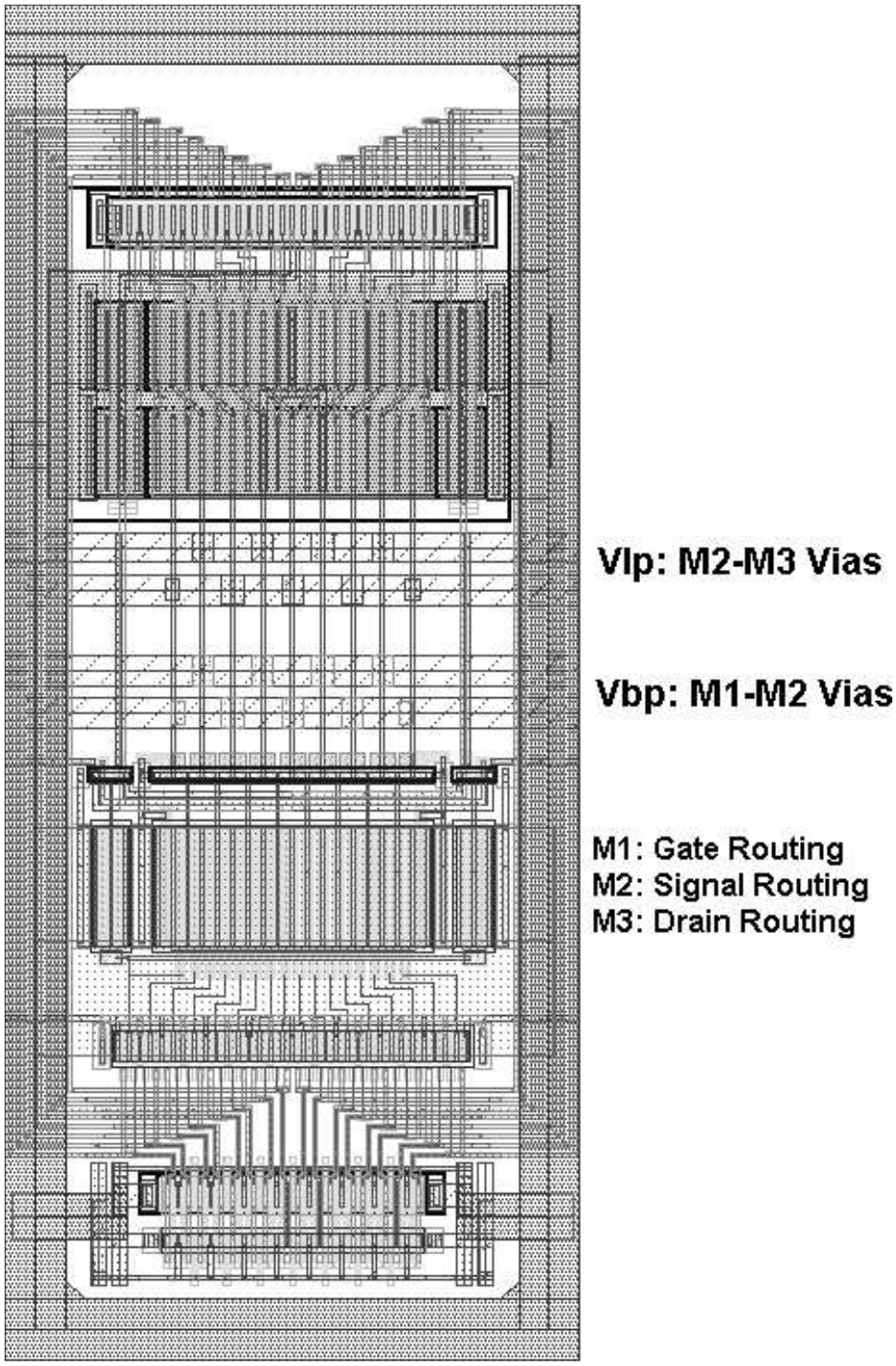



Fig. 54. Layout of the OTA $g_{m3}$ from Fig. 51.

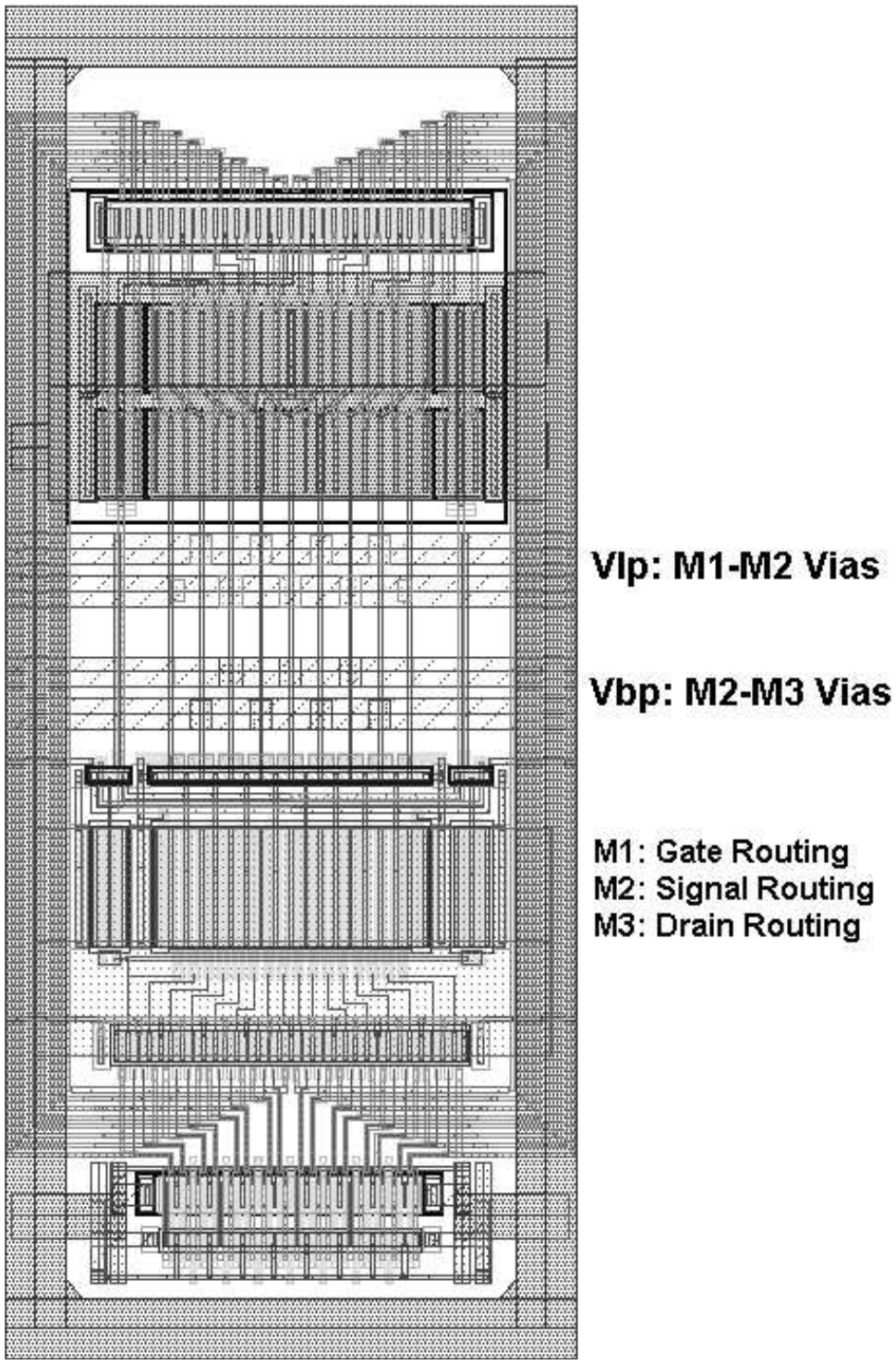



Fig. 55. Layout of the OTA $g_{m4}$ from Fig. 51.

### 3. Layout of the Bandpass Filter's Resonator

OTAs $g_{m3}$ and $g_{m4}$ from Fig. 51 form the resonator of the bandpass filter. These are also the cells that require the large, 8-bit thermometer coded bank of OTAs. In this section, the hierarchy of the resonator's layout is described.

The resonator is built in a binary fashion, with each level of the hierarchy instantiating two of the cells that are one level lower. The lowest level resonator is built by placing one of the $g_{m3}$ building block cell from Fig. 54 directly next to a $g_{m4}$ building block cell from Fig. 55. The resulting layout is displayed in Fig. 56. Each of these cells contain 16 levels of the thermometer encoding. The next level of hierarchy is displayed in Fig. 57. At this level, the digital controls are routed along the bottom of the layout. At one level higher, Fig. 58, some separation is added in between the placement to give space for routing at the top level. At this point 64 levels of thermometer encoding are accounted for. In Fig. 59, the layout begins to grow vertically. Finally, Fig. 60 displays the completed layout of the resonator, which includes all 256 levels of thermometer encoding.

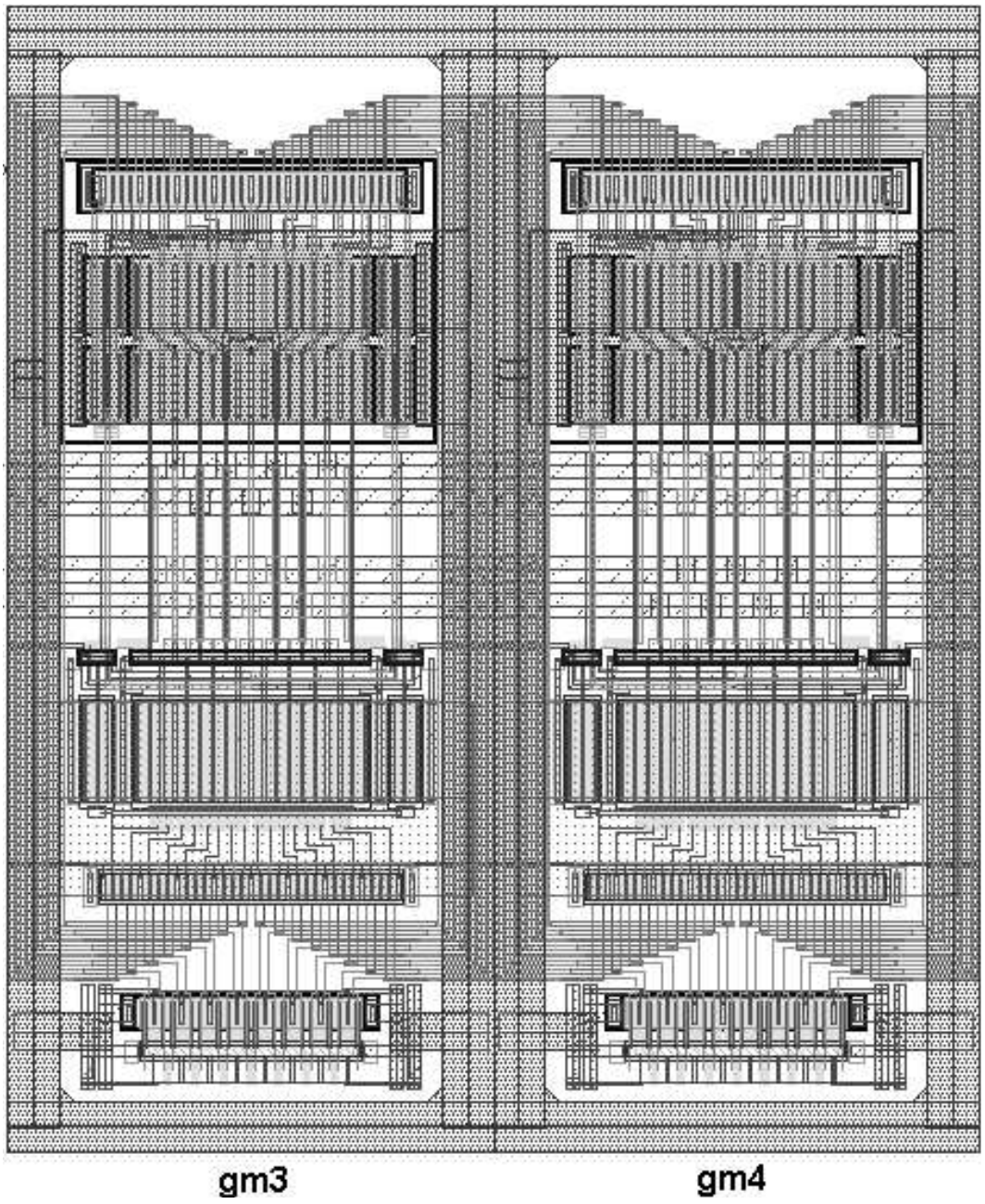



Fig. 56. First level of hierarchy in the layout of the resonator. Each of these contributes 16 levels of the thermometer coding.

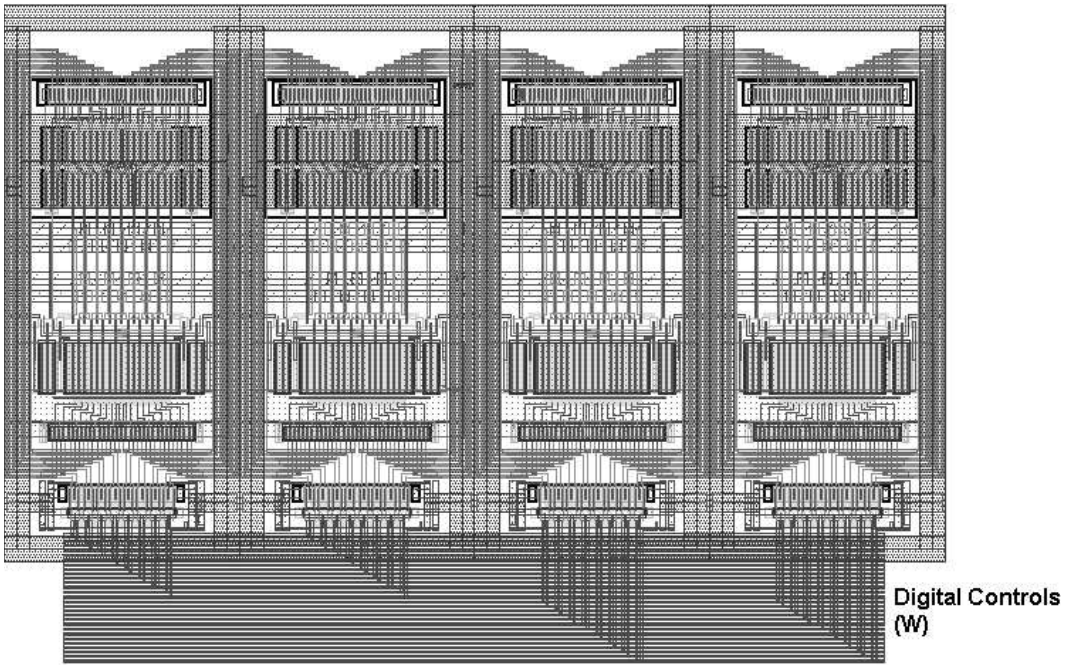



Fig. 57. Second level of hierarchy in the layout of the resonator. Each of these contributes 32 levels of the thermometer coding.

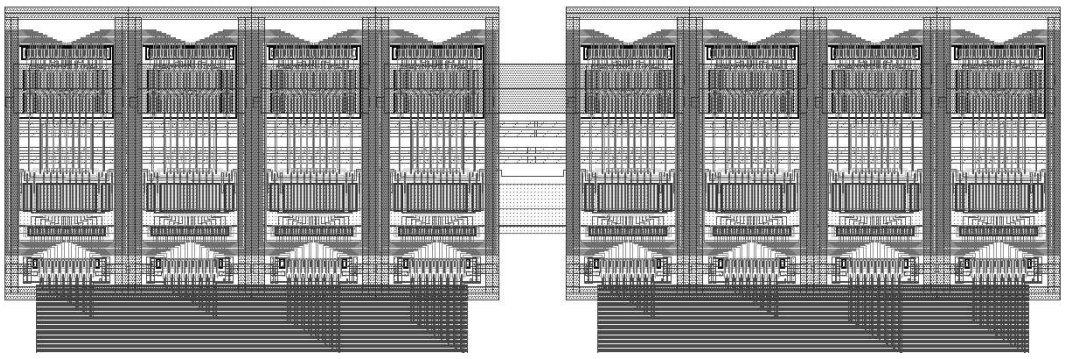


Fig. 58. Third level of hierarchy in the layout of the resonator. Each of these contributes 64 levels of the thermometer coding.

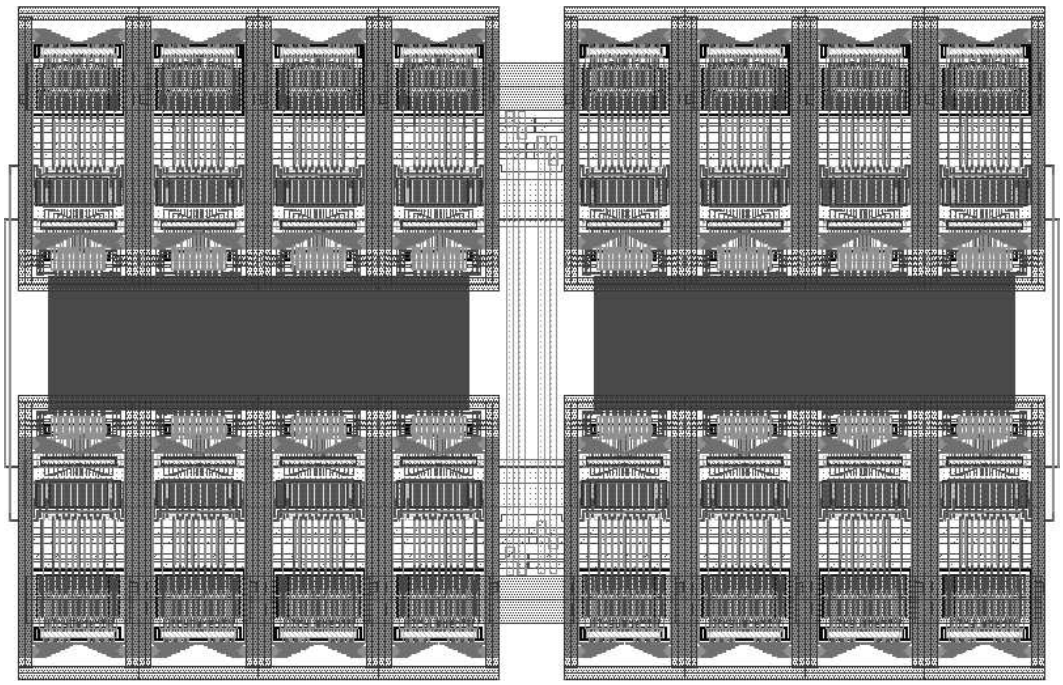


Fig. 59. Fourth level of hierarchy in the layout of the resonator. Each of these contributes 128 levels of the thermometer coding.

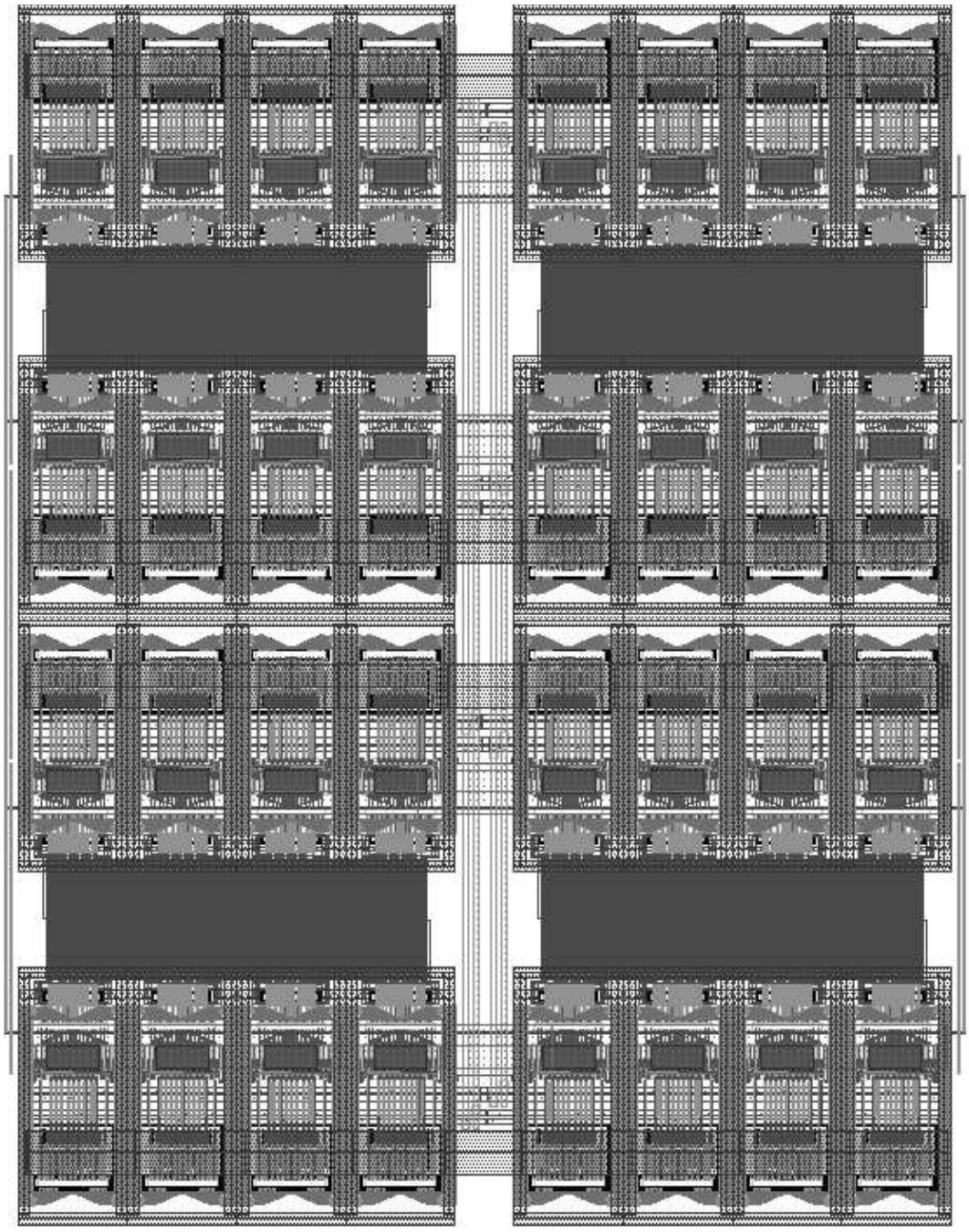


Fig. 60. Highest level of hierarchy in the layout of the resonator. This cell contains all 256 levels of the thermometer coding.

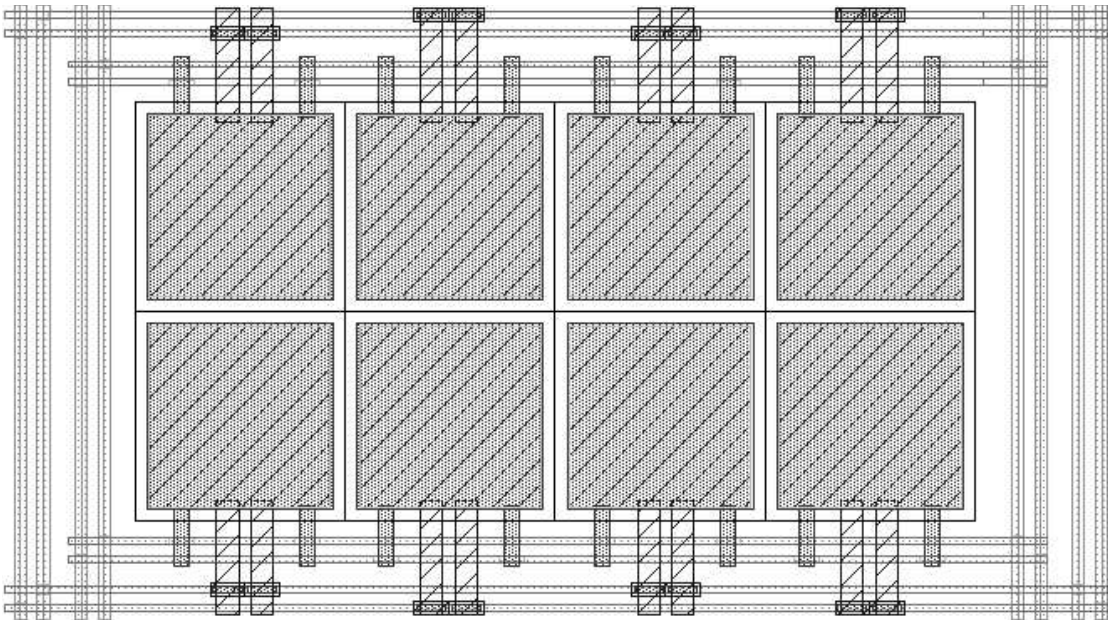


Fig. 61. Layout of the decoupling capacitors used at the filter's input.

### 4. Layout of the Bandpass Filter's Capacitors

Three different capacitor pairs were used in the design of the filter. First, metal-insulator-metal (MIM) caps were used as decoupling capacitors between the actual input and the filter input. The MIM capacitor uses metal layer 6 as the top plate, and metal layer 5 as the bottom plate. The 4 pF decoupling capacitors are labeled as $C_{DC}$ in Fig. 51. Their layout is displayed in Fig. 61. To improve matching, they are inter-digitized using the common centroid method.

The second and third capacitor pairs were the integrating capacitors used in the resonators. These are $C_1$ and $C_2$ from Fig. 51, and were built using a 4-bit bank of MIM capacitors with unit capacitance 100 fF. The layout of the unit capacitor is displayed in Fig. 62, and the layout of the full bank of capacitors is shown in Fig. 63.

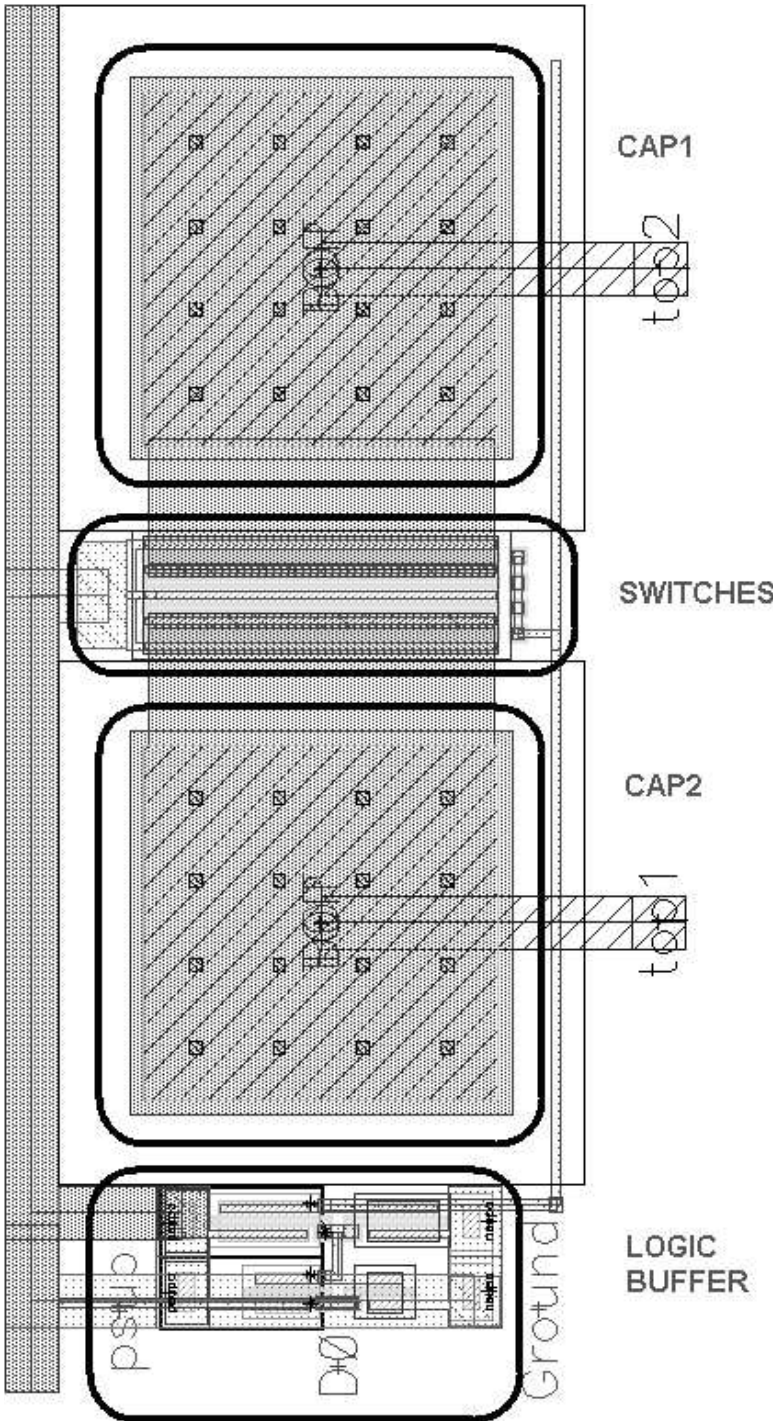



Fig. 62. Layout of the unit capacitor used in the integrating capacitor banks.

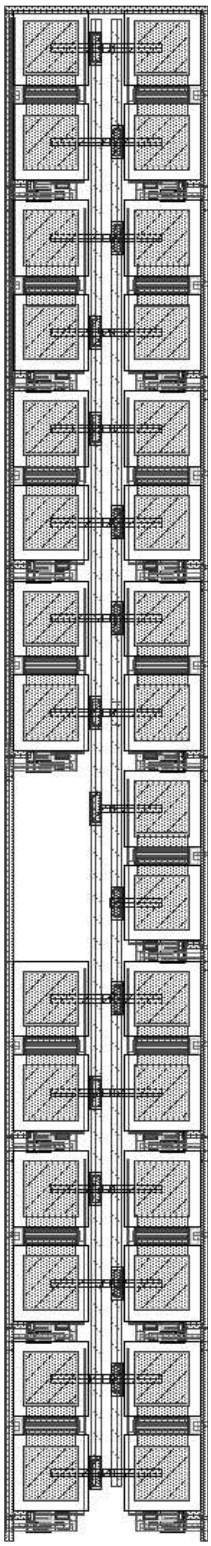


Fig. 63. Layout of the 4-bit integrating capacitor bank.

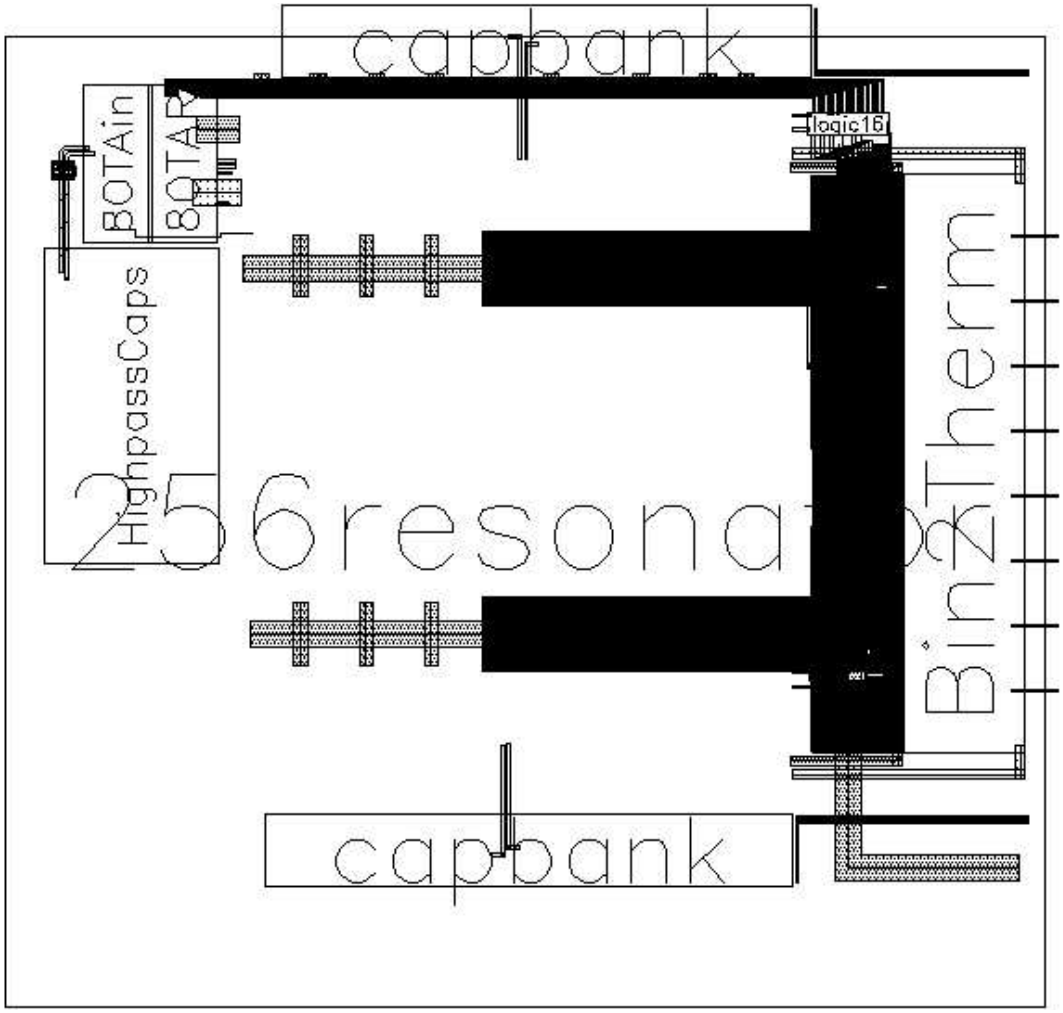



Fig. 64. Layout floorplan of the bandpass filter.

## 5. Bandpass Filter Top Level Layout

The final layout of the bandpass filter had a total area of $0.3mm^2$, measuring $570\mu$m by $520\mu$m. The floorplan of the layout is provided in Fig. 64. The top level layout showing all of the drawn layers is displayed in Fig. 65.

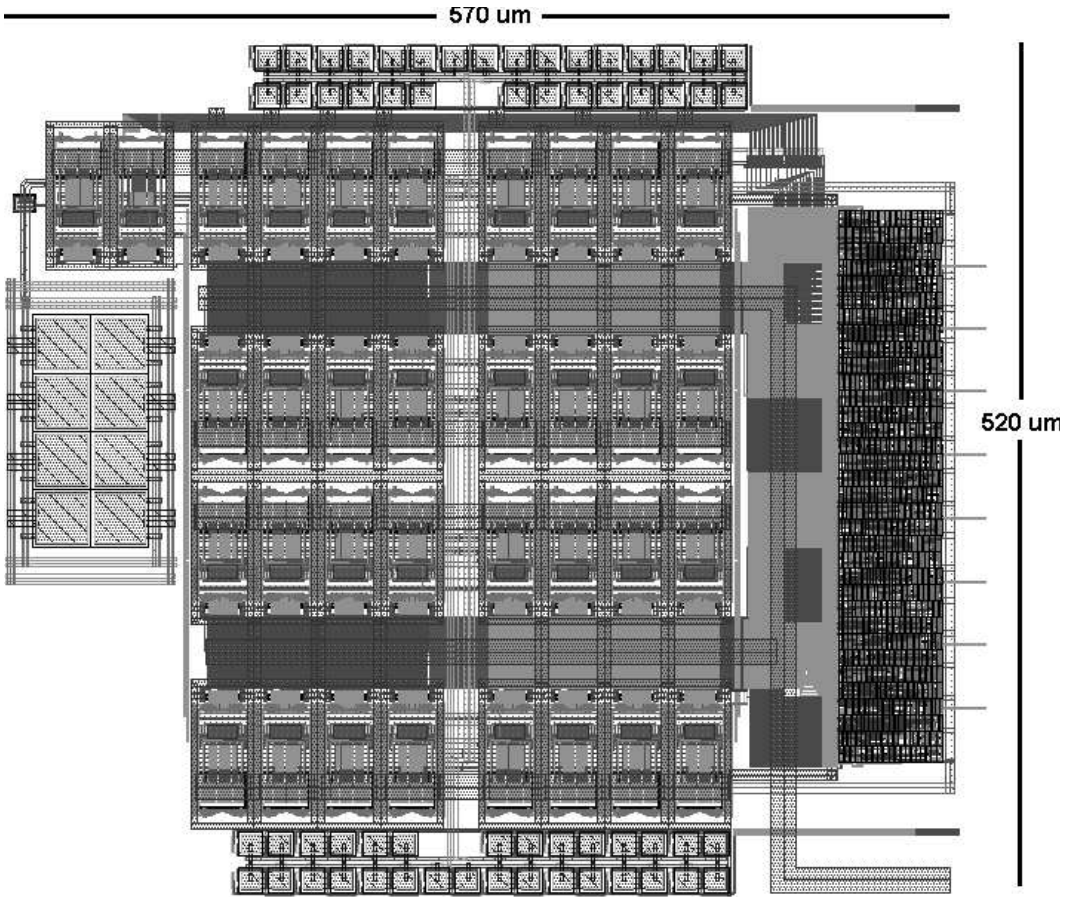



Fig. 65. Top level layout of the bandpass filter.

# CHAPTER VII

## EXPERIMENTAL RESULTS

The complete notch filter including center frequency adjustability and LMS tuning for maximum attenuation was fabricated in TSMC's 0.18 $\mu$m technology. A micrograph of the filter is displayed in Fig. 66. The shown micrograph consists of three notch filters, each having area 750 $\mu$m $\times$ 500 $\mu$m $= 0.375$ mm$^2$. This chapter describes the test setup and experimental measurements obtained from the notch filter.

### A. Test Setup

Two experimental setups were used in testing the notch filter. For time domain measurements, an arbitrary waveform generator (AWG) was used to supply the input to the filter, and an oscilloscope was used to observe the output, as displayed in Fig. 67. Alternatively, as shown in Fig. 68, a spectrum analyzer was used for taking frequency domain measurements. Many aspects of the test setup were common to both configurations. A 1.8V regulator was used as the analog supply, with a connecting potentiometer used as a current reference. National Instruments' LabView was used to serially apply the digital inputs to the filter. The output signals were buffered using operational amplifiers with 50$\Omega$ output resistance for the impedance matching requirements of the spectrum analyzer. Finally, single ended to differential conversion was performed at the input, and differential to single ended conversion was done at the output using baluns.

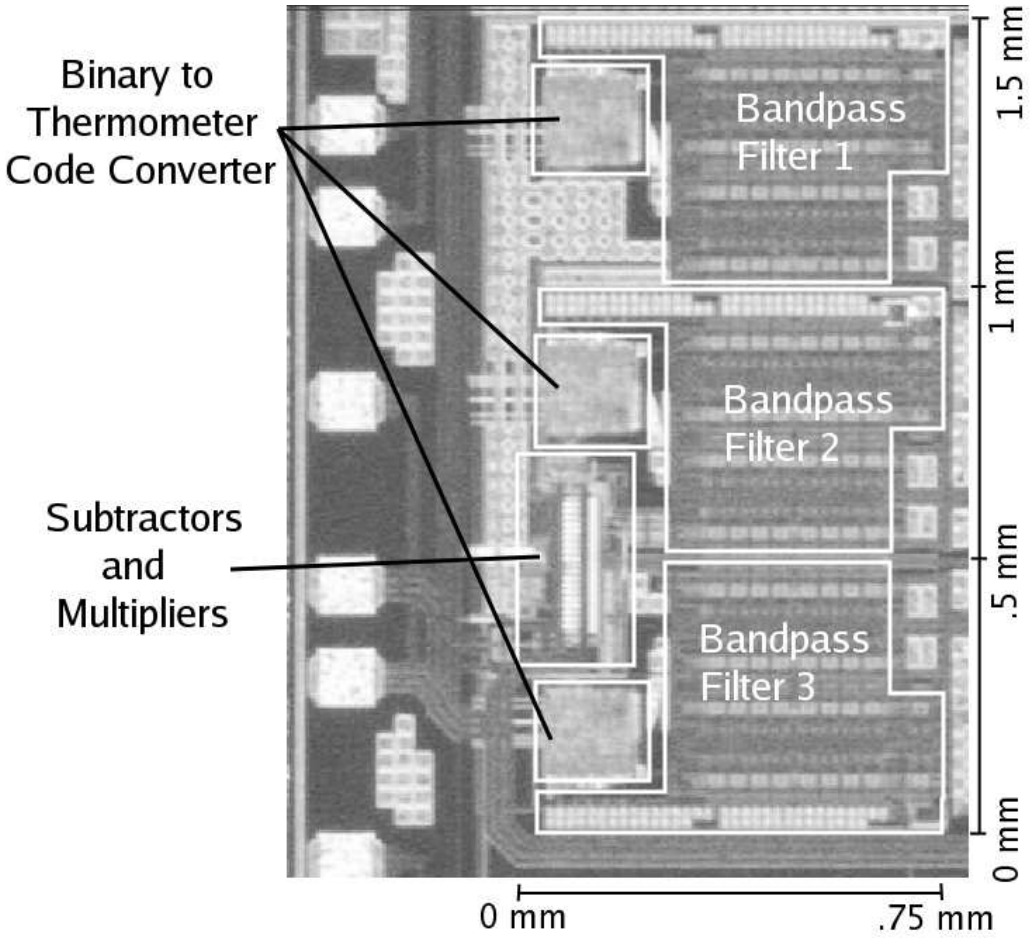



Fig. 66. A micrograph of three notch filter with LMS tuning and digital binary to thermometer code converter.

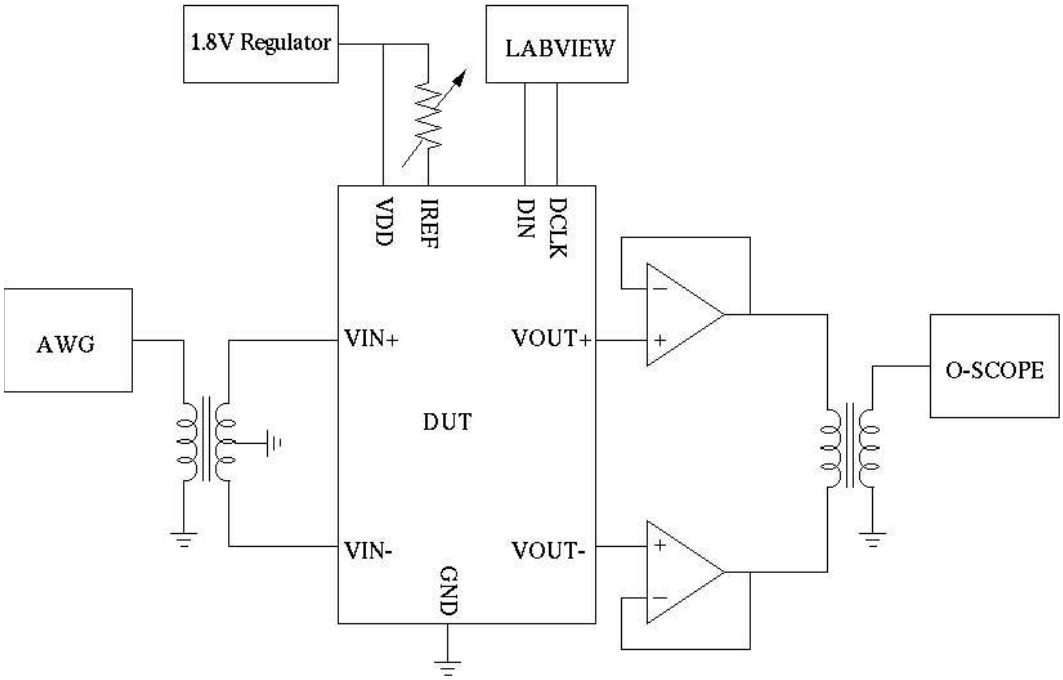



Fig. 67. Test setup for time domain measurements.

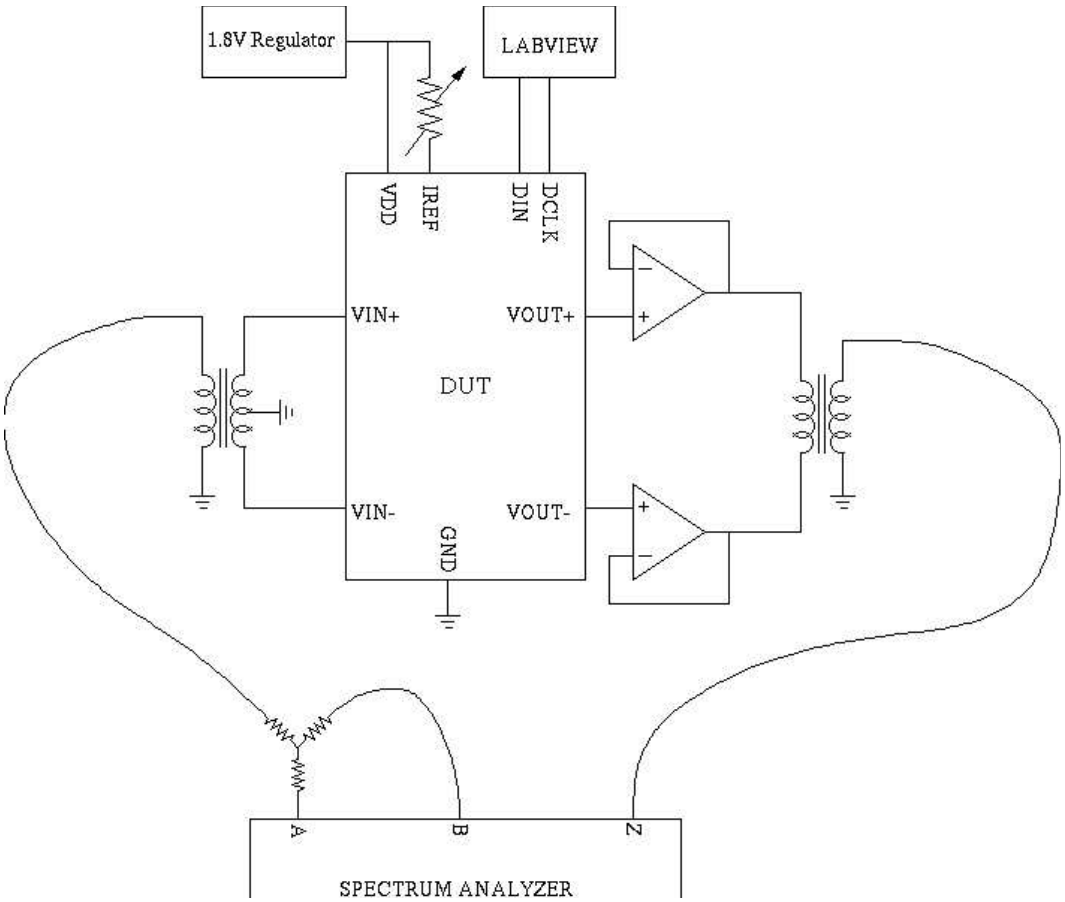



Fig. 68. Test setup for frequency domain measurements.

## B. Results

### 1. Frequency Domain Measurements

Fig. 69 displays the filter's characteristics versus the digital frequency control word, $W_{f0}$. The center frequency varied linearly with $W_{f0}$ from 1.63 MHz to 278.6 MHz. The worst case attenuation was 25 dB, and the best case was nearly 50 dB. The bandwidth was relatively constant, varying from 22 MHz to 27 MHz. The power consumption depends on the center frequency setting of the filter, and was measured to be $P_{diss} = 3.6 + 0.035\ W_{f0}$ mW. At most, the power consumption was 12.5 mW. Figure 70 displays the magnitude response of the notch filter for three adjacent low frequency $W_{f0}$ settings. Figure 71 displays the magnitude response of the notch filter for the three adjacent high frequency $W_{f0}$ settings. In both cases the frequency notches overlap below $-20$ dB, thus it is possible to attenuate any frequency within this continuous band by at least 20 dB.

### 2. Time Domain Measurements

MB-OFDM is a frequency hopping system, and thus RF interference only appears in the baseband periodically. If the notch filter is left on during all symbol periods, settling will occur in the symbol adjacent to that which has the interference. Figure 73 displays the filter's input, and the resulting settling behavior at the filter's output when the filter is left on during all symbols and is subject to a practical interference situation. By turning off the feedforward path of the notch filter, this residual settling can be avoided. Recall that the feedforward path can be turned off with the digital control $W_{on}$ from Fig. 23. To emulate the case where an interference appears periodically due to the frequency hopping nature of MB-OFDM, the signal in Fig. 72 was applied to the input of the filter. The measured settling behavior when the filter

Table VI. Measured performance of the notch filter

| **Measurement** | **Min** | **Max** |
|---|---|---|
| $\omega_{f0}$ | $2\pi$ 1.63 Mrad/s | $2\pi$ 278.6 Mrad/s |
| $\omega_{bw}$ | $2\pi$ 21.7 Mrad/s | $2\pi$ 27.1 Mrad/s |
| $\alpha_0$ | 25 dB | 49 dB |
| Power Cons. | 3.6 mW | 12.5 mW |
| Output Noise | 65.1 $nV^2$ | 69.7 $nV^2$ |

is turned on only during the symbol that contains interference is provided in Fig. 74. As expected, there is no settling seen in the adjacent symbol. A summary of the experimental results is provided in Table VI. The power required by the DSP for tuning the center frequency is not included in the indicated power consumption. The dominant use of the DSP's power consumption comes from the FFT processor, which is already used for decoding the UWB data and should not be included in the cost of the analog filter. Thus, the additional power required for filter consists only of the few DSP operations that interpret the FFT output for tuning, which should be relatively small. The worst case power of the filter was 12.5 mW, which is relatively small compared to the total system power that includes the LNA, mixer, and DSP.

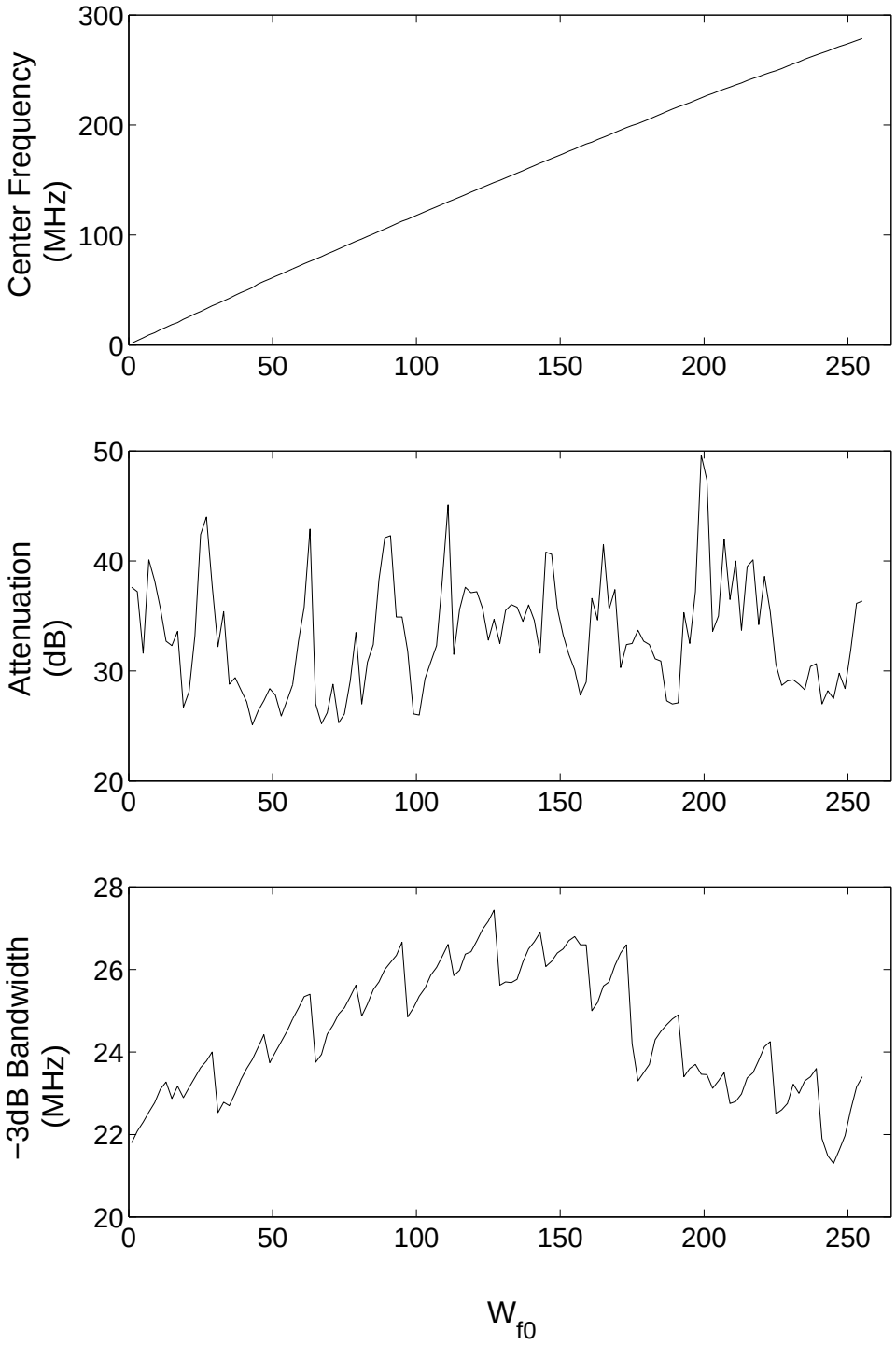



Fig. 69. Measured filter characteristics versus the frequency control word, $W_{f0}$.

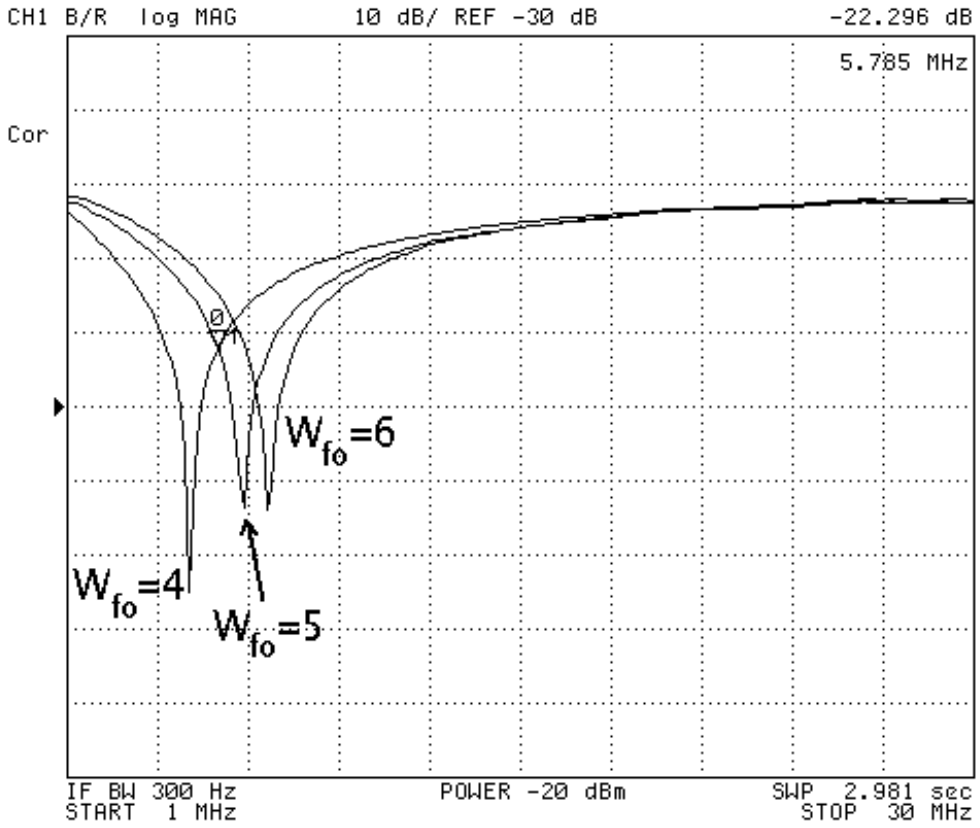



Fig. 70. Measured magnitude response for three adjacent low frequency $W_{f0}$ settings of the notch filter.

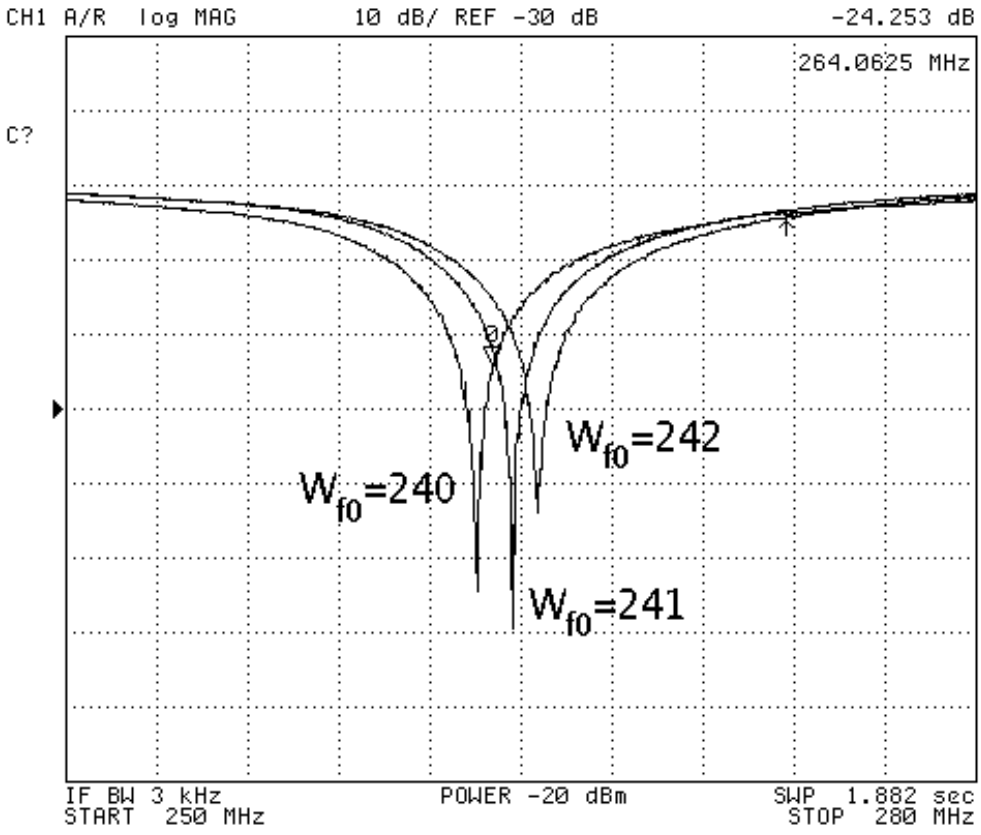



Fig. 71. Measured magnitude response for three adjacent high frequency $W_{f0}$ settings of the notch filter.

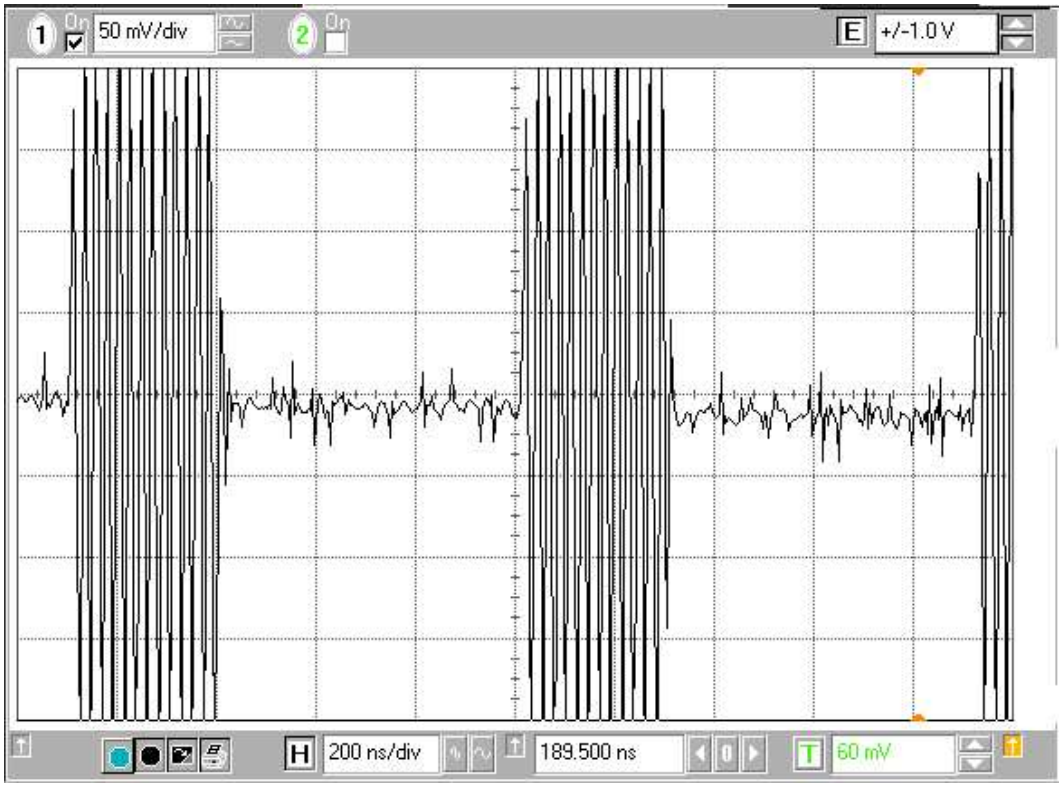



Fig. 72. Periodic interference input, $V_i$, applied to the filter.

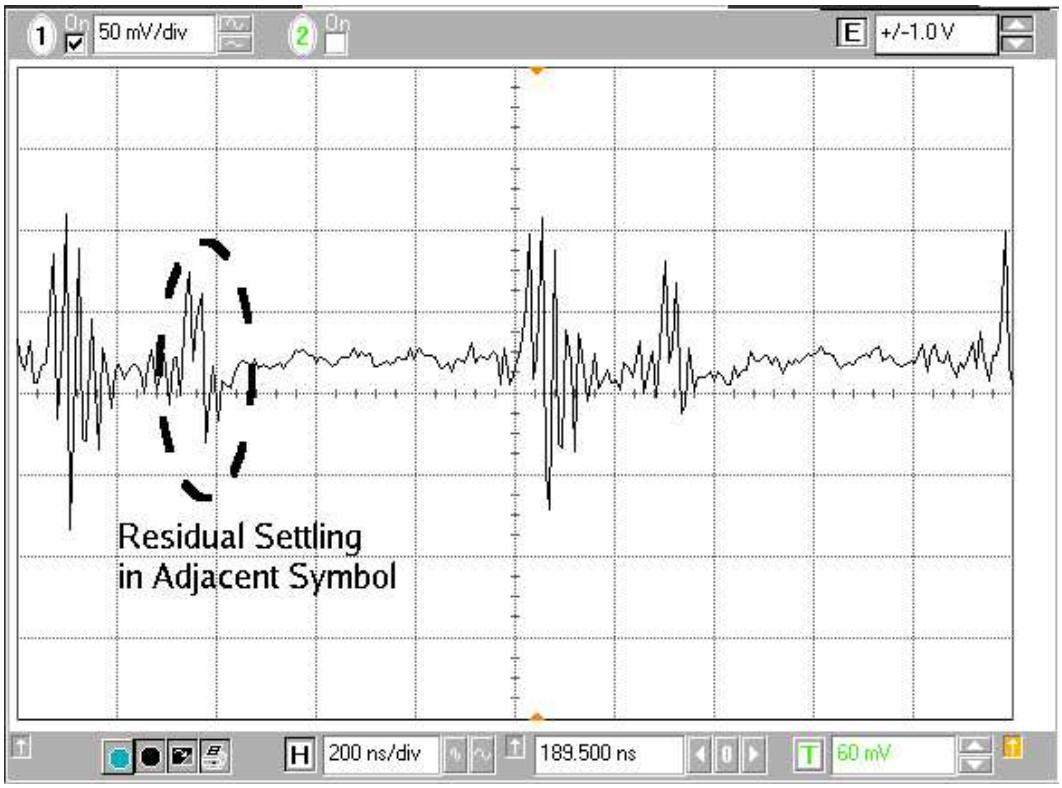



Fig. 73. Settling behavior of the notch filter's output, $V_o$, for the periodic interference input, $V_i$ of Fig. 72. In this case, the notch filter is left on during all symbols. Residual settling is seen in the symbol period adjacent to the interference symbol.

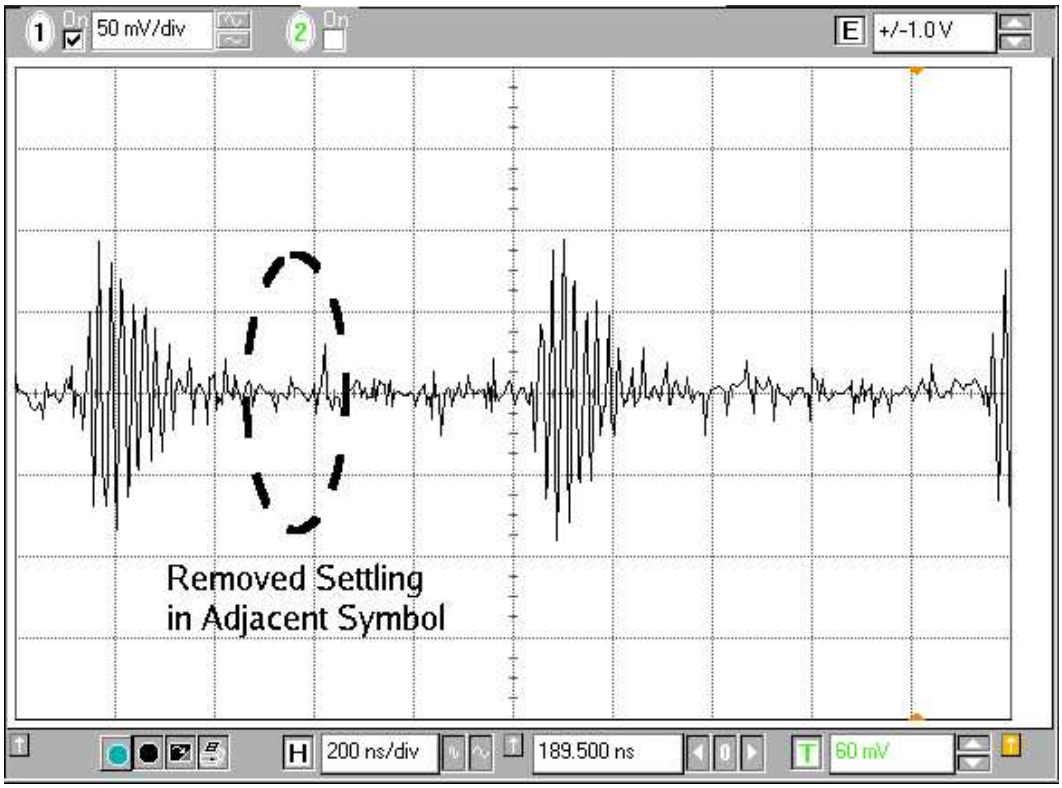



Fig. 74. Settling behavior of the notch filter's output, $V_o$, for a periodic interference input, $V_i$ of Fig. 72. In this case, the notch filter is turned off during the symbol periods that do not contain the interference. No residual settling is observed in the adjacent symbol.

# CHAPTER VIII

## A RAIL-TO-RAIL AMPLIFIER INPUT STAGE WITH ±0.35% $\mathbf{G_M}$ FLUCTUATION

The OTA was used as a building block cell in many aspects of the UWB notch filter design. In many cases it is useful for an OTA to be capable of accepting inputs with common mode levels at or near the supply levels. This chapter describes a novel technique for achieving this capability.

### A. Background

For an operational amplifier connected in the unity gain configuration, the operating signal swing is limited by the common mode range of the input stage and the allowable output signal range. To allow maximum signal amplitudes, these two ranges should extend from the positive supply to the negative supply levels (rail-to-rail operation). A simple class-AB amplifier can be used as the output stage to an amplifier, allowing rail-to-rail output signal swing [23]. The focus of this chapter is thus on extending the common mode range of the input stage.

Due to threshold voltage limitations, a traditional differential pair is not capable of processing signals with rail-to-rail common mode levels. An N-channel (P-channel) differential pair cannot process signals with low (high) common modes. An initial solution would be to combine N-channel and P-channel differential pairs in parallel. However, fluctuations in the total transconductance of the input stage, as illustrated in Fig. 75, could possibly create stability problems. This is because during the overlapping region of operation, the total transconductance doubles in magnitude. It is necessary then to maintain constant transconductance throughout all common mode input levels.

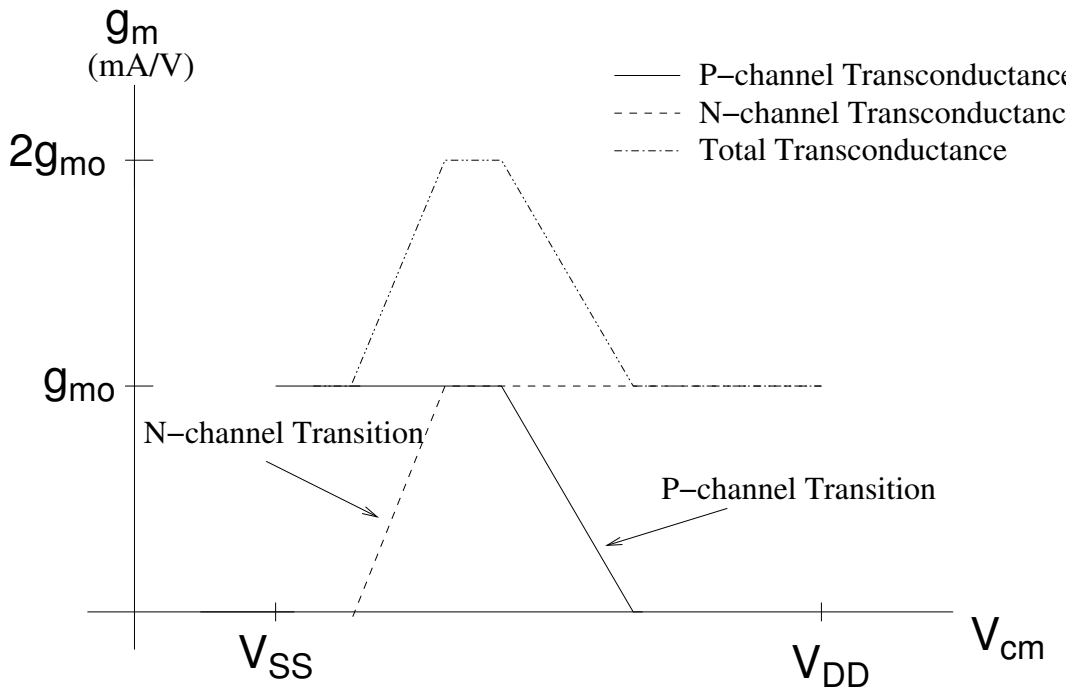



Fig. 75. Problem of non-constant transconductance introduced by parallel N-channel and P-channel differential pairs.

Many techniques for achieving constant transconductance ($g_m$) in rail-to-rail amplifiers have been introduced [24]– [25]. Most make use of parallel N-channel and P-channel differential pairs combined with complex circuitry to ensure that the sum of the $g_m$s of the two input pairs remains constant, as illustrated in Fig. 76. Based on information gathered in the current summation stage, some operation is made on the magnitude of the differential pair tail currents. In [26], the idea of shifting the input signals, and in effect the common mode range of the differential pairs, was introduced. The signals were shifted in a way that overlapped the transition regions of the two differential pairs, resulting in a constant overall transconductance, as illustrated in Fig. 77. Architectures such as these suffer from two primary drawbacks. First, in order to obtain constant total transconductance, the $g_m$ of the N-channel differential pair must precisely match that of the P-channel pair, which is difficult to realize

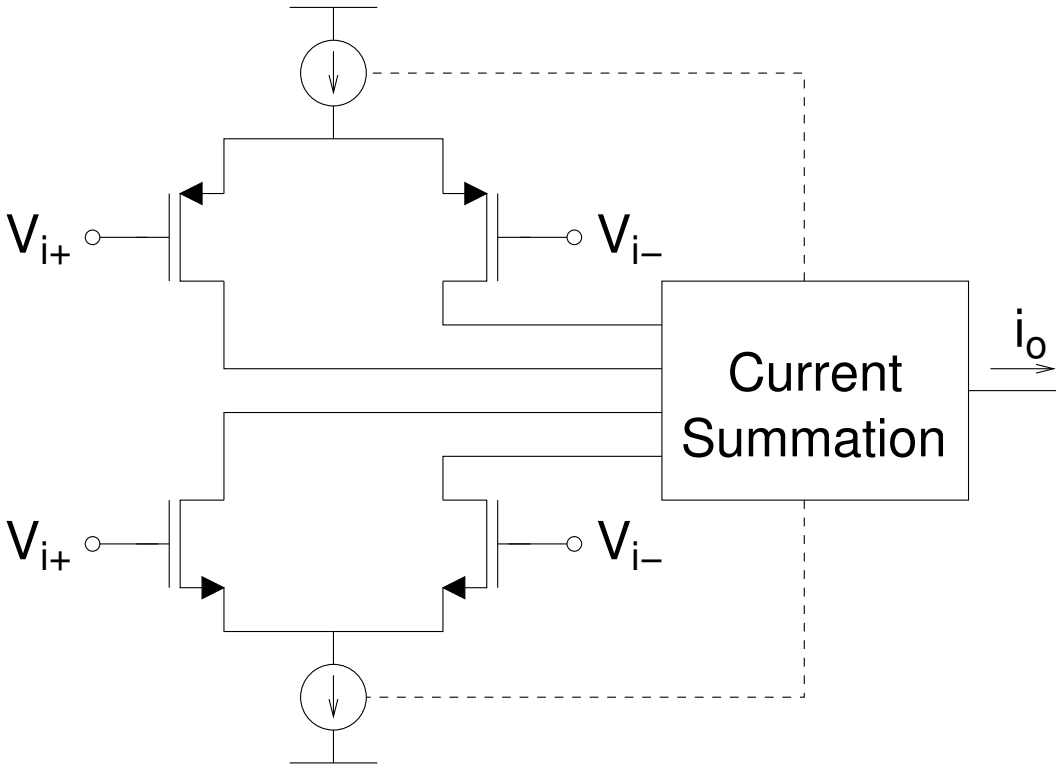



Fig. 76. Typical rail-to-rail input stage architecture.

given process variations. Reported architectures provide a total $g_m$ fluctuation from $\pm 1.5\%$ [27] to $\pm 10\%$. Second, the common mode rejection ratio (CMRR) of these circuits is usually degraded when the common mode level of the input lies within the transition region of the input stage, where both the N-channel and P-channel differential pairs are operating [28]. This degradation is typically between 40–60 dB. To overcome these problems, a technique that uses parallel same channel differential pairs was introduced [25]. This technique is similar to [26] in that it shifts the common mode range of one of the differential pairs. The primary difference is that rather than overlapping transition regions to obtain constant transconductance, the authors use feed-forward cancellation to maintain constant $g_m$ when both of the input pairs are operating. Since only one type of differential pair is used, the matching of the

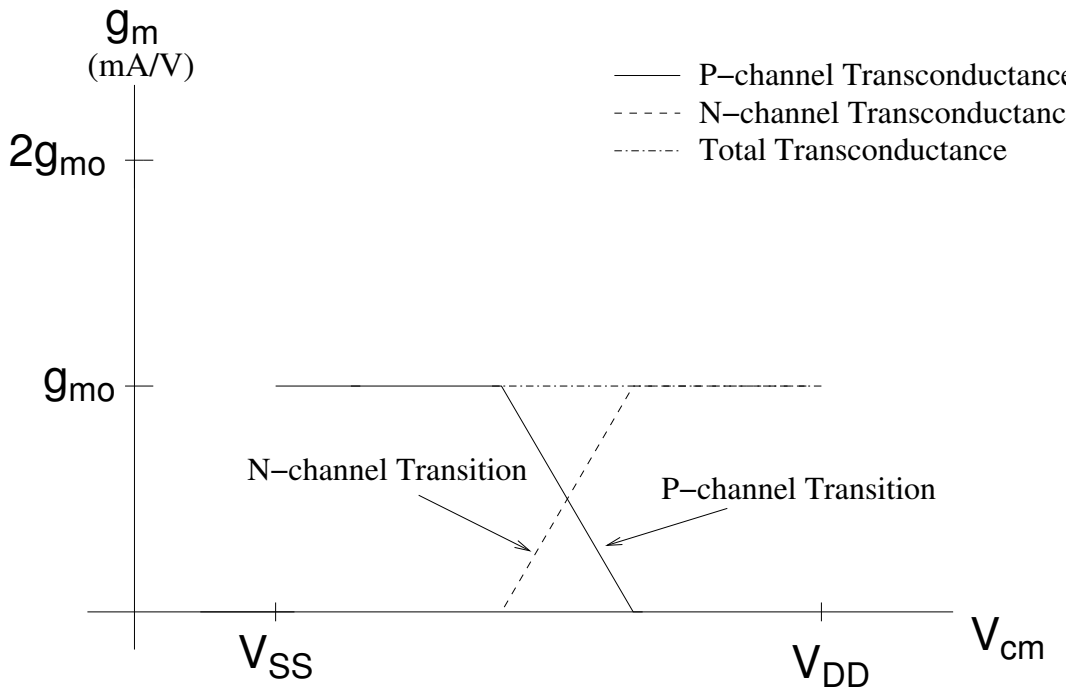



Fig. 77. Obtaining constant transconductance by shifting the common mode range of the input pairs to overlap transition regions.

the two input transconductors is much less sensitive to process variations. Still, the overall fluctuation in transconductance of this circuit was nearly $\pm 5\%$. Also, including the feed-forward transconductor, three differential pairs are used, as well as some additional biasing circuitry, which increases the power consumption of the amplifier.

For simplicity and accuracy, it is best to use a single differential pair at the input. In this case, the common mode range of the input pair must somehow be extended to accept rail-to-rail signals. In the past, this has been done using multiple input floating gate transistors (MIFG). The signal is attenuated using capacitive voltage division before it is processed by the amplifier [23, 29]. The ratio of the MIFG's capacitors is set so the input signal is attenuated enough to always reside within the common mode range of the actual differential pair. To ensure the signal is sufficiently attenuated, the capacitor ratio in these architectures is usually set to around five,

resulting in an attenuation of six [29]. This adversely affects the GBW as well as the noise response of the amplifier. Furthermore, even these architectures that use a single input differential pair exhibit some variance in the $g_m$ due to lambda effect on the tail current. As the common mode rises or falls, so does $V_{DS}$ of the transistor supplying the tail current, and accordingly, the current's magnitude. Circuit simulations result in almost 3% deviation in $g_m$ across rail-to-rail common mode inputs of a circuit implemented in this way.

In this chapter, a new input stage for rail-to-rail operation is introduced, which makes use of a single input differential pair. MIFG transistors are used, but feedback circuitry allows for a much lower attenuation than those previously reported. Rail-to-rail operation is achieved by shifting the input common mode level to a fixed DC level before the signal is input to the differential pair. It is assumed that any time constants introduced by gate leakage via tunneling effects are sufficiently large, and are thus neglected in this analysis.

## B. Programmable Level Shifters

Near zero variance in $g_m$ can be achieved by shifting the common mode component of the input signal to a fixed level that resides within the common mode range of the input differential pair. Since the amount of shift required is dependent on the common mode level of the input, programmable level shifting circuitry is needed. A simple, highly programmable level shifter (PLS) can be created with a MIFG transistor in a source follower configuration, as displayed in Fig. 78. One terminal to the MIFG transistor, $V_i$, serves as the input to the circuit. The other terminal, $V_{fb}$, determines the amount of shift by programming the effective threshold voltage of $M_1$ as seen from $V_i$. The amount of shift obtained from a transistor in the source follower configuration

is governed by the gate to source voltage:

$$V_{GS} = \sqrt{\frac{2I_D}{K_P W/L}} + V_T \tag{8.1}$$

For $C_i, C_{fb} \gg C_{gb1}, C_{gs1}, C_{gd1}$, the resulting gate voltage, $V_{g1}$ in Fig. 78, of the MIFG transistor with two inputs is:

$$V_{g1} = \frac{C_i V_i + C_{fb} V_{fb}}{C_i + C_{fb}} \tag{8.2}$$

Combining Eqs. (8.1) and (8.2), the amount of shift from the point of view of the input terminal is a recursive function of $V_i$, determined to be

$$V_{shift} = V_i - V_o = \sqrt{\frac{2I_D}{K_P W/L}} + V_T + \frac{C_{fb}}{C_i + C_{fb}}(V_i - V_{fb}) \tag{8.3}$$

Defining $V_{TE}$ as the effective threshold voltage as seen from $V_i$, the amount of shift from $V_i$ to $V_o$ is now:

$$V_{shift} = \sqrt{\frac{2I_D}{K_P W/L}} + V_{TE} \tag{8.4}$$

where

$$V_{TE} = V_T + \frac{C_{fb}}{C_i + C_{fb}} V_{diff} \tag{8.5}$$

and

$$V_{diff} = V_i - V_{fb} \tag{8.6}$$

Since $V_{shift}$ can be either a positive or negative value, $V_{TE}$ can also be programmed in either direction, with the amount of shift obtainable depending on the ratio of $C_{fb}$ to $C_i + C_{fb}$. Next we explore how to find a suitable value of $V_{fb}$ to shift the common mode level of differential signals to a constant value.

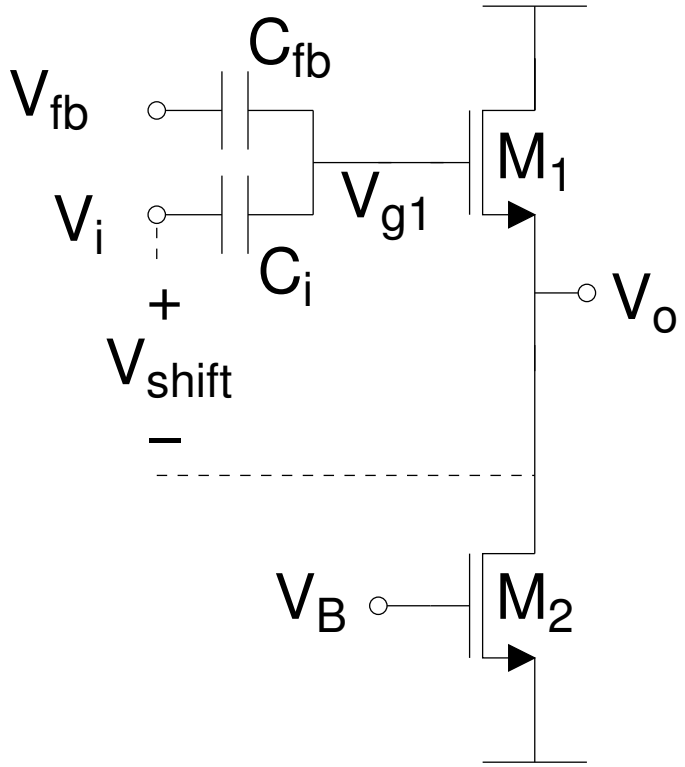



Fig. 78. Programmable Level Shifting (PLS) circuitry.

C. The Feedback Circuitry

Two programmable level shifters from the above section are now used as a pre-stage to a typical differential pair. The common mode level of the input signals is shifted to a constant value, yielding consistent operation independent of the common mode. In order to correctly program the level shifters, the common mode information must be extracted from the circuit, and fed back to the programming input, $V_{fb}$ of Fig. 78. This is done using the architecture displayed in Fig. 79. The source voltage of the differential pair, labeled in Fig. 79 as $V_{tail}$, behaves as an AC ground for differential inputs, and nearly as a buffer for common mode inputs. If this voltage remains constant, so will the magnitude of the tail current, resulting in near zero variation in $g_m$ of the differential pair. Any DC value that keeps the differential pair operating in the desired saturation region can be used as a reference. For convenience, the gate/drain voltage of $M_8$, $V_{ref}$, is used for comparing $V_{tail}$. This difference is magnified and returned to the PLSs as $V_{fb}$. The resulting feedback voltage becomes:

$$V_{fb} = A_f(V_{ref} - V_{tail}) \tag{8.7}$$

Due to the negative feedback, if the gain of the amplifier is large enough, $V_{tail}$ is forced to be approximately equal to $V_{ref}$, and a constant current is supplied to the differential pair regardless of the common mode. Also, since $V_{DS7}$ is equal to $V_{DS8}$, the magnitude of the tail current becomes precisely (neglecting device mismatch) equal to the reference current.

D. Design Considerations

Several considerations need to be made in the design of this amplifier. Two primary concerns in MIFG design are area and bandwidth. The addition of capacitors will

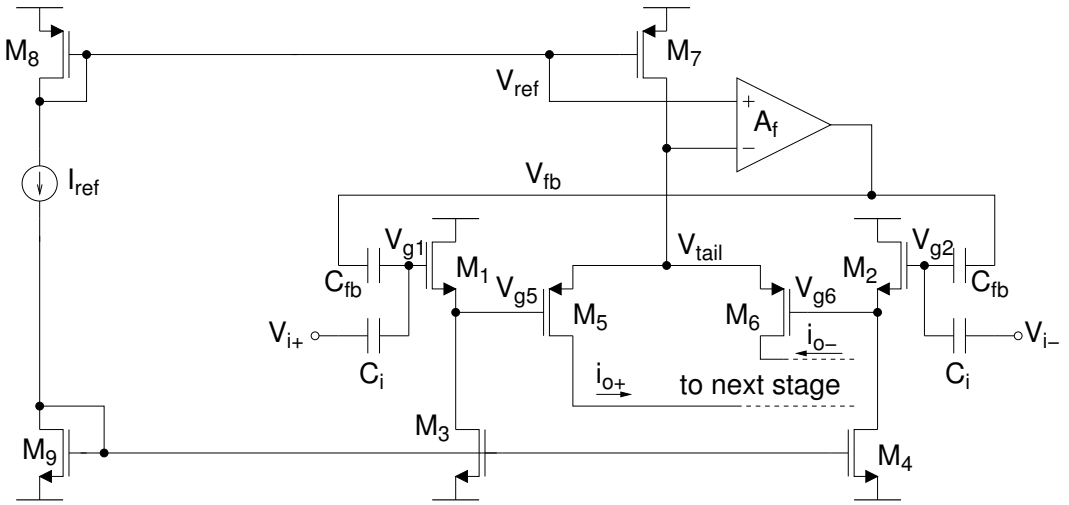



Fig. 79. Rail-to-rail input stage.

increase the area of the circuit compared to traditional amplifier design. Also, the attenuative effect of these capacitors reduces the effective transconductance of the input stage, degrading the GBW of the amplifier. One goal of this design should thus be to make these effects as small as possible. Proper biasing can help improve the circuit performance, and minimize the required area. Finally, a stability analysis of the feedback loop is performed to ensure proper operation of the circuit.

### 1. GBW and Biasing

Since this design first attenuates the input signal before it is processed by the amplifier, the gain bandwidth product will be reduced. It is thus desirable to make this reduction as small as possible. To achieve consistent rail-to-rail operation, the minimum attenuation can be obtained by setting $C_i = C_{fb}$ in Fig. 79. There are two necessary conditions for using this attenuation. First, the feedback amplifier, $A_f$, should have rail-to-rail output signal swing. Second, the condition $V_{fb} = -V_{cm}$ should be met, where $V_{cm}$ is the common mode level of the input. This implies that

the circuit should be designed such that when $V_{cm}$, is zero, $V_{tail}$ should equal $V_{ref}$.

The first requirement, that the feedback amplifier, $A_f$ has a rail-to-rail output swing, is easily met by using an OTA based on three current mirrors [30]. The second requirement, that $V_{fb} = -V_{cm}$ can be accomplished through careful design of the circuit in Fig. 79, using the following relationships.

$$C_i = C_{fb} \tag{8.8}$$

$$V_{tail} = \frac{V_{g5} + V_{g6}}{2} + \sqrt{\frac{I_{ref}}{K_{pp}(W/L)_{5,6}}} - V_{TP} \tag{8.9}$$

$$\frac{V_{g5} + V_{g6}}{2} = \frac{V_{g1} + V_{g2}}{2} - \sqrt{\frac{2I_{ref}}{K_{pn}(W/L)_{1,2}}} - V_{TN} \tag{8.10}$$

Solving Eqs. (8.2) and (8.8) yields:

$$V_{g1} + V_{g2} = \frac{(V_{in+} + V_{in-})C_i}{2C_i + C_{gs1} + C_{gb1} + C_{gd1}} + V_{fb} \tag{8.11}$$

$$V_{ref} = V_{DD} + V_{TP} - \sqrt{\frac{2I_{ref}}{K_{pp}(W/L)_8}} \tag{8.12}$$

Combining Eqs. (8.7)–(8.12):

$$V_{fb} = A_f \left(V_{DD} + 2V_{TP} + V_{TN}\right)$$
$$-A_F \left(\sqrt{\frac{2I_{ref}}{K_{pp}(W/L)_8}} + \sqrt{\frac{I_{ref}}{K_{pp}(W/L)_{5,6}}} - \sqrt{\frac{2I_{ref}}{K_{pn}(W/L)_{1,2}}} + \frac{V_{cm} + V_{fb}}{2}\right) \tag{8.13}$$

where $V_{cm} = (V_{in+} + V_{in-})/2$. Solving for $V_{fb}$, for sufficiently large $A_f$:

$$V_{fb} \approx 2\left(V_{DD} + 2V_{TP} + V_{TN}\right)$$
$$+2\left(\sqrt{\frac{2I_{ref}}{K_{pn}(W/L)_{1,2}}} - \sqrt{\frac{2I_{ref}}{K_{pp}(W/L)_8}} - \sqrt{\frac{I_{ref}}{K_{pp}(W/L)_{5,6}}}\right) - V_{cm} \tag{8.14}$$

Since $I_{ref}$, $(W/L)_{5,6}$, and $(W/L)_8$ are design variables for the differential pair, $(W/L)_{1,2}$ is solved for in terms of the other parameters. Setting $V_{fb} = -V_{cm}$ and solving

Eq. (8.14) for $(W/L)_{1,2}$ yields:

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2I_{ref}}{K_{pn}\left(\sqrt{\frac{I_{ref}}{K_{pp}(W/L)_{5,6}}} + \sqrt{\frac{2I_{ref}}{K_{pp}(W/L)_{8}}} - V_{DD} - 2V_{TP} - V_{TN}\right)^2} \quad (8.15)$$

As can be seen from Eq. (8.15), using an aspect ratio design method for obtaining $V_{fb} = -V_{cm}$ is susceptible to process variations in $K_{pp}$, $K_{pn}$, $V_{TP}$, and $V_{TN}$. Also, depending on the design of the rest of the amplifier, $(W/L)_{1,2}$ may need to be large to satisfy Eq. (8.15). This implies that the size of the capacitors $C_i$ and $C_{fb}$ will need to be larger as well, producing concerns about the area of the amplifier. To overcome these problems, we can achieve the desired result by generating a new reference for comparing $V_{tail}$. This can be accomplished using the circuit in Fig. 80. For this circuit, $(W/L)_{10} = (W/L)_4$, $(W/L)_{13} = (W/L)_1$, $(W/L)_{11} = (W/L)_5$, and $(W/L)_{12} = (W/2L)_7$. An important consideration in the design of this reference generator is to keep transistor $M_7$ in the saturation region. At the cost of added power consumption, this technique is more robust in the presence of fabrication tolerances because the desired reference is created based on transistor matching rather than single transistor characteristics. Furthermore, we gain a degree of freedom in the design of the PLS transistors. Smaller transistors can be used, yielding smaller floating gate capacitors, and less area.

To illustrate the more robust nature of the circuit in Fig. 80 as compared to that of Fig. 79 in regards to $g_m$ fluctuation, Monte Carlo simulations were run on each circuit. MOSFET threshold voltage and mobility were each varied using a normal distribution where 5% variation corresponds to $3\sigma$. The POLY-POLY2 sheet capacitance was also varied with a normal distribution with 10% $3\sigma$. The circuits were simulated 100 times each, and the variations of $g_m$ fluctuation over rail-to-rail common mode input are plotted as Figs. 81 and 82. As expected, the $g_m$ fluctuation

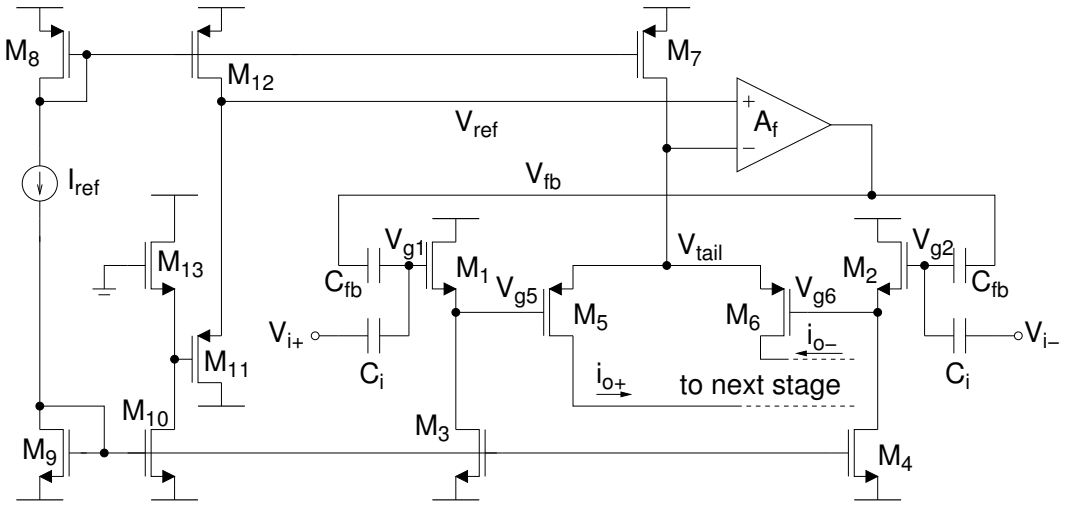



Fig. 80. Reference generation for the rail-to-rail input stage to ensure that $V_{cmg} \approx 0V$.

for the circuit in Fig. 79 is more sensitive to process variations compared to the circuit in Fig. 80. The standard deviations were simulated as 0.645% and 0.017% for Figs. 79 and 80, respectively.

## 2. Area

To minimize the area of the amplifier, the capacitors should be designed as small as possible. A traditional MIFG design rule is to make the floating gate capacitor 5–10 times the sum of the parasitic capacitance connected to the floating node. Using MIFG transistors thus usually comes with the cost of drastically increasing the necessary silicon area. In the case of this amplifier, the negative feedback partially compensates for the effects of the parasitics. The effects of the capacitance associated with $M_1$ from Fig. 79 on transconductance magnitude and transconductance fluctuation are now analyzed in order to minimize the area associated with this input stage.

Considering the small signal equivalent to the circuit in Figs. 79 and 80, the

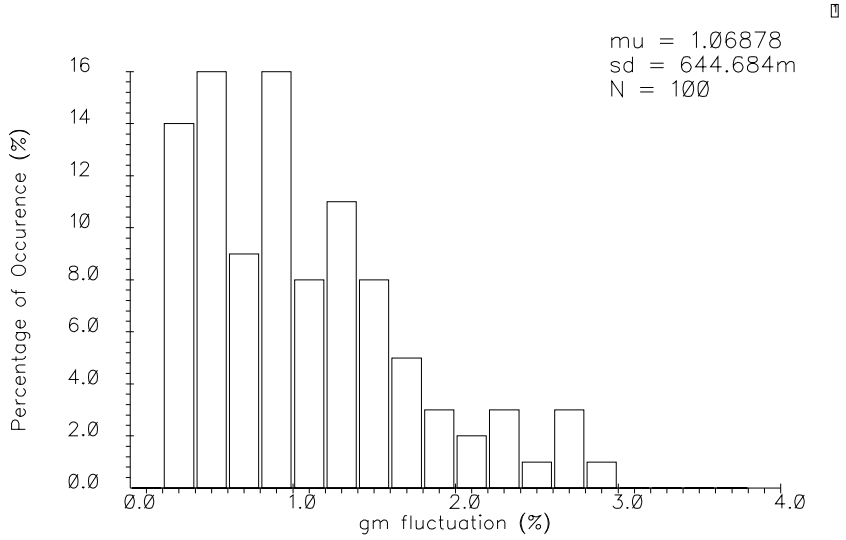



Fig. 81. Simulated statistical distribution of $g_m$ fluctuation in the presence of process variation for the circuit in Fig. 79.

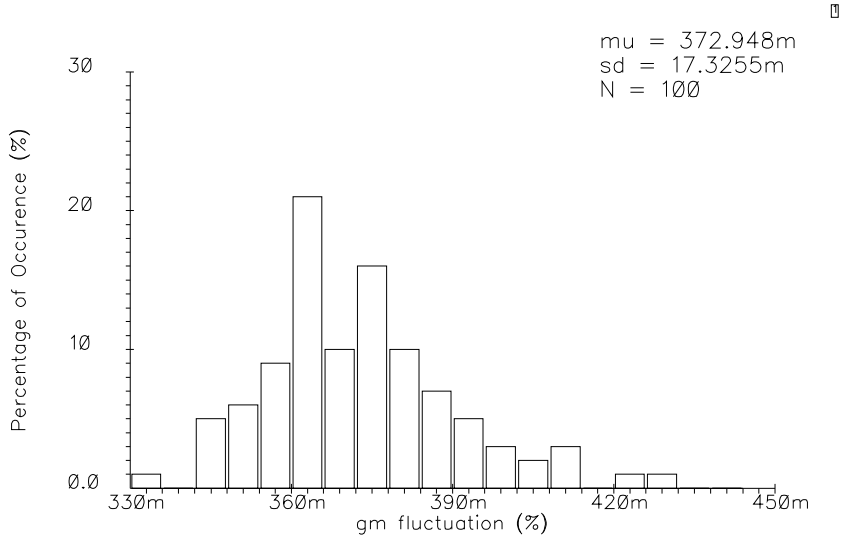



Fig. 82. Simulated statistical distribution of $g_m$ fluctuation in the presence of process variation for the circuit in Fig. 80.

differential output current of the transconductor will be:

$$i_o = i_{o+} - i_{o-} = g_{m5}v_{g5} - g_{m6}v_{g6} \tag{8.16}$$

Transistors $M_5$ and $M_6$ are matched, thus $g_{m5} = g_{m6} = g_m$, and

$$i_o = g_m(v_{g5} - v_{g6}) \tag{8.17}$$

Considering the source follower configurations of $M_1$ and $M_2$, and assuming $g_{mb1,2} = \chi_n g_{m1,2}$:

$$v_{g5} = \frac{v_{g1}}{1+\chi_n} \tag{8.18}$$

$$v_{g6} = \frac{v_{g2}}{1+\chi_n} \tag{8.19}$$

Assuming the parasitic capacitance, $C_{gs1} = C_{gs2} = C_{gs}$, $C_{gb1} = C_{gb2} = C_{gb}$, and $C_{gd1} = C_{gd2} = C_{ds}$:

$$v_{g1} = \frac{v_{fb}C_{fb} + v_{i+}C_i + v_{g5}C_{gs}}{C_{fb} + C_i + C_{gs} + C_{gb} + C_{gd}} \tag{8.20}$$

$$v_{g2} = \frac{v_{fb}C_{fb} + v_{i-}C_i + v_{g6}C_{gs}}{C_{fb} + C_i + C_{gs} + C_{gb} + C_{gd}} \tag{8.21}$$

where:

$$v_{fb} = -A_f v_{tail} \tag{8.22}$$

The voltage, $v_{tail}$, behaves as an AC ground for the differential voltages of $v_{g5}$ and $v_{g6}$, and as a source follower for common mode signals. Assuming $g_{mb5,6} = \chi_p g_{m5,6}$,

$$v_{tail} = \frac{v_{g5} + v_{g6}}{2(1+\chi_p)} \tag{8.23}$$

Using the common-mode representation of differential signals:

$$v_{i+} = v_{cm} + \frac{v_d}{2} \tag{8.24}$$

$$v_{i-} = v_{cm} - \frac{v_d}{2} \tag{8.25}$$

where $v_{cm}$ is the common mode component to the input signal, and $v_d$ is the differential input. Solving Eqs. (8.17)—(8.25), we obtain:

$$i_o = \frac{g_m v_d C_i}{(C_i + C_{fb} + C_{gd} + C_{gb})(1 + \chi_n) + \chi_n C_{gs}} \tag{8.26}$$

Thus, yielding a total effective transconductance of:

$$G_m = \frac{i_o}{v_d} = g_m \frac{C_i}{(C_i + C_{fb} + C_{gb} + C_{gd})(1 + \chi_n) + \chi_n C_{gs}} \tag{8.27}$$

Some attenuation in transconductance, and in turn the GBW, can not be avoided, due to the nature of floating gate transistors. In order to minimize the effects of $C_{gs}$, $C_{gb}$, and $C_{gd}$ on this attenuation, it should be ensured that:

$$C_i \gg \chi_n C_{gs}, C_{gb}, C_{gd} \tag{8.28}$$

However, this is perhaps not the best option. If $C_i$ and $C_{fb}$ are reduced in size, the die area will become smaller at the cost of reducing the effective transconductance ($G_m$) of the input stage. This $G_m$ degradation can be compensated for by widening the differential pair driver transistors, $M_5$ and $M_6$. Given a certain floating gate capacitor size, the aspect ratios of the driver transistors can be calculated by substituting $g_m = \sqrt{I_{ref} K_{pp} W_5 / L_5}$ into Eq. (8.27) and solving for $W_5/L_5$. Doing so yields:

$$\frac{W_5}{L_5} = G_m^2 \frac{[(C_i + C_{fb} + C_{gb} + C_{gd})(1 + \chi_n) + \chi_n C_{gs}]^2}{C_i^2 I_{ref} K_{pp}} \tag{8.29}$$

The effects of capacitor sizes on transconductance fluctuation is now analyzed. Note that the transconductance of the input stage will deviate from its nominal value as a result of changes in the voltage $v_{tail}$ due to $\lambda$ effects on transistor $M_7$. Using Eqs. (8.18)—(8.25), and solving for $v_{tail}$ yields:

$$v_{tail} = \frac{v_{cm} C_i}{(1 + \chi_n)(1 + \chi_p)(C_{fb} + C_i + C_{gd} + C_{gb}) + \chi_n (1 + \chi_p) C_{gs} + A_f C_{fb}} \tag{8.30}$$

For sufficiently large $A_f$, $v_{tail}$ can be approximated with:

$$v_{tail} \approx \frac{v_{cm} C_i}{C_{fb} A_f} \tag{8.31}$$

As long as the $C_{fb}A_f$ product is large, variations in $v_{tail}$ will be small, resulting in near zero fluctuations in the input stage transconductance across all common mode input levels within the supply range.

To save silicon area, we recommend setting $C_i = C_{fb} = C_{gs}$ and compensating for the additional attenuation by sizing the driver transistors $M_5$ and $M_6$ according to Eq. (8.29). Designing the floating gate transistors in this way offers large savings in capacitor area when compared to traditional designs that set the floating capacitors equal to 5–10 times the size of the parasitics [23, 29].

### 3. Feedback Loop Stability

As with any negative feedback system, it is important to consider the circuit stability. In the entire loop, there are four poles and two zeroes. If the feedback amplifier, $A_f$ in Fig. 79, is implemented with an OTA having transconductance $g_{mA}$, it will contribute two poles to the system. The dominant pole of the system will be associated with the output of the OTA, and a non-dominant pole will be associated with its internal node. A third pole and one zero is due to the MIFG level shifters, and the final pole and zero is due to the differential pair, which for common mode voltages behaves as a source follower. For this analysis, only the three most dominant poles and none of the zeros are considered. The capacitive load of the source followers consists of parasitic source to bulk and gate to source capacitors. These are assumed to be sufficiently small such that the zero and the possibility of complex conjugate poles in the source followers is neglected. The first non-dominant pole, $\omega_{ndgm}$ is from the OTA, and the second, $\omega_{nd1}$, is the smaller of the remaining two. Since for differential inputs, the

voltage $V_{tail}$ in Fig. 79 behaves as an AC ground, only changes in the common mode level of the input, $V_{cm}$, are considered. Assuming low frequency unity gain for the source followers and solving the feedback circuit for $V_{fb}/V_{cm}$ yields the following third order transfer function.

$$\frac{V_{fb}}{V_{cm}} = \frac{C_i}{C_i + C_{gg}} \frac{s^3 + (\omega_{ndgm} + \omega_{nd1})s^2 + \omega_{ndgm}\omega_{nd1}s - \dfrac{g_{mA}\omega_{ndgm}\omega_{nd1}}{2C_{fb}}}{s^3 + (\omega_{ndgm} + \omega_{nd1})s^2 + \omega_{ndgm}\omega_{nd1}s + \dfrac{g_{mA}\omega_{ndgm}\omega_{nd1}}{2(C_i + C_{gg})}} \tag{8.32}$$

where $C_{gg}$ is the total parasitic capacitance associated with the gate of transistor $M_1$ from Fig. 79. Using the Routh stability criteria, the circuit will be stable when the following condition is met:

$$\omega_{ndgm} + \omega_{nd1} > \frac{g_{mA}}{2(C_i + C_{gg})} \tag{8.33}$$

For simplicity, assume that $\omega_{ndgm} \ll \omega_{nd1}$ so that for stability it is sufficient to ensure that $g_{mA}/2(C_i + C_{gg}) < \omega_{nd1}$. This condition is easily met considering the fact that $\omega_{nd1}$ is due to a source follower circuit, and will typically be located at very high frequencies. Assuming that $g_{mA}$ of the feedback OTA is comparable in magnitude to the source follower transistor's transconductance, for stability, it should be ensured that $C_i$ in Fig. 79 is greater than the parasitic capacitances located at the nodes $V_{g5}$ and $V_{g6}$. Note that since $V_{tail}$ behaves nearly as a buffer for common mode changes of $V_{g5}$ and $V_{g6}$, the effects of the parasitic gate to source capacitors, $C_{gs5}$ and $C_{gs6}$, can be neglected.

To verify Eq. 8.32, the AC magnitude, AC phase and step responses were obtained via transistor level simulations, and compared to its equivalent mathematical response. These are plotted respectively in Figs. 83, 84, and 85. As seen by these figures, Eq. 8.32 is a sufficient approximation to the simulated behavior of the feedback. The parameters extracted from the simulation and used in evaluating Eq. 8.32 are:

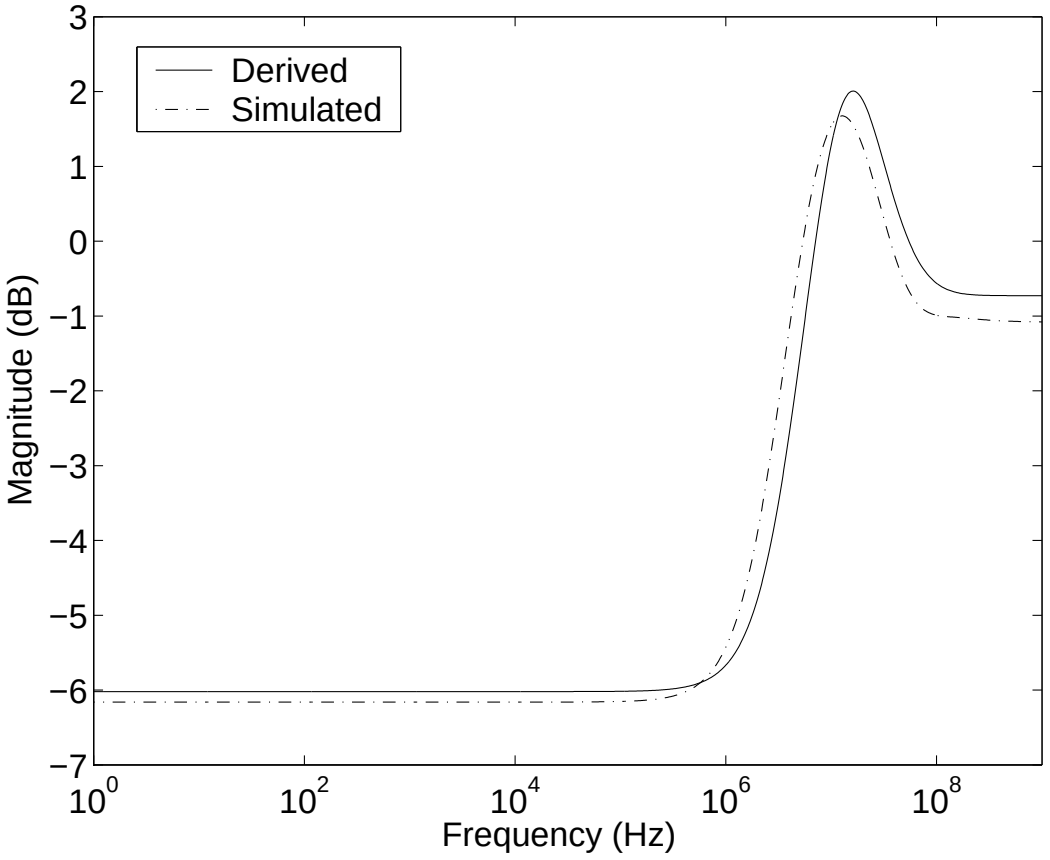



Fig. 83. Simulated and derived AC magnitude response of $V_{fb}/V_{cm}$.

$C_{fb} = 8$ pF, $C_i = 4$ pF, $C_{gg} = 0.35$ pF, $\omega_{ndgm} = 2\pi 30$ Mrad/s, $\omega_{nd1} = 2\pi 100$ Mrad/s, $g_{mA} = 378$ $\mu$A/V.

### 4. Noise and Linearity

The noise introduced by the feedback in this circuit will appear as a voltage at the node $V_{fb}$ in Fig. 79, which is a common voltage to both input transistors. Thus the feedback noise will be canceled by the subtraction operation of the differential pair. However, while the feedback itself does not introduce additional noise, the input referred noise of this topology will slightly suffer due to the first stage attenuating effect of MIFG transistors. If this attenuation is not excessive, the overall noise

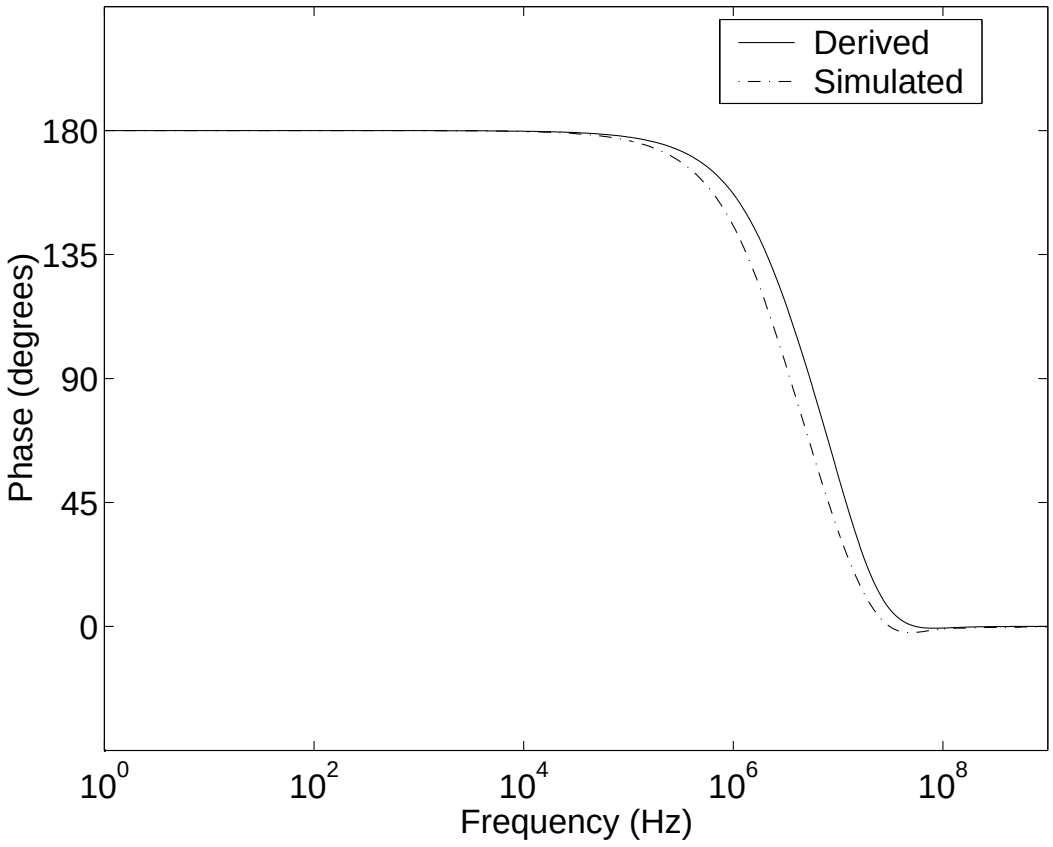



Fig. 84. Simulated and derived AC phase response of $V_{fb}/V_{cm}$.

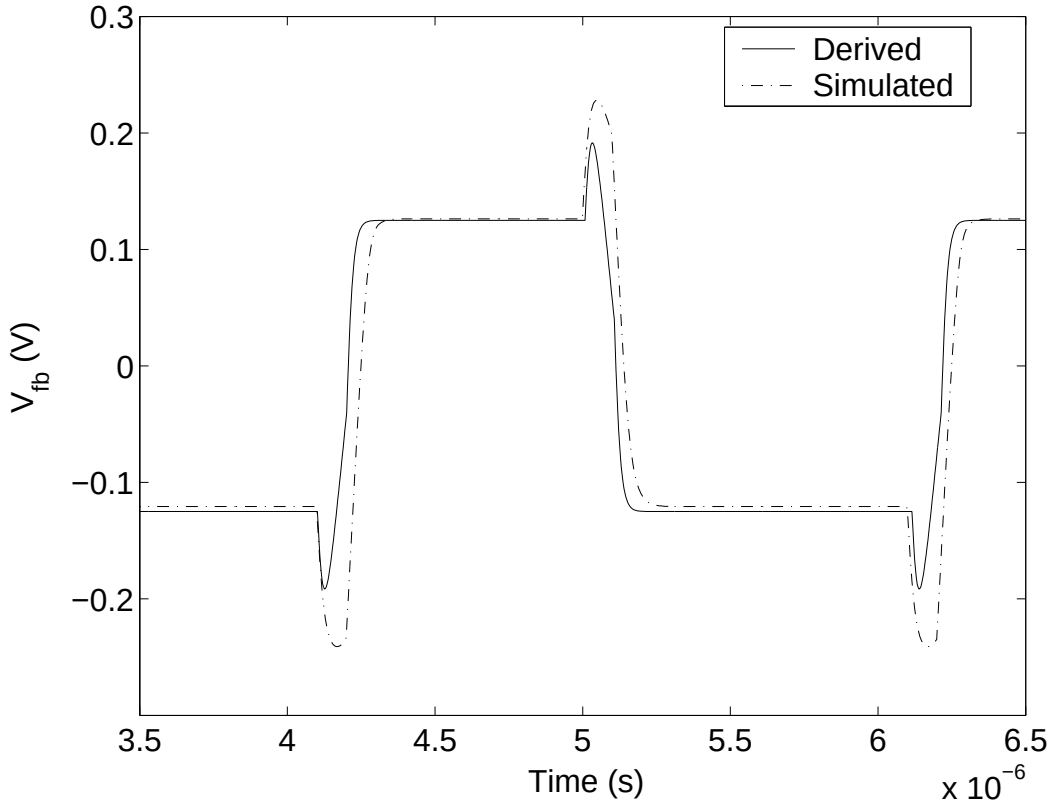



Fig. 85. Simulated and derived step response of $V_{fb}/V_{cm}$.

should be comparable to other rail-to-rail amplifier architectures that employ multiple differential pairs. For instance, assume $C_i = C_{fb}$, resulting in an attenuation of two. The input referred noise will thus be increased by a factor of two as compared to a traditional single channel differential pair. Now consider a rail-to-rail topology that uses complimentary differential pairs [26]. The transconductance of the N-channel and P-channel differential pairs are designed to be equal, and thus their noise contributions will also be the same. The input referred noise of these architectures are also twice as large as a traditional single channel differential pair.

This topology inherently possesses two linearization techniques for the differential V-I characteristics of the differential pairs. The first linearity enhancement results from the attenuation of the input. Assume the V-I characteristics of a traditional differential pair can be sufficiently expressed as a third order Taylor series where

$$i_o = g_1 v_d + g_2 v_d^2 + g_3 v_d^3 \tag{8.34}$$

where $i_o$ is the differential output current and $v_d$ is the differential input of the transconductor, resulting in $HD_2 = v_d g_2/(2g_1)$ and $HD_3 = v_d^2 g_3/(4g_1)$ [31]. Including the input attenuation of the proposed amplifier, the V-I characteristics will be

$$i_o = g_1 \frac{C_i}{C_i + C_{fb}} v_d + g_2 \left( \frac{C_i}{C_i + C_{fb}} v_d \right)^2 + g_3 \left( \frac{C_i}{C_i + C_{fb}} v_d \right)^3 \tag{8.35}$$

resulting in

$$HD_2 = \frac{v_d g_2 C_i}{2g_1(C_i + C_{fb})} \tag{8.36}$$

$$HD_3 = \frac{v_d^2 g_3 C_i^2}{4g_1(C_i + C_{fb})^2} \tag{8.37}$$

If $C_i = C_{fb}$ this technique offers a 6 dB improvement in $HD_2$ and 12 dB improvement in $HD_3$ in the differential V-I conversion as compared to a traditional differential pair.

The second linearization technique inherent to this topology lies in the fact that the feedback fixes the operating point of the differential pair. Much of the third order nonlinearity in traditional differential pairs is a result of $\lambda$-effects on the tail current source transistor modulating the second order effects of the differential pair [32]. These second order effects appear as a common mode signal at the coupled source of the driver transistors. The feedback used in this chapter successfully tracks and compensates for this error via the feedback voltage, $V_{fb}$.

## E. Experimental Results

The output current of the input stage went to a folded cascode circuit for gain enhancement, followed by the rail-to-rail class-AB output stage from [26]. The complete amplifier schematic is shown in Fig. 86. The suggested biasing improvements discussed in section 1 and displayed in Fig. 80 were developed after fabrication and verification, thus the experimental results provided here are only for the input stage displayed in Fig. 79. The circuit was fabricated through, and thanks to, MOSIS using AMI's $0.5\mu m$ process. A micro-graph is displayed in Fig. 87. Symmetric supply voltages of $\pm 1.5$ V were used. Since the focus of this chapter is on a rail-to-rail input stage, the measurement results have been divided into two subsections. Because the class-AB output stage limits the amplitudes of signals to the supply levels, the input transconductor was first characterized. The second section contains data on the entire amplifier, which includes the class-AB output stage. Five chips were received from MOSIS, and no significant differences were observed between them.

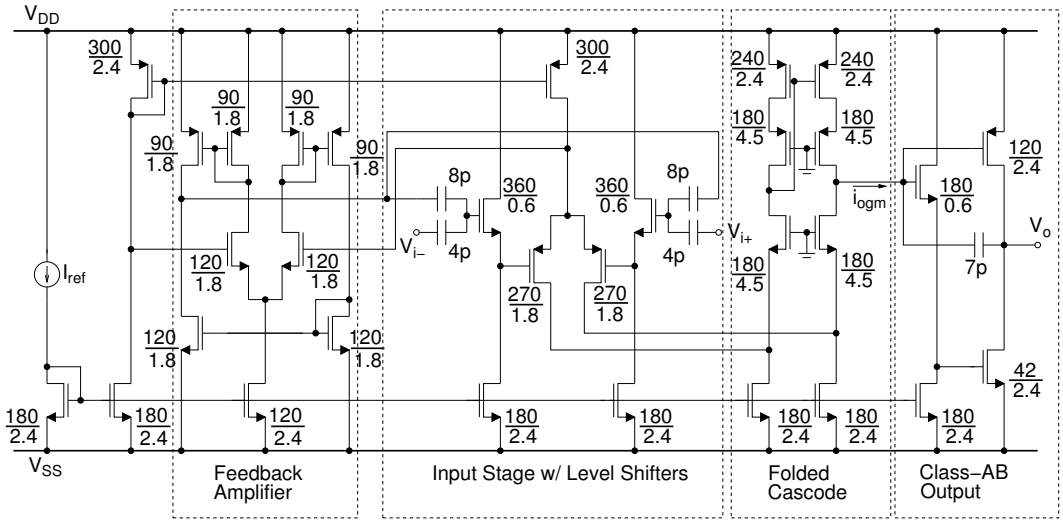



Fig. 86. Amplifier schematic.

### 1. The Input Transconductor

The output current of the input transconductor was taken from the output of the folded cascode stage, $I_{ogm}$ of Fig. 86. To measure the common mode range of the input, a common mode 50 Hz triangular signal with 4.4 $V_{pp}$ amplitude (shown in Fig. 88a) was added to a differentially applied sinusoid (shown in Fig. 88b). The output current of the transconductor was loaded with a $1k\Omega$ resistor, creating the output voltage shown in Fig. 88c. The output of the transconductance amplifier remained virtually unchanged, regardless of the common mode level, which ranged from -2.2 to 2.2 V.

A plot of the input stage transconductance against the input common mode level is given in Fig. 89. The transconductance varied by only $\pm 0.35\%$ for rail-to-rail common mode levels of -1.5V to 1.5V. The previous best reported results were $\pm 1.5\%$. Beyond the rails, from -2V to 2V, the change in transconductance was just $\pm 1\%$.

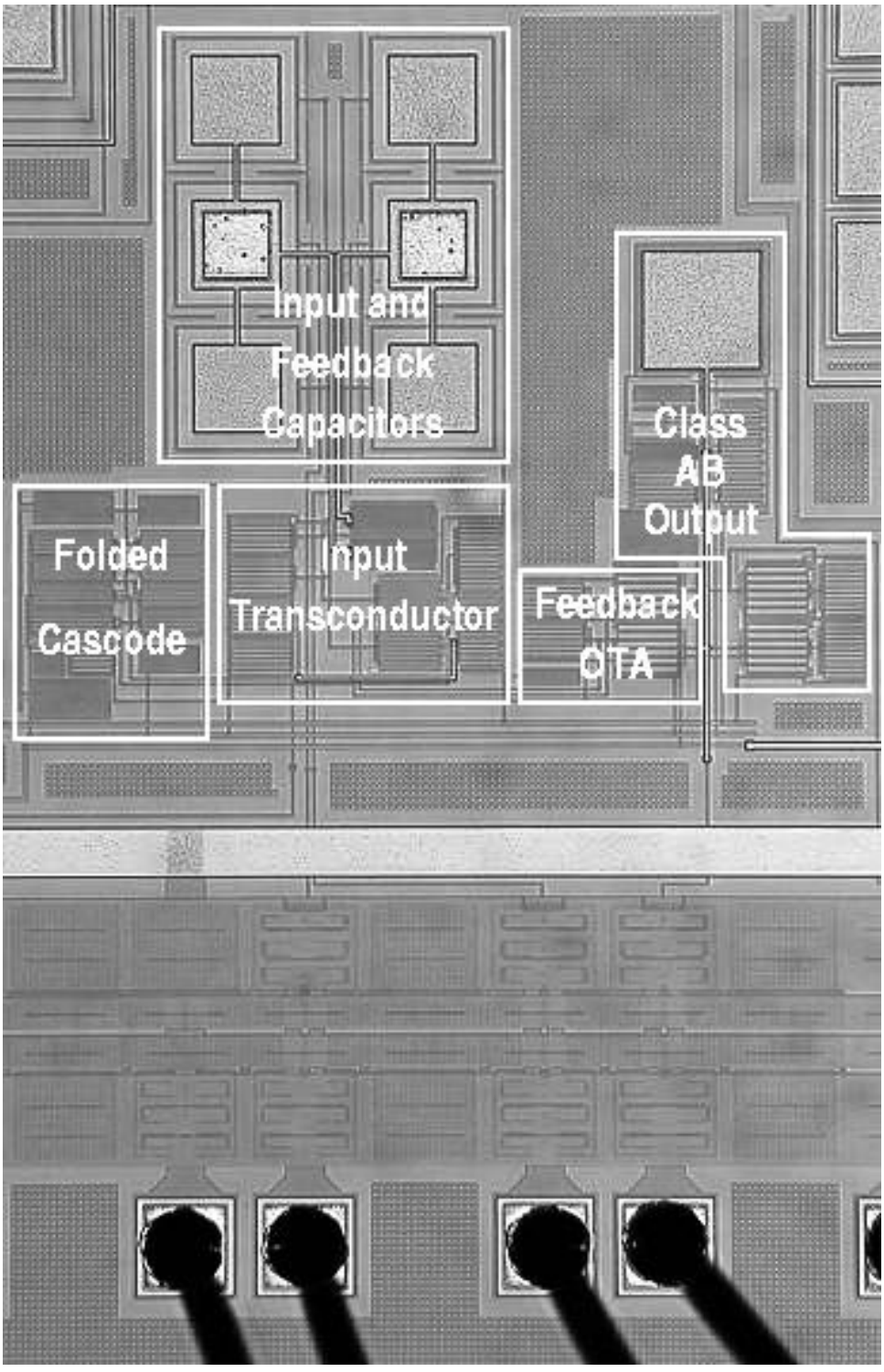
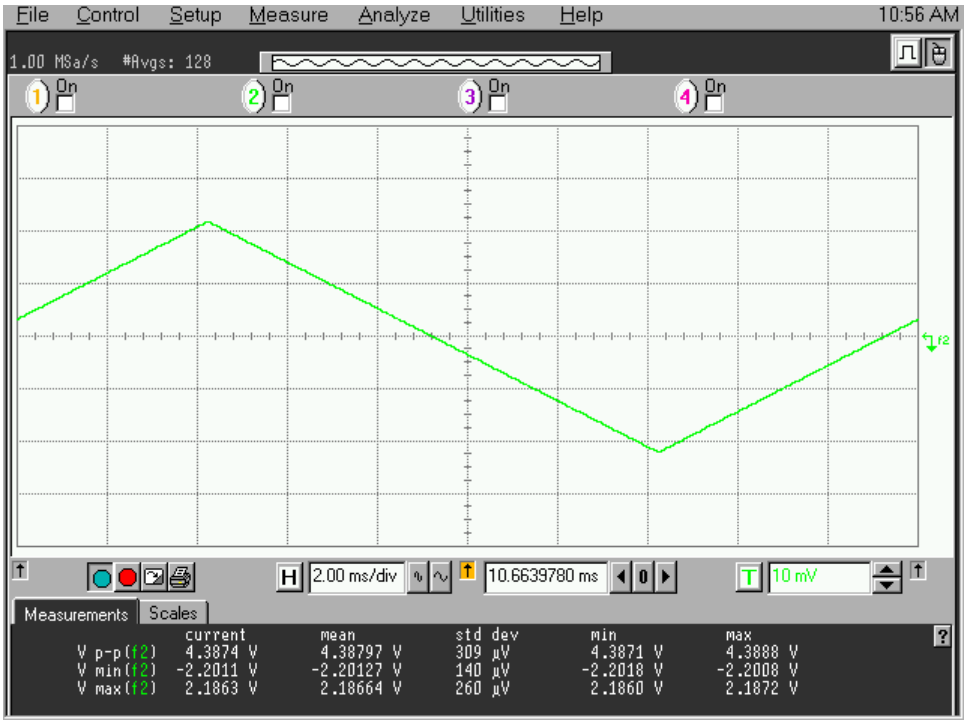



Fig. 87. Micro-graph of the amplifier.

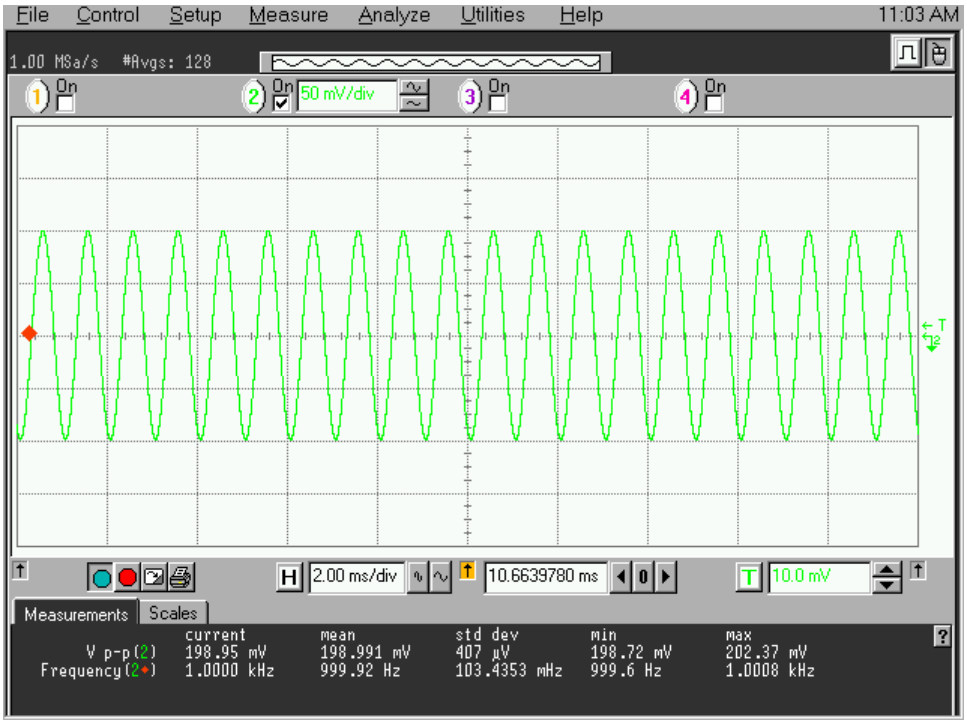
## 2. The Entire Amplifier with Rail-to-Rail Input Stage and Class-AB Output Stage

The following experimental results are for the complete operational amplifier. The AC open loop gain characteristics of the amplifier are displayed in Fig. 90. The GBW of the amplifier was 1.17 MHz, with a phase margin of 54° Since one of the primary applications of a rail-to-rail amplifier is a buffer, the amplifier was placed in the unity-gain feedback configuration. Figure 91 shows the response to a rail-to-rail step input. Figure 92 shows the response to a 2.3V step input. The overshoot was 10% and the 2% settling time was $1\mu s$. Since linearity is a concern in buffer design, the total harmonic distortion was measured, and plotted against different amplitudes and frequencies in Fig. 93. The spectrum of one such measurement is given in Fig. 94. This spectrum corresponds to the time domain output signal provided in Fig. 95. Table VII provides a comparison of this work to previous work on this topic. Please note that the area could have been reduced to $.21mm^2$ at the cost of $300\mu W$ of power using the techniques described in sections 1 and 2. Circuit simulations display comparable performance parameters to those experimentally verified in this chapter.




(a)

Fig. 88. Experimental results. a) Common mode input. b) Differential input. c) Output voltage, where $V_o = 1000I_o$ in response to an input equal to the common mode signal of Fig. 88a added to the differential signal of Fig. 88b.




(b)


(c)

Fig. 88 (Continued)

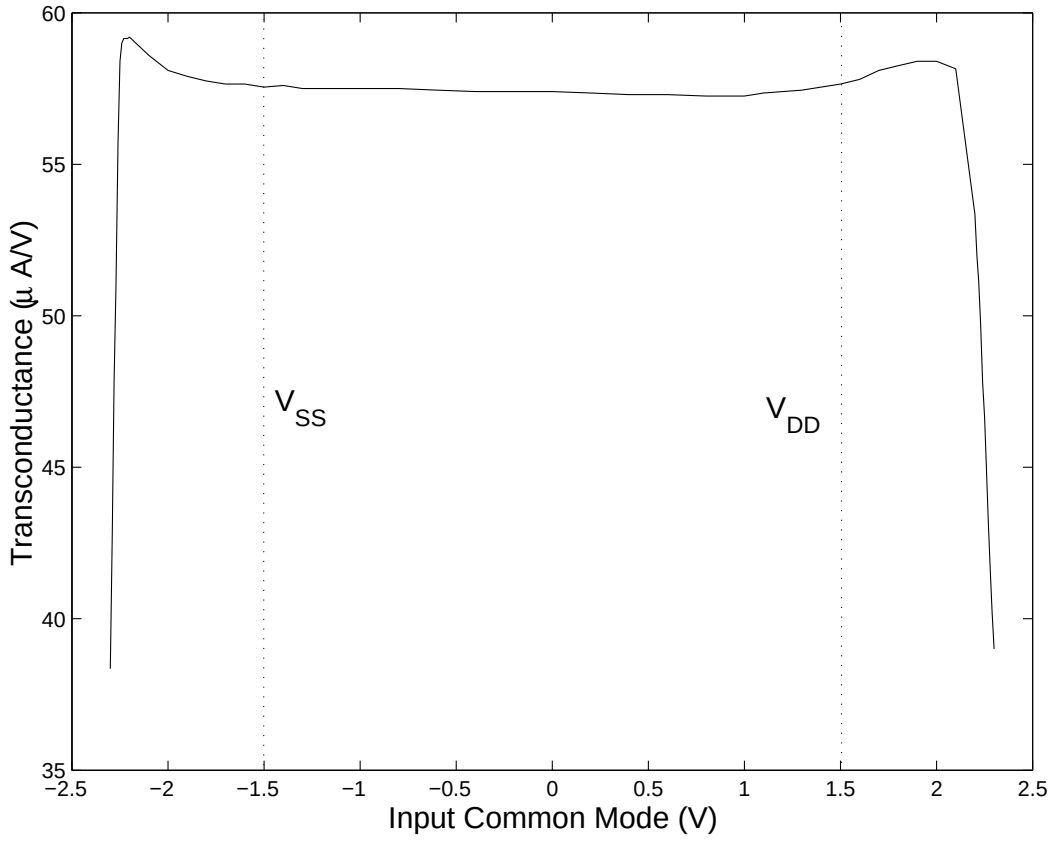



Fig. 89. Input stage transconductance vs. input common mode.

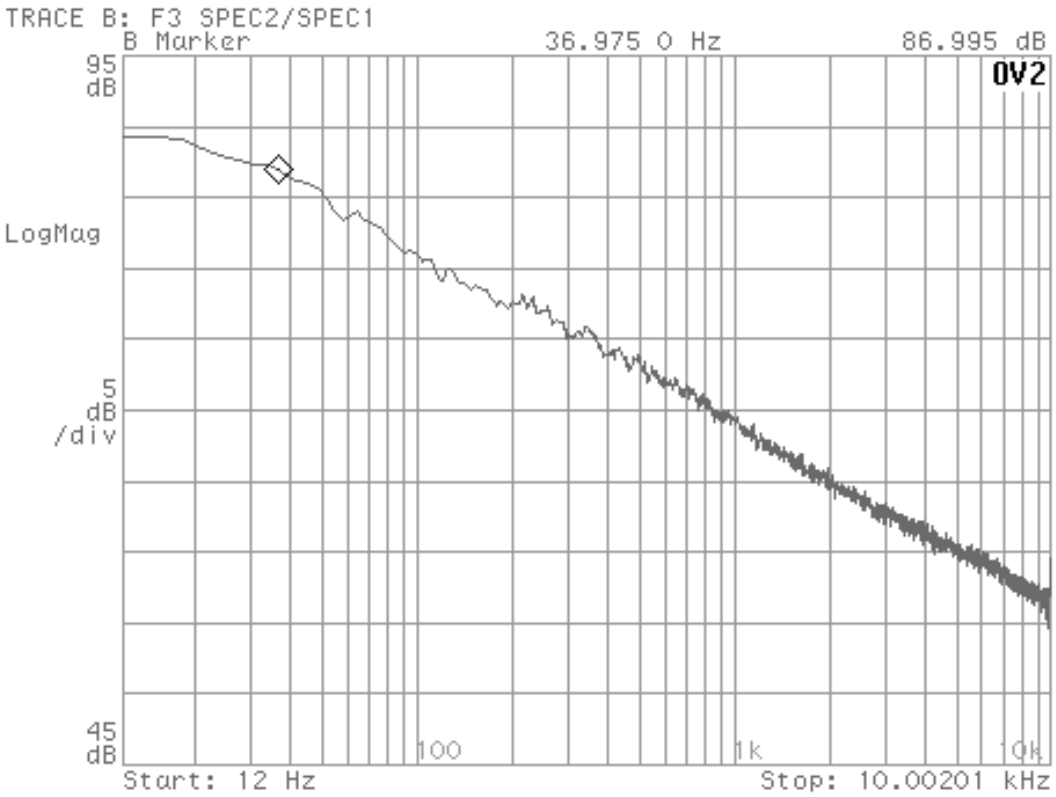



Fig. 90. AC gain of the amplifier versus frequency.

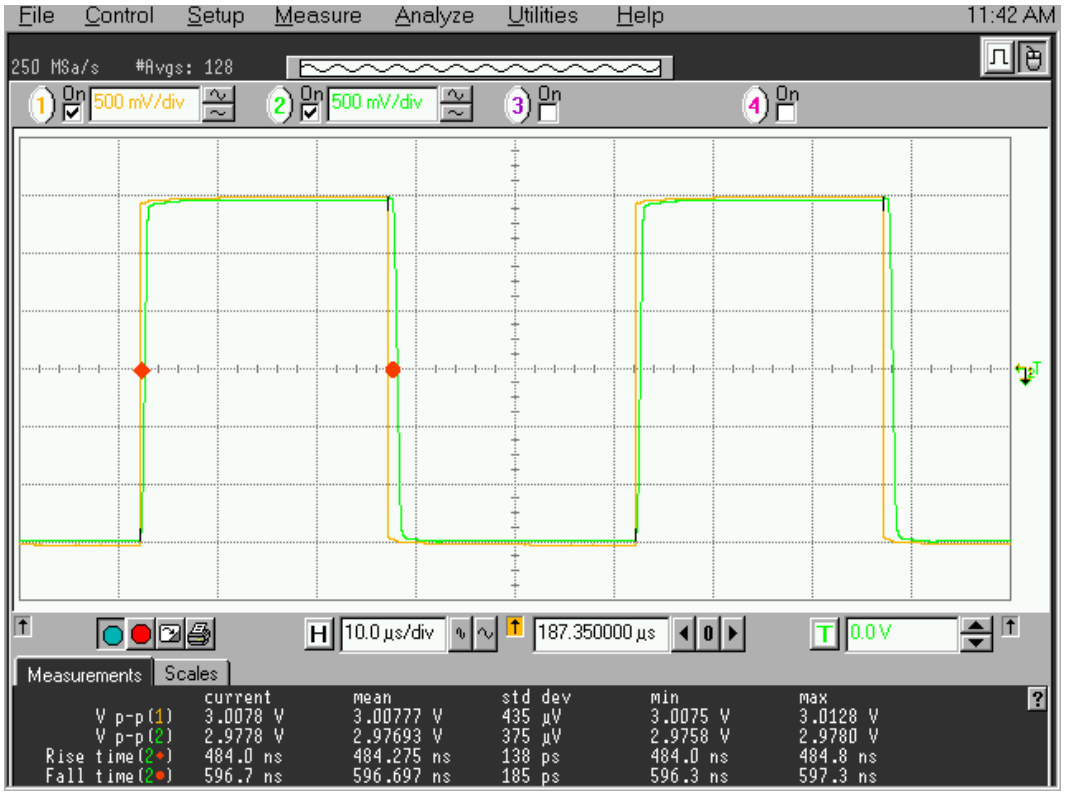



Fig. 91. Rail-to-rail unity gain step response.


Fig. 92. 2.3 $V_{pp}$, 100 kHz unity gain step response.

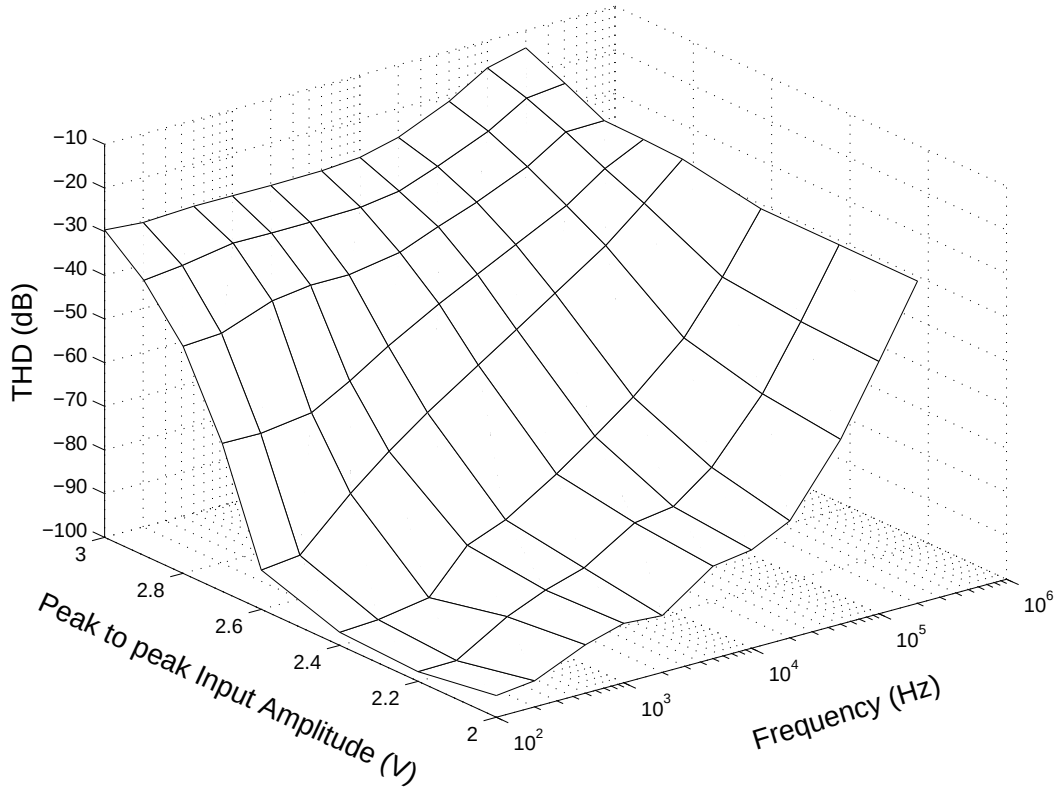



Fig. 93. THD vs. input amplitude and frequency.

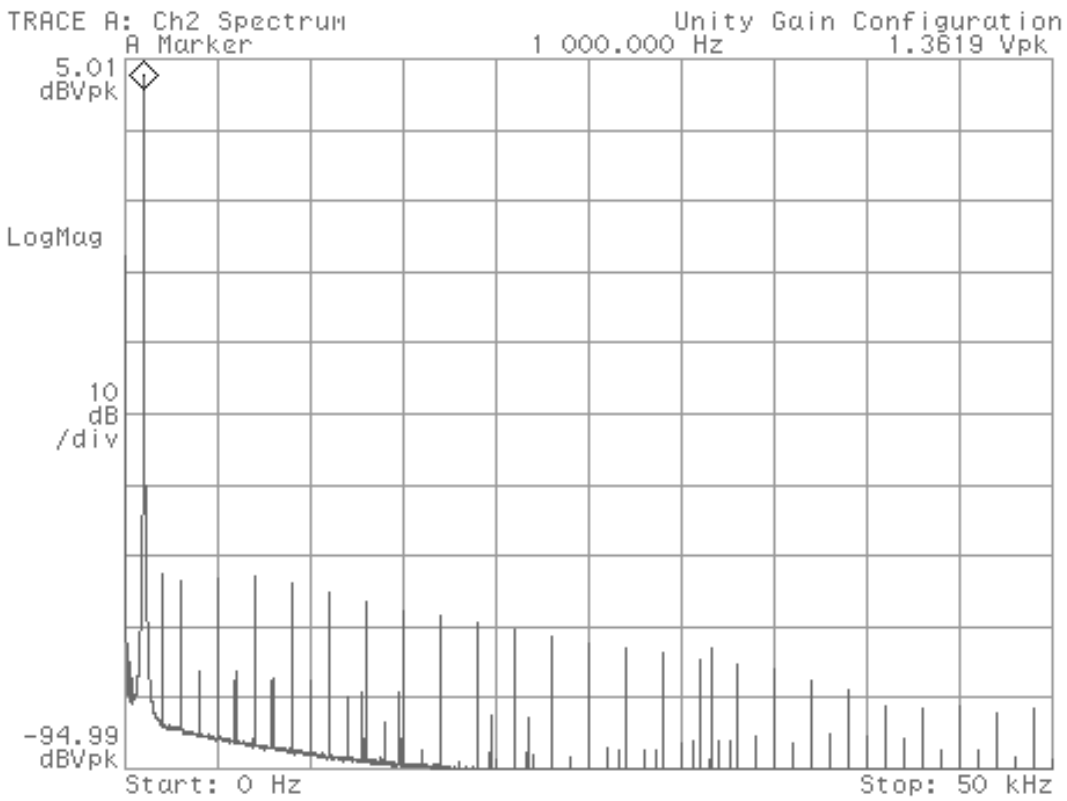



Fig. 94. Output spectrum of the amplifier in the voltage follower configuration for $V_{in} = 1.4 \sin 2\pi 1000t$. SFDR=70dB.

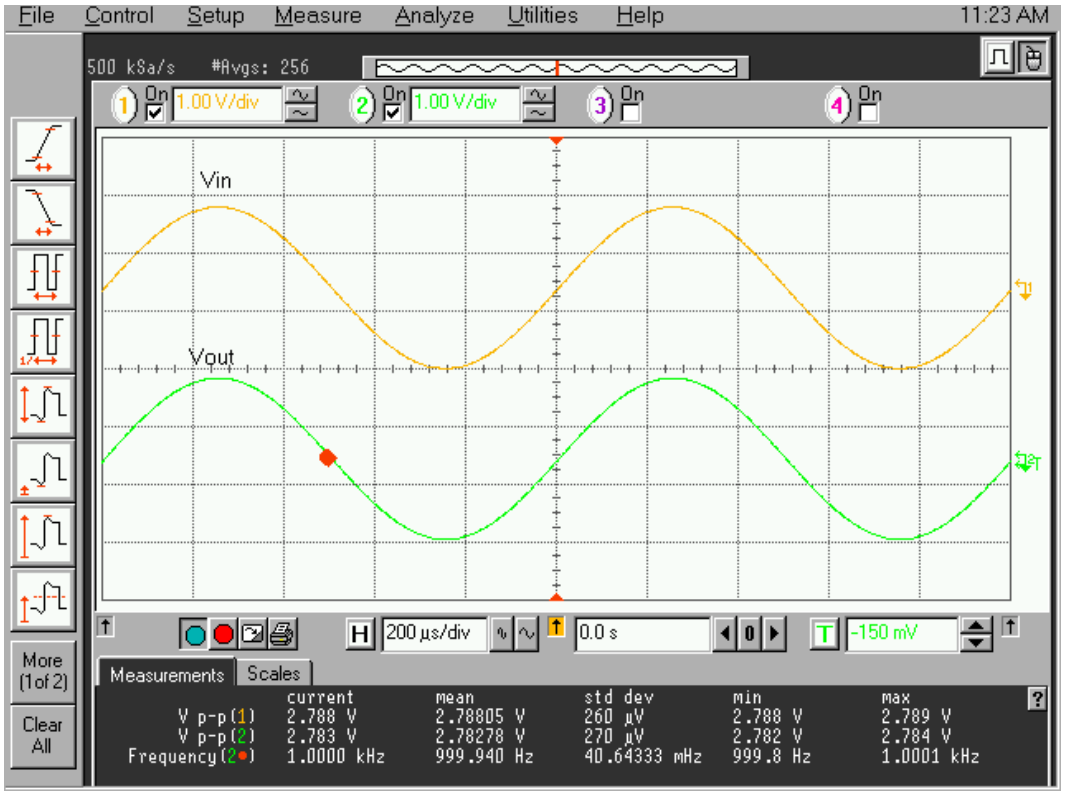



Fig. 95. Time domain waveform corresponding to the spectrum in Fig. 94.

Table VII. Table comparing this work to previous work

| **Parameter** | **This Work** | **[27]** | **[26]** | **[33]** | **[29]** | **[34]** |
|---|---|---|---|---|---|---|
| $\Delta g_m$ | $\pm 0.35\%$ | $\pm 1.5$ % | $\pm 4$ % | $\pm 3\%$ | NA | $\pm 4.6\%$ |
| Input Common Mode Range | $V_{SS}$ to $V_{DD}$ | $V_{SS}$ to $V_{DD}$ | $V_{SS} + .04$ to $V_{DD} - .07$ | $V_{SS}$ to $V_{DD}$ | $V_{SS}$ to $V_{DD}$ | $V_{SS}$ to $V_{DD}$ |
| DC Gain (dB) | 89 | 70 | 110 | 84 | 60 | 59 |
| GBW (MHz) | 1.2 | 1 | 3.2 | 1.3 | 5 | 5.9 |
| $CMRR_{DC}$ (dB) | 80 | NA | 88 | 56 | 47 | NA |
| SR (V/$\mu s$) | 5 | NA | 5.8 | 1 | 7 | 6.4 |
| Power (mW) | .51 | NA | .31 | .46 | .19 | NA |
| Area ($mm^2$) | .36 | NA | .12 | 1.2 | .09 | NA |
| Technology | $0.5\mu m$ | $0.8\mu m$ | $1.2\mu m$ | $.7\mu m$ | $0.8\mu m$ | $0.8\mu m$ |

# CHAPTER IX

## CONCLUSIONS

It has been shown that the received interference power of many practical interference sources may pose a threat to reliable UWB communication. To combat this problem, a baseband solution was provided for NBI in MB-OFDM UWB receivers. A notch filter was designed to be included after down-conversion and lowpass filtering in the UWB receive chain. The filter utilizes digital center frequency control, and an analog LMS control for minimizing the interference amplitude. The full design cycle, specification to design to layout to measurements , has been presented in this dissertation. The result was a fully functional notch filter, whose center frequency was measured to be tunable from 1.6 MHz to 278 MHz, and bandwidth was maintained around 23 MHz throughout the tuning range. This result was very close to the specification and initial schematic level design.

Furthermore, a new method for achieving constant $g_m$ in a rail-to-rail amplifier was introduced. It uses only one input differential pair by making use of programmable level shifters via MIFG transistors in the source follower configuration. The common mode is shifted to a constant value before the signal is input to the differential pair. Since the common mode level of the differential pair is fixed, consistent operation for rail-to-rail common mode inputs is achieved. Furthermore, since only one differential pair was used, there is no degradation in the CMRR for any input common mode levels, which is a problem for rail-to-rail architectures that use complimentary input differential pairs. Experimental measurements of this amplifier showed only $\pm 0.35\%$ deviation in the input stage transconductance, whereas the best previously reported was $\pm 1.5\%$.

## A. Future Work and Suggestions

To successfully complete the design cycle, the interference detection and center frequency tuning system need to be implemented and tested. Furthermore, since the filter's 24MHz bandwidth affects around 6 subchannels, some digital correction techniques may still be necessary.

One drawback of the filter is its large size. This is due to the 8-bit center frequency control being fully thermometer coded. If area is of more concern in the design, this 8-bit control could be segmented into thermometer coded MSBs and binary coded LSBs. For example, a 5-bit thermometer, 3-bit binary coding would result in an area reduction of 8x. Care must be taken to not segment too much into the binary coding because, due to mismatch between components, there may be too much spacing between adjacent channels, which would leave some frequencies in the UWB band that could not be filtered.

## B. Impact

The problem of narrowband interference from neighboring electronic devices has not attracted the attention it deserves. This work has shown that electromagnetic radiation levels from common devices are powerful enough to disrupt UWB communication. Furthermore, a novel analog notch filter has been designed and presented as a potential solution to this problem. The novelty of the filter lies in the implementation simplicity of the analog LMS feedback loop, and in the extremely wide center frequency tuning range that spans over two decades, while maintaining a near constant bandwidth.

# REFERENCES

[1] *Part 15 - Radio Frequency Devices*, Federal Communications Commission Std., Aug. 2003.

[2] R. Fisher, R. Kohno, H. Ogawa, H. Zhang, K. Takizawa, *et al.*, *DS-UWB Physical Layer Submission to 802.15 Task Group 3a*, IEEE Working Draft Proposed Standard, July 2004.

[3] A. Batra, J. Balakrishnan, A. Dabak, R. Gharpurey, J. Lin, *et al.*, *Multi-band OFDM Physical Layer Proposal*, IEEE Working Draft Proposed Standard, Sept. 2004.

[4] S. B. Weinstein and P. M. Ebert, "Data transmission by frequency-division multiplexing using the discrete Fourier transform," *IEEE Trans. Commun.*, vol. 19, no. 5, pp. 628–634, Oct. 1971.

[5] J. L. Cimini, "Analysis and simulation of a digital mobile channel using orthogonal frequency division multiplexing," *IEEE Trans. Commun.*, vol. 33, no. 7, pp. 665–675, July 1985.

[6] J. Bingham, "Multicarrier modulation for data transmission: an idea whose time has come," *IEEE Commun. Mag.*, vol. 28, no. 5, pp. 5–12, May 1990.

[7] "Test report for the LAN interface card, M3F2-PCIXE-2," Myricom Inc., Tech. Rep., Jan. 2004.

[8] "Test report for the LAN switch, M3-CLOS-ENCL," Myricom Inc., Tech. Rep., Nov. 2004.

[9] "Reply comments of Time Domain Corporation in the matter of revision of part 15 of the FCC's rules regarding ultra-wideband transmission systems," Time Domain Corporation, Tech. Rep., Feb. 1999.

[10] "Electromagnetic emissions test report and verification of compliance per FCC part 15, subpart b specifications for a class B digital device and ICES-003 class B on the PalmOne, Inc. Model: TREO 650 (CDMA)," Elliot Laboratories, Inc., Tech. Rep., Sept. 2004.

[11] M. Dirjish, "Cabinets, enclosures, and backplanes - no housing shortage for the electronics market," Nov. 2003. [Online]. Available: http://www.eepn.com/Issues/IssueID/121/Index.html

[12] J. Ellis, R. Roberts, and K. Siwiak, "P802.15. tg3a alt PHY selection criteria," IEEE, Tech. Rep., Dec. 2002.

[13] J. Foerster, "Channel modeling sub-committee report final," IEEE, Tech. Rep., Nov. 2002.

[14] L. B. Milstein, "Interference rejection techniques in spread spectrum communications," *Proc. IEEE*, vol. 76, no. 6, pp. 25–33, June 1988.

[15] J. D. Laster and J. H. Reed, "Interference rejection in digital wireless communications," *IEEE Signal Processing Mag.*, vol. 14, no. 3, pp. 37–62, May 1997.

[16] R. A. Iltis, J. A. Ritchey, and L. B. Milstein, "Interference rejection in FFH systems using least squares estimation techniques," *IEEE Trans. Commun.*, vol. 38, no. 12, pp. 2174–2183, Dec. 1990.

[17] R. Pasand, J. Nielsen, and A. Sesay, "UWB receiver based on filter bank architecture for suppression of narrowband interfrence noise," in *MILCOM 2004*,

vol. 2, Oct. 2004, pp. 579–585.

[18] T. Linder, H. Zojer, and B. Seger, "Fully analogue LMS adaptive notch filter in BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 31, no. 1, pp. 61–69, Jan. 1996.

[19] F. J. Kub, E. W. Justh, and B. Lippard, "Self-calibrating hybrid analog CMOS co-site interference canceler," in *IEEE Military Communications Conf. Proc.*, vol. 2, Nov. 1999, pp. 1051–1054.

[20] J.-M. Stevenson and E. Sanchez-Sinencio, "An accurate quality factor tuning scheme for IF and high-Q continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1970–1978, Dec. 1998.

[21] H. Gunhee and E. Sanchez-Sinencio, "CMOS transconductance multipliers: a tutorial," *IEEE Trans. Circuits Syst. II*, vol. 45, no. 12, pp. 1550–1563, Dec. 1998.

[22] G. Colli and F. Montecchi, "Low voltage low power CMOS four-quadrant analog multiplier for neural network applications," in *Proc. IEEE Int. Symp. Circuits and Syst*, vol. 1, May 1996, pp. 496–499.

[23] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Low-voltage class AB buffers with quiescent current control," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 915–920, June 1998.

[24] T. W. Fischer and A. I. Karsilayan, "Rail-to-rail amplifier input stage with constant $g_m$ and commonmode elimination,," *Electronics Letters*, vol. 38, no. 24, pp. 1491–1492, Nov. 2002.

[25] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-$g_m$ constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for vlsi cell libraries," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1364–1372, Aug. 2003.

[26] M. Wang, T. L. Mayhugh, S. H. K. Embabi, and E. Sánchez-Sinencio, "Constant-$g_m$ rail-to-rail CMOS op-amp input stage with overlapped transition regions," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 148–156, Feb. 1999.

[27] J. F. Duque-Carrillo, J. M. Carrillo, J. L. Ausin, and E. Sánchez-Sinencio, "Robust and universal constant-$g_m$ circuit technique," *Electronics Letters*, vol. 38, no. 9, pp. 396–397, Apr. 2002.

[28] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "On the common mode rejection ratio in low voltage operational amplifiers with complementary N-P input pairs," *IEEE Trans. Circuits Syst. I*, vol. 44, no. 8, pp. 678–683, Aug. 1997.

[29] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Low-voltage CMOS op-amp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating-gate transistors," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 1, pp. 111–116, Jan. 2001.

[30] E. Sánchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," in *IEE Proceedings-Circuits, Devices and Systems*, vol. 147, no. 1, Feb. 2000, pp. 3–12.

[31] E. A. Klumperink and B. Nauta, "Systematic comparison of HF CMOS transconductors," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 10, pp. 728–741, Oct. 2003.

[32] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst. I*, vol. 31, no. 10, pp. 891–894, Oct. 1984.

[33] G. Ferri and W. Sansen, "A rail-to-rail constant-$g_m$ low-voltage CMOS operational transconductance amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 10, pp. 1563–1567, Oct. 1997.

[34] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, , and J. L. Ausin, "General purpose rail-to-rail input circuit with constant behavior for VLSI cell libraries," in *IEEE Symposium on Circuits and Systems*, vol. 3, May 2002, pp. 607–610.

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