SLIDING-MODE AMPLITUDE CONTROL TECHNIQUES FOR HARMONIC OSCILLATORS

A Thesis

by

CHAD A. MARQUART

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2006

Major Subject: Electrical Engineering

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ABSTRACT

Sliding-Mode Amplitude Control Techniques for Harmonic Oscillators. (May 2006)

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Chair of Advisory Committee: Dr. Takis Zourntos

This thesis investigates both theoretical and implementation-level aspects of switching-feedback control strategies for the development of voltage-controlled oscillators. We use a modified sliding-mode compensation scheme based on various norms of the system state to achieve amplitude control for wide-tuning range oscillators. The proposed controller provides amplitude control at minimal cost in area and power consumption. Verification of our theory is achieved with the physical realization of an amplitude controlled negative-G_m LC oscillator. A wide-tuning range RF ring oscillator is developed and simulated, showing the effectiveness of our methods for high speed oscillators. The resulting ring oscillator produces an amplitude controlled sinusoidal signal operating at frequencies ranging from 170 MHz to 2.1 GHz. Total harmonic distortion is maintained below 0.8% for an oscillation amplitude of 2 V_{pp} over the entire tuning range. Phase noise is measured as -105.6 dBc/Hz at 1.135 GHz with a 1 MHz offset.

ACKNOWLEDGMENTS

I would like to thank my committee chair, Dr. Takis Zourntos, for all of his guidance and support. Thanks also to Dr. Sebastian Magierowski of the University of Calgary for his collaboration during the writing of this thesis.

I would like to extend my gratitude to Dr. Steven Wright for providing access to the lab facilities and equipment used for this research.

Finally, thanks to all of my friends and family for their support and encouragement over the course of this journey.

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CHAPTER I

INTRODUCTION: MODERN WIRELESS COMMUNICATIONS

In 1994 the Defense Advanced Research Projects Agency (DARPA) successfully demonstrated the first large-scale Software Defined Radio (SDR) [1]. The project was officially titled SPEAKeasy and marks a major milestone in the history of modern radio communications. SPEAKeasy Phase-1 successfully demonstrated the ability to change wireless communication schemes (multiband, multichannel, multiwaveform) "on the fly" through software manipulation. In recent years SDR has become a major area of interest in various areas of wireless communications.

Since its implementation in the military, radio communication has played a significant role in military campaigns all over the world. Radio communication can serve as an invaluable strategic tool but also provides opportunities for the compromise of sensitive tactical information. Because of this, militaries have invested much interest in the continued development of reliable, secure communication systems. All over the world military entities use numerous communication systems operating at different bandwidths, carrier frequencies; implementing different modulation and coding schemes.

Recent U.S. military events have demonstrated significant radio incompatibility problems between allies and different branches of military services. Such radio non-interoperability between allies during the allied invasion of Grenada (Oct. 1983) and Operation Desert Storm helped to spawn the creation of the SPEAKeasy project in 1991 [1]. The success of the SPEAKeasy project has since changed the direction of wireless communications in the military.

The journal model is *IEEE Transactions on Automatic Control*.

The Department of Defense (DoD) has committed to the use of the Joint Tactical Radio System (JTRS) for use in future military field operations. "JTRS is a family of common, software-defined, programmable radios that will become our Army's primary tactical radio for mobile communications" [2]. JTRS is being developed to transmit voice, video, and data communications at carrier frequencies ranging from 2 MHz to 2 GHz. Additionally, JTRS will be backwards compatible with many existing military (Legacy) and civilian communication protocols. Table I shows radio waveforms that are considered a priority for JTRS [3].

Table I. Priority Waveforms for JTRS [3]

Name	Frequency Band	Bandwidth	Waveform	Voice/Data Rate
SINCGARS ESIP	30-88 MHz	25 kHz	FM	75 Bps - 16 KBps
HAVE QUICK II	225-400 MHz	25kHz	AM/FM/PSK	75 Bps - 16 KBps
UHF SATCOM MILITARY	225-400 MHz	5 kHz, 25kHz	MIL-STD 181/182/183	75 Bps - 64 KBps
EPLRS	420-450 MHz	3 MHz	SADL	57 KBps, 228 KBps
Soldier Radio and WLAN	1.755-1.850 GHz	13 MHz	IEEE 802.11b/e/g	16 KBps, 1 MBps
Link-16	960-1215 MHz	3 MHz	MIL-STD 6016	2.4 KBps, 16 KBps

Mobile radios intended for use in JTRS are developed around the Software Communication Architecture (SCA) specifications published by the JTRS Joint Program Office (JPO). The SCA document defines necessary interfaces, behavior, and rules to make SDRs SCA compliant and capable for use in the JTRS. Guidelines in the SCA are selected to optimize portability, interoperability, and configurability of the software and hardware of an SDR while allowing flexibility to meet requirements and restrictions for specific operating domains [4]. While the SCA was initially developed for the JTRS it has rapidly gained attention in the commercial community and is widely accepted as the "de facto" standard for the general framework of SDRs.

Wireless communication also plays and essential role to disaster-relief efforts. Recent disasters such as the New York terrorist attacks of September 11, 2001 and Hurricane Katrina have exposed vulnerabilities of current wireless communication

systems to widespread destruction. Both of these disasters demonstrated how the lack of adequate communications can seriously impede relief efforts. Since the widespread destruction of Hurricane Andrew, the U.S. Federal Emergency Management Agency (FEMA) has expressed its desire to obtain a mobile wireless communication system specialized for disaster relief [5].

This mobile communication system specialized for disaster relief should be capable of quickly re-establishing local communication services disrupted by disasters while providing reliable communications between teams involved in the relief effort. During large-scale operations disaster relief teams may be composed of personnel from a number of different federal, state, local, and private sector organizations. Communication amongst these teams poses a problem since different organizations use communication systems that are not necessarily interoperable. A recent report by the 9-11 Commission recognizes "the lack of a federal program for communications interoperability among first responders" and makes radio interoperability of first responders one of its primary recommendations [6].

SDR also has numerous applications for the commercial sector. Throughout the world there exists numerous different commercial communication standards ranging in application from cordless and cellular telephony to Wireless Local Area Networks (WLAN). Currently many cellular phones include multiple chipsets in hardware allowing them to interface with multiple communication standards. Modern cellular phones typically are capable of communications using two or three wireless standards.

First, the phone must be capable of communicating with its original digital cellular network (e.g. GSM, CDMA). For rural areas where a basestation to the digital cellular network is out of range the phone can enter its analog roaming mode of operation (e.g. AMPS) allowing it to communicate with analog basestations that may be in the area. Finally, many modern phones also have a broadband mode of op-

eration allowing users to upload/download data files, pictures, video, etc. Table II provides specifications for some of the most popular cellular standards currently being implemented throughout the world.

Table II. Existing Cellular Communication Standards [7]

	AMPS	CDMA	GSM	W-CDMA
Frequency Range (MHz)	Tx: 824-849 Rx: 869-894	Tx: 824-849 Rx: 869-894 Tx: 1850-1910 Rx: 1930-1990 Tx: 1920-1980 Rx: 2110-2170	Tx: 824-849 Rx: 869-894 Tx: 880-915 Rx: 925-960 Tx: 1710-1785 Rx: 1805-1880 Tx: 1850-1910 Rx: 1930-1990	(IMT-2000) 1920-1980 2110-2170 (PCS 1900) 1850-1910 1930-1990
Multiple Access Method	FDMA	CDMA/FDMA	TDMA/FDMA	CDMA
Channel Spacing	30 kHz	1250 kHz	200 kHz	5 MHz
Modulation Type	FM	QPSK/OQPSK	GMSK	QPSK
Channel Bit Rate	N/A	1.2288 Mb/s	270.833 Kb/s	$\leq$ 384 Kb/s

While these cellular phones are capable of multi-standard communications the number of communication standards available are limited since each standard requires a different chipset. Implementation of SDR technology into these portable phones broadens their capacity to implement different communication standards. Such flexibility opens the door for numerous applications in terms of voice communications and multimedia.

Maintaining communications during intranational and international travel can become cumbersome as different regions implement different communication standards. SDR technology can allow for communications to remain uninterrupted while traveling through such regions. Additionally, it can also allow for the capability to communicate "peer to peer" with other mobile radios that may be using a number of different analog or digital communication schemes.

Another useful application of SDR is the capability to connect to the internet via a WLAN, or a Wireless Metropolitan Area Network (WMAN) that is implementing an IEEE wireless communication standard. The SDR might also be able to communicate

with various remote media devices in a home or office using Bluetooth™ technology. For example a person may wish to find a printer that is available locally to print out a hardcopy of an email recently received. Table III shows specifications for some of the most commonly implemented WLAN standards currently implemented.

Table III. Existing WLAN Standards [7]

	IEEE 802.11b	IEEE 802.11g	Bluetooth™	IEEE 802.15.3a
Frequency Range	2.4-2.4835 GHz	2.4-2.4835 GHz	2.4-2.4835 GHz	3.1-10.6 GHz
Multiple Access Method	CSMA-CSA	CSMA-CSA	TDMA	CSMA-CSA
Channel Spacing	25 MHz	25 MHz	1 MHz	528 MHz
Modulation Type	DBPSK/DQPSK	OFDM	GFSK	Pulse Shaping/OFDM
Data Rate	11 Mb/s	54 Mb/s	1 Mb/s	480 Mb/s

SDR provides a solution to many existing wireless communication issues in both the public and private sector. With the wide-spread implementation of SDR also comes potential for new protocols and concepts to advance the capabilities of wireless communication. A concept that has garnered much attention recently particularly for its potential to utilize frequency spectrum more efficiently is that of Cognitive Radio (CR).

CR was first introduced in an article for IEEE Personal Communications [8]. While current technology is not capable for affordable wide-spread implementation it is expected CR is expected by many to be the next generation of SDR. CR is a "more intelligent" form of SDR that is capable of managing its own resources and parameters by making informed decisions based upon awareness of one or many of the following factors [8]-[10]:

Location: Is the CR located in a geographical region where certain frequency bands are unlicensed? Is the CR located in an area accessible to a WLAN or WMAN?

Environment: Is the CR currently in a particularly noisy environment? Is the CR traveling in a vehicle?

Spectrum: Which frequency bands are currently being used? Can the CR use TDMA or FDMA to transmit/receive within a frequency band without creating interference?

User Behavior: Are there situations where the user prefers higher bandwidth for higher quality voice communications. Does the user desire periodic updates on weather, news, or email?

The autonomous nature of CR provides many opportunities for wireless communication. Probably the greatest opportunity exists for the possibility of adaptive spectrum utilization with CR. Frequency spectrum is considered to be a limited natural resource. This has caused frequency spectrum to be regulated by agencies such as the US Federal Communications Commission (FCC). Currently frequency spectrum is regulated using fixed spectrum allocation in which discrete frequency segments are allocated for specific devices and/or functions. This form of frequency allocation is considered by many to be inefficient since spectrum utilization varies with time and geographic location (e.g. urban areas vs. rural areas).

The recent desire for SDR and multi-standard communications has had a major impact on modern transceiver design. Fig. 1 shows a system-level diagram of a possible SDR architecture. The desire for SDR has encouraged frameworks to include more digital software-based hardware while minimizing analog hardware. Direct conversion based transceivers (zero IF) are being implemented much more frequently in recent years as opposed to the heterodyne based architectures which require conversion to an intermediate frequency (IF) before conversion to baseband (BB). Heterodyne based transceivers architectures being implemented are commonly digitized at the IF band and downconverted digitally to BB to avoid the need for additional mixers.

Advanced digital signal processing techniques are being implemented in transceiver architectures to increase the flexibility of processing both IF and BB signals

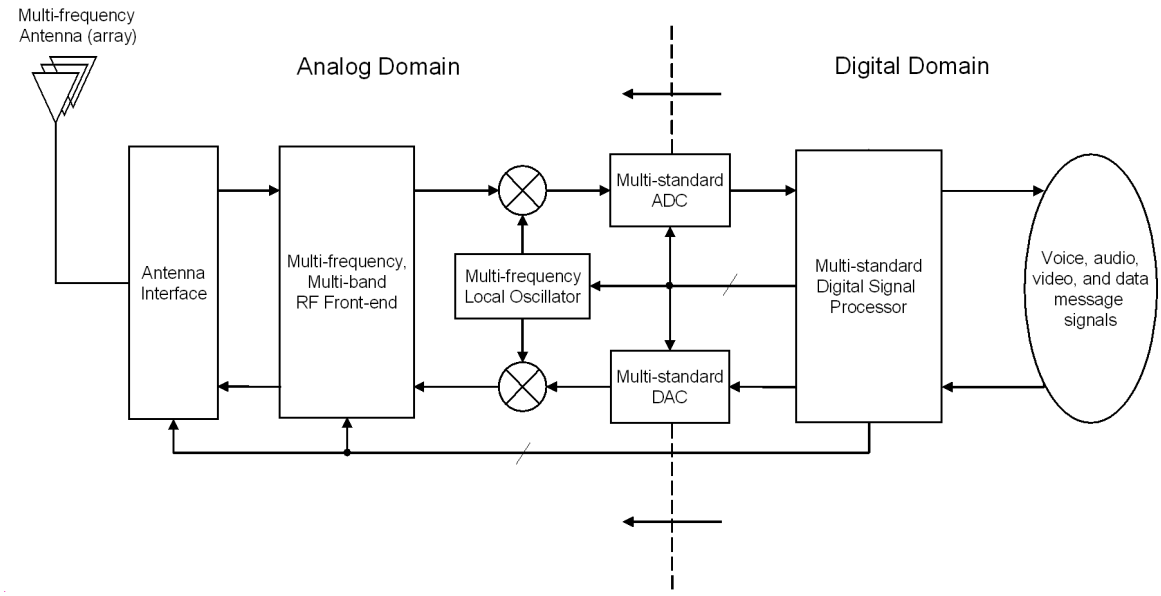


Fig. 1. Generalized View of a SDR Transceiver Architecture

in real-time. While digital technology has come a long way in its evolution it is still not yet practical to digitally process RF signals in real-time. Therefore, it appears that RF transceivers that are completely software-defined are not plausible in the near future. For now, SDRs will continue to require a hardware based RF front-end to operate.

The digital hardware implemented for baseband signal processing in the SDR transceiver is far more complex than the analog hardware implemented in the RF front-end. However, design of analog RF hardware tends to pose the greatest challenge in wireless transceiver design. There are many reasons for this, one of the main difficulties being the numerous tradeoffs encountered during the design of RF microelectronics. Fig. 2 shows a hexagon illustrating some of the important trade-offs that exist in the design of RF microelectronics. [11].

RF microelectronic systems are characterized by several opposable parameters. Changes made to improve a particular parameter in an RF system leads to the degra-

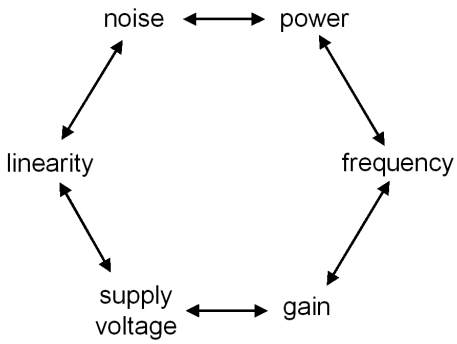


Fig. 2. RF Design Hexagon [11]

dation of other system parameters. Because of this, RF hardware must be customized for its application to optimize performance and meet required minimum specifications. For many modern communication standards such specifications can be very difficult to achieve. Such difficulty is often amplified by the need for RF designers to integrate analog systems using digital based IC technologies. Thus, the recent desire for SDR and multi-standard communications poses many challenges to the design of multi-frequency and multi-bandwidth RF front-ends.

Such challenges are reflected by the amount of research that has recently been reported on the development of RF hardware components suitable for multi-standard communications [12], [13], [14]. This trend has led to the development of programmable Analog to Digital Converters (ADCs), programmable Digital to Analog Converters, Programmable Filters. MEMS also shows promise in improving programmability as well as hardware reconfiguration.

The local oscillator (LO) of wireless transceivers has received much attention due to the desire for generation of a wide range of carrier frequencies. The LO of a RF transceiver generates the carrier frequencies used to modulate and demodulate message signals. The LO is typically implemented with a voltage controlled oscillator in some type of phase-locked loop (PLL) configuration. To increase the number of

operating frequencies of the RF transceiver emphasis has recently been placed upon increasing the tuning frequency range of VCOs.

A. VCO Design Challenges

The following are commonly used metrics to characterize the performance of a VCO. Results provided in Chapter V of this thesis are calculated based on these metrics.

Tuning Range is the range of oscillation frequencies the VCO is capable of operating at relative to its center frequency.

$$TR = 100 \times \left(\frac{f_{max}}{f_c} - 1 \right) [\%] \tag{1.1}$$

where f_c is the center frequency of the VCO and f_{max} is the maximum operating frequency. Typically, a wide tuning range is desired in a VCO to overcome process and temperature variations that may cause the center frequency of the VCO to vary. As mentioned previously, implementation of a VCO with a wide-tuning range can reduce the amount of hardware necessary to realize a multi-standard RF front-end.

Tuning Sensitivity is the rate at which the frequency of oscillation changes with respect to the control voltage at the center frequency.

$$K_{vco} = \frac{d\omega_o}{dV} \left[\frac{\mathrm{V}}{\mathrm{Hz}} \right] \tag{1.2}$$

Typically, a large tuning range is desired for a VCO while a large tuning sensitivity is not. A VCO with a large tuning sensitivity is more capable of converting amplitude noise from its control voltage into phase noise of the output frequency.

Phase Noise is the random fluctuations of the oscillation frequency (and thus phase) in a non-ideal oscillator. Phase noise degrades the signal to noise ratio (SNR) of wireless communications systems. Phase noise can also cause interference to other communication systems operating at neighboring frequencies.

A common method of measuring phase noise is as follows:

$$L(\triangle f) = \frac{P_{SSB}}{P_S} \left[\frac{\text{dBc}}{\text{Hz}}\right] \tag{1.3}$$

where P_S is the spectral power at the oscillation frequency (signal) and P_{SSB} is the spectral power of 1 Hz of bandwidth of a single-sideband offset frequency $\triangle f$ Hz from the carrier.

Harmonic Distortion an ideal harmonic oscillator produces a perfect sinusoid at the oscillation frequency (ω_o). When non-linearities enter the system it causes this sinusoid to become distorted. This distortion creates additional harmonics at different multiples of the fundamental frequency. This additional harmonic content is known as harmonic distortion. Harmonic distortion can be determined from the output power spectrum as follows

$$HD_i = \frac{P_i}{P_s} \left[\frac{\text{dBc}}{\text{Hz}}\right] \tag{1.4}$$

where HD_i is the amount of distortion present at the i^{th} harmonic. P_i is the spectral power of 1 Hz of bandwidth at the i^{th} multiple of the fundamental oscillation frequency and P_s is the spectral power at the fundamental oscillation frequency.

Total harmonic distortion is the sum of the distortion present for all harmonics

greater than the fundamental frequency

$$THD = \sum_{i=1}^{n} \frac{P_i}{P_s} \left[\frac{\text{dBc}}{\text{Hz}}\right] \tag{1.5}$$

another common representation of THD is as a percentage relative to the fundamental frequency

$$THD = 100 \times \sqrt{\sum_{i=1}^{n} \frac{P_i}{P_s}} \ [\%] \tag{1.6}$$

Reduction of harmonic distortion is essential to maximizing the performance of a wireless transceiver. When excessive harmonic distortion is transmitted or received by a wireless transceiver it can lead to significant interference of the message signal. Harmonic distortion can be reduced in a wireless transceiver through filtering and utilizing high quality linear components.

Figure of Merit a figure of merit (FoM) exists that is widely accepted in the RF community to provide a phase noise performance comparison of different offset frequencies and for VCOs operating at different oscillation frequencies.

$$FoM = L_{\triangle f} + 20\log(\tfrac{\triangle f}{f_o}) + 10\log(\tfrac{P_{cons.}}{1 \text{ mW}}) \text{ [dB]} \tag{1.7}$$

The FoM calculates a phase noise metric based upon the VCO oscillation frequency, measured phase noise, phase noise frequency offset, and power consumption.

B. Problem Description

Recently a great deal of research has been devoted towards increasing the tuning range and frequency stability (to improve phase noise) of Variable Frequency Oscillators (VFO). However not much research has devoted towards amplitude stability. For

most VFO topologies the amplitude of oscillation varies with oscillation frequency.

For wide-tuning range VFOs amplitude control techniques become necessary to prevent large deviations in oscillation amplitude over the frequency tuning range [15], [16]. Amplitude of oscillation is important since it can play a significant role in the total harmonic distortion (THD) and overall phase noise performance [16] of the oscillator.

Current techniques for amplitude control are either expensive to implement or cause significant degradation to phase noise performance. Better amplitude control techniques are desired for wide-tuning range VFOs that are relatively cheap to implement and do not severely degrade phase noise performance.

C. Proposed Solution

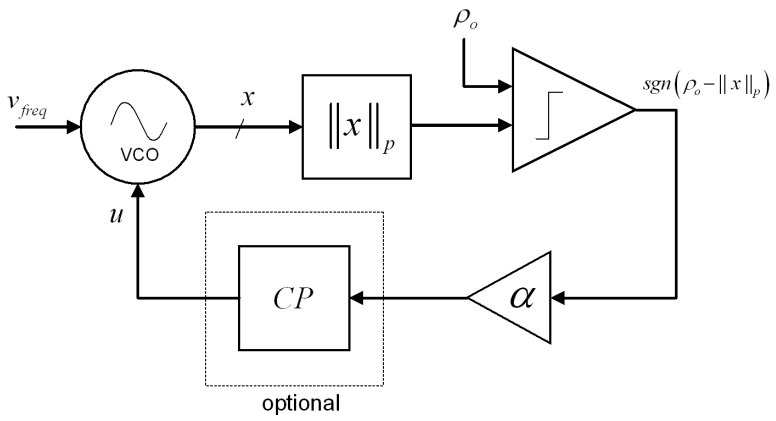


Fig. 3. VFO with Modified Sliding-Mode Amplitude Control

This thesis presents sliding-mode control (SMC) techniques applicable to harmonic oscillators to provide improved amplitude control. Fig. 3 shows the system-level diagram of the proposed SMC. This is a switch-based controller allowing for the potential cost of realization to be relatively low. This SMC can be implemented with sliding-manifolds based on any vector p-norm allowing for a number of different

realizations to be possible. The proposed controller may also implement an optional charge pump at the output of the SMC to reduce chattering.

D. Thesis Organization

The emphasis of this thesis is on the development of amplitude-control techniques for wide-tuning range VCOs. Sliding-mode techniques are proposed to control the amplitude of oscillation.

Chapter II provides background information on periodic oscillatory systems. Two commonly used VCO architectures are characterized and compared. Existing amplitude control techniques are discussed briefly.

Chapter III provides a general description of SMC. Mathematical sliding-mode compensation schemes based on various vector norms are proposed for the VCO architectures discussed in Chapter II. Design challenges of implementing SMC are discussed.

Chapter IV discusses the physical realization of an LC oscillator implementing SMC. This modified sliding-mode amplitude-controlled LC oscillator is designed and realized at the board-level using discrete components. Measurement results of the oscillator are discussed.

Chapter V discusses the physical realization of a modified SMC ring oscillator simulated using 0.18 μm TSMC CMOS technology. Simulation results are discussed and compared with ring oscillators reported recently in literature.

Chapter VI presents concluding remarks for the thesis.

CHAPTER II

VARIABLE FREQUENCY OSCILLATORS

A. Periodic Oscillatory Systems

Periodic oscillatory systems are systems that have a non-constant periodic solution [17]. The phase portrait of such systems contain trajectories with closed periodic orbits. As long as a periodic oscillatory system is not disturbed it will traverse its periodic orbit indefinitely.

1. Poincaré-Bendixson Criterion

The Poincaré-Bendixson criterion is a widely celebrated criterion used to prove the existence of periodic orbits for nonlinear systems of any order n. Fig. 4 shows the

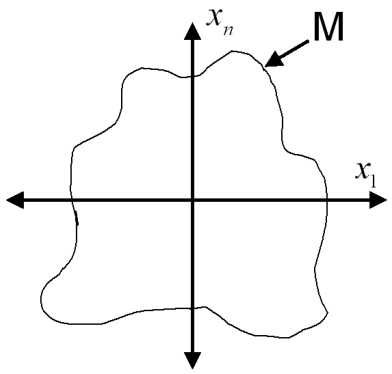


Fig. 4. Bounded Region for Periodic Orbit

state-space view a periodic system

$$\dot{x} = f(x) \tag{2.1}$$

where M is a closed bounded subset of the state-space. According to the Poincaré-Bendixson Criterion for a periodic orbit to exist, such a system must satisfy the

following conditions

1. M contains no equilibrium points, or contains only one equilibrium point such that the Jacobian matrix near this equilibrium has eigenvalues with positive real parts. (Hence, the equilibrium point is either an unstable focus or unstable node) [17].

2. Every trajectory starting in M stays in M for all future time [17].

A purely sinusoidal periodic orbit is capable of being bound by an elliptical region M. However, the shape and size of the closed and bounded region M can take any form as long as it is closed and non-overlapping. It is important to realize that the Poincaré-Bendixson Criterion provides necessary conditions for oscillation but not necessarily the sufficient conditions.

2. Barkhausen Criterion

The Barkhausen Criterion is a commonly used criterion used to provide sufficient conditions for oscillation of linearized systems.

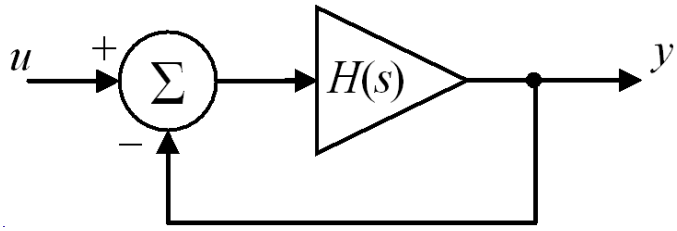


Fig. 5. Linear Feedback System

Fig. 5 shows the system-level diagram of a linear negative-feedback system. According to the Barkhausen criterion in order for this system to be capable of sustained oscillations the following conditions must exist [18]

$$|H(j\omega_o)| \leq 1 \tag{2.2}$$

$$\angle H(j\omega_o) = 180^\circ \tag{2.3}$$

3. Harmonic Oscillatory Systems

The simple harmonic oscillator provides a simple example of the behavior of periodic oscillatory systems. This linear oscillator model is helpful in understanding the behavior of nonlinear oscillatory systems even if they are of a higher degree of order.

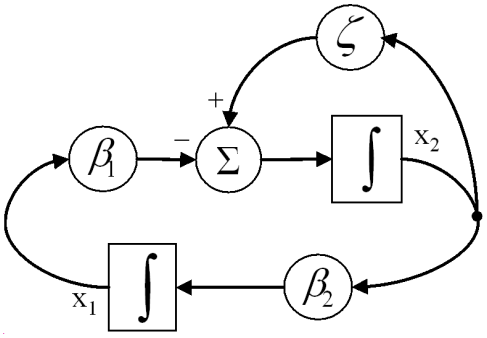


Fig. 6. System-Level View of Harmonic Oscillator

The harmonic oscillator shown in Fig. 6 can be characterized by the following state equations

$$\begin{aligned} \dot{x}_1 &= \beta_2 x_2 \\ \dot{x}_2 &= -\beta_1 x_1 + \zeta x_2 \end{aligned} \tag{2.4}$$

The characteristic eigenvalues for this system are given as

$$\lambda = \frac{\zeta}{2} \pm \frac{1}{2}\sqrt{\zeta^2 - 4\beta_1\beta_2} \tag{2.5}$$

The equilibrium classification of the harmonic oscillator is dependent on the value of ζ. Assuming $\zeta \ll \beta_1\beta_2$, the equilibrium is a stable focus when $\zeta < 0$, an unstable focus when $\zeta > 0$, and a center when $\zeta = 0$. The resulting time domain solution of

this system is given as

$$\begin{aligned} x_1(t) &= r_o e^{\frac{\zeta}{2}t}\cos(\omega_o t + \theta_o) \\ x_2(t) &= r_o e^{\frac{\zeta}{2}t}\sin(\omega_o t + \theta_o) \end{aligned} \tag{2.6}$$

where

$$r_o = \sqrt{x_1^2(0) + x_2^2(0)} \qquad \omega_o = \sqrt{\frac{\zeta^2}{4} - \beta_1\beta_2} \qquad \theta_o = \tan^{-1}(\tfrac{x_2(0)}{x_1(0)})$$

Mathematically, this system is capable of producing an ideal sinusoidal signal. However, there are two fundamental problems with its realization.

First, the system is not structurally stable. Perturbations imposed on the system cause a bifurcation at the origin from a center to either a stable focus or an unstable focus. Such perturbations essentially destroy the periodic orbit of the system. These perturbations are unavoidable since the system is constructed with non-ideal components which contain parasitics and generate noise.

Second, assuming such a system is realizable the amplitude of oscillation is determined by the initial conditions of the system. This means that there are an infinite number of possible periodic solutions for this system based on the initial conditions.

There are many physical realizations for oscillatory systems. For this thesis, two popular and fundamentally different oscillator topologies are selected for experimentation. The oscillator topologies selected are the negative-G_m LC oscillator and the ring oscillator.

B. Variable Frequency Oscillator Architectures

1. In-phase/Quadrature Negative-G_m LC Oscillator

Fig. 7 shows a linear model of a negative-G_m LC oscillator capable of generating both in-phase and quadrature (I/Q) signals. The state equations for this system are given

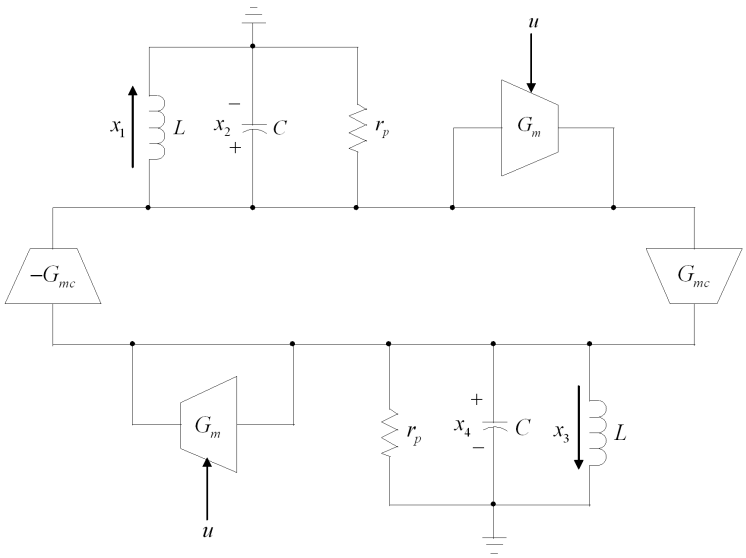


Fig. 7. I/Q Negative-G_m LC Oscillator

as

$$\begin{aligned}
\dot{x_1} &= \tfrac{1}{L}x_2 \\
\dot{x_2} &= -\tfrac{1}{C}x_1 + \tfrac{1}{C}\left[G_m - \tfrac{1}{r_p}\right]x_2 - \tfrac{1}{C}G_{mc}x_4 \\
\dot{x_3} &= \tfrac{1}{L}x_4 \\
\dot{x_4} &= -\tfrac{1}{C}x_3 + \tfrac{1}{C}\left[G_m - \tfrac{1}{r_p}\right]x_4 + \tfrac{1}{C}G_{mc}x_2
\end{aligned} \tag{2.7}$$

where G_m denotes the negative transconductance used to compensate for energy loss due to parasitics and r_p denotes the equivalent parallel resistance of the LC tank. When the oscillator has a large enough Q (typically, $Q > 5$), this resistance can be approximated as

$$r_p \cong \frac{L}{C}\left(\frac{1}{r_L + r_C}\right) \tag{2.8}$$

where r_L and r_C are the series resistance of the inductor (L) and the capacitor (C) respectively.

The eigenvalues for this system are given as

$$\begin{aligned}
\lambda_1 &= -\frac{L^2C\left(G_m-\frac{1}{r_p}\right)}{2L^2C^2} + j\frac{G_{mc}}{C} + \sqrt{\frac{\left(G_m^2-\frac{1}{r_p^2}\right)}{4C^2} + j\frac{G_{mc}\left(G_m-\frac{1}{r_p}\right)}{2} - \frac{G_{mc}^2r_p+G_m}{4r_pC^2} - \frac{1}{LC}} \\
\lambda_2 &= -\frac{L^2C\left(G_m-\frac{1}{r_p}\right)}{2L^2C^2} + j\frac{G_{mc}}{C} - \sqrt{\frac{\left(G_m^2-\frac{1}{r_p^2}\right)}{4C^2} + j\frac{G_{mc}\left(G_m-\frac{1}{r_p}\right)}{2} - \frac{G_{mc}^2r_p+G_m}{4r_pC^2} - \frac{1}{LC}} \\
\lambda_3 &= -\frac{L^2C\left(G_m-\frac{1}{r_p}\right)}{2L^2C^2} - j\frac{G_{mc}}{C} + \sqrt{\frac{\left(G_m^2-\frac{1}{r_p^2}\right)}{4C^2} + j\frac{G_{mc}\left(G_m-\frac{1}{r_p}\right)}{2} - \frac{G_{mc}^2r_p+G_m}{4r_pC^2} - \frac{1}{LC}} \\
\lambda_4 &= -\frac{L^2C\left(G_m-\frac{1}{r_p}\right)}{2L^2C^2} - j\frac{G_{mc}}{C} - \sqrt{\frac{\left(G_m^2-\frac{1}{r_p^2}\right)}{4C^2} + j\frac{G_{mc}\left(G_m-\frac{1}{r_p}\right)}{2} - \frac{G_{mc}^2r_p+G_m}{4r_pC^2} - \frac{1}{LC}}
\end{aligned} \tag{2.9}$$

Based upon the Poincaré-Bendixson Criterion these eigenvalues must be located on the imaginary axis or in the right-half plane (RHP) for a periodic orbit to exist. Analysis of the system eigenvalues shows that in order to accomplish this $G_m \geq \frac{1}{r_p}$. Using (2.8) the following relationship is obtained for the minimum transconductance required for sustained oscillations

$$G_m > \frac{C}{L}(r_L + r_C) \tag{2.10}$$

Notice that when $G_m = \frac{1}{r_p}$ the system resembles a pair of coupled simple harmonic oscillators (2.4). A detailed analysis of the I/Q oscillator is presented in [19]. This paper demonstrates that when this oscillator is designed appropriately the two individual LC tanks become injection-locked. The resulting system behavior can be modeled as a harmonic oscillator with orthogonal voltage states.

Based on the analysis presented in [19] the time domain solution for the I/Q negative-G_m LC oscillator can be approximated as

$$\begin{aligned}
x_1(t) &= \sqrt{\frac{C}{L}}\rho_o e^{(\frac{G_m}{2}-\frac{1}{2r_p})t}\cos(\omega_o t + \phi_o) \\
x_2(t) &= \rho_o e^{(\frac{G_m}{2}-\frac{1}{2r_p})t} - \sin(\omega_o t + \phi_o) \\
x_3(t) &= \sqrt{\frac{C}{L}}\rho_o e^{(\frac{G_m}{2}-\frac{1}{2r_p})t}\sin(\omega_o t + \phi_o) \\
x_4(t) &= \rho_o e^{(\frac{G_m}{2}-\frac{1}{2r_p})t} - \cos(\omega_o t + \phi_o)
\end{aligned} \tag{2.11}$$

where

$$r_o = \sqrt{x_1^2(0) + x_2^2(0) + x_3^2(0) + x_4^2(0)} \qquad \omega_o \cong \sqrt{\frac{1}{LC}} \pm \frac{G_{mc}}{2C}$$

The oscillation frequency of the oscillator becomes offset from the natural oscillation frequency of the matched LC tanks by $\frac{G_{mc}}{2C}$ [19].

As mentioned previously for the simple harmonic oscillator it is not practical to assume that the negative transconductance will cancel out the effective resistance of the tank exactly ($G_m - \frac{1}{r_p} = 0$) for all time. Intrinsic and extrinsic perturbations causes both the negative transconductance and the effective parallel resistance of the oscillator to vary slightly with time. Therefore, conventional LC oscillators are designed to resonate by making sure that the characteristic eigenvalues of the system are located in the RHP.

Forcing the system eigenvalues into the RHP allows the system to resonate, however, mathematically this does not bound the system within a closed region as specified by the Poincaré-Bendixson Criterion [17]. Physical bounds of the voltage and current sources are not included in (3.3). Howver, the amplitude of oscillation for the LC VCO is bound by the maximum available current or voltage (e.g. $2V_{DD}$). Assuming the oscillator is designed to not become clipped by the voltage rails the voltage amplitude of the oscillator after startup is given as

$$V_{swing} = I_{swing} \cdot r_p \tag{2.12}$$

Assuming, $\frac{1}{\sqrt{LC}} \gg \frac{G_{mc}}{2C}$ the frequency of oscillation can be approximated as

$$\omega_o \cong \frac{1}{\sqrt{LC}} \tag{2.13}$$

Substituting this into (2.8) gives

$$r_p = \frac{L^2\omega_o^2}{(r_L + r_C)} \tag{2.14}$$

Notice that r_p is directly proportional to ω_o^2. This relationship demonstrates the strong dependence of oscillation amplitude with oscillation frequency for LC based oscillators. For wide-tuning range VCOs some form of compensation to provide amplitude control becomes necessary.

2. Ring Oscillator

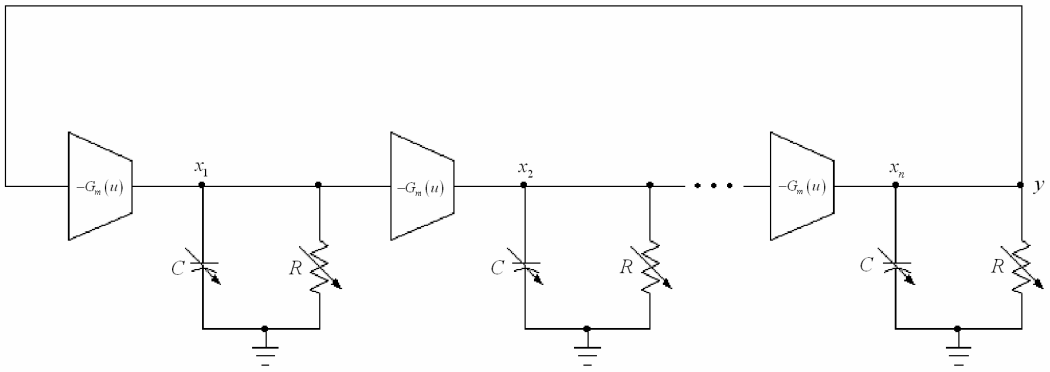


Fig. 8. Ring Oscillator

Fig. 8 shows a linearized n-order ring oscillator. The state-space model of this linearized ring oscillator is

$$\begin{aligned} \dot{x}_1 &= -\tfrac{G_m}{C}x_n - \tfrac{1}{RC}x_1 \\ \dot{x}_2 &= -\tfrac{G_m}{C}x_1 - \tfrac{1}{RC}x_2 \\ &\vdots \\ \dot{x}_n &= -\tfrac{G_m}{C}x_{n-1} - \tfrac{1}{RC}x_n \end{aligned} \tag{2.15}$$

Notice that the ring oscillator can have an unlimited number of delay stages in the feedback loop. Following the conditions specified by the Barkhausen Criterion (2.3) it is necessary to have an odd number of inverting delay stages for the topology shown in Fig. 8. We note that it is possible to implement a ring oscillator with an even number of stages as long as there is at least one non-inverting stage and an odd number of

inverting stages. It has been reported that increasing the number of these delay stages helps to improve overall phase noise at the cost of area and power consumption [20].

The characteristic eigenvalues of the n-order ring oscillator with an odd number of delay stages is given as

$$\begin{aligned}
&\lambda_1 = -\tfrac{G_m R+1}{RC} \\
&\lambda_{2,3} = \left[-(-1)^1 \cos\left(\tfrac{1\pi}{n}\right) \pm j \sin\left(\tfrac{1\pi}{n}\right)\right] \tfrac{G_m}{C} - \tfrac{1}{RC} \\
&\qquad\qquad \vdots \\
&\lambda_{n-1,n} = \left[-(-1)^{\frac{n-1}{2}} \cos\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) \pm j \sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right)\right] \tfrac{G_m}{C} - \tfrac{1}{RC} \\
&\forall\, n = 3, 5, \ldots, \infty
\end{aligned} \tag{2.16}$$

The characteristic eigenvalues of the n-order ring oscillator with an even number of delay stages (1 stage non-inverting, n-1 stages inverting) is given as

$$\begin{aligned}
&\lambda_{1,2} = \left[-(-1)^1 \cos\left(\tfrac{\pi}{n}\right) \pm j \sin\left(\tfrac{\pi}{n}\right)\right] \tfrac{G_m}{C} - \tfrac{1}{RC} \\
&\lambda_{3,4} = \left[-(-1)^2 \cos\left(\tfrac{2\pi}{n}\right) \pm j \sin\left(\tfrac{2\pi}{n}\right)\right] \tfrac{G_m}{C} - \tfrac{1}{RC} \\
&\qquad\qquad \vdots \\
&\lambda_{n-1,n} = \left[-(-1)^{\frac{n-1}{2}} \cos\left(\tfrac{\frac{n-2}{2}\pi}{n}\right) \pm j \sin\left(\tfrac{\frac{n-2}{2}\pi}{n}\right)\right] \tfrac{G_m}{C} - \tfrac{1}{RC} \\
&\forall\, n = 4, 6, \ldots, \infty
\end{aligned} \tag{2.17}$$

As discussed previously harmonic oscillatory systems typically are second-order systems in which the characteristic eigenvalues are complex conjugates. Analysis of the eigenvalues given for the ring oscillator shows that when the loop gain is approximately unity the system contains only one complex conjugate pair in the RHP. All other system eigenvalues are located in the LHP regardless of the order n. The steady-state system response of this system depends only on this RHP complex conjugate pair since the system response attributed to the LHP eigenvalues decays exponentially with time.

We note that if the loop gain becomes much greater than unity additional complex conjugate eigenvalue pairs may be forced into the RHP. When this happens it is possible for the output response become amplitude modulated between the oscillation frequencies of the complex conjugate eigenvalue pairs in the RHP.

Assuming that the loop gain is near unity and the real pole located in the LHP the steady-state time domain solution for the linearized ring oscillator is approximated as

$$\begin{aligned} x_1(t) &= x_1(0)e^{(A-A_o)t}\cos(\omega_o t + 1\left(\tfrac{\pi}{n}+\pi\right)+\phi_o) \\ x_2(t) &= x_2(0)e^{(A-A_o)t}\cos(\omega_o t + 2\left(\tfrac{\pi}{n}+\pi\right)+\phi_o) \\ &\vdots \\ x_n(t) &= x_n(0)e^{(A-A_o)t}\cos(\omega_o t + n\left(\tfrac{\pi}{n}+\pi\right)+\phi_o) \end{aligned} \tag{2.18}$$

where

$$A = G_m R \qquad A_o = \sec\left(\tfrac{\pi}{n}\right) \qquad \omega_o = \tfrac{\tan\left(\frac{\pi}{n}\right)}{RC}$$

For a ring oscillator implemented with identical delay cells the A_o parameter defined in (2.18) provides the minimum gain requirement for each delay cell to meet the unity feedback-loop gain requirement. This gain requirement is dependent on the number of delay stages in the ring.

Assuming that the ring oscillator has sufficient gain and is not experiencing significant clipping the time domain solution produces a sinusoid at the output of each delay cell. Notice that the sinusoids of adjacent delay cells encounter a phase shift of $\frac{\pi}{n}$ which can be attributed to the Barkhausen criterion that the overall phase shift must be equivalent to $180^\circ = \pi$ divided equally between the delay stages in the ring. An additional $180^\circ = \pi$ phase shift occurs through the inversion of each delay cell. The resulting phase shift between adjacent delay cells is then given by

$$\tan^{-1}\left(\frac{x_i}{x_{i+1}}\right) = \frac{\pi}{n} + \pi \tag{2.19}$$

We note that the oscillation frequency is inversely proportional to the the time constant of each delay cell. As mentioned previously the oscillation frequency of the LC oscillator is inversely proportional to the square root of the LC product. Compared to the LC oscillator the ring oscillator is capable of a much wider tuning range for variations in its RC time constant. Unfortunately, this relationship also allows for the ring oscillator to be much more susceptible to phase noise when compared to the bandpass behavior of the LC based VCOs.

C. Existing Amplitude Control Techniques

Many existing VCO architectures implemented have no explicit amplitude control [18]. Amplitude controllers often are not implemented due to additional complexity and likelihood for phase noise degradation. As mentioned previously, mathematically these VCOs are inherently unstable. A physical bound does exist on the maximum voltage swing and current swing that a VCO can achieve. Appropriate selection of the current bias of a VCO determines the maximum current swing that can be achieved. Assuming that transistors do not become clipped by the voltage rails the corresponding voltage swing is given as

$$V_{swing} = I_{swing} \cdot R \tag{2.20}$$

Considering this in the design of the VCO helps to minimize harmonic distortion in the the system and can lead to improved phase noise performance.

Control of the VCO amplitude of oscillation through proper selection of the current bias may be effective for narrowband applications. However, for wide-tuning range VCOs this technique is not as effective since most VCO topologies have an oscillation amplitude which is dependent on the oscillation frequency.

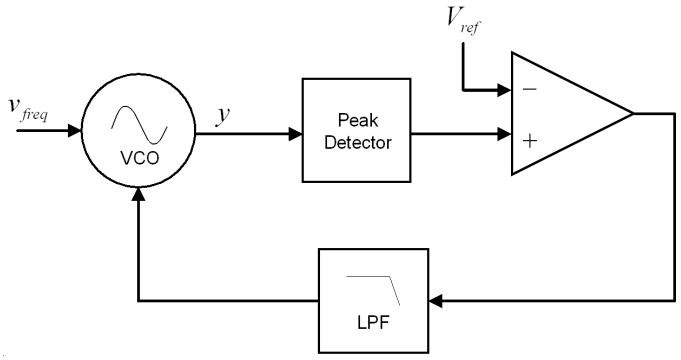


Fig. 9. Conventional Amplitude Gain Controller

Fig. 9 shows a commonly implemented amplitude gain controller (AGC). The controller observes the output response of the VCO and implements a peak detector to estimate the oscillation amplitude. The estimated oscillation amplitude is compared with a reference using a differential error amplifier to adjust the oscillation amplitude accordingly. Typically, a LPF is also implemented to filter out amplitude noise generated by the amplitude controller. This is important since any amplitude noise introduced to the VCO can potentially be transformed into phase noise.

A discretized version of this amplitude control is proposed in [15]. For this feedback control a peak detector is implemented to estimate the oscillation amplitude. A multi-bit voltage comparator compares this amplitude with the reference. The voltage comparator outputs a binary vector to a finite state machine which controls binary weighted array of current sources that supply the VCO. Switching on different combinations of the current sources allows for effective control of the bound on the oscillation amplitude without injecting amplitude noise from the peak detector or an error amplifier.

Peak detectors used for amplitude control of a VCO attempt to estimate the amplitude of oscillation through observation of only one signal vector. Fig. 10 shows the state-space view of how a peak detector based AGC attempts provide this bound.

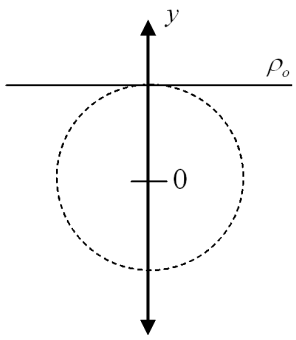


Fig. 10. Bounding Region of 2^{nd} Order AGC

A disadvantage of this control is that decisions are made based on only one state of the system. The peak detector is only accurate for only one instance ($\theta = 2\pi$) in the oscillation period ($\theta = \pi$, 2π for peak detection implementing full-wave rectification). An integrator is implemented to "hold" this peak for the duration of the oscillation period where the peak detector is not valid.

The drawback of this is that if the oscillation amplitude varies the peak detector requires at least one oscillation period ($\frac{1}{2}$ period for full-wave rectification) to detect the variance in amplitude. Wide-tuning range VCOs can further complicate the design of the controller since implementation of a fixed integrator may not be appropriate for all oscillation frequencies in the tuning range. The sliding-mode amplitude control techniques discussed in this thesis provide a more robust method for amplitude control of harmonic oscillators. The following Chapter explains how SMC techniques can significantly improve response time while providing several cost-effective options for realization.

Many topology specific amplitude control techniques also exist for various VCOs. Such techniques include replica feedback biasing for current-controlled ring oscillators to achieve constant voltage swing in spite of variations in current biasing. Many diode based amplitude controllers have also been proposed that limit the oscillation

amplitude to the "turn-on" voltage of the diodes implemented. While each of these control techniques have been shown to be effective at providing amplitude control they have the drawback of being application and topology specific. The sliding-mode amplitude control techniques discussed for this thesis are applicable to any VCO where states are observable and harmonic behavior is desired.

CHAPTER III

PROPOSED MODIFIED SLIDING-MODE COMPENSATION

A. Sliding-Mode Control

Sliding-mode control (SMC) is a type of control in which the dynamics of a nonlinear system are altered through the use of high-speed switching controls. The switching controls alter the system dynamics forcing the system states to traverse a desired sliding manifold.

SMC involves two phases of operation:

1. The system trajectory is forced onto the desired sliding manifold in finite time for any set of initial conditions.

2. The system trajectory is confined to the sliding manifold indefinitely. The resulting behavior of the system confined to the sliding manifold (called the "sliding-mode") is verified to exhibit the desired properties (boundedness, limit cycle behavior, etc.).

The ideal sliding manifold for a sinusoidal oscillator is an ellipse (not necessarily a unit circle). Forcing a periodic oscillatory system to "slide" directly onto an elliptical orbit causes the system to produce a sinusoidal response with minimal harmonic distortion.

Fig. 11 shows the desired sliding-manifold for a harmonic oscillator. The sliding manifold used to confine the system trajectory divides the state space into two regions. The output state of the SMC depends on which of these regions the system is currently operating in:

1. "Growth Region": System state is enclosed by the sliding manifold. SMC

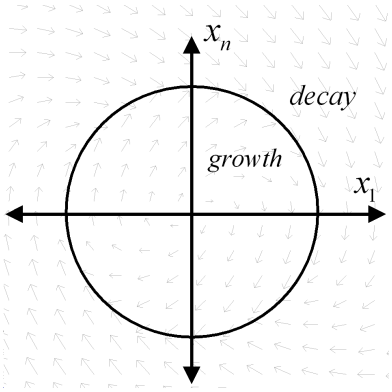
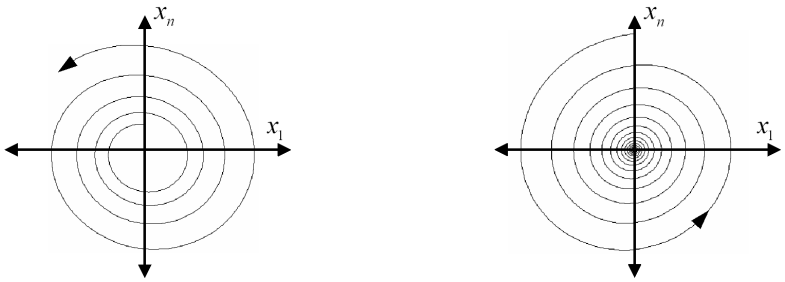


Fig. 11. Sliding Manifold for Harmonic Oscillator

creates an unstable focus at the origin causing the oscillation amplitude to increase exponentially with time.

2. "Decay Region": System state is outside of sliding manifold. SMC creates an stable focus at the origin causing the oscillation amplitude to decrease exponentially with time.



(a) Unstable Focus (b) Stable Focus

Fig. 12. Vector Norms Implemented as Sliding-Manifolds

Toggling the classification of the equilibrium at the origin between a stable focus and an unstable focus causes the amplitude of oscillation to grow exponentially or decay exponentially with time. Fig. 12 shows the trajectory of each of these

equilibrium classifications in state-space. Switching between these equilibrium classifications allows for effective control of the system trajectory. The SMC implements such switching behavior to attract the system trajectory onto a desired sliding manifold. Analysis of the system behavior of the VCO architectures discussed previously exposes opportunities for control of the equilibrium classification at the origin. It will be shown that control of the transconductance of each VCO provides such an opportunity.

Advantages of SMC are that it is robust and relatively cheap to implement since the controller is switch-based. One of the main considerations in the implementation of SMC is the chattering noise generated in the system due to the finite propagation delay of the SMC switches. Excessive chattering is of particular importance to a VCO since it can significantly degrade its phase noise performance.

B. Application to the I/Q Negative-G_m LC Oscillator

Analysis of (3.3) and (2.10) provides insight towards a relationship to toggle the classification of the focus at the origin. It was previously mentioned that when (2.10) is not satisfied the origin becomes either a center or a stable focus. Otherwise if (2.10) is not satisfied the origin is an unstable focus. The SMC utilizes this relationship in order to bifurcate the origin so that the system trajectory is pushed towards a desired sliding-manifold. To accomplish this the transconductance of the negative-G_m LC oscillator described in (3.3) is designed to be

$$G_m(u) = \frac{1}{r_p} + \alpha \operatorname{sgn}(u) \tag{3.1}$$

where α is the switching gain of the SMC and the input u is based upon the sliding manifold used to bound the periodic orbit. To minimize the switching gain of the

SMC a DC component is included to cancel out the equivalent parallel resistance of the LC tank (r_p).

The proposed sliding-mode compensated negative-G_m LC oscillator is given as

$$\begin{aligned}
\dot{x_1} &= \tfrac{1}{L}x_2 \\
\dot{x_2} &= -\tfrac{1}{C}x_1 + \tfrac{\alpha}{C}\,\mathrm{sgn}(\sigma_\infty)x_2 - \tfrac{G_{mc}}{C}x_4 \\
\dot{x_3} &= \tfrac{1}{L}x_4 \\
\dot{x_4} &= -\tfrac{1}{C}x_3 + \tfrac{\alpha}{C}\,\mathrm{sgn}(\sigma_\infty)x_4 + \tfrac{G_{mc}}{C}x_2
\end{aligned} \tag{3.2}$$

The proposed SMC is designed to provide amplitude control of the negative-G_m LC oscillator.

1. Periodic Stability Analysis

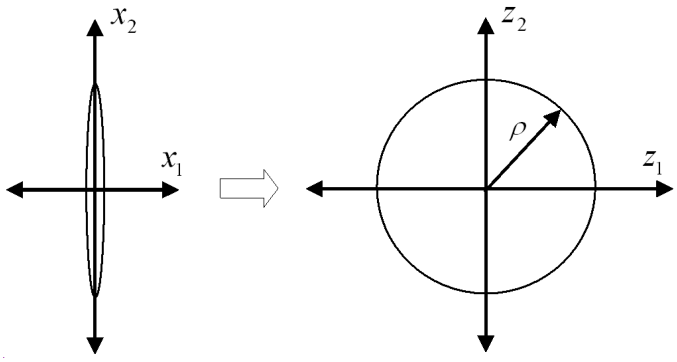


Fig. 13. State-Space Transformation of LC Oscillator

To simplify stability analysis of the Negative-G_m LC Oscillator a system transformation is performed. This system transformation changes the elliptical periodic orbit of each individual LC oscillator to a circular periodic orbit. Fig. 13 illustrates this transformation. In order to normalize both of these states to equivalent units z_1

is transformed based upon the reactance of the LC tank.

$$\begin{aligned} z_1 &= \sqrt{\tfrac{L}{C}}x_1 \\ z_2 &= x_2 \\ z_3 &= \sqrt{\tfrac{L}{C}}x_3 \\ z_4 &= x_2 \end{aligned} \tag{3.3}$$

Giving the following transformed system

$$\begin{aligned} \dot{z_1} &= \tfrac{1}{\sqrt{LC}}z_2 \\ \dot{z_2} &= -\tfrac{1}{\sqrt{LC}}z_1 + \tfrac{\alpha}{C}\operatorname{sgn}(u)z_2 - \tfrac{G_{mc}}{C}z_4 \\ \dot{z_3} &= \tfrac{1}{\sqrt{LC}}z_4 \\ \dot{z_4} &= -\tfrac{1}{\sqrt{LC}}z_3 + \tfrac{\alpha}{C}\operatorname{sgn}(u)z_4 + \tfrac{G_{mc}}{C}z_2 \end{aligned} \tag{3.4}$$

For the SMC to be effective the resulting system should produce a stable limit cycle with an orbit that resembles a unit circle. The radius of the orbit is defined based on the desired amplitude of oscillation ($\rho_o > 0$). To demonstrate this a Euclidean distance function is used to determine the distance that the system state is away from the desired periodic orbit

$$\rho = \sqrt{z_1^2 + z_2^2 + z_3^2 + z_4^2} \tag{3.5}$$

$$\sigma = \rho_o - \rho \tag{3.6}$$

where ρ_o is the desired amplitude of oscillation for the system. Using this distance function a quadratic Lyapunov function candidate is created

$$V = \frac{1}{2}\sigma^2 \tag{3.7}$$

The resulting derivative of the Lyapunov function is determined using the transformed system model given in (3.4).

$$\dot{V} = \sigma\dot{\sigma} = -\frac{1}{2}\left(z_1^2 + z_2^2 + z_3^2 + z_4^2\right)^{-\frac{1}{2}}\left(2z_1\dot{z_1} + 2z_2\dot{z_2} + 2z_3\dot{z_3} + 2z_4\dot{z_4}\right) \tag{3.8}$$

Substitution of (3.5) and (3.4) gives

$$\dot{V} = -\frac{\alpha}{\rho}\sigma\,\mathrm{sgn}(u)(z_2^2 + z_4^2) \tag{3.9}$$

based on this result u is selected to be

$$u = \sigma \tag{3.10}$$

resulting in

$$\dot{V} = -\frac{\alpha}{\rho}|\sigma|(z_2^2 + z_4^2) \tag{3.11}$$

From this result it can be concluded that V is monotonically decreasing for $\sigma \neq 0$, or $z_2 \neq 0$ and $z_4 \neq 0$.

$$\dot{V} < 0, \quad \forall\, x \in R^2\ and\ \sigma \neq 0,\ z_2, z_4 \neq 0 \tag{3.12}$$

Also we note that

$$\dot{V} = 0,\ \text{ if } \quad \sigma = 0,\ \text{ or } \ z_2, z_4 = 0 \tag{3.13}$$

This demonstrates that the distance parameter σ is either decreasing or held constant with time. The only instance where $\sigma \neq 0$ is constant occurs when $z_2, z_4 = 0$. It can be demonstrated that this constant $\sigma \neq 0$ situation only occurs for finite moments in time resulting in no change to the trajectory of the system.

We note that it is impossible for σ to be constant with time and not equal to zero. In other words the condition

$$\sigma \neq 0,\ \ \dot{\sigma} = 0\ \ \forall\, t\ \geq\ 0 \tag{3.14}$$

cannot occur. From (3.4) this condition implies

$$z_2, z_4 = 0 \;\Rightarrow\; \dot{z_2}, \dot{z_4} = 0 \;\Rightarrow\; z_1, z_3 = 0 \;\Rightarrow\; z(t) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \forall\, t \;\geq\; 0$$

Notice that this situation only occurs at the origin. Assuming that the oscillator is not initialized at the origin and that $\rho_o > 0$ it can be concluded that (3.14) can never occur.

Therefore, the distance metric $|\sigma|$ decreases monotonically. This proves that the circular periodic orbit (transformed) with radius ρ_o is attractive. The sliding-mode compensation forces the system towards this orbit for any $\rho > 0$ and any set of initial conditions $x \in R^2 - \{0\}$. When the system is on the desired periodic orbit it never leaves the orbit. Thus an elliptical limit cycle exists for all time.

The only remaining uncertainty of this SMC is the system behavior when the trajectory is located on the sliding manifold. To determine this sliding-mode solution it is assumed that

$$\sigma = 0 \Rightarrow \dot{\sigma} = 0 \tag{3.15}$$

Substitution of (3.6) gives

$$\dot{\rho} = 0 \Rightarrow \frac{1}{2}(z_1^2 + z_2^2 + z_3^2 + z_4^2)^{-\frac{1}{2}}(2z_1\dot{z_1} + 2z_2\dot{z_2} + 2z_3\dot{z_3} + 2z_4\dot{z_4}) = 0 \tag{3.16}$$

This can be simplified since $-\dot{\rho} = 0$

$$z_1\dot{z_1} + z_2\dot{z_2} + z_3\dot{z_3} + z_4\dot{z_4} = 0 \tag{3.17}$$

Substitution of (3.4) gives

$$\begin{aligned} &\tfrac{\alpha}{C}\,\mathrm{sgn}(u)(z_2^2+z_4^2)=0 \\ &\therefore\ z_2, z_4 = 0\ or\ \mathrm{sgn}(u)=0 \end{aligned} \tag{3.18}$$

It was shown previously that

$$\begin{aligned} &z_2, z_4 \neq 0\ \forall\ t\ \geq 0 \\ &\therefore\ \mathrm{sgn}(u)=0 \end{aligned} \tag{3.19}$$

Substitution of this result back into (3.3) gives the sliding-mode solution

$$\begin{aligned} \dot{x_1} &= \tfrac{1}{L}x_2 \\ \dot{x_2} &= -\tfrac{1}{C}x_1 - \tfrac{G_{mc}}{C}x_4 \\ \dot{x_3} &= \tfrac{1}{L}x_4 \\ \dot{x_4} &= -\tfrac{1}{C}x_3 + \tfrac{G_{mc}}{C}x_2 \end{aligned} \tag{3.20}$$

Assuming $G_m(0) = r_p$ the sliding-mode solution resembles a pair of coupled simple harmonic oscillators. We note that the SMC is essentially shutoff when the system is on the sliding manifold allowing for the natural harmonic behavior of the system to only be present. From [21] it can be concluded that the system trajectory approaches the sliding-mode solution when the system is initialized off of the sliding manifold.

C. Application to Ring Oscillator

From the Barkhausen criterion it is known that the open-loop gain of the ring oscillator must be greater than unity for resonation to occur. When this loop gain is less than unity the origin becomes a stable focus causing oscillations to decay exponentially with time. As with the negative-G_m LC oscillator toggling this equilibrium classification at the origin between a stable focus and an unstable focus allows for effective control of the system trajectory. There are numerous methods to control the

open-loop gain of the ring oscillator. The most appropriate method for manipulating the open-loop gain may depend on the topology of the individual delay cells. Overall, manipulating the open-loop gain of the ring through the transconductance of each delay cell is an effective method of control without introducing significant noise into the system. To allow for minimal switching gain the transconductance of each delay cell is selected to have the following control

$$G_m(u) = \frac{\sec\left(\frac{\pi}{n}\right)}{R} - \alpha\,\mathrm{sgn}(u) \tag{3.21}$$

where α is the switching gain of the sliding-mode controller. A_o is a DC component of the sliding-mode control designed to set the open-loop gain to unity. The proposed sliding-mode compensated ring oscillator is given as

$$\begin{aligned}
\dot{x}_1 &= -\tfrac{1}{RC}x_1 - \tfrac{1}{C}\left[\tfrac{\sec(\frac{\pi}{n}}{R} - \alpha\,\mathrm{sgn}(u)\right]x_n \\
\dot{x}_2 &= -\tfrac{1}{RC}x_2 - \tfrac{1}{C}\left[\tfrac{\sec(\frac{\pi}{n})}{R} - \alpha\,\mathrm{sgn}(u)\right]x_1 \\
&\vdots \\
\dot{x}_n &= -\tfrac{1}{RC}x_n - \tfrac{1}{C}\left[\tfrac{\sec(\frac{\pi}{n}}{R} - \alpha\,\mathrm{sgn}(u)\right]x_{n-1}
\end{aligned} \tag{3.22}$$

1. Periodic Stability Analysis

To simplify the analysis of the ring oscillator an equivalence transformation is applied to the original linear model of the ring oscillator given in (2.15).

$$z = Px \tag{3.23}$$

The linearized model is transformed into an algebraically equivalent Modal Form [22] in order to decouple adjacent states from each other and divide the system into disjoint sets. For an odd number of delay stages (n) the P matrix is given as

$$P^{-1} = [\lambda_1, Re(\lambda_2), Im(\lambda_2), \ldots Re(\lambda_{n-1}), Im(\lambda_{n-1})] \tag{3.24}$$

The Modal Form is determined using the characteristic eigenvalues given in (2.16). The modal form for an odd number of delay stages n is

$$\begin{aligned}
\dot{z}_1 &= -\tfrac{1}{RC}[G_m R + 1] z_1 \\
\dot{z}_2 &= \tfrac{1}{RC}\left[-(-1)^1 \cos\left(\tfrac{1\pi}{n}\right) G_m R - 1\right] z_2 + \sin\left(\tfrac{1\pi}{n}\right) z_3 \\
\dot{z}_3 &= -\sin\left(\tfrac{1\pi}{n}\right) z_2 + \tfrac{1}{RC}\left[-(-1)^1 \cos\left(\tfrac{1\pi}{n}\right) G_m R - 1\right] z_3 \\
&\vdots \\
\dot{z}_{n-1} &= \tfrac{1}{RC}\left[-(-1)^{\frac{n-1}{2}} \cos\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) G_m R - 1\right] z_{n-1} + \sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_n \\
\dot{z}_n &= -\sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_{n-1} + \tfrac{1}{RC}\left[-(-1)^{\frac{n-1}{2}} \cos\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) G_m R - 1\right] z_n
\end{aligned} \tag{3.25}$$

The sliding-mode control (3.21) is then substituted into (3.25) giving the following transformed nonlinear system

$$\begin{aligned}
\dot{z}_1 &= -\tfrac{1}{RC}\left[\sec\left(\tfrac{\pi}{n}\right) + 1 - \alpha R \operatorname{sgn}(u)\right] z_1 \\
\dot{z}_2 &= -(-1)^1 \cos\left(\tfrac{1\pi}{n}\right) \tfrac{\alpha}{C} \operatorname{sgn}(u) z_2 + \sin\left(\tfrac{1\pi}{n}\right) z_3 \\
\dot{z}_3 &= -\sin\left(\tfrac{1\pi}{n}\right) z_2 - (-1)^1 \cos\left(\tfrac{1\pi}{n}\right) \tfrac{\alpha}{C} \operatorname{sgn}(u) z_3 \\
&\vdots \\
\dot{z}_{n-1} &= -(-1)^{\frac{n-1}{2}} \tfrac{1}{RC}\left[\tfrac{\nu(n)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R \nu(n) \operatorname{sgn}(u)\right] z_{n-1} + \sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_n \\
\dot{z}_n &= -\sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_{n-1} - (-1)^{\frac{n-1}{2}} \tfrac{1}{RC}\left[\tfrac{\nu(n)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R \nu(n) \operatorname{sgn}(u)\right] z_n
\end{aligned} \tag{3.26}$$

where

$$\nu(n) = \cos\left(\tfrac{\frac{n-1}{2}\pi}{n}\right)$$

Analysis of (3.26) shows that $\dot{z}_1$ is dependent only on z_1. The remaining states of the modal form for this linear odd-ordered ring oscillator contains $\frac{n-1}{2}$ pairs of states that resemble a set of decoupled 2^{nd}-order harmonic oscillators.

Each of these decoupled oscillators is characterized by

$$\begin{aligned}
\dot{z}_i &= -(-1)^i \tfrac{1}{RC}\left[\tfrac{\cos\left(\frac{i\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R\cos\left(\tfrac{i\pi}{n}\right)\operatorname{sgn}(u)\right] z_i + \sin\left(\tfrac{i\pi}{n}\right) z_{i+1} \\
\dot{z}_{i+1} &= -\sin\left(\tfrac{i\pi}{n}\right) z_i - (-1)^i \tfrac{1}{RC}\left[\tfrac{\cos\left(\frac{i\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R\cos\left(\tfrac{i\pi}{n}\right)\operatorname{sgn}(u)\right] z_{i+1} \\
\forall \quad & i = 2, \ldots, \tfrac{n-1}{2} + 1
\end{aligned} \tag{3.27}$$

To demonstrate stability in the sense of Lyapunov multiple Lyapunov candidates are created for each of these autonomous state subsets.

$$V_T = V_1 + V_2 + \ldots + V_{\frac{n-1}{2}+1} \tag{3.28}$$

Each of these Lyapunov candidates excluding V_2 are Globally Asymptotically Stable (GAS) with respect to the origin. This is shown first with candidate V_1 which is defined as

$$V_1 = \frac{1}{2} z_1^2 \tag{3.29}$$

Taking the derivative gives

$$\dot{V}_1 = z_1 \dot{z}_1 = -\left[\frac{1 + \sec\left(\frac{\pi}{n}\right)}{RC} + \frac{\alpha}{C}\operatorname{sgn}(u)\right] z_1^2 \tag{3.30}$$

Thus

$$\dot{V}_1 < 0, \; \forall\, \alpha < \frac{1 + \sec\left(\frac{\pi}{n}\right)}{R} \tag{3.31}$$

Next it is shown that Lyapunov functions $V_3, \ldots, V_{\frac{n-1}{2}-1}$ are also GAS.

$$V_{i-\frac{i}{2}+1} = \frac{1}{2} z_i^2 + \frac{1}{2} z_{i+1}^2, \;\; \forall\, i = 4, 6, \ldots, n-1 \tag{3.32}$$

Taking the derivative gives

$$\dot{V}_{i-\frac{i}{2}+1} = z_i \dot{z}_i + z_{i+1} \dot{z}_{i+1}, \;\; \forall\, i = 4, 6, \ldots, n-1 \tag{3.33}$$

Substitution of (3.26) gives

$$\dot{V}_{i-\frac{i}{2}+1} = \frac{1}{RC}\left\{\frac{\cos\left(\frac{i-\frac{i}{2}\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R\cos\left(\frac{\pi}{n}\right)\mathrm{sgn}(u)\right\}(z_i^2 + z_{i+1}^2) \tag{3.34}$$
$$\forall\, i = 4, 6, \ldots, n-1$$

Since

$$\cos\left(\frac{i-\frac{i}{2}\pi}{n}\right) < \cos\left(\frac{\pi}{n}\right),\ \ \forall\, i = 4, 6, \ldots, n-1 \tag{3.35}$$

Then

$$\dot{V}_{i-\frac{i}{2}+1} < 0,\ \ \forall\, \alpha < \frac{\cos\left(\frac{\pi}{n}\right) - \cos\left(\frac{3\pi}{n}\right)}{R\cos^2\left(\frac{\pi}{n}\right)},\ \ \forall\, i = 4, 6, \ldots, n-1 \tag{3.36}$$

We note that requirements upon the switching gain (α) becomes increasingly difficult to meet as the number of delay stages increases.

It is then shown that each Lyapunov candidate excluding V_2 is GAS with respect to the origin. Since each of these candidates contains disjoint state subsets its can then be concluded that the states themselves are GAS with respect to the origin. This is important because after enough time has passed (T) these states become negligibly small.

$$\begin{aligned} &(\forall\, \epsilon > 0)(\exists T > 0)\ \text{ s.t.} \\ &|z_i(t)| < \epsilon,\ \ \forall\, t \geq T \\ &\forall\, i = 1, 4, 5, \ldots, n \end{aligned} \tag{3.37}$$

This is significant since it shows that $\forall t > T$ the contribution of all system states other than z_2 and z_3 is less than ϵ. Setting ϵ to a negligible value allows for these states to be essentially ignored for the overall stability analysis of the entire system. After enough time has passed the following approximation is valid

$$V_T \cong V_2,\ \ \forall\, t > T \tag{3.38}$$

Since all other Lyapunov candidates are GAS with respect to the origin periodic stability of the SMC is demonstrated based on the remaining Lyapunov candidate V_2. A distance metric with respect to the sliding-manifold is defined as

$$\sigma = \rho_o - \rho \tag{3.39}$$

where

$$\rho = \sqrt{z_2^2 + z_3^2} \tag{3.40}$$

The quadratic Lyapunov candidate V_2 is defined based on this distance metric

$$V_2 = \frac{1}{2}\sigma^2 \tag{3.41}$$

taking the derivative gives

$$\dot{V}_2 = \frac{1}{\rho}\cos\left(\frac{\pi}{n}\right)\sigma\dot{\sigma} = \frac{1}{\rho}\cos\left(\frac{\pi}{n}\right)\sigma(z_2\dot{z_2} + z_3\dot{z_3}) \tag{3.42}$$

Substituting (3.26) gives

$$\dot{V}_2 = \frac{\alpha}{\rho C}\cos\left(\frac{\pi}{n}\right)\sigma\,\mathrm{sgn}(u)(z_2^2 + z_3^2) = \alpha\frac{\rho}{C}\cos\left(\frac{\pi}{n}\right)\sigma\,\mathrm{sgn}(u) \tag{3.43}$$

From this result u is selected to be

$$u = \rho_o - \sqrt{z_1^2 + z_2^2 + \ldots + z_n^2} \cong \sigma,\ \ \forall\, t > T \tag{3.44}$$

which results in

$$\dot{V}_2 = -\alpha\frac{\rho}{C}\cos\left(\frac{\pi}{n}\right)|\sigma|,\ \ \forall\, t > T \tag{3.45}$$

From this it can be concluded that

$$\dot{V}_2 < 0,\ \ \forall\, z \in R^2 \tag{3.46}$$

The distance metric $|\sigma|$ decreases monotonically. This proves that the circular periodic orbit with radius ρ_o is attractive. The sliding-mode compensation forces the system towards this orbit for any $\rho > 0$ and any set of initial conditions $z \in R^n - \{0\}$. When the system is on the desired periodic orbit it never leaves the orbit. Thus, a limit cycle exists for all time. We note that the periodic stability analysis of an even-order ring oscillator shows the same relationship.

To determine the sliding-mode solution of the ring oscillator it is assumed that

$$\sigma = 0 \Rightarrow \dot{\sigma} = 0 \tag{3.47}$$

Substitution of (3.6) gives

$$\dot{\rho} = 0 \Rightarrow \frac{1}{2}(z_1^2 + z_2^2 + \ldots + z_n^2)^{-\frac{1}{2}}(2z_1\dot{z_1} + 2z_2\dot{z_2} + \ldots + 2z_n\dot{z_n}) = 0 \tag{3.48}$$

This can be simplified since $-\dot{\rho} = 0$

$$z_1\dot{z_1} + z_2\dot{z_2} + \ldots + z_n\dot{z_n} = 0 \tag{3.49}$$

Substitution of (3.26) gives

$$\alpha\frac{\rho}{C}\cos\left(\frac{\pi}{n}\right)\mathrm{sgn}(u) = 0, \;\; \forall\, t > T \tag{3.50}$$

Giving the following result

$$\begin{aligned} &\alpha\tfrac{\rho}{C}\cos\left(\tfrac{\pi}{n}\right)\mathrm{sgn}(u) = 0, \; \forall\, t > T \\ &\therefore \; \mathrm{sgn}(u) = 0, \;\; \forall\, t > T \end{aligned} \tag{3.51}$$

Substitution of this back into (3.26) gives the sliding-mode solution

$$\begin{aligned}
\dot{z}_1 &= -\tfrac{1}{RC}[sec\left(\tfrac{\pi}{n}\right)+1]z_1 \\
\dot{z}_2 &= \sin\left(\tfrac{1\pi}{n}\right) z_3 \\
\dot{z}_3 &= -sin\left(\tfrac{1\pi}{n}\right) z_2 \\
&\vdots \\
\dot{z}_{n-1} &= -(-1)^{\frac{n-1}{2}} \tfrac{1}{RC}\left[\frac{\cos\left(\frac{\frac{n-1}{2}\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R\,\mathrm{sgn}(u)\right] z_{n-1} + \sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_n \\
\dot{z}_n &= -\sin\left(\tfrac{\frac{n-1}{2}\pi}{n}\right) z_{n-1} + -(-1)^{\frac{n-1}{2}} \tfrac{1}{RC}\left[\frac{\cos\left(\frac{\frac{n-1}{2}\pi}{n}\right)}{\cos\left(\frac{\pi}{n}\right)} - 1 + \alpha R\,\mathrm{sgn}(u)\right] z_n
\end{aligned} \tag{3.52}$$

Assuming $t > T$ reduces the system to 2^{nd}-order

$$\begin{aligned}
\dot{z}_2 &= \sin\left(\tfrac{\pi}{n}\right) z_3 \\
\dot{z}_3 &= -\sin\left(\tfrac{\pi}{n}\right) z_2
\end{aligned} \tag{3.53}$$

This solution shows that $\forall\, t > T$ when the system is on the sliding manifold it behaves like a simple harmonic oscillator. From [21] it can be concluded that the system trajectory approaches the sliding-mode solution when the system is initialized off of the sliding-manifold.

D. Equivalence of Vector Norms

The desired trajectory of a harmonic oscillator is an elliptical orbit. Implementing a sliding-manifold based on the Euclidean distance (2-Norm) that the system is from the origin provides for optimal system response. This is true since this sliding-manifold follows the same trajectory as the desired response. The 2-norm is defined as

$$\|x\|_2 = \sqrt{\sum_{i=1}^{n} |x_i|^2} \tag{3.54}$$

Unfortunately, implementation of a control based upon the 2-norm requires squaring functions which can be difficult to realize especially at high frequencies. However, it is possible to use other vector p-norms to approximate a 2-norm based sliding manifold. Utilizing non-elliptical sliding manifolds can significantly decrease the cost of implementing the SMC with minimal loss in overall performance.

To illustrate the following distance function is defined based upon any vector p-norm

$$\sigma_p = \rho_o - \|x\|_p \tag{3.55}$$

Assume that for both oscillators discussed previously u is redefined as

$$u = \sigma_p \tag{3.56}$$

Analysis of (3.9) and (3.45) shows that when

$$\text{sgn}(\sigma_2) = \text{sgn}(\sigma_p) \Rightarrow \dot{V} < 0 \tag{3.57}$$

Thus V is monotonically decreasing and a limit cycle exists. Thus, different vector p-norms can be implemented for the SMC while still ensuring periodic stability of the oscillator.

1. Sliding Manifold Based upon 1-Norm

The 1-norm is a non-elliptical vector norm that is commonly used for mathematical systems. Fig. 14 shows the state-space view of the 1-norm for an n-order system. The equation used to calculate the vector 1-norm is given as

$$\|x\|_1 = \sum_{i=1}^{n} |x_i| \tag{3.58}$$

An equivalence relationship exists between the 2-norm and the 1-norm as fol-

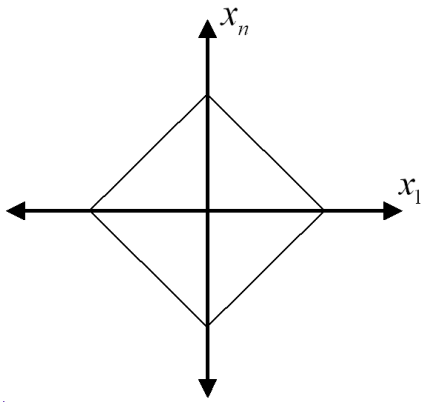


Fig. 14. 1-Norm Based Sliding Manifold

lows [17]

$$\begin{aligned} \|x\|_2 \leq \|x\|_1 \leq \sqrt{n}\|x\|_2 \\ \tfrac{1}{\sqrt{n}}\|x\|_1 \leq \|x\|_2 \leq \|x\|_1 \end{aligned} \tag{3.59}$$

Fig. 15 shows a state-space view of implementing a sliding-manifold based on the 2-norm approximated using the 1-norm. The unshaded region in this figure shows the regions in state-space where $\text{sgn}(\sigma_1) = \text{sgn}(\sigma_2)$. Within the unshaded regions V is monotonically decreasing, thus, the shaded regions are attractive and are the only regions where a limit cycle can exist.

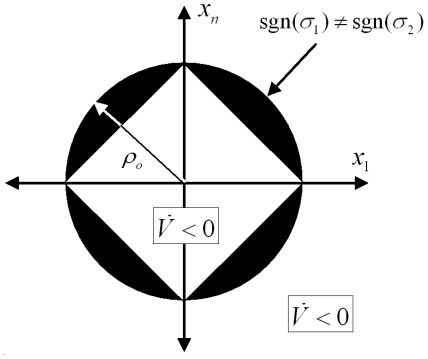


Fig. 15. Equivalence of Control Laws Based on 1-Norm and 2-Norm

From (3.57) it is shown that once the system trajectory enters the shaded region

in Fig. 15 it never leaves that shaded region.

$$\begin{aligned} &(\forall\, \rho_o > 0)(\exists T > 0) \text{ s.t.} \\ &\|x(t)\|_2 < \infty,\ \forall\, t \in [0, T] \\ &\|x(t)\|_2 < \rho_o,\ \forall\, t \geq T \end{aligned} \tag{3.60}$$

Thus once the system is operating within this attractive region it can be assumed that

$$\|x\|_2 \leq \rho_o, \forall t > T \tag{3.61}$$

providing a bound for the maximum error between the distance functions

$$|\|x\|_1 - \|x\|_2| \leq (\sqrt{n} - 1)\rho_o \tag{3.62}$$

We note that implementation of this control law does not necessarily mean that this is the magnitude of chattering to be expected. Notice from Fig. 15 that there are four instances in the oscillation period where each of these sliding-manifolds intersect with the 2-norm based sliding-manifold. Minimizing the switching gain of the SMC minimizes the distance that the system trajectory can stray from its harmonic orbit between each of these intersections. Unfortunately, large switching delays in the SMC can actually increase these distance errors beyond this maximum error as well.

2. Control Law Based upon ∞-Norm

The ∞-norm is a non-elliptical vector norm similar to that of the 1-norm. Fig. 16 shows the state-space view of the 1-norm for an n-order system. The ∞-norm is actually equivalent to the 1-norm rotated 45° about the origin. The ∞-norm is defined as

$$\|x\|_\infty = max(|x_1|, |x_2|, \ldots, |x_n|) \tag{3.63}$$

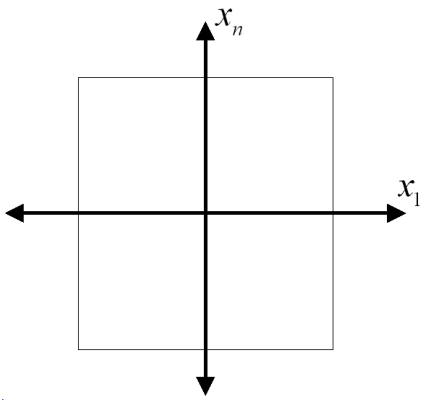


Fig. 16. ∞-Norm Based Sliding Manifold

The ∞-norm also has an equivalence relationship with the 2-norm [17].

$$\begin{aligned} \|x\|_2 \leq \|x\|_\infty \leq \sqrt{n}\|x\|_2 \\ \tfrac{1}{\sqrt{n}}\|x\|_\infty \leq \|x\|_2 \leq \|x\|_\infty \end{aligned} \tag{3.64}$$

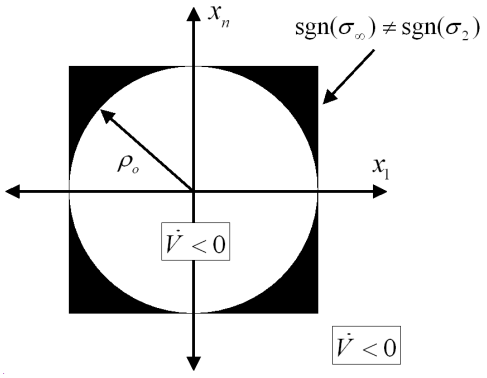


Fig. 17. Equivalence of Control Laws Based on ∞-Norm and 2-Norm

Fig. 17 shows a state-space view of the implementation of a sliding-manifold based on the 2-norm approximated by the ∞-norm. The unshaded region in this figure shows the regions in state-space where $\mathrm{sgn}(\sigma_\infty) = \mathrm{sgn}(\sigma_2)$. Within the unshaded regions V is monotonically decreasing, thus, the shaded regions are attractive and

are the only regions where a limit cycle can exist.

From (3.57) it is shown that once the system trajectory enters the shaded region in Fig. 17 it never leaves that shaded region.

$$\begin{aligned} &(\forall\, \rho_o > 0)(\exists T > 0) \text{ s.t.} \\ &\|x(t)\|_\infty < \infty,\ \forall\, t \in [0, T] \\ &\|x(t)\|_\infty < \rho_o,\ \forall\, t \geq T \end{aligned} \tag{3.65}$$

Thus once the system is operating within this attractive region it can be assumed that

$$\|x\|_\infty \leq \rho_o, \forall t > T \tag{3.66}$$

providing a bound for the maximum error between the distance functions

$$|\|x\|_\infty - \|x\|_2| \leq (\sqrt{n} - 1)\rho_o \tag{3.67}$$

As with the 1-norm this does not necessarily dictate what is expected in terms of chattering. Minimizing the switching gain of the SMC will help to reduce the amount of chattering present in the system.

E. Chattering

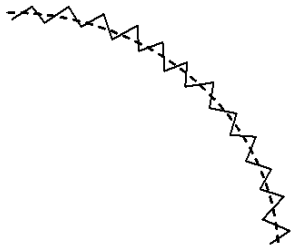


Fig. 18. Chattering about the Sliding Manifold

Propagation delays of the SMC causes the system to oscillate or chatter about

the sliding manifold. Fig. 18 shows an example in states-space of how switching delays cause the system trajectory to oscillate or chatter about the sliding manifold. Chattering becomes prevalent for large switching gains and/or large switching delays. Chattering is an important consideration when implementing SMC of a VCO since variations of amplitude lead to variations of frequency through voltage-dependent device parasitics.

The amplitude of voltage chattering from the sliding-mode control with finite switching delays can be estimated using the time domain solution determined for the harmonic oscillator (2.6). This voltage chatter can be estimated as

$$V_{\varepsilon} = e^{\alpha\tau_d} + 1 - e^{-\alpha\tau_d} \tag{3.68}$$

where τ_d is the propagation delay of the SMC and α is the switching gain of the SMC. This relationship assumes that the VCO is biased to behave similar to a simple harmonic oscillator.

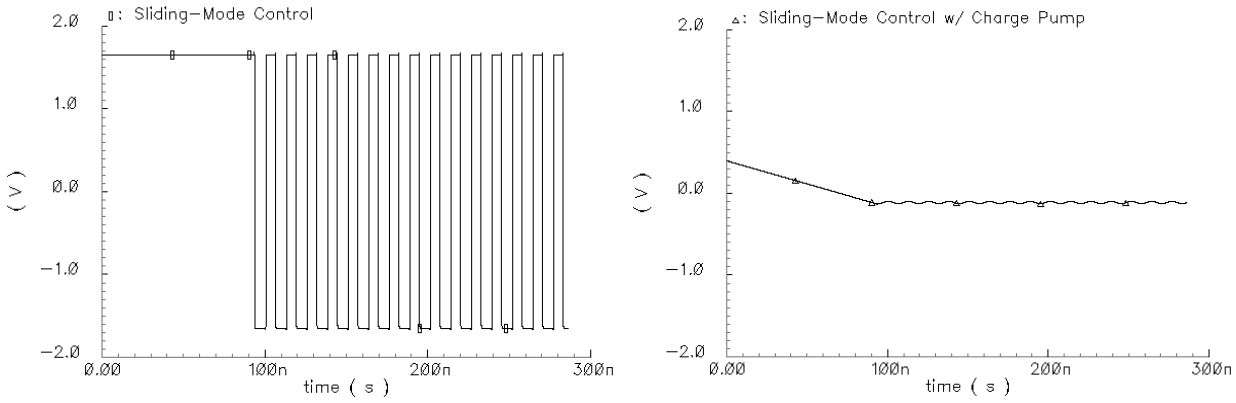
This relationship given by (3.68) does demonstrate that minimizing the switching gain of sliding-mode controller with finite switching delay minimizes the magnitude of chattering. If a harmonic oscillator can be DC biased to so that it has a center at the origin this switching gain can be infinitesimally small. Of course, non-idealities and noise cause the characteristic eigenvalues to vary slightly with time.

For the SMC to be effective the switching gain must be large enough to compensate for these stochastic variations. Process and temperature variations must also be considered when selecting the optimal switching gain. Additionally, (2.8) shows that for LC based VCOs r_p varies with the oscillation frequency. Either the DC component of the SMC must be designed to vary with ω_o to cancel r_p or the switching gain must be further increased to assure a limit cycle will exist

As mentioned in Chapter II the output swing of a VCO is bound either by the

voltage rails or the current sources. To minimize harmonic distortion appropriate selection of current biasing is necessary to assure that the voltage swing never grows large enough to force transistors to become cutoff or saturated. Design of this current bias requires knowledge of the effective output resistance of the VCO for all operating frequencies. Exploitation of this physical bound in VCOs allows for the stability requirements of the SMC to be relaxed.

A charge pump can be implemented to integrate the output of the SMC. This helps to further reduce chattering of the VCO assuming that the current swing is bounded. Fig. 19 compares the output of a SMC switching from rail-to-rail implemented with and without a charge pump at the output. It is important to realize that the charge pump is not used to rigorously prove stabiliy, but to improve (empirically) the chattering behavior present in the SMC. The modified SMC with a charge pump is implemented to provide an incremental control of the maximum current swing of the VCO.



(a) SMC w/o Charge Pump (b) SMC w/ Charge Pump

Fig. 19. Example of Output Response of Sliding-Mode Controller

Assuming appropriate current biasing this modified SMC allows for effective control of the maximum voltage swing of the VCO and thus control of the oscillation

amplitude. The advantage of the charge pump is that it provides a DC bias that automatically compensates for changes in the VCO impedance as it is varied to tune the oscillation frequency. Selection of the charge pump capacitance and current sources results in a trade-off between the amplitude of the switching gain and the response time of the SMC. Fig. 20 shows the system-level diagram of the proposed SMC.

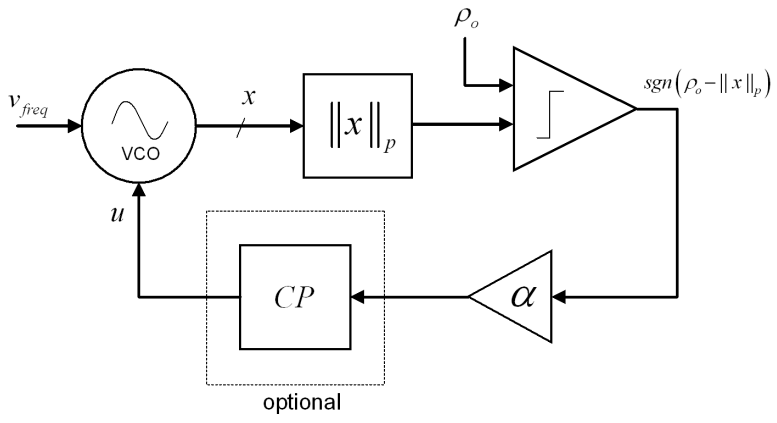


Fig. 20. VCO with Modified Sliding-Mode Amplitude Control

CHAPTER IV

LC OSCILLATOR REALIZATION

A. Circuit Description

To verify its functionality the proposed sliding-mode amplitude control is realized as a physical electrical circuit ("board-level"). The sliding manifold based on the ∞-norm is chosen to approximate the 2-norm since full-wave rectifiers are not necessary for realization. A negative-G_m LC oscillator capable of generating both in-phase and quadrature (I/Q) signals is selected for realization. There are several modulation schemes which require an I/Q oscillator for proper operation making it desirable for multi-standard communications.

$$\begin{aligned}
\dot{x_1} &= \tfrac{1}{L}x_2 \\
\dot{x_2} &= -\tfrac{1}{C}x_1 + \tfrac{1}{C}k\,\mathrm{sgn}(\sigma_\infty)x_2 - \tfrac{1}{C}G_{mc}x_4 \\
\dot{x_3} &= \tfrac{1}{L}x_4 \\
\dot{x_4} &= -\tfrac{1}{C}x_3 + \tfrac{1}{C}k\,\mathrm{sgn}(\sigma_\infty)x_4 + \tfrac{1}{C}G_{mc}x_2
\end{aligned} \tag{4.1}$$

We note that the current-mode states of the LC tanks are not directly observable. An estimator is necessary to observe this state.

$$x_1 = \frac{1}{L}\int x_2 + x_1(0) \tag{4.2}$$

This estimator is realizable but can be expensive to implement.

Another challenge occurs when implementing the SMC since the observed state x_1 must be transformed to equivalent units as x_2 so that the observed trajectory

follows a unit circle rather than an ellipse.

$$z_1 = \sqrt{\frac{L}{C}} x_1 \tag{4.3}$$

This transformation is necessary for the norm based sliding-manifold implemented in the sliding-mode control to be accurate. This transformation can be included in the design of the estimator.

$$z_1 = \sqrt{\frac{1}{LC}} \int x_2 + x_1(0) = \omega_o \int x_2 + x_1(0) \tag{4.4}$$

Notice that the resulting estimator is dependent on the oscillation frequency. This estimator must be tuned with the LC tank to accurately observe x_1. Realization of this oscillator poses many challenges since inaccuracies can lead to errors in the sliding-mode control. Thus, realization of this estimator is not very practical in terms of cost. A common alternative for generating quadrature sinusoids is to couple multiple LC tanks together.

Although, this oscillator is a 4^{th}-order system when the oscillator is operating in steady-state it can be assumed that states are in quadrature. When this is the case it is unnecessary to observe all of the states to implement the SMC. To simplify the realization of the system it is assumed that states that operate 180° out of phase can be considered redundant in the calculation of vector norms. Assuming the oscillator is operating in steady state only one pair of orthogonal states is needed to estimate $\|x\|_\infty$.

Assuming

$$x_2 = -x_3 \Longrightarrow |x_1| = |x_4|$$
$$x_4 = -x_1 \Longrightarrow |x_2| = |x_3|$$

Then

$$max(|x_2|, |x_4|) \equiv \|x\|_\infty \tag{4.5}$$

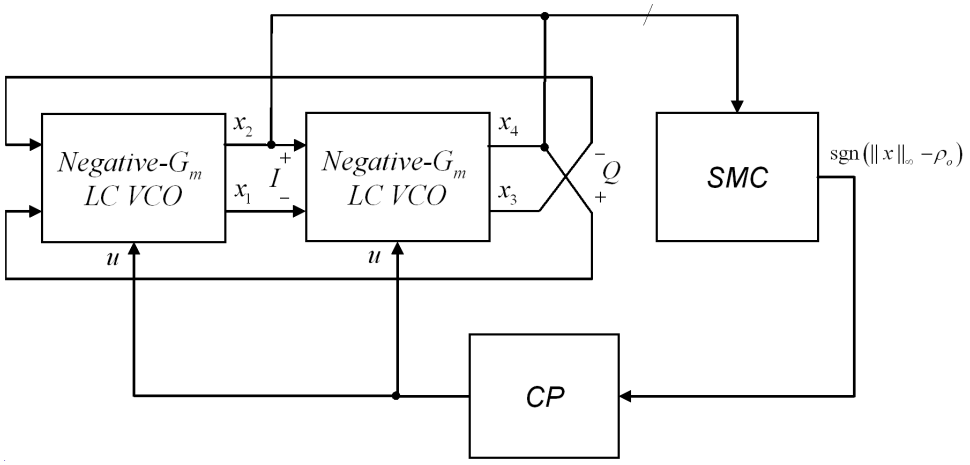


Fig. 21. I/Q LC Oscillator

Fig. 21 shows the system-level diagram of the proposed amplitude-controlled I/Q LC oscillator. The oscillator consists of two negative-G_m LC resonators coupled together in a feedback loop. Assuming the oscillators are matched the feedback network becomes injection locked and the entire system oscillates at an oscillation frequency offset from the oscillation frequency of the individual LC tanks.

We note that this physical realization is intended to demonstrate the functionality of the sliding-mode control. The oscillator realized is not intended for any specific application. The amplitude-controlled oscillator is realized on a protoboard using discrete commercial components. The oscillation frequency is selected to be on the order of 10 MHz due to speed limitations of DIP integrated circuits (IC) and the relatively large parasitics encountered with protoboard realizations.

1. Oscillator Design

Fig. 22 shows the proposed topology for the I/Q LC negative-G_m oscillator. Cross-coupled NMOS transistors are used to provide the negative transconductance necessary to compensate for parasitics present in the individual LC tanks. Transcon-

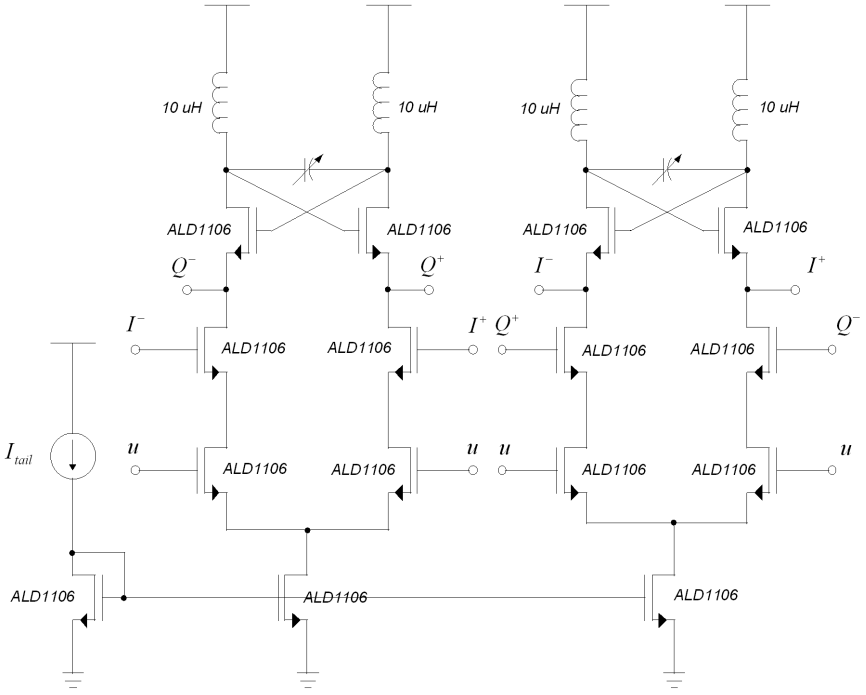


Fig. 22. Proposed Quadrature Negative-G_m LC Oscillator

ductance is controlled via source degeneration by operating NMOS transistors in the triode region. The overall transconductance of the each VCO is inversely proportional to resistance of these transistors operating in triode.

$$G_m(u) = \frac{g_{m_n}}{1 + g_{m_n} R_s(u)} \tag{4.6}$$

The SMC control is configured to provide control of the amplitude of oscillation via incremental control of the DC current of each LC tank. While a DC current bias exists for both VCOs the source degeneration determines the amount of current entering the individual LC tanks at any given time.

Using source degeneration to control the transconductance is much less invasive then varying the current bias of each resonator. Amplitude noise entering the gates of triode transistors is not amplified as much as noise entering active transistors.

Additionally source degeneration improves the linearity of the driving transistors at the cost of gain.

Matched quad NMOS transistor arrays (Analog Linear Devices "ALD1106") are used throughout the physical realization. Each matched array is used to match transistors performing the same function (current source, source degeneration, negative G_m, oscillator coupling). The datasheet for these NMOS arrays provides the NMOS worst case gate capacitance $C_{in} = 3$ pF. The total parasitic tank capacitance is estimated to be around 10 pF including parasitics from solder connections and wiring.

From (2.8) it is apparent that maximizing the inductance of the LC tank minimizes power consumption of the oscillator. Using this relationship it is desired to select a varactor for realization that has a small C_{min}. To demonstrate the effectiveness of this control wide tuning range varactors (2.8-30 pF) are used to achieve an exceptionally large continuous tuning range.

Based on the tank capacitance range the LC tank inductor is selected using the time domain solution defined in (2.11). Using the relationship for the oscillation frequency the tank inductance is selected to be 10 μH to generate a 10 MHz center frequency.

2. Sliding-Mode Controller

As mentioned previously the sliding manifold based on the ∞-norm is to be implemented for the sliding-mode controller. We note that implementation of this sliding-mode control can be performed without the use of rectifiers based on this relationship

$$\begin{aligned} sgn(\|x\|_\infty - \rho_o) \equiv \mathrm{sgn}(x_2 - \rho_o) \text{ OR } \mathrm{sgn}(\rho_\mathrm{o} - \mathrm{x}_2) \\ \text{OR } \mathrm{sgn}(\mathrm{x}_4 - \rho_\mathrm{o}) \text{ OR } \mathrm{sgn}(\rho_\mathrm{o} - \mathrm{x}_4) \end{aligned} \tag{4.7}$$

The drawback of this control law realization is the need for additional voltage comparators which tend to require large amounts of power for high speed operation. Additional power consumption is not of major concern since fabrication of this oscillator is intended only to verify the functionality of the proposed sliding-mode amplitude control.

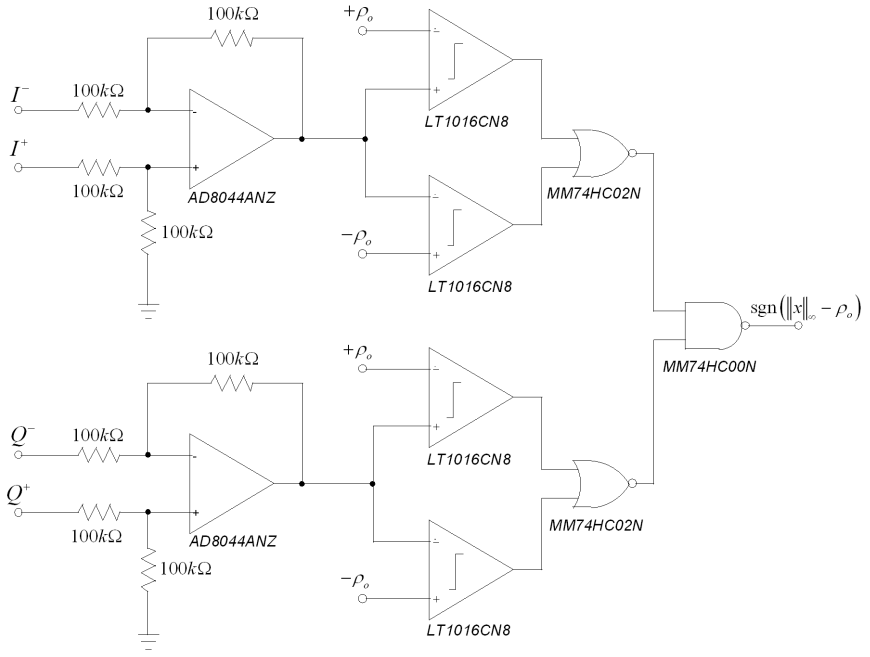


Fig. 23. Proposed Sliding-Mode Amplitude Controller

Fig. 23 shows the proposed topology for the ∞-norm based sliding-mode controller. A voltage subtractor is implemented to observe the single-ended voltage states while simultaneously providing a buffer for the LC tanks. The voltage subtractors are implemented using wide bandwidth (170 MHz) op-amps (Analog Devices "ALD8044ANZ").

To minimize chattering of the SMC it is desired to minimize the propagation delay of the control loop. Additionally, the worst case propagation delay of the SMC must be less than the smallest oscillation period expected from the oscillator.

Assuming that the largest oscillation frequency is 12.5 MHz the propagation delay of the SMC should significantly less than $t_p \ll 80$ ns.

Voltage comparators (Linear Technologies "LT1016") with a worst case propagation delay of $t_p \leq 15$ ns are selected for implementation in the SMC. These comparators are accurate and interface directly to TTL/CMOS logic. These comparators are also power hungry consuming 28 mA to 40 mA per comparator. Four of these voltage comparators are implemented in the SMC.

The output of the voltage comparators are "OR"ed together to establish the rectangular sliding-manifold. Based on Demorgan's Law a four input OR logic gate is realized using two high-speed ($t_p < 15$ ns) CMOS NOR logic gates (Fairchild Semiconductor "MM74HC02") and one high-speed ($t_p < 15$ ns) CMOS NAND logic gate (Fairchild Semiconductor "MM74HC00").

3. Charge Pump

A charge pump is implemented at the output of the SMC to minimize chattering of the SMC and filter amplitude noise from entering the oscillator. Fig. 24 shows the proposed topology for the charge pump. This topology is modified from the topology proposed in [23]. This charge pump is resistant clock-feedthrough implementing varactors on the current mirror gates and buffering the charge pump switches from the output.

Matched transistors arrays (Advanced Linear Devices NMOS: "ALD1106", PMOS: "ALD1107") are implemented to physically realize the charge pump. To improve matching between the current mirrors resistors are implemented in the branches that do not contain switching transistors. The resistor values are selected to match the typical "ON"-resistance of the switching transistors used in the mirrored branch.

Selection of the current biases and charge pump capacitor normally depends

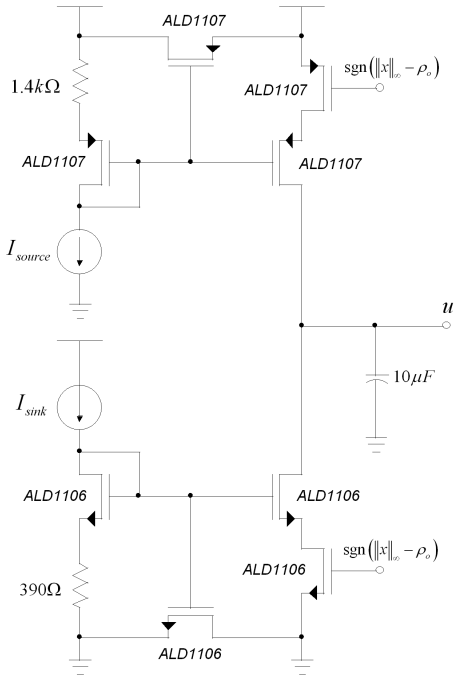


Fig. 24. Proposed Charge Pump for LC Oscillator

on the desired lock-time of the VCO implemented in a PLL. Since this oscillator is not intended to work in a PLL the capacitor is chosen to be significantly large ($C_{CP} = 10$ μF) to achieve minimal chattering and noise.

B. Measurement Results

Fig. 25 shows a photograph of the physical realization of the sliding-mode amplitude controlled I/Q LC oscillator. The realization consumes the majority of a 100 mm $\times$ 160 mm protoboard. The majority of this area is consumed by the matched transistors arrays used to realize the charge pump and the individual negative-G_m LC resonators. The Tektronix 1012 oscilloscope is used for time domain measurements. The Hewlett Packard HP 4395A spectrum analyzer is used for all frequency spectrum measurements. Fig 26 shows a photograph of the I/Q LC oscillator undergoing

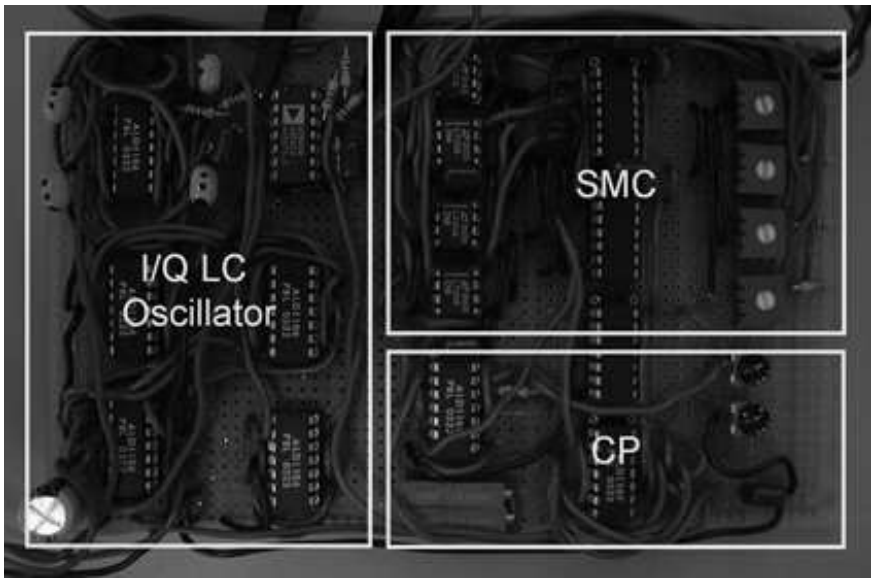


Fig. 25. Protoboard Realization of Amplitude-Controlled I/Q *LC* Oscillator

measurement.

The I/Q *LC* oscillator realized has an oscillation frequency spanning

$$5.8 \text{ MHz} \leq \text{f}_\text{o} \leq 9.4 \text{ MHz}$$

where the tuning range is determined as

$$TR = 23.7\%$$

The center frequency of the oscillator is 7.6 MHz.

We note that the operating frequencies measured are about 3 MHz less than the intended design. This can be attributed to the large parasitics encountered from the wires and punch through connections of the protoboard realization.

Although matched transistor arrays are utilized mis-match of the passive components can be expected between the individual *LC* oscillators. To compensate for this mis-match tuning of the current bias is necessary to achieve the desired phase shift of 90°.

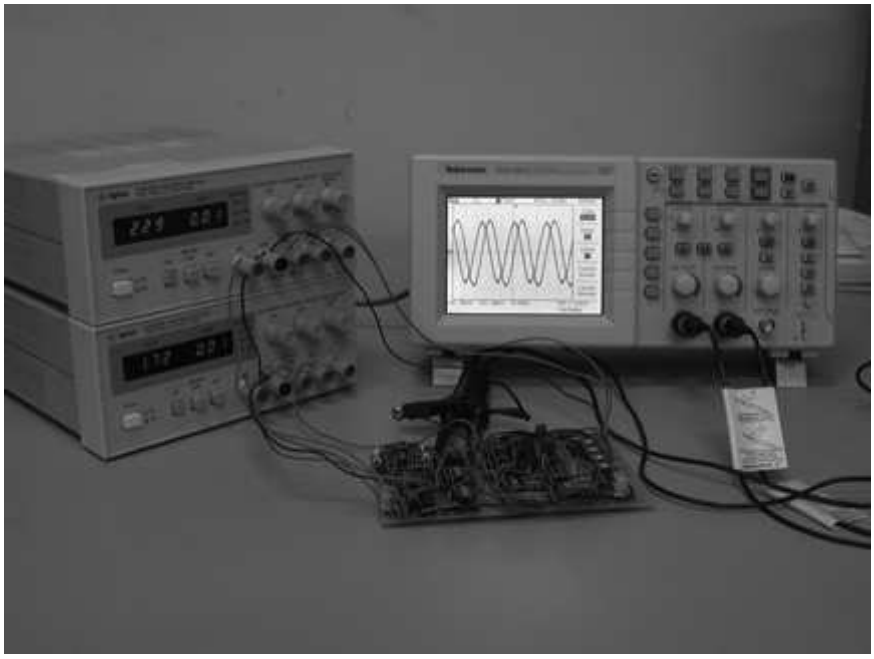
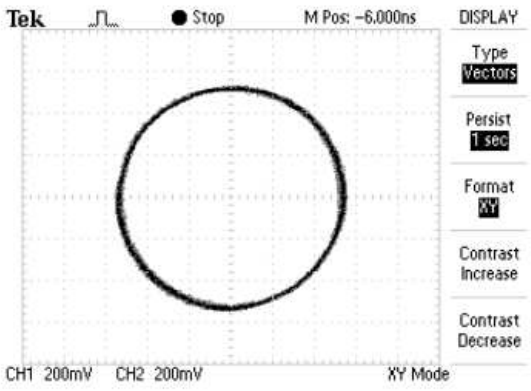
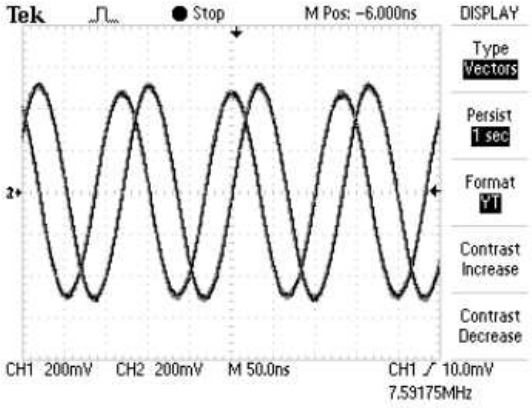


Fig. 26. Photograph of I/Q *LC* Oscillator



(a) State-space Plot



(b) Time Domain Plot

Fig. 27. Output Response of Amplitude Controlled *LC* Oscillator

Fig. 27 shows time domain plots and state-space plots of the oscillator operating at center frequency with the SMC set to $\rho_o = 1$ V. Fig. B shows the state-space plot of the in-phase and quadrature voltage of the I/Q oscillator. Notice that the trajectory of these states follows a periodic orbit that closely resembles that of a unit circle. The oscillator follows this trajectory indefinitely for all frequencies in the tuning range as long as the desired amplitude of oscillation can be achieved given the amount of current biasing the individual tanks.

Experiments were performed on the oscillator with the SMC disabled. A constant DC bias is used to replace the input of the SMC. As expected experimental results show that without the SMC implemented the amplitude of oscillation varies significantly as the frequency of oscillation is varied. These results helps to verify that a limit cycle is indeed established by the SMC.

Fig. B shows the time domain plot of the I/Q oscillator operating at center frequency with oscillation amplitude of 1 V_{pp}. As expected the waveforms of the voltage states exhibit sinusoidal behavior at an oscillation amplitude of 1 V_{pp}. As with the state-space plot of the oscillator the time domain shows that the sinusoids are 90° out of phase. Overall, results show that the SMC I/Q *LC* oscillator behaves as predicted from the theoretical analysis of Chapter III.

THD measurements are calculated based upon analysis of the first 10 harmonics of one of the voltage states of the oscillator. Fig. 28 shows the resulting THD analysis of the I/Q oscillator for different oscillation amplitudes. As expected the THD does increase with the amplitude of oscillation. The THD is around 1% for oscillation amplitudes less than 2 V_{pp}. Overall, the amplitude-controlled oscillator exhibits excellent performance in terms of harmonic distortion for all oscillation amplitudes.

Fig. 29 shows the single sideband (SSB) power spectrum analysis of the I/Q *LC* oscillator. The phase noise relative to the carrier is determined based on this

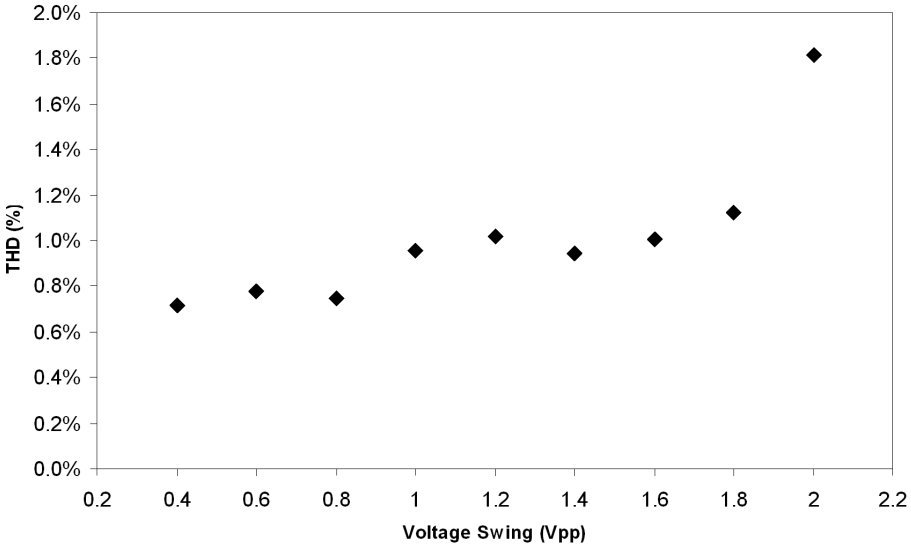


Fig. 28. Harmonic Analysis of *LC* Oscillator

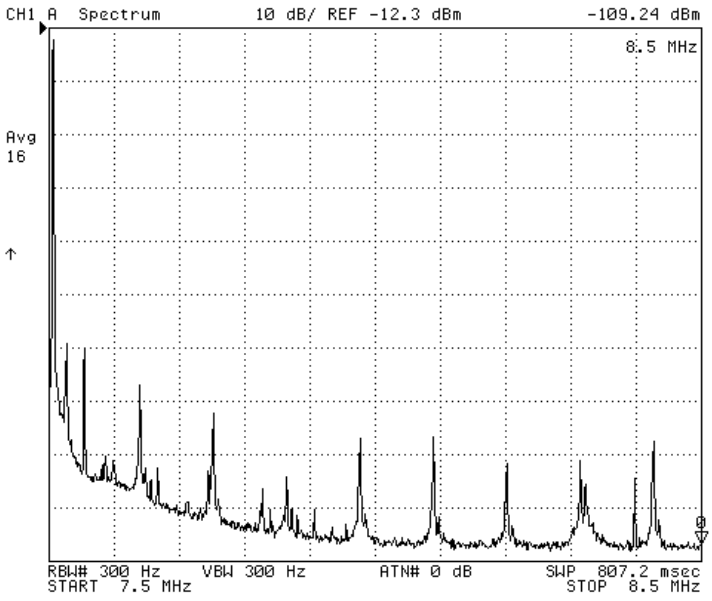


Fig. 29. Measured Phase Noise of *LC* Oscillator

figure. Table IV shows phase noise measurements taken from this figure at commonly used frequency offsets. The phase noise performance of the fabricated *LC* oscillator in general is poor compared with recently reported *LC* QVCOs fabricated on-chip [19], [24], [25]. We emphasize that the goal of this circuit realization is too verify the effectiveness of the amplitude control provided by the SMC. The oscillator is not intended to achieve excellent phase noise performance. Degraded phase noise performance compared with IC realizations is expected due to the large parasitics introduced with the protoboard realization.

Table IV. Phase Noise Analysis of I/Q Oscillator

Freq. Offset	Phase Noise
10 kHz	-53 dBc/Hz
20 kHz	-61 dBc/Hz
50 kHz	-73 dBc/Hz
100 kHz	-82 dBc/Hz
200 kHz	-86 dBc/Hz
500 kHz	-94 dBc/Hz
1 MHz	-95 dBc/Hz

Notice that the sideband contains several spurious tones at multiple frequency offsets from the carrier frequency. Analysis of the phase noise of the oscillator without the implementation of SMC produces similar spurious tones. These additional tones originate from effects inherent to the I/Q topology not necessarily from the SMC.

Fig. 30 shows a comparison of different phase noise measurements taken of the *LC* oscillator operating at center frequency. Phase noise measurements are taken for the oscillator operating with the proposed SMC (with and without the CP). Phase noise measurements are taken for the oscillator operating at center frequency without the

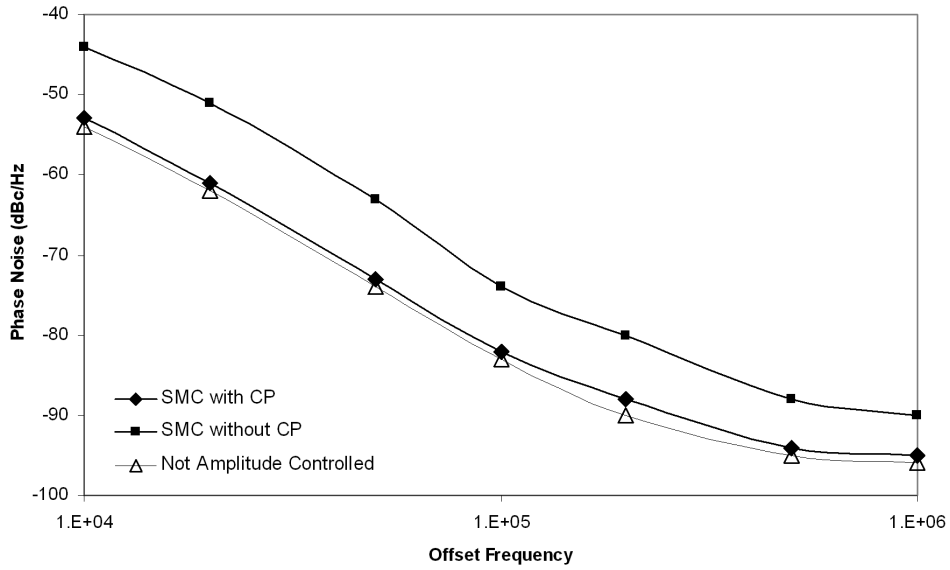


Fig. 30. Phase Noise Comparisons of *LC* Oscillator

proposed SMC. These phase noise measurements were obtained by powering-down the SMC and applying a DC voltage (V_{DD})to the source degeneration transistors operating in triode.

Comparing phase noise plots with SMC and without shows that although the oscillator does not exhibit excellent phase noise performance the SMC causes minimal additional phase noise degradation (1-2 dB). Analysis of the phase noise performance of SMC without the CP shows how chattering of the SMC can severely degrade phase noise performance of the oscillator. For applications with large switching delays in the SMC the charge pump is necessary minimize degradation of phase noise performance due to chattering

CHAPTER V

RING OSCILLATOR REALIZATION

A. Circuit Description

The ring oscillator was selected for integrated circuit realization to demonstrate the effectiveness of this amplitude control for high frequency oscillators over an extremely wide tuning range. The ring oscillator is selected to have three delay stages since the increased power consumption of additional delay cells does not justify the improved phase noise performance [20].

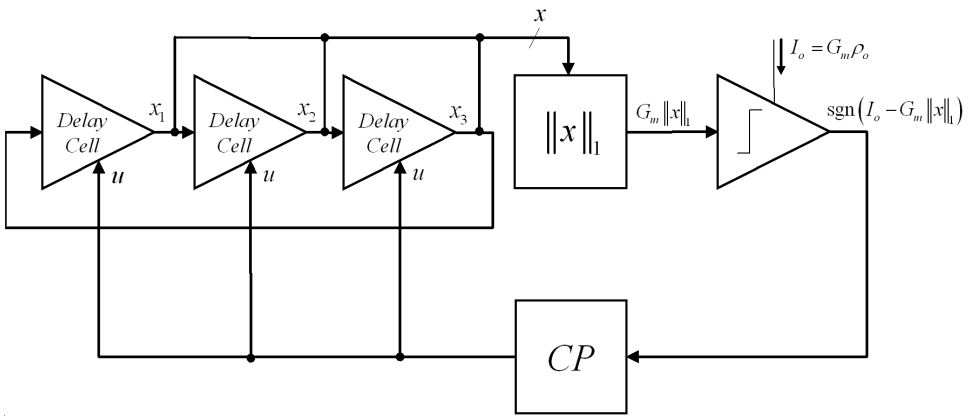


Fig. 31. Proposed Amplitude-Controlled 3-Ring Oscillator

To minimize power consumption a sliding manifold based on the 1-norm is selected for implementation. The realization of the 1-norm only requires one comparator whereas known practical realizations of the ∞-norm sliding manifold requires at least one comparator for each delay cell. The drawback of the realization of the 1-norm is that it requires full-wave rectification as well as a summation circuit.

Fig. 31 shows the proposed topology of the three ring oscillator with sliding-mode compensation. The ring oscillator is designed and simulated based upon TSMC

0.18 μm CMOS technology. Technology files were obtained from the MOSIS website (www.mosis.com) and used for SPECTRE and RFSPECTRE simulations.

1. Delay Cell

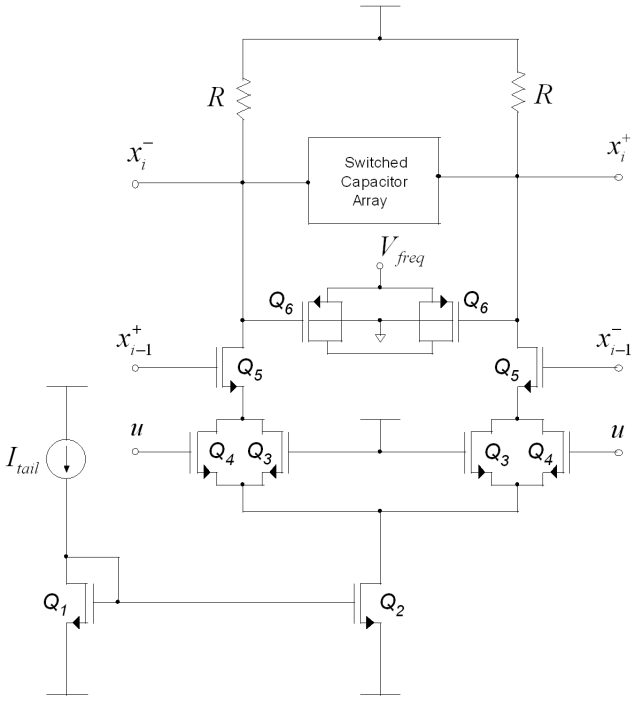


Fig. 32. Proposed Delay Cell for Ring VCO

Fig. 32 shows the proposed topology for each delay cell of the three-ring VCO. A differential topology is selected to minimize common-mode noise. This particular topology was selected to maximize tuning range and linearity while limiting the resulting tuning sensitivity. Utilizing passive resistors for loading instead of active transistors enhances linearity while reducing parasitics and transconductance (flicker) noise which can degrade phase noise performance.

The resistor value was selected to be large enough to minimize the transconductance necessary for oscillation while allowing the maximum desired oscillation

frequency to be achievable. The relationship between oscillation frequency and the time constant of each delay cell is provided in (2.18).

$$f_{osc_{max}} = \frac{\tan\left(\frac{\pi}{3}\right)}{2\pi RC} = 2 \text{ GHz}$$

Estimating parasitics from NMOS transistors to be in the neighborhood of 100 fF gives $R \approx 1.4$ kΩ. Using this resistor value the capacitor array and driving transistors can be designed.

Controlling the frequency of oscillation with a band-switched binary-weighted capacitor discretizes the tuning range into distinct frequency bands. This allows for wide-tuning range with reduced overall continuous tuning sensitivity. The maximum capacitance desired for the array is determined by the minimum oscillation frequency desired for the VCO.

$$f_{osc_{min}} = \frac{\tan\left(\frac{\pi}{3}\right)}{2\pi RC} = 200 \text{ MHz}$$

Given that $R = 1.4$ kΩ gives $C_{max} \approx 1$ pF. When all of the capacitors are activated in the capacitor array the total capacitance should be greater than 1 pF. We note that tuning sensitivity can be reduced with additional capacitor stages in the array. Each stage also contributes additional parasitics that reduces the maximum oscillation frequency and also degrades phase noise. The capacitor array was selected to have four stages to optimize this tradeoff.

Fig. 33 shows the topology used for the binary weighted capacitor array. The switching control scheme used is based on the topology proposed in [26]. This topology efficiently utilizes the entire voltage range available to minimize "on-resistance" while maximizing isolation of the NMOS based switches implemented.

The resulting capacitors for the array must increment by the amount given as:

$$\Delta C = \frac{1 \text{ pF} - 0.1 \text{ pF}}{2^4} = 56 \text{ fF}$$

this incremental amount is increased to $\Delta C = 65$ fF to compensate for process and temperature variations.

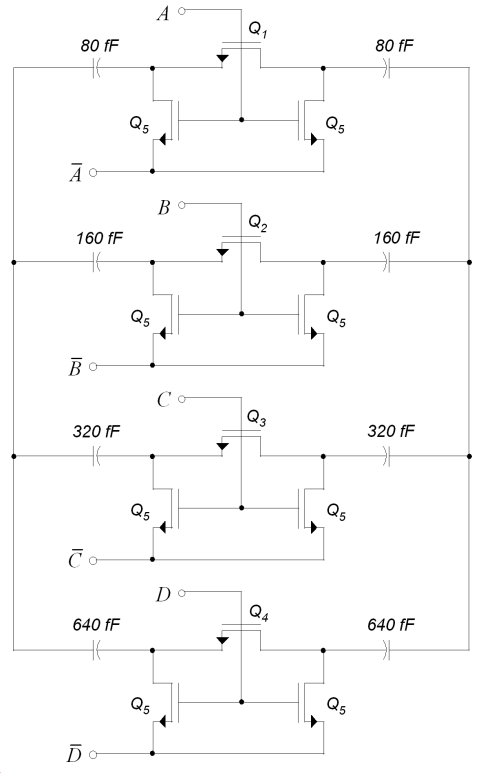


Fig. 33. Band-switched Capacitor Array

A PMOS inversion-mode varactor is used for continuous frequency tuning while a switched capacitor array is implemented to increase tuning range through band-switching while maintaining a limited tuning sensitivity. The PMOS varactor is designed so that the overall capacitance tuning range is approximately 80 fF to exceed the incremental capacitance of the capacitor array. Table V shows the resulting CMOS transistor sizes used for the capacitor array.

The tail current of the delay cell is selected to minimize DC voltage offset at the output of each delay cell.

$$I_{tail} = 2\frac{V_{DD}}{R} = 2\frac{1.65 \text{ V}}{1.4 \text{ k}\Omega} = 2.4 \text{ mA}$$

Table V. Transistor Sizing of Capacitor Array

Q	$\frac{W}{L}$	W (μm)	L (μm)
1	20	4	0.2
2	20	4	0.2
3	30	6	0.2
4	40	8	0.2
5	1.5	0.3	0.2

The driving transistors are desired to be minimal to reduce phase noise degradation. The transconductance of these transistors must be large enough to to meet minimum gain requirements for resonation as specified previously in (2.18).

$$G_m \geq \frac{sec(\frac{\pi}{3})}{R} = 1.43 \ \frac{\text{mA}}{\text{V}}$$

The transconductance of the individual NMOS drivers are selected as $g_{m_n} = 2.5 \ \frac{\text{mA}}{\text{V}}$ to provide enough headroom for control via source degeneration as well as to compensate for process and temperature variations.

Source degeneration with NMOS transistors operating in the triode region provide the point of access for control of the transconductance of each delay cell. The sliding-mode based control varies the resistance of the source degeneration transistors to incrementally control the overall transconductance of the delay cell.

$$G_m(u) = \frac{g_{m_n}}{1 + g_{m_n} R_s(u)} \tag{5.1}$$

The source degeneration resistance must become large enough to allow the VCO to be dampened by the sliding-mode control.

$$R_s(u)_{max} \geq \frac{R}{sec\left(\frac{\pi}{n}\right)} - \frac{1}{g_{m_n}} = 300 \ \Omega$$

Proper sizing of the triode transistors is necessary to assure this maximum resistance

can be reached. A DC biased (V_{DD}) triode region NMOS transistor is designed to be lightly larger than this to bound this source degeneration resistance.

$$r_{ds_{triode}} = \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}(V_{GS} - V_T)\right]} \tag{5.2}$$

The controlled triode region NMOS transistors are designed iteratively to minimize chattering while providing the desired tuning range of oscillation amplitudes.

Finally, the current source of the delay cell is designed to based on the desired tail current (I_{tail} = 2.4 mA). The current source is designed to have a saturation voltage ($V_{ds_{sat}}$ = 200 mV). Additionally, the channel length is increased to increase the output resistance of the current source to improve power source supply rejection (PSRR) and common-mode noise rejection (CMRR). Table VI shows the resulting CMOS transistor sizes used for the delay cell.

Table VI. Transistor Sizing of Delay Cell

Q	$\frac{W}{L}$	W (μm)	L (μm)
1	25	16	0.6
2	250	160	0.6
3	16.67	5	0.3
4	13.33	4	0.3
5	26.67	8	0.3
6	2	4	2

2. 1-Norm Detector

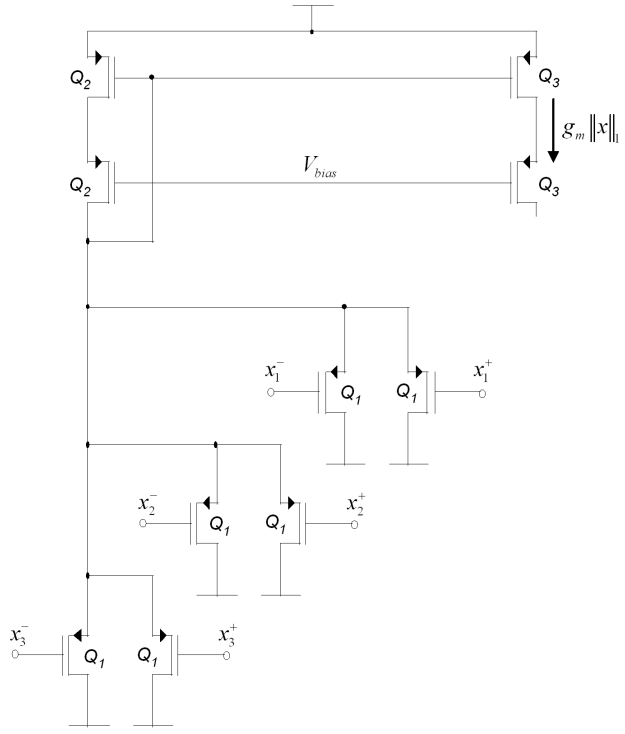


Fig. 34. Proposed 1-Norm Detector for Ring Oscillator

Fig. 34 shows the proposed topology for the 1-norm detector implemented as the sliding manifold. This topology exploits the differential topology of the VCO to rectify the individual phases of the system states. Source followers biased near the the cutoff region are used to produce a current-mode half-wave rectified signal for each differential phase of each state.

Summing the half-wave rectified current signals at a single node produces a current-mode estimate of the 1-norm of the VCO. This technique for achieving full-wave rectification is simple and fast, however, it has the disadvantage of allowing common-mode noise to enter the control loop. The charge pump implemented at the controller output helps to compensate for high frequency common-mode noise that

enters the control loop.

Maximizing speed while maintaining accuracy is the primary goal for the components in the sliding-mode control loop. The driving transistors of the source followers are minimized to maximize the speed of the 1-norm detector. The current mirror is biased so that the driving transistors are nearly cutoff when the output voltage of each corresponding delay cell is near 0 V. Table VII shows the resulting CMOS transistor sizes used for the 1-norm detector.

Table VII. Transistor Sizing of 1-Norm Detector

Q	$\frac{W}{L}$	W (μm)	L (μm)
1	2	0.6	0.3
2	2.5	1	0.4
3	2.5	1	0.4

3. Current Comparator

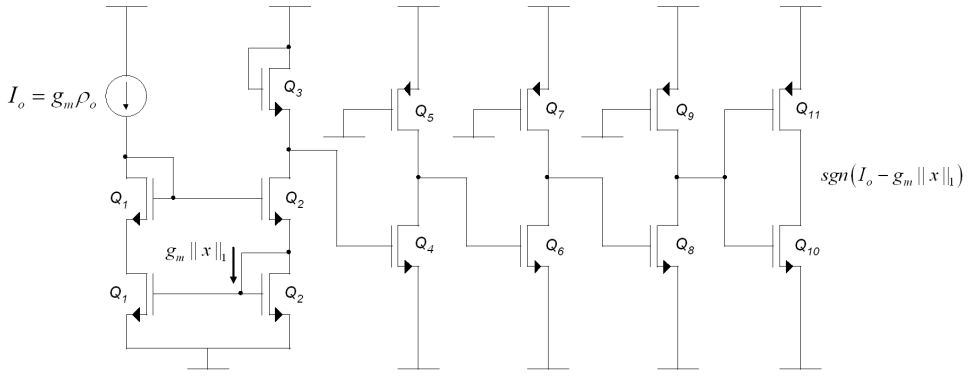


Fig. 35. Proposed Current Comparator for Ring Oscillator

The current comparator implemented for the controller is shown in Fig. 35. This topology was selected due to its large open loop gain and small propagation delay

(< 500 ps). The current comparator proposed is modified from the topology proposed in [27].

This comparator implements a Wilson current mirror to output the current difference between the current reference (I_{ref}) and the output of the 1-norm detector. Several low-gain inversion stages are used to increase the accuracy of the current comparator without contributing significant RC time constants that slow-down its operation. A high gain digital inverter is included at the output to boost the gain of the comparator assuring rail-to-rail operation.

Transistors sizes for the current comparator are designed primarily to maximize speed of operation and minimize DC offset. Minimal sizes are used whenever possible in the comparator design. Table VIII shows the resulting CMOS transistor sizes used for the current comparator.

Table VIII. Transistor Sizing of Current Comparator

Q	$\frac{W}{L}$	W (μm)	L (μm)
1	2.5	1	0.4
2	2.5	1	0.4
3	0.3	0.6	2
4	2	0.6	0.3
5	1.5	0.6	0.4
6	2	0.6	0.3
7	1.625	0.65	0.4
8	2	0.6	0.3
9	1.5	0.6	0.4
10	7.5	1.5	0.2
11	3	0.4	0.2

4. Charge Pump

The proposed topology for the charge pump is shown in Fig. 36. This topology is selected due to its fast switching speed and resistance to clock feed-through [23]. Notice that the cascode current mirrors provide a buffer between the charge pump capacitor and the CMOS switches. CMOS varactors are used to further reduce charge leakage from the CMOS switches onto the gate voltage of the current mirror. Table IX shows the resulting CMOS transistor sizes used for the charge pump.

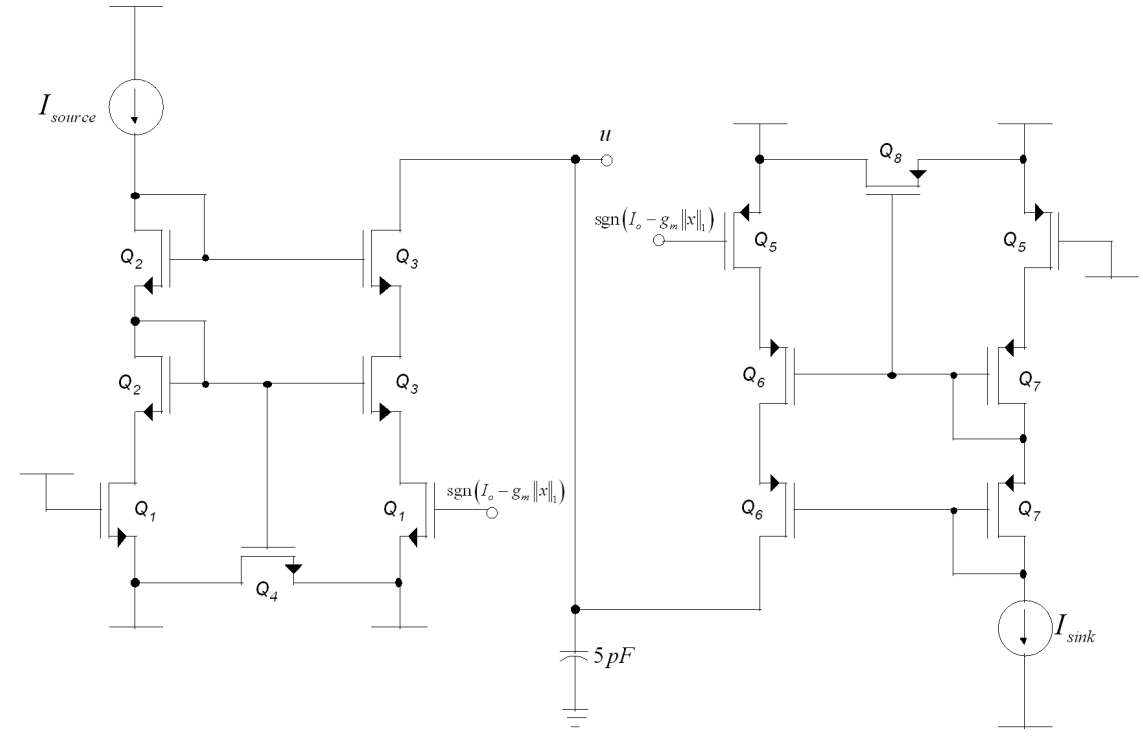


Fig. 36. Proposed Charge Pump for Ring Oscillator

To reduce chattering of the VCO the charge/discharge rate of the charge pump is minimized. The charge pump capacitor is selected to be 5 pf so that it is significantly larger than parasitics of the transistors but does not consume a large amount of area. The charge/discharge current of the charge pump is selected to be $I_{source} = I_{sink} =$

Table IX. Transistor Sizing of Charge Pump

Q	$\frac{W}{L}$	W (μm)	L (μm)
1	2	0.4	0.2
2	2	0.6	0.3
3	2	0.6	0.3
4	1	2	2
5	5	1.0	0.2
6	5	1.5	0.3
7	5	1.5	0.3
8	1	2	2

1 μA. We note that selection of these parameters determines the overall response time of the amplitude control. The desired response time depends on the PLL being used to lock the phase of the VCO.

B. Simulation Results

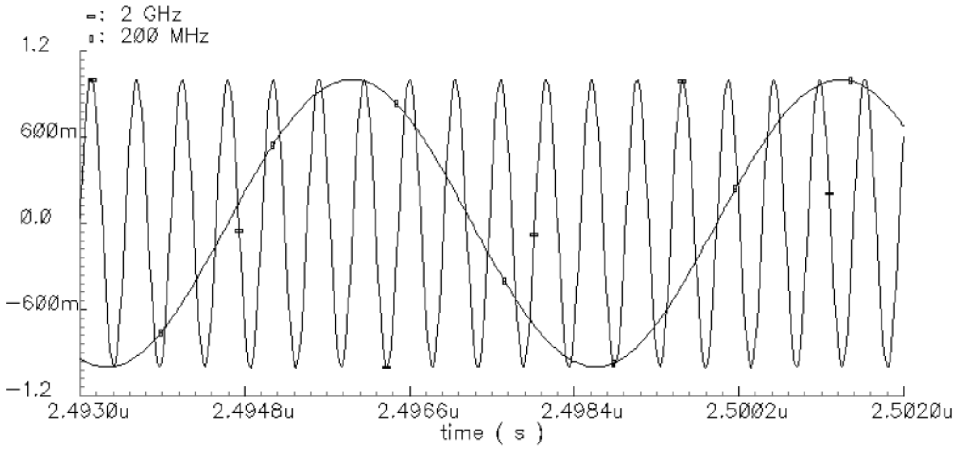


Fig. 37. Transient Analysis of Ring Oscillator

Transient analysis of the ring oscillator shows that the VCO produces a linear sinusoidal output for a large range oscillation frequencies. Fig. 37 shows two plots of the state response of one delay cell in the ring oscillator operating at 200 MHz and at 2 GHz.

Simulations show that the amplitude controller maintains the oscillation amplitude near 1 $V_p p$ for all oscillation frequencies in the tuning range. The maximum variance in amplitude for the frequency tuning range is 54 mV. This variance can be attributed to the finite gain present in both the 1-norm detector and the current comparator. This finite gain creates a dead-zone in the SMC which effectively widens the sliding manifold. Widening of the sliding manifold allows for the size of the periodic orbit to vary slightly while still being confined to the sliding manifold.

Fig. 38 shows the tuning range of the ring oscillator vs. tuning voltage for each possible band-switched mode of operation. The 3-ring oscillator realized can operate at oscillation frequencies ranging over a decade span

$$170 \text{ MHz} \leq f_o \leq 2.1 \text{ GHz}$$

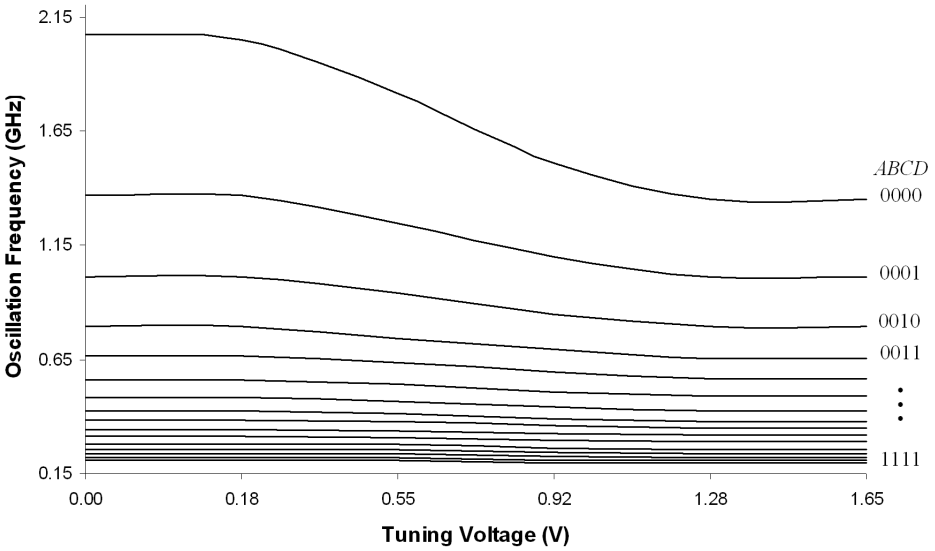


Fig. 38. Tuning-Range Analysis of Ring Oscillator

giving a resulting tuning range of

$$TR = 185\%$$

The center frequency of the ring oscillator is $f_c = 1.135$ GHz. The frequency tuning sensitivity varies depending on the frequency bands activated in the band-switched capacitor array. The tuning sensitivity around the center frequency is

$$K_{vco} \cong 400 \ \frac{\text{MHz}}{\text{V}}$$

As larger capacitors are implemented in the array the effect that the varactor has on the oscillation frequency becomes significantly weaker. The tuning sensitivity at the lower oscillation frequencies is much smaller than the upper oscillation frequencies.

Fig. 39 shows the THD analysis of the ring oscillator. Simulations show that the proposed amplitude-controlled ring oscillator exhibits excellent linearity. THD remains under 1% for oscillation amplitudes less than 2 V_{pp}. As the oscillation amplitude increases the THD increases exponentially as transistors begin to operate less

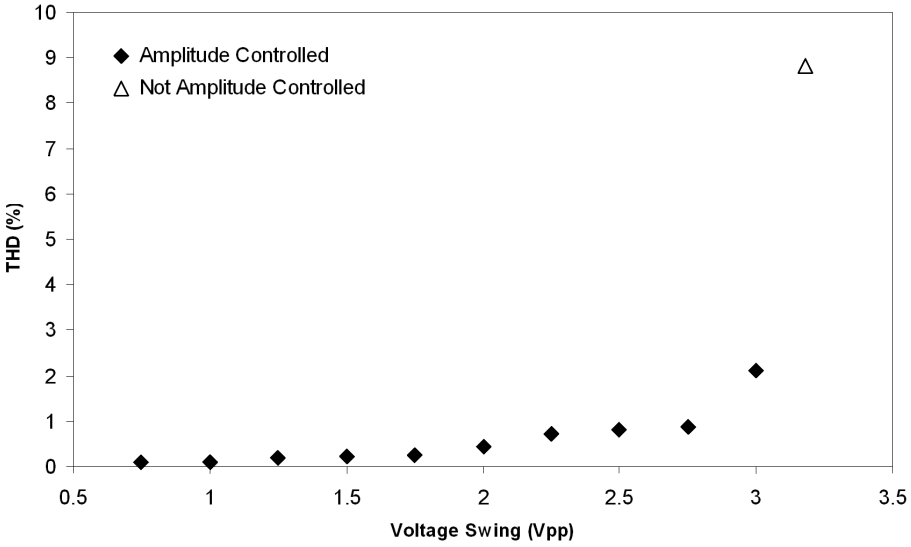


Fig. 39. Harmonic Distortion Analysis of Ring Oscillator

in the active region of operation.

The THD performance is also shown for when the SMC is removed from the ring. Notice that when the ring oscillator is operating rail-to-rail the THD is near 9%. We note that this particular ring oscillator is not designed to not become overly saturated. Many other VCO topologies reported are designed intentionally to become heavily saturated in an attempt to improve phase noise performance. The THD of such ring oscillators can be expected to be significantly higher than 9%.

Fig. 40 shows the phase noise performance of the ring oscillator operating with an oscillation amplitude of 2 V_{pp} over the span of the tuning range. The phase noise improves as the oscillation frequency decreases. This can be attributed to fact that the larger static capacitors in the switch-based array are being utilized decreasing the impact that the voltage dependent parasitic capacitors have on the oscillation frequency.

Fig. 40 also contains the phase noise performance of the ring oscillator without the

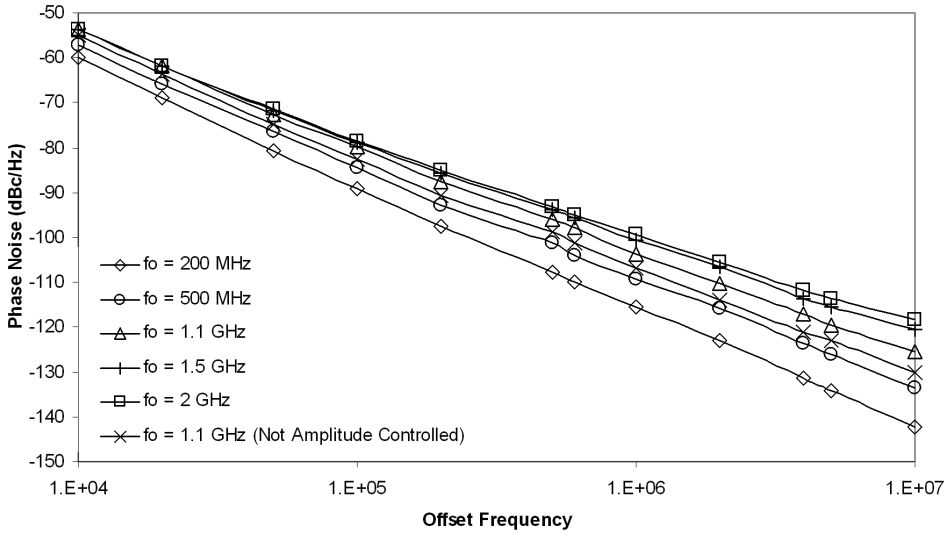


Fig. 40. Phase Noise Performance of Ring Oscillator

SMC implemented. Notice that implementing the amplitude controller does degrade phase noise. Amplitude noise is generated by the additional transistors of the SMC as well as switching noise noise from the current comparator. A large degree of the phase noise degradation can also be attributed to the difference in the oscillation amplitude of the ring oscillator with and without amplitude control since phase noise is relative to the carrier signal.

The spurious tones present in the *LC* oscillator are not as prevalent in the ring oscillator. This can be attributed to less switching logic in the 1-norm realization as well as the increased PSRR performance of the CMOS delay cells. Of course simulations also include ideal voltage sources which have perfect voltage regulation. Additional switching noise may become evident in a physical realization if non-ideal voltage sources are implemented with limited voltage regulation.

The phase noise analysis of common frequency offsets around the center frequency is provided in Table X. To compare the phase noise performance of this VCO with other reported works the FoM presented in Chapter I is calculated

Table X. Phase Noise Analysis of Ring Oscillator

Freq. Offset	Phase Noise
10 kHz	-55.83 dBc/Hz
20 kHz	-63.9 dBc/Hz
50 kHz	-74.5 dBc/Hz
100 kHz	-81.7 dBc/Hz
200 kHz	-89.5 dBc/Hz
500 kHz	-97.9 dBc/Hz
1 MHz	-105.6 dBc/Hz
2 MHz	-112.3 dBc/Hz
5 MHz	-121.5 dBc/Hz

$$FoM = L(1\text{ MHz}) + 10\log\left(\tfrac{1\text{ MHz}}{1.135\text{ GHz}}\right) + 10\log(24) = -152.9\text{ dB}$$

Table XI shows a comparison of the phase noise FoM of this work with other recently reported ring oscillator VCOs. The FoM achieved with the SMC is comparable with recent VCO architectures. Simulations of the ring oscillator realized for this thesis achieve phase noise performance comparable to saturated ring oscillators. The benefit of the prosed ring oscillator is that it operates over a wide-frequency tuning range with a controlled oscillation amplitude as well as controlled THD.

Table XI. Phase Noise Comparison of Recently Reported Ring Oscillators

Ref.	Freq. Range	Phase Noise (Offset)	Power	FOM
[28]	0.44 - 1.595 GHz	-93 dBc/Hz (1 MHz)	26 mW	-142.9 dB
[29]	0.66 - 1.27 GHz	-105.5 dBc/Hz (600 kHz)	15.5 mW	-157.1 dB
[30]	0.8 - 1.28 GHz	-100 dBc/Hz (1 MHz)	5.5 mW	-154.7 dB
[31]	0.1 - 3.5 GHz	-106 dBc/Hz (4 MHz)	16.2 mW	-152.7 dB
[32]	2.5 - 5.2 GHz	-90.1 dBc/Hz (1 MHz)	17 mW	-148.9 dB
[33]	5.16 - 5.93 GHz	-99.5 dBc/Hz (1 MHz)	-	-
This Work	0.17 - 2.1 GHz	-105.6 dBc/Hz (1 MHz)	24 mW	-152.9 dB

CHAPTER VI

CONCLUSION

Modified sliding-mode control techniques are proposed that provide amplitude control of harmonic oscillators. Amplitude stability in the sense of Lyapunov is demonstrated for a I/Q negative-G_m LC oscillator and a ring oscillator. Techniques are discussed to reduce chattering originating from the sliding-mode controller.

Verification of this amplitude control is accomplished with the physical realization of a I/Q negative-G_m LC oscillator. Measurement results show that the modified sliding-mode control scheme is successful at providing amplitude control of voltage-controlled oscillators.

A high-frequency, wide tuning-range, sinusoidal three-ring oscillator is developed and simulated at the transistor level using TSMC 0.18 μm CMOS technology. Simulations show the effectiveness of implementing this amplitude control over a wide-tuning range with minimal degradation to phase noise. The resulting ring oscillator has over a decade of frequency tuning range with low harmonic distortion.

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