VARIANCE REDUCTION AND OUTLIER IDENTIFICATION FOR I_{DDQ} TESTING OF INTEGRATED CHIPS USING PRINCIPAL COMPONENT ANALYSIS

A Thesis

by

VIJAY BALASUBRAMANIAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2006

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Duncan M. Walker
Committee Members,	Jennifer L. Welch
	Weiping Shi
Head of Department,	Valerie E. Taylor

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ABSTRACT

Variance Reduction and Outlier Identification for I_{DDQ} Testing

of Integrated Chips Using Principal Component Analysis. (December 2006)

Vijay Balasubramanian, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Duncan M. Walker

Integrated circuits manufactured in current technology consist of millions of transistors with dimensions shrinking into the nanometer range. These small transistors have quiescent (leakage) currents that are increasingly sensitive to process variations, which have increased the variation in good-chip quiescent current and consequently reduced the effectiveness of I_{DDQ} testing. This research proposes the use of a multivariate statistical technique known as principal component analysis for the purpose of variance reduction. Outlier analysis is applied to the reduced leakage current values as well as the good chip leakage current estimate, to identify defective chips. The proposed idea is evaluated using I_{DDQ} values from multiple wafers of an industrial chip fabricated in 130 nm technology. It is shown that the proposed method achieves significant variance reduction and identifies many outliers that escape identification by other established techniques. For example, it identifies many of the absolute outliers in bad neighborhoods, which are not detected by Nearest Neighbor Residual and Nearest Current Ratio. It also identifies many of the spatial outliers that pass when using Current Ratio. The proposed method also identifies both active and passive defects.

DEDICATION

To my mother

ACKNOWLEDGMENTS

I would like to thank my committee chair, Dr. Walker, and my committee members, Dr. Welch and Dr. Shi, for their guidance and support throughout the course of this research. Thanks to my friends and the department faculty and staff for making my time at Texas A&M University memorable. I also would like to extend my gratitude to the Department of Computer Science, Department of Electrical and Computer Engineering, NuView Mehta Foundation and Verizon for the scholarships and assistantships awarded to me.

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I. INTRODUCTION

1.1 Basics of Testing

Testing of Integrated Chips (ICs) is a manufacturing step that ensures that the manufactured physical device does not have any kind of defects. The quality of a manufacturing process is measured by its *yield*, which is the fraction of good chips produced. The quality of testing is measured in terms of *defect level* (DL), which is the ratio of faulty chips that pass all tests; and *fault coverage*, which is the percentage of potential circuit faults that are tested. Testing helps with quality assurance and ensures that specifications are met in the final product shipped to customers. Feedback from testing, along with other comprehensive data collected during the manufacturing process, can be analyzed using statistical process control [1] to improve manufacturing quality. The manufacturing process produces wafers in batches known as lots, with each wafer containing multiple ICs.

With recent advances in manufacturing technology, transistor geometries have shrunk significantly. Consequently, this has resulted in an increase in IC transistor density (number of transistors per unit area). Moore's Law [2] states that transistor density is expected to double approximately every eighteen months. IC manufacturers have the capability to pack more functionality into any chip without significantly increasing its size. As a result, the complexity of testing ICs has also increased rapidly.

This thesis follows the style of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

An ideal testing scheme would maximize fault coverage, while minimizing defect level and overall test costs. Any scheme would have to make a trade-off between fault coverage and test cost, as it is unnecessarily expensive and impossible for any test to screen all possible defects [3]. It is also important for any scheme to avoid false negatives. Any chip erroneously identified as defective has to be discarded and is a loss to the manufacturer. This is known as test *overkill*.

1.1.1 Types of Tests

Tests applied at the wafer level are known as *wafer sort tests*. Wafer sort tests are cost effective as they help in avoiding the cost associated with packaging defective chips. The savings achieved by early identification of defective chips becomes more significant as the cost of packaging increases [4]. There are two types of tests typically applied to ICs: *functional and parametric* tests. Functional tests are used to verify if known inputs result in expected behavior and outputs. A failure of this type means that the chip does not meet specifications and is definitely a defective chip. Parametric tests measure the value of specific parameters across the ICs in a wafer and mark a chip as a failure if the measurement falls outside normal expectations. Examples of parametric tests include speed (F_{MAX}), minimum operating voltage (MINVDD) and quiescent leakage current (I_{DDQ}) tests. Chips that fail functional tests are not subjected to parametric testing. Parametric failures indicate a problem with the quality of the chip, even if the specifications are met. An example of a parametric failure could be a chip that consumes more power than normal. This chip can still be used unless there are strict power constraints. Since these chips are still functional, the distinction between defective

chips and good chips is not always definitive, and the classification decision is subjective.

1.1.2 Defects and Faults

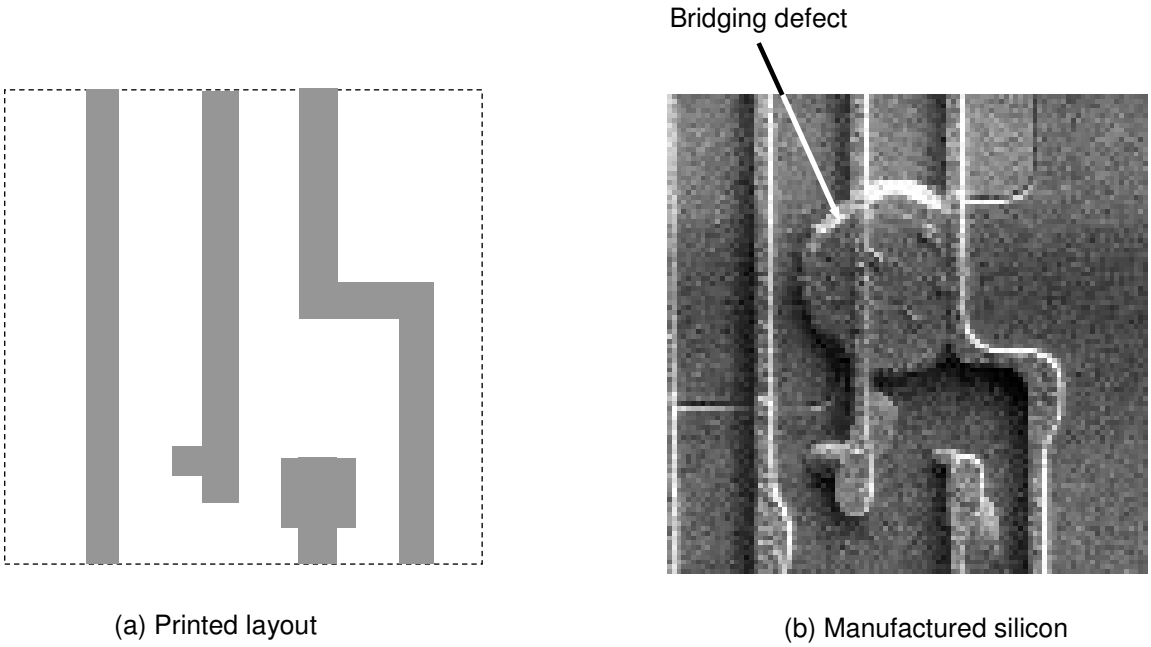


Figure 1. (a) Original layout and (b) actual silicon with bridging defect [5]

A *defect* is defined as a physical deformation leading to device malfunction. Examples of defects include processing defects (missing contact windows), material defects (crystal imperfections), and packaging defects (contact degradation). There are infinite defects that can occur at the physical level, and thus it is impossible to test for all possible defects. Since multiple defects manifest themselves with similar behavior in the IC, defects are modeled as *faults*. Faults are higher-level abstractions of defects, with a

finite number of fault locations on a chip. Examples of fault models include stuck-at-zero (node values always at logic 0) and AND-bridge (short between two nodes modeled to behave as an AND gate) models. Figure 1 gives an example of a bridge between two nodes. A chip that does not have any defects will be referred to as a *good* chip in the rest of the thesis.

Defects do not always cause functional failures. For example, the presence of a bridge between V_{DD} and ground nodes of a chip increases the current flowing through ground and thereby increases the power consumption of the chip. This circuit, even though it might pass all functional tests, might still be a reliability risk.

A defect has to be *observable* for it to be detected. A defect is observable at a node, if it affects the behavior or output of the IC. Functional tests strive to achieve high fault coverage on different fault models. In order for the defect to be detected, it has to be *excited*. Exciting a defect involves the use of a test vector that causes the defective node to behave differently than the defect-free node.

Defects can be classified into *active* and *passive* defects. Active defects are those defects that are pattern dependent. This means that the defect is observable only for specific input patterns. It is the responsibility of the test engineer to ensure that the test strategy has high fault coverage on these types of defects. Passive defects are pattern independent. Defects can further be classified as *local* and *global* process defects. Global process defects like mask misalignment affect the functioning of a whole wafer and local process defects like bridges affect ICs in a specific locality.

1.1.3 Statistical Post Processing

Burn-in (BI) tests have been the traditional method used for screening low reliability chips. During BI, ICs are subjected to stress at high voltage and temperature. The concept behind BI is that most of the risky chips fail at the early stages of their life (*infant mortality*) [6]. BI accelerates the aging process and catches infant mortality. Chips surviving BI are expected to have a low probability of failing in the field. The effectiveness of burn-in is decreasing because of the high costs and other physical effects [7]. Statistical post processing (SPP) of parametric test data collected at wafer sort has been suggested as an alternative to BI for identifying infant mortality [8].

In order to account for the lack of clear distinction between the values of good and defective chips, SPP methods have to allow for variable thresholds when setting pass/fail limits. This should prevent too many chips having marginal values from being categorized as defective [9]. The threshold limit should take into consideration the trade-off between DL and yield. Chips marked as defective because of unacceptable parametric data values will be referred to as *outliers* in the rest of the thesis. Outlier chips are known to have low reliability in the field [8]. The advantages of SPP methods are savings in time, fixtures, equipments and handlings [10]. Some examples of parametric tests used for SPP are low voltage (MINVDD) [11] and quiescent leakage current (I_{DDQ}) [12] tests.

1.2 I_{DDQ} Testing

The leakage current (I_{DDQ}) of a circuit is the current that flows through the ground nodes of an IC during its operation. The quiescent state for an IC is the state when all nodes have finished switching. A node is said to switch when its value changes from a binary 1 to 0 or vice versa.

The main idea behind I_{DDQ} testing is that in a good chip, there is no direct path between V_{DD} and ground for static inputs. Theoretically, this means that there should be no current flow to the ground node of any chip. In practice, there is always some background leakage current, but the magnitude of this current is negligible. The only time when the leakage current is expected to be higher is when the input changes. This causes some transistors to become open and others to close. This creates a temporary path between V_{DD} and ground. This value settles back to being negligible once the circuit reaches quiescent state. The presence of defects like a short across transistors can create a new path between V_{DD} and ground at quiescent state, thus increasing the leakage current. This unexpected increase can be used to identify defects in chips.

For example, Figure 2 shows a CMOS inverter circuit with one PMOS and NMOS transistor. When the input is logic 0, the PMOS transistor is closed and the NMOS open, causing the output to be logic 1. When the input changes from logic 0 to 1, the NMOS transistor turns on and the PMOS transistor turns off causing both transistors to be closed for a short time. This causes an increase in the leakage current above the usual noise. The final output settles to logic 0 and the leakage current stabilizes once both transistors reach their final state. The presence of a short across the PMOS

transistor as indicated in Figure 2, prevents it from being open, thus creating a path between V_{DD} and ground, increasing the quiescent leakage current. This type of defect is an active defect manifesting itself for an input of logic 0.

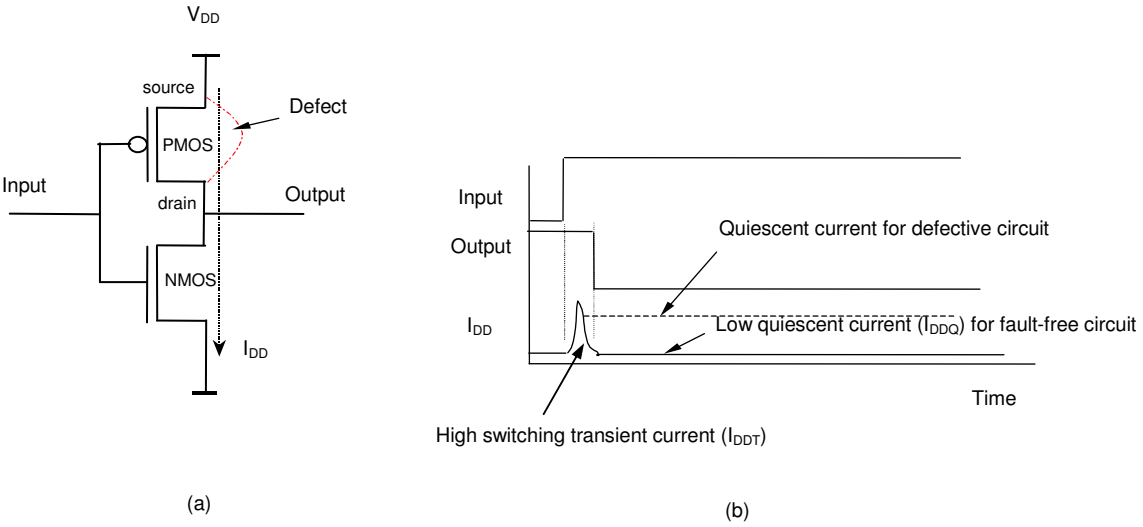


Figure 2. (a) Inverter CMOS circuit and (b) inverter timing diagram [5]

I_{DDQ} tests have the capability to detect shorts between two switching nodes, between a signal and V_{DD} and between V_{DD} and ground. The first two defects are active defects and the third defect is a passive defect. Some engineers consider passive defects benign, since they do not affect circuit functionality. Chips with passive defects are unusable under strict reliability constraints. I_{DDQ} testing falls under the category of parametric tests and there is no clear distinction between the values of leakage current of a defective chip and good chip.

1.2.1 Advantages of I_{DDQ} Testing

There are many advantages of I_{DDQ} testing [13]. One of the main advantages of I_{DDQ} testing is that it has 100% observability, unlike functional tests, such as a stuck-at test. Any defect that elevates leakage current can be detected by observing the power supply current. The only responsibility of test engineers is to excite all possible defects. Further, high fault coverage can be achieved by using a relatively small number of test vectors [14]. It has also been shown that I_{DDQ} tests are superior in identifying bridging defects when compared with voltage-based tests [15]. I_{DDQ} is also a viable alternative to BI tests [12] and can be used to identify weak ICs with latent defects. I_{DDQ} testing also detects some defects that are not detected by any other test methods [7], [16]. Some examples of this include resistive shorts, delay faults and faults in redundant logic.

1.2.2 Technology Effects on I_{DDQ}

The number of transistors in ICs is constantly increasing. During quiescent operation, the CMOS IC has about half of its transistors on (closed) and the other half off (open). Each of the transistors in the off state contributes a small leakage current. As the number of transistors increase, this background leakage current also increases.

The rapid increase in transistor density indicated by Moore's Law is achieved by constantly decreasing transistor geometries. In particular, the channel length (L) of a transistor has decreased considerably. The channel length is defined as the distance between the source and drain terminals of a MOS transistor. If the power supply voltage (V_{DD}) of a transistor is not lowered simultaneously with L, the internal electric field of

the transistor increases, decreasing the reliability of the transistor. Thus, V_{DD} is reduced to improve reliability and to decrease power consumed by the transistor. Consequently, the threshold voltage of the transistor (V_{TH}) has to be reduced in order to decrease the switching speed of transistors. The subthreshold leakage current of a MOSFET transistor is given by

$$I_{SUB} = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot V_t^2 \cdot e^{V_{GS} - \frac{V_{TH}}{\eta \cdot V_t}} \cdot (1 - e^{\frac{-V_{DS}}{V_t}})$$

where μ is the carrier mobility, C_{OX} is the gate capacitance per unit area, W is the channel width, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_t is the thermal voltage and η is a technology dependent parameter [17]. As indicated by the formula and as shown in Figure 3, the subthreshold leakage current increases exponentially with decrease in V_{TH} [18].

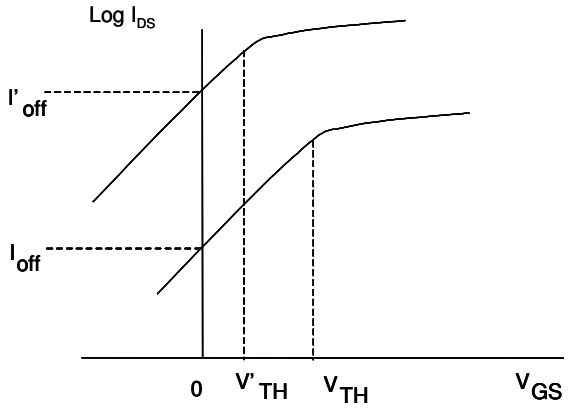


Figure 3. Effect of threshold voltage (V_{TH}) on I_{DDQ} [5]

Another phenomenon known as the *short channel effect* (SCE) [19] also increases the magnitude of leakage current of a short channel transistor. Figure 4 shows eight different components that affect the leakage current of a short channel transistor as suggested in [18]. I_1 is the reverse bias saturation current flowing across the PN junction of drain-to-substrate and well-to-substrate. I_1 is a significant component of the leakage current of long channel transistors. I_2 is the subthreshold leakage current and is a result of current flow from the drain to the source terminal. This current flows when V_{GS} is less than V_{TH}. *DIBL* is the channel surface current induced by the lowering of V_{TH}. *GIDL* occurs when a large electric field at the oxide-to-drain interface (due to V_{DD} bias voltage across the gate and drain terminals) causes charge tunneling and hole electron pairs subsequently. I_5 starts when applied voltage causes the charge depletion region of the source and drain to expand and meet, creating a short which allows the flow of current through them. This specifically affects short channel transistors where the source and drain depletion regions are closer to each other. I_6 affects transistors with width less than 0.5 μm. I_7 is caused because of the presence of very thin gate oxides, which allow for tunneling of electrons across it. I_8 is caused because of the injection of hot carriers into the oxide.

For short-channel transistors, all eight components can play a significant role, whereas long channeled transistors have only one significant leakage component (I_1). I_2 is insignificant for long channel transistors because of higher values of V_{TH}. All the other components are a result of physical phenomenon associated with smaller geometries.

Because of this, SCE causes a further increase in leakage current values of short channel transistors.

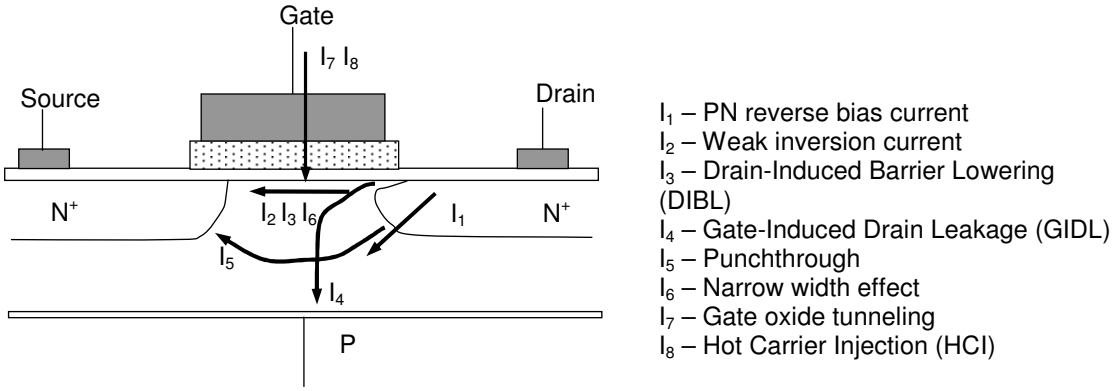


Figure 4. Leakage current components for short channel CMOS transistor [18]

Maintaining exact measurements for small transistor geometries is difficult. Any error in the actual transistor geometries causes some variations in the performance of the chip. Any IC will have many physical and environmental variations because of the complexity of the manufacturing process. This expected variation across the various parameters of a short channel transistor is known as *process variation*. Process variations occur due to variations in oxide thickness, imperfections in spatial uniformity of gas flow in various manufacturing steps etc.

For *deep submicron* (DSM) technology (technology using short channel transistors), the impact of process variation on IC performance is expected to be significant [20]. An example of the effect of process variation is that I_{DDQ} measurements of an IC will have large variations because of variations in *L* (because of the exponential

relationship between I_{SUB} and L). Process variations can affect the performance of an IC by up to 35% [21].

1.2.3 Challenge Facing I_{DDQ}

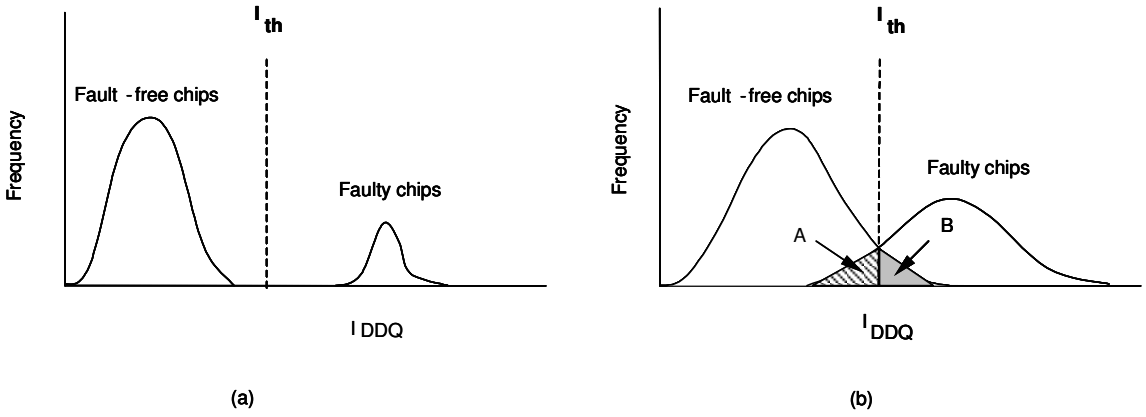


Figure 5. Effect of single I_{DDQ} threshold on (a) old and (b) DSM technologies [5]

Traditionally, it has been easy to estimate the expected leakage current values for defect free ICs empirically or through simulations. Any IC with I_{DDQ} value greater than the estimated value was considered faulty. This simple methodology is unsuitable for advanced and smaller technologies. The increase in I_{DDQ} because of defects is not significant when compared to background I_{DDQ}. This makes it hard to identify if a chip has high I_{DDQ} values because of SCE or because of a defect. The effect of process variation further complicates this process. Process variation creates an overlap in the I_{DDQ} values of defective and good chips as shown in Figure 5. This overlap causes any single threshold to create false negatives also known as *test overkill* (region B in Figure

5 causing loss to manufacturer) as well as false positives also known as *test escapes* (region A in Figure 5 affecting DL). This has contributed to a decrease in the overall resolution of I_{DDQ} testing [19]. Hence, the International Technology Roadmap for Semiconductors [22] considers I_{DDQ} to be a very difficult challenge.

1.3 Research Objectives

The aim of this research is to improve the resolution of I_{DDQ} testing for DSM technologies, by identifying defective chips when taking into account the effects of SCE and process variations. The proposed research method aims to achieve variance reduction in the leakage current values of ICs in order to widen the gap between leakage current of defective and good chips.

1.4 Structure of Thesis

The rest of the thesis is organized as follows: Section II covers some of the previous work published in this field; Section III covers the proposed method and research methodology. Results obtained from implementing proposed method on I_{DDQ} values of an industry standard chip are presented in section IV, followed by conclusions in Section V.

II. PREVIOUS WORK

Initially, I_{DDQ} testing methods concentrated on estimating maximum I_{DDQ} of good chips and any chip with I_{DDQ} greater than this value was considered defective. The threshold limit can be set through circuit simulations [23] - [25] or statistical analysis of empirical data [26]. Example of empirical analysis is identifying defective chips from the distribution of I_{DDQ} data. Defective chips with high I_{DDQ} values tend to be present at the tail of the distribution. Good chip I_{DDQ} values have to be estimated on a vector-to-vector basis in order to account for the different paths that are sensitized by each test vector.

The usability of such methods has decreased with the use of short channel transistors. Efforts of the research community have shifted to techniques resistant to the effect of SCE and process variations. The bulk of research efforts have concentrated on three classes of methods for improving I_{DDQ} testing:

- The first class of methods uses manipulate measured I_{DDQ} to achieve *variance reduction*. This reduces the overlap between defective and good chip distributions.
- The second class of methods uses the correlation/dependence of I_{DDQ} with other parameters to identify defective chips.
- Finally, other methods use complex statistical analysis techniques to group chips as defective and good.

This section contains an overview of some of the important literature published by the research community. There are other techniques like the use of statistical clustering, wafer signatures, eigen-signatures, design for I_{DDQ} testability, and I_{DDT} based techniques [27] that are not covered in this section.

2.1 Current Signature

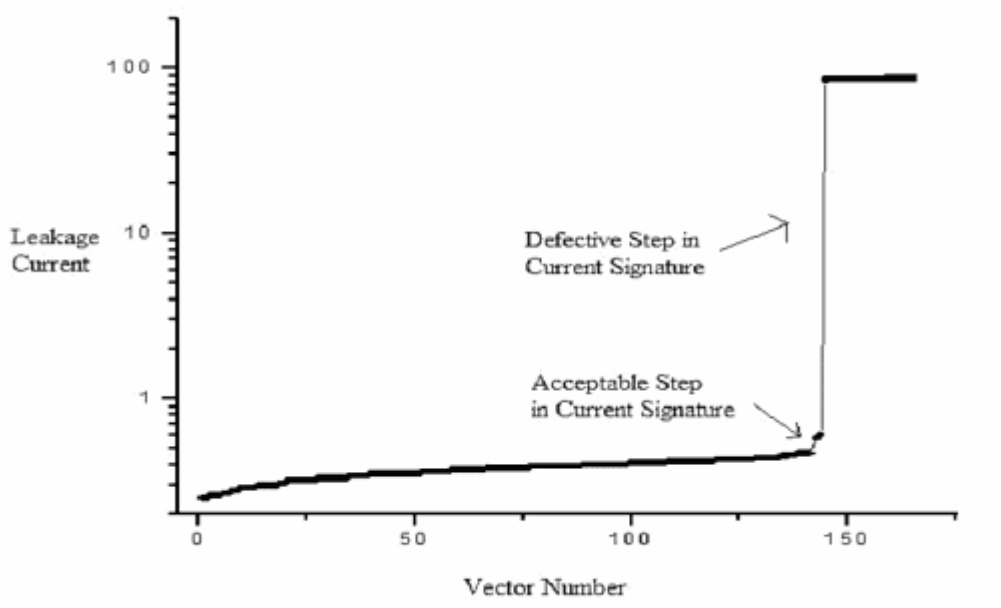


Figure 6. Example of current signature

The current signature [28] of a chip is the graphical plot of I_{DDQ} measurements for all test vectors sorted in ascending order. The presence of an active defect causes a rise in measured I_{DDQ} and causes a step in the signature. Any chip with a sufficiently

large step in the signature is considered defective. Current signatures are also very useful for failure diagnosis [29]. Figure 6 gives an example of a current signature.

Current signatures do not detect chips with passive defects, as the I_{DDQ} measurements of all vectors will be elevated and do not produce any steps. In order for current signatures to be effective, there has to be a sufficient number of test vectors. Measurement of I_{DDQ} is a slow process because of the waiting required for the chip to settle into the quiescent state. This makes it impractical to measure I_{DDQ} for many vectors.

2.2 Current Ratios

The current ratio (CR) of a chip is defined as the ratio of maximum I_{DDQ} to minimum I_{DDQ} over all test vectors. It has been observed that the current ratios of good chips are almost equal, even for DSM technologies [30]. Current ratios are independent of the absolute value of currents and thus are self-scaling with process variations. For testing, the vectors causing minimum and maximum I_{DDQ} values can be estimated using circuit characterization and the expected CR is calculated. The tester measures the I_{DDQ} for these two vectors on all chips and rejects a chip if the CR is not within expected CR and its guard band. CR has the same disadvantages of current signatures in that it has difficulty detecting passive defects. The presence of a passive defect increases the I_{DDQ} of all vectors proportionately, decreasing CR. The main disadvantage of CR is that some defective chips can still have the same CR value as good chips, thus making it hard to detect them.

2.3 Statistical Outlier Rejection Methods

Statistical techniques like Chauvenet's Criterion and the Tukey Test [31] can be used to estimate if entries in a population do not conform to normal behavior. Both these methods assume that the distribution of the population is normal. I_{DDQ} values can be expected to have a lognormal distribution because of the exponential relationship between I_{DDQ} and L. Lognormal data can be converted to the normal distribution by taking a natural log of the original data. The converted data set will still not be completely normal because of the effect of process variations and measurement noise.

Chauvenet's Criterion uses the probability of occurrence of a measurement to detect outliers. An observation is an outlier if the number of measurements at least as bad as the observation is less than a coefficient c,

$$n(\textit{worse than observation}) = N \cdot Pr(\textit{Occurrence of Measurement})$$

where N is the total number of observations. The probability of occurrence can be obtained from a normal error integral table. The value of c for a normal distribution is 0.5. The Tukey Test rejects an observation as an outlier if it falls outside the range of

$$[\, LQ - k \cdot IQR,\ UQ + k \cdot IQR]$$

where k is a constant, LQ is the first quartile value, UQ the third quartile value and IQR is the inter-quartile region ($UQ - LQ$). If the distribution is normal, a k of 1.5 corresponds to the 3σ limit. For both these test methods, the coefficients must be chosen carefully taking into account the normality of the data set, in order to retain their effectiveness.

2.4 Correlation/Dependence of I_{DDQ} on Other Parameters

The leakage current of a good chip (explained in Section 2) depends on the temperature *T*.

$$I_{DDQ} \propto e^{T}$$

A good chip with no defects can be expected to have higher leakage at higher temperatures. This relationship can be exploited to test ICs by making current measurements at two different temperatures [32]. I_{DDQ} in the presence of defects may remain the same or decrease with an increase in temperature. The problem with this approach is that it is impractical because of the costs associated with testing at multiple temperatures during production. However, it is useful in diagnosis.

Another physical parameter that affects I_{DDQ} is the power supply voltage. I_{DDQ} measurements for the same test vector at multiple voltages can be used to identify defective chips [33]. Implementation of testing at multiple voltage levels is not straightforward at the production level and there is a decrease in voltage spread with the decrease in V_{DD} for DSM transistors.

There is a high correlation between the leakage current of an IC and its maximum operating frequency. Both parameters are dependent on the channel length. Shorter channel length results in a linear increase in switching speed, but an exponential increase in leakage current. This correlation can be exploited to identify defective chips [34].

2.5 Justification for Variance Reduction

The idea behind variance reduction is that underlying process variations affecting I_{DDQ} testing can be removed with the help of a reasonably accurate estimation of good chip I_{DDQ} values ($\hat{I}$) [35]. The residue ($\tilde{I}$) calculated by

$$\tilde{I} = I - \hat{I}$$

where I is the measured I_{DDQ} test response, will have a distribution with reduced variance and reduced overlap of good and faulty chip distributions. Applying statistical techniques on the residual to identify outliers will improve DL and decrease false negatives.

Assume that the estimates for good chip I_{DDQ} values $\hat{I}$ are accurate and the wafer predominantly contains good ICs. In this situation, the mean value of residual $\tilde{I}$ would be nearly zero. Mathematically,

$$E[\tilde{I}] = E[I - \hat{I}] = E[I] - E[\hat{I}] \approx 0$$

In a wafer with outlier measurements, with ε being the offset from I, the expected value of the residual is:

$$E[I + \varepsilon - \hat{I}] = E[\tilde{I} + \varepsilon] = E[\tilde{I}] + \varepsilon \approx \varepsilon .$$

This shows that the effect of the defect will still be present in the residual and that information is not lost with variance reduction [35]. This is true only if the estimate $\hat{I}$ is reasonable.

For any wafer, the variance of $\tilde{I}$ is

$$Var(\tilde{I}) = \sigma_I^2 + \sigma_{\hat{I}}^2 - 2\rho \cdot \sigma_I \cdot \sigma_{\hat{I}}$$

where σ^2 represents variance and ρ is the covariance between I and $\hat{I}$. In order to reduce the variance of $\tilde{I}$, there must be a high correlation between I and $\hat{I}$ [35]. The following cases from [35] clarify this situation:

- If the good chip I_{DDQ} estimate is the mean of the measured values, then $\sigma_{\hat{I}} = 0$ and the variance of $\tilde{I}$ will be the same as the variance of I.
- If the good chip estimate is the same as the measured values, then $\sigma_{\hat{I}} = \sigma_I$ and $\rho = 1$. This causes the variance of $\tilde{I}$ to be zero.
- If $\sigma_{\hat{I}}^2 = 0.8\sigma_I^2$ and $\rho = 0.8$, then $Var(\tilde{I}) = 0.2\sigma_I^2$.

Thus, any reasonably accurate good chip I_{DDQ} estimate can be used to achieve variance reduction and to improve the likelihood of detecting the presence of a defect.

In order to formulate a good estimate of good chip I_{DDQ}, data statistics such as lot means, standard deviation of wafer means, average wafer standard deviation and standard deviation of wafer standard deviations can be used as clues to identify variation sources more accurately [36].

2.6 Delta I_{DDQ}

Delta I_{DDQ} is a variance reduction method that tries to eliminate background leakage currents [37]. The delta I_{DDQ} of a chip for the i^{th} vector is defined as

$$\Delta I_{DDQ}(i) = I_{DDQ}(i) - I_{DDQ}(i-1)$$

where $I_{DDQ}(i)$ and $I_{DDQ}(i-1)$ are the leakage current measurements for the i^{th} and $(i-1)^{st}$ vectors. For a good chip, the mean value of ΔI_{DDQ} should almost be equal to zero since

each vector will sensitize similar leakage paths. The presence of an active defect causes a spike in the ΔI_{DDQ} values. The assumption here is that there is at least one test vector that causes excitation of a defect and one adjacent vector that exhibits normal leakage values. The presence of a passive defect causes all the I_{DDQ} values to be high and thus does not affect ΔI_{DDQ}. The effectiveness of delta I_{DDQ} depends on the number of test vectors. The limited number of test vectors reduces its effectiveness. The future of delta I_{DDQ} for DSM technologies is questionable [15].

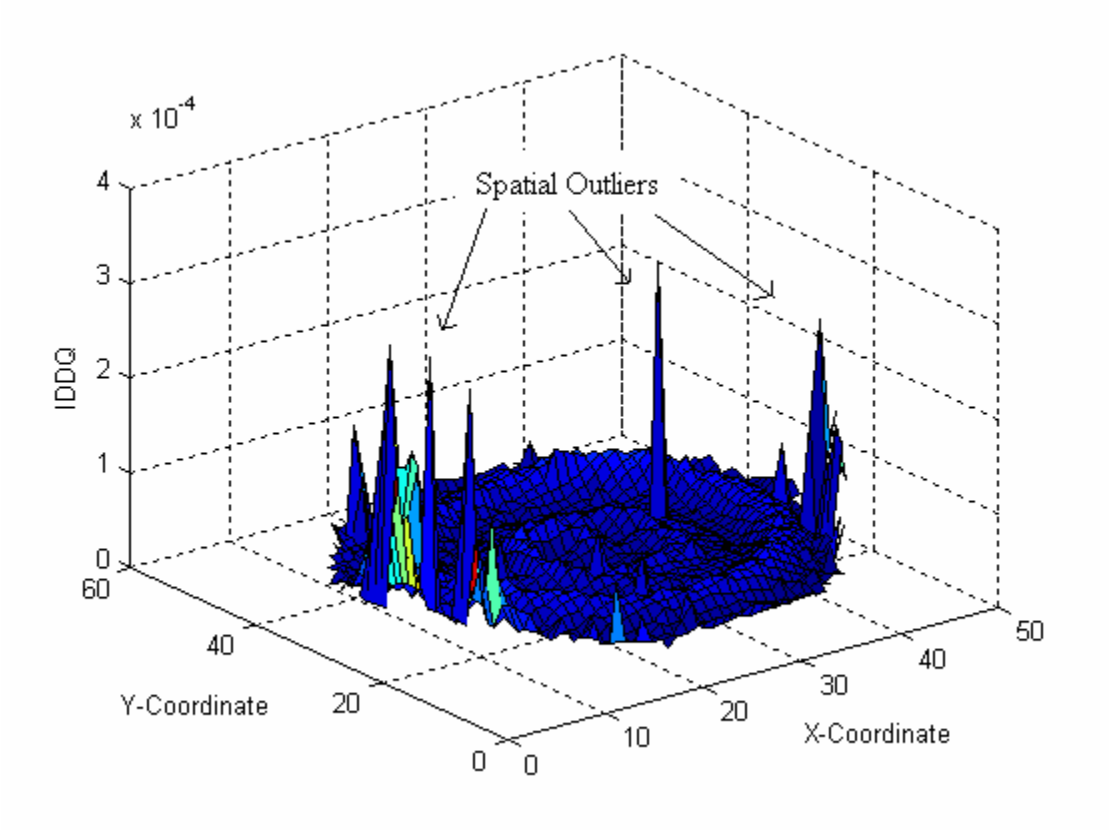


Figure 7. Wafer level raw I_{DDQ} surface plot

2.7 Wafer Level Spatial Correlation Methods

The good chip I_{DDQ} values of neighboring chips on a wafer have high correlation as they undergo similar process parameters and changes. As a result, the I_{DDQ} values of neighbors can be used as an estimate for the purpose of variance reduction. Defect clustering also suggests that a chip with many defective neighbors is more likely to fail. Any chip that has significantly higher I_{DDQ} values when compared to its neighbors is a termed a *spatial outlier*. Every chip in a wafer has at most eight immediate neighbors. Chips on the wafer edge will have less than eight neighbors and other chips might have less than eight if some of the neighbors failed functional tests (and so no I_{DDQ} test was applied). Figure 7 shows an example of I_{DDQ} surface plot across a wafer. Many methods have been proposed that take advantage of the spatial correlations between chips. Wafer level post processing has applicability to other parametric test data and helps in improving the early failure rate [8]. The main disadvantage of wafer level analysis is that any defective chip present in a bad neighborhood will pass because of conformance with chips in the immediate neighborhood, increasing the DL.

2.7.1 Nearest Neighbor Residual (NNR)

The mean I_{DDQ} at a location over all test vectors is used as the I_{DDQ} of an IC for spatial analysis. This method uses the median of neighboring chips I_{DDQ} as the estimator for variance reduction [38]. The median is resistant to outliers, so the estimate will retain its accuracy even in the presence of defective neighbors. High residuals are considered an indicator of defective chips. If any chip does not have all its eight neighbors, chips at

longer distances are used to obtain at least eight for use in the estimate. To avoid the bias generated by choosing random chips at longer distances, all the chips at a particular distance from the current chip being tested are used. The effectiveness of NNR depends on the smoothness of the within-wafer measurement values. In the presence of regular spatial patterns, such as due to stepper fields, sophisticated neighbor selection methods must be used to identify neighbors with the highest correlation [39].

2.7.2 Neighbor Current Ratio (NCR)

The NCR value of a node is defined as the ratio of the I_{DDQ} of a chip to that of its neighbor for the same test vector [40]. The NCR value of a good chip is expected to be equal to one. Process variation causes some variation in the value of NCR, but it should be close to one. The maximum NCR value of a chip over all test vectors and all neighbors is used for outlier analysis. NCR is a variance reduction method using the ratio as the mode of variance reduction rather than the residual. In the absence of neighbors, dies at farther distances can be used in a method similar to that of NNR.

2.7.3 Spatial Fit Method

The I_{DDQ} values coupled with the X and Y location of neighbors can be manipulated to estimate maximum good chip I_{DDQ} values for the purpose of variance reduction. Using I_{DDQ} as the value for the Z dimension, linear regression can be used to form the best fit plane and the estimate for the current chip being tested can be extracted from the plane [41]. For forming the best-fit plane, one needs at least three data points, and if a chip does not have three neighbors, dies at longer distances are used.

2.7.4 Immediate Neighbor Difference I_{DDQ} Test (INDIT)

This method is similar to NNR. The main difference is that the analysis is performed on a vector-by-vector basis. The residual for a chip is calculated as the maximum of the residual with each of the neighbor [42]. Outlier analysis is performed on the residual data for each vector.

2.7.5 Neighbor Selection Using Location Averaging

A fixed neighborhood for wafer level spatial analysis works fine when the I_{DDQ} across the wafer exhibits a smooth pattern. Along with smooth patterns, I_{DDQ} data also exhibit systematic patterns across the wafer, due to processing effects such as the stepper field. Linewidth variation within the stepper field results in a checkerboard pattern in measured values across the wafer. The effects of such patterns vary on a wafer-to-wafer and lot-to-lot basis. This makes it essential to use a neighbor selection scheme that dynamically identifies inherent patterns across a wafer.

Location averaging [39] is one such method. The first step involves using every candidate neighbor as the estimate for the whole wafer. The best residual obtained across the whole wafer using this estimate is computed (median of residuals). The candidate neighbors that have the best residual with respect to the whole wafer are used for performing variance reduction.

2.8 CR and NCR

A combination of CR and NCR can be effectively used to weed out false positives from each of the tests [43]. The advantages of CR and NCR complement each other. For example, low CR value and a correspondingly high NCR value indicate the presence of a passive defect. This kind of defect, which escaped detection in CR, will be detected by NCR. Conversely, CR can detect a chip in a bad neighborhood that contains an active defect, which may escape the NCR test. The presence of a passive defect in a bad neighborhood is one situation where neither CR nor NCR identifies the defect.

2.9 Independent Component Analysis (ICA)

ICA has been suggested as an SPP method to identify outliers in I_{DDQ} data [44]. ICA is a multivariate statistical analysis technique that extracts statistically independent sources of variations from the original data. The independent sources of variations are used to model the underlying process parameters and process variations. NNR analysis is performed on each of the extracted source to identify outliers.

2.10 Variable Reduction Using Principal Component Analysis (PCA)

PCA is another multivariate statistical technique that is used to extract uncorrelated sources of variations from a data set. A variable reduction (VR) method [45] based on PCA can be used to remove I_{DDQ} measurements from the data set that provide redundant information and other measurements that explain very little variance. VR is used to reduce the complexity of the data set being analyzed. The output of VR is

run through PCA again, the Euclidian distance of all chips is calculated with the source values as coordinates, and a contour is set. Any chip that falls outside this contour is considered defective (or a candidate for burn-in).

2.11 Need for Future Research

There is no one test that can identify all defects while avoiding false negatives and false positives. Each test has its own advantages where they catch specific kinds of defects or defect behaviors. Development of new test methods will increase the total number of defects detected and reduce the DL.

None of the variance reduction methods explained in this section attempt to model the measured I_{DDQ} values based on underlying physical factors like SCE, when trying to estimate good chip values. The contribution of this thesis is to use principal component analysis for the purpose of variance reduction and specifically, to estimate good chip I_{DDQ} values. The effects of physical factors are inherently accounted for by PCA. The proposed outlier rejection techniques also attempt to identify passive and active defects, irrespective of if they are present in a good or bad neighborhood.

III. PROPOSED METHOD

The main causes for the decrease in resolution of I_{DDQ} testing are the effects of SCE and process variations. In the technique proposed in this thesis, a multivariate statistical analysis method known as principal component analysis (PCA) is used to model and extract the effects of SCE and process variations. PCA is preferred over ICA because the physical parameters affecting IC performance are correlated to each other rather than independent to each other. The extracted parameters are used to estimate the good chip I_{DDQ} values for the purpose of variance reduction. Analysis is performed on a wafer-by-wafer basis because different process parameters may have varying significance in different wafers.

3.1 Principal Component Analysis

Multivariate statistics consists of procedures that involve the observation and analysis of more than one statistical variable. PCA is one such procedure that aims to reduce the dimensionality of a data set while retaining majority of the variance of the original data set [46]. Reduction in the dimensionality is possible only when the inputs are interrelated. For example, suppose we are interested in studying the variance and correlation/covariance structures of p variables in a data set x. We would have to analyze the data as well as $\frac{1}{2} \cdot p \cdot (p-1)$ entries in the correlation/covariance matrix. This is not feasible unless the size of p is small. An alternative approach is to analyze a derived data set y (obtained using PCA), which retains most of the variance and

correlation/covariance information from x using m variables. If $m<p$, then the amount of data to be analyzed reduces.

The set of variables outputted by PCA are known as *principal components* (PCs or components). PCA extracts components concentrating on variances. PCs are extracted in increasing order of variance explained and all PCs are uncorrelated. The variability in the original data set is projected onto a set of new axes. PCA extracts as many PCs as the number of variables (p). In general, the first few (m) components are expected to explain most of the variance in the original data, where $m << p$ for large values of p. The rest of the components are not important in terms of the variance of the original data set. Figure 8 shows an example of how to visualize PCA. The original data set has two variables (x and y) and PCA outputs two PCs, with the first PC explaining most of the variance. There is no reduction in the number of meaningful components because of the small value of p. However, PCA helps in better visualization of the data.

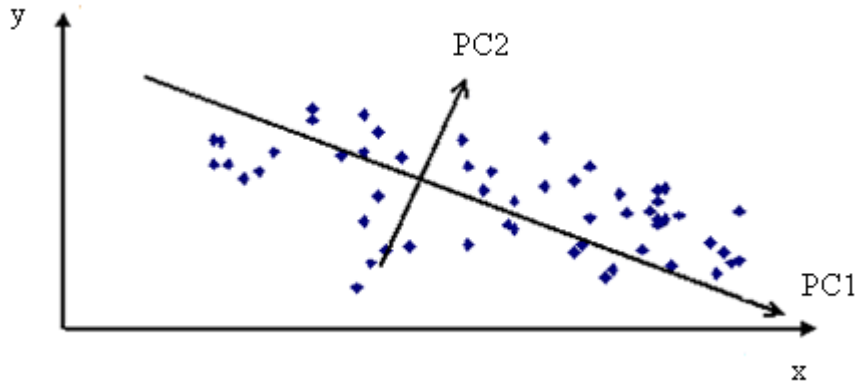


Figure 8. Visualization of PCA

3.1.1 Scree Test

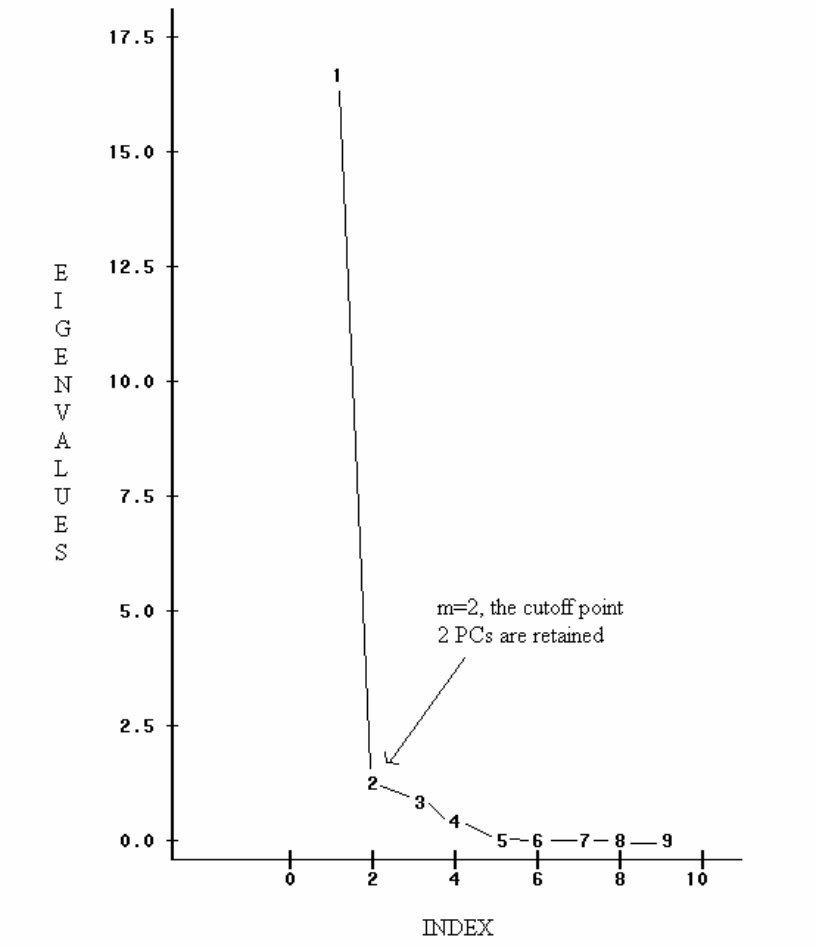


Figure 9. Scree plot for selecting significant PCs

There are many ways to decide on the number of PCs to retain (choosing the value of *m*) during dimensionality reduction. One such method known as the Scree test uses a graph known as the Scree plot [47]. The Scree plot is a line graph of the eigenvalues of each PC against their index. The eigenvalues are computed during PCA,

and represent the importance of each component. The number of PCs to be retained (m) is chosen such that the slope of all lines before the m^{th} PC are all steep and to the right of the m^{th} component are not steep. The definition of steep and not steep is subjective. Figure 9 shows an example of a Scree plot with a cutoff point.

3.1.2 Factor Scores, Factor Pattern and Factor Loading Matrices

The new data set that is output by PCA is referred to as *factor scores* (y) in the rest of the thesis. Another feature of PCA is that the PCs extracted are a linear combination of the p variables in the original dataset x standardized (x_{STD}). The coefficients used to achieve this transformation will be referred to as the *factor loading matrix* (A).

$$y = x_{STD} \cdot A$$

The original data set can also be represented as a linear combination of the extracted PCs. The coefficients of this transformation will be referred to as the *factor pattern matrix* (B).

$$x_{STD} = y \cdot B$$

$$x_k = y_1 b_{k1} + y_2 b_{k2} + \ldots + y_p b_{kp}$$

where x_k is the k^{th} variable in x_{STD}.

3.2 Variance Reduction Using PCA

The main idea behind the proposed method is that PCA is used to model the inherent physical effects that are affecting the leakage current in DSM transistors. The good chip I_{DDQ} values of all chips in a wafer are estimated by manipulating the output of PCA and outliers are identified from the reduced data. In order to run PCA on the data, we need to identify the input data set. For this case, the input will be the I_{DDQ} measurements of all chips across one wafer for multiple test vectors. Each test vector I_{DDQ} value is a variable for PCA. Some preprocessing is done on the data, to make it more suitable for PCA.

3.2.1 Normalizing Transformation

PCA does not make any assumptions about the distribution of the input data set. However if the input data set follows the normal distribution, the accuracy of the PCs extracted increases. I_{DDQ} follows the lognormal distribution and the natural log of I_{DDQ} measurements is used to make the inputs closer to the normal distribution.

3.2.2 Scaling of Data

Applying the normalizing transforms to I_{DDQ} data causes negative values to be part of the data set used as input to PCA. To avoid this, I_{DDQ} data is scaled before the normalizing transform is applied. The formula used for scaling is:

$$I_{SCALED\_i} = \frac{I_{DDQ\_i}}{\min(I_{DDQ\_i})}$$

where I_{DDQ_i} is the I_{DDQ} measurement for the i^{th} vector and I_{SCALED_i} is the scaled value for the i^{th} vector.

3.2.3 Extreme Outlier Removal

The presence of extreme outliers in a data set has a disproportionate impact on the PCs, and in some cases, the PCs may be significantly determined based on these outliers [46]. These extreme outliers with very high I_{DDQ} values for some test vectors need to be removed from the data set, to avoid distorting the results. For this purpose, a very high hard threshold can be used. If any chip has a measured I_{DDQ} value that is greater than this threshold, it can be rejected as an outlier. Other techniques that can be used are statistical methods like the Tukey test or Chauvenet's criterion. Any of the methods covered in Section II. Previous Work should work for this purpose. Care has to be taken to ensure that the pass/fail threshold is not too strict, as the objective is to remove the extreme outliers only.

3.2.4 Variance Reduction

Running PCA on the normalized, extreme outlier removed I_{DDQ} data, outputs a set of factor scores, the factor pattern and factor loading matrices, and the Scree plot. The factor scores will be the score of each chip on the different components. The results will contain as many components as the number of test vectors in the original data set. As explained above, the first several components explain most of the variance in the input data set. The Scree plot is used to identify how many of the components to retain for further manipulation.

In the I_{DDQ} data, the first component output by PCA explains most of the variance. This component likely explains transistor gate length variation. Gate length varies more than other process parameters, and affects I_{DDQ} through the short channel effect. The second component is likely to be V_{TH} implant variation, which directly affects leakage. The labeling provided with this analysis is just an educated guess based on the knowledge of underlying physics of ICs. It would be impossible to identify the components with high confidence based only on the I_{DDQ} measurements.

The variances explained by the significant components are expected for all chips across a wafer, including defective ones. These components theoretically exacerbate the problem of identifying defective chips, by increasing good chip I_{DDQ} values and by causing significant variations in measured I_{DDQ}.

The significant components in the original I_{DDQ} measurements can be used to estimate good chip I_{DDQ} for the purpose of variance reduction. Reduced data can be calculated by subtracting the good chip I_{DDQ} values from the original I_{DDQ} measurements. The only variance remaining in the reduced data should be that caused by defects. To calculate the reduced I_{DDQ} data, the factor pattern matrix and the factor scores need to be manipulated.

$$x_{RED} = x_{STD} - y_{1..m} \cdot B_{1..m}$$

where x_{RED} is the reduced I_{DDQ} data, x_{STD} is the standardized original I_{DDQ} data, $y_{1..m}$ is the factor scores for the first m significant component and $B_{1..m}$ is the factor pattern matrix containing coefficients for the first m significant components.

3.2.5 Outlier Identification

Active defects present in chips increases the I_{DDQ} measurements for defective chips and only for the test vector exciting the defect. The increase in I_{DDQ} by this kind of defect should not account for significant variance in the original data. I_{DDQ} outliers caused by active defects should be a part of the other ignored components. On the other hand, passive defects increase the I_{DDQ} of a chip for all test vectors. This might cause significant variations in the original data, and might be hidden in the significant components.

In order to identify active defects, we need to perform statistical analysis on the reduced I_{DDQ} measurements. The variance of the reduced data set should be much lower than the variance of the original data. Any kind of statistical method covered in the previous work, such as the Tukey test, can be applied at this stage, on each of the test vectors. Further variance reduction should be avoided as the main cause of variations have already been identified and extracted.

In order to identify passive defects, we need to analyze the significant components. We can perform statistical outlier analysis using methods such as the Tukey test, or apply variance reduction methods like NCR or NNR to each of the significant components to identify passive defects hidden in each of them.

3.3 Overview of Proposed Method

The following steps are an overview of the proposed method with the flow chart shown in Figure 10.

- Scale data.
- Apply normalizing transform to I_{DDQ} measurements.
- Remove extreme outliers from transformed data.
- Run PCA on data.
- Use Scree plot to identify number of significant components.
- Compute standardized I_{DDQ} values.
- Perform data reduction using factor scores and factor pattern matrices.
- Identify active defects in reduced data.
- Identify passive defects in different significant components.

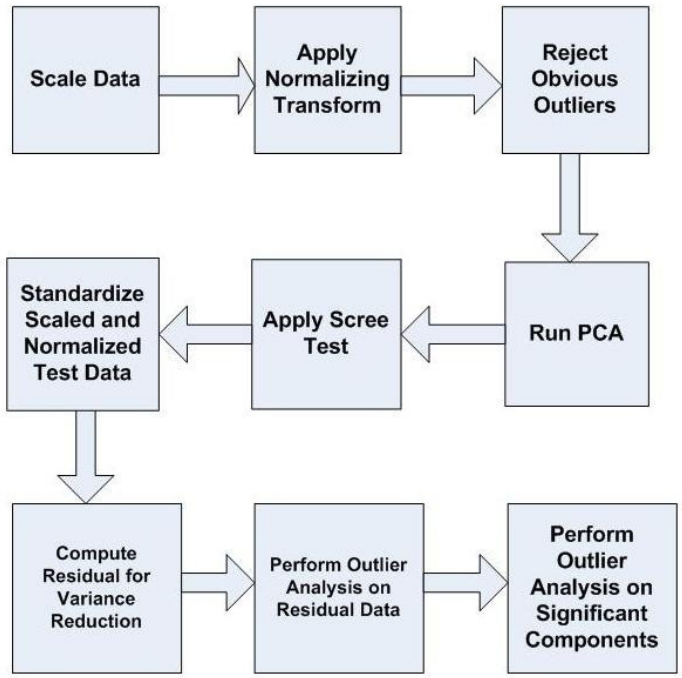


Figure 10. Flow chart of proposed method

IV. IMPLEMENTATION AND RESULTS

The scripts used to execute the different stages of the proposed solution approach were implemented in Matlab. The script for PCA was written in SAS, which outputs the factor pattern, factor scores and factor loading matrices for any given input.

The idea was implemented and tested on I_{DDQ} measurements from a high-volume industry chip manufactured using 130 nm technology. The I_{DDQ} data set contains measurements for 10 test vectors across 14 different wafers. Leakage current was measured for each test vector pre and post voltage stress (an elevated voltage designed to cause failure in weak transistor gate oxides).

All analysis for the proposed method has been performed on scaled and normalized I_{DDQ} measurements and not the original measurements. Any reference to I_{DDQ} with respect to the proposed method is actually referring to the scaled and normalized data. The analysis for evaluation on classic methods such as NCR, NNR etc. have been done using the original I_{DDQ} measurements without any scaling or normalizing transforms. The reason is that methods such as NCR and NNR are self-scaling.

4.1 Normalizing Transformation

Figure 11 shows the normal probability plot of scaled I_{DDQ} measurements for a vector across one wafer, and Figure 12 shows the normal probability plot of the same vector after applying the natural logarithm as a normalizing transform. This transformation is used because I_{DDQ} is exponential in transistor threshold voltage, which

in turn is primarily linear in transistor gate length. Since gate length variation is the dominant process variation, if gate length is Normal, then I_{DDQ} will be lognormal. Using the log transform should result in data that is Normal, except for outliers.

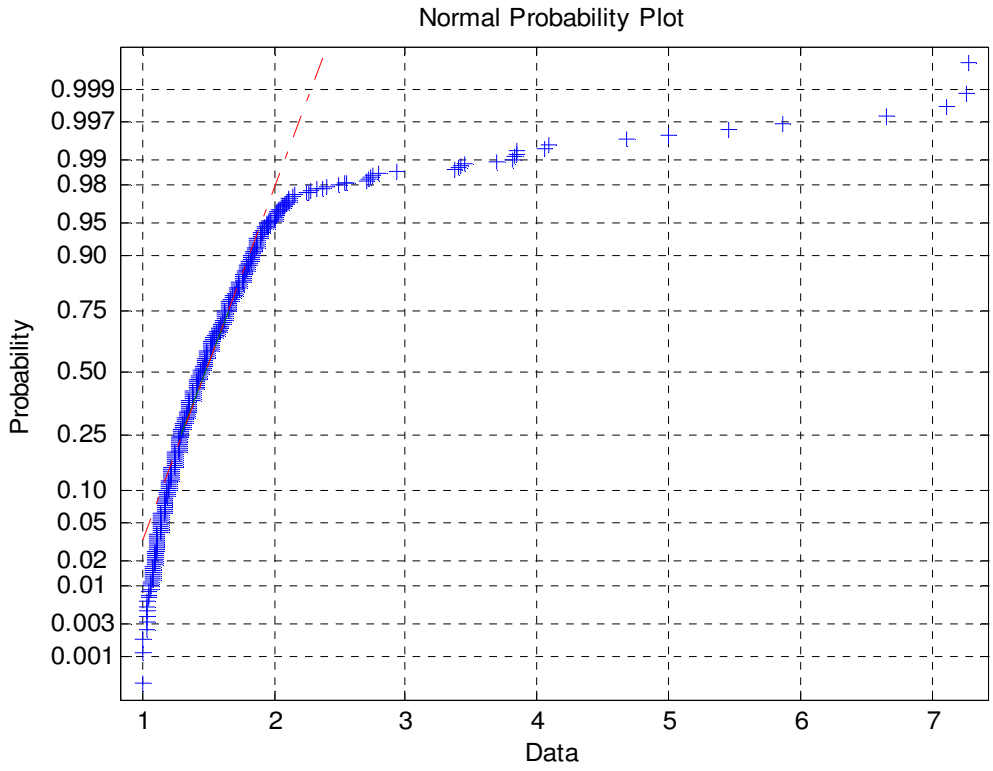


Figure 11. Normal probability plot of scaled I_{DDQ} data

The normalized data values in Figure 12 are closer to the normal line (red) than in Figure 11. Since our outlier analysis techniques and PCA depend on normally-distributed data, the log of the scaled I_{DDQ} values is used for analysis.

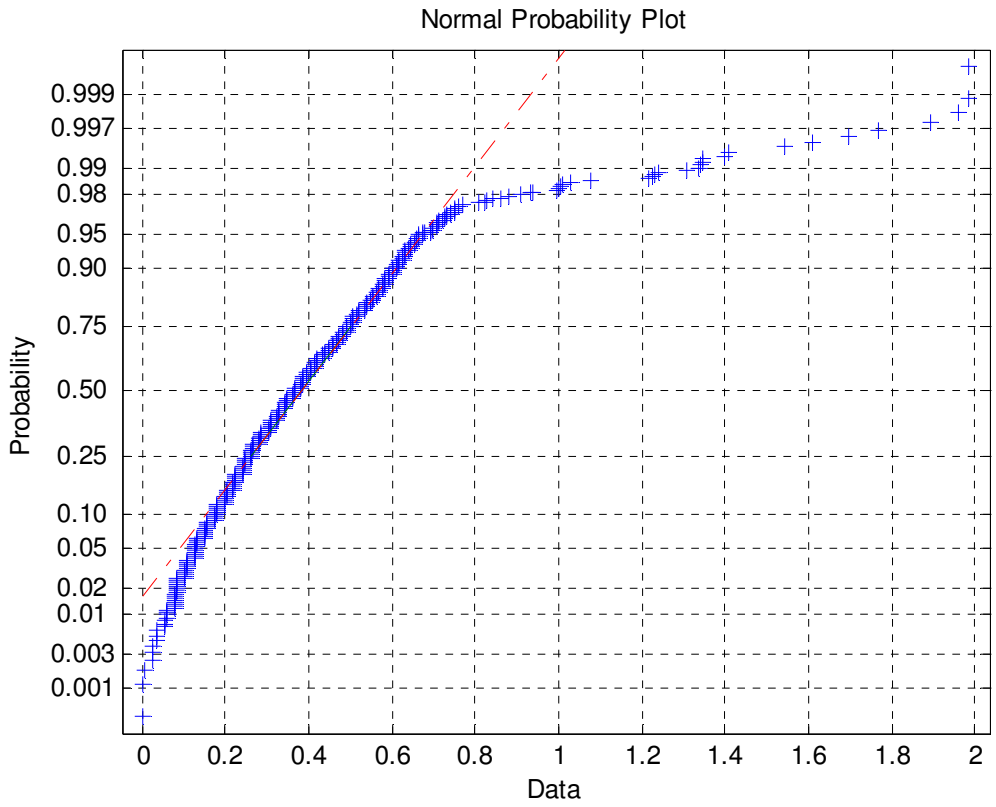


Figure 12. Normal probability plot after normalizing transform

4.2 Pre and Post Stress Data

As mentioned above, the I_{DDQ} data set contains leakage current measurements for different test vectors at nominal operating voltage. The chips were then subjected to stress at higher voltages. The same test vectors were reapplied to the chips again at nominal operating voltage. For chips without gate oxide defects, the voltage stress does not affect I_{DDQ} significantly. For some chips with defects, applying high voltage can either heal the defect (causing post-stress I_{DDQ} to be lower), or cause a low reliability

chip to become defective (post-stress I_{DDQ} is higher). Any chip that has a significant positive or negative shift in I_{DDQ} is a defective chip with reliability issues.

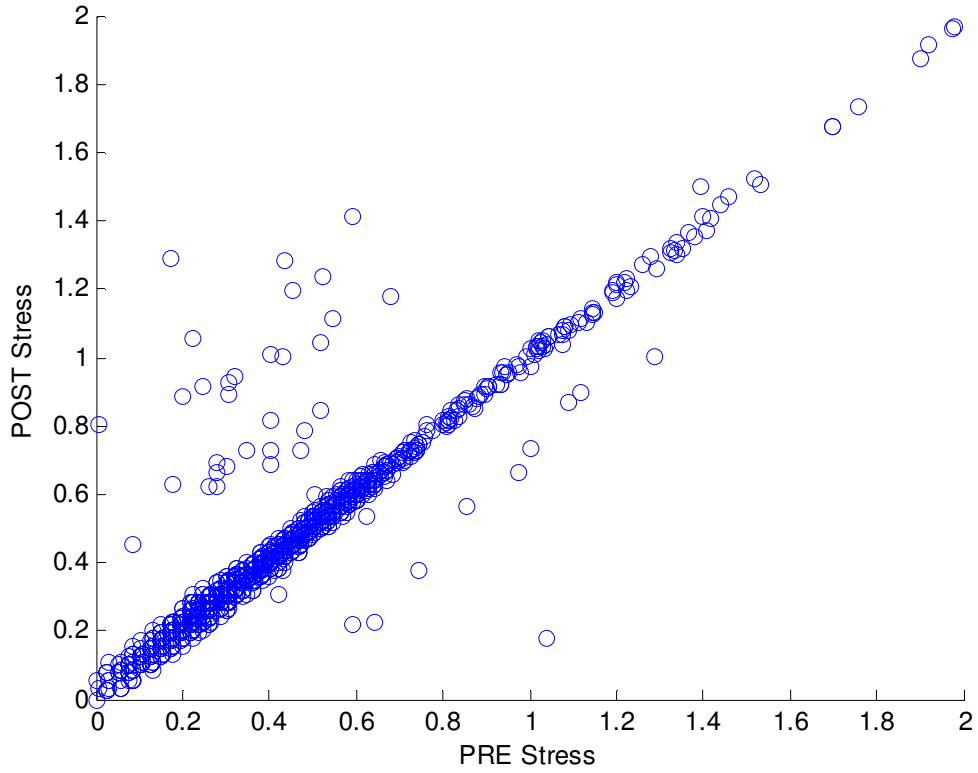


Figure 13. Pre vs. post stress normalized I_{DDQ} scatter plot

Figure 13 shows that most of the pre and post stress measurements fall on the $x=y$ line, with a small guard band around it. These chips did not have any significant shift in their I_{DDQ} measurements. The data points above the line are chips in which the leakage current increased after stress and the points below the line are healer chips, which have lower I_{DDQ} after stress. Both the pre and post stress data is used in the

analysis as two different test vectors because of their combined ability to identify defective chips. Pre stress data is referred to as vectors 1-10 and post stress is referred to as vectors 11-20. For classic I_{DDQ} analysis methods, analysis is performed on the pre and post stress data separately and the results are combined.

4.3 Statistical Information about Test Data

Table I shows the correlation matrix between the I_{DDQ} measurements of different vectors for wafer 1. The post stress vectors are not included in this table because of their similarities with the pre stress data.

Table I. Correlation matrix of wafer 1 pre stress vectors

Vector	1	2	3	4	5	6	7	8	9	10
1	1	0.7117	0.7361	0.9545	0.9727	0.9829	0.9712	0.9786	0.8952	0.9724
2	0.7117	1	0.5231	0.7066	0.708	0.7196	0.7112	0.7161	0.6456	0.7164
3	0.7361	0.5231	1	0.7571	0.7347	0.7421	0.7336	0.7367	0.7277	0.7352
4	0.9545	0.7066	0.7571	1	0.9671	0.9615	0.9594	0.9596	0.8982	0.9605
5	0.9727	0.708	0.7347	0.9671	1	0.9767	0.9778	0.9808	0.9036	0.9695
6	0.9829	0.7196	0.7421	0.9615	0.9767	1	0.9776	0.9823	0.8922	0.9802
7	0.9712	0.7112	0.7336	0.9594	0.9778	0.9776	1	0.9821	0.8873	0.9709
8	0.9786	0.7161	0.7367	0.9596	0.9808	0.9823	0.9821	1	0.8968	0.972
9	0.8952	0.6456	0.7277	0.8982	0.9036	0.8922	0.8873	0.8968	1	0.8804
10	0.9724	0.7164	0.7352	0.9605	0.9695	0.9802	0.9709	0.972	0.8804	1

One can observe from Table I that all the test vectors except vectors 2 and 3 are highly correlated with each other. Vectors 2 and 3 do not have high correlation with any of the other test vectors, except their corresponding post stress vector (not displayed). Many of the wafers in the test data follow a correlation structure similar to Table I. Table II shows the correlation matrix of wafer 3, in which none of the test vectors are highly-

correlated. Wafer 4 has a similar correlation structure. This indicates that there can be significant variation in the behavior of ICs on different wafers. For this reason, the test data analysis is performed wafer-by-wafer.

Table II. Correlation matrix of wafer 3 pre stress vectors

Vector	1	2	3	4	5	6	7	8	9	10
1	1	0.3457	0.4611	0.5108	0.4148	0.4678	0.4886	0.3783	0.4924	0.5133
2	0.3457	1	0.5927	0.4204	0.3938	0.5345	0.5556	0.4405	0.5276	0.5278
3	0.4611	0.5927	1	0.5797	0.4595	0.6493	0.6528	0.4909	0.6802	0.6472
4	0.5108	0.4204	0.5797	1	0.3919	0.5463	0.5347	0.4043	0.5583	0.5649
5	0.4148	0.3938	0.4595	0.3919	1	0.4904	0.4923	0.3319	0.4657	0.4412
6	0.4678	0.5345	0.6493	0.5463	0.4904	1	0.7348	0.5733	0.7277	0.7387
7	0.4886	0.5556	0.6528	0.5347	0.4923	0.7348	1	0.5826	0.7428	0.7116
8	0.3783	0.4405	0.4909	0.4043	0.3319	0.5733	0.5826	1	0.5398	0.5161
9	0.4924	0.5276	0.6802	0.5583	0.4657	0.7277	0.7428	0.5398	1	0.7467
10	0.5133	0.5278	0.6472	0.5649	0.4412	0.7387	0.7116	0.5161	0.7467	1

4.4 Extreme Outlier Removal

Since the I_{DDQ} data is used as input to principal component analysis, extreme outliers must be removed from that data to maintain the integrity of PCA. Of the different methods explained before, the Tukey test was used to remove extreme I_{DDQ} values. The Tukey test analyzes the data on a vector-by-vector basis and sets different limits for each vector, but uses the same Tukey coefficient. As a recap, a value x is considered to be an outlier if

$$x > UQ + k \cdot IQR$$

where k = 3.5, UQ is the upper quartile and IQR is the inter-quartile range. The lower bound was not considered because we do consider low I_{DDQ} values in this research. The

Tukey test was chosen because of its simplicity, ease of implementation and normality of the test data over the *IQR*. A *k* value of 3.5 was chosen to allow for a loose limit (1.5 corresponds approximately to the 3σ limit for normal data) that would still reject extreme values. Figures 14 and 15 show the normal probability plots for I_{DDQ} measurements of the first vector on Wafer 1, before and after outlier removal.

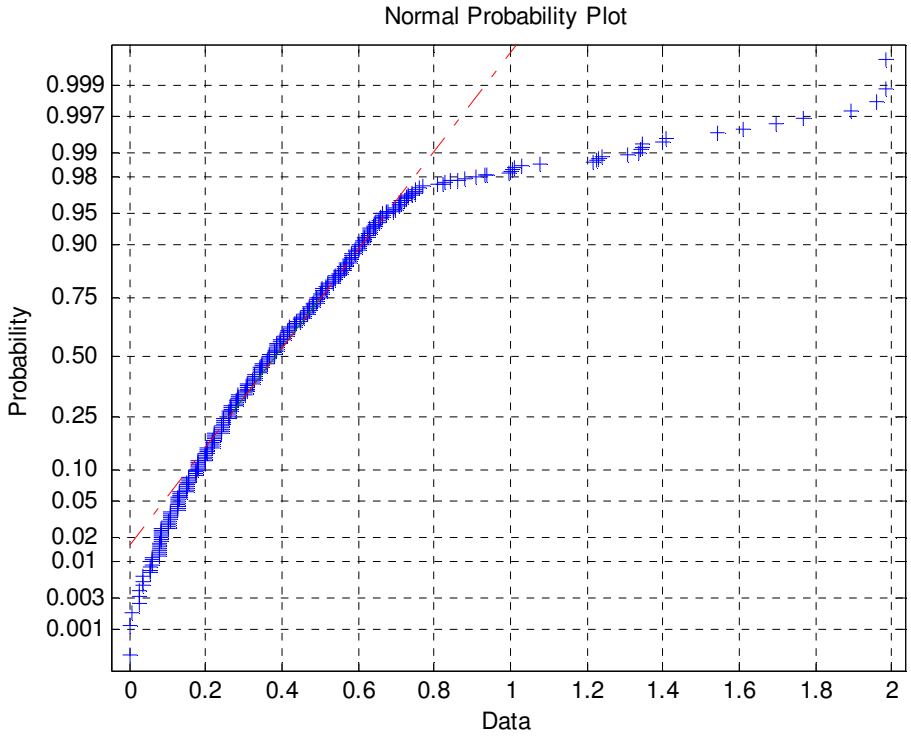


Figure 14. Normal probability plot for normalized I_{DDQ} of wafer 1 vector 1

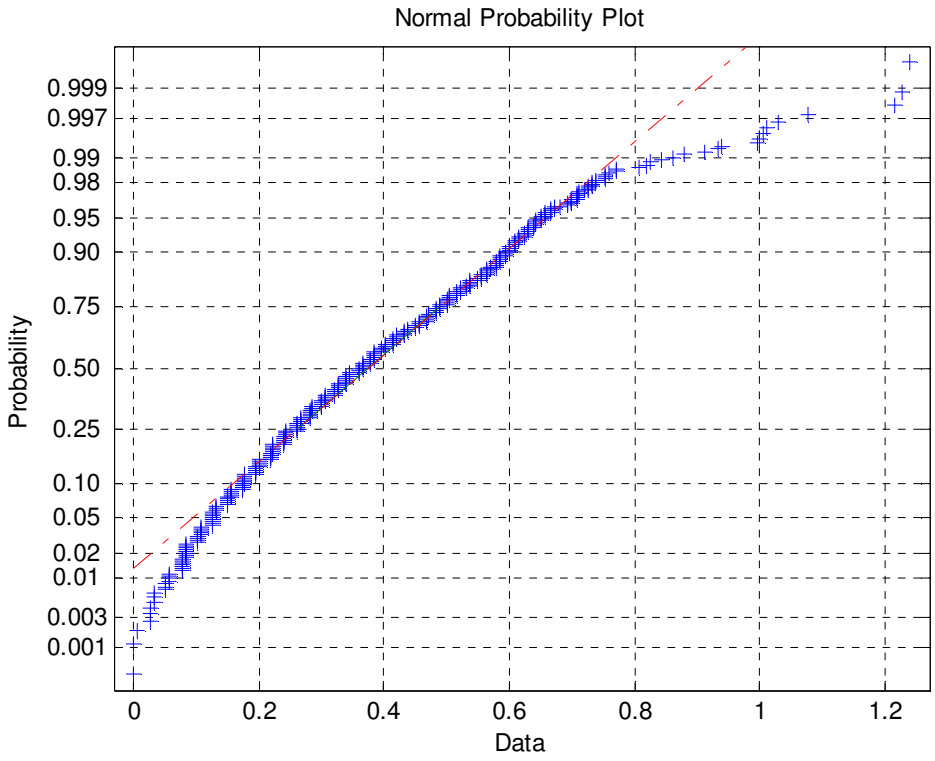


Figure 15. Effect of removing extreme outliers for wafer 1 vector 1

Spatial analysis using NNR with outliers rejected using the Tukey test with a coefficient of *k=3.5,* was also performed on the input data after removal of Tukey outliers. The idea behind this was that any chip that is an extreme spatial outlier is also an obvious outlier. For this case, spatial analysis did not identify any extreme outliers. This can be attributed to Tukey outliers being a super set of the extreme spatial outliers.

4.5 PCA

After removing extreme outliers from I_{DDQ} data, PCA was run using the scaled and normalized I_{DDQ} measurements as the input data set.

Table III. Percentage of variance explained by PCA components wafer-by-wafer

Wafer	1	2	3	4	5	6	7	8	9	10
Component 1	83.45	75.59	50.25	55.49	70.78	78.36	78.5	79.75	87.9	75.45
Component 2	6.05	6.26	5.62	5	7.88	7.02	6.15	8.1	3.5	6.1
Component 3	4.85	4.19	4.61	4.68	6.36	5.47	3.8	3.15	2.65	4.1
Component 4	2.2	2.38	4.215	4.86	2.46	1.67	2.05	2.15	1.15	2.55
Wafer	11	12	13	14						
Component 1	76.8	80.15	70.45	84.1						
Component 2	5.65	4.1	5.65	7.1						
Component 3	4.8	3.15	4.5	2.35						
Component 4	2.45	2	3.45	1.9						

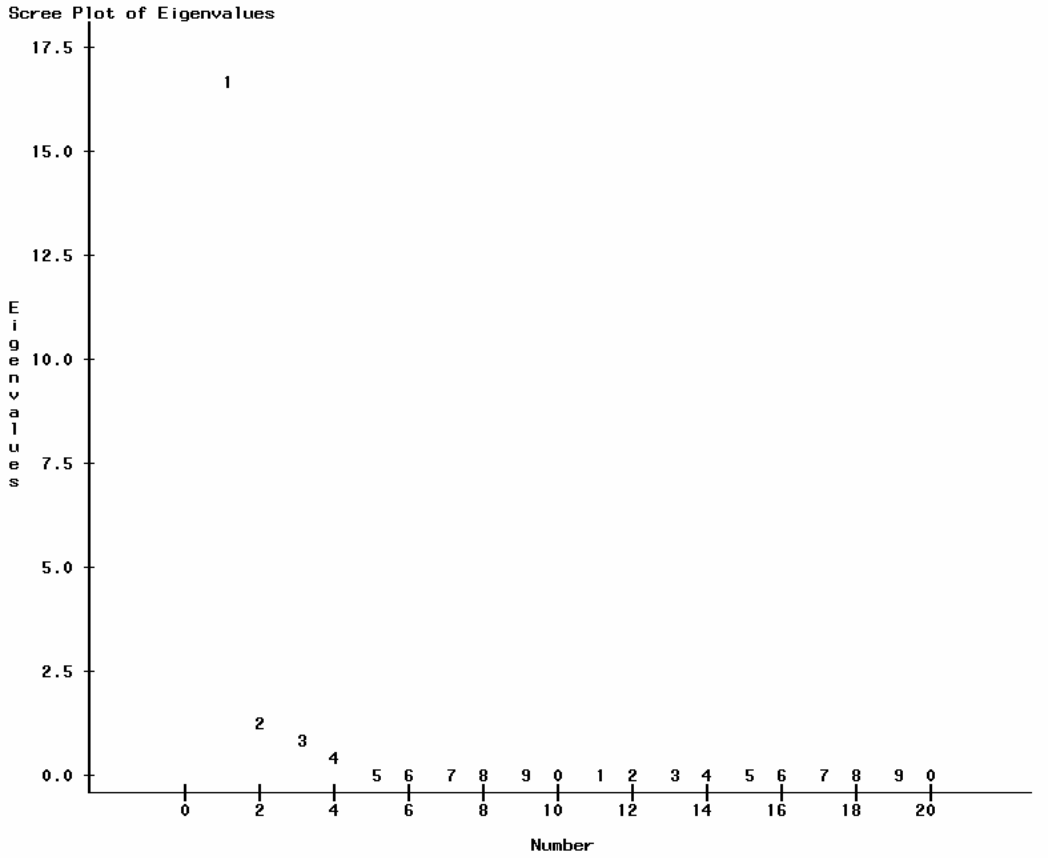


Figure 16. Scree plot of eignevalues for wafer 1

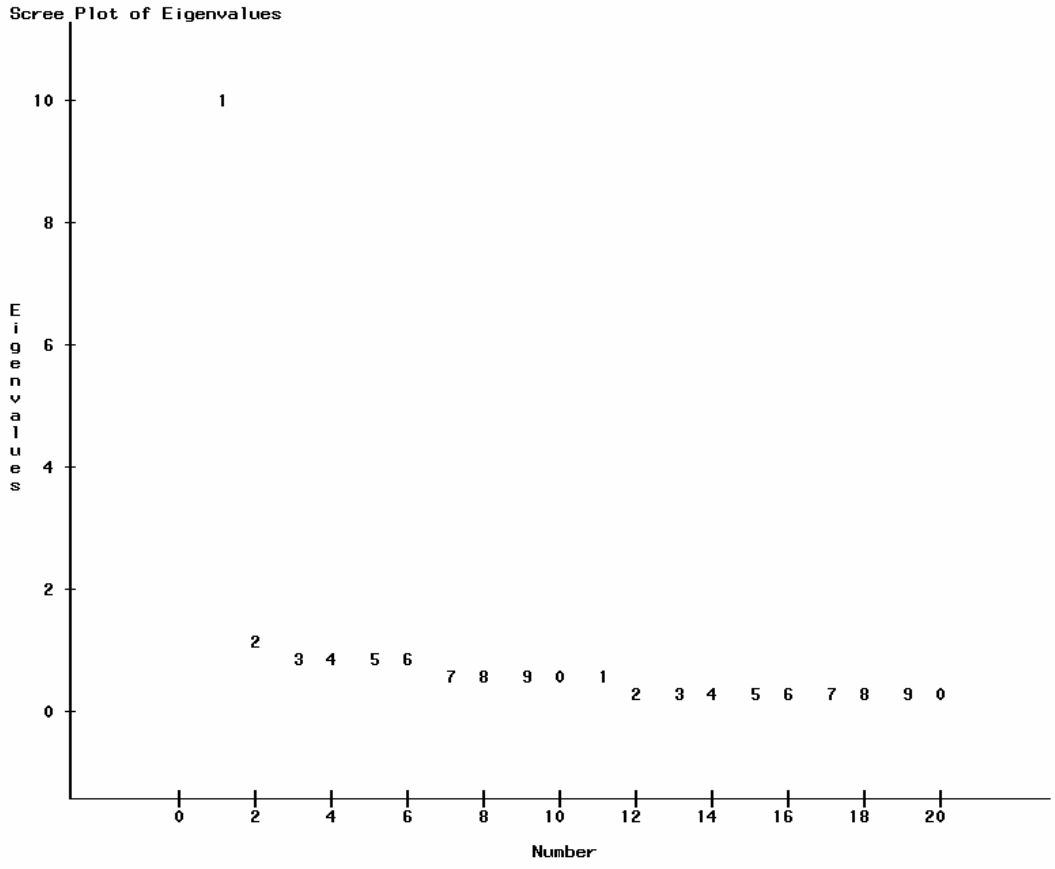


Figure 17. Scree plot of eigenvalues for wafer 3

Table III lists the percentage of variance in the original data explained by the first four components output by PCA. For most wafers, the first component explains most of the variance. This can be expected because of the high correlations between the I_{DDQ} measurements of most of the test vectors. The first component for wafers 3 and 4 explains only about 50% of the variance. This is because of the poor correlation between the I_{DDQ} of different test vectors for these wafers. Figures 16 and 17 show the Scree plot for wafers 1 and 3. The Scree plot explains the significance of the different components.

PCA outputs 20 components because there are 20 test vectors in the input data. The first two components for each wafer were identified as significant using the Scree test. The addition of chip X and Y location as inputs to PCA was evaluated, but it did not significantly increase the variance explained by the components.

4.6 Component Identification

Figures 18 and 19 show the surface plots of several vectors in wafers 1 and 3. They also contain the surface plot of the significant components. Wafers 1 and 3 are used here because they are representative of the structure of data present in the remaining wafers.

It can be observed from the surface plots that the first component looks similar to the surface plots of vectors in both wafers. The first component based on the figures can be labeled as the expected I_{DDQ} at any given location considering I_{DDQ} of all test vectors. This component can be assumed to explain the effects of SCE. The second component is more difficult to identify and label. The second component tries to explain the variance in the I_{DDQ} measurements for the test vector with the most variance. For example, in wafer 1, component 2 extracted information about vector 2.

4.7 Variance Reduction

The factor pattern, factor score and factor loadings output by PCA are for the standardized input I_{DDQ} data. As a result, all the following plots are based on analysis of standardized data. The variance for each standardized vector is 1 for any wafer.

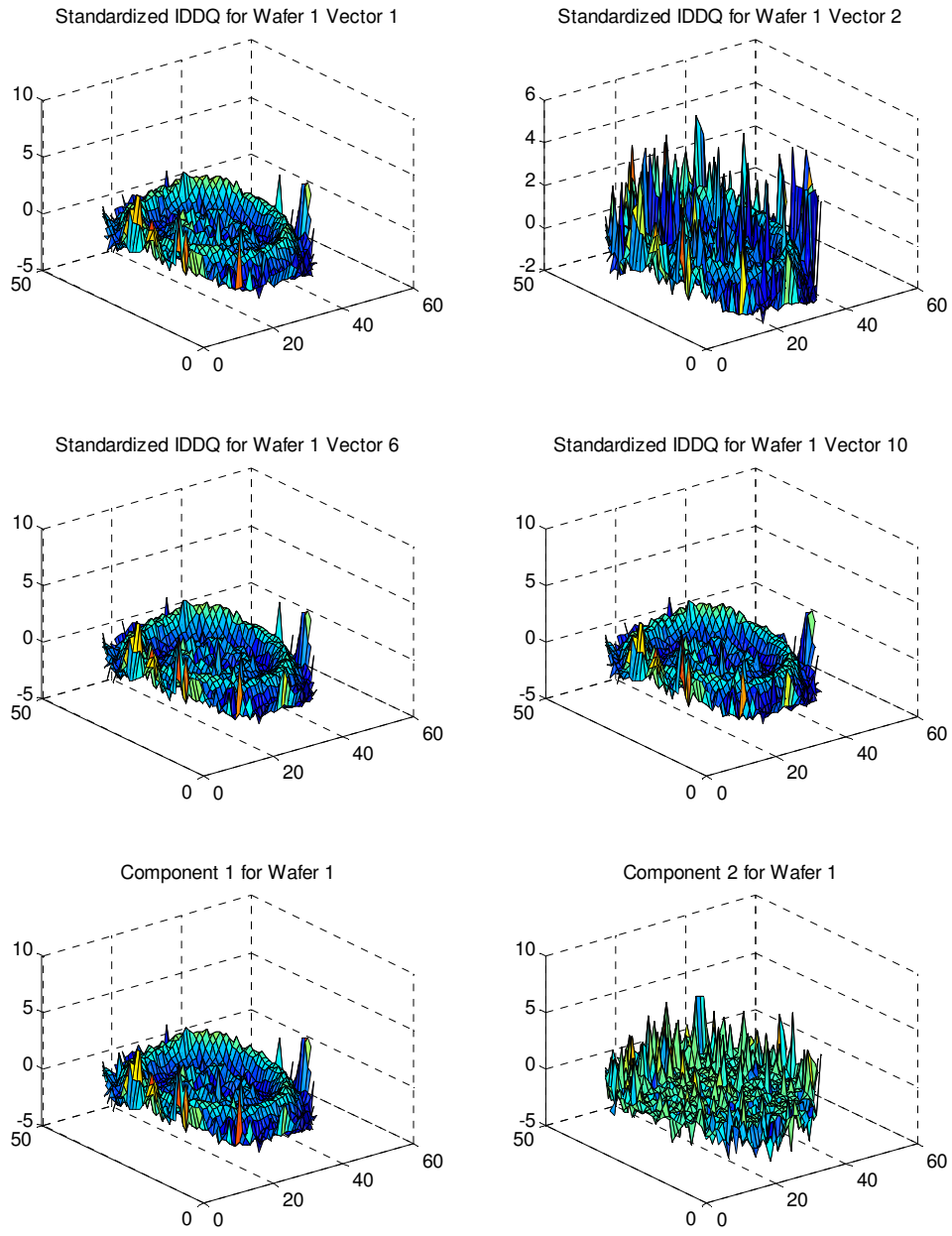


Figure 18. Surface plot of wafer 1 I_{DDQ} and significant components

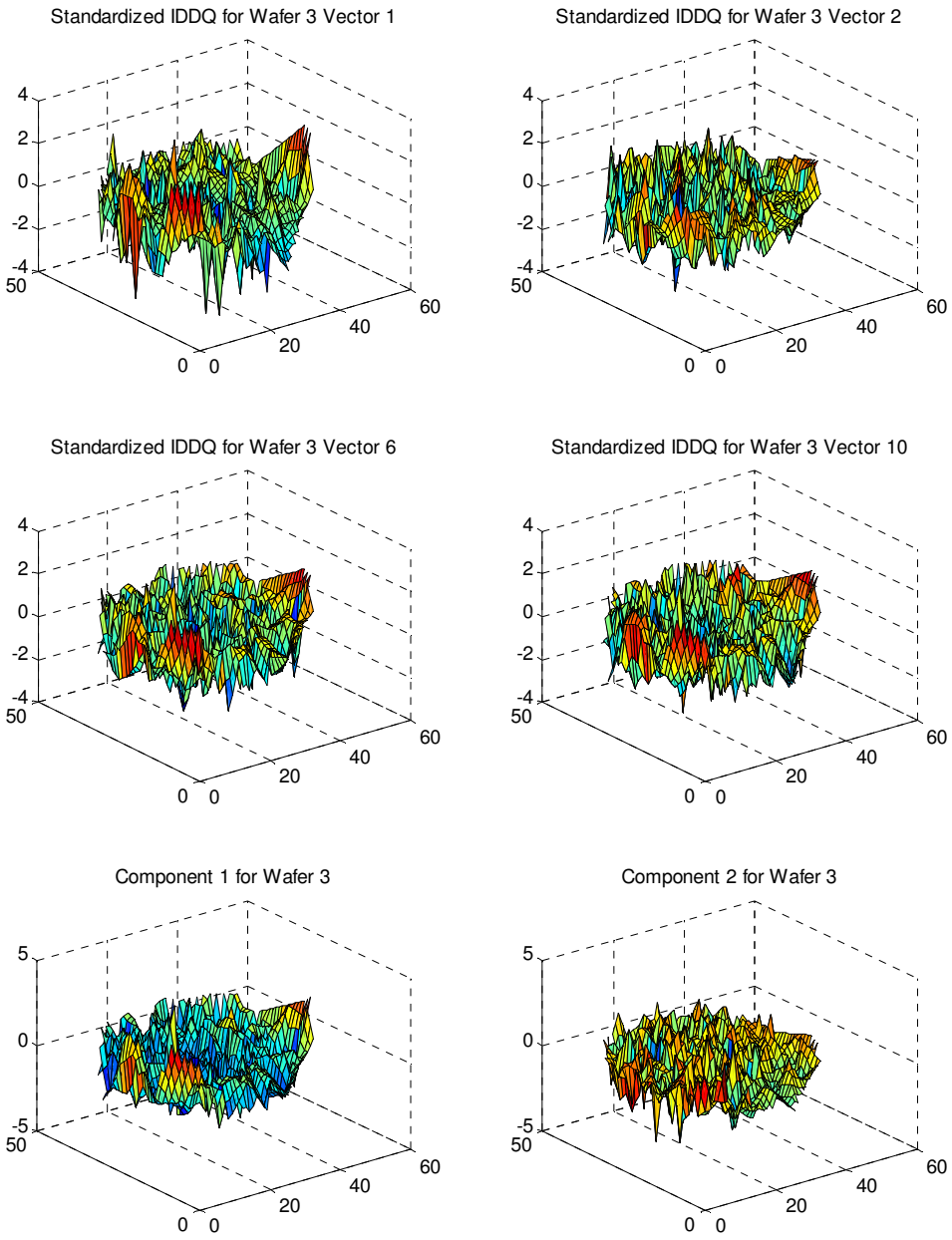


Figure 19. Surface plots of wafer 3 I_{DDQ} and significant components

Table IV. Variance of reduced vector data for wafers 1 and 3

	Vector 1	Vector 2	Vector 3	Vector 4	Vector 5	Vector 6	Vector 7	Vector 8	Vector 9	Vector 10
Wafer 1	0.0493	0.1974	0.3136	0.0716	0.0426	0.0369	0.0416	0.0398	0.2147	0.0456
Wafer 3	0.6813	0.2272	0.4026	0.6083	0.7258	0.3203	0.3215	0.6544	0.3192	0.3104

The proposed variance reduction method creates reduced test data, with the I_{DDQ} of each vector reduced. Table IV shows the variance of the reduced data. For wafer 1, the variance reduces considerably for all vectors except for 2, 3 and 9, which have less correlation with other vectors. Variance reduction for wafer 3 achieves some reduction, but not comparable to wafer 1. This can again be attributed to the lack of high correlations between the I_{DDQ} measurements for the vectors in wafer 3. Figures 20, 21, 22 and 23 give a visual representation of the reduction by displaying the surface plot of the original as well as the reduced I_{DDQ} data along with the normal probability plot.

As observed in Figure 20 for wafer 1 vector 1, the surface plot of the reduced I_{DDQ} values is smooth and without significant variation. The main sources of variation are large positive and negative spikes in the surface plot. The positive spikes are due to defective chips. In the normal probability plot of the reduced data for wafer 1 vector 2, one can observe that almost 50% of the chips have a reduced data close to zero (between the probability range of 0.25 to 0.75). This shows that the prediction for vector 2 through PCA is accurate for 50% of the data.

For wafer 3, no significant inferences can be made from observing the reduced data in Figures 22 and 23.

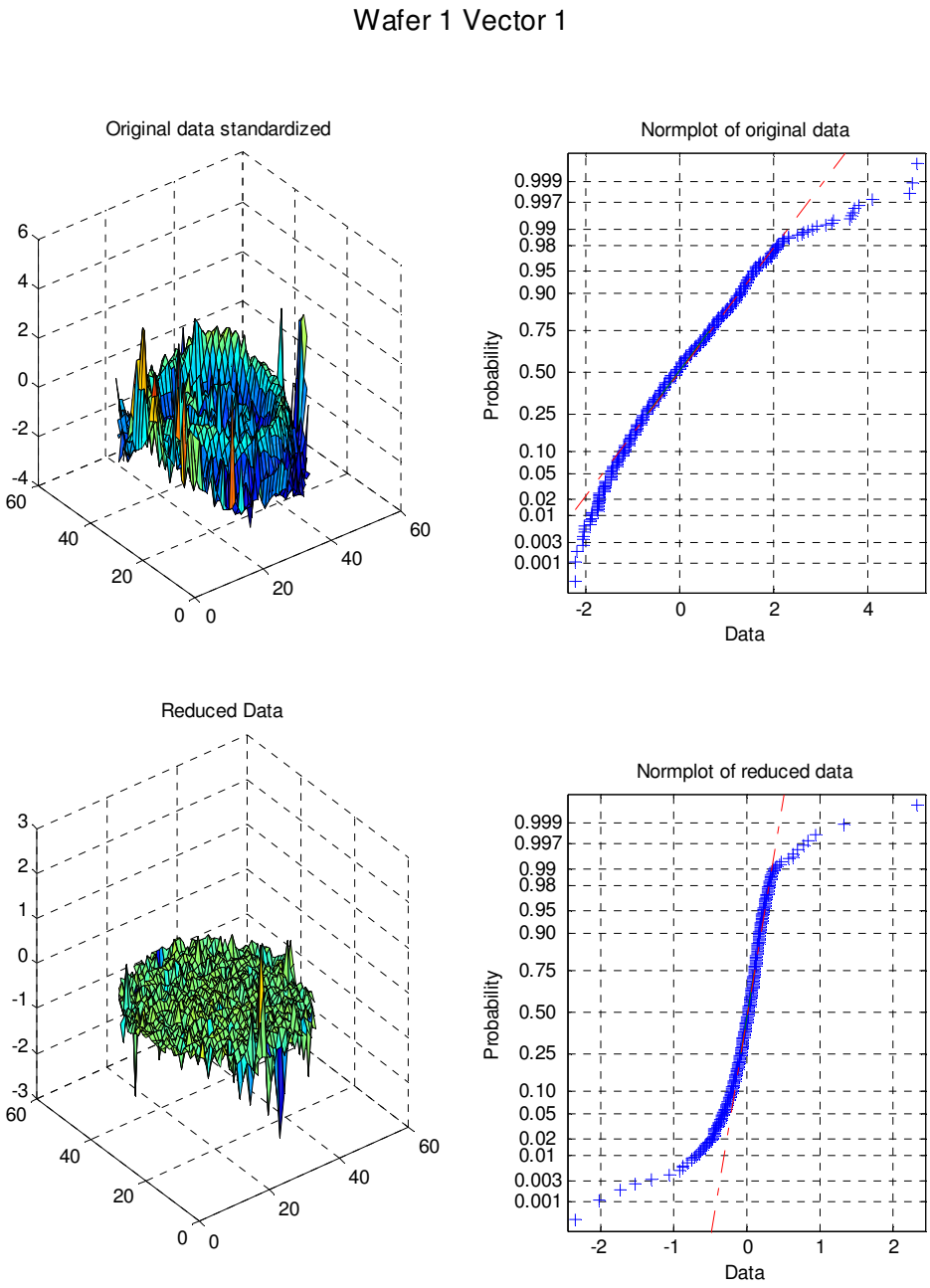


Figure 20. Variance reduction for wafer 1 vector 1

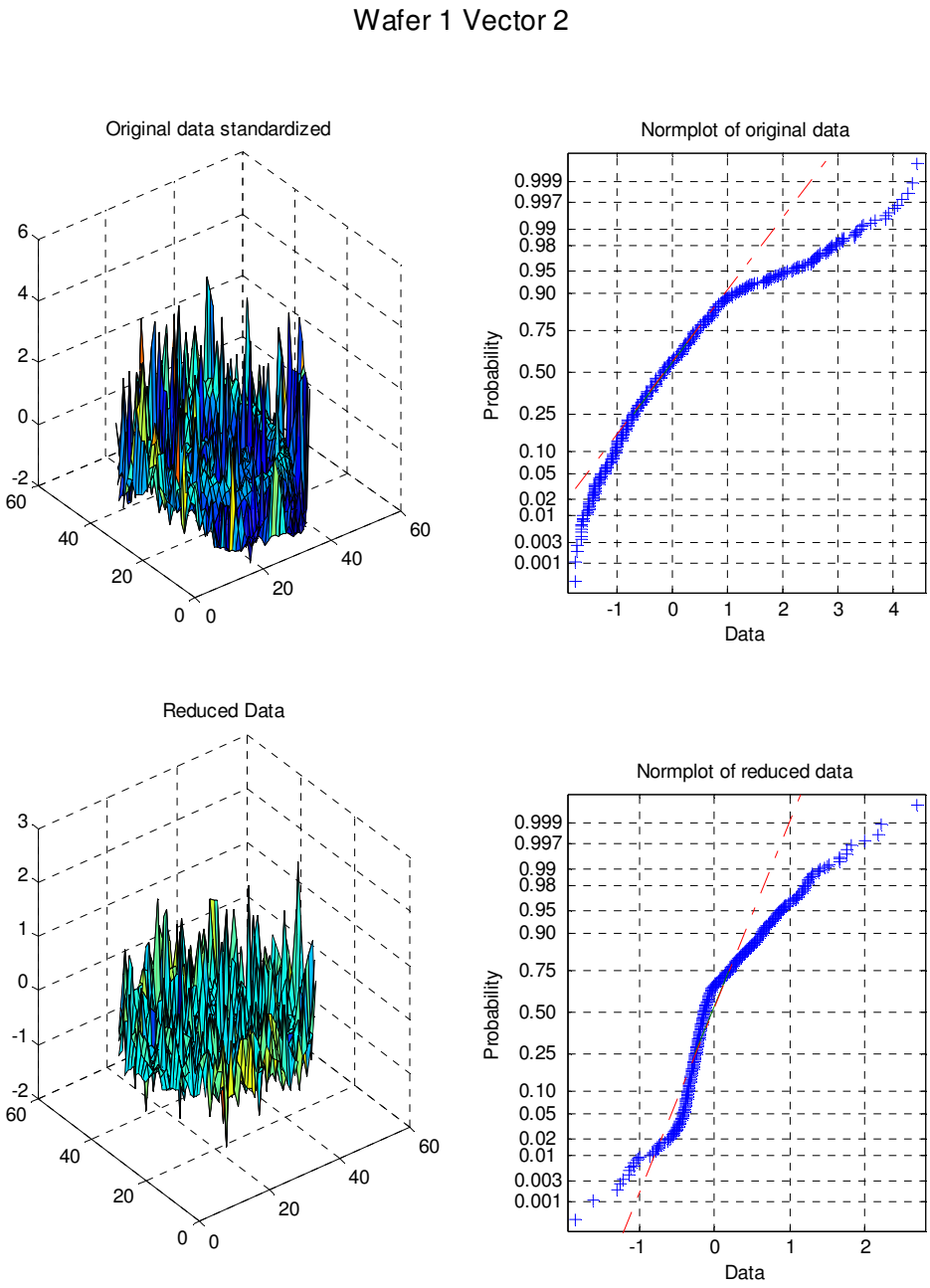


Figure 21. Variance reduction for wafer 1 vector 2

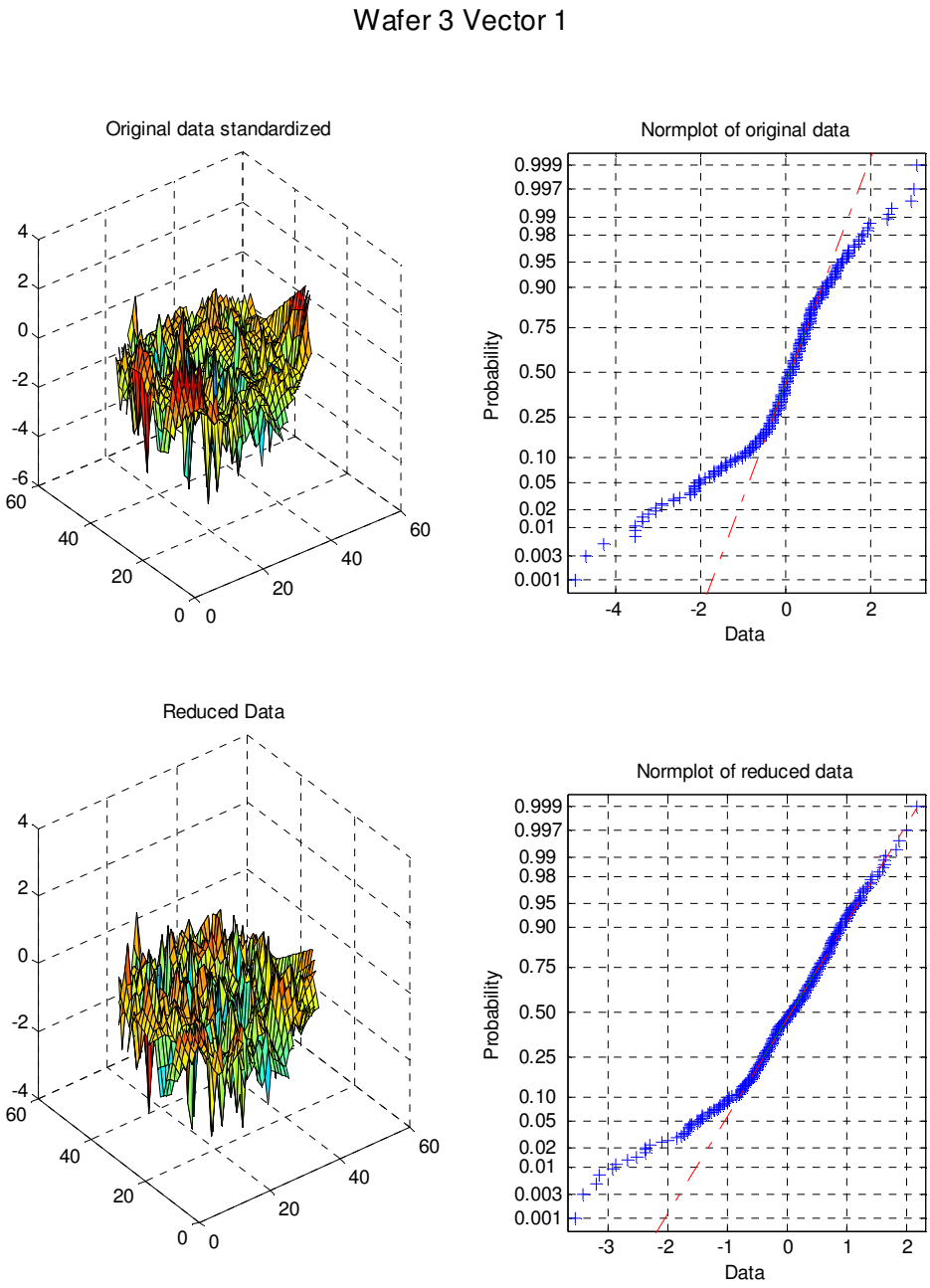


Figure 22. Variance reduction for wafer 3 vector 1

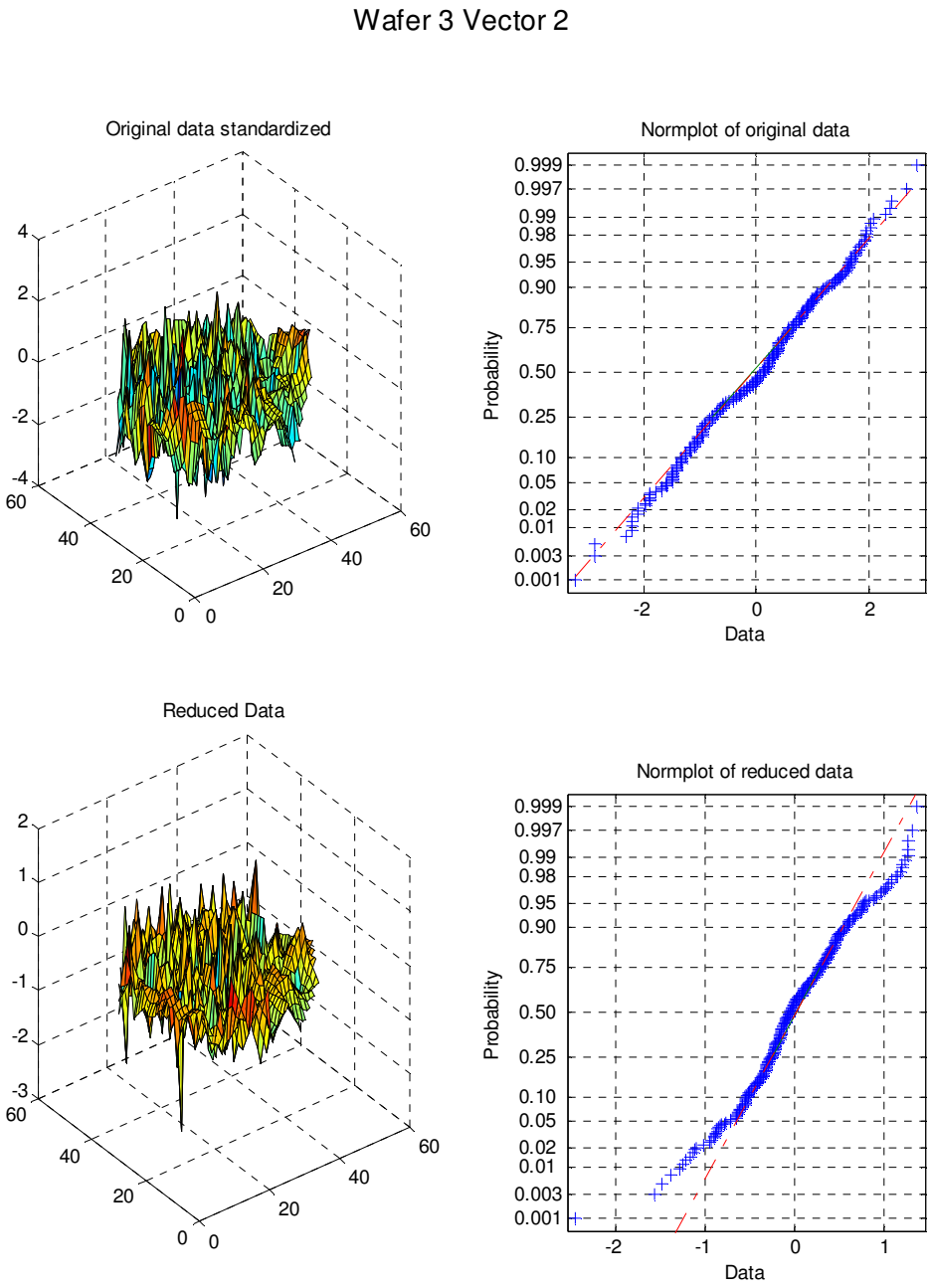


Figure 23. Variance reduction for wafer 3 vector 2

4.8 Outlier Identification

In order to identify defective chips in the input data, outlier analysis needs to be performed on the reduced data as well as the first and second components. All the plots in this subsection are with respect to the standardized I_{DDQ} data.

4.8.1 Detecting Chips with Passive Defects

The components represent the variance expected for all the chips in a wafer for all test vectors. Outlier analysis on the first and second components identifies passive defects. A combination of Tukey test and spatial analysis was used to analyze the components. The Tukey test classifies a chip as defective if its measurement for either component is too high. A Tukey coefficient of $k=1.75$ was used for the first component and $k=2$ was used for the second component. These values were set based on visual observation of the data. The coefficients can be adjusted to trade between yield and defect level.

The output of the Tukey test is then subjected to spatial analysis to identify spatial outliers that do not conform to its neighbors. Tukey is performed before spatial analysis, in order to reject outliers that would distort the spatial analysis. NNR was used for the wafer level spatial analysis. After finding the residuals in NNR, a Tukey test with coefficient k=2.5 was used to remove outliers. Eight neighbors of a chip were chosen from a 5x5 square matrix around it, with the chip under analysis being in the center of the square. Correlations between the center chip and the neighboring chips were

computed. The top eight neighbors for which there is I_{DDQ} data are used in the NNR analysis. Fewer neighbors are used if eight are not available.

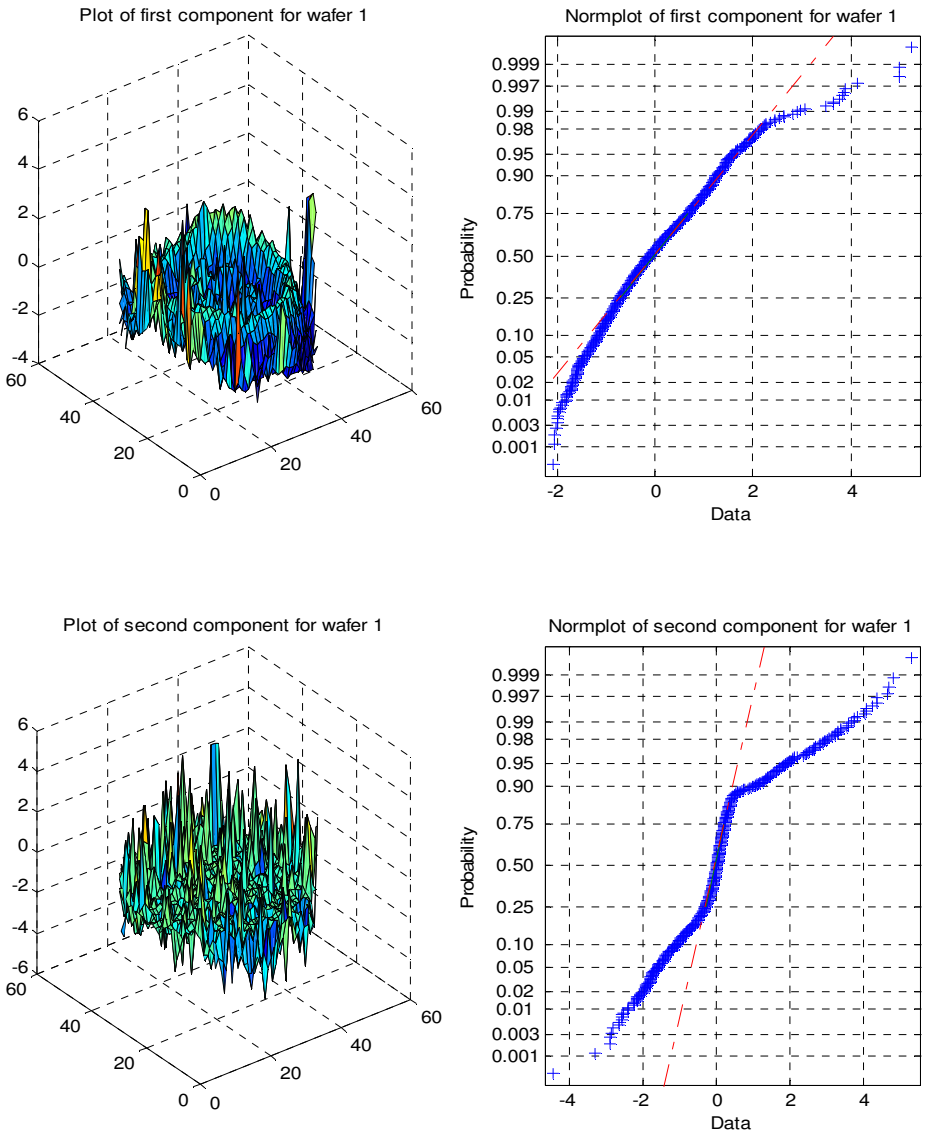


Figure 24. Surface and normality plot of first two components of wafer 1

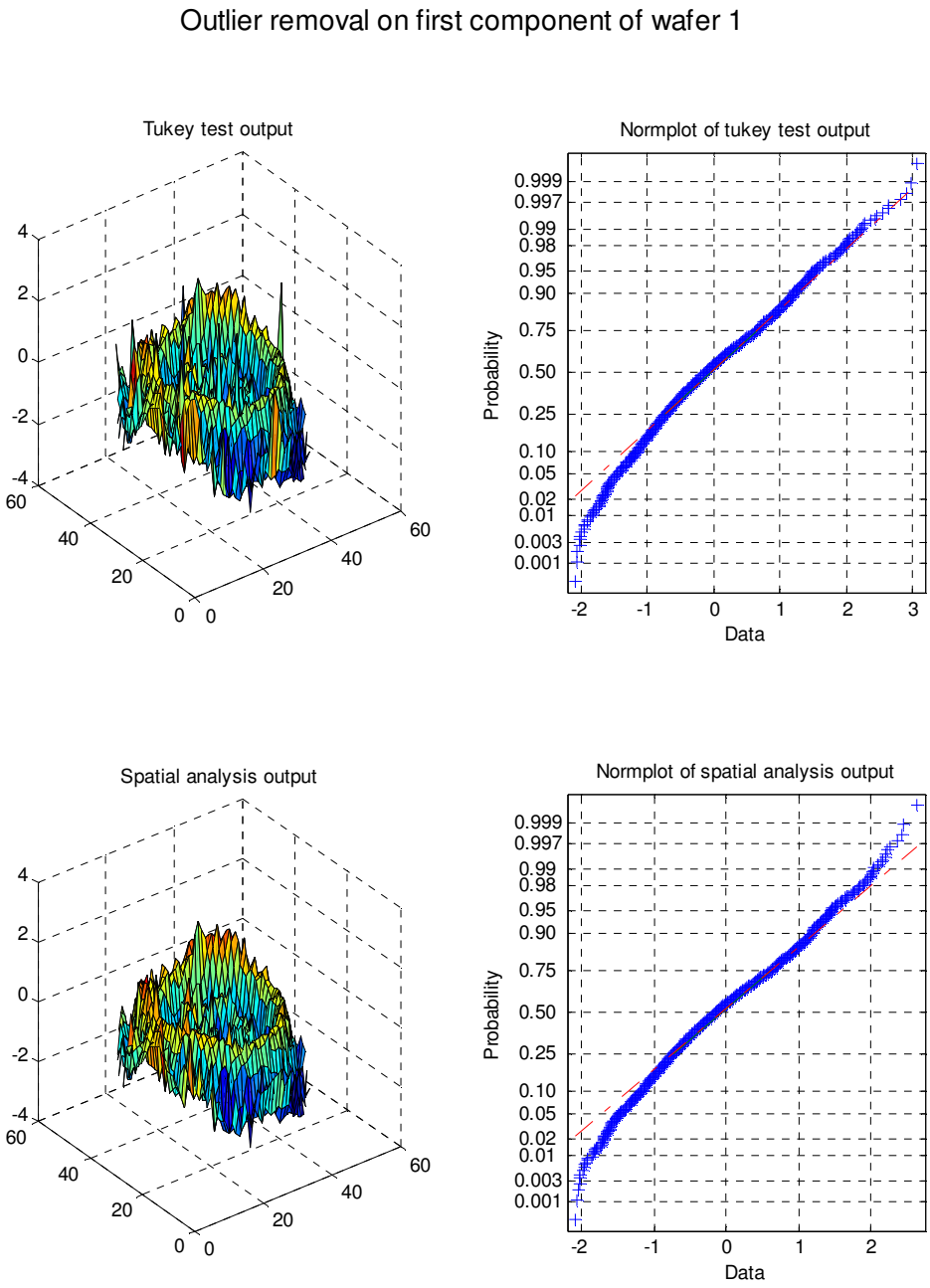


Figure 25. Outlier analysis on first component of wafer 1

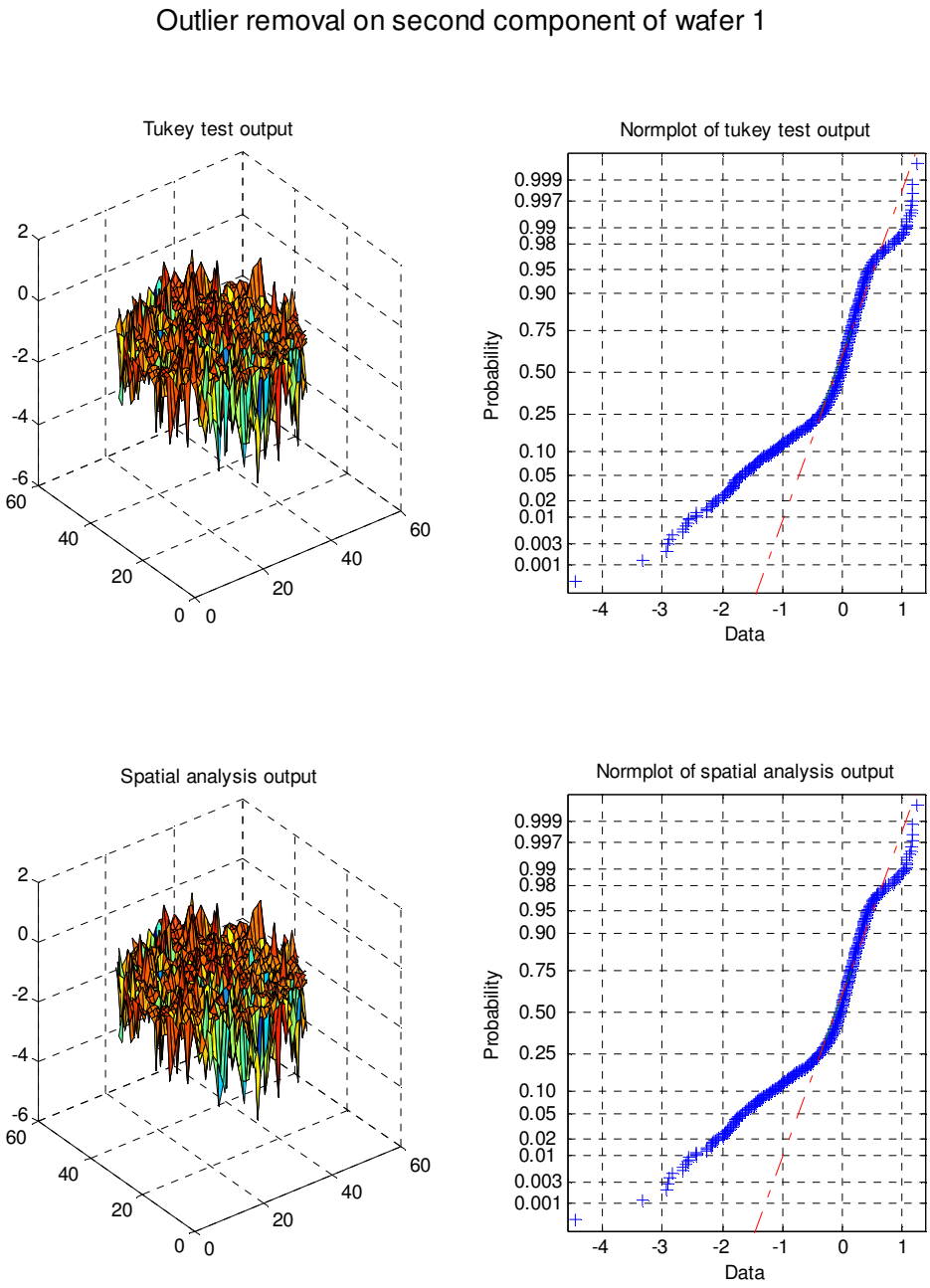


Figure 26. Outlier analysis on second component of wafer 1

Figures 24 – 26 are visual representations of the outlier analysis performed on the components for wafer 1. Outlier analysis of the first component for wafer 1 rejected 26 out of 1340 chips (tukey test rejected 11 and spatial analysis rejected 15). The surface plots of Figure 24 give an idea of the kind of outliers that are caught using spatial analysis. Outlier analysis on the second component rejected 123 out of 1340 chips (tukey test rejected 118 and spatial analysis rejected 5). The second component has a strict threshold because the majority of chips (approximately 75%) have a value very close to zero, reducing the tolerance of the Tukey test.

Figures 27 – 29 are visual representations of the outlier analysis performed on wafer 3. The analysis rejected 2 of 500 chips (Tukey rejected 2 and spatial analysis rejected 0) based on the first component and no outliers were detected in the second components. (Note that wafer 3 has only one-third the voltage test yield of wafer 1). The failure rate for wafer 3 is low because of the high variance in the values for both the components. The total number of chips mentioned here is after the removal of extreme outliers from the data and the number of outliers do not include extreme outliers.

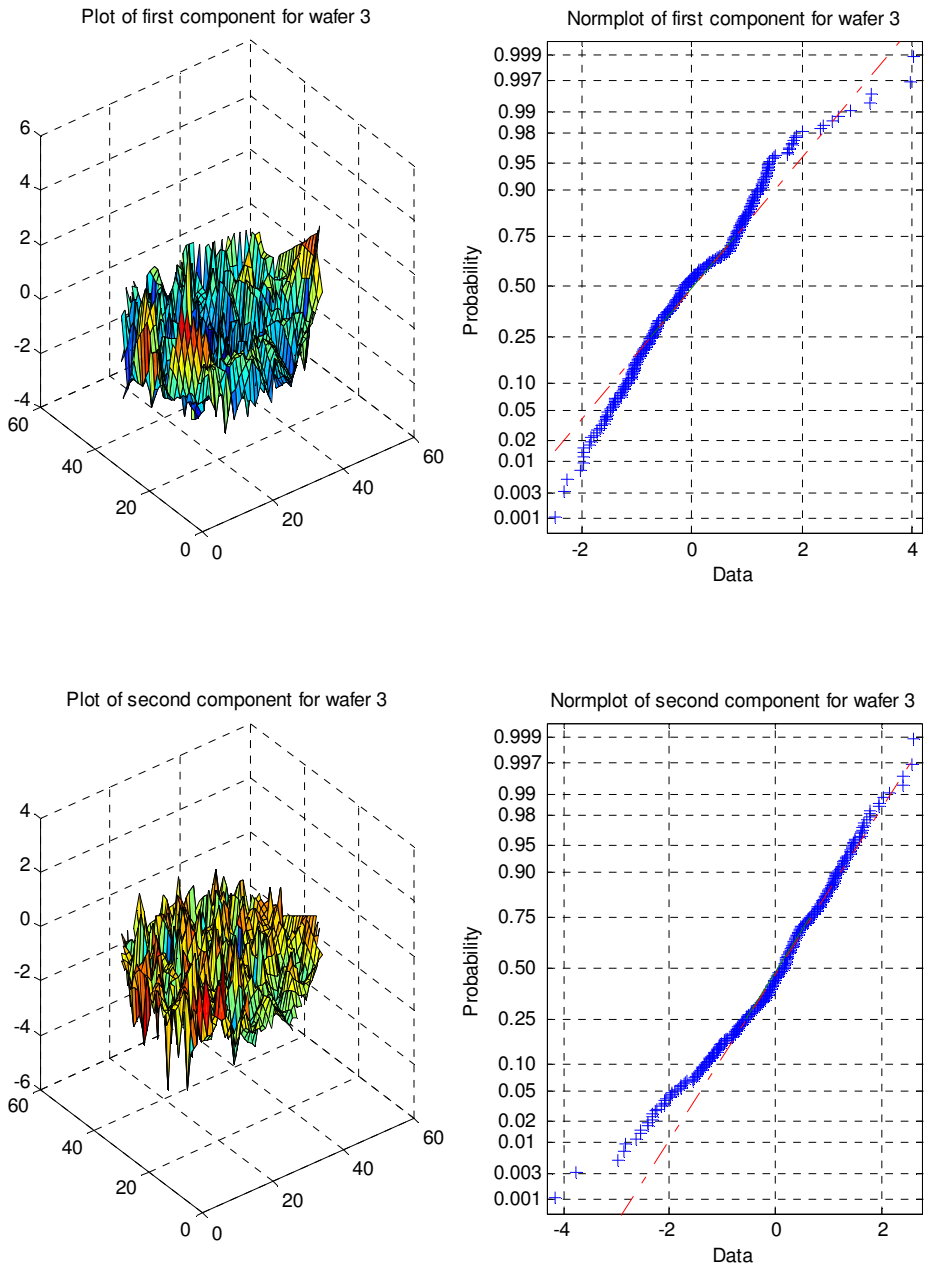


Figure 27. Surface and normality plot of first two components of wafer 3

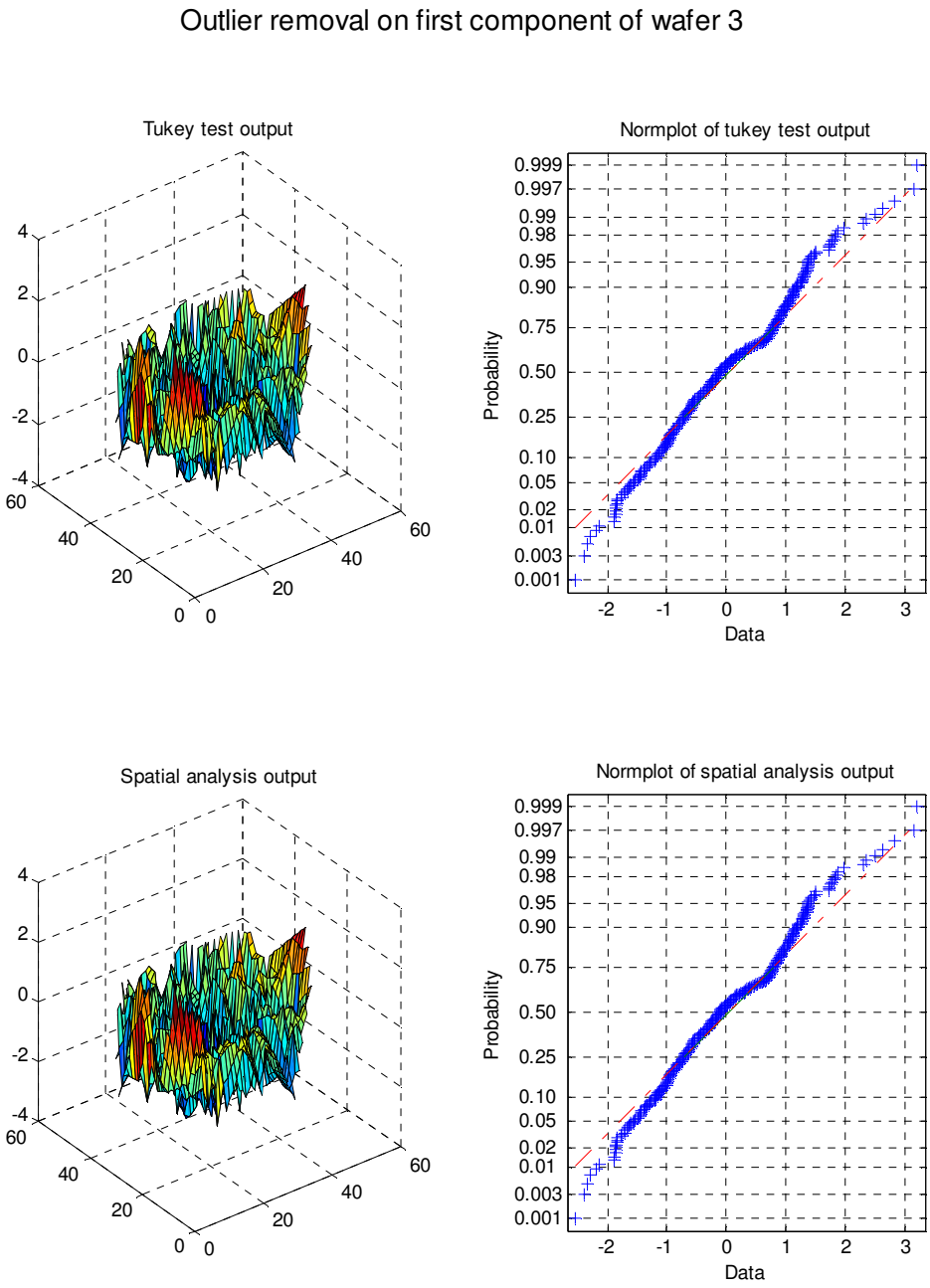


Figure 28. Outlier analysis on first component of wafer 3

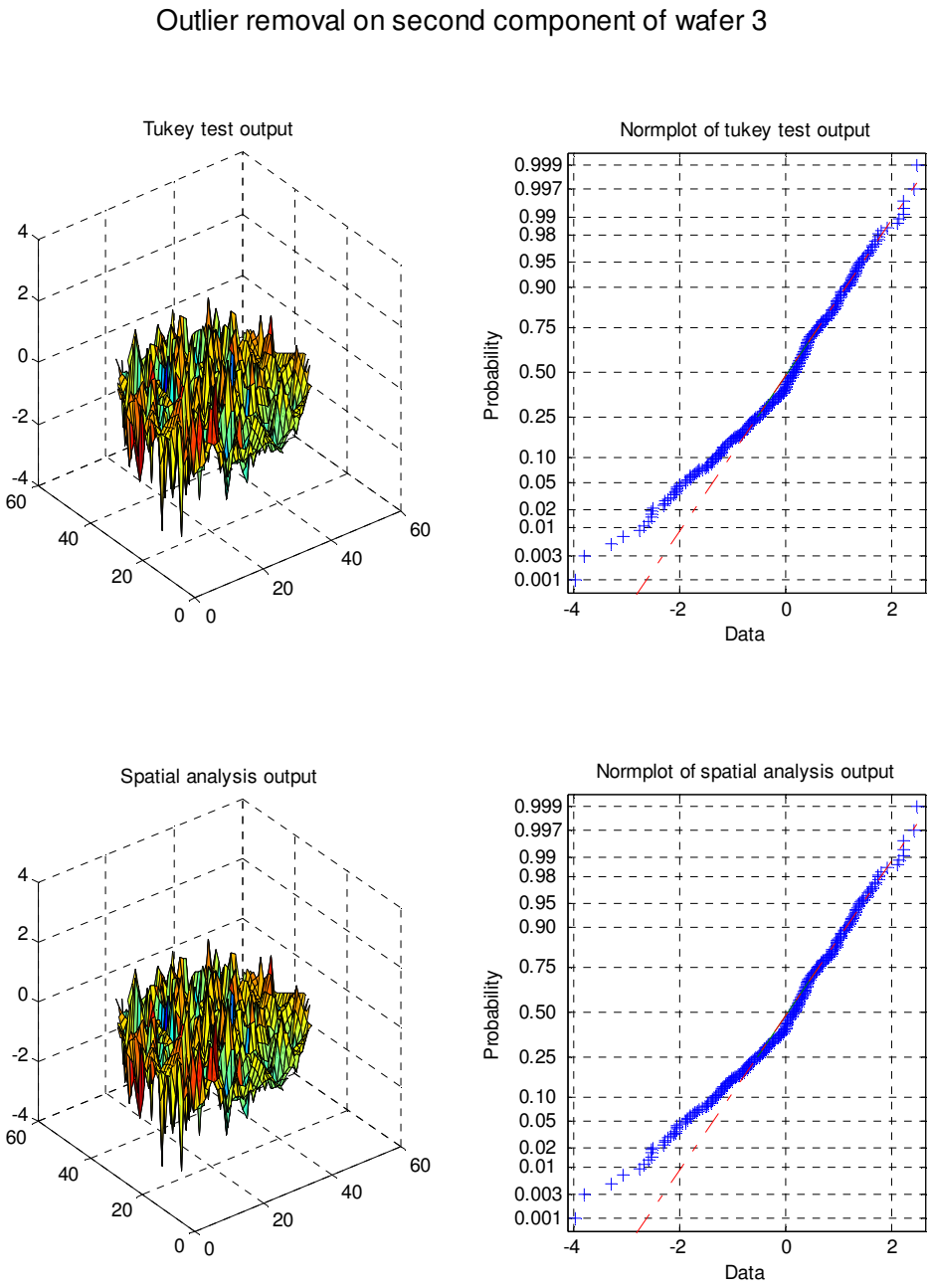


Figure 29. Outlier analysis on second component of wafer 3

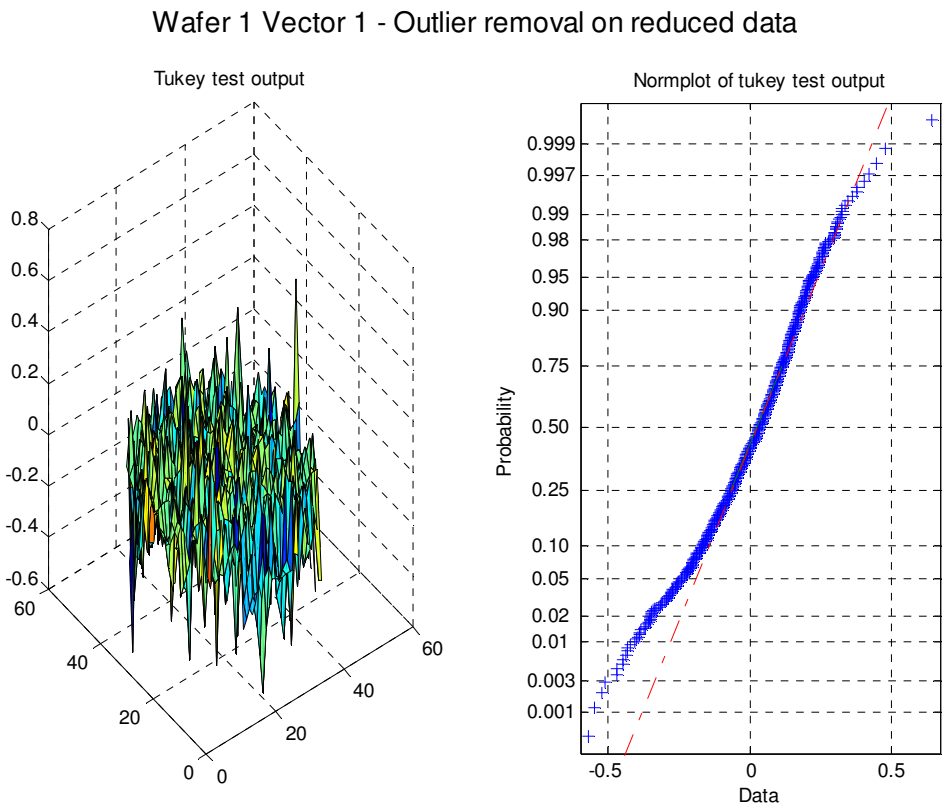


Figure 30. Tukey output for wafer 1 vector 1 reduced data

4.8.2 Detection of Chips with Active Defects

Chips with active defects have higher I_{DDQ} values only for circuit states that sensitize the defect. This increase in I_{DDQ} should affect only some of the vectors and consequently will cause a smaller change in the variance in the original I_{DDQ} measurements. As a result, this defect-induced variance will not be extracted as a part of the significant components. Outlier analysis will have to be performed on the reduced

data to be able to catch these defects. Outliers in the reduced data are identified with the Tukey test using a coefficient of *k=3*.

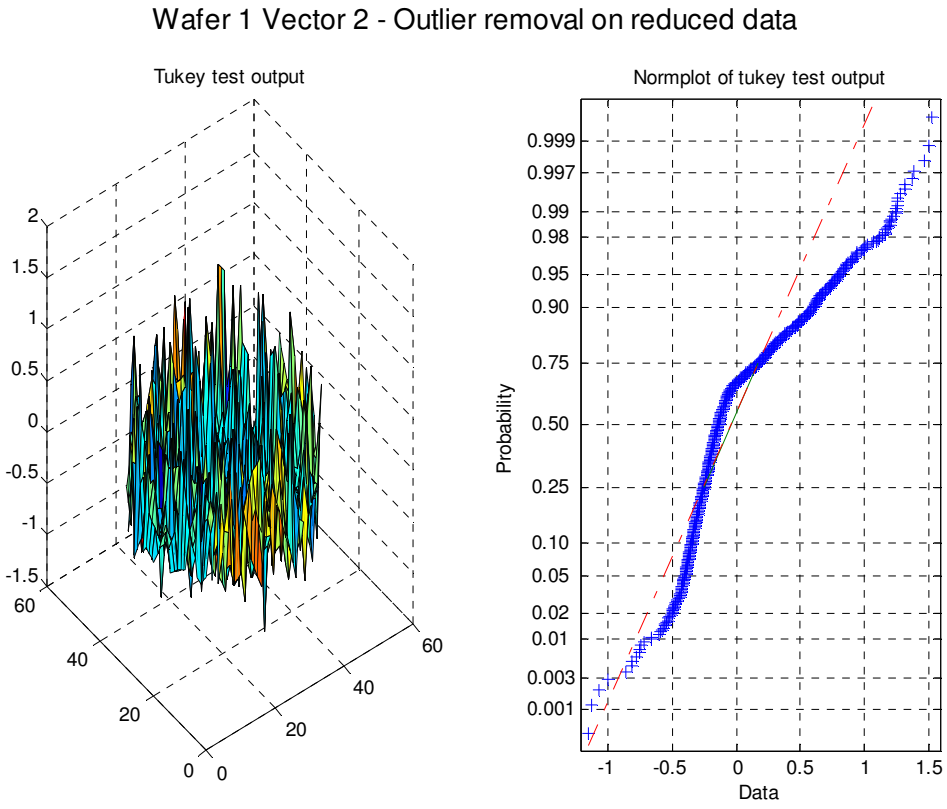


Figure 31. Tukey output for wafer 1 vector 2 reduced data

For most of the wafers and test vectors, the reduced data is similar to the surface plot of wafer 1 vector 1 in Figure 20. The presence of a positive spike in an otherwise smooth surface plot indicates that the original I_{DDQ} measurement for this chip is well above the expected I_{DDQ} computed using the components. These chips can be classified as defective with active defects. The presence of negative spikes in the surface plot

indicates that the measured I_{DDQ} was much lower than the expected value. This can be caused because of the presence of elevated I_{DDQ} chips distorting the model. These kinds of chips are not classified as defective, as any chip with low I_{DDQ} because of a defect will experience significant functional failure, which would have been detected as part of functional tests.

Figures 30 and 31 show the effect of applying the Tukey test to the reduced I_{DDQ} data of wafer 1 for vectors 1 and 2. A total of 61 out of 1340 chips were identified as defective. Figures 32 and 33 show the effect of a Tukey test applied to the reduced data of wafer 3, vectors 1 and 2. In this situation, 26 out of 500 chips are identified as defective.

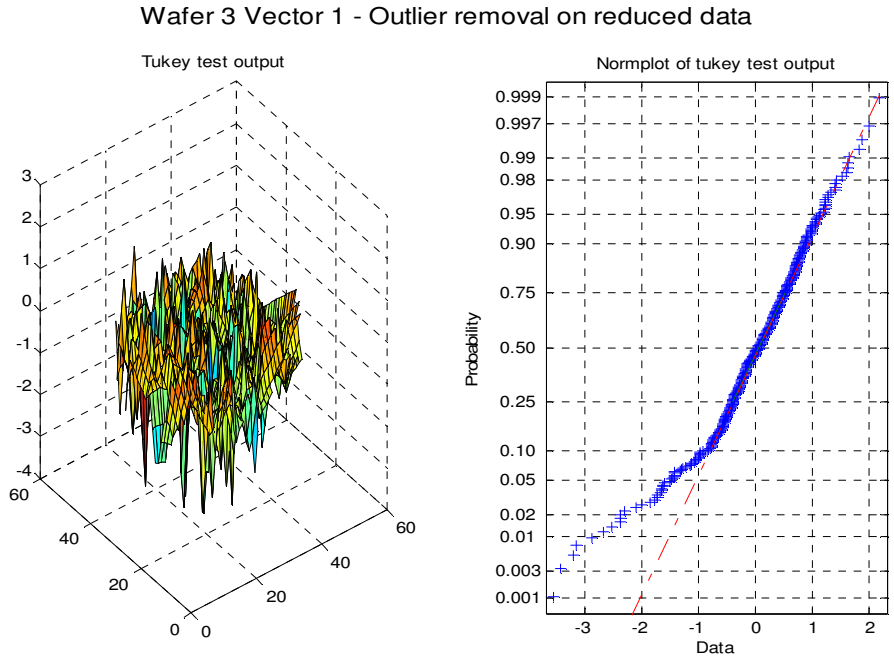


Figure 32. Tukey output for wafer 3 vector 1 reduced data

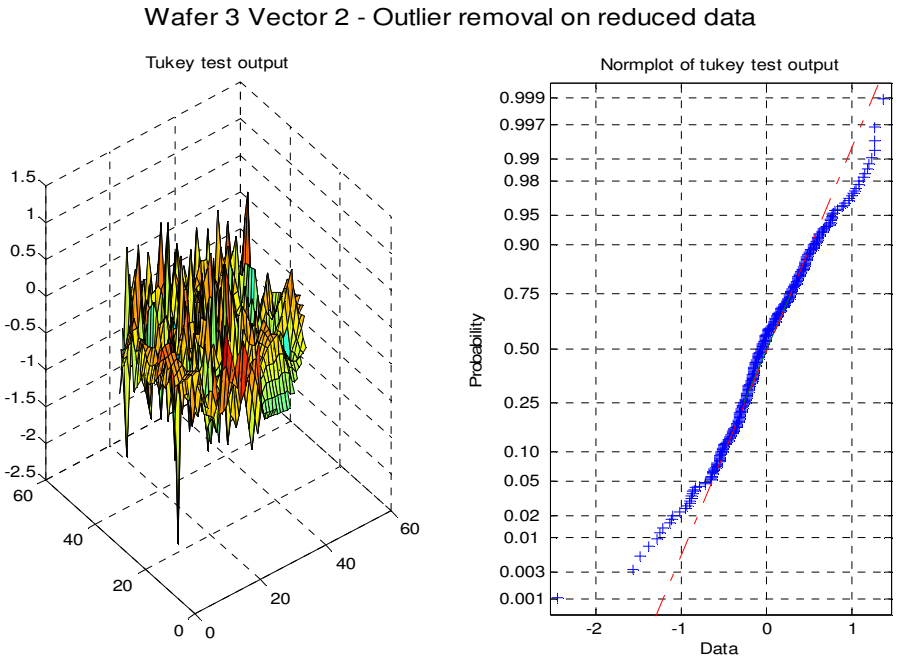


Figure 33. Tukey output on wafer 3 vector 2 reduced data

By observing figures 30 and 31 in comparison with figures 20 and 21, one can observe that chips some chips which have negative residue are still being rejected by tukey test. This is happening because of the presence of a corresponding high residue for this chip in another test vector, which causes tukey to identify and reject it.

4.9 Final List of Outliers

The chips rejected by the proposed method are from three different analysis stages. The first sets of chips rejected are the extreme outliers. The second set of chips rejected is the outliers in the component data. The final sets of chip rejected are outliers

in the reduced data. There can be overlap between chips that fail the analysis on components of PCA and chips that fail because they are outliers in the reduced data.

For wafer 1, 207 out of 1358 chips were identified as defective, including extreme outliers. For wafer 3, 35 out of 507 chips were identified as defective. The locations of the chips that passed voltage test and those chips that were rejected in the analysis of the I_{DDQ} data are shown in Figure 34. As noted earlier, wafer 3 has relatively low yield.

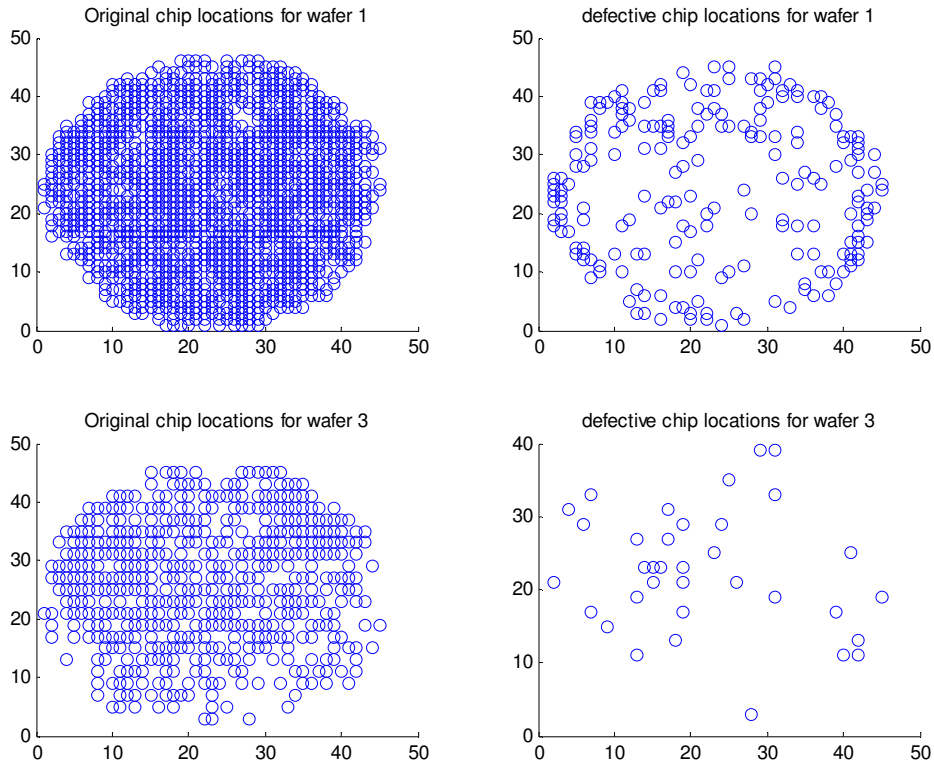


Figure 34. Plots of chip locations/defective chip locations for wafers 1 and 3

4.10 Competitive Analysis

Table V. Summary of number of chips rejected by different methods

Wafer	Total Chips	Proposed Method Failures	NNR Failures	NCR Failures	CR Failures
1	1358	207	46	87	79
2	1176	129	22	67	54
3	507	35	8	18	8
4	456	85	5	13	6
5	1079	178	19	56	38
6	639	70	28	45	26
7	418	87	18	41	17
8	453	92	24	25	20
9	232	35	10	6	7
10	1413	307	66	77	98
11	1349	299	74	72	71
12	1313	253	72	80	67
13	1324	164	65	57	40
14	656	78	13	18	19

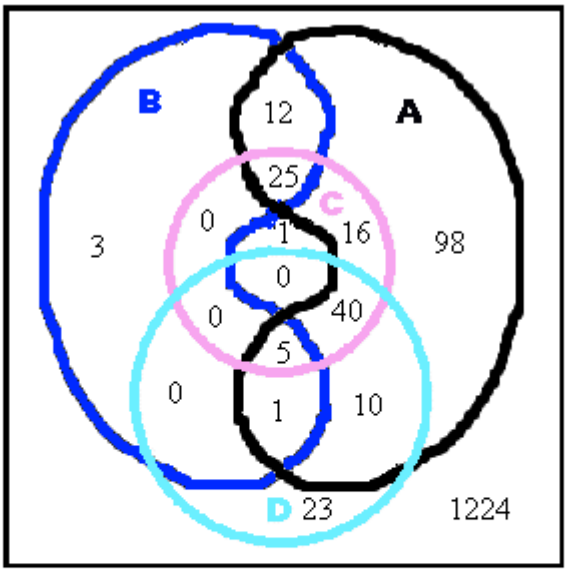
In this section, the proposed outlier analysis method is compared to several widely-published methods. Table V contains a summary of the number of chips identified as defective by the different techniques for each wafer and Table VI contains the number of chips identified as defective uniquely by NNR, NCR and CR when compared against the proposed method. Figure 35 shows the Venn diagram of the number of defective chips identified by the proposed method, NCR, CR and NNR for wafer 1. The sizes of the different regions in the Venn diagram are not indicative of the size of the set. In the absence of actual burn in data, it is very difficult to compare the

performance of different methods, as the final decision about whether a chip is defective or not is subjective.

Table VI. Comparison of proposed method with NCR, NNR and CR

Wafer	Unique NNR Failures	Unique PM Failure vs NNR	Unique NCR Failures	Unique PM Failure vs NCR	Unique CR Failures	Unique PM Failure vs CR
1	3	164	1	121	23	151
2	0	107	9	71	9	84
3	2	29	12	29	4	31
4	0	80	5	77	0	79
5	0	159	0	122	4	144
6	3	45	15	40	9	53
7	3	72	7	53	0	70
8	2	70	0	67	0	72
9	3	28	0	29	0	28
10	8	249	0	230	0	214
11	3	228	1	228	2	230
12	6	187	2	175	5	191
13	11	110	3	110	2	126
14	0	65	0	60	5	64

The following analysis for comparison of the different methods concentrates on wafer 1 vector 2 because most of the chips identified as defective in the proposed method for wafer 1 are because of component 2, which essentially accounts for the variance in vector 2.



A = Proposed Method Outliers, B = NNR Outliers,
C = NCR Outliers. D = CR Outliers
Universal Set = All chips of wafer 1
{A+B+C+D} = 234
{Universal Set} = 1358

Figure 35. Venn diagram of wafer 1 outliers

4.10.1 NNR vs. Proposed Method

NNR analysis, as explained in Section II. Previous Work, was implemented on the original I_{DDQ} measurements to identify spatial outliers. After forming the residuals using neighbor mean I_{DDQ} information, a Tukey test with a coefficient of k=2 was used to identify the outliers. Table V indicates that the proposed idea classified more chips defective than NNR. The proposed method has a tighter rejection limit.

The main reason than NNR underestimates the number of defective chips is that the mean I_{DDQ} at a location can suppress the effect of an outlier I_{DDQ} measurement unless the outlier is off by a significant value. This can be observed in Figures 36 and 37 for wafer 1 vector 2, where the mean is not representative of the spatial variations in vector 2 I_{DDQ} values.

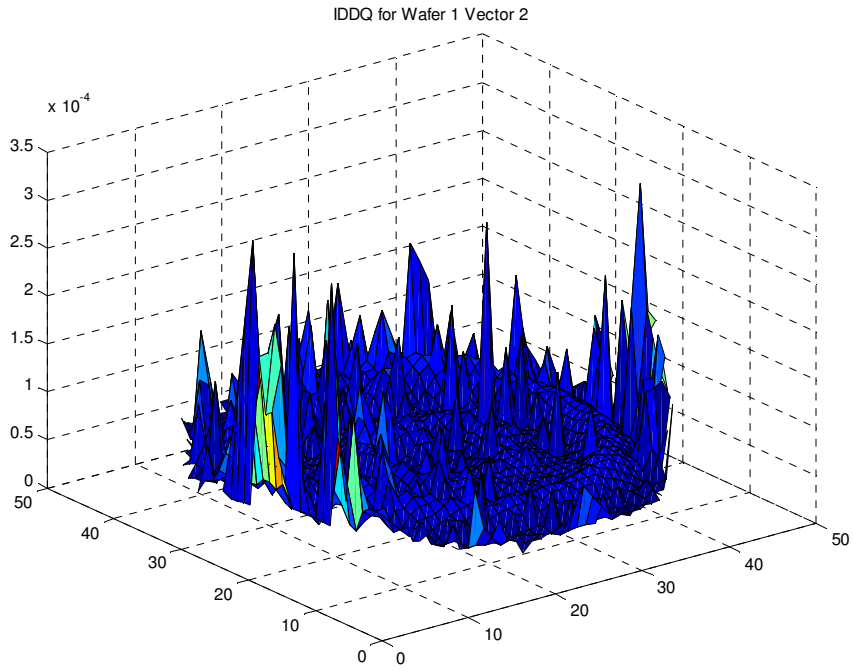


Figure 36. Surface plot of wafer 1 vector 2 raw I_{DDQ}

Figure 37 shows that the mean has high I_{DDQ} only when the I_{DDQ} for all test vectors are abnormal. The mean of the raw I_{DDQ} data causes the effect of outliers with high values only on one vector, to get lost along with the effects of minor variations in

I_{DDQ} data. Figure 38 shows the surface plot of wafer 1 vector 2 raw I_{DDQ} values with all NNR outliers removed. One can observe that a significant amount of absolute outliers still exist in the wafer. Another problem with NNR is that a defective chip in a bad neighborhood cannot be detected. These two factors contribute to NNR passing a lot of chips that the proposed method rejects.

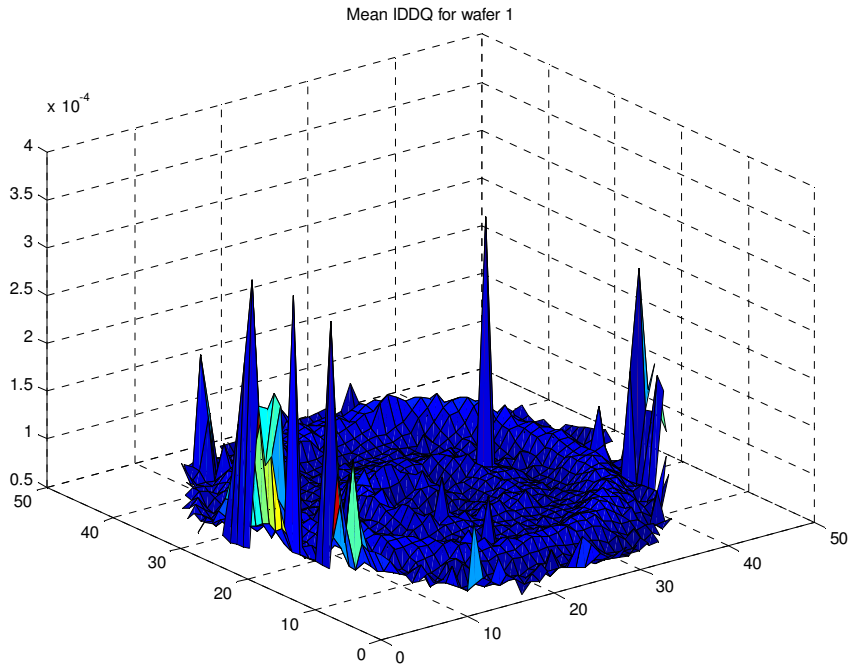


Figure 37. Mean raw I_{DDQ} used during NNR for wafer 1

4.10.2 NCR and CR vs. Proposed Method

Both NCR and CR were implemented on the I_{DDQ} data set, to evaluate their performance against the proposed method. The details of the implementation are the

same as explained in Section II. Previous Work. A Tukey test with coefficient k=2 was used to identify and remove outliers from the residual.

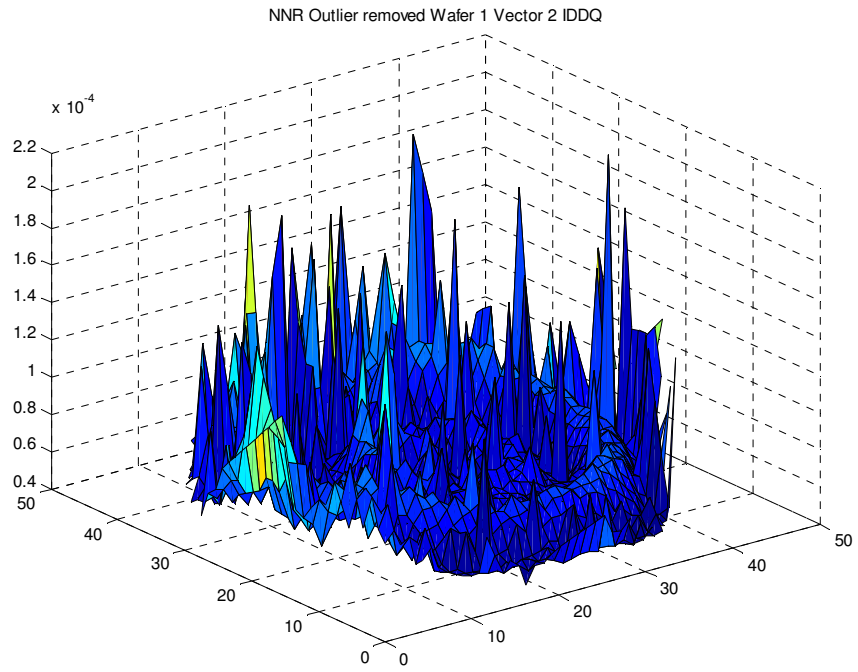


Figure 38. Surface plot of wafer 1 vector 2 raw I_{DDQ} of chips passing NNR

The number of chips rejected by NCR and CR is listed in Table V and the comparison of NCR/CR with the proposed method is available in Table VI. The proposed method has tighter thresholds than NCR. NCR has the problem that a defective chip in a bad neighborhood cannot be detected. Figure 39 shows the surface plot of raw I_{DDQ} measurements for wafer 1 vector 2 after removing NCR outliers. One can observe

that even after removing NCR outliers, there are many absolute outliers that can be observed in the plot. Most these outliers are present in a bad neighborhood or they are not too high when compared to their neighbors, but they are large in an absolute sense.

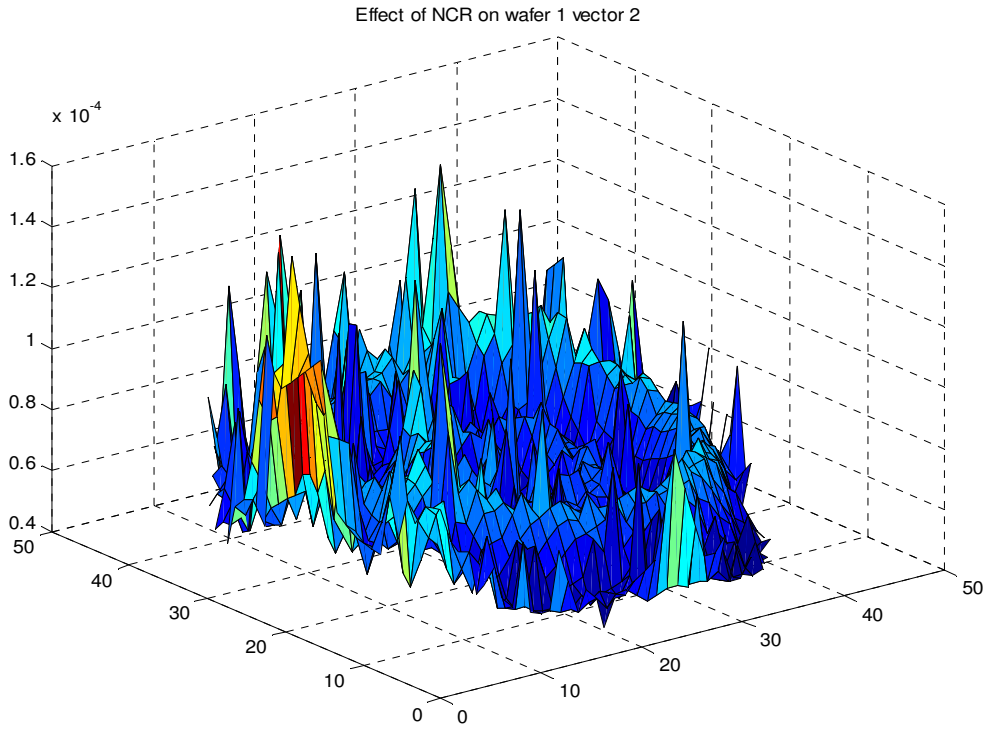


Figure 39. Surface plot of wafer 1 vector 2 raw I_{DDQ} with NCR outliers removed

The main problem with CR is that defective chips with CR approximately equal to one are not detected. These are defective chips with passive defects that cause a raise in both the minimum and maximum I_{DDQ} values. Figure 40 is a surface plot of the wafer 1 vector 2 raw I_{DDQ} measurements after removing CR outliers. Another problem with

CR is that chips are identified as outliers based on intra-die computations. CR does not take any of the spatial information into account. As a result, there are many spatial outliers than can be identified in Figure 40.

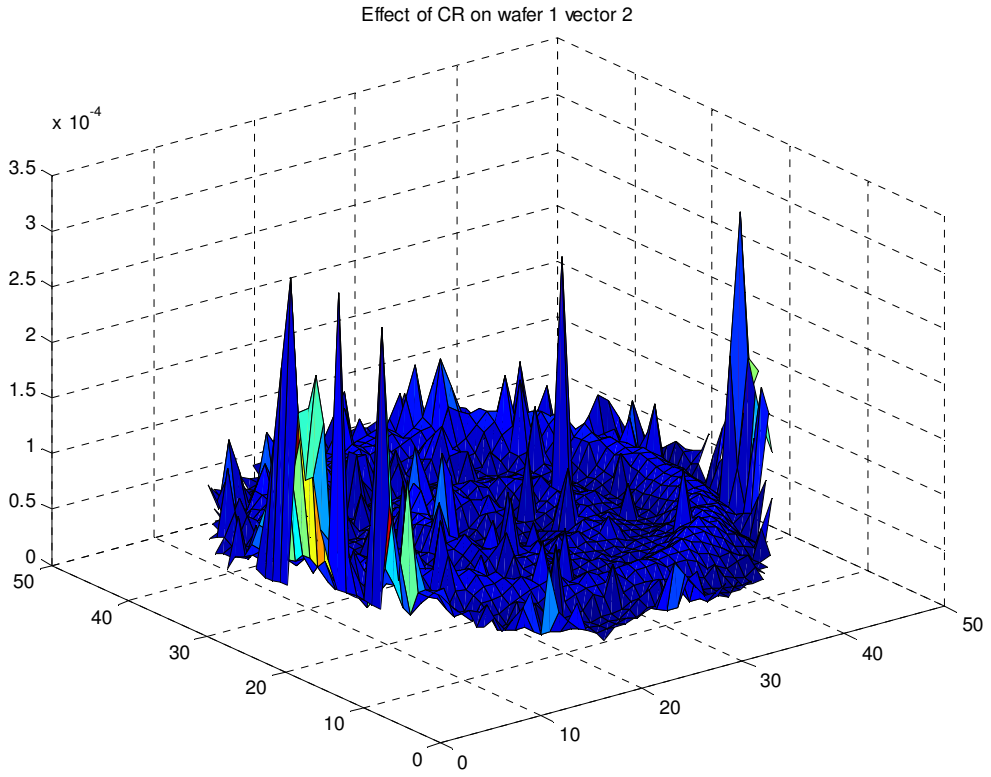


Figure 40. Surface plot of wafer 1 vector 2 raw I_{DDQ} with CR outliers removed

4.10.3 Result of Proposed Method on Wafer 1 Vector 2

Figure 41 shows the surface plot of raw I_{DDQ} data for wafer 1 vector 2, with all the outliers identified by the proposed method (PM) removed.

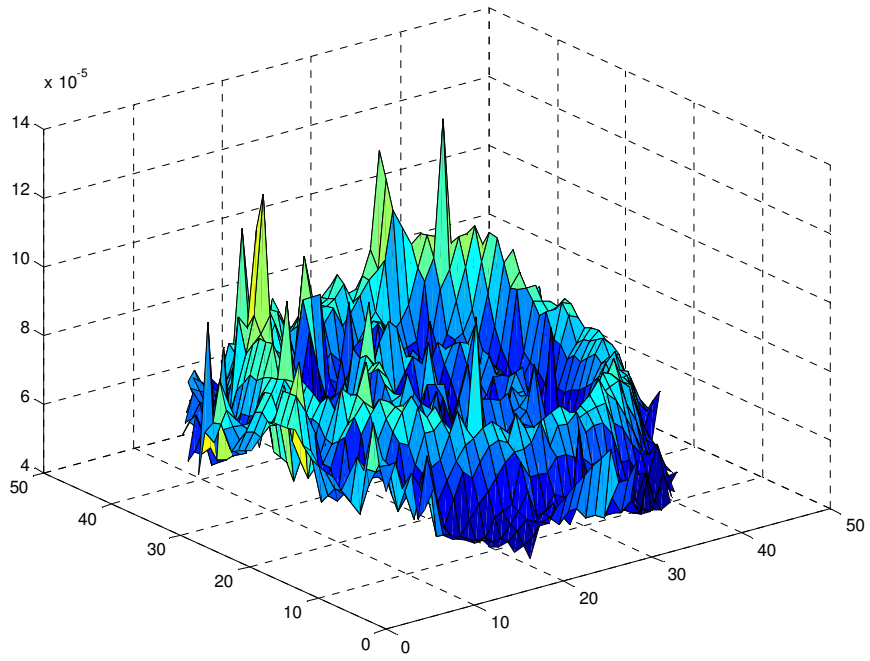


Figure 41. Surface plot of wafer 1 vector 2 raw I_{DDQ} with PM outliers removed

When compared against the surface plot of raw I_{DDQ} data in Figure 36, one can observe that almost all of the chips on the outer edge of the wafer, with high absolute raw I_{DDQ} values have been identified as defective chips. Additionally most of the spatial outliers with low absolute I_{DDQ} have also been rejected as outliers.

Figure 42 contains a mesh plot of wafer 1 vector 2 raw I_{DDQ} values of all the chips rejected by the proposed method (and values of 0 for I_{DDQ} for all accepted chips to improve visibility of rejected chips). Figure 43 is a mesh plot of wafer 1 vector 2 raw I_{DDQ} data for all chips in the wafer. The figures are presented at different angles, to enable a better view of the different bumps in the smooth surface of wafer 1 vector 2 I_{DDQ}.

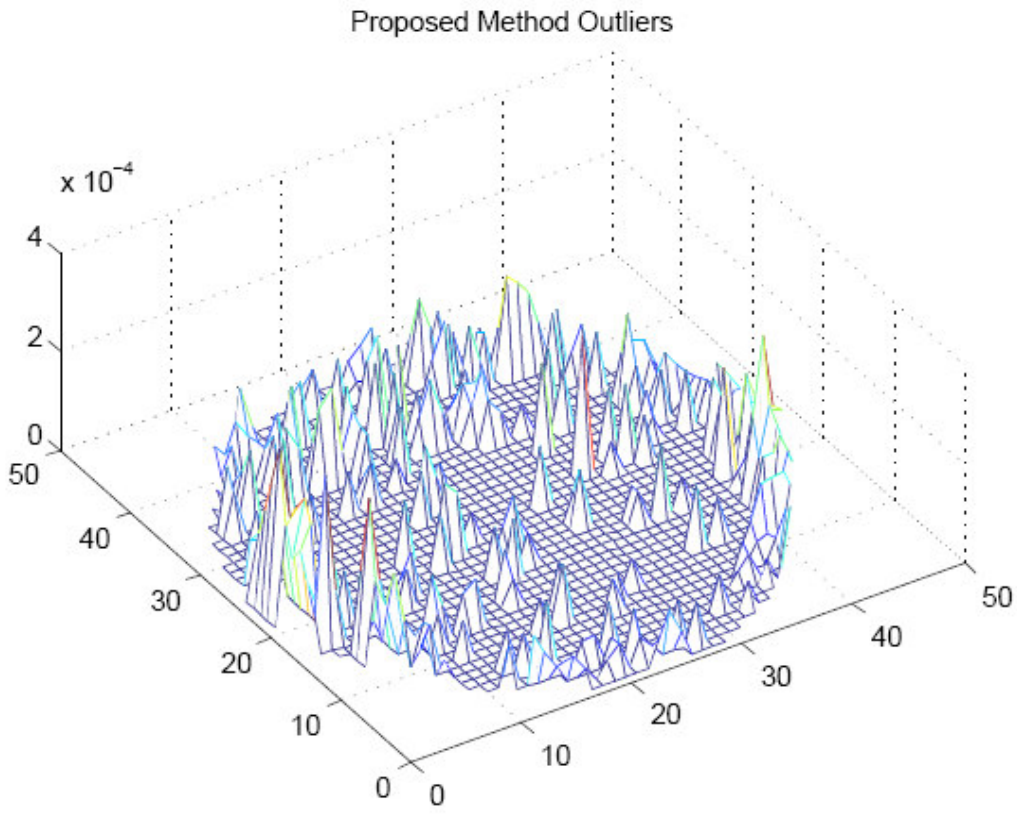


Figure 42. Mesh plot of wafer 1 vector 2 raw I_{DDQ} of PM outlier chips

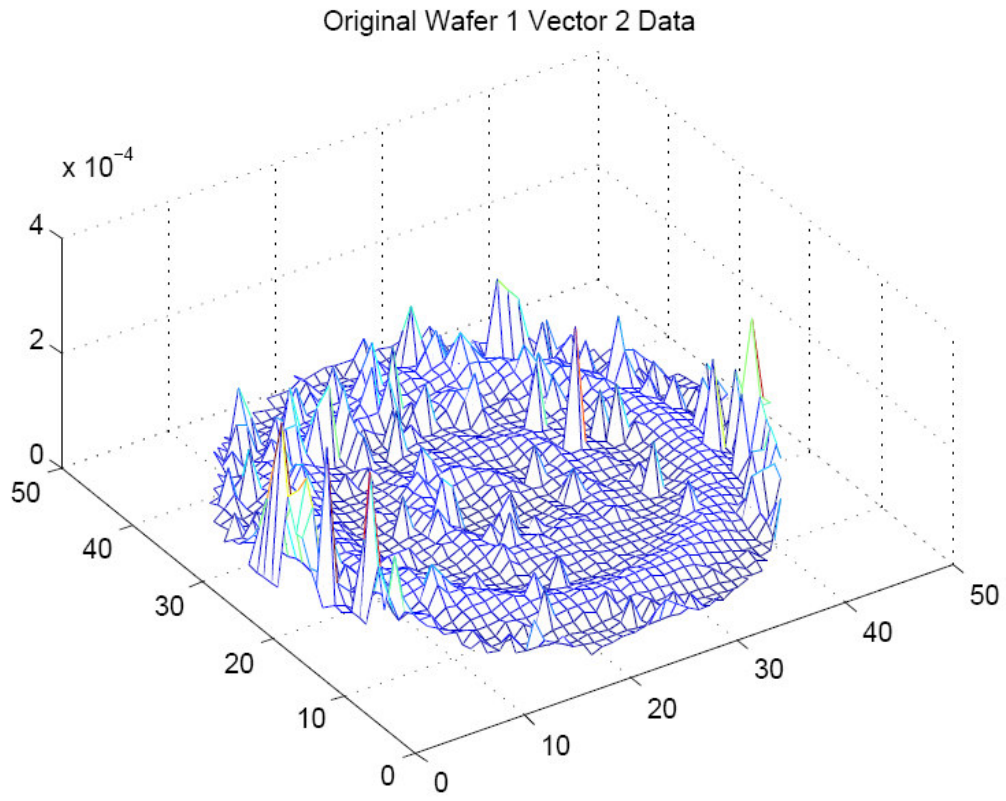


Figure 43. Mesh plot of wafer 1 vector 2 raw I_{DDQ} data

Most of the spikes in Figure 42 are also present in Figure 43. This shows that most of the defective chips identified by the proposed method are either spatial or absolute outliers in the original raw data. There are some bumps in Figure 42 (about 60), which even though not present in Figure 43, are not false negatives because the same location was identified as a defective chip by analysis on another vector. There are some false negatives with very low absolute I_{DDQ}, which could be avoided by tweaking the thresholds used in the implementation.

V. SUMMARY AND CONCLUSIONS

A new methodology using a multivariate statistical analysis technique known as principal component analysis has been developed to achieve variance reduction in I_{DDQ} data. The components extracted by PCA are used to model the good chip expected I_{DDQ} and the residue is calculated using this estimate. The residue is shown to have lower variance than the original I_{DDQ} measurements. Outliers are identified by analyzing the residual and estimate. The significant components extracted by PCA are shown to account for the most variance in the I_{DDQ} data. Theoretically, this can be thought of as the effect of transistor gate length variation (SCE) and threshold voltage variation.

The advantage of this method is that the effects of SCE and other physical effects are inherently considered and accounted for by PCA. Significant variance reduction is achieved as part of the reduction process. Analyzing the components as well as the residual can identify both passive defects and active defects. Any of the already existing outlier techniques can be applied to the residual and significant components to identify outliers. This method catches many of the defects that were undetected using CR, NCR and NNR.

The main disadvantage of the proposed method is that it is very sensitive to the correlation between the I_{DDQ} measurements of different test vectors. PCA extracts components that are linear combinations of the original I_{DDQ} measurements. High correlation between the vectors assures that the prediction of good chip I_{DDQ} values is accurate. The presence of a vector with low correlation causes the prediction for that vector to be inaccurate and might result in high yield loss because of inaccurate

predictions. If all the vectors have low correlations with each other (Wafer 3), the components extracted using PCA do not provide much information and thus variance reduction will not be significant.

The method proposed in this thesis does not detect all possible defects. Every method catches some unique defects, while letting other defective chips go undetected.

5.1 Future Directions for Research

Future research can concentrate on adding additional data as input of PCA, to improve the prediction for good chip I_{DDQ} extracted from the components of PCA. For example,

- A function of the *x* and *y* coordinate of a chip can be developed and provided as an input to PCA, to extract spatial information.
- I_{DDQ} measurements across multiple wafers can be an input to PCA, to better predict I_{DDQ} across the whole lot.
- I_{DDQ} measurements at different temperatures and voltages can be used to take advantage of the dependence of I_{DDQ} on these parameters.
- Other parameter data like MINVDD, F_{MAX} can also be used to take advantage of their correlation with I_{DDQ} (as they are affected by the same process parameters).

The leakage current was used by itself in this research, because it was the only data available. The use of *X* and *Y* as separate inputs to PCA did not yield any significant improvements in the result.

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