HIGH FREQUENCY CONTINUOUS-TIME CIRCUITS AND BUILT-IN-SELF-TEST USING CMOS RMS DETECTOR

A Thesis

by

RADHIKA VENKATASUBRAMANIAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2005

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Weiping Shi
	Sergiy Butenko
Head of Department,	Costas Georghiades

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ABSTRACT

High Frequency Continuous-Time Circuits and

Built-In-Self-Test Using CMOS RMS Detector. (December 2005)

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Birla Institute of Technology and Science, Pilani

Chair of Advisory Committee: Dr. Jose Silva-Martinez

The expanding wireless market has resulted in complex integrated transceivers that involve RF, analog and mixed-signal circuits, resulting in expensive and complicated testing. The most important challenges that test engineering faces today are (1) providing a fast and accurate fault-diagnosis and performance characterization so as to accelerate the time-to-market and (2) providing an inexpensive test strategy that can be integrated with the design so as to aid the high-volume manufacturing process. The first part of the research focuses on the design of an RMS detector for built-in-self-test (BIST) of an RF integrated transceiver that can directly provide information at various test points in the design. A cascode low noise amplifier (LNA) has been chosen as the device under test (DUT). A compact (< 0.031 mm^2) RF RMS detector with negligible input capacitance (< 13 fF) has been implemented in 0.35 µm CMOS technology along with the DUT. Experimental results are currently being assimilated and compared with the simulation results. Frequency limitations were encountered during the testing process due to unexpected increase in the value of the N-well resistors. All other problems faced during the testing, as well as the results obtained so far, are presented in this thesis.

In the second part of the research, the use of the RMS detector for BIST has been extended to a continuous-time high-frequency boost-filter. The proposed HF RMS detector has been implemented along with a 24 dB 350 MHz boost filter as the DUT on 0.35 µm CMOS technology. The HF RMS detector occupies 0.07 mm^2 and has an input capacitance of 7 fF. The HF RMS detector has a dynamic range greater than 24 dB starting from -38 dBm of input power. The bandwidth and boost of the filter have been accurately estimated in simulation using the HF RMS detector. The sensitivity of an intermediate band pass node of the filter has also been monitored to predict the filter's sensitivity to Q errors.

The final part of the research describes the design of a single-ended to differential converter for use in a broadband transceiver operating from 50-850 MHz. This circuit is used as the second stage in the transceiver after the LNA. The design has been simulated on a 0.35 um CMOS process and has a power consumption of 13.5 mW and less than 8 dB of noise figure over the entire band. It is capable of driving a 500fF load with less than 1dB of gain ripple over the entire band (50-850 MHz).

DEDICATION

To my parents.

ACKNOWLEDGEMENTS

First I would like to express my sincere gratitude to my advisor Dr. Jose Silva-Martinez for his invaluable guidance throughout my thesis research. I have kept him late on many evenings with my questions and problems, and he has always been very patient and understanding. I am deeply indebted for the immense amount of knowledge that I have gained from him. His love for analog circuits was very infectious and his spark for constant innovation very stimulating.

I am very thankful to Dr. Edgar Sánchez-Sinencio for being a constant source of support through many a rough patch and for serving on my committee. He has always been a source of encouragement and inspiration with an ever-smiling countenance.

I would like to thank my committee members, Dr. Weiping Shi and Dr.Sergiy Butenko, for exposing me to two new fields-CAD and non-linear programming. I greatly benefited from my brief stint at both and will undoubtedly be using the knowledge I have gained in the future.

I have learned a lot from the technical discussions that I have had with Alberto Valdes-Garcia. His dedication and perseverance were very motivating. I am also very grateful to Chinmaya Mishra who has extended his support and guidance on numerous occasions.

I had the opportunity of working with three brilliant people during my research. Rangakrishnan Srinivasan designed the low noise amplifier and the buffer which were used as the device under test (DUT) for the RF RMS detector. He sat with me through all the discussions on the RF RMS detector all the way until the chip was sent to fabrication.

The HF RMS detector was designed for the built-in-self-test of the boost-filter designed by Manisha Gambhir and Vijayakumar Dhanasekaran. They extended their help to me ungrudgingly every time I turned to them with questions about the simulation and testing of the filter.

I would like to thank all my friends including Gopinath Vageesan, Vishnu Raghavan, Praveen Kota, Anantharaman Balasubramanian, Aravind Aluri, Nitin Ved, Prakash Sankarasubramanian, Sumee Khanna, Bhavani Radhakrishnan, Preethi Premkumar, Divya Narayanan and Ramya Anantharaman for making my time at A&M truly memorable; and the last four for extending their hospitality to me every time I visited College Station to do my testing. Life at A&M would never have been the same without all of them.

I am deeply indebted to Sivakumar Ganesan for being a friend, teacher, fellow student, helper, listener, pacifier and encourager as, and when, the time demanded.

Finally, I owe everything that I have done to my parents who have supported me through every single moment of my life. I have taken every single one of my problems to them with the strong confidence that they would be solved and have never returned disappointed. Nothing would have been possible without their blessings, encouragement, motivation, guidance and love. I would also like to thank my younger brother for his love, affection and encouragement.

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1. INTRODUCTION

1.1 PROBLEM STATEMENT

1.1.1 Built-In-Self-Test

As the complexity and operating frequency of integrated transceivers continue to increase, their testing and characterization has become a veritable challenge to test engineers. Traditional monolithic testing using off-chip test equipment is no more possible because (1) it is very time-consuming and has become a liability to the time-to-market of the final product (2) RF and high-frequency test equipment is very expensive and is detrimental to the cost of the final product (3) off-chip testing cannot be used for the characterization of the individual building blocks in an integrated transceiver.

Built-In-Self-Test (BIST) presents the answer to all the above problems by providing inexpensive and fast solutions for the complete characterization of the transceiver as well as for the characterization of individual building blocks to improve the fault coverage. BIST typically involves the placement of suitable sensors at various nodes in a transceiver that can extract information from those nodes and processing of that information to predict the behavior of each block in the transceiver. Apart from being used for testing, these sensors can be used for early detection of parametric faults during the product development phase.

The problem at hand is (1) to design a CMOS sensor that can operate at RF

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frequencies (2) to optimally place the sensors at strategic positions in an RF transceiver and (3) to devise a simple strategy without using any complex test stimulus or test equipment for intelligently characterizing the building blocks in a transceiver with the information obtained from the sensors.

An ideal sensor would be one that can provide a DC voltage corresponding to the RF power present at a node (i.e. a peak or RMS detector) because the DC voltage is conducive to easy and simple processing using low-cost tester and/or analog-to-digital conversion and on-chip digital processing circuitry. Multiple nodes could be observed from a single output pad since DC voltages can be multiplexed easily.

An RF RMS detector is more suitable for BIST rather than an RF peak detector because of the fact that an RF peak detector's output depends upon the input signal's PAR (Peak to Average envelope power Ratio). [1] compares peak detectors and RMS detectors and discusses advantages of the latter over the former. The desired characteristics of the RF RMS detector [2] are (1) high input impedance at the frequency of test to prevent loading and performance degradation of the RF circuit under test (2) minimum area overhead and (3) dynamic range suitable for the target building blocks.

Addressing the problem of optimal placement, a typical transceiver with suggested observation nodes has been shown in [2] and reproduced below in figure 1.1 for convenience. This placement is "optimal" in the sense that a number of useful measurements (table 1.1) can be extracted at those points.

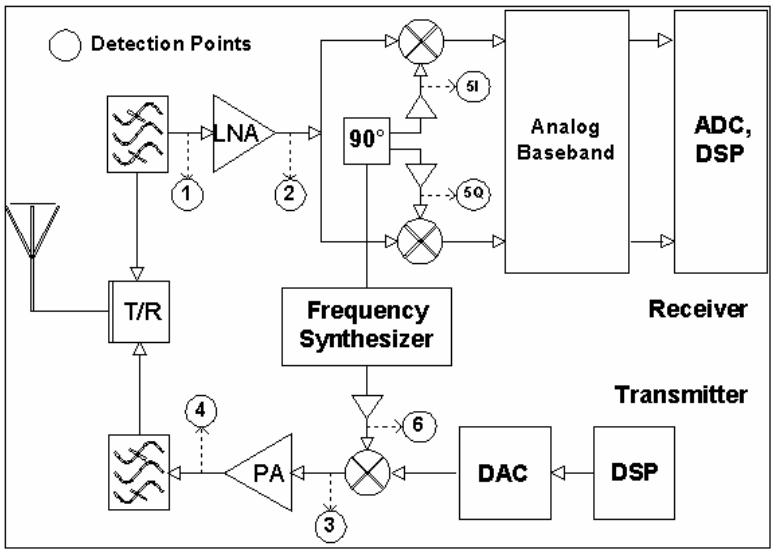


FIG 1.1 DETECTION POINTS IN A TRANSCEIVER [2]

TABLE 1.1 MEASUREMENTS FOR THE BUILT-IN TRANSCEIVER CHARACTERIZATION

Observation Point	Measurements
1	Calibration path
2	LNA gain and 1dB compression point.
3	Up-converter output power.
4	PA gain and 1dB compression point
6	Local oscillator output power
$5_{I,}\ 5_{Q}$	Phase and magnitude mismatch between I & Q channels.

Using the above placement, a simple test strategy can be devised by using an RF source and without the need for any complex test stimuli as outlined in [2]. By varying the input RF source, the gain and 1-dB compression point of the LNA can be found from the RMS detectors placed at location 1 and 2. A corresponding measurement can be

made for the power amplifier using the detectors placed at 3 and 4. In transceiver implementations, buffers are employed at the output of the local oscillator signal (LO) to assure proper switching in the mixers. Observation pints 5 and 6 monitor the output amplitude of these buffers. This is important because the conversion gain and noise figure of the mixers depends on the LO signal amplitude.

The goal of this research is to design a compact CMOS RF RMS detector that satisfies all the requirements listed above. The capabilities of the RF RMS detector have to be demonstrated with a suitable DUT (at least one block of the integrated transceiver) by elaborating on the simple test strategy outline suggested above.

1.1.2 Single-Ended to Differential Conversion

In a broadband receiver operating in the range of 50-850 MHz, the complex filter forms the second stage after the LNA. The LNA has a single-ended output whereas the complex filter has a differential input. This entails a single-ended to differential signal conversion after the LNA. The single-ended to differential conversion can be very costly in terms of area and power because of the number of stages. The reason for this is elaborated as follows. A single differential pair driven by a single ended input will not produce outputs which are exactly fully differential because, the two paths to the output are not symmetrical. That is, one path suffers from an extra parasitic pole at the common node of the two input transistors. In figure 1.2, i_{ac2} suffers from an extra pole because of the parasitic capacitance C of the current source Ibias.

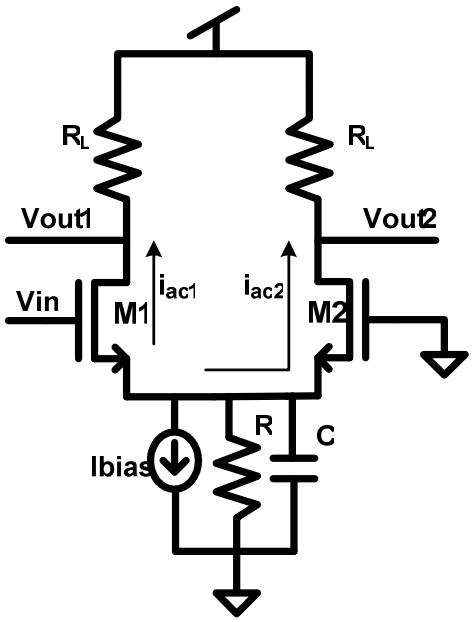


FIG 1.2 COMMON NODE PARASITIC POLE IN DIFFERENTIAL PAIR

However, it can be shown that by using successive pairs of differential amplifiers, the phase error in differential signals can be corrected. Hence, the commonly used method of producing perfectly complementary signals lies in using cascaded differential pairs [3]. But, as indicated before, this method is costly in terms of both power and area. Thus, the problem at hand is to produce perfect differential signals from a single-ended signal without sacrificing area and power.

1.2 BACKGROUND

1.2.1 High Frequency Built-In-Self-Test

This sub-section briefly describes the techniques implemented in BIST from the literature and discusses the built-in-sensors most relevant to this research, in some detail.

Some of the oldest proposed methods in the history of BIST include loop-back and wafer-probe testing [4-7]. Loop-back techniques focus on hooking up the transmitter to the receiver in order to generate digital inputs and outputs that can help in fault diagnosis. However, apart from basic fault-diagnosis, loop-back techniques cannot perform the characterization of each individual block which is essential for improving the fault coverage. In the case of wafer probe testing, the RF signal drive and response observation capabilities are limited and RF testers prove to be very expensive. This is very detrimental to the cost of the final product because all dies that pass the wafer-probe test are tested again after they are packaged and hence, the testing procedure becomes very expensive.

Other recently employed methods for testing RF paths are noise-reference-based testing, which typically involves feature extraction of the individual blocks in the transceiver using noise-reference-based comparators and digital signal processing [8, 9], and estimating the extracted spectral density at various nodes in the receiver from statistical samples [10, 11]. These methods use white noise either as an excitation signal or as a reference and require memory and processing resources, which can be obtained from a System on Chip (SoC) environment.

The most primitive forms of embedded sensors or detectors were designed using thermal detectors [12] and diodes [13]. But, thermal detectors are not conducive to integration and suffer from slow response times due to slow thermal time constants. Moreover, since the RF power measurement is based on comparison with respect to a known reference, the method also suffers from matching and isolation problems. Diode

detectors work as peak detectors based on the principle of rectification using a diode and averaging using a simple RC filter. They have wide detection bandwidths and can respond to high frequencies. But, at high input amplitudes, the response of the diodes deviates significantly from the square law and hence the linearity of diode-based sensors is limited by the square law. They also exhibit poor stability over temperature.

After the first generation of sensors, embedded testing evolved into using logarithmic sensors and true RMS detectors [14, 15]. Both these methods are described in detail in the subsequent paragraphs using suitable examples.

Logarithmic amplifiers are basically peak detectors. A 450 MHz CMOS RF power detector [16] based on a successive detection CMOS logarithmic amplifier has been proposed to measure the RF power at the antenna during transmission. The successive detection log-amp consists of a cascade of six CMOS limiting amplifiers which have a gain of 9 dB in their linear region and a rectifying trans-conductor cell at the input and output of each of the limit amplifiers. The outputs of the rectifying trans-conductor are summed together and low pass filtered to produce a voltage proportional to the log of the input. The DC transfer function of the log-strip is

$$V_{out} = V_{slope} * \log_{10}\left(V_{in} / V_{\text{int}\,ercept}\right)$$

The block diagram of the log-amp is shown below in figure 1.3.

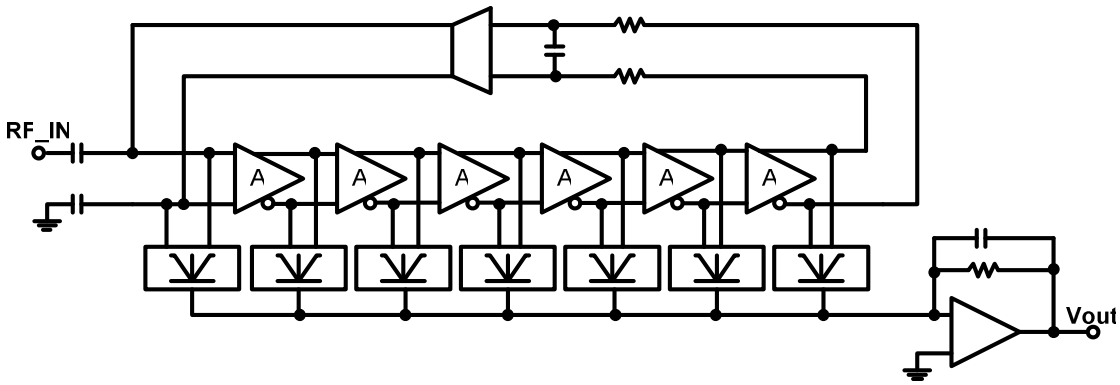


FIG 1.3 BLOCK DIAGRAM OF 450 MHZ CMOS RF POWER DETECTOR [17]

The circuit has a power consumption of 10 mA and occupies 0.5 mm^2. It must however be remembered that the total area of all the inserted sensors in a transceiver should be less than 10% of the total area of the transceiver. Taking the example of a typical Bluetooth receiver [18], the total area of the chip is 6.25 mm^2 and incorporating more than one sensor on this receiver will increase the area overhead by more than 10%. The total power consumption of the sensor should also be a small fraction of the transceiver's total power consumption. 10mA forms 15% of the total power consumption of the receiver in [18]. The circuit has an excellent dynamic range of 50 dB at 450 MHz and also shows log conformance up to 900 MHz with a dynamic range of around 25 dB. However, the dynamic range of the log-strip is determined by the number of stages in the cascade and the gain of each stage. Increasing the dynamic range at RF frequencies would either entail an increase in the number of stages (which would mean a further increase in area) or an increase in the gain of each stage (further increase in the power consumption). Hence, the frequency range of the sensor can be extended up to RF

frequencies (of the order of 2 GHz) by compromising the area or power which may make it unsuitable for BIST.

True RMS detectors are based on the definition of RMS detection, that is, the output is the square root of the average of the input waveform squared. True RMS detectors are independent of the shape of the input waveform and an example of a true RMS detector is the commercial stand-alone RMS detector AD8361 [19] from Analog Devices which using bi-polar transistors. It has two identical squaring cells whose outputs are balanced by a high-gain error amplifier. The RF signal (RFIN in Fig 1.4) is applied to the input of the first squaring cell to generate a current proportional to vin^2. This current is then filtered through a simple RC filter and applied to one input of a high gain error amplifier. A fraction of the DC voltage at the output of the high gain error amplifier is applied as the input to a second squaring cell. The output of the second squaring cell is applied to the inverting input of the error amplifier thus completing the negative feedback loop which now ensures excellent stability of calibration and canceling scaling effects. The error amplifier forces the average signal of the first squaring signal to be equal to the signal delivered from the second squaring cell thus ensuring that the output of the error amplifier is equal to the root mean square of the input. The basic block diagram is shown below in figure 1.4.

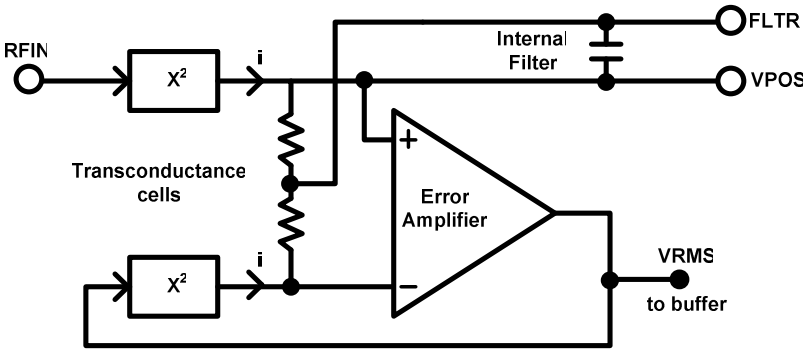


FIG 1.4 AD8361–TRUE RMS DETECTOR

The AD8361 can operate with a single supply from 2.7 to 5.5 V with very low power of 3.3 mW at 3V supply and exhibits an input dynamic range of 30 dB at 2.5 GHz. It provides a numerous salient features and is very robust at the cost of increased complexity and area.

In contrast to true RMS detectors, RMS detection can also be performed by detecting the average value of a given waveform. A pseudo-RMS-current-converter for sinusoidal signals has been described in [20] using a precision current rectifier. Average detection is simpler than true RMS detection in terms of the complexity involved and the average value can be related to the true RMS value depending on the type of input waveform as shown in [20]. Figure 1.5 depicts the precision current rectifier which forms the core of the idea in [20] derived from [21].

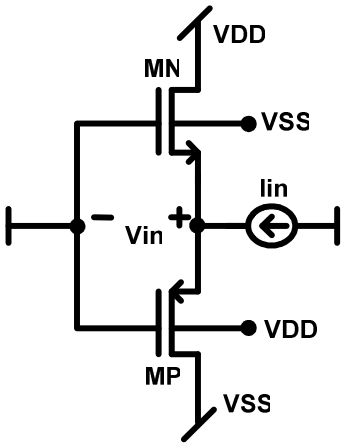


FIG 1.5 CLASS B RECTIFIER

During positive excursions of vin, MP is turned ON, MN is turned OFF and Ip=Iin and vice versa. Thus by adding Ip and In, full wave rectification has been performed. However, the Class-B rectifier has the well-known problem of dead-band. Large voltage swings are needed at vin in order to turn on the MN and MP [17]. An expression for the amount of voltage swing needed has also been derived in [17]. A method to solve this dead band problem has been proposed in [17] through an offset correction circuit using a feedback amplifier. However, this technique increases the complexity, area and power consumption.

The obvious solution to the problems faced in the Class B rectifier is to use Class AB rectifier [22]. The two input transistors MN and MP in the figure below are biased by a small current source Ib and are ready for conduction. Hence, the dead-zone region can easily be avoided and the current Ib can be subtracted to improve the precision. [22] only shows the application for half-wave rectification, however, [23] shows its application to full wave rectification. The frequency of operation in [22] is limited to 200

MHz because of the fact that it has been designed in a 2um technology. It is possible to extend the frequency of operation by using lower transistor lengths. The Class AB rectifier is shown below in figure 1.6.

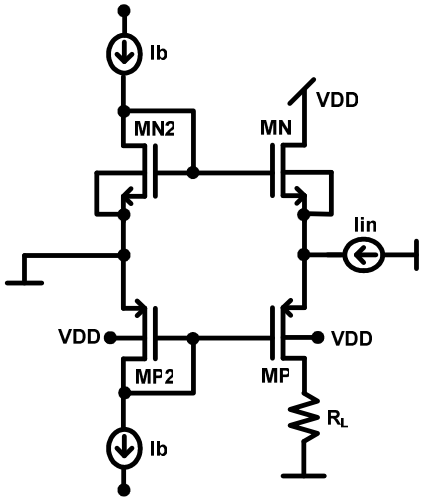


FIG 1.6 CLASS AB RECTIFIER

An RF power detector using a Silicon MOSFET [24] proposes the basic principle of deforming the input RF signal using a non-linear device (Silicon MOS transistor) into a DC component and a number of harmonics. Using a basic RC filter, the harmonics are filtered out and the DC component is extracted. T1 (figure 1.7) is a Common-gate CMOS transistor and the RF signal at its drain is deformed by its drain-source resistance Rds1. The signal at the source is composed of a DC current and a number of harmonics. The DC component is then filtered out using RL and C1.

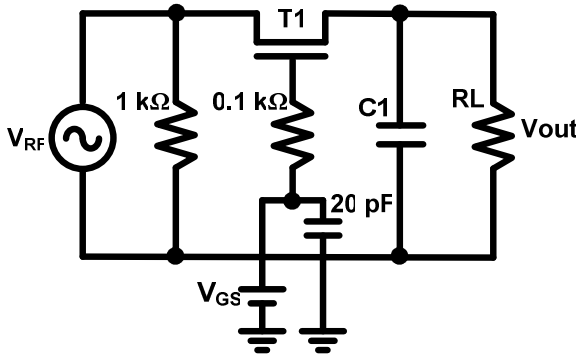


FIG 1.7 RF POWER DETECTOR USING A SILICON MOSFET [24]

The prediction of the RF power detector results is based on the accurate modeling of the non-linearity of the silicon MOSFET and hence the design is subject to modeling errors especially at high frequencies around 2 GHz as shown in the paper. However the circuit works well around 1 GHz. One of the major drawbacks of this circuit is that it occupies an area of 1 mm^2. One power detector would increase the area overhead of the receiver in [18] by more than 15%, thus making it unsuitable for BIST.

1.2.2 Single-Ended to Differential Conversion

The most common active single ended to differential converters or rather phase splitters use either a single transistor or a common-gate-common-source (CGCS) or differential pair implementations. These three main implementations are discussed in some detail below.

A phase splitter using a single transistor has been used in [25] (figure 1.8). The collector and emitter terminals of the BJT have been tapped to produce differential signals:

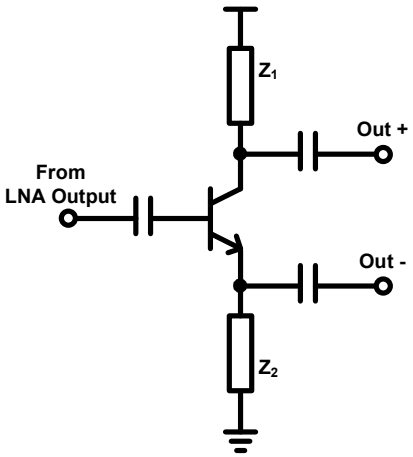


FIG 1.8 PHASE SPLITTER USING A SINGLE TRANSISTOR

However, this method is not robust because of the phase error and gain imbalance in the two outputs due to the mismatch between the two loads connected to the two outputs. A number of efforts have been made to reduce this gain and phase imbalance by minimizing the error due to Cgs and Cgd by changing the gate width and by adjusting the drain-source voltage [26] (4 degrees of phase error) as well as by attaching off-chip loads to the two outputs, but this method still remains non-vigorous.

A CGCS implementation has been proposed with less than 0.5 dB of amplitude balance and less than 5 degrees of phase error [27] for broad band applications from 0.5 to 10 GHz. The basic idea that has been used is shown below in figure 1.9.

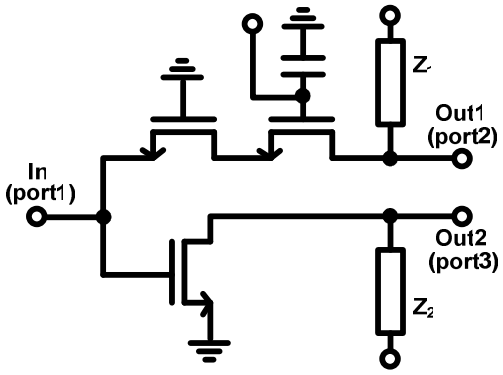


FIG 1.9 CG-CS PHASE SPLITTER

The disadvantage of the idea is that it has a -5 dB insertion loss which can degrade the SNR and linearity in an integrated transceiver.

It has already been indicated that using a single differential pair for phase splitting can cause significant phase error at the output because of the mismatch in the two paths to the output (figure 1.2). An active differential broad-band phase splitter has been proposed for Quadrature Modulator Applications [28]. It has been shown through detailed theoretical analysis that the phase error of a single differential amplifier (of about 40%) can be reduced significantly down to 5.7% or 0.9% by adding a cascade of two or three similar stages. However, the disadvantage of this circuit is that the current dissipation is at least 15.2 mA for achieving less than 2 degrees of phase error; hence less phase error can be achieved at the expense of high power consumption.

1.3 PROPOSED IDEAS AND MAIN ACHIEVEMENTS

It has been seen in the previous section that the main constraints associated with the design of an RMS detector for RF frequencies are the area, power consumption, input capacitance and input dynamic range. A compact CMOS RF RMS detector has

been presented in this work. It occupies less than 0.031 mm^2 of area, has an input dynamic range greater than 30 dB and an input capacitance of less than 13 fF. The capability of the RF RMS detector for characterizing the gain and 1-dB compression point of a cascode Low Noise Amplifier at 2.4 GHz has been demonstrated in simulation. The RF RMS detector has been implemented in silicon along with the cascode LNA on TSMC 0.35um technology. Testing results are still being assimilated and compared to the simulation results. Frequency limitation problem was encountered during the testing of the RF RMS detector due to unexpected increase in the value of the N-well resistors. All other problems faced as well as the results obtained so far are presented in this thesis.

The concept of the RMS detector has been extended to the continuous-time testing of a high frequency (350 MHz) boost (24 dB) filter designed for read channel applications. The high-frequency (HF) RMS detector occupies 0.07 mm^2 area and has an input capacitance of 7 fF. The dynamic range of the RMS detector has been verified to be greater than 24 dB starting from an input power of -38 dBm. The bandwidth and boost of the filter have been accurately estimated in simulation using the HF RMS detector. The sensitivity of an intermediate band pass node of the filter has also been monitored to predict sensitivity to Q errors. The HF RMS detector has been implemented in TSMC 0.35um technology along with the DUT. The experimental results are yet to be verified as the IC is still under fabrication.

A simple and stable phase splitter has been proposed for use in a broadband transceiver operating from 50-850 MHz and it can generate fully differential signals with

less than 2 degrees of phase error as well as provide high linearity with minimum power consumption, while adding as little noise as possible. The design has been simulated on a 0.35 um CMOS process and has a power consumption of 13.5 mW at $\pm$ 1.5 V and less than 8 dB of noise figure. It is capable of driving a 500 fF load with less than 1dB of gain ripple over the entire band.

1.4 THESIS ORGANIZATION

This section gives a brief description of the organization of this thesis. This thesis has been divided into 4 sections.

Section II is the core of the thesis and discusses the design of the RF RMS detector. Each block of the RF RMS detector has been described in detail and simulation results have been presented. The testing strategy from [2] has been used for the experimental verification of the DUT (2.4 GHz CMOS cascode LNA) using the RF RMS detectors. All issues faced during the experimental verification have been described in detail and the results have been presented.

Section III discusses the design of the HF RMS detector for continuous time testing of the 350 MHz 24 dB boost filter. A testing strategy has been developed for the estimation of the bandwidth and boost of the filter. Simulation results have been presented for verification of the test strategy.

Section IV deals with the design of the phase splitter for broadband applications from 50-850 MHz. The basic theory behind the idea has been explained followed by the verification of the results in simulation.

2. RF BUILT-IN-SELF-TEST USING RF RMS DETECTOR

This section discusses the design of the RF RMS detector. Each block of the RF RMS detector has been described in detail and simulation results have been presented. The testing strategy from [2] has been used for the experimental verification of the DUT (2.4 GHz CMOS cascode LNA) using the RF RMS detectors. All issues faced during the experimental verification have been described in detail and the results have been presented.

2.1 DEFINING THE DUT

A simple CMOS cascode low noise amplifier was chosen as the DUT because it simultaneously satisfies numerous specifications on Gain, NF and Linearity and thus provides a number of challenges to the RF RMS detector. The LNA was targeted to work at 2.4 GHz because this is the ISM band employed by widely used wireless standards such as Bluetooth, Wi-Fi and Zigbee. The LNA is not capable of driving the load capacitance of the output pin. Hence a buffer is necessary at the output of the LNA, shielding the LNA from the load capacitance. Moreover, the buffer's input capacitance models the input capacitance of the mixer which forms the next stage to the LNA in a transceiver. Figure 2.1 shows the basic schematic of the DUT.

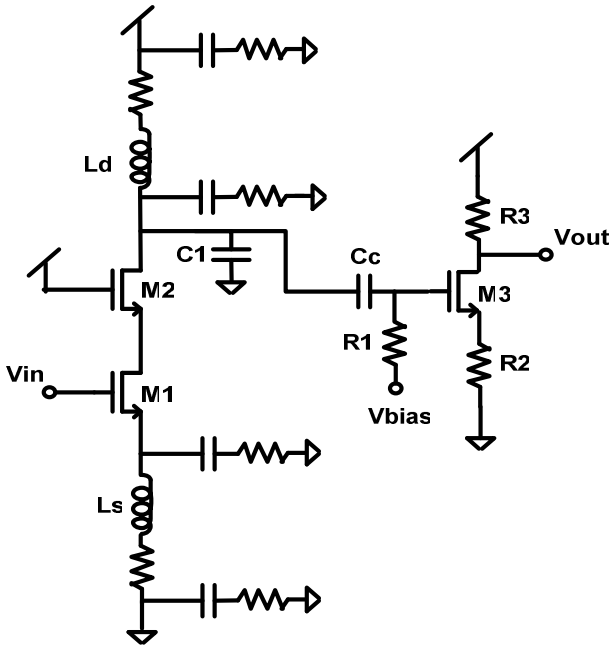


FIG 2.1 SCHEMATIC OF LNA-BUFFER COMBINATION

In the schematic, the drain and source inductors (Ld and Ls) have been shown with their pi-models from ASITIC [28]. The value of the inductors and the model parameters are shown in figure 2.2.

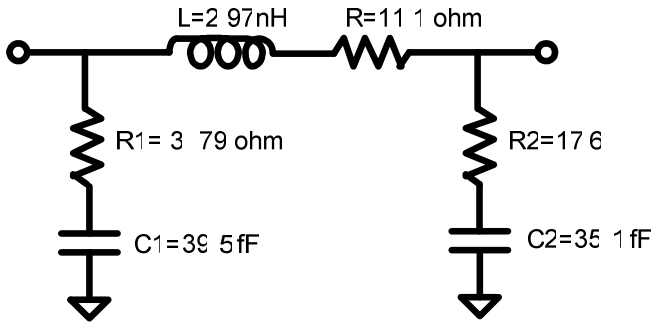


FIG 2.2 INDUCTOR PI-MODEL

The buffer was chosen to be a simple common source configuration. A source degeneration resistor was employed as the buffer needs to be more linear than the LNA because in a cascade of two RF blocks, the total linearity is greatly influenced by the linearity of the second block. The buffer output was terminated in a 50 ohms load in order to achieve good output match (s_{22}), although using an open-drain configuration would have been better in order to have flexibility over the buffer loss and linearity (more on this in the section on testing results). R1 was used to DC bias the buffer and was chosen to be 2Kohm. Figure 2.3 shows the gain in the LNA and its 1-dB compression point.

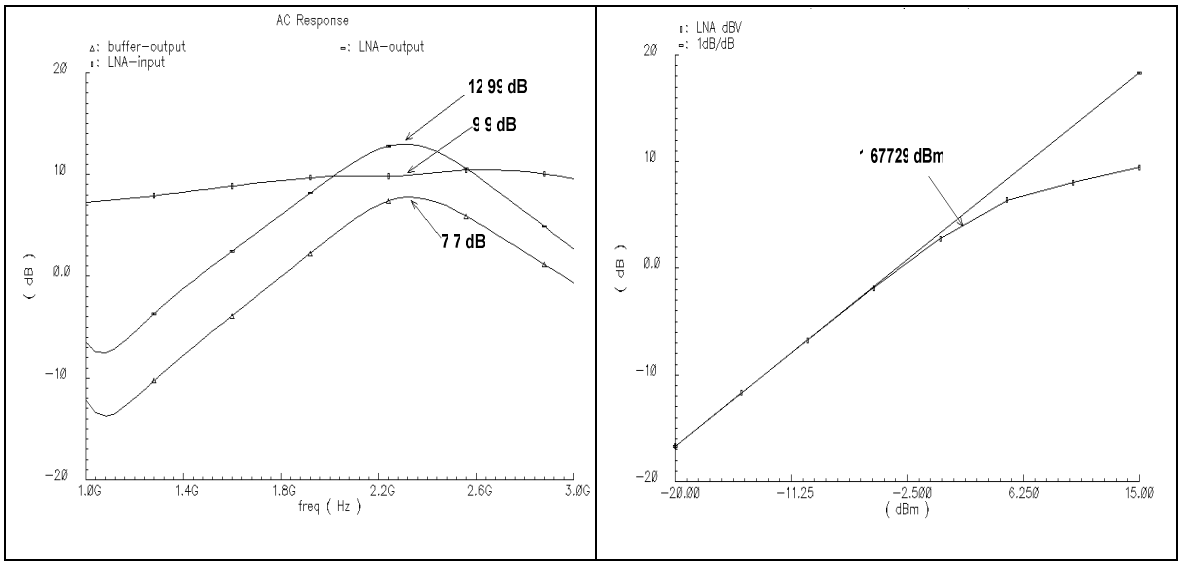


FIG 2.3 LNA CHARACTERIZATION

Table 2.1 summarizes the different specifications of the LNA and the LNA-Buffer combination.

TABLE 2.1 LNA-BUFFER PERFORMANCE SUMMARY

LNA gain at 2.4 GHz	3 dB
Buffer loss at 2.4 GHz	-4.8 dB
1-dB compression point of LNA	1.67 dBm
1-dB compression point of LNA-Buffer	-0.79 dBm

According to the Bluetooth specification, the sensitivity level at the input of the LNA is -70 dBm for 0.1 % BER [29,18] and the maximum signal level at the input of the LNA is -20 dBm. Hence, the RMS detector should ideally be capable of detecting signals as low as -70 dBm and in the worst case, at least as high as -20 dBm. The actual level of sensitivity achieved in the RF RMS detector during the simulation and testing phases have been demonstrated under the appropriate sections. From the specifications of the DUT in Table 2.1, the RF RMS detector should be able to detect a maximum signal of 1.67 dBm in its linear range (the input 1-dB compression point of the LNA).

2.2 BASIC ARCHITECTURE AND SPECIFICATIONS OF RF RMS DETECTOR

2.2.1 Specifications

A signal can be characterized by either measuring its peak value or its RMS value. RMS detection is a better way to characterize a signal rather than peak detection because in peak detection, the output is dependent on the signal PAR [1]. Further, it has been demonstrated in section 1.2.1 that detecting the average value of a signal is simpler than true RMS detection in terms of complexity, area and power consumption using appropriate examples from literature. For this application on built-in-testing, true RMS detection is unnecessary because we are only concerned with relative difference in the

outputs of two RMS detectors connected at the input and output of the LNA. Further, CMOS sensors are more preferable from the point of integration into standard processes, which do not have the privilege of using bipolar transistors. Hence, the basic specifications for the CMOS RF RMS detector are:

- Simple and robust design – to enhance repeatability of the RF RMS detector at different nodes as desired and perform reliable and accurate characterization of the signal at the various nodes.
- Minimum area – the entire built-in-test-circuitry needs to be less than 10% the area of the entire receiver.
- Low input parasitic capacitance – the RMS detector should not load the node to which it is connected

2.2.2 Basic Architecture Using Current Mirror as a Rectifier

The two most important elements needed for a simple RMS detector would be a rectifier and a filter to extract the DC level of the rectified signal. The simplest rectifier that can be used is the current mirror. The operation of a current mirror as a rectifier is described in detail under section 2.2.3. The usage of a current mirror as a rectifier entails the need for a voltage-to-current conversion at the input. It also needs a filter that can extract the DC level of the rectified AC current and current-to-voltage conversion at the output. Figure 2.4 shows the basic architecture for extracting the DC voltage of an RF sinusoidal signal.

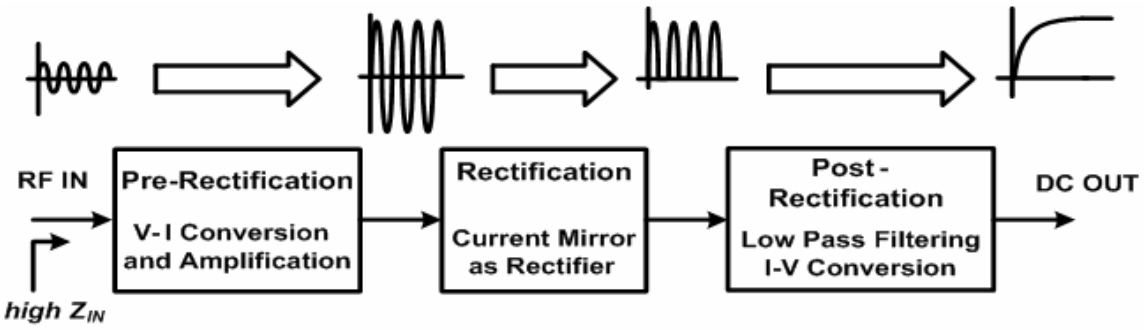


FIG 2.4 BLOCK DIAGRAM OF RMS DETECTOR

2.2.3 Operation of Current Mirror as a Rectifier

The simplest rectifier that can be used is a basic current mirror. The basic functioning of the current mirror as a rectifier is shown below in figure 2.5.

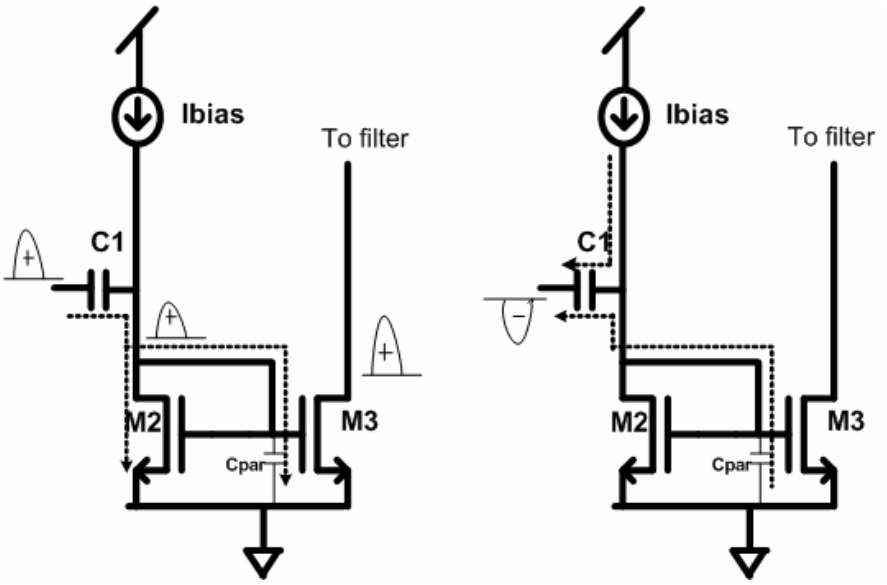


FIG 2.5 CURRENT MIRROR AS A RECTIFIER

The working principle is to control the region of operation of the transistors M2 and M3 using AC signals. During the positive cycle, AC current through M2 ensures that M2 is now operating in saturation region. This current is mirrored and amplified through M3, which is now operating in saturation region. During this time, the parasitic capacitances at the gate of M3 are charged. During the negative cycle, the current is extracted out of M2, hence discharging the capacitor at the gate of M3 thus pushing it into cut-off region. Hence the current is not mirrored to M3 during the negative cycle. A substantial portion of the current is mirrored into M3 during the positive cycle and this summarizes the operation of the current mirror as a rectifier.

M2 and M3 need to be biased by a small current source Ibias which can keep them is weak inversion because of the fact that if the current mirror solely operated on AC signals, there would be a minimum signal swing needed at the gate of M2 to turn it on. This would reduce the sensitivity of the current mirror to low signal values. Hence, it is very advantageous to keep the MOS transistor biased in the weak inversion region using a small current source Ibias. Although the current mirror is now more sensitive to small signal levels, any AC current amplitude smaller than Ibias will not be rectified. Hence, the rectification and the averaging function at low signal levels is not very effective and the resolution is reduced. This places a restriction on the value of Ibias. Figure 2.6 depicts the transient current (left) and its averaged value (right) at the drain of M3 for an Ibias of 50 uA. It can be seen from the transient response that at low signal levels, the rectification is poor and the AC current is mirrored to the drain of M3 in both

the positive and negative cycles. This causes the flat portion in the averaged transfer characteristic on the right.

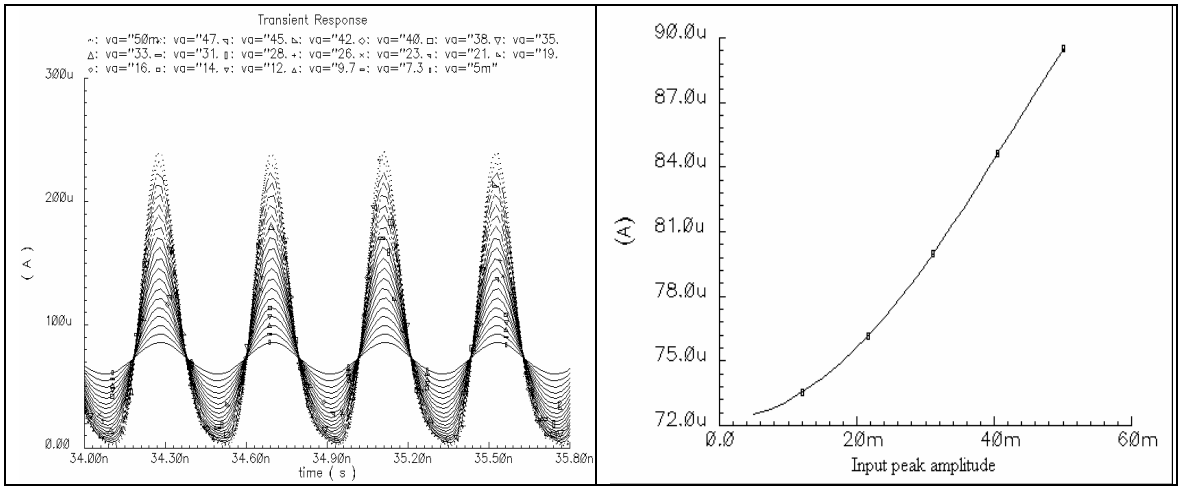


FIG 2.6 POOR RECTIFICATION AT LOW SIGNAL LEVELS–CURRENT MIRROR AS RECTIFIER

2.2.4 Complete Schematic Using Current Mirror as a Rectifier

The basic architecture has been implemented in the circuit level in [2] and a test strategy has been proposed for the use of the RF RMS detector to characterize the gain and 1-dB compression point of an LNA. The voltage-to-current conversion has been performed using a simple common source transistor with RC source degeneration. The input stage is described in detail in section 2.3.3. The average value of the rectified current has been extracted using a simple PMOS current mirror load with capacitor C2 (Fig 2.7) and converted to a DC voltage using a resistor. The post-rectification is described in detail in section 2.3.2. The complete schematic is shown below in figure 2.7.

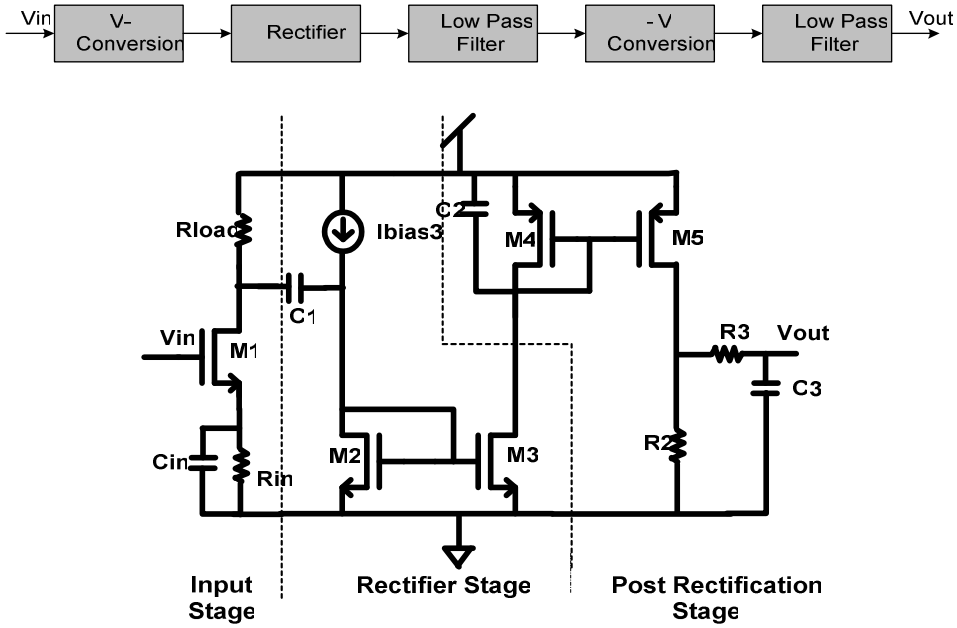


FIG 2.7 RMS DETECTOR USING CURRENT MIRROR AS RECTIFIER

In figure 2.7, AC current injected during the positive cycle splits up between the parasitic capacitances of M1 and the rectifier (through C1). Current efficiency, which is defined as the ratio of the current injected into the rectification stage to the current generated in the V-I conversion stage, is thus reduced. The current efficiency can be increased by increasing the aspect ratio of M1 which in turn will increase the input parasitic capacitance. This problem has been solved in [2] by using current mirrors with current gain. A detailed analysis on the design of these current mirrors will be given in section 2.3.4.

The RMS detector with current mirror as rectifier [2] achieves a linear dynamic range of 20 dB with a slope of 60mV/dBm with 10mW of power consumption at 3.3V

power supply. It presents an input capacitance of 22.5 fF and occupies an area of just 0.013 mm^2.

2.2.5 Disadvantages of RMS Detector Using Current Mirror as Rectifier

The most fundamental disadvantage of using the current mirror as a rectifier as demonstrated in section 2.2.3 is that the resolution at low signal levels is reduced. Another striking disadvantage is the fact that the dynamic range of the RMS detector extends only up to 0 dBm. This precludes the use of this RMS detector for characterization of the DUT described in section 2.1 as the input 1-dB compression point of the LNA is 1.67 dBm. The following section describes an alternate solution.

2.3 RF RMS DETECTOR USING CLASS AB CURRENT RECTIFIER

The problems associated with using a current mirror as a rectifier can be solved by using a Class AB current rectifier. It has been shown in section 1.2.1 using appropriate examples derived from literature that the Class AB rectifier is better than the Class B rectifier in avoiding the problem of the dead-zone. The design considerations of the Class AB along with the details on how it avoids the above mentioned problems are described below.

2.3.1 Class AB Rectifier

The Class AB rectifier along with the I-V conversion and filtering is shown in figure 2.8.

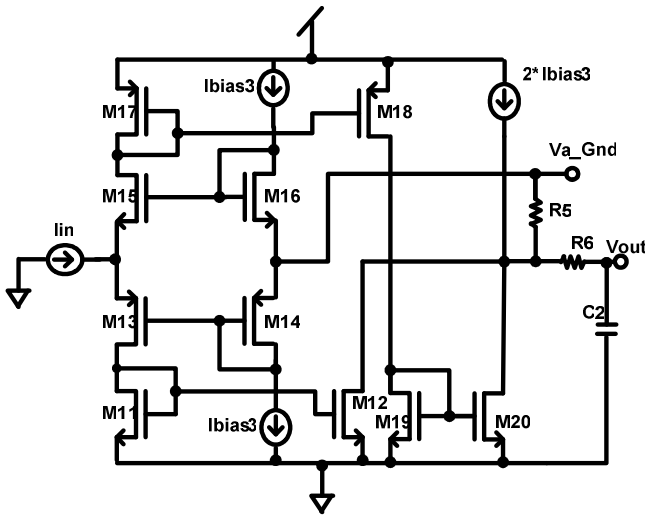


FIG 2.8 CLASS AB RECTIFIER

A small DC bias current Ibias3 and diode connected transistors M16 and M14 are used to generate a constant potential drop of Vtn+Vtp between the gates of the common-gate transistors M15 and M13, thus maintaining the transistors in weak inversion. The DC potential at the source of M16 and M14, which defines the DC voltage at the source of M15 and M13 due to symmetry, has been connected to analog ground. Positive input currents (Iin >0) flow through M13 thus causing Vsg_{13} to increase and Vgs_{15} to decrease. Thus, during the positive cycle, M15 is in the cutoff region and the current is mirrored through transistors M11-M12 to the output. During the negative cycle, the opposite happens and negative input current flows through M15 and M13 operates in the cutoff region. The negative current is mirrored through M17-M18 and is mirrored again through M19-M20 to add another level of inversion so that the positive and negative halves can be added in the same direction to produce full wave rectification. This technique suffers from unequal signal delays of the negative and positive components

due to the extra current mirror in the negative cycle which produces a phase difference between two halves of current as shown below in figure 2.9. The criticality of the phase shift is explained below.

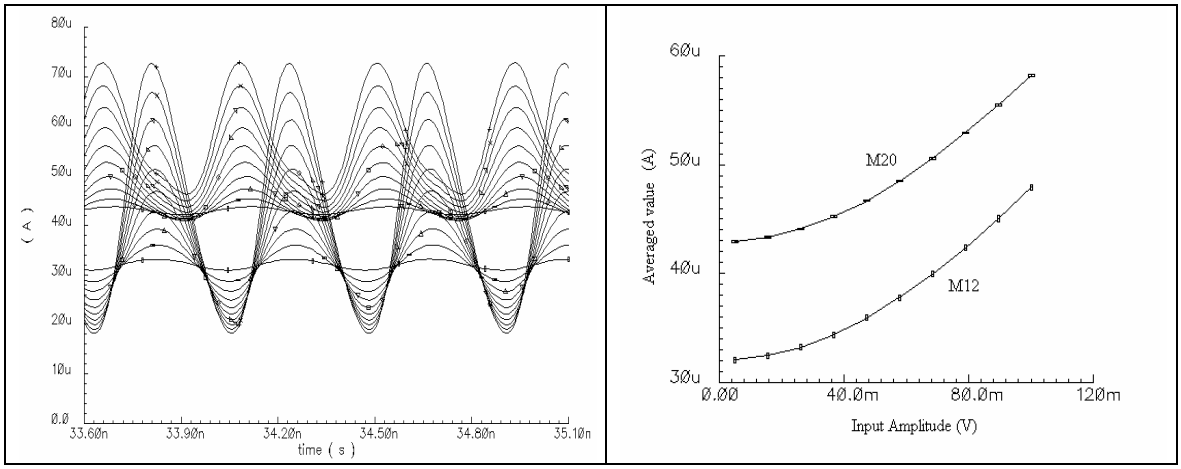


FIG 2.9 POSITIVE AND NEGATIVE COMPONENTS OF THE RECTIFIED CURRENT

Figure 2.10 on the next page shows the total added transient current through the resistor R5 and its averaged value for different amplitudes of the input RF signal. It can be seen that the phase shift is not a limitation because the total rectified waveform is finally averaged using the R-C filter at the output and hence the high frequency components are filtered out.

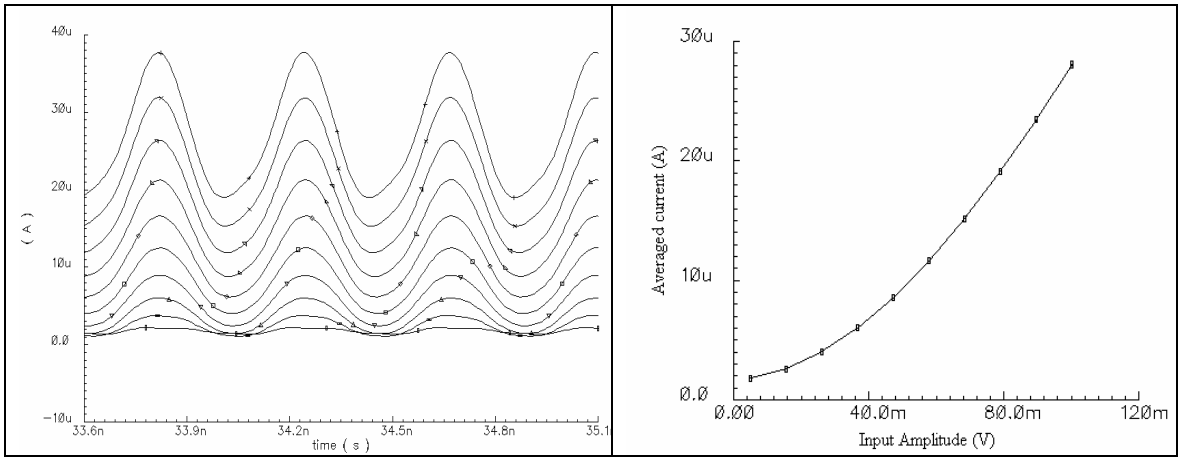


FIG 2.10 RECTIFIED COMPONENTS ADDED TOGETHER

However it must be noticed in the figure 2.9 that there are unequal DC offsets (different from Ibias3) in the positive and negative components of the rectified signal. This is because the rectifier is subject to mismatches in the DC current mirroring in the current mirrors M11-M12 and M19-M20. The DC drain-source voltages of M12 and M20 are very close to half the supply voltage and hence much larger than their gate-source voltages. M12 and M20 are biased by a constant DC source 2*Ibias3 in figure 2.8. Ideally, 2*Ibias3 provides the sum of the two DC currents in M12 and M20. The difference in the current not supplied by 2*Ibias3 is either sourced or sunk through the resistor R5. This can be reduced by using a large resistor value. But, a large value can cause a significant DC offset at the output which is undesirable. Further, the DC offset for any two RMS detectors at different nodes would be different because of process variations. This problem is described in more detail in the section on testing results.

However, by using cascode current mirrors, this problem can be rectified. Although this has not been attempted in this RMS detector in order to enable operation

at RF frequencies, the RMS detector designed for the built-in-test of the 350 MHz boost filter has incorporated this solution (described in the section 3).

It can also be seen from figure 2.9 that the current at the drain M20 shows a certain amount of filtering when compared to the current at the drain of M12 (this can be seen by the fact that the lowest points in the rectified signal do not touch or cross the DC level). This is clearly seen in the figure 2.11 showing the current in the NMOS current mirror M19-M20. It can be seen that the current in M19 also shows a certain amount of filtering although reduced.

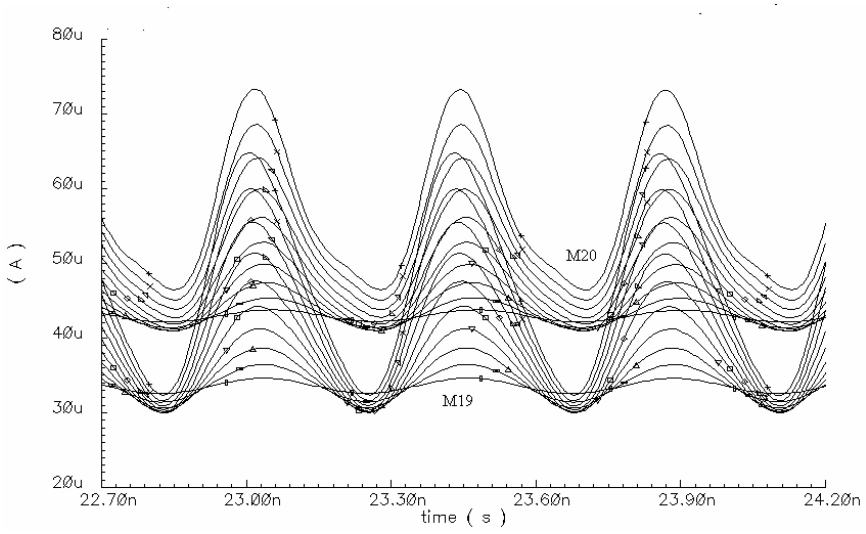


FIG 2.11 NEGATIVE COMPONENT OF THE RECTIFIED CURRENT

This is because of the fact that the current in M20 (M20 is referenced to figure 2.8) has passed through two current mirrors each with pole locations of the order of 5 GHz. Hence, with two poles very close to each other, they reflect as a pole at half the frequency which is located very close to the frequency of interest. This explains the

filtering action that is observed at the drain of M20 in figure 2.9 (left) and hence the reduced slope in the transfer characteristic of the average AC current at the drain of M20 in figure 2.9 (right). This effect is not seen in the AC current at the drain of M12 (figure 2.9) (M12 is referenced to figure 2.8) because of the fact that the current at the drain of M12 passes through only one current mirror and whose pole location is at 5 GHz. For lower pole locations, the advantage of full wave rectification would be lost.

It can be seen that the full-wave rectification through the use of Class AB rectifier has a number of advantages over using a simple current mirror as a rectifier. First of all, the dynamic range is now increased because the averaging is now done over the full wave rectified waveform (the final transfer characteristic is shown in figure 2.24 which shows the increased dynamic range as compared to the dynamic range of the RF RMS detector using half-wave rectification [2]) and further, the DC current in the rectifier can be subtracted/added at the output and hence the offset at the output can be reduced (in this case it is added as 2*Ibias3 in figure 2.8 as the output of two NMOS current mirrors are added at the output. If the output of two PMOS current mirrors are added at the output, in the case where the extra inversion is applied to the positive component, 2*Ibias3 would have been subtracted). NMOS current mirror was the obvious choice because of reduced aspect ratio for the same trans-conductance and thus lesser parasitic capacitances.

The main frequency limitation of the rectifier is the pole location at the input of the rectifier. The fact that the input node is a low impedance node along with the fact that the circuit has been pre-biased enables the frequency of operation to be extended to

the GHz range. Since the gates of M15 and M13 are attached to signal ground, the location of the input pole can be approximately calculated as shown in the expression below.

$$\frac{1}{\left(\frac{1}{gm_{15}}\left\|\frac{1}{gm_{13}}\right.\right)\cdot\left(Cgs_{15}+Cgs_{13}+Csb15+Csb13\right)}$$

At very high frequencies, there may be significant phase shift between the positive and negative halves. This could lead to overlap in the positive and negative rectified waveforms and we may loose the advantages of full wave rectification described above. This can be reduced by adding additional phase shift in the negative direction also. The pole locations in the current mirrors (M17-M18 and M11-M12) are designed to be at twice the frequency of operation. A reduction in the pole locations in the current mirrors can cause loss of resolution in the transfer characteristic of the RMS detector sue to loss in the current mirrors.

2.3.2 Post-Rectification Current-to-Voltage Conversion and Filtering

For the sake of simplicity, an RC filter is used for extracting the DC value from the rectified signal. The RMS detector is intended to operate at 2.4 GHz and the R-C filter at the output has a single pole response. For 40 dB suppression in the output ripple, the corner frequency of the RC filter should be located at 24 MHz. Hence the time constant at the output is 6.6ns. Which implies a filter with a 4K resistor at the output would need a 1.65 pF capacitor. The amount of suppression at the output needs to be chosen by keeping in mind the time constant that can be tolerated at the output and the

area constraint which will determine the maximum value of the capacitor that can be used.

2.3.3 Input Voltage-to-Current Conversion and Current Magnification

The input stage for the proposed RMS detector using the Class AB current rectifier is the same as that of the RMS detector with current mirror rectifier in [2] and is described in detail in this section. The simplest way to perform voltage-to-current conversion is to use a common-source transistor.

The trans-conductance of the input stage is very critical as it dictates the output dynamic range of the RMS detector i.e. the maximum and minimum DC voltage at the output of the RMS detector in its linear region of operation. The trans-conductance of a common-source transistor is dictated by the input gate bias and its bias current. The dependence of the operating point of the input transistor on the input voltage can be removed by biasing the transistor with a fixed current source. This is shown in figure 2.12.

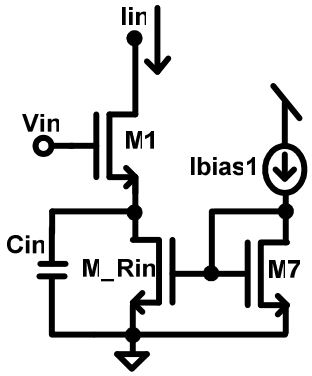


FIG 2.12 INPUT STAGE

The current through the input transistor is fixed at Ibias1 through M-Rin which operates in the saturation region. This makes the trans-conductance independent of the gate bias voltage. Cin is added in order to reduce the effective source degeneration at RF frequencies. The trans-conductance is given by

$$G_m = \frac{g_m}{1 + g_m Z_s} = \frac{g_m}{1 + g_m \left(R_{in} \left\| \frac{1}{sC_{in}} \right. \right)} = \frac{\frac{1}{R_{in}} \left(1 + sR_{in}C_{in}\right)}{\left(1 + \frac{sC_{in}}{g_m}\right)} \tag{2.1}$$

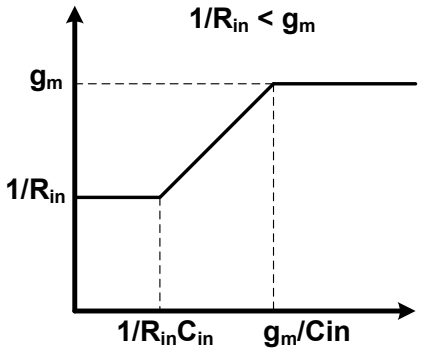


FIG 2.13 INPUT TRANS-CONDUCTANCE AT HIGH FREQUENCY

It can be seen from figure 2.13 and equation 2.1 that there is a pole (g_m/C_{in}) and a zero ($1/R_{in}C_{in}$). The capacitor Cin shorts the source of M1 to ground at high frequency thus causing the effective trans-conductance to be equal to gm. The value of g_m/C_{in} is chosen to be before the frequency of interest (Cin was chosen to be 600 fF for this design). For the targeted frequency of 2.4 GHz and accounting for process variations, the location of the pole should not be greater than 1 GHz in the design (figure 2.15).

Figure 2.14 shows the variation the trans-conductance for a fixed gate bias of 1.8 V (the gate bias voltage for the LNA and buffer) and varying bias currents from 50 uA to 400 uA.

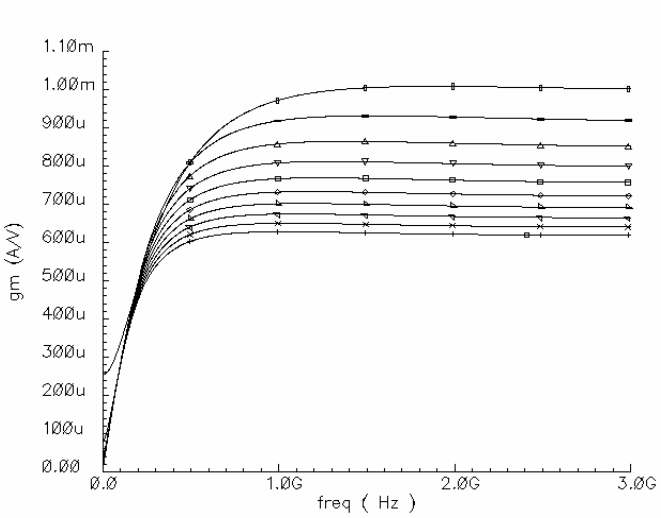


FIG 2.14 VARIATION OF INPUT TRANS-CONDUCTANCE WITH BIAS CURRENT

Capacitor Cin plays an important role in the input impedance of the RMS detector. It can be shown that the total input impedance is given below in equation (2.2) (R_{in} is the R_{ds} of transistor M_Rin and g_{m1} and C_{gs1} are the trans-conductance and gate-source capacitance of input transistor M1 in figure 2.12).

$$Z_{in} = \frac{1}{sC_{gs1}} + \frac{R_{in}}{1 + sC_{in}R_{in}}\left(1 + \frac{g_{m1}}{sC_{gs1}}\right) \tag{2.2}$$

For $sC_{in}R_{in} >> 1$ at Rf frequencies, the input impedance becomes:

$$Z_{in} = \underbrace{\frac{1}{sC_{gs1}} + \frac{1}{sC_{in}}}_{\text{Reactive}} \Big| \underbrace{-\frac{g_{m1}}{\omega^2 C_{in} C_{gs1}}}_{\text{Resistive}} \tag{2.3}$$

A shown in the equation above, the reactive component is composed of Cin in series with Cgs1. Hence for values of C_{in} much larger than C_{gs1}, the net reactive component will only be dominated by C_{gs1}. However, for values of C_{in} smaller than or comparable to C_{gs1}, the net capacitance at the input would decrease.

For a common source transistor with only a source degeneration resistor, the input impedance increases. However, the addition of the source degeneration capacitance removes the effect of the source degeneration resistor by creating a short across the resistor as frequency increases. Hence, the effective input impedance decreases as the value of the capacitance increases. This is shown in figure 2.15.

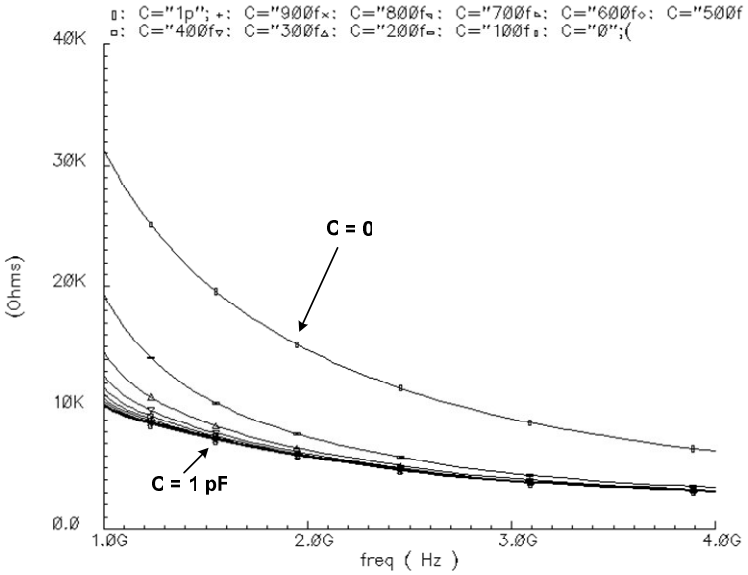


FIG 2.15 VARIATION OF INPUT IMPEDANCE WITH SOURCE DEGENERATION CAPACITANCE

A large bias current (and hence a large trans-conductance) would demand a large aspect ratio for the input transistor in order to maintain sufficient overdrive. This would in turn increase the parasitic input capacitance. This necessitates the use of current magnification before the AC current can be fed to the rectifier stage because a part of the AC current is absorbed by the parasitic present at the input of the rectifier which reduces the current efficiency, which is defined as the ratio of the current injected into the rectification stage to the current generated in the V-I conversion stage.

2.3.4 Bandwidth Enhanced Current Mirror

The bandwidth of a simple current mirror is at the maximum half the f_t of the MOSFET [30]. In our case of current magnification where the ratio of the current mirror is greater than unity, the maximum frequency of operation is far lesser than half of ft because increase in the current would mean increased power consumption and larger transistor sizes to maintain sufficient overdrive to keep them in saturation. The bandwidth enhancement using the high speed current mirror resistive compensation technique [30] provides a solution to this problem. The schematic and small-signal model are shown in figure 2.16. The technique is based upon using a resistor between the gate and drain of the diode connected transistor in a current mirror so as to introduce an extra pole-zero pair and convert the single pole response to a second order transfer function shown below.

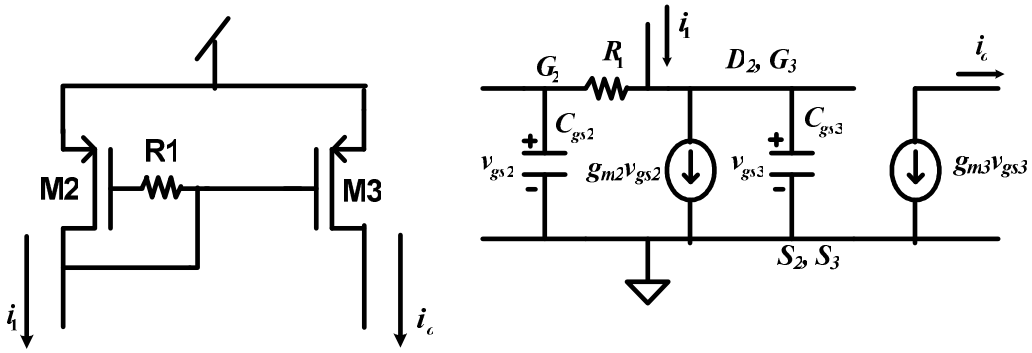


FIG 2.16 BANDWIDTH ENHANCED CURRENT MIRROR

The output to input current transfer function can be derived as [17]:

$$\frac{i_o}{i_1} = \frac{\frac{g_{m3}}{g_{m2}}\left(1 + sC_{gs2}R_1\right)}{1 + \frac{s\left(C_{gs3} + C_{gs2}\right)}{g_{m2}} + \frac{s^2 C_{gs2}C_{gs3}R_1}{g_{m3}}} \tag{2.4}$$

This yields a zero at $\omega_Z = \frac{1}{C_{gs2}R_1}$ and two poles. In [30], the design is done such that $R_1 = 1/g_{m2}$ and $C_{gs2} = C_{gs3}$, thus canceling one of the poles with the zero and extending the bandwidth to g_{m2}/C_{gs3}.

Using bandwidth enhanced current mirrors, the magnitude of the current being fed into the rectifier can be increased thus increasing the resolution in the transfer characteristic of the RMS detector. By placing the zero before the two poles, a slight peaking can be obtained in the response. If the peak is designed such that it is at least 2-3 times the desired frequency of operation, then the actual gain at the desired frequency of operation would only be slightly greater than the DC gain. This slight raise would help in maintaining the desired gain amidst the losses in the parasitic capacitances. The

following figure shows the nature of the peaking for different values of the resistor R1. At the peak frequency, the current mirror turns out to be highly unreliable (detailed explanation given in the next paragraph). Hence, although the peaking and bandwidth enhancement are beneficial, the value of the resistor should be chosen such that the peak frequency is placed at least twice the frequency of interest. A physical intuitive reason for the peaking is given below in figure 2.17.

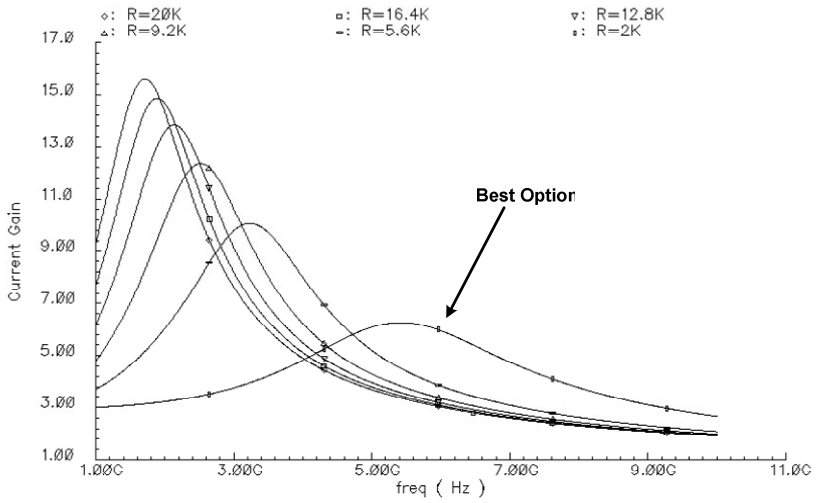


FIG 2.17 VARIATION OF PEAK FREQUENCY WITH RESISTOR

The peaking due to the pole and zero can be physically explained as follows. At high frequencies, the impedance due to the capacitance C3 (refer to figure 2.18) reduces and C3 is charged up. R is high impedance at all frequencies and hence the charge stored across C2 is different from the charge across C3, thus, causing V2 and V3 to be different. M2 and M3 no longer act as current mirrors and this causes peaking in the frequency response.

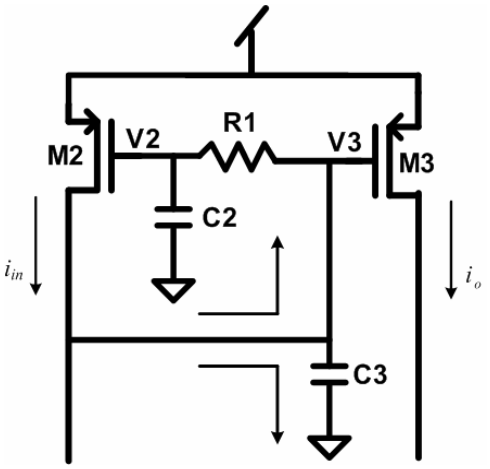


FIG 2.18 PEAKING IN BANDWIDTH ENHANCED CURRENT MIRRORS

In the realized RMS detector, two levels of current mirroring were performed in order to improve the current efficiency discussed before. The partial schematic showing the input stage and the current magnification stage is shown below in figure 2.19. M2-M3 and M6-M9 form the two bandwidth-enhanced current mirrors. M7-M5 forms a DC current subtractor which subtracts a part of the magnified DC current from M3. This helps in reducing the DC current in M6 and hence reducing its aspect ratio and also reduces the power consumption because not all DC current is amplified. Resistor R2 acts as high impedance and prevents any AC leakage through the gate-drain capacitance of M5 from creating an AC voltage at the gate of M7 and M_Rin.

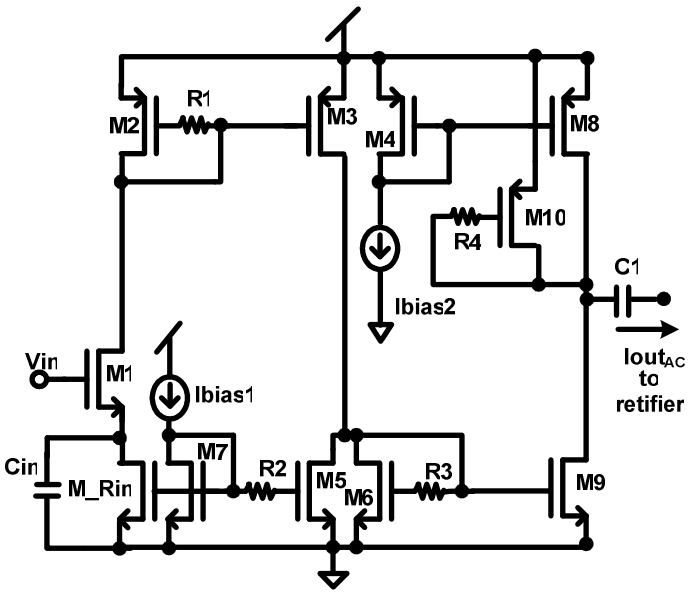


FIG 2.19 INPUT STAGE

Ibias2 is chosen such that the current through M8 is equal to the current through M9. Now, without M10, the drain nodes of M8 and M9 are shorted together which will create high impedance at that node. This implies that there could be a wide variation in the voltage of that node with process. Hence, that node has been biased through a gate drain connected transistor M10. R4 presents high impedance to any AC current leakage to the gate of M10. The sizing of M10 is critical because a small aspect ratio would create a large drain-source drop across the transistor and reduce the drain-source voltage drop of M9. However, increasing the size of M10 would increase the parasitic capacitance at that node. The sizing of M10 thus plays an important role in the current efficiency which has been defined before as the ratio of the current generated in the input stage to the ratio of the current fed into the rectifier.

2.3.5 Complete Schematic of RF RMS Detector with Class AB Rectifier

The complete schematic of the RF RMS detector is shown below in figure 2.20. Table 2.2 lists the component values of the devices referenced to figure 2.20.

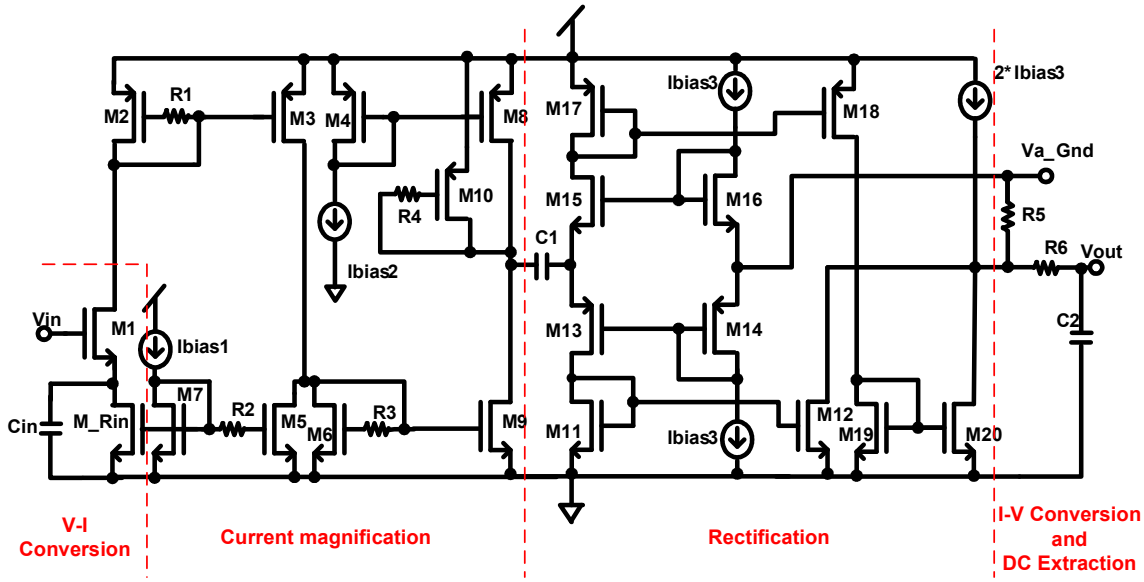


FIG 2.20 RF RMS DETECTOR–COMPLETE SCHEMATIC

TABLE 2.2 COMPONENT DESIGN VALUES–RF RMS DETECTOR

M1	4 µm/0.4 µm, m=2	Cin	600 fF	M10	6 µm/0.4 µm, m=3
M2	6 µm/0.4 µm, m=2	R1	2 KΩ	M11	6 µm/0.4 µm, m=1
M3	6 µm/0.4 µm, m=6	R2	2 KΩ	M12	6 µm/0.4 µm, m=1
M4	6 µm/0.4 µm, m=2	R3	2 KΩ	M13	6 µm/0.4 µm, m=2
M5	2 µm/0.4 µm, m=2	R4	10 KΩ	M14	6 µm/0.4 µm, m=2
M6	6 µm/0.4 µm, m=2	R5	4 KΩ	M15	6 µm/0.4 µm, m=1
M7	2 µm/0.4 µm, m=2	Ibias1	400 µA	M16	6 µm/0.4 µm, m=1
M8	6 µm/0.4 µm, m=6	Ibias2	200 µA	M17	6 µm/0.4 µm, m=2

TABLE 2.2 (CONT.)

M9	6 µm/0.4 µm, m=6	Ibias3	20 uA	M18	6 µm/0.4 µm, m=2
M_Rin	2 µm/0.4 µm, m=1	C1	5 pF	M19	6 µm/0.4 µm, m=1
R6	4 KΩ	C2	600 fF	M20	6 µm/0.4 µm, m=1

Figure 2.21 shows the complete realized RMS detector on silicon in 0.35 um technology.

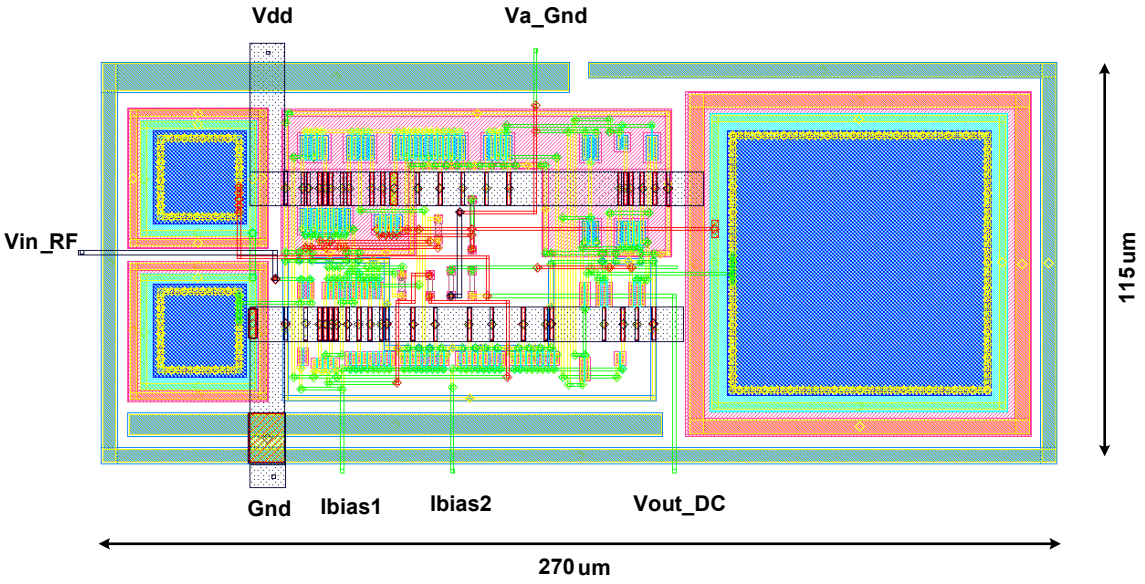


FIG 2.21 RF RMS DETECTOR–LAYOUT

2.3.6 Simulation Results of RF RMS Detector with Class AB Rectifier

Figure 2.22 on the next page shows the input parasitic capacitance of the RF RMS detector. The RF RMS detector using Class AB current rectifier has an input capacitance of 13 fF at the frequency of interest.

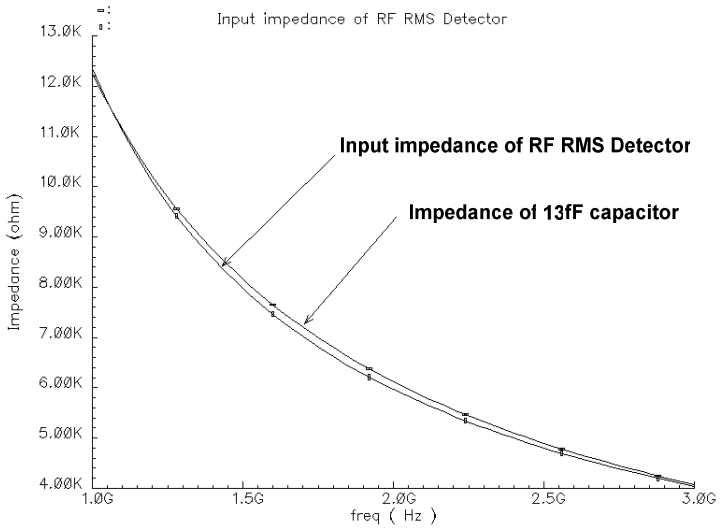


FIG 2.22 RF RMS DETECTOR–INPUT PARASITIC CAPACITANCE

Figure 2.23 on the next page shows the transfer characteristic of the RF RMS detector with output DC voltage on the y-axis and input peak voltage amplitude on the x-axis. The characteristic is linear from 20mV and extends beyond 450 mV. 400mV of peak input amplitude corresponds to 2dBm of input power (referenced to 50 ohms) which is greater than the 1-dB compression point of the LNA (1.67 dBm). 20mV corresponds to approximately -24 dBm of input power (referenced to 50 ohms) which is lower than the maximum specification of -20 dBm. Hence, the dynamic range of the RF RMS detector is sufficient to characterize the LNA.

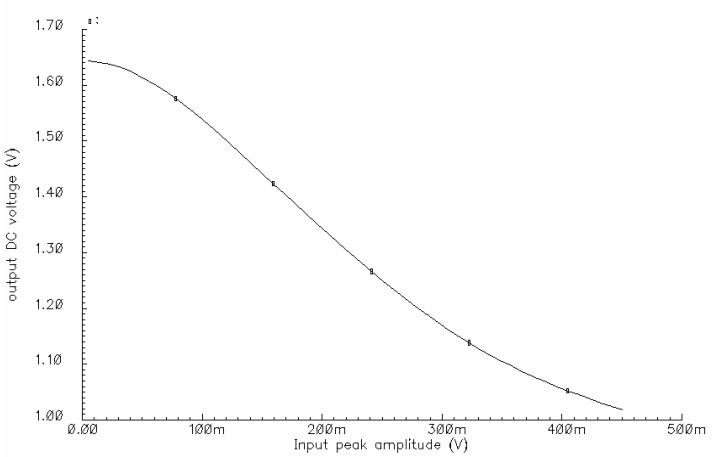


FIG 2.23 RF RMS DETECTOR–TRANSFER CHARACTERISTIC (V/V)

Figure 2.24 shows the transfer characteristic of the RF RMS detector in V/dBm. This graph is most important for estimating the gain and linearity of the LNA as has been demonstrated in the next section. The y-axis shows the DC output voltage of the RMS detector corresponding to the input power (in dBm) at its input.

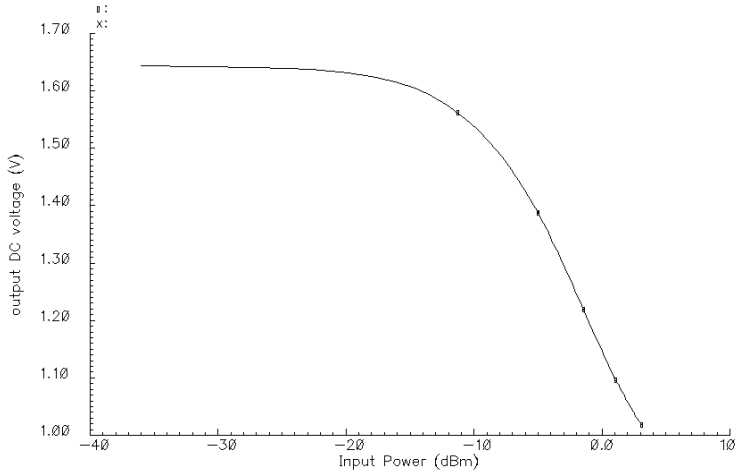


FIG 2.24 RF RMS DETECTOR–TRANSFER CHARACTERISTIC (V/DBM)

2.4 BUILT-IN-TEST STRATEGY FOR THE LNA-BUFFER WITH RMS DETECTORS

The test setup of the LNA and buffer with the RMS detectors is shown below in figure 2.25.

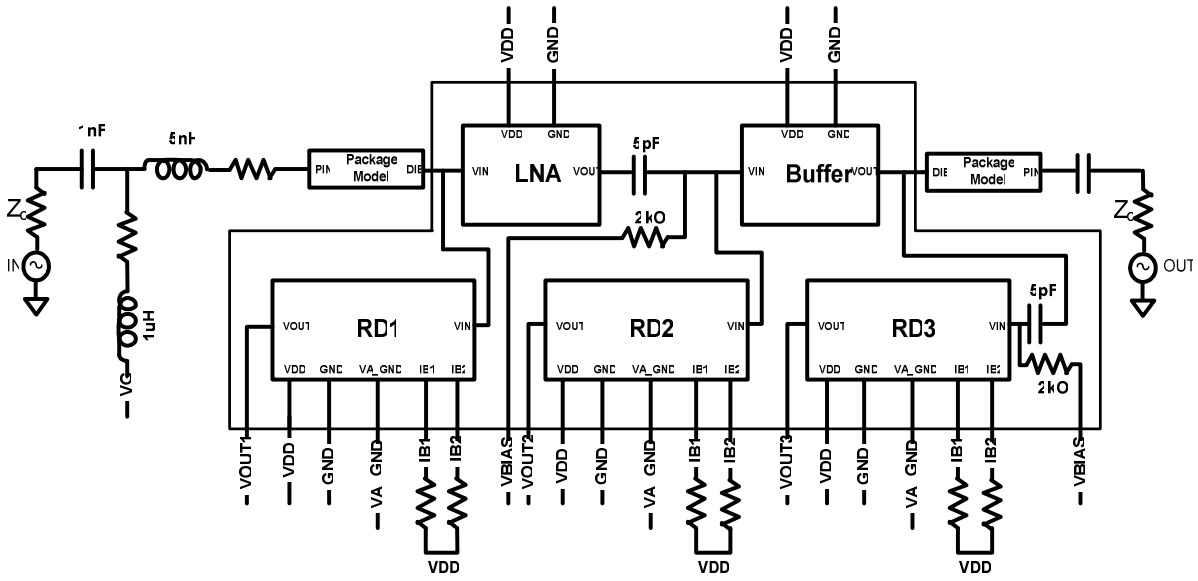


FIG 2.25 TEST SETUP–LNA AND BUFFER WITH RF RMS DETECTORS

[2] outlines the testing strategy for the characterization of the LNA and buffer with the RF RMS detectors. A sinusoidal signal with suitable input power is given such that the output DC voltages can be mapped to corresponding powers that lie in the input dynamic range of the stand-alone RMS detector. This is not so difficult a task as it seems. This power can be estimated by looking at the transfer characteristic of the stand-alone RMS detector in V/dBm and keeping in mind the expected gain/loss of the

LNA/buffer, the maximum power that can be tolerated at the input of the LNA and the s11 achieved in the setup. The outputs of the three RMS detectors are then mapped to the transfer characteristic of a stand-alone RMS detector to predict the gain. Figure 2.26 shows the gain estimation of the LNA and buffer with the RF RMS detectors. It can be seen that the estimated value exactly matches the gain specified in table 2.1.

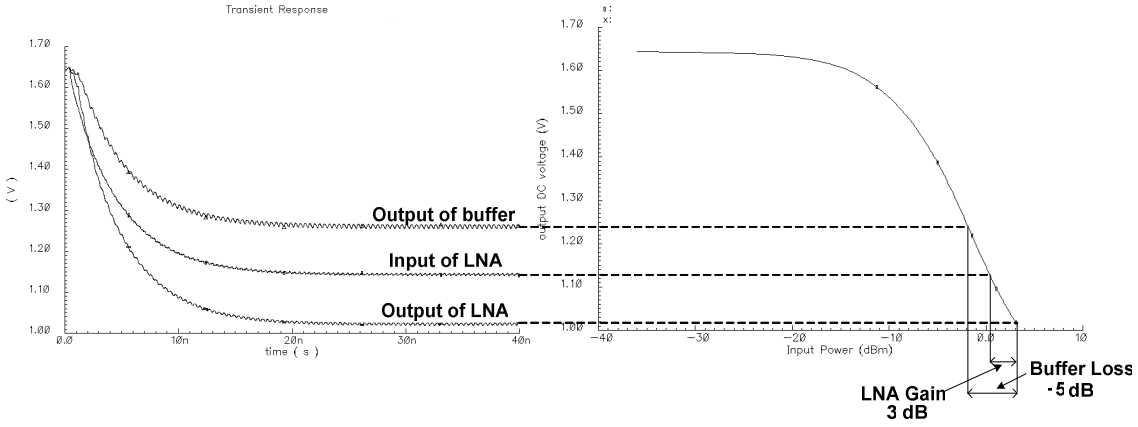


FIG 2.26 LNA GAIN ESTIMATION WITH RF RMS DETECTORS

For estimating the 1-dB compression point the input power is swept up to a value greater than the larger of the two 1-dB compression points of the LNA and the whole system. Next, the outputs of the three RMS detectors are plotted with respect to the input power on the x-axis. For a given input amplitude, the gain of the LNA can be measured as the difference in dB from the response of the detector at the output to the reference response (output of the detector at the input). As it can be observed, the input amplitude for which the gain decreases by 1dB can be easily extrapolated. Figure 2.27 shows the 1-

dB compression point estimation of the LNA. Alternatively, the gain/loss of the LNA/buffer can also be estimated from figure 2.27.

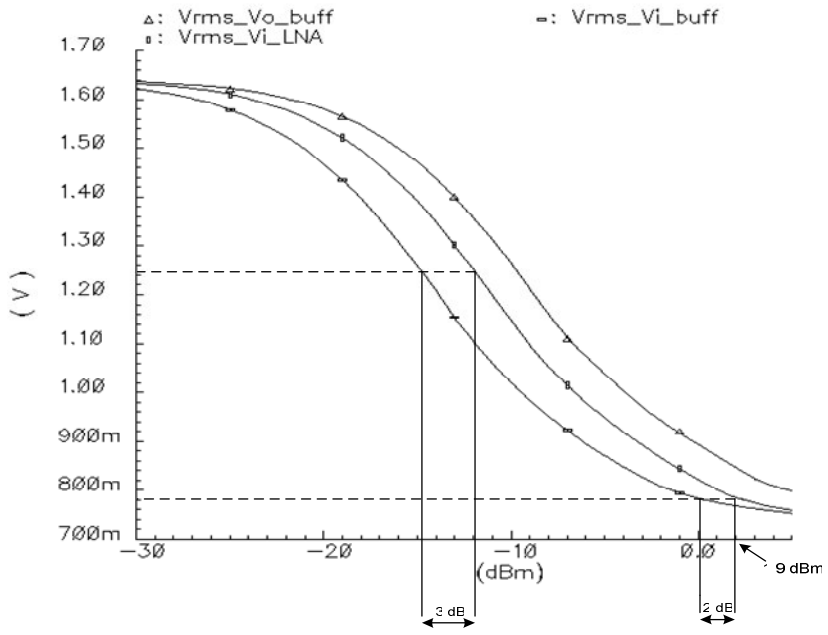


FIG 2.27 LNA LINEARITY ESTIMATION WITH RF RMS DETECTORS

It has been shown that the 1-dB compression point of the LNA and the gain of both the LNA and the LNA-buffer system have been estimated very accurately with the RF RMS detector.

2.5 TESTING RESULTS

The LNA and buffer along with the RMS detectors were implemented on silicon in TSMC 0.35 um technology and figure 2.28 shows the chip microphotograph. A stand-alone buffer was laid out for de-embedding the loss of the buffer and a stand-alone RF RMS detector for creating a reference mapping table of RF input amplitude versus the

output DC voltage. ESD protection was applied to the input pins of the LNA and stand-alone RMS detectors.

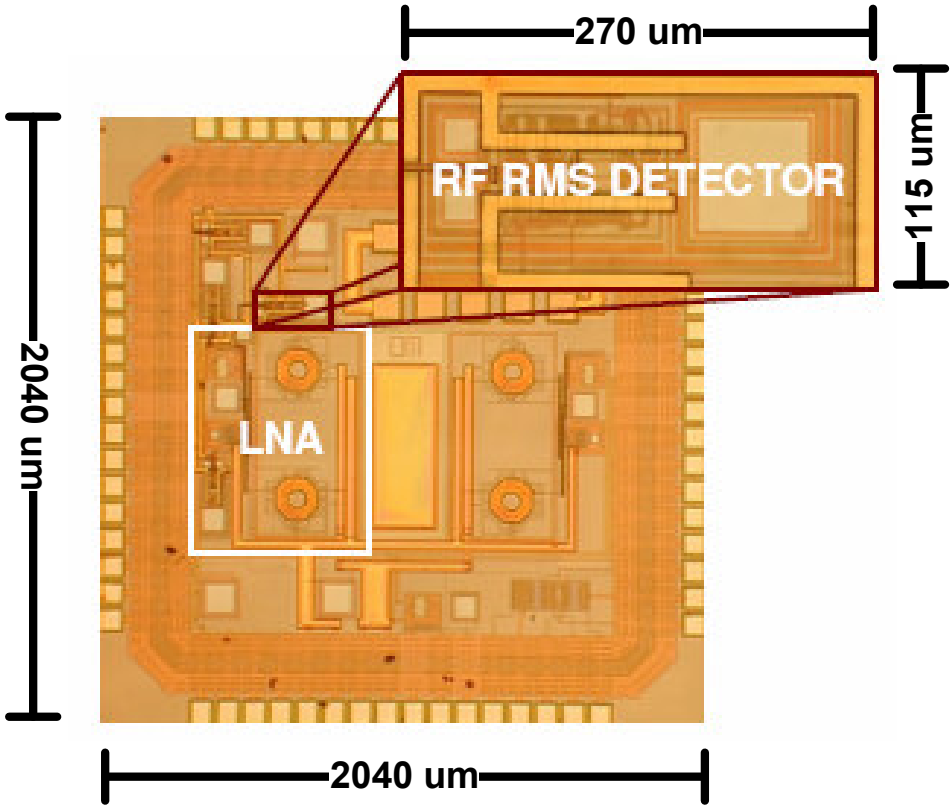


FIG 2.28 RF RMS DETECTION–CHIP MICROPHOTOGRAPH

A PCB was manufactured for simultaneous off-chip as well as on-chip testing the LNA-Buffer system using the off-chip testing equipment (network analyzer/signal generator/spectrum analyzer) and the RMS detectors respectively. Proper precautions were taken to filter out the DC signals using chip capacitors and regulators were used to stabilize the DC voltages. Ground planes were used to remove any interaction between the input and output traces of the LNA-Buffer system. Care was taken to ensure that the

resonant frequency of the passive chip components used in the input match and for biasing were at least four times greater than the frequency of interest (2.4 GHz). The RF connectors used on board were placed as close to the input and output pins as possible in order to prevent the traces from acting as transmission lines. Broad-band input match was used for the stand-alone buffer using a 50 ohms chip resistor.

2.5.1 Testing the Stand-Alone RF RMS Detector

It was found during the basic bias point test that the RMS detectors at the input of the LNA (RD1), output of LNA (RD2) and output of buffer (Rd3) had output offsets (from analog ground) which differed by more than 200mV. Upon checking the resistance between the analog ground pin and the output, it was found to be 80 K as opposed to the expected value of 8K. On further analysis, it was found that, if the N-well resistors are not made wide enough, their drawn width could be even ten times their expected value [31]. This fact had been overlooked during the implementation on silicon and the fault went undetected because the simulator used was not capable of indicating a minimum required width and the extracted value of that the simulator showed (i.e. the expected value) was deceiving. It has previously been mentioned in section 2.3.1 that there is a small DC current flowing through the resistor R5 (figure 2.8) because of the mismatch in the current mirrors. An increase in the resistor value will magnify that small DC current into a large output DC offset. Further, resistor values vary widely with process. Small changes in leakage currents combined with large variations in large resistor values with process can cause large and different offset voltages at the output of the RMS detectors. In order to reduce the offset at the output, output of the RMS

detectors were connected to analog ground and the output current was extracted. This make the two 40K resistors to become parallel to each other and reduce the offset.

Moreover, the resistor values in the bandwidth enhanced current mirrors are also approximately ten times their expected value. It can be seen from figure 2.18 that the bandwidth of the current mirrors drastically reduces and there can be excessive peaking in the current gain right at the frequency of interest. Hence, the RMS detectors cannot be expected to work at 2.4 GHz, the frequency at which they were targeted. Figure 2.29 shows the transfer characteristic of the RF RMS detector from 1 to 2.4 GHz.

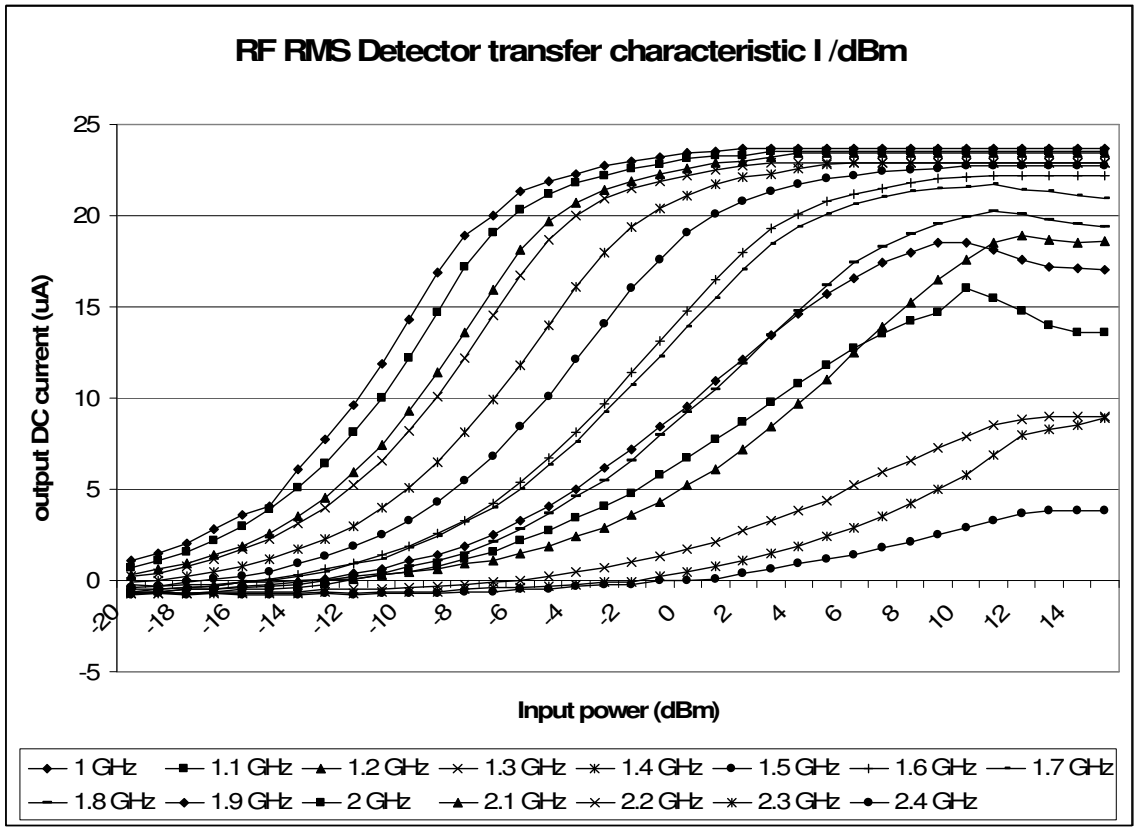


FIG 2.29 RMS DETECTOR TRANSFER CHARACTERISTIC–EXPERIMENTAL RESULT

The maximum frequency up to which the RMS detector can be expected to give meaningful results for the LNA and buffer gain and 1-dB loss would be 1.8 GHz.

2.5.2 LNA-Buffer Characterization with RF RMS Detectors

Figure 2.30 shows the LNA gain characterization using the RF RMS detectors connected to the input and output of the LNA. Estimation of the LNA gain is possible only up to 1.7 GHz as seen from figure 2.29. However, the network analyzer results affirm that the LNA gain peaks at approximately the frequency at which it was designed as seen in the following figure. However the LNA gain could not be recovered because of the problems associated with the estimation of the loss of the stand-alone buffer (section 2.5.3).

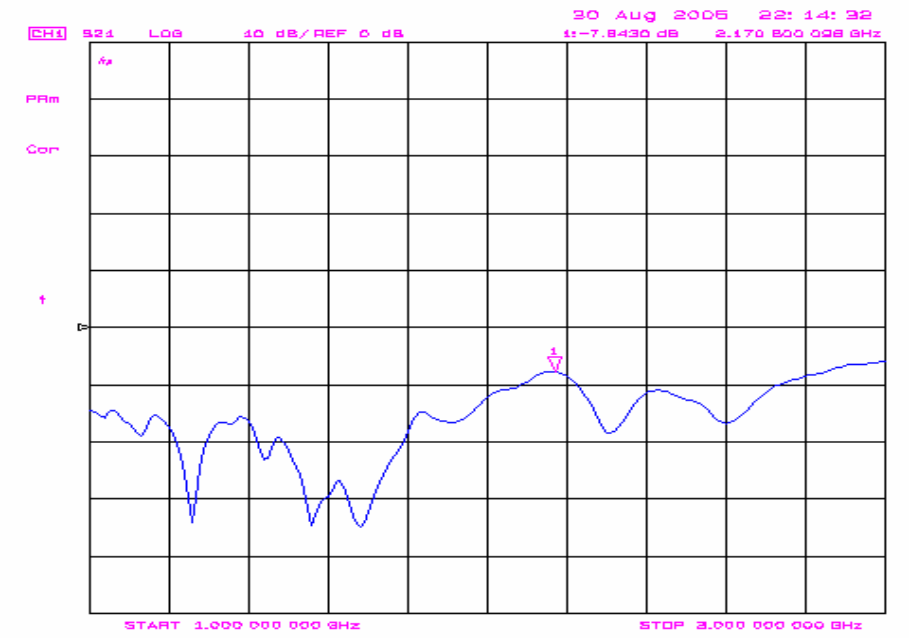


FIG 2.30 S_{21}–LNA-BUFFER COMBINATION–NETWORK ANALYZER

Figure 2.31 shows the estimation of the gain of the LNA using the RMS detectors up to 1.7 GHz. After that frequency, the RMS detection is unreliable because of the bandwidth limitation due to increased resistor values.

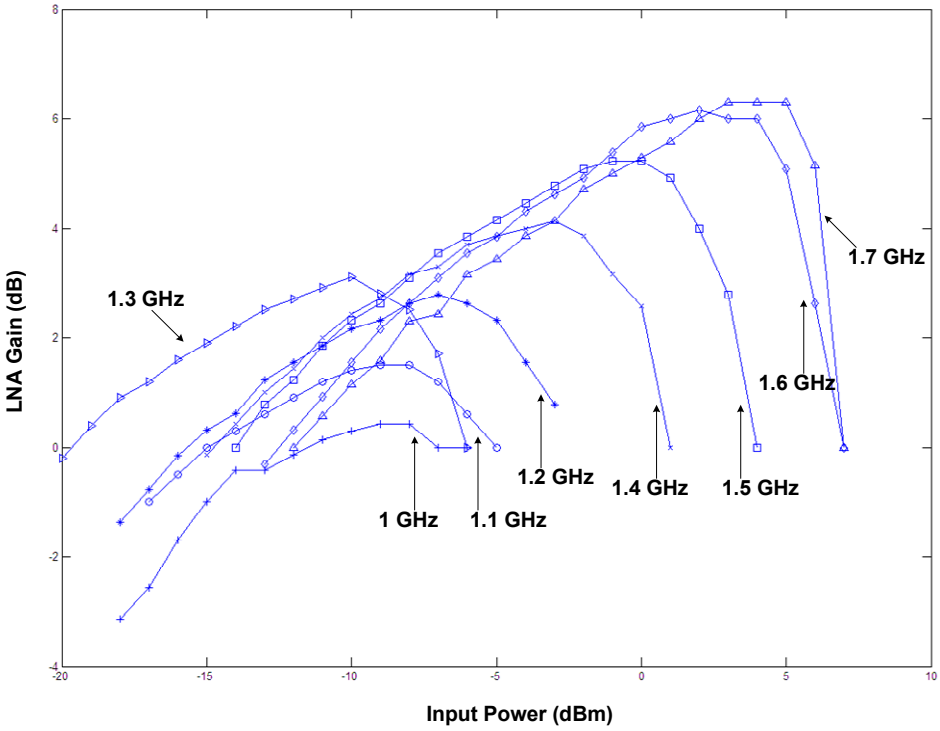


FIG 2.31 LNA GAIN–EXPERIMENTAL ESTIMATION USING RMS DETECTORS

It can be seen that the peak of the estimated gain is shifted with respect to the input power. This is because of the negative frequency response of the RMS detectors with respect to the input power (i.e. the RMS detectors respond to higher input powers as frequency increases). The gain of the LNA estimated by the RMS detectors does not match that of the simulation results because of the errors in the inductor modeling for the

chosen technology. However, the gain still increases with frequency as was expected though the absolute value of the LNA gain could not be verified by any other means because of the problems associated with the stand-alone buffer (section 2.5.3).

Figure 2.32 and figure 2.33 show the estimation of the 1-dB compression of the LNA using the RMS detectors and the spectrum analyzer at 1.7 GHz. It can be seen that the 1-dB compression point measured in both cases matches with an error of 0.5 dB.

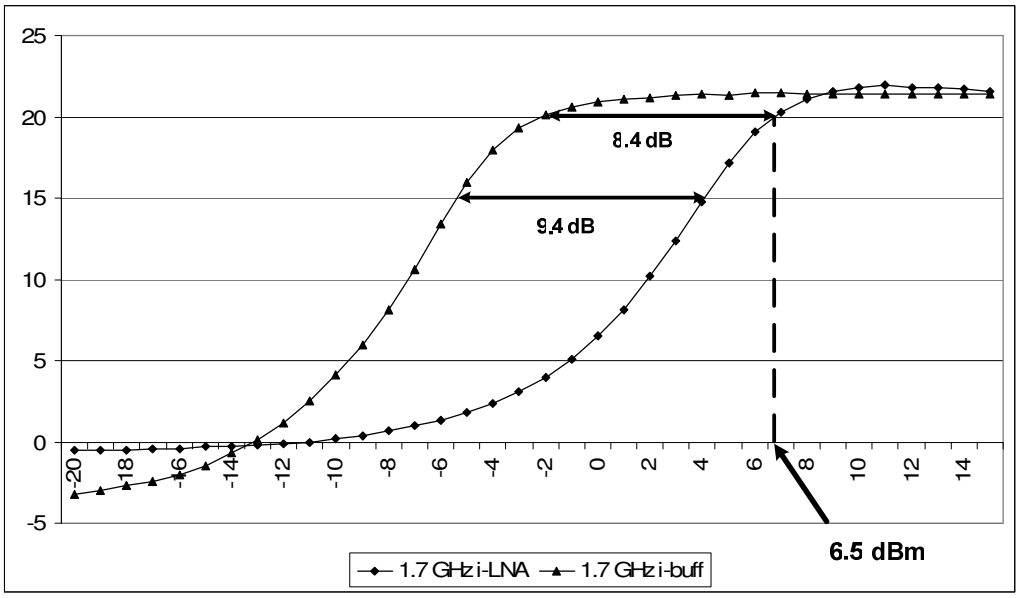


FIG 2.32 LNA LINEARITY–EXPERIMENTAL ESTIMATION USING RMS DETECTORS

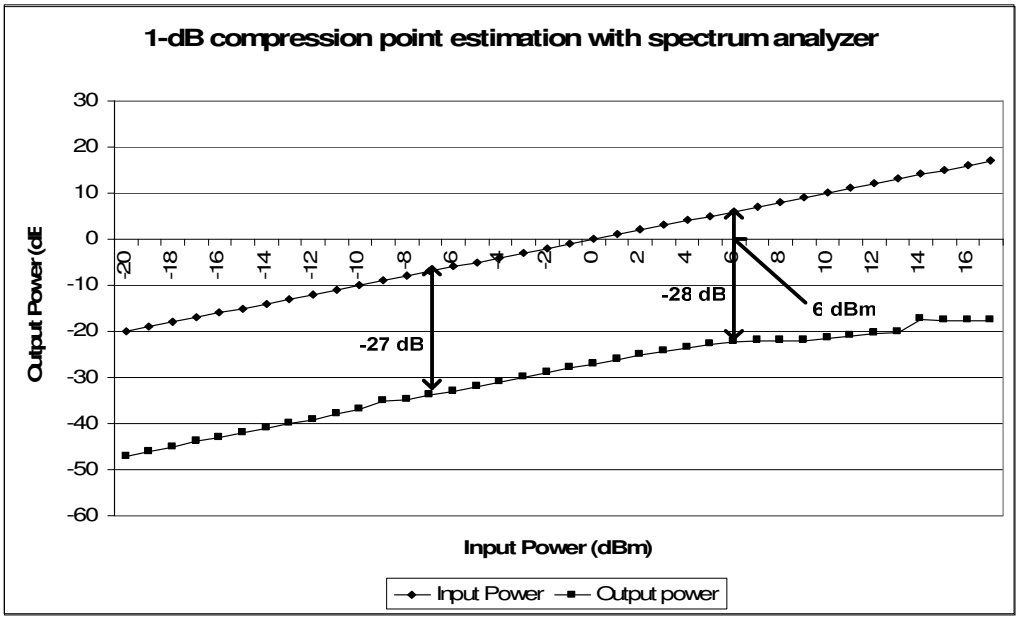


FIG 2.33 LNA LINEARITY–EXPERIMENTAL ESTIMATION USING SPECTRUM ANALYZER

2.5.3 Problems Associated with Stand-Alone Buffer

The de-embedding of the loss of the buffer connected to the LNA turned out to be almost impossible because of the fact that the stand-alone buffer has a bond-pad connected to its input which produces some resonant gain whereas this is not present in the case of the buffer connected to the LNA. Because of the resonant gain of the bond-pad, the signal level at the input of the stand-alone buffer is very different from the signal at the input of the buffer connected to the LNA. Figure 2.34 shows the input match of the stand-alone buffer showing the way it is connected. Because of the presence of the 2K ohm biasing resistor, it was impossible to cancel the resonant gain of the bond-wire. If the 2K ohm resistor had been designed to be a 50 ohm (Z_o) resistor (broad band input match inside the chip), then it would have been possible to acquire the

loss of the buffer because now, the bond-wire inductance is terminated in a low impedance.

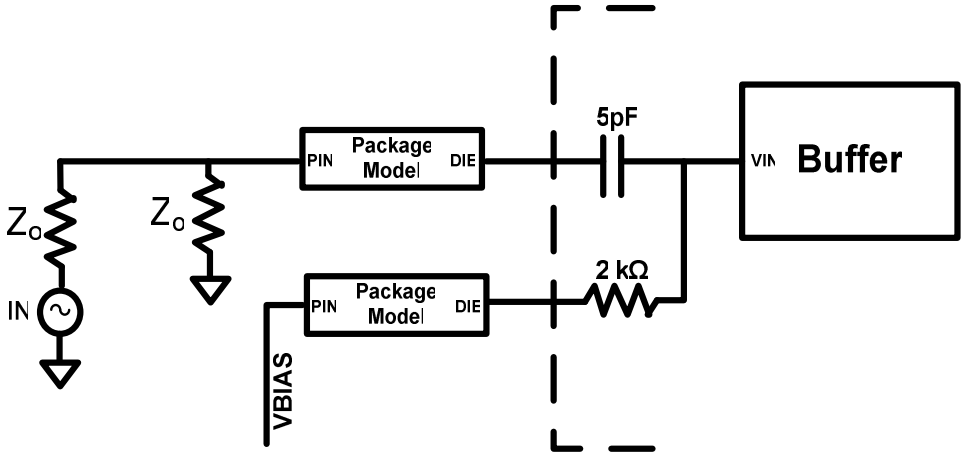


FIG 2.34 INPUT MATCH OF THE STAND-ALONE BUFFER AS DRAWN

3. BUILT-IN-SELF-TEST OF CONTINUOUS TIME FILTER

This section discusses the design of the HF (High Frequency) RMS detector for built-in-test of a 350 MHz boost filter. The bandwidth and boost estimation of the filter using the HF RMS detector has been demonstrated using simulation results. The HF RMS detector along with its DUT has been implemented on TSMC 0.35um technology. The IC is in fabrication.

3.1 DEFINING THE DUT

A pre-designed low power, 350MHz, 24dB boost filter for read-channel applications [1] was used as the DUT. Table 3.1 lists the overall performance summary for the filter.

TABLE 3.1 FILTER–PERFORMANCE SUMMARY

SPECIFICATION	VALUE
Filter Type	5^{th} Order LP Butterworth
Cut-Off Frequency	350MHz
Boost in band	24dB
SINAD	> 36dB
Signal Swing	250mV p-p differential
SNR	40dB
Supply voltage	3V
Current Consumption	13 mA

Figure 3.1 shows the AC response of the low pass filter output depicting the 24 dB boost.

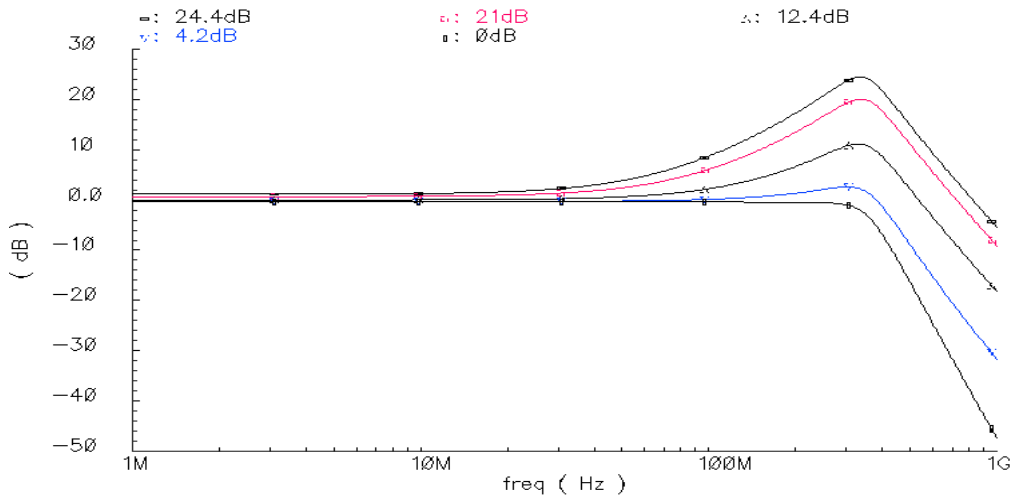


FIG 3.1 LOW PASS FILTER AC RESPONSE SHOWING FILTER BOOST

This high-boost filter forms an ideal DUT for testing the RMS detector because it can showcase the versatility of the RMS detector (called the HF RMS detector henceforth) in being able to detect AC voltages over a wide dynamic range, as well as in being able to measure the bandwidth of the filter in continuous-time.

3.2 SPECIFICATIONS AND DETECTION POINTS FOR THE HF RMS DETECTOR

- The primary functions of the HF RMS detector would be to predict the boost and bandwidth of the filter. Hence the RMS detector should have a linear range greater than 24 dB and a bandwidth exceeding 350 MHz.

- Since the filter is sensitive to parasitic capacitances, the HF RMS detector should have minimum input capacitance.
- The HF RMS detector can also be used to capture Q-errors by connecting it to an intermediate band-pass node, thus obviating the need for dedicated phase detection.
- The various detection points are shown below in figure 3.2.

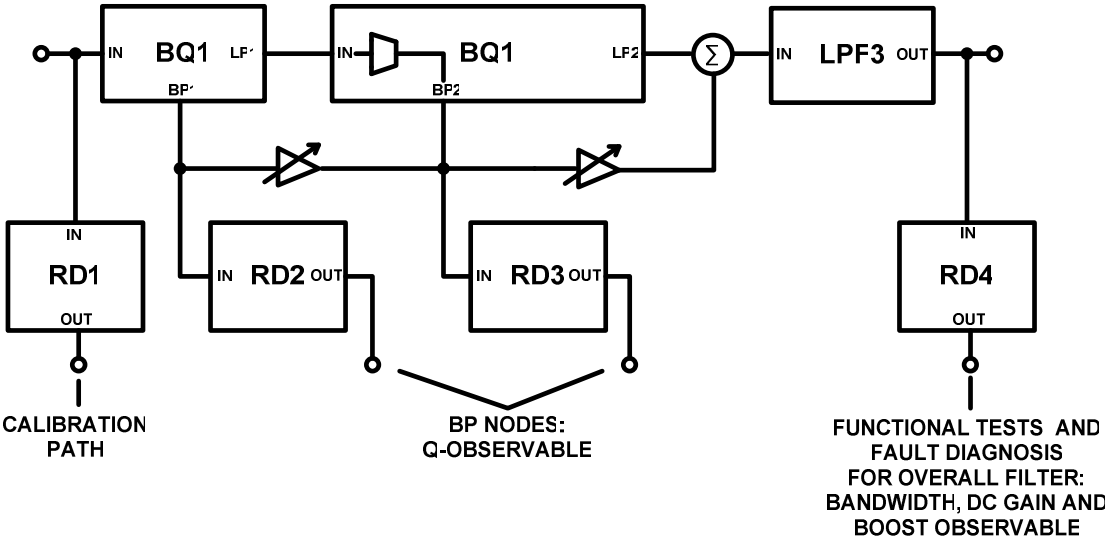


FIG 3.2 DETECTION POINTS–HF RMS DETECTOR

RD in the above figure stands for the HF RMS detector. RD1 is placed at the input of the filter and serves as a reference for all measurements taken with RD2, RD3 and RD4. The filter is comprised of two bi-quads in series with a low pass filter. Bi-quad1 (BQ1) has an available band-pass node. Bi-quad2 (BQ2) has a band-pass node cascaded with a second order low pass node. The Q-errors can be captured at the output

of these band-pass nodes, thus obviating the need for dedicated phase detection as band-pass nodes are more sensitive to Q-errors. RD4 is attached at the output of the filter for estimating its boost, DC gain and bandwidth. Section 3.4 discusses the estimation of all the above parameters using the RMS detectors with post-layout simulation results.

3.3 HF RMS DETECTOR

The following sections discuss the changes that need to be incorporated to the RF RMS detector.

3.3.1 Input Stage

The RF RMS detector was designed for a single ended input. However, the filter has differential input and output. Hence the HF RMS detector needs to have an OTA at its input which can feed the current directly to the rectifier circuit (after current magnification). Figure 3.3 shows the input stage of the HF RMS detector.

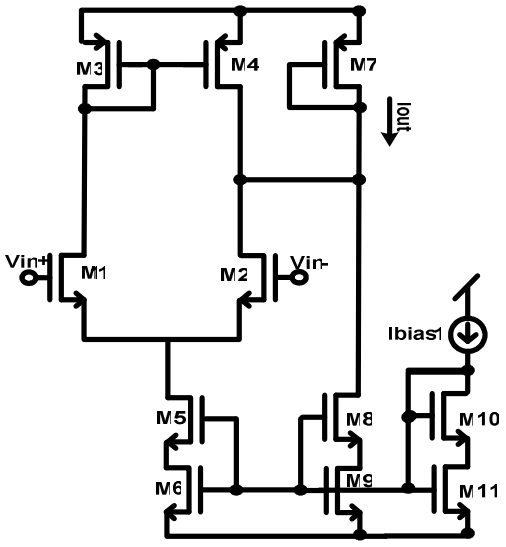


FIG 3.3 HF RMS DETECTOR–INPUT STAGE

The input stage is a differential amplifier with a simple V-I converter implemented with the diode connected transistor M7. M7 is biased with exactly half the current of the differential amplifier with cascode current mirrors for precise current mirroring in order to equalize the DC voltages at the drains of the two input transistors (m1 and M2). This design is suitable for high frequency application because all the nodes in the signal path are low impedance nodes.

Ibias1 should be made large enough to extend the bandwidth to greater than 350 MHz. However, the overdrive of the input transistors should be greater than 350 mV in order to maintain high linearity. Hence, a large Ibias1 will demand large aspect ratios for the input transistors thus increasing the input parasitic capacitance. It must also be remembered that the V-I converter needs to be biased with a DC current which is at least three times the maximum AC current flowing through it so as to prevent any rectification.

3.3.2 Cascode Current Mirrors in the Class AB Rectifier

It has been shown in section 2.3.1 that imperfect current mirroring can cause large DC offsets at the output of the RMS detector. This was also observed during the testing of the RF RMS detector. Hence, cascode current mirrors have been used in the HF RMS detector in order to reduce the DC offset at the output. The additional poles created by the cascode current mirrors can be tolerated since RF frequencies are not being targeted.

Figure 3.4 shows the modified Class AB rectifier with cascode current mirrors for precise current mirroring. The transistor dimensions are shown in table 3.2.

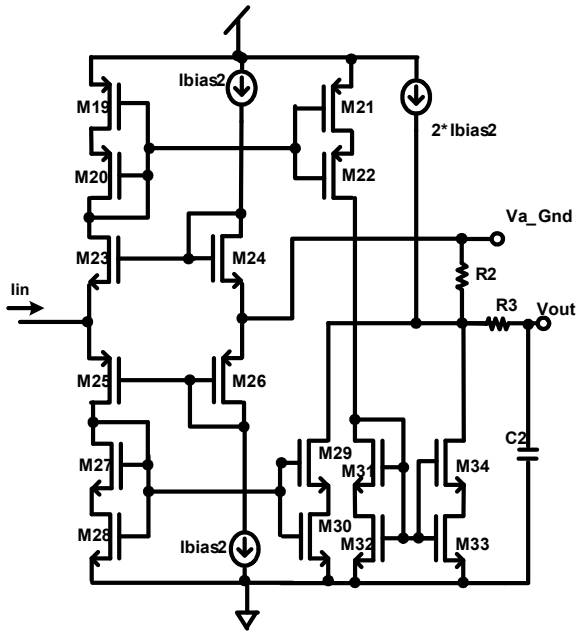


FIG 3.4 CLASS AB RECTIFIER WITH CASCODE CURRENT MIRRORS

All the design considerations observed in the design of the Class AB rectifier for the RF RMS detector apply to this design also (sections 2.3.1 and 2.3.2). The maximum signal level at the output of the filter is 250 mV_{PP} differential input AC signal (which corresponds to approximately -14 dBm of single ended RMS AC signal). In order to achieve a boost of 24 dB at the output of the filter, the input signal needs to be as low as -38 dBm of input single ended RMS AC signal (i.e. approximately 4mV peak single ended AC signal). Hence the RMS detector has to be sensitive to $14mV_{PP}$ differential input signal. Hence, the DC current in the rectifier has to be reduced to as minimum as possible while still maintaining sufficient bandwidth in the cascode current mirrors (2uA has been used for this design). Figure 3.5 shows the total rectified current through R2

and its averaged value for small signal amplitudes at the input. The increase in the linearity can be compared with that of figure 2.10 for the RF RMS detector.

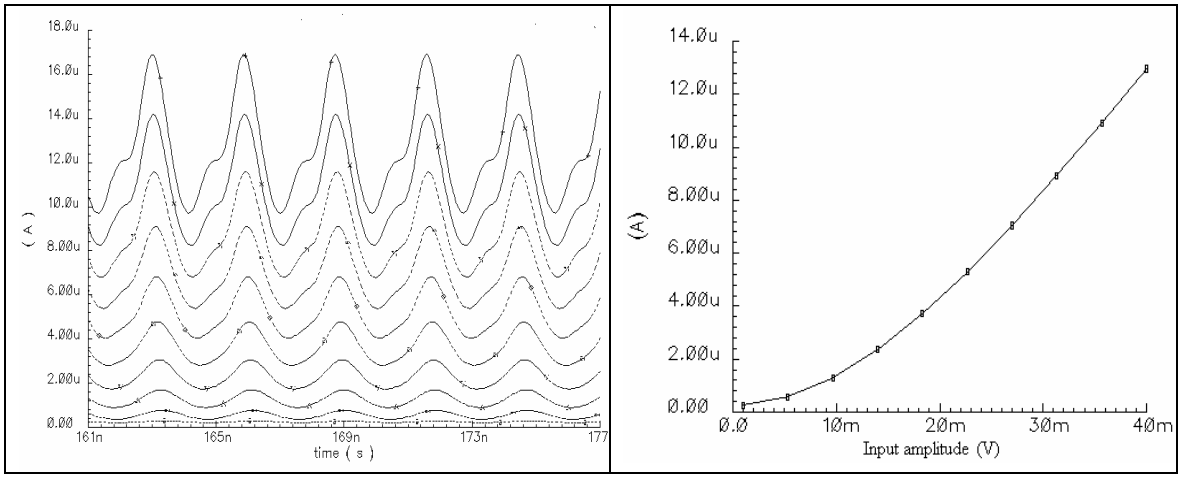


FIG 3.5 RECTIFIED COMPONENTS ADDED TOGETHER

Figure 3.6 shows the transient currents at the drain of M29 and M34 by varying the amplitude of the input Ac signal. It can be seen that the DC offset current is less than 1 uA.

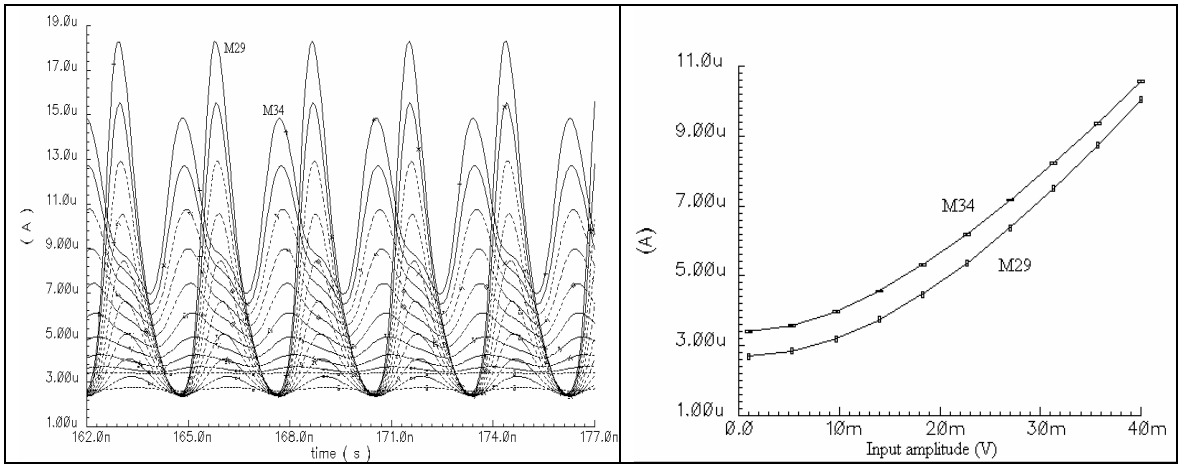


FIG 3.6 POSITIVE AND NEGATIVE COMPONENTS OF THE RECTIFIED CURRENT

As explained in section 2.3.1, the current at the drain of M34 (Figure 3.4) shows rectification due to the additional level of mirroring which causes bandwidth limitation. The additional phase shift at the drain of M34 can also be attributed to the additional level of current mirroring for the negative component of the current.

3.3.3 Complete Schematic of HF RMS Detector

The complete schematic of the HF RMS detector is shown below in figure 3.7.

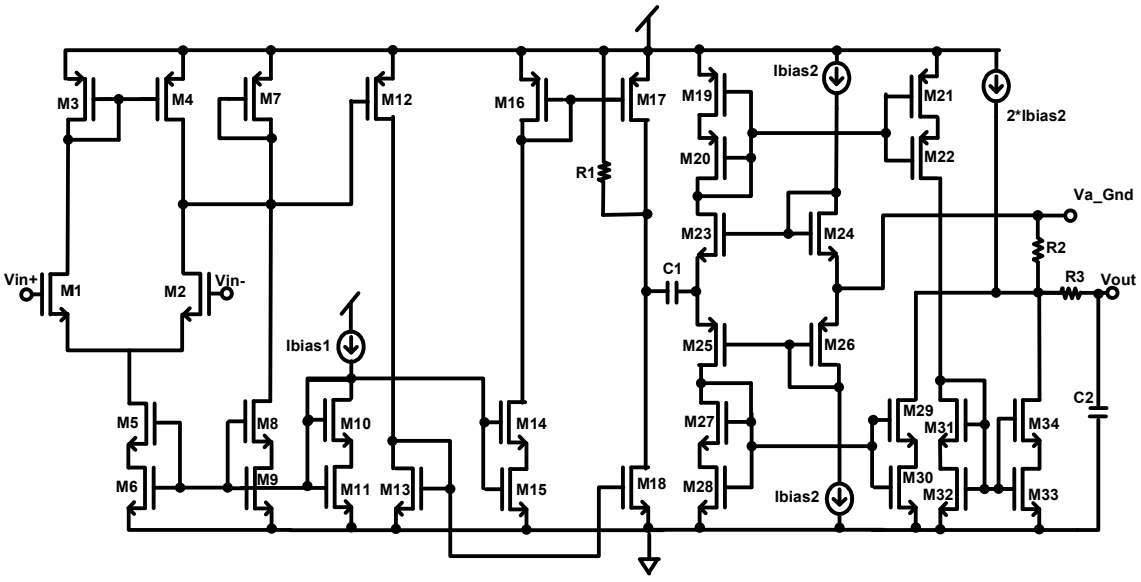


FIG 3.7 HF RMS DETECTOR–COMPLETE SCHEMATIC

TABLE 3.2 COMPONENT VALUES–HF RMS DETECTOR

M1,M2	4 µm/0.4 µm, m=2	R1	50 KΩ	M18	6 µm/0.4 µm, m=4
M3,M4	6 µm/0.4 µm, m=2	R2	10 KΩ	M23,M24	6 µm/0.4 µm, m=1
M5,M6	3 µm/0.4 µm, m=4	R3	10 KΩ	M25,M26	6 µm/0.4 µm, m=2
M7,M12	6 µm/0.4 µm, m=2	Ibias2	2 µA	Ibias1	1.3 mA

TABLE 3.2 (CONT.)

M8,M9	3 μm/0.4 μm, m=2	C2	1 pF	C1	5 pF
M10,M11	3 μm/0.4 μm, m=8	M19, M20, M21, M22			6 μm/0.4 μm, m=2
M14,M15	3 μm/0.4 μm, m=8	M27, M28, M29, M30			6 μm/0.4 μm, m=2
M16	6 μm/0.4 μm, m=4	M31, M32, M33, M34			6 μm/0.4 μm, m=1
M17	6 μm/0.4 μm, m=2				

For this application, there is no need for bandwidth enhancement in the current mirrors as the target frequency of operation is around 350 MHz. The current mirror M13-M18 is used to provide current magnification in order to increase the current efficiency (defined as the ratio of the current going in to the rectifier stage to the current generated in the input stage). R1 is used to bias the high impedance node at the drain of M18. R1 has been connected from Vdd to the drain of M18. The value of R1 is determined by the desired voltage at the drain of M18 and the maximum tolerable current through it. A small value of R1 will cause a large current to flow through it thus pushing M18 into the linear region. A large value of R1 is also detrimental as even a small current through it can cause a large voltage drop across it. Hence, R1 should be chosen after simulating for process variations as large as 60%. The layout of the HF RMS detector is shown below in figure 3.8

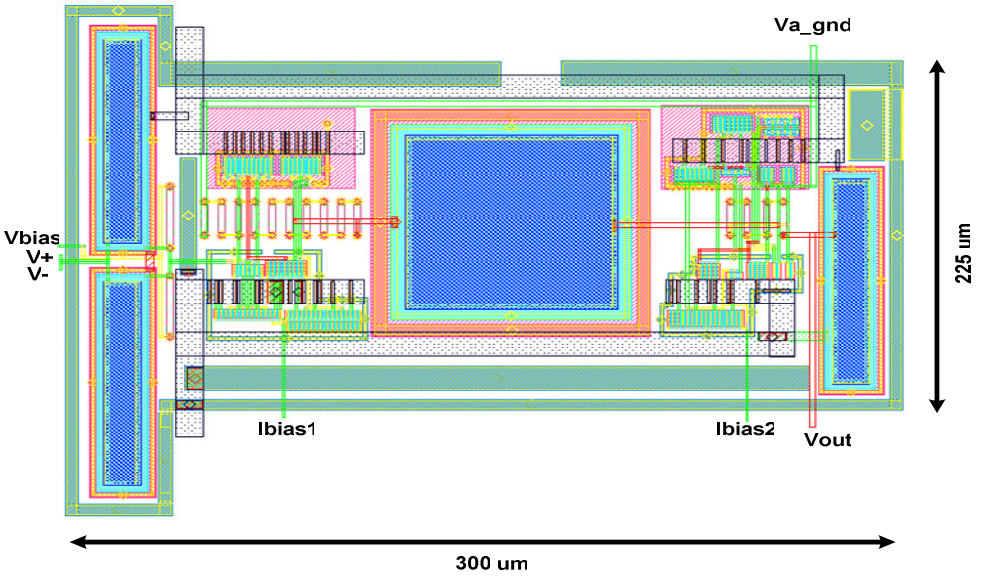


FIG 3.8 HF RMS DETECTOR–LAYOUT

3.3.4 Simulation Results

Figure 3.9 shows the input capacitance of the HF RMS detector over the frequency range of interest. It can be seen that the input capacitance is always lesser than 7 fF.

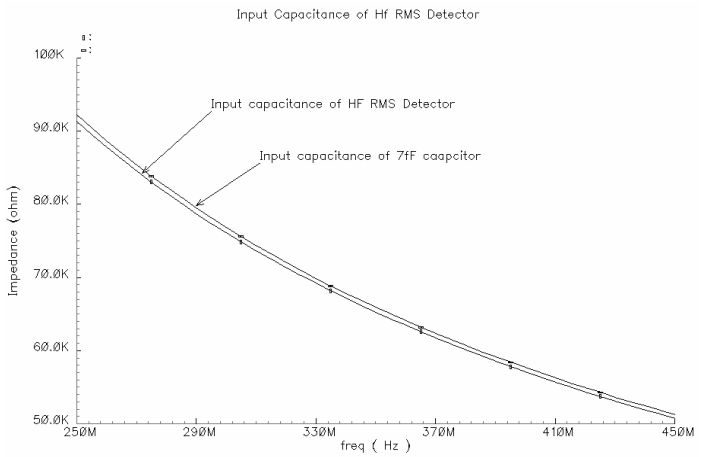


FIG 3.9 INPUT IMPEDANCE OF HF RMS DETECTOR

Figure 3.10 shows the post-layout transient response of the HF RMS detector for different values of the input signal level at 350 MHz. The peak amplitude of the input signal was varied in steps of 10mV starting from 4mV and the output DC voltage of the HF RMS detector has been plotted with respect to time. It can be seen that the settling time is less than 100ns and the output DC voltage changes in equal increments depicting linear transfer characteristic (Figure 3.11)

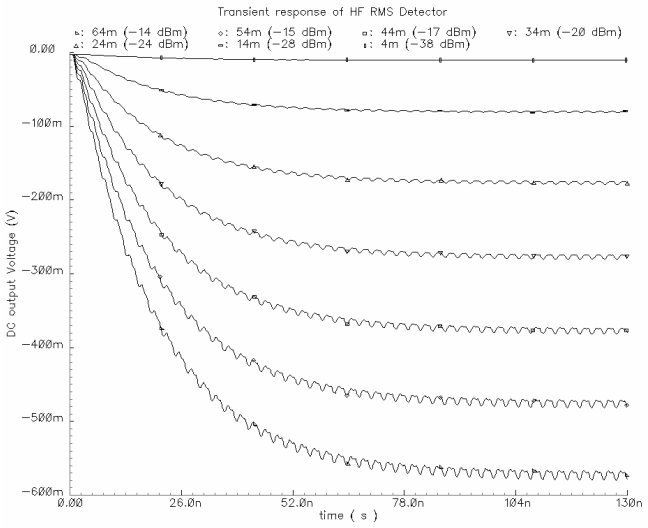


FIG 3.10 TRANSIENT OUTPUT OF THE HF RMS DETECTOR FOR VARYING INPUT VOLTAGES

Figure 3.11 shows the transfer characteristic of the HF RMS detector in (V/V). It can be seen from the transfer characteristic that the HF RMS detector is linear from around $4mV_P$ (-38 dBm RMS) to $62.5mV_P$ (-14 dBm RMS) of single ended input which satisfies the requirements for boost verification of the filter.

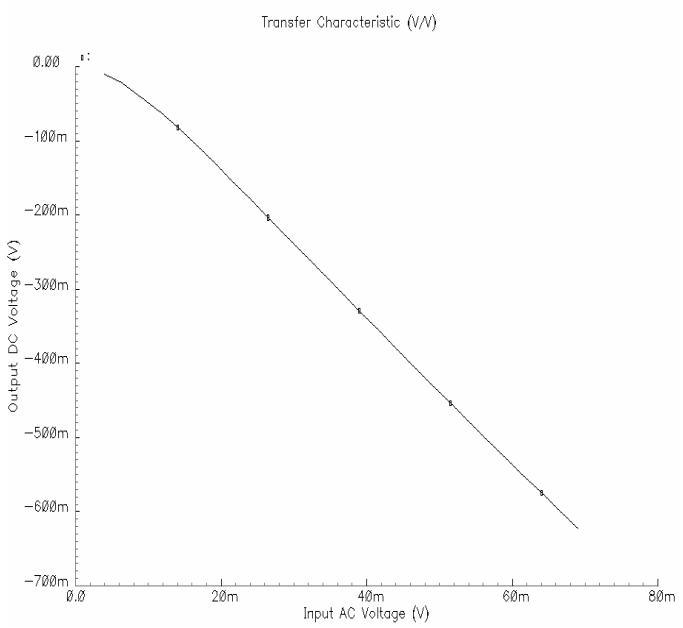


FIG 3.11 TRANSFER CHARACTERISTIC OF THE HF RMS DETECTOR AT 350 MHZ (V/V)

3.4 TEST STRATEGY FOR FILTER WITH HF RMS DETECTORS

The following sub-sections illustrate the post-layout estimation of the bandwidth, and boost at the output of the filter and sensitivity to Q-errors at an intermediate band-pass node.

3.4.1 Predicting the Bandwidth

The input frequency is swept from 300 MHz to 400 MHz and the response of the two RMS detectors connected at the input and output of the filter are recorded. The output RMS detector's response is a combination of its frequency response (which can be normalized against the input RMS detector's frequency response) and the gain response of the filter. Hence, the exact frequency at which the filter's gain drops by 3 dB can be estimated by mapping the DC voltages from the two RMS detectors to the

transfer characteristic of a stand-alone HF RMS detector (V/dBm). This is illustrated in the simulation result shown below in figure 3.12.

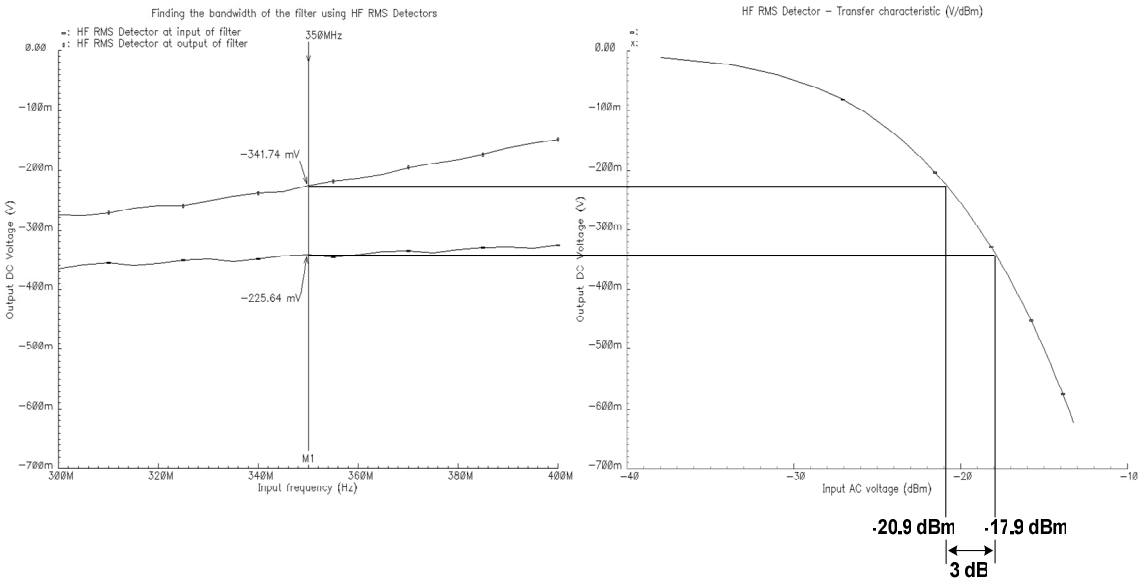


FIG 3.12 ESTIMATING THE FILTER'S BANDWIDTH USING THE HF RMS DETECTOR

3.4.2 Estimating the Filter's Boost

Figure 3.13 illustrates the boost estimated using the HF RMS detectors when the filter has been designed to give its maximum boost (24 dB at 366 MHz from the post-layout simulation results). The transient outputs of the HF RMS detectors at the input and output of the filter are recorded and compared against the transfer characteristic of the HF RMS detector (V/dBm) to find the filter's boost.

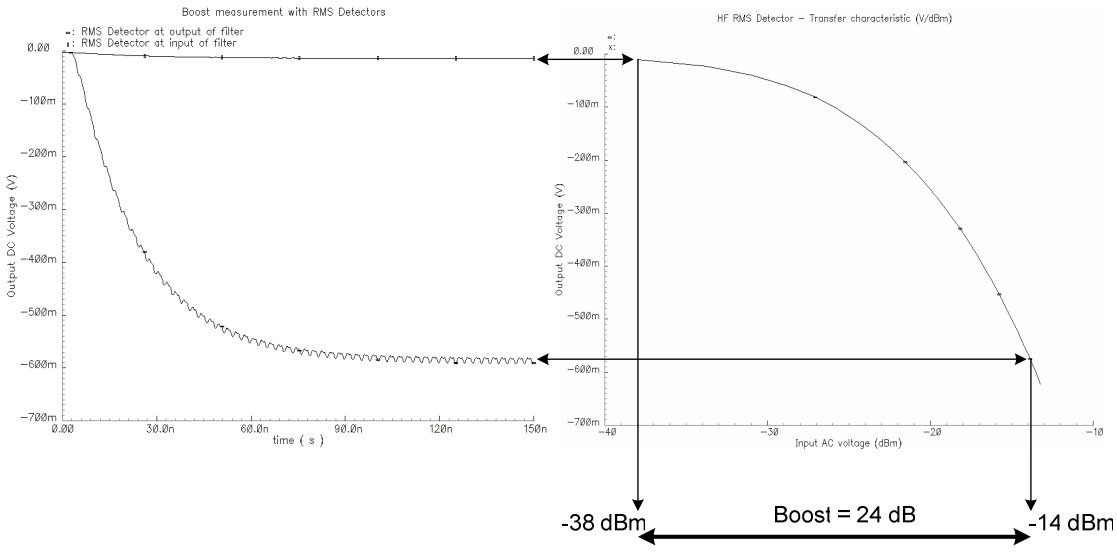


FIG 3.13 ESTIMATING THE BOOST OF THE FILTER USING THE HF RMS DETECTORS

3.4.3 Estimating the Sensitivity to Q Errors

Figure 3.14 depicts the frequency response of the filter at an intermediate band-pass node.

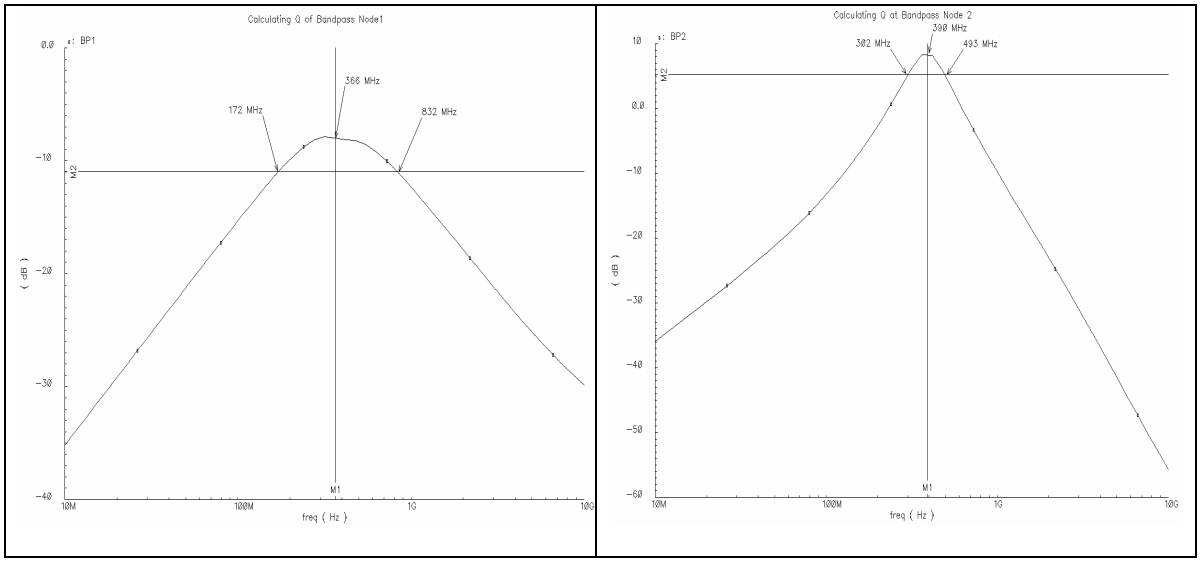


FIG 3.14 INTERMEDIATE BAND-PASS NODE RESPONSE OF THE FILTER

For estimating any Q-errors in the filter's response, the frequency of the input signal can be varied and the response of the output RMS detector can be recorded (of course, after normalizing against the input RMS detector's frequency response). Then, the Q of the intermediate node can be estimated from the formula $Q = \frac{\text{center frequency}}{f_2 - f_1}$ where f_1 and f_2 are as indicated in figure 3.14. The Q of the intermediate band pass nodes were estimated with less than 10% error using the RMS detectors.

4. SINGLE-ENDED TO DIFFERENTIAL CONVERTER

4.1 DIFFERENTIAL OUTPUT PHASE ERROR FOR A SINGLE-ENDED INPUT

In a broadband receiver (figure 4.1) operating in the range of 50-850 MHz, the complex filter takes in differential input signals. This entails a single-ended to differential signal conversion after the low-noise amplifier.

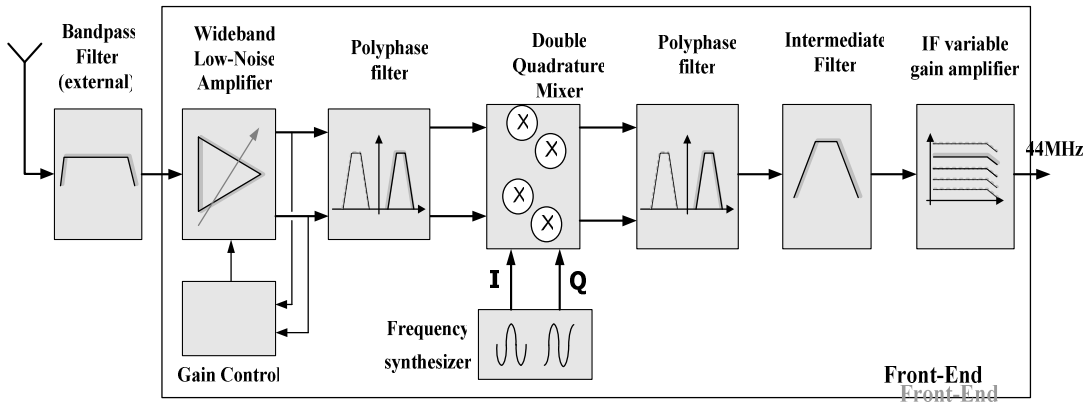


FIG 4.1 BROADBAND RECEIVER BLOCK DIAGRAM
(PICTURE COURTESY: JIANHONG XIAO, SYSTEM LEVEL DESIGNER FOR BROADBAND TV TUNER, ANALOG AND MIXED SIGNAL CENTER, TAMU)

Three simple ways of phase-splitting are to use a single transistor and tap its drain and source terminals, CG-CS configuration or use a simple differential pair. The first two methods have been explained in section 1 with the aid of suitable examples form literature. A single differential pair which is given a single ended input will not produce outputs which are exactly fully differential. This is because of the extra pole

created in one of the paths due to the parasitic capacitance of the current source (as seen in figure 1.2).

It can be shown that this phase error due to the parasitic pole of the current mirror mainly occurs as a common mode mismatch in the output signals of the differential pair. Hence, by using cascaded differential amplifiers this common-mode error can be reduced. However, using cascaded differential pairs can be very costly in terms of area and power. To satisfy the specifications of less than 1 dB ripple in the gain over the entire band of interest (50 MHz – 850 MHz), each differential pair consumes at least 5mA of current. Each stage also introduces noise, and adds a substantial amount of area. Hence, the need arises to convert the single-ended signal to differential signals within a single stage using as minimum power as possible.

4.2 PROPOSED SOLUTION

4.2.1 Specifications

The specifications for the converter are shown below in table 4.1.

TABLE 4.1 SPECIFICATIONS–SINGLE ENDED TO DIFFERENTIAL CONVERTER

Frequency band of interest	50 – 850 MHz
Phase Difference between the two outputs	180 degrees
Power Consumption	< 5mA
Noise Figure	< 8 dB (This being the second stage after the LNA)
Gain ripple over entire band	< 1dB
Gain difference over entire band	< 1dB
Load capacitor at each output	500 fF

Among all these constraints, the power consumption is the toughest one. Hence the need is to minimize the number of stages and try to perform the single ended to differential conversion with as minimum power consumption as possible. The idea is described in detail below.

4.2.2 Basic Idea

The circuit shown below in figure 4.2 forms the basis of the proposed solution.

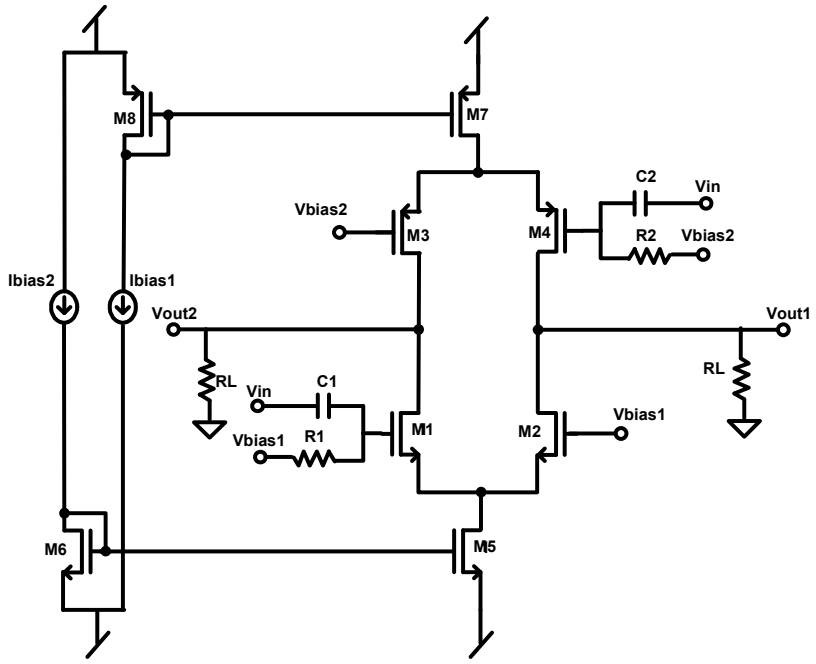


FIG 4.2 CORE IDEA–SINGLE ENDED TO DIFFERENTIAL CONVERTER

Table 4.2 lists the component values and the DC bias currents for the above circuit.

TABLE 4.2 COMPONENT VALUES–SINGLE ENDED TO DIFFERENTIAL CONVERTER

NMOS input	10u/0.4u (m=4)	PMOS input	6u/1u (m=4)
NMOS current mirror	2u/0.4u (m=4)	PMOS current mirror	8u/0.4u (m=4)
Vdd	1.5 V	Vss	-1.5 V
I_{DC}-NMOS	400 uA	I_{DC}-PMOS	15 uA

The basic idea is that, if by careful design, the pole at the NMOS and the PMOS current-source is cancelled properly by introducing the same amount of phase shift in both the output currents, then perfect differential outputs can be produced. If g_{mn} is the trans-conductance of the NMOS transistors and g_{mp} is the trans-conductance of the PMOS transistors, then the small signal flowing out of Vout1 is $(g_{mn}-g_{mp})$*Vin and the current flowing out of Vout2 is $(g_{mp}-g_{mn})$*Vin.

4.2.3 Strengths and Weaknesses for the Stand-Alone Core

For the above mentioned core idea to function properly, the trans-conductance of the NMOS and the PMOS have to be as widely different as possible. There are two ways of varying the trans-conductance, the first being to vary the current and the second being to vary the aspect ratio. But for purposes of maintaining broadband operation, increasing the aspect ratio too much will prevent us from satisfying the bandwidth specifications within the constraint on power consumption. Hence, the former method was adopted.

The main disadvantage of this circuit is that the effective trans-conductance is reduced (difference in the trans-conductance of the NMSO and the PMOS) thus reducing the Signal to Noise Ratio (SNR). By adopting the strategy of using widely different DC

bias currents in the NMOS and the PMOS sections, there is a certain amount of DC current that now flows into the output along with the AC current. Hence, it was found necessary to use a very small resistor at the outputs connected to ground (to maintain the dc operating point) that sinks in the difference in the DC current. However, the DC gain is reduced drastically by using small resistor values; thus reducing the SNR further.

Although the circuit is not capable of producing voltage outputs, its current outputs satisfy the specification on output phase error with very low power consumption. The very low power consumption is expected because the differential output current and is based on basically the difference in the trans-conductance of the NMOS and the PMOS transistors. It was found that the total power consumption was less than 1.5 mA. Hence, the next task would be to convert the current outputs to voltage outputs without compromising the results obtained on the output phase error and the power consumption. The following figures summarize the results obtained from the current outputs.

Figure 4.3 shows the variation of the differential output phase error in the currents over frequency. The error is less than 1.6 degrees from 50 - 850 MHz.

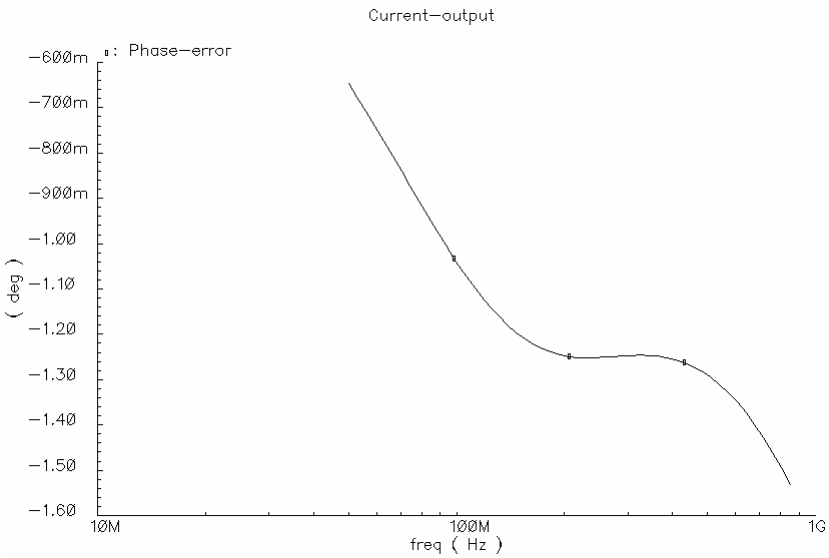


FIG 4.3 DIFFERENTIAL OUTPUT CURRENTS–PHASE ERROR

The total trans-conductance at the output is shown below in figure 4.4. There is an error of about 10% in the two outputs:

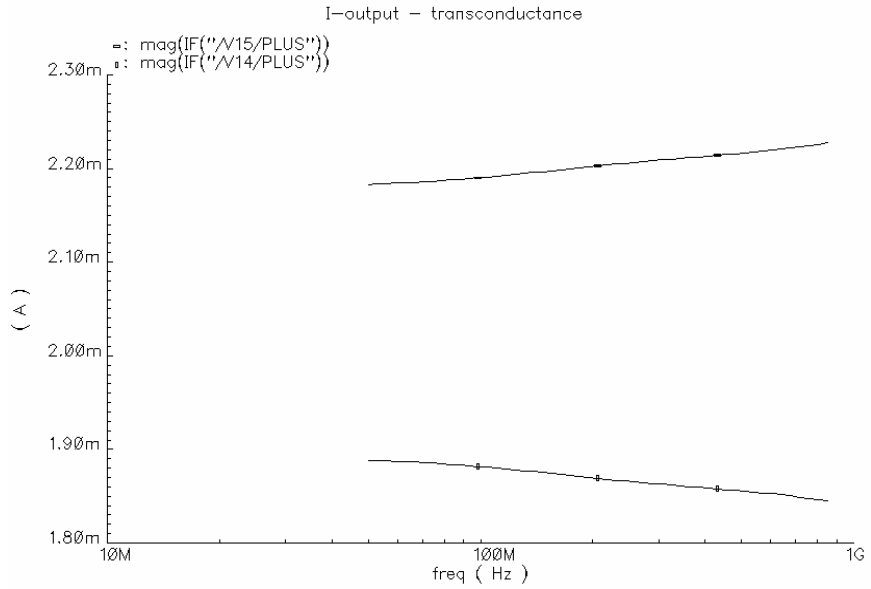


FIG 4.4 DIFFERENTIAL OUTPUT CURRENTS–TRANS-CONDUCTANCE

4.2.4 Current to Voltage Conversion

The easiest current to voltage converter is a resistor but a very large resistor cannot be tolerated at the output because a large resistor will not sink in the difference in the two DC currents. On the other hand, it will try to equalize the DC currents in the NMOS and the PMOS transistors, thus destroying the whole core idea. Hence, there is a need for a trans-impedance amplifier that can convert the AC output current into voltage with very low input impedance while still satisfying the requirements of less than two degrees of phase error and less than 1 dB gain ripple at its output. It needs to have very low power consumption; otherwise the advantage gained in the core would be squandered. It should be capable of driving the 500 fF input capacitance of the complex filter at each of its outputs (which would mean that it should also have low output impedance) and be robust to process variations.

4.2.5 Final Design

The answer to all the above mentioned constraints is the Cherry Hooper amplifier, which can convert current input to voltage output with low input and output impedances (1/gm).

The final structure incorporating a differential Cherry-Hooper amplifier is shown below in figure 4.5.

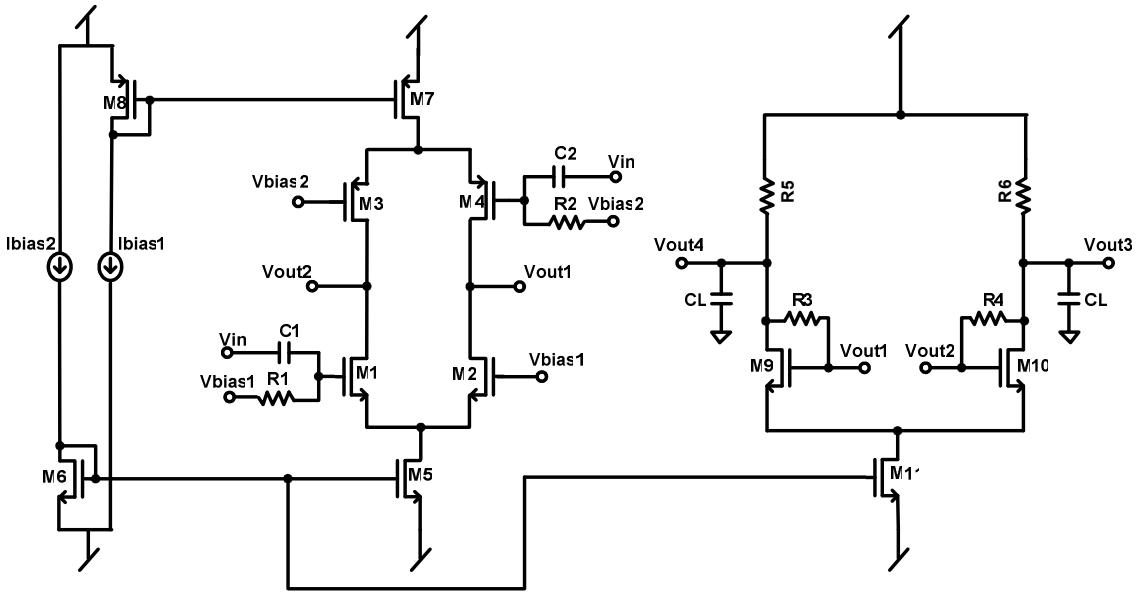


FIG 4.5 FINAL DESIGN

The final aspect ratios of all the transistors and the resistor values are listed below in table 4.3.

TABLE 4.3 COMPONENT VALUES–FINAL DESIGN

Stage -1 – Core – Single Ended to Differential Converter			
NMOS input	10u/0.4u (m=10)	PMOS input	6u/1u (m=4)
NMOS current mirror	2u/0.4u (m=1,4)	PMOS current mirror	7u/0.4u (m=4)
Vdd	1.5 V	Vss	-1.5 V
I-NMOS	400 uA	I-PMOS	10 uA
Cbias	10 uF	Rbias	1 M ohm
Vbias – NMOS	300 mV	Vbias – PMOS	400 mV
Stage -2 – Cherry Hooper differential trans-conductor			
NMOS input	20u/0.4u (m=10)	NMOS current source	2u/0.4u (m=8)
Load resistor	300 ohm	Feedback Resistor	1 K ohm

Figure 4.6 shows the output characterization plots. It can be seen that all the specifications have been met.

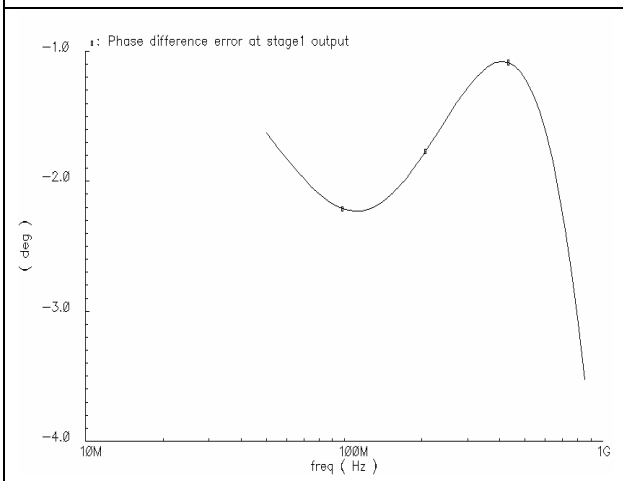
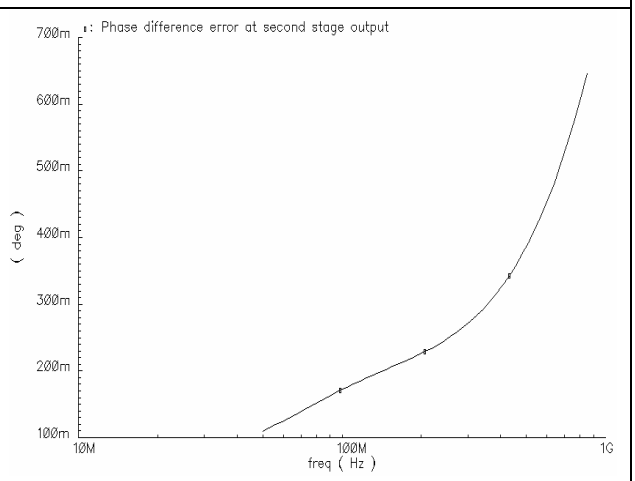
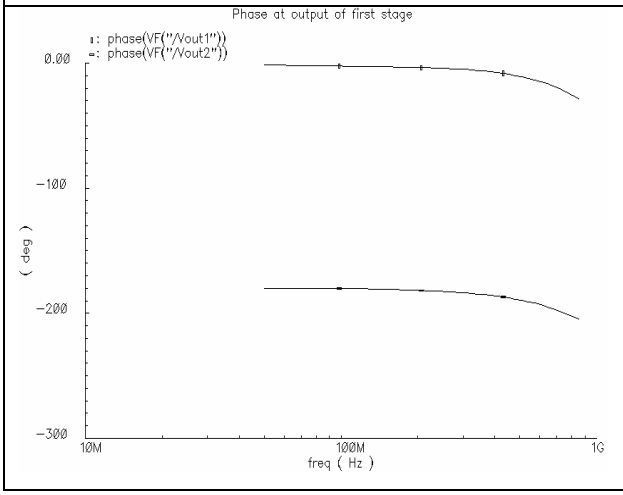
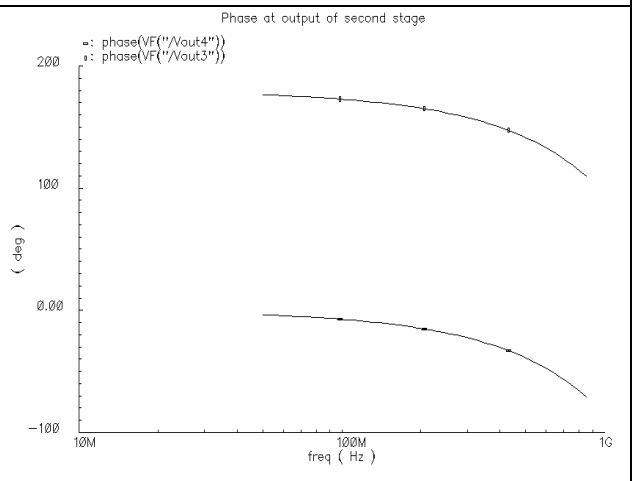
Phase error at the output of the first stage	Phase error at the output of the second stage
	
Phase response at the output of first stage	**Phase response at the output of second stage**
	

FIG 4.6 SIMULATION RESULTS–FINAL DESIGN

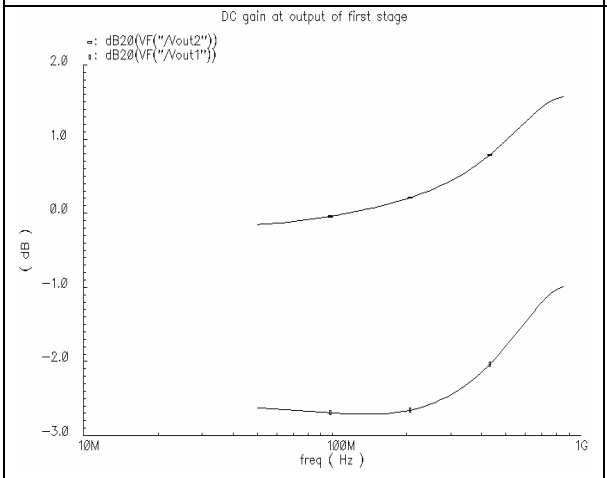
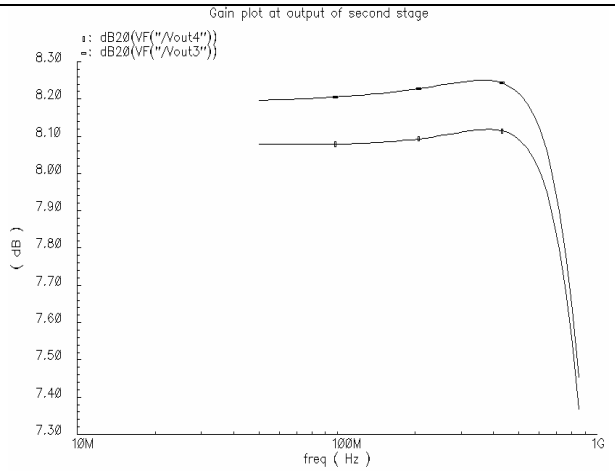
Gain response at the output of the first stage	Gain response at the output of the second stage
	
First stage current consumption = 1.5 mA	Second stage current consumption = 3mA

FIG 4.6 (CONT.)

It can be seen that, the addition of the Cherry-Hooper amplifier degrades the phase error at the first stage output. But due to its high gain, it improves the phase error at the final output. Actually, the phase error at the first stage output was sacrificed a little to obtain high gain in the second stage and lesser overall Noise Figure.

The trans-impedance amplifier consumes almost twice as much power as the first stage (3mA, in comparison to the first stage's 1.5mA), but the total power consumption is still within the specification limits.

The total variation in the gain over the entire band of interest is less than 1 dB and the total difference in the gain between the two outputs is also less than 1 dB.

The total noise figure from the outputs of the second stage to the input of the first stage was found to be less than 8 dB as shown in figure 4.7 on the next page.

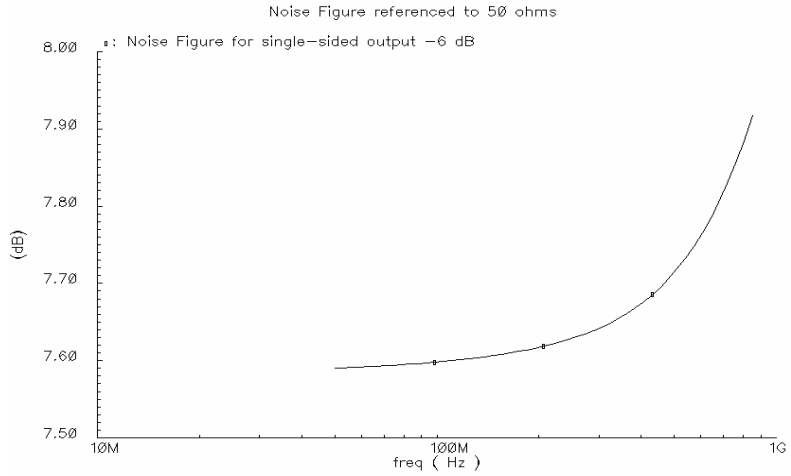


FIG 4.7 NOISE FIGURE–FINAL DESIGN

4.3 ROBUSTNESS ANALYSIS, ADVANTAGES AND DISADVANTAGES

4.3.1 Robustness Analysis

A number of parametric simulations were done to evaluate the effect of process and temperature variations on the phase error and noise figure (figure 4.8).

Effect on Phase Error at the final output	Effect on Total Noise Figure
W/L of the NMOS transistor - Stage1	

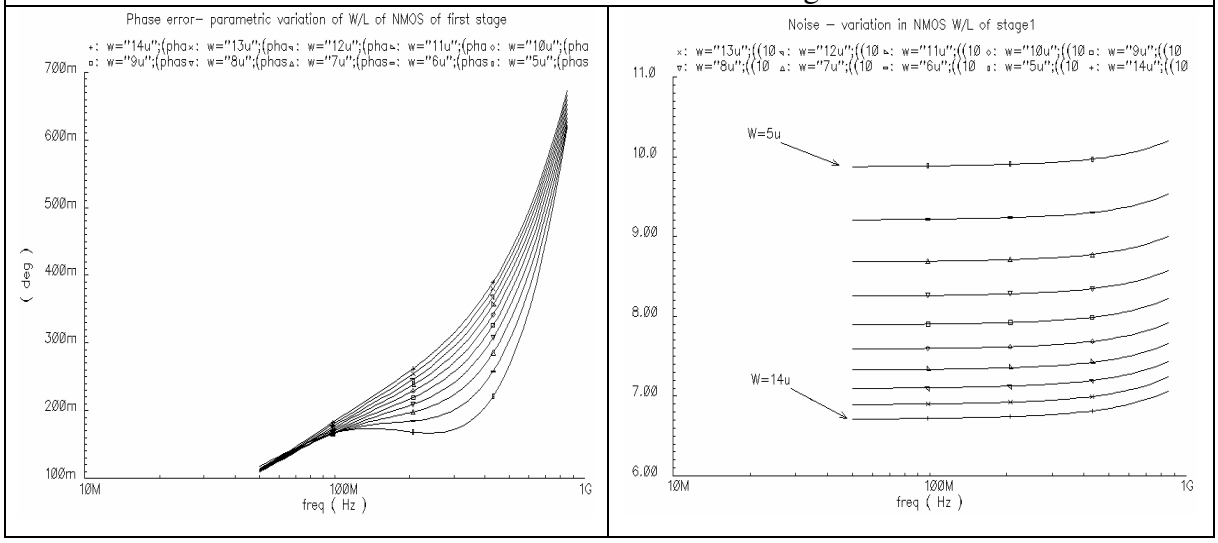
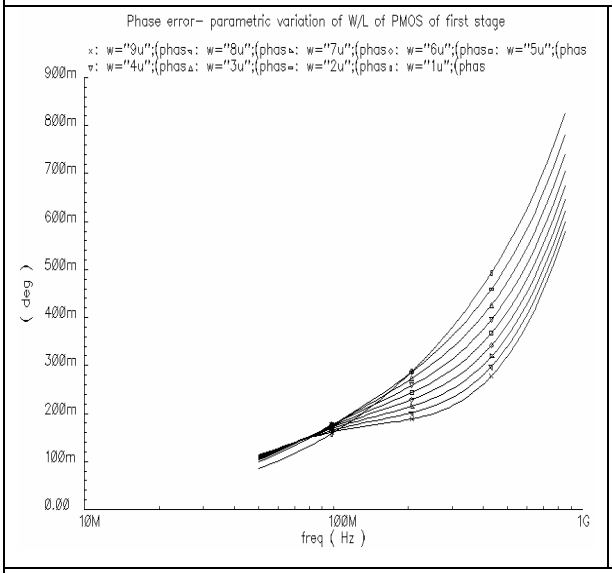
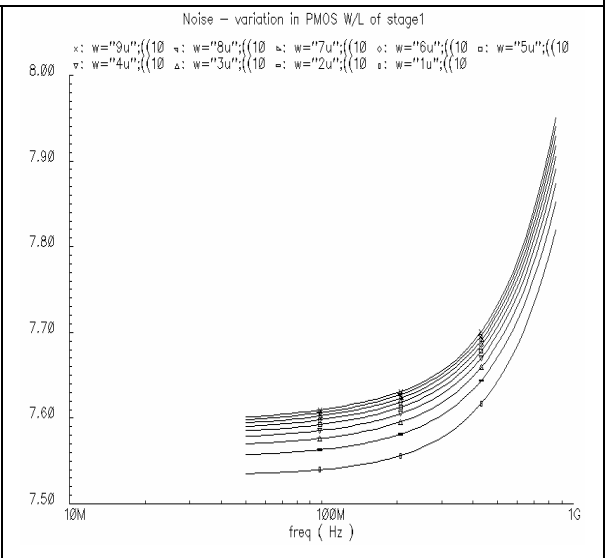


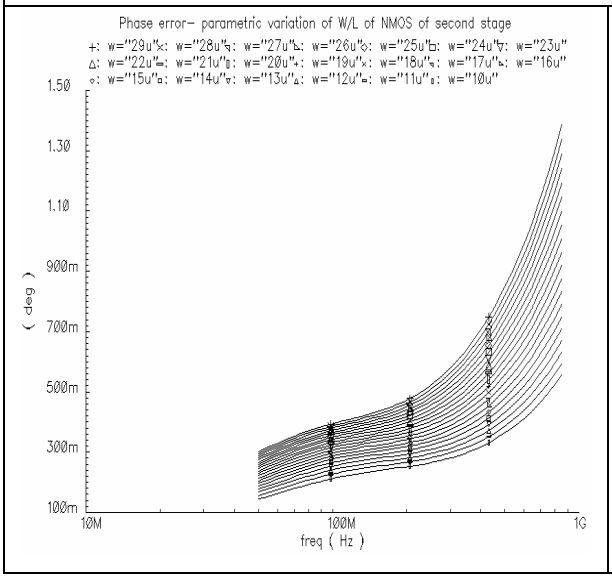
FIG 4.8 ROBUSTNESS ANALYSIS–FINAL DESIGN

W/L of the PMOS transistor – stage1





W/L of the NMOS transistor – stage2



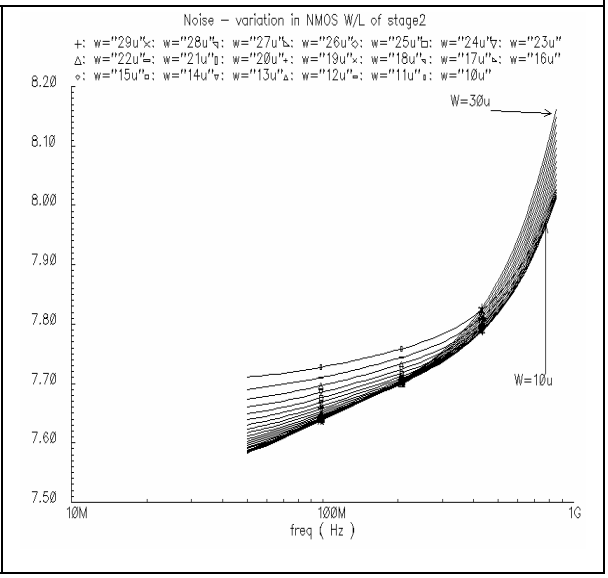


FIG 4.8 (CONT.)

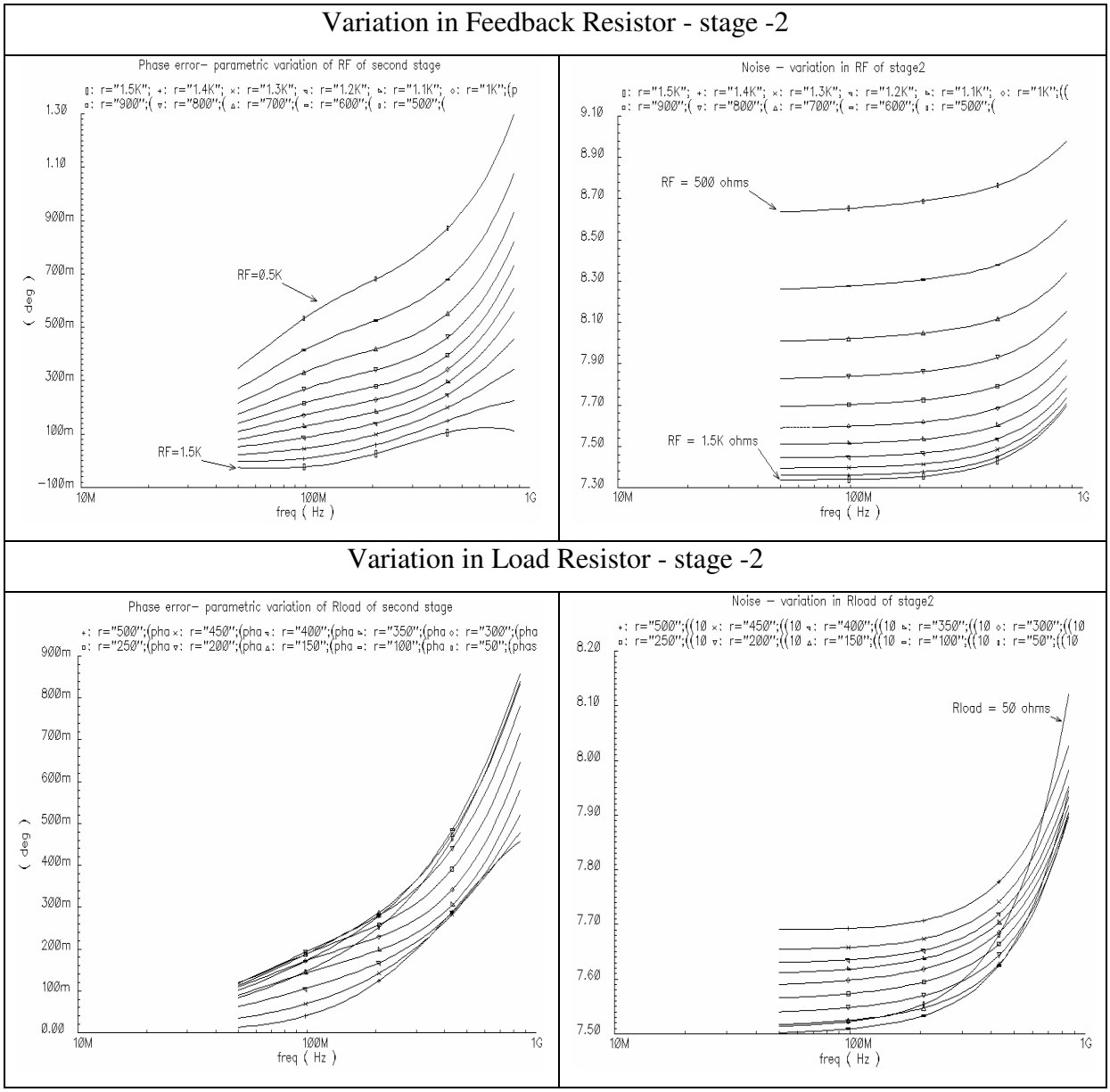

Variation in Feedback Resistor - stage -2
Phase error– parametric variation of RF of second stage
RF=0.5K
RF=1.5K
(deg)
freq (Hz)
Noise – variation in RF of stage2
RF = 500 ohms
RF = 1.5K ohms
freq (Hz)
Variation in Load Resistor - stage -2
Phase error– parametric variation of Rload of second stage
(deg)
freq (Hz)
Noise – variation in Rload of stage2
Rload = 50 ohms
freq (Hz)

FIG 4.8 (CONT.)

The analysis of the various results obtained above, are as follows:

- It can be seen that the noise figure increases drastically for decrease in the aspect ratio of the NMOS input transistors of the first stage. This makes sense because the NMOS transistors carry much larger current than the PMOS transistors and hence their drain noise is the most important one. Correspondingly, the aspect ratio of the NMOS transistors in the second stage can also affect the noise figure, but the effect of this aspect ratio is much more muted in comparison to the previous one. The PMOS aspect ratio in contrast has no effect on the NF because it carries very little current (less than 5 uA) and its only effect can be the gate-induced noise which can increase the total noise figure by less than 0.1 dB.
- A decrease in the feedback resistor to 500 ohm from the nominal value of 1K ohm can cause the noise figure to exceed the specification by 0.2 dB. This is also very intuitive because its noise directly appears at the input of the second stage and gets *magnified* by the first stage because the first stage has attenuation. But, this effect cannot be very corrosive as can be seen from the graphs.
- The load resistor shows lesser effect on the noise figure than the feedback resistor because its noise is first divided by the large gain of the second stage before it appears at the input. This is clearly reflected in the graphs.
- The phase error always remains within the specification whatever the variation; this is a very good indication of the robustness of the design.

Using various parametric analyses, the robustness of the circuit was demonstrated and it was found that the only weak point is the variation in the noise

figure because of the NMOS input transistors in the first stage. Otherwise the circuit is very robust.

4.3.2 Advantages of Proposed Solution

- The design uses a novel current-mode single-ended to differential conversion which reduces the power consumption drastically because it is only based on the difference in trans-conductance between the NMOS and the PMOS transistors and has been seen to easily achieve broad-band operation within 1.5 mA of current consumption.
- This method does not depend on any external passive components (which can have 30 % variation with process) to cancel the extra pole due to the current-source transistor. It has been shown that with variation in various circuit parameters, the circuit still satisfies all conditions and is very robust.
- This circuit is fully differential and any process variation in one current mirror can also be expected to affect the other (though may not be to the same degree) and hence the phase error variation with process can be expected to be small.
- The Cherry Hooper amplifier's low input and output impedances have been well exploited to provide the necessary phase error and broadband operation at its output.

4.3.3 Disadvantages of Proposed Solution

- The first stage has attenuation because its output is current and hence the NMOS input transistors of the first stage contribute the most to the noise figure as they also carry much more current than the PMOS transistors.
- The advantage of very low power consumption in the first stage is lost in the Cherry-Hooper amplifier (although the total power consumption still meets the

specification), which consumes almost twice the current. This stage needs to be re-designed and optimized for lower power-consumption.

- The circuit's overall noise figure is sensitive to the aspect ratio of the input NMOS transistor in the first stage. This needs to be handled. Trying to increase the voltage gain of the first stage by sacrificing more phase error can probably rectify the problem because, the Cherry-Hooper amplifier maintains a very low phase error at its output.

4.4 FUTURE WORK

The future work in terms of improving the circuit design has already been populated upon in the previous section. Once the design is finalized, the circuit needs to be implemented on silicon and tested.

5. CONCLUSIONS

A compact (< 0.031 mm2) RF RMS detector with negligible input capacitance (<13 fF) and greater than 25 dB dynamic range has been designed for RF BIST. It has been implemented in TSMC 0.35 um technology along with an RF DUT–CMOS cascode LNA for gain and linearity estimation. Experimental results have been compared with the simulation results. Bandwidth limitation problem was encountered during testing due to unexpected increase in the value of the N-well resistors.

The RF RMS detector has been extended for the BIST of a 350 MHz, 24 dB boost filter. The HF RMS detector occupies 0.07 mm^2, with input capacitance of 7 fF and sufficient dynamic range to estimate the boost of the filter. Simulation results have been demonstrated for bandwidth and boost estimation using the RMS detectors.

A simple and robust single-ended to differential converter has been designed and simulated for 50-850 MHz broadband TV tuner application. The design has been simulated on a 0.35 um CMOS process and has a power consumption of 13.5 mW and less than 8 dB of noise figure over the entire band. It is capable of driving a 500fF load with less than 1dB of gain ripple and 0.7 degrees of phase error over the entire band.

REFERENCES

[1] M. Gambhir, D. Vijay, J. Silva-Martinez and E. Sanchez-Sinencio, "A 43 mW, 330 MHz, 24 dB Programmable Boost Filter for Read Channel Applications", submitted to *IEEE Journal of Solid-State Circuits*, 2006.

[2] A. Valdes-Garcia, R. Venkatasubramanian, R. Srinivasan, J. Silva-Martinez and E. Sanchez-Sinencio, "A CMOS RF RMS Detector for Built-in Testing of Wireless Receivers", in *Proc. 23rd IEEE VLSI Test Symposium*, Palm Springs, CA, May 2005, pp. 249-254.

[3] E. Tiiliharju and K.A.I. Halonen, "An Active Differential Broad-Band Phase Splitter for Quadrature Modulator Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no 2, pp. 679-686, Feb 2005.

[4] M.S. Heutmaker and D.K. Le, "An Architecture for Self-Test of a Wireless Communication System Using Sampled IQ Modulation and Boundary Scan", *IEEE Communications Magazine*, pp. 98-102, June 1999.

[5] M. Jarwala, D. Le and M.S. Heutmaker, "End to End Test Strategy for Wireless Systems", in *Proc. IEEE International Test Conference*, Washington, DC, October 1995, pp. 940-94.

[6] S. Ozev and C. Olgaard, "Wafer Level RF Test and DFT for VCO Modulating Transceiver Architectures", in *Proc. 22nd IEEE VLSI Test Symposium*, Napa Valley, CA, April 2004, pp. 217-222.

[7] S. Bhattacharya and A. Chatterjee, "High Coverage Analog Wafer Probe Test Design and Co-optimization with Assembled Package Test to Minimize Overall Test Cost", in *Proc. 21st IEEE VLSI Test Symposium*, Napa Valley, CA, May 2003, pp. 89-95.

[8] S.S. Akbay and A. Chatterjee, "Feature Extraction Based Built-in Alternate Test of RF Components Using a Noise Reference", in *Proc. 22nd IEEE VLSI Test Symposium*, Napa Valley, CA, April 2004, pp. 273-278.

[9] M.G.C. Flores, M. Negreiros, L. Carro and A.A. Susin, "A Noise Generator for Analog to Digital Converter Testing", in *Proc. 15th Symposium on Integrated Circuits and Systems Design*, Porto Alegre, Brazil, September 2002, pp. 135-140.

[10] M. Negreiros, L.Carro and A.A. Susin, "A Statistical Sampler for Increasing Analog Circuits Observability", in *Proc. 15th Symposium on Integrated Circuits and Systems Design*, Porto Alegre, Brazil, September 2002, pp. 141-145.

[11] M. Negreiros, L. Carro and A.A. Susin, "A Statistical Sampler for a New On-Line Analog Test Method", in *Proc. 8th IEEE International On-line Testing Workshop*, Isle of Bendor, France, July 2002, pp. 79-83.

[12] S. Bhattacharya and A. Chatterjee, "Use of Embedded Sensors for Built-In-Test of RF Circuits", in *Proc. International Test Conference*, Charlotte, NC, 2004, pp. 801-809.

[13] T. Guldbrandsen, "Analysis of Diodes Used as Precision Power Detectors above the Square Law Region", *Conference on Precision Electromagnetic Measurements*, Ottawa, Canada, June 1990, pp.48.

[14] J. C. Cowles, "The Evolution of Integrated RF Power Measurement and Control", in *Proc. 12th IEEE Mediterranean Electrotechnical Conference,* Dubrovnik, Croatia, pp.131-134, May 2004.

[15] G. Klahn, "True RMS Power Detection with High Dynamic Range", *IEEE MTT-S International Microwave Symposium Digest,* pp.1773-1776, June 1999.

[16] S. Ho, "A 450 MHz CMOS RF Power Detector", *2001 Digest of Papers IEEE Radio Frequency Integrated Circuits Symposium*, pp.209-212, May 2001.

[17] M.W. Baker, S. Zhak and R. Sarpeshkar, "A Micropower Envelope Detector for Audio Applications [Hearing Aid Applications]" *International Symposium on Circuits and Systems,* vol. 5, May 2003, pp. 45-48.

[18] W. Sheng, B. Xia, A.E. Emira, C. Xin, A.Y. Valero-Lopez et. al., "A 3-V 0.35-/spl mu/m CMOS Bluetooth Receiver IC", *IEEE Journal of Solid State Circuits*, vol. 38, no. 1, pp. 30-42, Jan 2003.

[19] Analog Devices TruPwr™ AD8361 data sheet, available from: http://www.analog.com/UploadedFiles/Data_Sheets/656100390AD8361_c.pdf

[20] Z. Wang, "Novel Pseudo RMS Current Converter for Sinusoidal Signals Using a CMOS Precision Current Rectifier", *IEEE Transactions on Instrumentation and Measurement,* vol. 39, no. 4, August 1990.

[21] Z. Wang, "Novel CMOS Precision Current Rectifier," Tech. Rep., The Electronics Laboratory (IfE), Swiss Federal Institute of Technology (ETH), Zurich, 1989.

[22] J. Ramirez-Angulo, "High Frequency Low-Voltage CMOS Diode", *Electronic Letters,* vol.28, no. 3, pp. 298-300, Jan 1992.

[23] J. Ramirez-Angulo, R.G. Carvajal, J. Tombs and A. Torrelba, "Very Low-Voltage Class AB CMOS and Bipolar Precision Rectifiers", *Electronic Letters*, vol. 35, no. 28, pp. 1904-1905, Oct 1999.

[24] M. Ratni, B. Huyart, E. Bergeault and L. Jallet, "RF Power Detector Using a Silicon MOSFET", *1998 IEEE MTT-S International Microwave Symposium Digest*, vol.2, pp.1139-1142, June 1998.

[25] C.P. Morera and E.Kerherve, "Dual Mode RF Receiver Front-end Using a 0.25-/spl mu/m 60-GHz f/sub T/ SiGe:C BiCMOS7RF Technology", *17th Symposium on Integrated Circuits and Systems Design*, pp. 88-93, September 2004.

[26] H. Koizumi, S. Nagata, K. Tateoka, K. Kanazawa and D. Ueda, "A GaAs Single Balanced Mixer MMIC with Built-In Active Balun for Personal Communication Systems," *Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 77 – 80, May 1995.

[27] M. Kawashima, T. Nakagawa and A. Katsuhiko, "A Novel Broadband Active Balun," in *33rd Proc. Eur. Microwave Conf.*, Munich, Germany, 2003, pp.495–498.

[28] A. Niknejad, "ASITIC: Analysis and Simulation of Spiral Inductors and Transformers for ICs", http://rfic.eecs.berkeley.edu/~niknejad/asitic.html, accessed September 2005.

[29] A. A. Emira, A. Valdes-Garcia, B. Xia, A.N. Mohieldin, A. Valero-Lopez et al., "A Dual-Mode 802.11b/Bluetooth Receiver in 0.25/spl mu/m BiCMOS", *Proc. IEEE International Solid-State Circuits Conference*, vol.1, Feb 2004, pp. 270-280.

[30] T. Voo and C. Tomazou, "High-Speed Current Mirror Resistive Compensation Technique", *Electronic Letters*, vol. 31, no.4, February 1995, pp. 248-250.

[31] C. Auricchio, R. Bez and A.Grossi, "Narrow Width Effects in CMOS N(P)-Well Resistors", *Proc. IEEE International Conference on Microelectronic Test Structures",* March 1996, pp. 25-28.

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