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A METHODOLOGY FOR MEMORY CHIP STRESS LEVELS PREDICTION

A Thesis

by

KARTIK SHARMA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2005

Major Subject: Mechanical Engineering

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Approved by:

Chair of Committee, Sheng Jen (Tony) Hsieh
Committee Members, Steve Suh
Andrew K. Chan
Head of Department, Dennis L. O'Neal

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ABSTRACT

A Methodology for Memory Chip Stress Levels Prediction. (August 2005)
Kartik Sharma, B.Tech, B.I.E.T. Institute, Jhansi, India
Chair of Advisory Committee: Dr. Sheng-Jen (Tony) Hsieh

The reliability of an electronic component plays an important role in proper functioning of the electronic devices. The manufacturer tests electronic components before they are used by end users. Still at times electronic devices fail due to undue stresses existing inside the microelectronic components such as memory chips, microcontrollers, resistors etc. The stresses can be caused by variation in the operating voltage, variation in the usage frequency of the particular chip and other factors. This variation leads to variation in chip temperature, which can be made evident from thermal profiles of these chips.

In this thesis, effort was made to study two different kind of stress existing in the electronic board, namely signal stress based on variation in duty cycle/frequency of chip usage and the voltage stress. Memory chips were tested using these stresses causing change in heating rates, which were captured by infrared camera. This data was then extracted and plotted to obtain different curves for the heating rate. The same experiment was done time and again for a large number of chips to get heating rate data.

This data consisting of average heating rate for large number of chips was used to build Neural Network model (NN). Back Propagation algorithm was used for modeling because of its advantage of converging to solution faster compared to other algorithms. To develop a prediction model, data sets were divided into two-third and one-third parts.This two-thirds of the data was used to build the prediction model and the remaining one third was used to evaluate the model. The designed model would predict the stress levels existing in the chips based on the heating rates of the chips.

Results obtained suggested

1. There is difference in heating rate for chips stressed at different stress levels.
2. Accuracy of the model to predict the stress is high (greater than 90 %).
3. Model is robust enough that is it can yield efficient results even if there is presence of noise in the data.
4. Generic methodology can be proposed based on the experiments.

This work is progress in the direction of making a predictive model for a complete electronic device, which can predict the stress level existing on any component in the device and will provide an opportunity to either protect the data or removal of the defected components timely before it even fails.

ACKNOWLEDGEMENTS

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Regards to my family and the folks back home who enlighten me with their support every time I need it.

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NOMENCLATURE

SYMBOLS	DEFINITION
amb	Ambient
AH_i	Average heating rate
V_{ss}	Ground pin on SRAM
$H_1, H_2, \ldots, H_N$	Heating rate
MSE	Mean square error
a, b	Parameter for extreme value distribution
γ, β, α	Parameter for log logistic distribution
RMS error	Root mean square error
T	Time (seconds)
V	Voltage
V_{cc}	Voltage input pin on SRAM

CODES

CODE	PROGRAM NAME
1	1206.asm
2	1206ram2.asm
3	1206ram 3.asm
4	1.asm
5	IncrementsRAM.asm
6	IncrementsRAMwdelay.asm
7	Zerosnfswesc.asm
8	Zerosnfswescndelay.asm.

SET CODE	PROGRAM NAME
9	SRAM more -FLASH same
10	SRAM 200k -FLASH same
11	SRAM same -FLASH same
12	SRAM same -FLASH 150k

CHAPTER I
INTRODUCTION

1.1 Motive

Chips are widely used in all kind of electronic components, but they are highly prone to failure. Chip in an electronic device may fail due to voltage overstress or signal overstress existing in the chip. Voltage stress may cause gate oxide breakdown [1], electro migration or breaking of bonds at high temperature. Electrostatic discharge and electrical overstress (EOS) caused due to voltage overshoot are blamed for up to 60% of field failures [2]. Due to the unavailability of accurate circuit level simulation tool lots of work had been done on simulation models [3]. Other detection technologies include Wunsch- Bell Paradigm [4], non-destructive solutions using percolation and FEA tools.

Similarly, signal stress caused due to variation in duty cycle and chip usage may lead to unnecessary heating in the chip, which can lead to the failure of processor chip and other high frequency electronic devices. Jung et al. [5] mentioned duty cycle correction scheme. Okuda et al. [6] gave the different method for duty cycle error correction, while Chen et al. [7] described the effect of dynamic stress testing on memory application.

Currently most of the methodologies for chip testing study the defective chip and try to narrow down on possible causes, which must be avoided or try to analyze the defects using simulation models, rather then collecting real time data, while the chip is in operation. Nowadays demand is for methodology based on the concurrent technology that can give real time analysis of the chip condition and can predict the failure before time based on the stress level existing in the chip.

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits.*

1.2 Nature of the Problem

When the end user uses the electronic components, at times they are subjected to extreme conditions, which might make them to work outside their design limits. In this research two of those extreme conditions were studied: signal stress and voltage stress. Here in this thesis work, we define signal stress due to variation in signals sent in/ out of the particular chip.

In addition, voltage stress refers to the increase in the voltage at address and data pins on chips. Device components at times have to work at maximum capacity, resulting in increased heating rate of the device. The most familiar example is the cooling fan use to cool off over the microcontroller in a PC. The stress resulting on the chip due to the variation in the signals is what we call as the signal stress and can lead to component failure either due to excessive heating or due to internal stuck in faults in the registers.

The voltage stress is caused when the component has to work at some higher voltage than the usual. This result in various kinds of failures in the chip most common is the gate failure at the pins on the chip. Failure can be slow or avalanche depending on the stress level. Voltage stress results in the increase of the temperature of the chip or heating rate and chip may fail due to the breakdown at very high temperature.

For both of these stresses we saw that the heating rate plays a crucial role and increases with increase in both signal stress and voltage stress. As a result heating rate was taken one of the parameters which if kept under control or if there are some methods to detect the variation in the heating rate and then we can avoid chip failure.

1.3 Problem Statement

In this research work, the failure of the chip was identified due to the increase in signal stress caused by the variation in duty cycle and/or frequency of memory chip usage and voltage stress caused due to voltage overstressing on pins. It is assumed that heat will be generated over time as chips are subjected to stresses.

In this research work, heating rate was considered as a primary parameter for developing an analytical model using this parameter to predict the stress level existing in the chips. Neural Network is proposed as a modeling technique for this research work.

1.4 Scope and Objective of Research

The scope of research work is to build a predictive model and methodology which can avoid the failure of the chips under actual conditions by predicting the stress levels existing in the electronic components or board as a whole.

The research objectives can be summarized as follows:

- To understand the relationship between heating rate and stress levels.
- To build a Neural Network model for failure prediction based on the voltage stress existing in the component using the relationship between stress and heat rates of the electronic components while in operation.
- To build similar kind of Neural Network model for failure prediction based on signal stress existing in the component using the relationship between heating rates given by chips and corresponding stress level existing in the chips.
- To test the noise tolerance of the model developed using statistical tools.
- To proposed a generic methodology for electronic stress level prediction.

1.5 Format of Research Work

The progress of research work, starting from the idea of studying the thermal profile and then carrying out experiments and modeling to build the prediction model is mentioned in the following chapters.

Chapter II in the research work consists of the literature review on the possible stresses existing in the chip, failure caused due to stresses, current methodologies and prediction techniques.

Chapter III talks about the various aspects of board and the chip and design of experiment.

Chapter IV describes the way experiments were conducted for all the stresses to gather the heating rate information.

Chapter V gives the results obtained from experiments and inferences obtained on the basis of results.

In chapter VI the model was tested for its robustness by comparing the deviation in data to its effect on the model results.

Chapter VII consists of the generic methodology that can be for creating a prediction model based on the stress existing in chips.

Finally last chapter VIII consists of the conclusion drawn and the future work that can be done on similar lines of research.

The entire procedure of using thermal profiles and using Neural Network modeling technique is innovative and can be successful in predicting the chip failures. The conclusion is drawn in the end based on the results from the neural model and its noise tolerance efficiency.

CHAPTER II
LITERATURE REVIEW

2.1 Introduction

The research work is related to stress level prediction which is a part of field of reliability and testing. This chapter starts with brief history on chip reliability and testing. First few page deals with the reliability theory, followed by sections which talk about current techniques and prediction methodologies. The last section in literature review talks about stresses specifically those that were our main concern in this research work.

Chip reliability and testing is vast field of research in electronics industry today. Every year millions of dollars are spent to find out the answers to various reliability issues and for the analysis of chip failure. Two main reasons for many research efforts in the field of chip reliability and failure analysis are given below:

- First, the use of memory in electronic devices is indispensable and thus their failure during operation is not only irritating to end-users, but may result in the loss of life and valuable information.
- Secondly, historically speaking the number of bits per chip has quadrupled roughly every 3.1(π) years; and as memory chips have become more complex, so have their faults and sensitivity to faults. On the other hand, due to economic reasons, the test cost per chip (which is directly related to the test time) cannot be allowed to increase significantly. As a direct consequence, economical memory testing has been the subject of a large research effort.

2.2 Electronic Reliability

As the first reliability studies have been made in the USA, at the beginning the American definition has been adopted: "The reliability is the probability that a certain product does not fail for a given period of time, and for certain operational and environmental conditions" [8].

The evolution of reliability field can be traced between the milestones of the semiconductor manufacturing history as given by Birolini, Kuehn, Knight and Bazu. The first studies concerning the electronic equipment and its reliability have been made for the purpose to improve the military avionics technique and the radar systems of the army. The mathematical formulation of the reliability and its utilization for material tests originate in ideas born in WWII when Werner Von Braun and his colleagues worked on V1 missiles. They started from an idea that a chain can't be more resistant than its weakest link. But repeated failure and multiple errors make them realize that all the constructive elements must play a role in reliability evaluation [8].

As of today reliability has been defined as the probability that an item will perform a required function under stated conditions for a stated period of time. Factors affecting the reliability of a product cover a large range of variables including design, manufacturing, application and the human involvement factor at each stage of production.

For a product to have high reliability it should have a low failure rate; and in order to achieve a low failure rate, careful failure analysis is needed. The origin of device failure analysis began with the invention and fabrication of the transistor. Initially single transistor, such as point contact structures and micro alloy germanium devices, could be analyzed by adopting previously developed metallurgical cross- sectioning procedure [8].

The entire semiconductor industry was revolutionized by silicon planar technology. Optical microscopy was extensively used at that time.

With the introduction of multiple devices fabricated within the same chip (ICs), electrical diagnostics became more complicated. Failure analysis technology continued to grow in parallel with IC fabrication in devising ways for selective passivation removal and methods for isolating individual transistor [8].

Reliability studies are performed to find out the reasons for chip failure and methods to avoid the failure. During its lifetime, a memory chip goes through various phases from wafer to final wear out period where it is highly susceptible for failure.

Failure classification of the memory device can occur, depending on the cause, depending on the speed of failure or depending on the technical complexity. For simplicity, all failures can be broadly characterized into two categories [9].

- *Failure Due to Manufacturing Defects at Chip Level and PCB Board Level:* These failures arises due to the defects during manufacturing processes such as Epitaxy, Oxidation, Patterning, Diffusion, Thermal treatment, Cleaning, Etching, Bonding etc. [10]. PCB board defects may be caused due to improper wiring, missing chips and defect on board etc.
- *Failure Due to User Environment:* This type of failure arises unexpectedly when the user is in control of the device. These may be catastrophic failures causing interruption of the normal operation, or drift failures, producing defective operation by varying electrical characteristics. These defects are primarily caused due to electrical overstress, thermal overstress, and environmental stresses.

Most failures arising during the manufacturing and the user environment stage are due to the stresses that are inherent during the whole life cycle of the device. From the wafer stage until final packaging a device has to go through lots of mechanical and thermal stresses and in practice, lots of these stresses still remain inside the memory and affect functioning at the later stage. The next section describes current techniques for memory chip testing that are widely used in industries to detect these failures.

2.3 Current Approaches in Testing Memory Chips

Lots of research has already been devoted to the techniques being used in order to test the memory chips. These tests are done to find out the reliability of the chip while in operation. Here some of those important techniques are summarized.

Testing for inbuilt manufacturing defect can be done through electrical tests using flying probe testers, using manufacturing defect analyzers, using automated optical inspection, infrared thermography, acoustic micro imaging, and laser systems [11].

For environmental stress screening stress may be applied in combination or in sequence on an accelerated basis within the product design capabilities. Stressing can be thermal cycling, vibration or both. Temperature range used is -65 to 230 deg F [11].

For finding the faults existing during functional or operating conditions electrical characterization is performed. It is a parametric, experimental analysis of the electrical properties of a given integrated circuit; its purpose is to investigate the influence of different operating conditions on the IC's behavior. Electrical characterization is thorough and exhaustive and can be carried out on an automatic test equipment (ATE) and resulting in all practical combinations; device supply voltages, logic input/output voltages, temperatures, timing conditions, parametric variations, various test patterns, operating frequency responses, modes of operation and power consumption [9].

Screening tests and test strategies includes Burn in (statically or dynamically), constant acceleration, ESD tests, glassivation, high temperature storage, hot carriers, humidity or damp test, latch up test which simulate voltage overstress on signal and power supply line as well as power on/ power off sequences**,** seal test, soft errors, solderability, thermal cycles and time dependent dielectric breakdown [11].

Test programs for the RAM memory consist of three items: DC parametric test, AC parametric test and functional test (although they often are applied simultaneously). A memory test program comprises various tests such as continuity check, leakage tests, a variety of functional tests, dynamic or timing tests, and parametric tests. Functional tests by far are the most important test where in DUT (device under test) is in dynamic test mode, which uses fast changing input stimuli to check the DUT's internal logic, i.e. check the storage and retrieval of standard patterns at rated cycle times. Various test patterns and truth tables are use for the functional test. Some of these test patterns include GALPAT, DIAPAT, MARCH, CHECKERBOARD [9].

Other tests that can be performed and play the most important role during the life cycle of the memory device are termed under *life testing*. The purpose of life test is to obtain information about the lifetime properties of the components. The term reliability testing is often used synonymously with lifetesting. As actual test for the memory device

life cycle is not feasible, several kinds of accelerated tests are performed and inferences about the reliability of the components under different set of loading conditions can be made based on a proven acceleration model [12].

Accelerated tests [13] (ATS) are used widely in manufacturing industries, particularly to obtain timely information on the reliability of product components and materials. Generally, information from tests at high levels of stress (e.g. use rate, temperature, voltage, or pressure) is extrapolated, through a physically reasonable statistical model, to obtain estimates of life or long-term performance at lower, normal levels of stress.

There are fundamentally two different methods of accelerating a reliability test:

- Increase the use rate of the product
- Increase the aging rate of the product by changing the conditions in which it is ought to work i.e. its loading conditions, thus decreasing the safety margin.

There are two important prerequisites that must be fulfilled, if useful information is to be derived from an accelerated life test:

- The failure mechanisms generated in the accelerated test must be the same as those observed under normal operating conditions.
- Its must be possible to extrapolate the lifetest results from the accelerated conditions to normal operating conditions.

Most accelerated tests data analyses include a combination of graphical methods (scatter and probability analysis) and analytical methods (regression analysis) based on the maximum likelihood (ML) estimation. These methods use the statistical models such as Arrehenius model, Monte Carlo simulation etc. Though most of the literature is devoted to using statistical methods for accelerated testing but there are other methods as well to analyze the data obtained from the accelerated tests. Few examples of new techniques that have evolved after different combinations of these traditional methods and using new devices are:

- Methodology for finding the *metallization and the gate defects* are photoemission microscopy, liquid crystal analysis [14], Voltage contrast [15] or internal probe [16, 17].
- Methodologies for SRAM defect due to the gate oxide short [18] based on the surveillance of the circuit current consumption (IDDQ) are more efficient than logic testing.
- Methodology for *Defect in chips due to metallization* shorts and the technique to single out the defect [19] can be external electrical functional test or internal contact less beam testing.
- Methodologies for SRAM bit failure due to the high frequency operations [20] uses nanoprobes and a minute manipulator is use to find out these defects.
- Methodology for *SRAM cell cold failure* [21] is based on using the electrical signatures of the transistors of SRAM cell after isolating the cell**.**

All the methods that are described above are those, which can either find the defect and errors in the memory at the time of inspection or at the user level. But what about predicting the reliability of the chip in future or say lifetime of the memory chip? Most of the research work that is being presented is based on the handbooks that were developed by the reliability engineers based on the experience and the statistical data. Most of those handbooks still serve as the guide to predict the lifetime estimation of the memory device [22]. But as already mentioned in earlier text, today need is for concurrent methodologies which can help in either protecting the component or provide opportunity for safe transfer of the important information before failure can occur.

2.4 Prediction of Stress Failure in Electronics and in Memory Chips

In 1860, A.Wohler presented some of the earlier fatigue failure information; the S-N curve that he showed identifies the stress below, which no failure will occur. Reliability engineering for electronics started with the establishment of the Ad Hoc Group on reliability of electronic component in 1950s.The first formal handbook was

publication of RCA called TR- 1100. In the following years RCA proposed a new prediction model for microcircuits, based on work of Boeing Aircraft Company. One was steady state temperature and other was mechanical related failure rate. The advent of complex microelectronics devices pushed the application of MIL-HDBK beyond reasons and they are used in comprehensive number around the world these days [23, 24].

Given the system architecture and parts, reliability prediction models are used to assess the influence of the magnitude and duration of the stresses on the reliability of the parts and systems, so that stress, environment controlling techniques and derating techniques can be implemented. For electronics derating parameters include current, voltage, power frequency and temperature [25].

The traditional approach to predict the long-term reliability of devices in field use involves implementing statistical models, using the exponential or constant failure rate model [26, 27, and 28]. Modified traditional approach is doubly conservative. After a time of 10^4 hr or say 1year it fixes the failure rate to be constant [29]. Other prediction techniques involve using the MIL-HDBK, Bellcore TR-NWT standard handbook, for the failure rate prediction. The new approach: Physics of failure modeling [12] arises due to lot of dissatisfaction in traditional technique. New approach is based on developing number of models for physics of failure lifetime evaluation. These models address the long-term wear out phase primarily. Modeling of electromigration failure and corrosion had already been mentioned in the modeling literatures.

Many of these approaches are used for the stress failure analysis of the memory chips. One such model based on the physics of failure approach was given by [9] called as *SYRP- for predicting failure rate* in a lot- based on the physics of failure lifetime evaluation.

Though most of the prediction methods that are being used in the memory chips are based on the RPP (reliability prediction procedures) as given in MIL-HDBK-217. Dynamic life testing methodology is used for purpose of quantifying the performance degradation during IC operation. Infact dynamic life testing is done for two major types

of degradation mechanisms: electrical ones (such as latchup, ESD, hot carrier effect, dielectric break down and electromigration) and environmental ones (produced by thermal stress, humidity) [12].

The accelerated tests stand-alone as the best-suited method for predicting the life time performance of the memory device. These tests are based on the fact that the life of a memory device can be compressed to few days or even to few hours. Thus faults that would occur in the memory in the near future occur during the test and estimation and prediction about the lifetime of the memory device can be made.

2.4.1 Traditional Accelerated Test, Statistical Models and Methods

For predicting the failure of the components using accelerated techniques, two statistical methods are widely used. One of them is Arrehenius model, which is used to predict the failure based on temperature-accelerating factor. The other one is the Eyring model based on the voltage-accelerating factor.

There are few other models that don't use statistical methods or mathematical modeling but use other advanced methods such as Neural Networks or Computer Aided Design for doing accelerated tests. Though these tests are not done on the memory devices but they have been done for residual life prediction from vibration based signals using Neural Network approach where in the input data is fed in to the feed forward back propagation Neural Network [30]. The device produces a signal of different frequencies or when device starts malfunctioning is known. As a result the signals at which the failure or the malfunctioning occurs are noted and then used for the input in Neural Networks [31, 32].

Next section talks about stresses, which can cause chip failure and are studied in this research work.

2.5 Stresses on Memory Chips

Till now we already reviewed reliability, current techniques for detection and also failure prediction techniques. In this section stresses that are existing within the chips, which leads to its failure at manufacturing stage or after a lifetime are discussed. We also talked about the current work that's been done in voltage stress and signal stress specifically, which is main concern of this research work as well.

2.5.1 *Mechanical Stresses*

Both tensile and compressive stresses exist inside the memory device. If we look at the wafer grain surface due to ion implantation and bonding there are different stresses at the grain boundaries. These stresses can cause the failure of the memory devices if they are present in excess.

2.5.2 Electrical Stresses

SRAM when under operating conditions is subjected to different kind of stresses. These stresses can be voltage stress, current stress, or current density.

2.5.3 Environmental Stresses

Stresses arise due to the internal and external conditions such as vibration, shock, radiation, humidity, temperature, and contaminants. The failure mechanisms involved in all these process are generally corrosion, distortion, fatigue, fracture and wear. These defects may cause electro migration, change in electrical parameters, deformation, cracking, change in resistance, degradation, acid formation, material fatigue, shorting of electrical parts, and permanent stress etc [11].

The stresses that are being studied in this research work are voltage stress and signal stresses. This section describes the current study and research being done in either detecting these stresses in chips or predicting failure due to them.

2.5.4 Voltage Stress

The chip may fail due to various different reasons when subjected to higher than normal voltage. Generally if voltage overload is slowly applied then bond wires fail and if it is applied relatively fast then silicon junctions fail. But the location of the failure depends on the current path and melting temperature of the materials. Various methods are used to either predict overstress directly, or find a model that simulate the conditions and that data can be used to find out when the chip is going to fail [2].

One of the major reasons for failure due to chip overstress is ESD (electrostatic discharge). ESD failures are usually due to a brief, high intensity static charge, often caused when an improperly grounded human or machine handles the chip. Similarly EOS (electrical overstress) failures typically involve long term low intensity stress such as might arise if a part consistently ran at a higher voltage or clock speed than intended [2].

Some of the novel techniques used for detecting of stress is using thermal simulators. In [33] algorithm for thermal simulations is given for electothermal simulation. This algorithm helps in studying the transient thermal effect caused due to existence of electrical overstressing. The algorithm is based on the region wise exponential approximation technique and a recursive convolution scheme. Like wise lots of other electrothermal circuit models are defined to simulate the conditions resulting from the thermal degradation setting in the chips due to overstressing [34].

In another approach electrical overstress is considered to be the effect of plasma instabilities and Wunsch-Bell thermal paradigm was used for practical failure modeling [35]. Also an engineering method based on the failure threshold of diodes and transistors due to reverse biasing pulses that are generated due to electrical overstressing is mentioned in [36].

Along with research for predicting electrical stress there is an ongoing effort to predict the defects that are produced due to overstressing. iTEM which is a reliability diagnosis tool for electromigration [37] and iCET a chip level electrothermal simulator which gives the CMOS on chip steady state temperature profile and circuit performance

for given input conditions [38] are used. Substrate resistance extraction method that accurately calculates, the distribution of injection current into the substrate during ESD or latch up resulting from overstressing is mentioned in [39].

Most of these methods create the simulation of the component failure but today demand is for the concurrent technologies, which can predict the failure before time and avoid the unnecessary failure of the chips. One of the current technologies based on the concurrent engineering was developed at Hughes Aircraft Company, radar system group. They developed software called HAC RPP, which concurrently does the computation of derated and stressed part failure rate/ unit and identifies overstressed part problem [40].

2.5.5 Signal Stress

Signal stress can be caused due to variation in signal frequency, clock frequency, duty cycle or if the signal voltage is kept higher than the normal.

Signal stress we used for the research was the stress induced, when continuous signals are send to chip and chip processes that information as compared to when its working intermittently. This kind of stress can be understood as the variation in the duty cycle as well as the variation in the frequency because it depends upon, how frequently code is running on the chip and the duration for which the code was running each time.

Most of the work done for signal stress is based on finding out the defects during the duty cycle variation and defects due to variation in frequency.

Research has been done on variation in the frequency to outline various defects and detection techniques. Nowadays chips are being made which can work in access of 200 MHz. Dobberpuhl [41] mentioned the technique for self stress test for the systems working at very high frequency. It investigates the reliability concerns due to hot carrier injection, electromigration under realistic circuit conditions**.** Snyder et al. [42] did work to analyze the reasons of failure while the chip is working at very high frequency. Ikeda, Yoshida et al. [43, 44] described various different techniques such as nanoprobes, selective etching and TEM observations to analyze the bit failure that occurs at low voltage and high frequency operating speeds.

Research has been done to understand and detect the defects caused by the variation in frequency. The most prominent defect that may arise is the hot carrier injection as mentioned in [45].

The work on frequency variation in most of the researches deals with the variation induced due to variation in clock frequency of sending the signals but here in the research the term frequency means as to how frequent we are using particular component. This way we can avoid its overuse or prevent it from failure due to overuse by comparing the heating rate for the chip when it is working continuously and when its working intermittently.

There were several codes, which were run on the chip for reduced duty cycle. The heating rate difference was calculated to give us the fair good results from which we can show that there is fairly good reason between the heating rate when chip is working continuously and when its working intermittently.

As memory chip was used in the research so there was no significant increase in the chip-heating rate, which can cause the failure. But if the similar work is done for the microcontroller then we can build a heating rate model for variation in signal stress that is duty cycle and the frequency of the signals and avoid over heating which can lead to the failure of the chip.

From the literature review it is clear, though lot of work is done for chip failure and controlling the parameter which might lead to its failure but lesser work is done in predicting the chip failure if it might occur while chip is being used. This research work is thus novel in finding out the possibility of predicting the chip failure due to two most important parameters namely voltage overstress and signal stress.

All this can prove to be a step towards building a predictive model for complete electronic device based on the similar lines of conclusion.

CHAPTER III
DESIGN OF EXPERIMENTS

3.1 Introduction

This chapter details the features of the 8051 board used for the research. Description of static random access memory and its functional diagram, material used, detailed test set-up along with the data acquisition techniques and finally the hypothesis used for testing are given. This design of experiments gives the overall view of the various components, which were used for the research and also the test setup that was used to do the experiments.

3.2 Experimental Setup

This subsection consists of the details about the micro controller board that was used for the research work. It discusses the basic features of 8051 board, description of SRAM used manufactured by Samsung, function of the SRAM, test set-up, material used and finally data acquisition and imaging procedure.

3.2.1 Features of 8051 Board

Some of the features of the 8051 board used were standard 87C52 CPU clocked at 22.1184 MHz, with on board 32k SRAM (2000-7FFF) and 30k FLASH ROM (8000-F7FF). It can also work at high-speed baud rates: 115200, 75600, 38400, etc. It had eight LED’s controlled by 8 dedicated I/O lines. Figure 3.1 shows the layout of the board and the SRAM used.

Requirement for the board were DC Voltage (8 - 15 volts), AS-31 Assembler or Compiler, Terminal Emulation Program, e.g. HyperTerminal (windows) or VB code. The internal layout allows the data transfer between micro controller-FLASH, micro controller-SRAM.

3.2.2 General Description of SRAM

The SRAM used belonged to K6X0808C1D family of CMOS chips [46]. It supported low data retention voltage and current. The normal operating voltage range for

SRAM was (Vcc Range: 4.5 V- 5.5V). Voltage on any pin relative to V_{ss} was (–0.5 to +0.5 V on V_{cc}) and maximum was 7.0 V. Voltage on V_{cc} supply relative to V_{ss} was (–0.3 to 7.0 V).

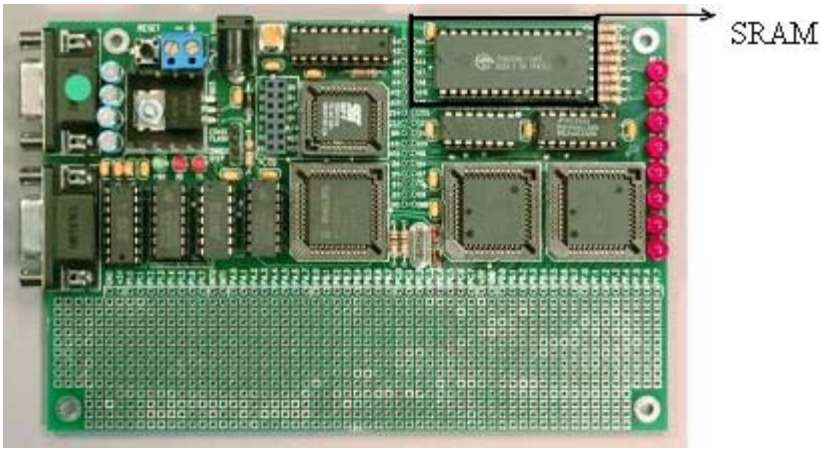

Figure 3.1 Layout of the board and SRAM used for experiments.

3.2.3 Function of SRAM Diagram

Since the goal of the experiment was to excite the SRAM it is important to understand the functioning of the component to excite it the most. The SRAM functions in a series of steps as is shown quite well in the timing diagrams. To explain its function it is important to know the overall function of the SRAM in tandem with the 8051 microcontroller. The microcontroller is able to send and retrieve data from the SRAM by sending two important pieces of information: the address of data to be read/written and the data to be written if that is the command to be used. The SRAM is tied to the microcontroller by several lines as shown in Figure 3.2.

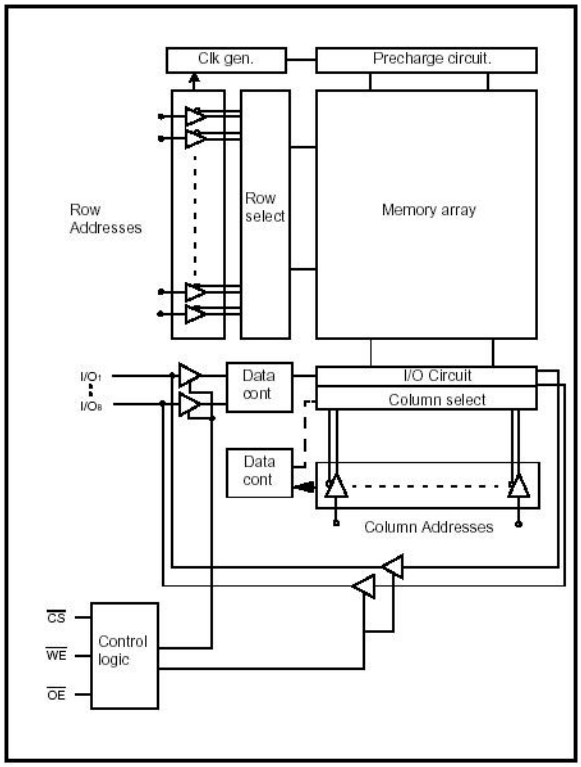

Figure 3.2 Functional block diagram for SRAM.

The first lines are the write enable, and output enable lines, or WE and OE, which are used in reading and writing data to the SRAM. The other single wire connected is the chip select wire. This wire is used in indicating that this particular chip is to be used to store the incoming data, and will thus be used in writing data to the chip. This is incase there are multiple RAM chips for one particular board, it may be necessary to send data to a different RAM chip. The last individual line on the SRAM is the line tied to the system clock of the microcontroller. This is to allow the chip to sync up with the controller so that all data is captured properly and not at in between values. It is also used so that the SRAM will know when exactly eight bits have been entered and are ready to be read into and placed in memory. Also going from the controller to

the SRAM are a series of address and data lines. There are 15 address lines, and 8 data lines used to transmit data.

The read cycle shown in Figure 3.3 is a simple process that essentially requires two steps out of the microcontroller. It first will begin sending the address bits to the RAM chip(s). The RAM chip(s) will receive the bits and one will be pulsed low on its CS line. At this point it will also have its OE line pulsed low as well, enabling it to send the data specified by the address it is receiving.

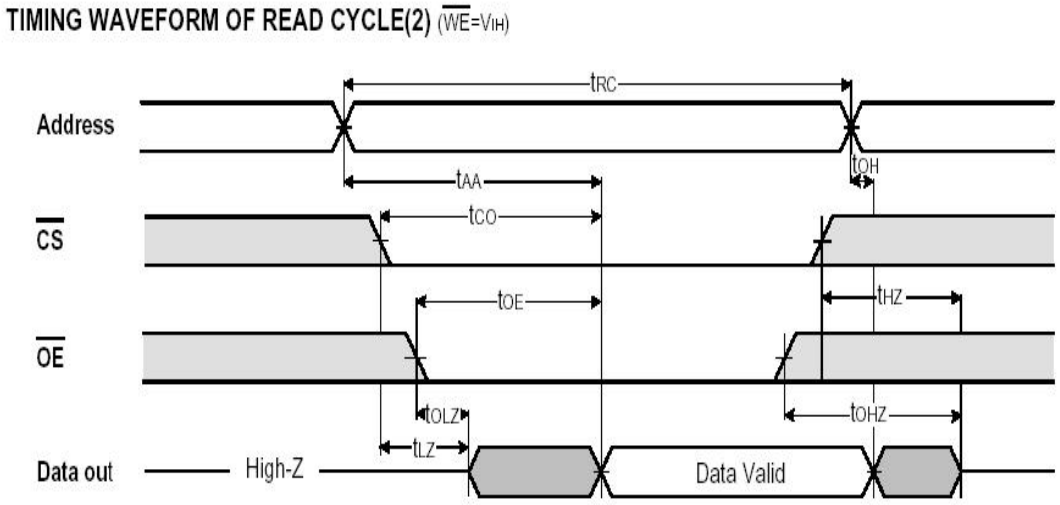

Figure 3.3 Timing waveform for the read cycle.

The write cycle shown of the SRAM in Figure 3.4 is quite similar to the read cycle with the exception that the microcontroller sends data to the SRAM which is one more step in the process. To write to the SRAM, the first step is for the microcontroller to send an address to the SRAM followed by pulsing the chip select line and write enable line low. This will allow the address lines to bring in the memory location to be written to and will divide the information into row and column addresses. At this point the data will be coming in and placed into the address specified on the address lines.

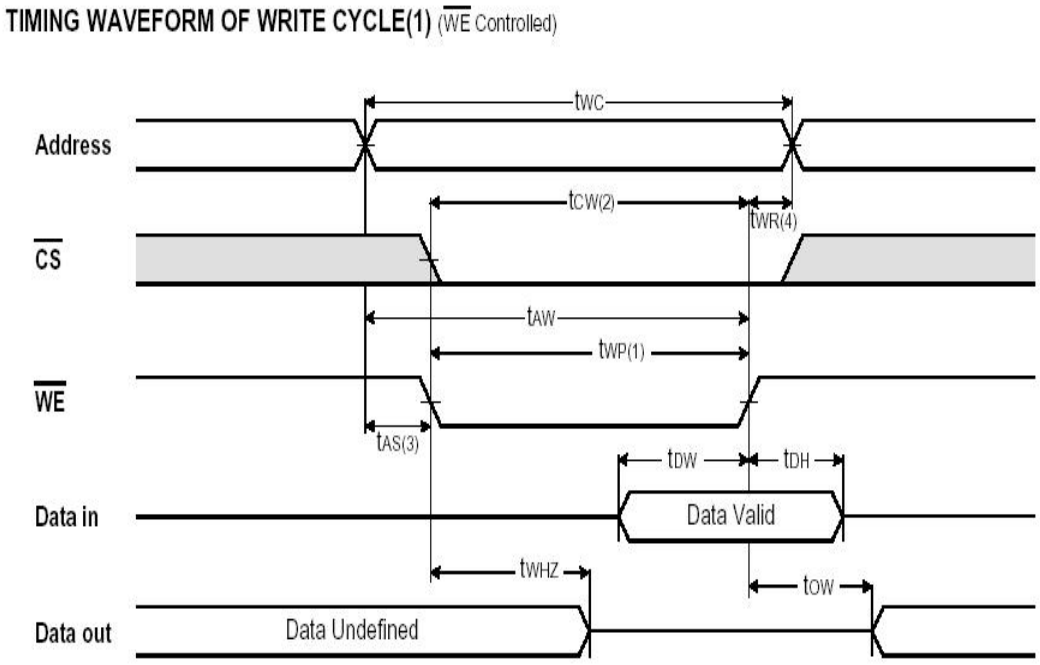

Figure 3.4 Timing waveform for write cycle.

3.2.4 Materials

Electronic equipment used for the experiments include 8051 development board communicating with computer through COM port, a enclosure with infrared camera inside it, special arrangement for experiments, bread board, connectors to stress the chips, power supplies. Also two thermocouples one for measuring temperature of the room and other inside the box, O-scope and digital multimeters were used. Various software tools were used for evaluating, collecting and analysis of data such as MATLAB's Neural Network tool box, Statistical software tools like Statmost, Best Fit.

3.2.5 Test Set-Up

A connector was mounted on a board. Chips were placed over this connector while the board was kept on a fixture inside a black box that also has an infrared camera mounted inside it. This infrared camera was used for imaging the chip on the board,

while chips were stressed. The other end of connector was soldered to another connector via ribbon cable. This second connector was inserted in the slot for SRAM on the micro controller board. The purpose of this kind of arrangement was to keep SRAM separated from all the components on the micro controller board. As imaging was done for heating rate from SRAM so there was no use keeping the micro controller board having all the other components beside SRAM under infrared camera. That is why micro controller board was kept outside the box and only the ribbon cable connects the SRAM on the board, inside the box, with micro controller board outside the box.

Beside experimental setup few softwares were also used. VB code APPENDIX B was used to synchronize the time between turning the power on, on the micro controller board, sending the code on the board and start imaging through infrared camera. This VB code mimics the HyperTerminal in windows but saves all kind of manual operations involving opening and sending the data file to micro controller. Besides that all the process of opening the files and sending the code and running it can be done by single command thus its easy to turn the power on and enter the command to send the code simultaneously. This way synchronization between turning the power on and sending the code was achieved. Power was turned on and at the same time code was sent on micro controller board as soon as first scan gets over. This way all three are synchronized.

Two more softwares were used. WinTes to take the images using IR camera and Thermal View to get the heating rate data from the images obtained from IR camera. With this setup completed, we were ready for experiments.

3.2.6 Image and Data Acquisition Procedure

1. Once the codes were stored on SRAM, board was kept over a fixture inside an enclosed chamber.
2. Infrared camera that was permanently fixed inside the chamber was positioned to take images of chip over board.

3. Once chip was properly placed and chamber was closed, VB code was used to start the codes already stored. VB code was used to synchronize the time between turning the power on and running the code.
4. Each code was run on the chip for specific time duration during which infrared camera takes images every 20 secs or 7 secs depending on the experiments.
5. At the end of the trial we had several images from which data regarding the variation in the heating rate was obtained using Thermal View software. The heating rate was plotted on excel charts.

3.3 Hypothesis

In general terms hypothesis can be understood as the basis of doing any experiment. For every experiment we need to test certain hypothesis. Components of hypothesis are [47]:

3.3.1 Null Hypothesis: According to the null hypothesis

$$H_0 = \text{All } \tilde{\mu}_i \text{ are same}$$

where $\tilde{\mu}_i$ is the performance variable which is the heating rate in our case.

Performance Variable = $\tilde{\mu}_i$ = "Average Heating Rate"

3.3.2 Alternative Hypothesis: According to the alternative hypothesis

$$H_a = \text{At least two of the } \tilde{\mu}_i \text{ 's are different}$$

Model can only be created if Alternative Hypothesis proved to be true.

CHAPTER IV
EXPERIMENTS

4.1 Introduction

Our main aim was to build a predictive model based on the heating rate emitted from the chip under voltage stress and signal (frequency/ duty cycle) stresses. For reaching on to that point we needed to follow certain steps.

These steps included finding out the heating rate for chips, which were stressed, extracting data using thermal view and finally building a model.

But before starting on the actual experiments from which model was created, few preliminary experiments were done to explore the parameter settings needed. This information would help us to reduce the errors in the later stage of the experiments.

Sections in this chapter discuss about results from preliminary experiments, methods to avoid errors and details of all the experiments done, while stressing.

The experiments can be categorized into two parts.

- *Preliminary Experiments:* These experiments served as a platform and mean to standardize the second set of experiments. This set of experiments included experiments for ascertaining parameters such as “how long the chip should be stressed, what should be the cooling time, what should be the stress levels on the chip, what codes needed to be used etc.?”
- *Full Experiments:* The second set of experiments referred to experiments that were needed for obtaining data for developing Neural Network. This set included experiments for voltage stress and signal frequency/duty cycle stress.

4.2 Preliminary Experiments

Following are the results that were obtained from preliminary experiments. At the end of these experiments we had all the necessary information that was needed to do the experiments that would finally give us the heating rate data to build the model.

- Heating rate from chips became constant in approximately 2 minutes, thus scanning time was reduced to less than 5 minutes.
- Cooling time for the chip was same irrespective of whether it was a stressed chip or unstressed chip.
- There was little effect due to random noise by infrared camera.
- While doing voltage stressing, with positive voltage overstressing on V_{cc} and ground on V_{ss} pins on chip as shown in Figure 4.1, no difference in heating rate between various stress levels was obtained. This was also proved by considering results from both F-test and excels graphs. Neither there was any difference in memory map between stressed and unstressed chips. The reason might be V_{cc} pins are better protected against voltage surge than data or address pins or V_{cc} pin connections do not directly interacts with the die area.
- Heating rate difference was obtained when stressing was done on data pins and address pins simultaneously. The detail of the test are as follows:

1. **Pins to be stressed:** Two data pins and an address pin were selected because it was possible to clearly differentiate between heating rates while stressing these pins. Although earlier V_{cc} pin was stressed but heating rate failed to give any significant difference for unstressed and stressed chips.
2. **Stress Levels:** For the experiment 10 chips were stressed for five minutes each starting at 5.5V and going till 6.75 V. Chips were tested after every five minutes of stress to see if they were still working or not. Based on the finding it was concluded that out of 10 chips 7 of them failed when 6.75 V was supplied for five minutes. Thus the highest stress voltage was kept at 6.75 V.
3. **Time for Stressing:** Experiment results suggest that chip failure occur while temperature exceeds 350 °F and chips attain that temperature within first two minutes for the least voltage stress used. So the time for least stress level was around 2 minutes and it decreased correspondingly with increase in the stress level depending on how fast upper limit of temperature (>= 350 °F) was reached.

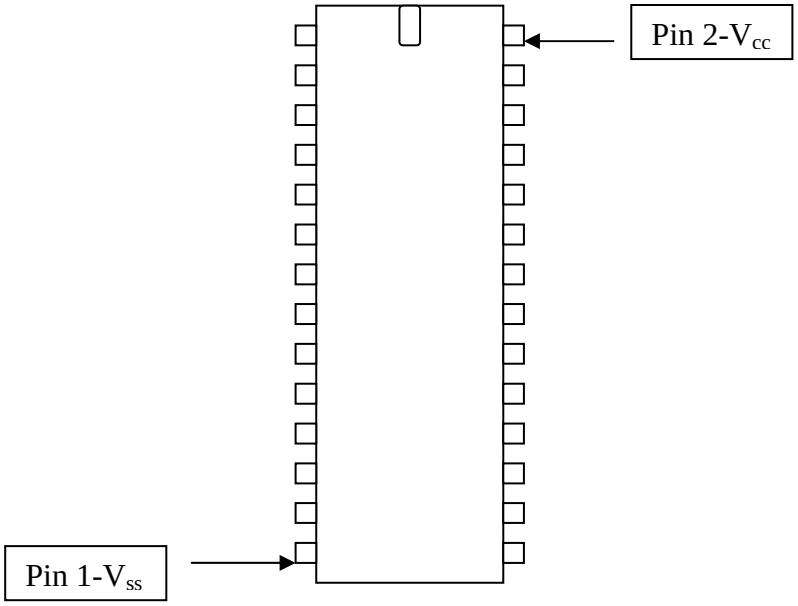

Figure 4.1 Pins that were stressed V_{cc} (+) and V_{ss} (-).

- From the graphs between the heating rate and average heating rate, we observed that variation in heating rate was much smoother for graphs based on average of heating rates thus it was decided to build model based on average of heating rates for chip and die area.

  Average Heating rate for a cell (particular row and column) at N^{th} time interval is defined by taking the average of heating rate of cell, at that time interval and at all previous time intervals.

  Consider that initial heating rate is given as H_o and subsequent heating rates for every interval are defined as H_1, H_2,…..,H_N, then average heating rate at N^{th} time interval is

$$AH_N = \sum_{i=1}^{N} H_i \qquad 4.1$$

AH_i = Average heating rate at i^{th} time interval

H_i = Heating rate at i^{th} time interval

- Increase in the temperature of the chips was exponential. At higher voltage which was around 7V the increase in the temperature from ambient to the failure temperature (>300 °F) was within couple of seconds.
- The failure rate of the chips was thus exponential as well; i.e. the time for failure decreases exponentially with increase in the stress level.
- There exists heating rate difference between unstressed chip and stressed one if stressed chip was made to run just after it was stressed but if its allowed to cool down for a day or two, no difference in heating rate exists between the two chips. The reason may be the tendency of the chip internal architecture to snap back to it normal conditions once it cools down.
- For the particular memory chip that was suppose to work within the range of 4.5V to 5.5V the failure rate was significantly higher at 6.75 V and above.
- When chip temperature is above 350 °F, the failure rate is around 40%.

4.3 Avoiding Errors

Few house keeping things to be aware of while doing the experiments are as follows.

- Do not touch the chips with bare hands or blow air near the chips.
- Try maintaining the ambient environment constant inside the chamber.
- Try maintaining the same chip position and Infrared camera position.
- Check for possibility of shorts on the board.
- Check for any inconsistency in data due to environmental factors or due to human errors such as time lag between turning power on and sending code to the micro controller board.

4.4 Experiments with Signal Stress-I

Signal stress experiment was done in two parts based on different ways of applying signal (frequency/duty cycle) stress.

First experiment was done to find out the effect of signal density variation for the data transfer across the SRAM and the micro controller. This kind of signal stress imitates the stress existing due to the variation in frequency of usage of particular component, SRAM in our case.

For the experiment, two codes each with two modifications were used. In the next paragraph, basic differences in the codes are explained. More detailed explanation is provided in APPENDIX A.

Two codes were used along with two modified codes, from each one of them, consisting of series of NOPs (No operation loop) in the codes. Code 5 “IncrementsRAM.asm” incremented the value by 1 moving across the SRAM memory and increased the value till it reaches to the end of the address and then repeats the loop back again. Code 6 was the modification in the code 5 with finite number of NOP loops in the code, which caused the delay in execution of commands in the code. Code 7 “Zerosnfswesc” filled the address with zeros till it reaches to memory address 7FFF and then it looped back and filled the addresses with F’s, this procedure was done repeatedly till “ESC” key was pressed. Code 8 was the variation in the code 7 with NOPs loop in the code, which does the same operation as explained for code 6 above.

For each one of them, time for execution of the commands was different on SRAM therefore they stressed the chips to different extent, depending on the usage of SRAM. For codes with NOPs the commands NOPs were executed faster than the instructions in the codes without NOPs. As a result the code with NOP heated the chip far more than those without NOPs.

Also between the two codes there was slight heating rate difference because of variation in data stored at different memory addresses as these values corresponds to variation in voltage level stored in the chip capacitors. Table 4.1 shows the test matrix based on the above description.

Table 4.1 Test matrix for the experiment based on the different tests on unstressed chips.

Number of chips	**Codes Used**
40	Code 5 – IncrementsRAM.asm
	Code 6 – IncrementsRAMwdelay.asm
	Code 7- Zerosnfswesc.asm
	Code 8- Zerosnfswescndelay.asm

In these experiments two trials were done on each chip. Testing was done on 40 chips; out of which two-third were used to develop Neural Network model and one-third test the model. The amount of time between each subsequent trial was reduced to 7-8 minutes, which includes 2-3 minutes of blowing air in the chamber, 2 minutes of leaving the box open and lastly 2 minutes of leaving the box closed. In total of 4 codes were made to run for 3 minutes on each chip and adding repeated trials to it, we did 8 trials on each chip, which took around hour and half for each chip. Again specific care was taken to keep the chip position to be same for every trial and for every test and to avoid or reduce the error due to human intervention.

4.4.1 Procedure

The design for the experiment and test set-up was already mentioned in detail in chapter-II. Following steps describe the procedure for performing signal stress experiment.

1. Once the codes were stored on SRAM (for Signal Density stress-I), board was kept over a fixture inside an enclosed chamber.
2. Infrared camera which was permanently fixed inside the chamber was positioned to take images of chip (SRAM) on the board.

3. Once chip was properly placed and chamber was closed, visual basic (VB) code automate the testing procedures by synchronizing the time between turning the power on, running the code and start imaging the chip for its heating rate.
4. Each code was run on the chip for a minute and a half for which infrared camera takes images every 20secs.
5. At the end of the trial we have 7 images from which data regarding the variation in the heating rate was obtained using an in-house written software called thermal view. The heating rate was plotted on excel charts.

4.5 Experiments with Signal Stress-II

This section talks about experiments consisting of signal stress caused due to the change in the duty cycle and also due to change in the frequency of chip usage. Codes were stored both on flash memory and SRAM so that when delay was caused SRAM should not be used instead code should run on flash for the time we want to cause the delay. Four different sets of codes were used to change the frequency of data in and out of the SRAM. Each set of code consisted of one code on SRAM and one code on flash.

The code on SRAM runs for different duration for each set of code and thus gives the change in duty cycle of SRAM. Similarly code spent different time on flash before jumping on to SRAM which gave the variation in frequency of chip usage.

The time spent on either of the chip was mentioned in ratio of SRAM: flash which means the ratio of time, spent on SRAM in comparison to that on flash. For the first code this ratio was 20:1 that means code was running 20 times more on SRAM than on flash. For the second code these ratios was 3:1 and still code was running on SRAM for longer duration than on flash. For the third code the ratio was 1:1 that is equal time spent on SRAM and on flash. For the last and the fourth code this ratio is 1:3 that is code on the flash was running 3 times more in comparison to the one on SRAM. The function of each code is separately mentioned in APPENDIX A. Table 4.2 shows the test matrix based on the above description.

It can be noticed that time spent on SRAM was decreasing as we moved from code 1 to code 4 and thus its heating rate as well.

Testing was done on 40 chips, out of which two-third were used to develop Neural Net model and one- third for evaluating accuracy of the model. Number of trials was reduced from 5 to 2 for every chip while running each set of code. The time spent between the trials was also reduced as the external conditions in the room were stable. Again specific care was taken to keep the chip at the same position for every trial to avoid human intervention error.

The design, test set-up and procedure followed for the experiments were similar to that of Signal Stress-I.

Table 4.2 Test matrix based on the different sets of codes

Number of Chips	**Code used on SRAM and Flash**	**Ratio of time spent**
40	Code set 9: SRAM more-Flash same	20:1
	Code set 10: SRAM 200k-Flash same	3:1
	Code set 11: SRAM same-Flash same	1:1
	Code set 12: SRAM same-Flash 150k	1:3

.

4.6 Experiments with Voltage Stress

In this experiment we stressed two data pins simultaneously at varying voltages. Several sets of chips were stressed for before finally arriving at the conclusion as to how many chips needed to be stressed and how? During the course of the experiments several things were noted. Few of them are summarized below.

4.6.1 Procedure for Stressing

1. 10 chips were placed on the breadboard. Data pins 2, 3 and address pin 4 were stressed simultaneously as shown in Figure 4.2.
2. Each chip was stressed with the voltage starting from 5.5V and stressed for 5 minutes. Once stressed this chip was tested if it was still working or not. If it was working then voltage was increased by 0.25 to 5.75 V and the chip was stressed for 5 minutes again. The whole procedure was repeated till the chip failed.

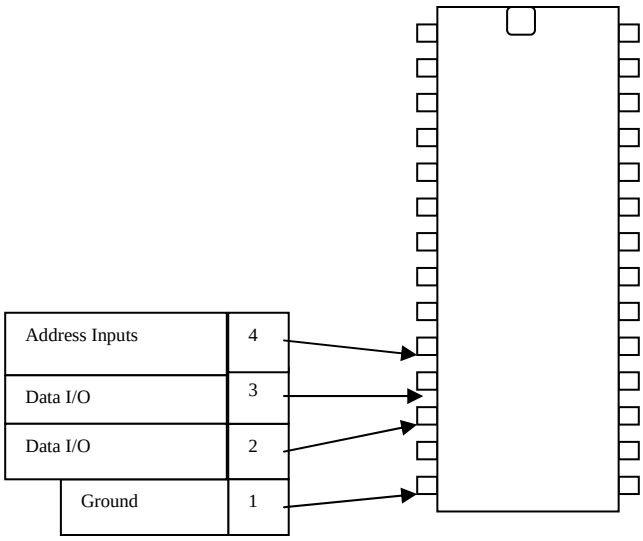

Figure 4.2 SRAM and the pins stressed.

3. From the experiments highest voltage at which chip can be stressed was considered to be 6.75 V with high probability of chip failure if it was stressed for 5 minutes.
4. The stress level was divided into four different categories 6V, 6.25V, 6.5V and 6.75V and each category consisted of 10 chips each. In total, we had 40 chips that were tested for 4 stress levels as shown in Table 4.3.

Table 4.3 Test matrix for the experiment based on the different stress levels used.

Number of chips	Stress level Used
1st set- 10 chips	6 V
2nd set- 10 chips	6.25 V
3rd set- 10 chips	6.5 V
4th set- 10 chips	6.75 V

4.6.2 Procedure for Imaging

1. For starting the experiment chip was placed on a connector (1) on the board and the board was kept under the IR camera inside the box. The other end of the connector was soldered to second connector (2), which was outside the box on the breadboard. The reason for this arrangement was that when we stressed the pins of the connector outside the box it sends the same voltage to the corresponding pins on the chips. So we can stress the chip while scanning it under IR camera by applying voltage on corresponding pins of the connector (2) outside the chamber.
2. Once setup was ready the connector outside the enclosure was stressed with 6V in such a way that it will stress the corresponding pins 2, 3 and 4. 2 and 3 were data pins whereas 4 was the address pin. Figure 4.2 shows the stressed pins on SRAM. The chip was stressed till its temperature starts increasing drastically. At the same time IR camera was turned on to take the scans every 7 seconds. The temperature determined the scanning time and the scanning was usually stopped whenever temperature reached around 350◦F.
3. Usually heating starts around 20 minutes or so for 6V whereas it took just 8 mins or so for temperature to increase when stressed at 6.25V, 6.5V and 6.75V. Once all the chips were scanned, thermal view software was used to obtain the data from the images. This data was plotted in the excel sheets to see the difference in the heating

rate of the stressed chips. The heating rate data obtained from the first four images in a scan were used as an input to the Back Propagation algorithm in Neural Networks.

4. We had 40 scans in total, 10 scans each for individual stress level equal to the number of chips for each stress level. Out of these 40 scans 28 scans or two-third was used to train the neural net and 12 scans or one-third were used for the testing purposes. MSE (mean square error) value was the factor defining the accuracy and the efficiency of the Neural Network method.

CHAPTER V
RESULTS

5.1 Introduction

This chapter describes all the experiment results obtained from infrared imaging over the chip, while it was stressed. The heating rate data was plotted in the Excel sheet and the graphs are shown for various set of experiments. This heating rate data was then used to train Neural Network to build a model based on the training set and the testing set used. MSE (Mean Square Error) was considered as the parameter to define efficiency of particular model. Thus MSE is shown for various topologies and using various training functions based on Back propagation algorithm.

The chapter consists of three sections. First section consists of the results from the signal stress-I, second from section-II. Finally third section consists of the results from voltage stress.

Heating rate data obtained using infrared camera was extracted using thermal view software. Excel charts were then used to plot the heating rate graphs. These graphs gave the visual representation of the heating rate curves for different stress levels. On these heating rate data statistical analysis was done to find out if the heating rate belong to different classes because then only it was possible to build efficient Neural Network model. Using heating rate data Neural Network model was build. As previously said out of the heating rate from all 40 chips two third was used to train the model and remaining one third was used to test the model. Details of the procedure are given in the subsequent sections.

5.2 Results from Signal Stress-I

5.2.1 Thermal Profiles

For every chip, average heating rate was obtained for both the chip and die area on chip using four different stress levels. Figure 5.1 shows the chip area and die area on a chip while imaging.

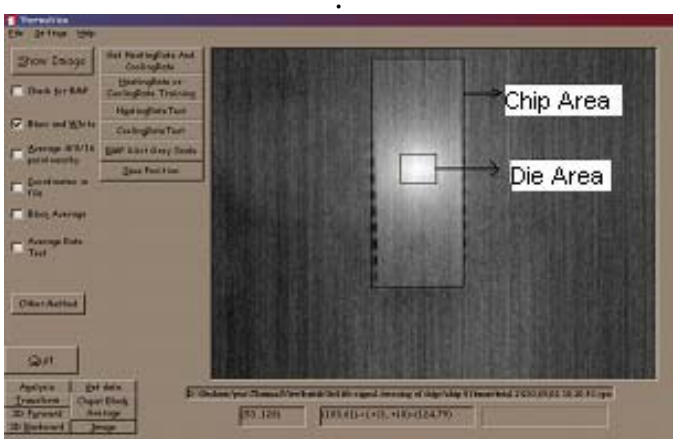

Figure 5.1 Chip area and the die area using Thermal View.

Figure 5.2 shows the average heating rate trend for the chips using heating rate for the die area. Average heating rate for the codes with NOPs was pretty similar and was significantly higher than the heating rate for the codes with NOPs. Among the codes with NOPs heating rate was higher for the code in which each memory address was increased by 1.

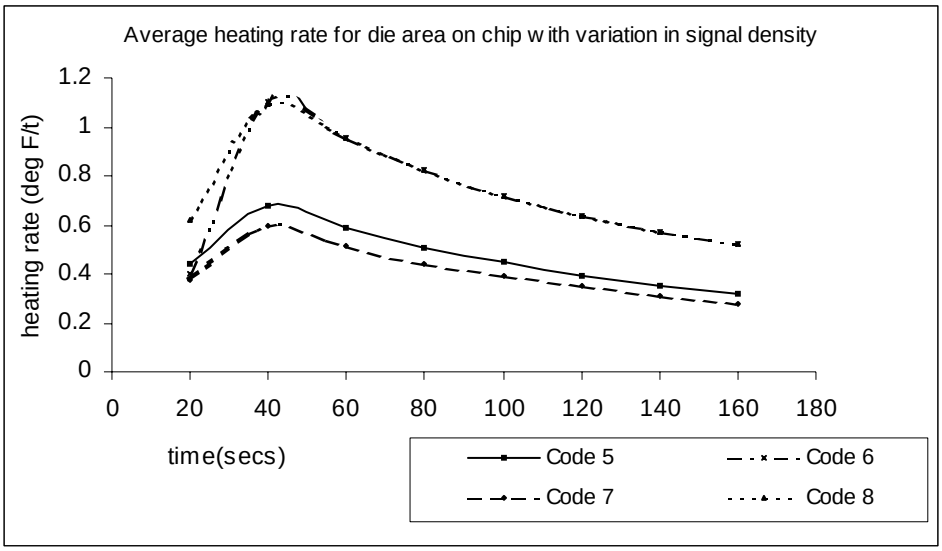

Figure 5.2 Variation in heating rate for die area on chips for signal stress-I.

5.2.2 Statistical Analysis Results

Heating rate graphs in Excel showed that average heating rate differs for each code mimicking various stress levels. But to prove it definitely, statistical *f-test* using STATMOST software was done. If the critical *f-value* is higher than the *f-value* from the data then it's difficult to differentiate between the data into different classes. But if *f-value* from the data is higher than critical *f-value*, it means that it is possible to differentiate data into different classes.

F-test results from the analysis showed that the critical *f-value* was much smaller than the *f-value* from data thus it was possible to clearly differentiate between the heating rate data from various stress levels. Table 5.1 shows the *F-test* results obtained.

Table 5.1 F-test results for SD-I die area**.**

***F- Test* results for SD – I for die area**		
Column Name	**Mean**	**Standard Deviation**
Code 5	3.0165	0.6756
Code 6	4.5626	0.4825
Code 7	2.6622	0.3570
Code 8	4.8448	0.4887
f-value for confidence interval 95%		**153.6855**
Critical *f-value* (0.05,3)		**2.6732**

5.3 Model Development Approach for Signal Stress-I

In this section complete methodology regarding neural net is described. Basic 3-2-1 network is shown in Figure 5.3 consisting of 3 input nodes, 2 hidden nodes and one output node. Neural net model is more or less like brain having millions of neurons and hence the name.

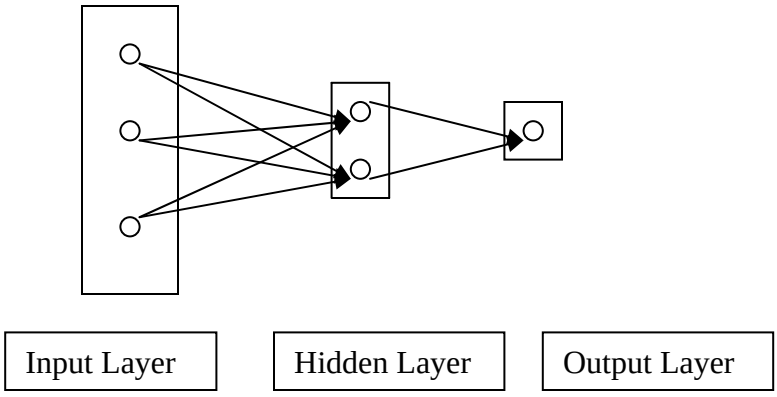

Figure 5.3 3-2-1 topology of Neural Network prediction model.

The underlying premise behind neural net methodology was the training of the network using input data based on some primary assumptions regarding the choice of network, number of nodes, layers, and training functions used. Repeated tests can be performed in order to obtain the best network. Neural Net is capable of complex modeling using large number of parameters while adjusting the values of the weights associate between elements (nodes) in order to reduce the error.

Each NN consist of three layers based on their precedence. First layer is called the input layer and the last one as output layer while all the layers in between are termed as hidden layers. Each layer consists of several nodes, which act as neurons (analogy to brain). These nodes link to other nodes in subsequent and the preceding layer. These links (synapses analogy to brain) have individual weights, which determine the strength of particular connection. For our case we had one input layer with 3 input nodes connected to 2 nodes in the first hidden layer which in turn are connected to 1 node in the out put layer.

Two-third of the data was separated from the experimental result that was used for evaluation or training purpose of NN whereas the rest of one-third was used for testing the NN. Data was fed through the input nodes, which propagated towards the end to give an output based on the training function used. This output was compared with the desired output and weights and biases were adjusted automatically in order to bring the output result close to desired out put as much as possible. Finally degree of accuracy of the results was compared after evaluating MSE. The process was over if error was either zero, close to prescribed value or the output couldn’t be improved further. Back propagation algorithm is used for this work because of its advantages to lead to minimum error rate using non-linear modeling faster than other algorithms.

The model development approach consist of three parts

- *Principle analysis dealt* with screening the noise and identifying possible primary classes.
- *Network Structure formulation* dealt with process of deciding about the number of layers and number of nodes in each layer.
- *Parameter setting determination* involved, setting the training function, learning rate, MSE, number of iterations or epochs.

5.3.1 Principle Analysis

There is no precise method to decide about the primary classes for the input data to the NN. Thus according to the rule of thumb we took four classes based on four stress levels. For both Signal stress-I and signal stress–II we had four stress levels based on the different frequencies for running the codes and different duty cycles on SRAM. Like wise there were four classes of out put values based on the stress levels.

As NN is highly data driven thus analysis was done over various different tabulated heating rate data obtained from Infrared imaging. For both signal stresses average heating rate was chosen as the correct representation due to smooth variation rather than highly erratic variation as obtained for the other heating rates. The heating rate unit was taken as ° F/t. From the heating rate data it was observed that the heating rate was highest for snapshot 2^{nd} and decreased later on. First snapshot was meant for synchronization and thus was erased before any kind of modeling.

For modeling purpose the data from snap shot #2 was taken as input node I, data from snapshot #3 was taken as input node II and the sum of heating rate data for next four snap shots #4, 5, 6, 7 were taken as input node III. This would maximize the usage of thermal profile of each stressed chips.

5.3.2 Network Structure Formulation

The best combination for making model was chosen to be the one described above. Based on that combination number of input nodes were determined to be three,

though again necessarily it was not hard and fast rule. It was just matter of convenience. Similarly numbers of hidden layers were taken to be one followed by an output layer. As for number of nodes two topologies were used, one having two nodes in hidden layer (3-2-1 topology) and another with three nodes in the hidden layer (3-3-1 topology). Again MSE was used to determine which topology worked best.

5.3.3 Parameter Setting Determination

Various training functions and learning algorithm were used as described in NN matlab toolbox [48]. Various trials were used to determine the epochs, MSE and learning rate parameter. Table 5.2 shows various learning functions can be applied for Back propagation method.

Table 5.2 Various learning functions for back propagation method.

Training Functions	**Learning Algorithm associated** [49]
TrainRP	Resilient Back Propagation
TrainOSS	One step secant method
TrainSCG	Scaled conjugate gradient algorithm
TrainGDA	Gradient descent with adaptive learning rate
TrainLM	Levenberg- Marquardt algorithm
TrainGD	Basic gradient descent
TrainGDM	Gradient descent with momentum
TrainCGB	Powell- Beale conjugate gradient algorithm
TrainCGP	Polak- Ribiere conjugate gradient algorithm
TrainCGF	Fletcher- Reeves conjugate gradient algorithm
TrainGDX	Adaptive learning rate algorithm

5.4 Matlab Results for Signal Stress-I

Once its verified that heating rate from different stress levels belong to separate classes, NN model was developed based on the average heating rate data from both chip and die area. The NN model was trained using the data and then compared with the output to check the error. Based on the error both weights and biases were adjusted. This procedure goes on till error goes to zero or close to preset value.

Table 5.3 Matlab results obtained using different training functions for die area on chip and using signal stress –I.

Training function	**Network Used 3-2-1**		**Network Used 3-3-1**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	0.0126	3937	0.0127	7891
TrainOSS	0.0127	903	0.0128	2339
TrainSCG	0.0127	53	0.0122	208
TrainGDA	0.0127	238593	0.0127	315226
TrainLM	0.0116	17	0.0120	23
TrainGD	0.0131	1200000	0.0107	1012226
TrainGDM	0.0131	1200000	0.0132	1200000
TrainCGB	0.0128	25	0.0128	51
TrainCGP	0.0128	43	0.0129	73
TrainCGF	0.0128	63	0.0129	73
TrainGDX	0.0125	64232	0.0114	32437
Average MSE	**0.0128**		**0.0124**	

Table 5.4 Matlab results obtained using different training functions for chip area and using signal stress –I.

Training function	**Network Used 3-2-1**		**Network Used 3-3-1**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	0.0713	53701	0.0726	24226
TrainOSS	0.0666	14926	0.0825	9209
TrainSCG	0.0672	1141	0.1319	2601
TrainGDA	0.0712	1200000	0.0786	1200000
TrainLM	0.0744	20010	0.0952	7958
TrainGD	0.0640	1200000	0.0677	1200000
TrainGDM	0.0656	1200000	0.0646	1200000
TrainCGB	0.0666	536	0.0634	63
TrainCGP	0.0638	364	0.0658	142
TrainCGF	0.0640	369	0.0630	80
TrainGDX	0.0665	411324	0.0819	555933
Average MSE	**0.0674**		**0.0788**	

5.5 Inferences for Signal Stress-I

The tables above gave the MSE using topologies 3-2-1 and 3-3-1 and different training functions.

- For different topologies different training function can yield least MSE. In the Table 5.3 for SD-I die area MSE for 3-2-1 topology was least for *TrainLM* whereas for 3-3-1 networks it was least for *TrainGD.*
- Similarly Table 5.4 shows that MSE for chip area using 3-2-1 topology and 3-3-1 topology was least for *TrainCGP* and *TrainCGF* respectively.

- For die area and chip area 3-3-1 topology gave the lowest error rate.
- The function, which takes the least iterations, does not necessarily yield the lowest error rate.
- In general training functions requiring more number of iterations for particular topology (3-2-1) continue requiring greater number of iterations for increased number of nodes in topology (3-3-1). The reason might be that the sample to parameter ratio (weights, bias) was higher for 3-2-1 resulting in better results.
- Lowest error rate for die area was 0.0107 obtained for *TrainGD* using 3-3-1 topology and for chip area it was 0.0630 for *TrainCGF* using 3-3-1 topology.
- NN results showed that the MSE for die area was several times smaller than that of the chip area. Even the lowest average error rate 0.0123 was for die area with 3-3-1 topology. Difference between error rates from all the training functions was 0.0025, which was infact significantly low.

5.6 Results from Signal Stress-II

Similar to results in signal stress-I here too, the subsections consist of results from heating rate, statistical results and finally generating Neural Network model. For varying stress levels, different code sets were mentioned which are already described in the experiment section in the previous chapter.

5.6.1 Results from Thermal Profile

Figure 5.4 shows the heating rate trend for various code sets. It can be seen from the graph that the average heating rate for set code–9 is highest as the code spent 20 times more time on SRAM as compared to FLASH. This average heating rate curve is followed by code set 10, 11 and 12 depending on decrease in time spent on SRAM. For code set-9 heating rate was 1.2 °F/t followed by 0.8, 0.6 and 0.4 °F/t for code set-10, code set-11 and code set-12 respectively.

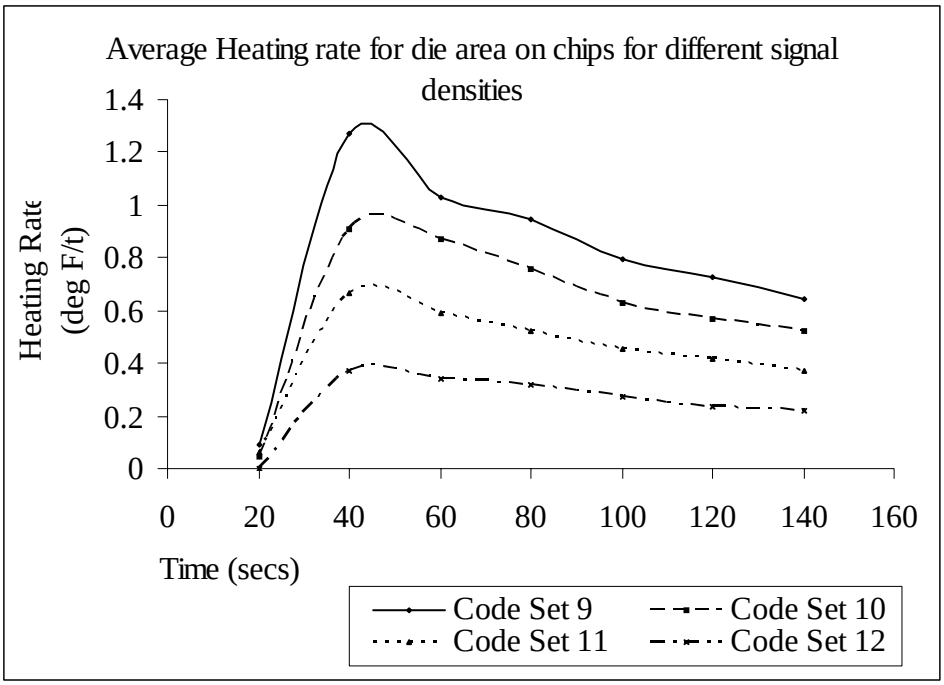

Figure 5.4 Variation in heating rate for die area on chips for signal stress-II.

5.6.2 Statistical Results

Though excel graph shows the variation in heating rate from one code to another or one stress level to another but to prove it definitely again *F-test* was done. The results of *F-test* are shown in Table 5.5. Again results from the *F-test* showed that it is possible to develop a NN model because statistically, heating rate from different stress levels belong to different classes.

Table 5.5 F-test results for SD-II die area.

***F-test* results for SD – II for die area**		
Column Name	**Mean**	**Standard Deviation**
Code Set-5	1.8022	0.3754
Code Set-6	3.0590	0.5430
Code Set-7	4.2717	0.6018
Code Set-8	5.5031	0.5512
f-value for confidence interval 95%		**357.9142**
Critical *f-value* (0.05,3)		**2.6641**

5.7 Matlab Results for Signal Stress-II

Heating rate data from excel files was used to develop training set data (consisting of two third of heating rate data) and testing set data (from remaining one third of heating rate data) for NN model. Heating rate data from first scan was discarded. Training and testing data files were made from rest of the scans. The NN model was based on Back propagation algorithm using various training functions. Three layered networks 3-2-1 and 3-3-1 were used.

Two methods were used for developing NN model, based on the heating rate for die area to verify the best suited method for arranging heating rate data among nodes.

In method Ist- Heating rate from second snapshot was taken Input-I, heating rate from third snap shot was taken as Input-II and finally heating rate from snapshot 4th was taken as Input-III.

For method IInd- Heating rate data from second scan was used as input- I, heating rate data from third scan was used as input- II and finally sum of heating rate data from remaining four scans were used as an input- III. The comparisons for results from the NN model are shown in Table 5.6 below.

Table 5.6 Matlab results obtained using network 3-2-1 and two different methods of training the data.

Training function	**Method Ist**	**Method IInd**
	MSE	**MSE**
TrainRP	0.1127	0.0923
TrainOSS	0.1110	0.0935
TrainSCG	0.1129	0.0935
TrainGDA	0.1446	0.0937
TrainLM	0.1132	0.0951
TrainGD	0.1115	0.0980
TrainGDM	0.1113	0.0981
TrainCGB	0.1197	0.1034
TrainCGP	0.1207	0.1052
TrainCGF	0.1225	0.1065
TrainGDX	0.1110	0.094
Average MSE	**0.1174**	**0.0976**

5.8 Inferences for Signal Stress-II

From the NN results it can be seen that the average error rate was smaller for method II (0.0976). Thus for further analysis and development of model for both die area and chip area, data was arranged according to method II.

Again NN model was developed and results were obtained using average heating rate data from chip area and also from die area. The results from the training functions for die area and chip area are given below in Table 5.7 and Table 5.8 for 3-2-1 and 3-3-1 topologies.

Table 5.7 Neural Network results for SD-II stress for die area.

Training function	**Network Used 3-2-1 (die-SD-II)**		**Network Used 3-3-1 (die-SD-II)**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	**0.0923**	45903	**0.0529**	87011
TrainOSS	0.0935	31461	0.0555	65083
TrainSCG	0.0935	2756	0.0555	5543.
TrainGDA	0.0937	1200000	0.0738	1200000
TrainLM	0.0951	24088	0.0973	1200000
TrainGD	0.0980	1200000	0.0977	1200000
TrainGDM	0.0981	1200000	0.0958	1200000
TrainCGB	0.1034	435	0.0945	901
TrainCGP	0.1052	335	0.0539	2497
TrainCGF	0.1065	104	0.0936	444
TrainGDX	0.0941	1200000	0.0554	1200000
Average MSE	**0.0976**		**0.0751**	
High- Low	**0.0142**		**0.0448**	

Table 5.8 Neural Network results for SD-II stress for chip area.

Training function	**Network Used 3-2-1 (chip-SD-II)**		**Network Used 3-3-1 (chip-SD-II)**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	0.1585	1200000	0.1629	1200000
TrainOSS	0.147	15437	**0.1323**	28546
TrainSCG	0.1459	891	0.1324	3849
TrainGDA	0.1469	1200000	0.1357	1200000
TrainLM	0.1472	92	0.1439	4241
TrainGD	**0.1469**	1200000	0.1571	1200000
TrainGDM	**0.1469**	1200000	0.1450	1200000
TrainCGB	0.1471	696	0.1328	1370
TrainCGP	0.147	999	0.1444	1101
TrainCGF	0.147	1070	0.1442	1296
TrainGDX	0.147	267544	0.1556	1200000
Average MSE	**0.1479**		**0.1442**	
High- Low	**0.0116**		**0.0306**	

- In Table 5.7 for die area MSE was least for *TrainRP* for 3-2-1 and 3-3-1 topology.
- For results obtained from heating rate of chip area in Table 5.8 MSE for 3-2-1 topology and 3-3-1 topology was least for *TrainGD*- *TrainGDM* and *TrainOSS* respectively.
- For both chip and die area lowest error rate is for 3-3-1 topology.

- Lowest error rate for die area was 0.0529 obtained for *TrainRP* using 3-3-1 topology, similar to SD-I and for chip area least MSE this time was 0.1323 for *TrainOSS* using 3-3-1 topology.

NN results showed that the MSE for die area was several times smaller than that of the chip area. The lowest average error rate 0.0751 is for die area with 3-3-1 topology and the difference between the error rate using best topology from all the training functions was just 0.0448 which was still low.

5.9 Results from the Voltage Stress

On similar cue as in signal stress results, here too heating rate was obtained for two positions chip area and die area. Apart from that heating rate curves are shown for different stress levels in excel graphs. From those heating rate data Neural Net model is developed based on the heating rate from first four snapshots. One of the main differences between NN model for voltage stress and the signal stress lies in the fact that for the signal stresses the heating rate from first snapshot was neglected or discarded but that was not the case for voltage stress.

5.9.1 Results of Thermal Profile

For every chip average heating rate was obtained for both the chip area and the die area on chip using four different stress levels. Figure 5.5 shows the chip area and die area on a chip while imaging.

Figure 5.6 shows the average heating rate for all the chips for one particular stress level whereas Figure 5.7 shows the average heating rate comparison between different stress levels after taking average of heating rate for all chips.

- Heating rate was highest when voltage stress was 6.75 V.
- Also heating rate was highest for the first snap and then it started decreasing.
- Fewer images were needed as stress level increased because higher the stress level faster was the temperature rise up to likely temperature of failure.

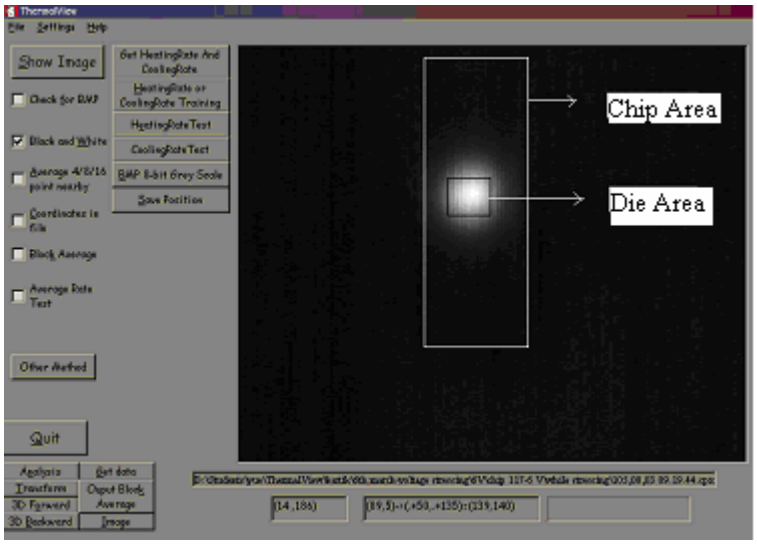

Figure 5.5 Die area and chip area while imaging.

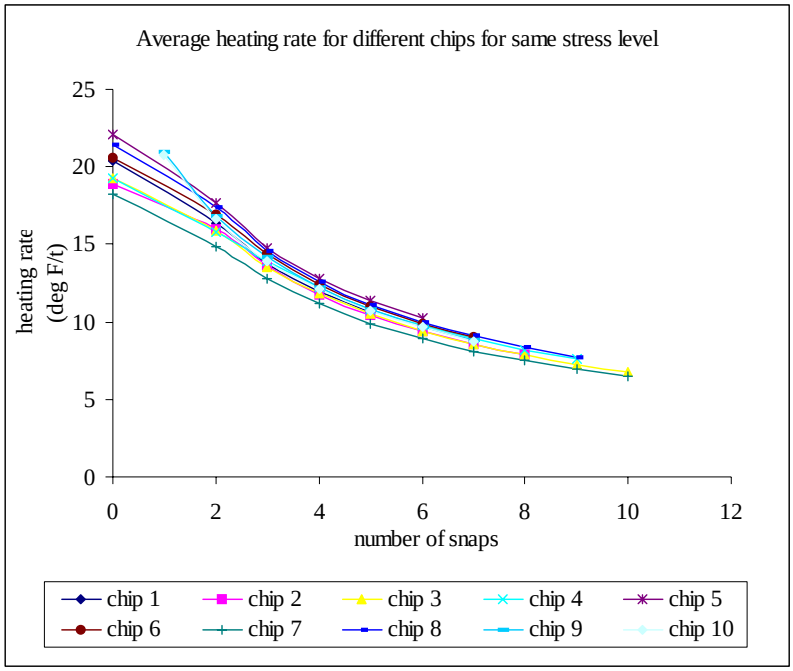

Figure 5.6 Average heating rate trend for different chips for same stress level.

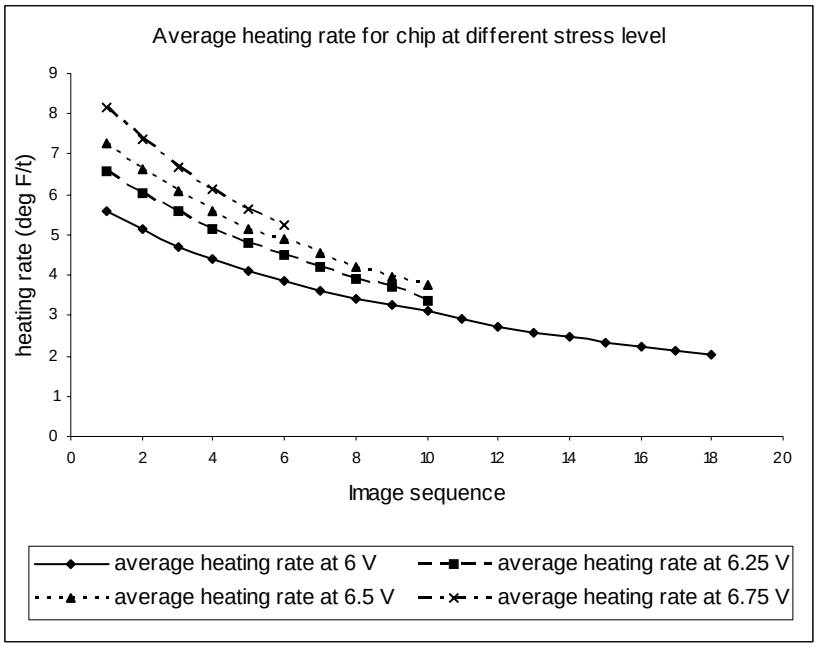

Figure 5.7 Average heating rate trends for different stresses.

5.10 Model Development Approach for Voltage Stress

Model development approach was similar to the one mentioned in signal stress –I and signal stress-II in previous sections. The only difference was in the arrangement of data for modeling purpose. For modeling purpose data from snap shot #1 was taken as input node I, sum of data from snapshot # 2, 3 and 4 were taken as input node II and the sum of data from snapshot #1, 2, 3 and 4 were taken as input node III. This would maximize the usage of the stressed chip thermal profile.

5.11 Matlab Results for Voltage Stress

Tables 5.9 and 5.10 below shows the Matlab results for die area and chip areas respectively from the heating rates obtained during voltage overstressing. The inferences drawn are shown in the next section.

Table 5.9 Neural Network results for voltage stress for die area.

Training function	**Network Used 3-2-1 (die-VS)**		**Network Used 3-3-1 (die-VS)**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	0.0342	1200000	0.0343	1200000
TrainOSS	0.0355	7191	0.0370	15817
TrainSCG	0.0355	263	0.0356	342
TrainGDA	0.0360	1200000	0.0353	1200000
TrainLM	0.0409	6519	0.0409	5937
TrainGD	0.0364	1200000	0.0364	1200000
TrainGDM	0.0364	1200000	0.0372	1200000
TrainCGB	0.0356	94	0.0346	140
TrainCGP	0.0357	70	0.0352	102
TrainCGF	0.0355	120	0.0355	162
TrainGDX	0.0355	79371	0.0373	1118810
Average MSE	**0.0361**		**0.0363**	
High- Low	**0.0067**		**0.0066**	

Table 5.10 Neural Network results for voltage stress for chip area.

Training function	**Network Used 3-2-1 (Voltage stress- chip area)**		**Network Used 3-3-1 (Voltage stress- chip area)**	
	MSE	**Epochs**	**MSE**	**Epochs**
TrainRP	0.0470	1200000	0.0472	1200000
TrainOSS	0.0451	3104	0.1297	32194
TrainSCG	0.0451	120	0.0451	246
TrainGDA	**0.0450**	1200000	**0.0449**	1200000
TrainGD	0.0454	1200000	0.0454	1200000
TrainGDM	0.0454	1200000	0.0468	1200000
TrainCGB	0.0452	72	0.0454	95
TrainCGP	0.0451	456919	0.0460	113
TrainCGF	0.0451	102	0.0451	108
TrainGDX	0.0452	484587	0.519	1200000
Average MSE	**0.0454**		**0.1015**	
High- Low	**0.0020**		**0.0848**	

5.12 Inferences for Voltage Stress

1. For different topologies different training function can yield least MSE. In the Table 5.9 for die area MSE for 3-2-1 and 3-3-1 topology was least for *TrainRP* (0.0342 and 0.0343).
2. Similarly Table 5.10 shows that MSE for chip area using 3-2-1 topology and 3-3-1 topology was least for *TrainGDA* (0.0450 and 0.0449).
3. Based on the heating rate data any of the topology can yield lowest error rate. For die area 3-2-1 topology gave the lowest error rate whereas 3-3-1 gave lowest error rate for chip area.

4. The function, which takes the least iterations, does not necessarily yield the lowest error rate.
5. In general training functions requiring more number of iterations for particular topology (3-2-1) continue requiring greater number of iterations for increased number of nodes in topology (3-3-1). The reason might be that the sample to parameter ratio (weights, bias) was higher for 3-2-1 resulting in better results.
6. Lowest error rate for die area was 0.0342 obtained for *TrainRP* using 3-2-1 topology and for chip area it was 0.0449 for *TrainGDA* using 3-3-1 topology.
7. NN results showed that the MSE for die area was smaller than that of the chip area. The lowest average error rate (0.0361) was for die area with 3-2-1 topology. Difference between error rates from all the training functions was 0.0067, which was infact significantly low.

CHAPTER VI
MODEL TOLERANCE

6.1 Introduction

Following chapter deals with the noise tolerance of the neural model developed based on the heating rate from the experimental results. Noise can be caused when data is dispersed about its mean, more than it should be. For dispersing the data standard deviation was increased keeping the mean constant. It was assumed that when data is dispersed then there is overlapping between two adjacent heating rate data distribution proportional to inducing noise. Explanation for whole procedure is given in detail in the following sections.

Here the point which is necessary to make is the evaluation of noise as overlapping ratio. Increasing standard deviation of the data can increase overlapping ratio. With increase in overlapping ratio between the data, noise would also increase. Neural network model was made based on the different standard deviations. It was assumed that the MSE from the neural model developed using the deviated data would also change (if the solution were already saturated). Thus effect of inducing noise can be observed by comparing MSE with overlap ratio.

The chapter is divided into three sections based on the three different experiments conducted. Two of these experiments were done using signal stresses and one of the experiments was done using voltage overstressing.

6.2 Generating Data for Signal Stress-I

Once neural model was made based on the experimental heating rate data sets, more data sets were generated using statistical software for comparison of degree of sensitivity to the presence of noise in the data set. The method used was as follows:

Numbers of data points (heating rate data) for each stress level from experiments were 28 for training set and 12 for testing set (40 in all). From these data points curve fitting was done and more data points (400 for training file and 100 for testing file) were

generated satisfying the curve fit. As a result a large number of data points were created with the same standard deviation as the original data set (termed as base case or category-A). For studying effect of noise, heating rate data corresponding to input to node 1 and node 2 of neural network were taken. This input was termed as Input –I and Input-II, and each one of these inputs consist of four stress levels. Now the deviation was increased further by varying Input-I and Input-II in order to increase the noise within the model. The percentage of the noise was measured by equivalent parameter called overlap ratio. More the overlap ratio greater was the noise in the data. Overlap ratio is defined as the ratio of overlap area between heating rate PDFs from data of Input-I and Input-II to the individual area under each PDFs for Input –I and Input-II. This area is shown in Figure 6.1. It is assumed that difficulty for NN model to distinguish between the data points increases with increase in overlapping. This difficulty for NN model can cause increase in MSE for the model.

Standard deviation increases overlap and thus increases both overlap ratio and MSE. This overlap ratio was then compared with MSE obtained from NN model based on that particular deviated data set. A good noise tolerant model is the one in which the increase in MSE is relatively low as compared to increase in overlap ratio.

The model was based on the heating rate data, which yields least MSE among the topologies. In all three data sets were generated using best fit. First category (category-A) consisted of data set generated from original data set from experiments. Second in which deviation of the data set was increased 3 times (category-B) and the third in which deviation was increased by 6 times (category-C). In short the steps followed for generating and testing the model for tolerance are:

- Determine the classes (Input-I and Input-II) and perform distribution-fitting technique of existing heating rate data.
- Generate more data by increasing the standard deviation of the data set.
- Calculate overlap ratio and run NN model based on the changed data set.
- Compare the results to check the noise tolerance for the model.

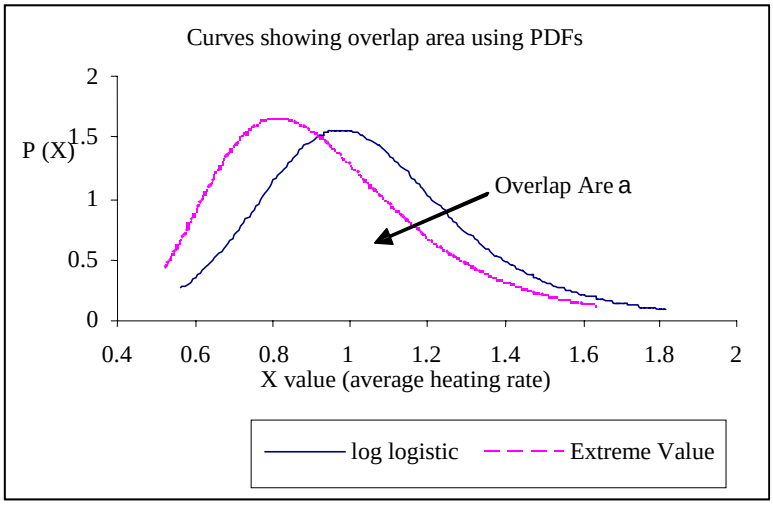

Figure 6.1 Overlap area of two distributions.

-X is the heating rate.

-P (X) is the probability density of variable X.

6.3 Increase in Standard Deviation and Calculation of Overlap Area

This section shows how standard deviation was increased and overlap ratio was calculated. As already mentioned, 400 data sets were generated from evaluation data set and 100 from testing data sets for each stress level and three inputs used for three nodes of neural network, using Best-fit software. These generated data sets follow the same trend as original heating rate obtained from experiments for each stress level and hence represent increased heating rate data set for each stress level.

For noise amplification in data, input-I and input-II were taken which represent input to the node-I and node –II of the Neural Network respectively. Each input consisted of heating rate from four different stress levels. Heating rate from input-I was compared with corresponding heating rate from input-II for the same stress level.

Thus we calculated increase in overlap area with increase in the standard deviation for all these four stress levels. The entire procedure is shown using an example

to calculate standard deviation and overlap ratio. The heating rate used was obtained from input-I and input-II for stress level 2. The increase in standard deviation was kept to be three times more than the generated data sets for this stress level.

The generated data for stress level 2 follows the probability density distribution (PDF) as given by *log logistic* and *extreme value distribution* in Input-I and Input-II respectively. The curves in the Figure 6.2 show probability distribution function for both heating rates with 95 % confidence interval.

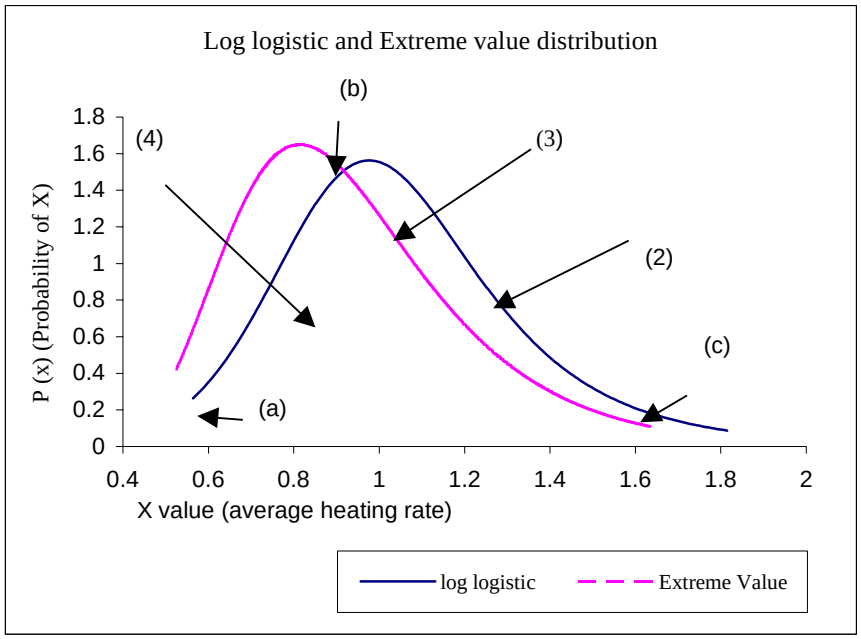

Figure 6.2 Probability density distributions with 95% confidence interval**.**

6.3.1 Increasing Standard Deviation

Taking log logistic distribution first; mean, variance and standard deviation for log logistic distribution are given as:

$Mean = \beta * \theta * cosec\ \theta + \gamma$ 6.2

$Variance = \beta^2 * \theta * (2 * cosec\ (2\theta) - \theta * cosec^2 \theta)$ 6.3

Standard Deviation = Sq. Root (Variance) 6.4

Log logistic curve is determined with three parameters (γ,β,α) where $\alpha = (\pi/\theta)$. Best- fit generated the initial data set of 400 data, from experimental results thus we had values for all these parameters as well as mean, variance and standard deviation for the initial generated data set. Other data sets were generated with increase in the deviation of this initial generated data set.

Mean, variance and standard deviation for initial generated data set were given as:

Mean = 1.0643
Variance = 0.0115
Standard Deviation = 0.1072

$(\gamma, \beta, \alpha) = (0.6806, 0.3701, 6.7915)$

Standard deviation was increased by three times for next set of generated data set. Thus new values while keeping mean constant were given as:

Mean = 1.0643
Variance = 0.10335
Standard Deviation = 0.3215

These parameters were used to solve equations 6.2 and 6.3 to get new (γ,β,α) given in equation 6.5. As there were two equations thus only two unknowns can be obtained. Therefore we took α to be constant for these calculations.

$(\gamma, \beta, \alpha) = (0.0869, 1.1106, 6.7915)$ 6.5

Now equations to be solved in such way so that mean does not change but variance change according to standard deviation. Curves obtained by new (γ,β,α) is shown in Figure 6.3 and represented by (2).

Now taking PDF for corresponding heating rate in input-II, which follows extreme value distribution and determined by parameters *(a, b)*. Mean, variance and standard deviation were given by:

$Mean = a + 0.577*b$ 6.6

$Variance = (\pi^2*b^2)/6$ 6.7

Standard Deviation = Sq. Root (Variance) 6.8

Mean variance, standard deviation and initial value of parameters for the initial PDF of the generated data set were given as:

Mean = 0.9432
Variance = 0.0091
Standard Deviation = 0.0954

(a, b) = (0.9003, 0.0744)

Again keeping mean, constant and varying standard deviation by three times we get new values for mean, variance and standard deviation given as:

Mean = 0.9432
Variance = 0.0818
Standard Deviation = 0.2861

From these new values we solved equations 6.6 and 6.7 to get the new values of *(a, b)* given in 6.9. In this way we generated a new curve with standard deviation three times more than the initial generated curve from experimental data. This curve is shown as (3) in the Figure 6.3.

(a, b) = (0.8145, 0.2231) 6.9

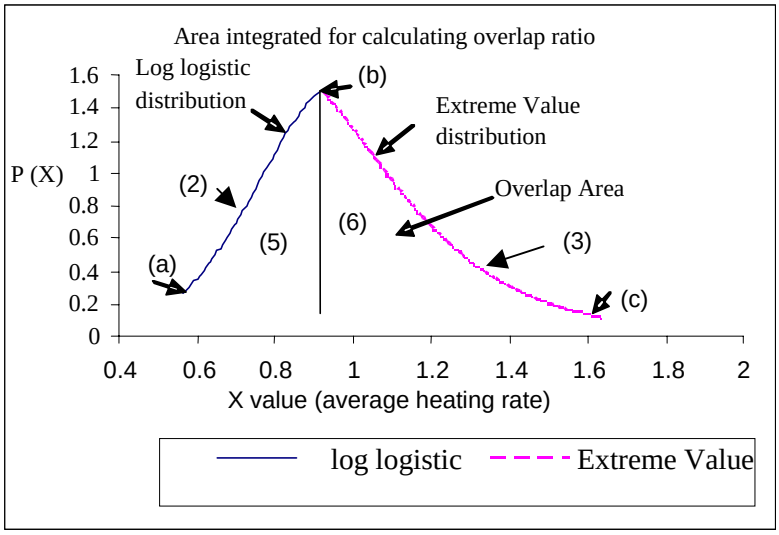

Figure 6.3 Area needed to be integrated for overlap ratio.

6.3.2 Overlap Area

To calculate the overlap ratio the overlap region (4) was divided into two region (5) and (6) as shown in Figure 6.3.

Point ‘a’ is minimum X value for PDF (2).

Point ‘c’ is maximum X value for PDF (3).

Point ‘b’ is intersection point for both PDFs.

Points ‘a’ and ‘c’ were obtained when PDF’s were drawn using Best-fit software. For calculating ‘b’, PDF’s of two curves were compared. At this point both curves gave the same value. MS excel was used to get ‘b’.

Once all three points are obtained, Matlab was used to integrate the PDF’s over the range ‘a’ to ‘b’, for PDF from curve (2) and from ‘b’ to ‘c’, for PDF from curve (3). This way overlap area (4) under the distribution was calculated quantitatively. Finally for particular standard deviation this overlap area was obtained for all four-stress levels.

The percentage increase in area or combined overlap ratio, due to increase in standard deviation while keeping mean constant, was calculated by taking ratio of change in overall area to original area under the curves. The original area corresponds to the area under distribution of initial generated data set obtained from experimental heating rate data.

6.4 Noise Tolerance Results for Signal Stress-I

Also for comparison between overlap ratio or noise with results from Neural Network, Matlab results were obtained for all three generated data sets (category A, B and C) and overlap ratio was calculated using excel. Table 6.1 gives the overlap ratio for base case and for categories B and C having deviations of three times and six times respectively more than the base case. Results are shown in the Table 6.2 and 6.3 below and the inferences regarding noise tolerance of the model are drawn based on the results.

Table 6.1 Overlap percentage between classes (input-I and input-II).

Category	**Content**	**Class**	**Overlap**
A	Base Case	Input-I and Input-II	**0.2137**
B	Standard Deviation- 3 times	Input-I and Input-II	**0.3771**
C	Standard Deviation- 6 times	Input-I and Input-II	**0.4022**

Table 6.2 Average error rate for SD-I die area.

Category	**A**	**B**	**C**
Function	**MSE**	**MSE**	**MSE**
TrainRP	0.0151	0.0503	0.3749
TrainOSS	0.0160	0.0267	0.3704
TrainGDA	0.0231	0.0364	0.3665
TrainLM	0.0269	0.0203	0.3505
TrainGD	0.0296	0.0372	0.3682
TrainGDM	0.0249	0.0425	0.3691
TrainCGB	0.0128	0.0154	0.3703
TrainCGP	0.0128	0.0283	0.3564
TrainCGF	0.0126	0.0307	0.3718
High-Low	**0.0170**	**0.0349**	**0.0213**
Average MSE	**0.0193**	**0.0319**	**0.3664**
Percentage Overlap (I and II)	**0.2137**	**0.3771**	**0.4022**

Table 6.3 Number of iterations needed for SD-I die area.

Category	**A**	**B**	**C**
Function	**Iterations**	**Iterations**	**Iterations**
TrainRP	1200000	8490	1200000
TrainOSS	19080	907	846
TrainGDA	1200000	45989	68562
TrainLM	5016	10	5
TrainGD	1200000	336982	291218
TrainGDM	1200000	301415	289133
TrainCGB	49	58	86
TrainCGP	1200000	211	120
TrainCGF	113	100	114
Average Iterations	**669362**	**77129**	**205564**

6.5 Inferences for Signal Stress-I

- For all training functions the error rate increased as the standard deviation for each class increased. That is there was increase in MSE between category A-B and B-C.
- Neural Net model was noise tolerant upto a certain overlapping ratio. If the overlap was increased further MSE error increased drastically but until overlap ratio was less than that maximum limit, increase in MSE was pretty low. For e.g.: though for above generated data overlap ratio increased to 21.47 % from 37.71 % but the change in MSE error was just around 2% (0.0193 – 0.0319). But when it was increased to 40 % for category C, there was sudden increase in the MSE error. Thus it can be said that model was noise tolerant even when data was overlapping until 38 % (approx.). Again it was observed that training functions like *TrainCGF*, *TrainCGB* and *TrainCGP* converged faster than any other training function.

6.6 Generating Data for Signal Stress-II

Again new data set were generated based on the method described in section A of signal stress. Category A was generated from best-fit curve satisfying the experimental data. In Category A deviation of the data sets was same as that of the original set. Category B was generated with three times of deviation of original data set that is base case and Category C was generated with six times of deviation of base case.

6.7 Noise Tolerance Results for Signal Stress-II

Matlab results were obtained for all three generated data sets and overlap ratio was calculated using excel. Table 6.4 gives the overlap ratio for base case and for categories B and C having deviations of three times and six times respectively more than the base case. Results are shown in the Table 6.5 and 6.6 below and the inferences regarding noise tolerance of the model are drawn based on the results.

Table 6.4 Overlap percentage between classes (input-I and input-II).

Category	**Content**	**Class**	**Overlap**
A	Base Case	Input-I and Input-II	**0.2926**
B	Standard Deviation- 3 times	Input-I and Input-II	**0.4092**
C	Standard Deviation- 6 times	Input-I and Input-II	**0.4528**

Table 6.5 Average error rate for signal density-II die area.

Category	**A**	**B**	**C**
Function	**MSE**	**MSE**	**MSE**
TrainRP	0.1223	0.1013	0.1104
TrainOSS	0.1212	0.1111	0.1134
TrainSCG	0.1239	0.0994	0.1208
TrainGDA	0.1343	0.1176	0.1297
TrainLM	0.1374	0.1097	0.1121
TrainGD	0.1152	0.0974	0.0980
TrainGDM	0.1313	0.0970	0.1185
TrainCGB	0.1226	0.1087	0.1084
TrainCGP	0.1067	0.1102	0.1075
TrainCGF	0.1068	0.1087	0.1127
TrainGDX	0.1300	0.1074	0.1184
High-Low	**0.0233**	**0.0206**	**0.0317**
Average MSE	**0.1228**	**0.1063**	**0.1136**
Percentage Overlap (I and II)	**0.2926**	**0.4092**	**0.4528**

Table 6.6 Iterations needed for signal density-II die area.

Category	**A**	**B**	**C**
Function	**Iterations Needed**	**Iterations Needed**	**Iterations Needed**
TrainRP	1200000	1200000	1200000
TrainOSS	106258	45138	40466
TrainSCG	66275	2455	8071
TrainGDA	1200000	1200000	1200000
TrainLM	1200000	127221	33340
TrainGD	1200000	1200000	1200000

Table 6.6 continued

Category	**A**	**B**	**C**
Function	**Iterations Needed**	**Iterations Needed**	**Iterations Needed**
TrainGDM	1200000	1200000	1200000
TrainCGB	854	236	228
TrainCGP	567	305	348
TrainCGF	561	385	1110
TrainGDX	1200000	12000000	1039061
Average Iterations	**670410**	**561431**	**538420**

6.8 Inferences for Signal Stress-II

- Interesting fact worth to note over here was that the error rate in the model was already saturated. Though the overlap ratio increased but error rate for deviated data set was smaller than the base case.
- Neural Net model was noise tolerant. Though for above generated data overlap ratio increased from 29.26 % to 40.92% from Category A to B but error rate decreased from 12.28% to10.63%. Similarly moving from category B to C overlap ratio increased from 40.92% to 45.28% but there was just slight increase in error rate from 10.63%to 11.36%. Again it was observed that training functions like *TrainCGF*, *TrainCGB* and *TrainCGP* converged faster than any other training functions.
- The number of iterations also had no relationship with MSE or the overlap ratio. Least MSE can have higher or lower number of iterations than other categories.

6.9 Generating Data for Voltage Stress

For voltage stress also the basic premise for development of generated data sets and Neural Network based on that, was similar to that of signal stress experiments. In Category A deviation of the data sets was same as that of the original set. But unlike for signal stress, Category B was generated after adding +6 deviation to original data set that was base case and Category C was generated after adding +9 deviation to original data set**.** This was done because the difference between the heating rate in Input-I and Input-II was pretty large, thus unless deviation was increased +6 or +9 more than original case, heating rate data would not overlap.

6.10 Noise Tolerance Results for Voltage Stress

Matlab results were obtained for all three generated data sets and overlap ratio was calculated using excel**.** Table 6.7 gives the overlap ratio for base case and for categories B and C having deviations of six times and nine times respectively more than the base case. Results are shown in the Tables 6.8 and 6.9 below and the inferences regarding noise tolerance of the model are drawn based on the results.

Table 6.7 Overlap percentage between classes (input-I and input-II).

Category	**Content**	**Class**	**Overlap**
A	Base Case	Input-I and Input-II	No overlap Region*
B	Standard Deviation +6	Input-I and Input-II	0.1128
C	Standard Deviation + 9	Input-I and Input-II	0.1493
* Based on 95 % Confidence Interval			

Table 6.8 Deviation results from voltage stress chip area.

Category	**A**	**B**	**C**
Function	**MSE**	**MSE**	**MSE**
TrainRP	0.0389	0.0421	0.0412
TrainOSS	0.0373	0.0446	0.0394
TrainSCG	0.0372	0.0488	0.0408
TrainGDA	0.0385	0.0432	0.0405
TrainLM	0.0423	0.0450	0.0444
TrainGD	0.0411	0.0438	0.0403
TrainGDM	0.0411	0.0437	0.0403
TrainCGB	0.0374	0.0421	0.0425
TrainCGP	0.0354	0.0460	0.0401
TrainCGF	0.0374	0.0444	0.0397
TrainGDX	0.0373	0.0454	0.0394
High-Low	**0.0051**	**0.0067**	**0.005**
Average MSE	**0.0385**	**0.0445**	**0.0407**
***Percentage Overlap (I and II)**	**No overlap**	**0.1128**	**0.1493**
* Based on 95 % confidence interval			

Table 6.9 Number of iterations for voltage stress chip area**.**

Category	**A**	**B**	**C**
Function	**Iterations**	**Iterations**	**Iterations**
TrainRP	1200000	141434	1200000
TrainOSS	6959	17503	16777
TrainSCG	609	1549	966
TrainGDA	1200000	1200000	1200000
TrainLM	11078	1200000	2224
TrainGD	1200000	1200000	1200000
TrainGDM	1200000	1200000	1200000
TrainCGB	182	176	137
TrainCGP	497	732	298
TrainCGF	369	406	413
TrainGDX	231976	967499	315350
Average Iterations	**459243**	**539027**	**466924**

6.11 Inferences for Voltage Stress

- Generally with increase in deviation, MSE also increased. That is average error rate increased from category A to B (0.0380-0.0445). But once its saturated there was no further increase in error rate as observed from category B to C (0.0445-0.0407).
- Neural Net model was noise tolerant. Though for above generated data overlap ratio was increased to 11.28% in category B the increase in error rate was from 3.8% to 4.4%. Similarly moving from category B to C overlap ratio increased from 11.28% to 14.93% but error rate decreases to 4.04% due to saturation of overlap ratio. Again it was observed that training functions like *TrainCGF*, *TrainCGB* and *TrainCGP* converged faster than any other training function.

CHAPTER VII
GENERIC METHODOLOGY FOR STRESSING

7.1 Introduction

This chapter gives generic methodology to be followed for any other chip and board, for developing similar kind of stress level prediction model.

Test setup for any other board with any other chip will remain more or less same. Component to be studied should be removed from the board because

- It will be practically difficult to place whole board under camera.
- Also heating rate of one component will affect the heating rate of another component and also heating rate captured by the imaging device.

Thus component or chip under study should be kept under the infrared camera or imaging device without having any other component in its vicinity. For that cables and connectors can be used to connect the chip to its main board when it is removed and placed on separate board to study under infrared camera. The board with chip is kept under infrared camera inside a closed chamber to avoid any effect from surroundings.

Once this is done next step in the procedure is to stress the chip. If it is signal stress than parameter which is causing the variation in signal stress should be determined. If it's the voltage stress then preliminary experiments based on either the knowledge of chip architecture or hit and trial procedure should be adopted to find out which pins need to be stress to observe change in heating rate.

Until this point the steps for voltage stress and signal stress for all kind of experiments are same. But after this there exists some changes in the way experiment is done for both voltage and signal stress which is as follows:

7.2 Generic Methodology for Stressing

Based on the experiments Figure 7.1 represents the generic methodology for model based on signal stressing and voltage stressing, on different chips and boards.

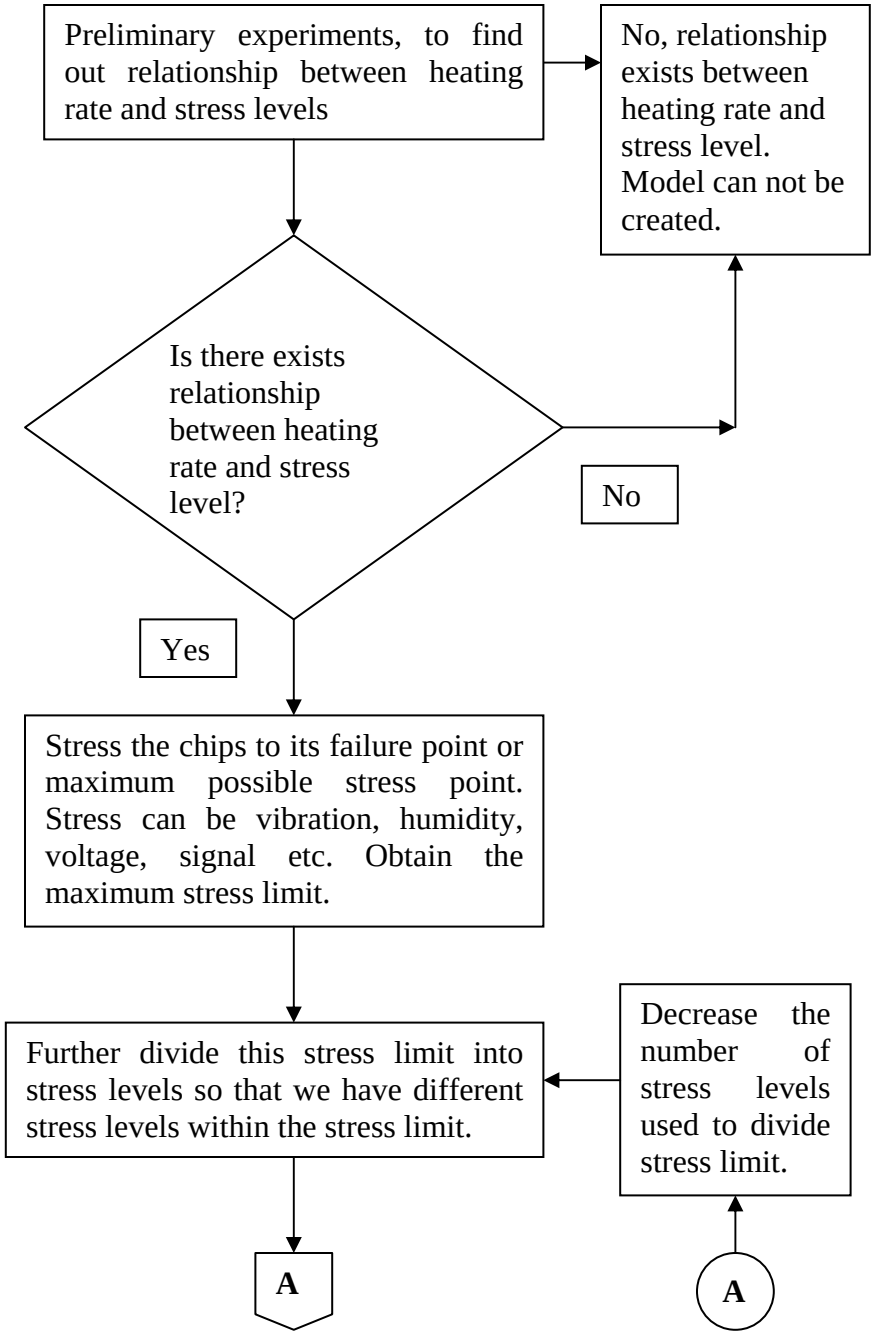

Figure 7.1 Generic methodology for building a stress prediction model**.**

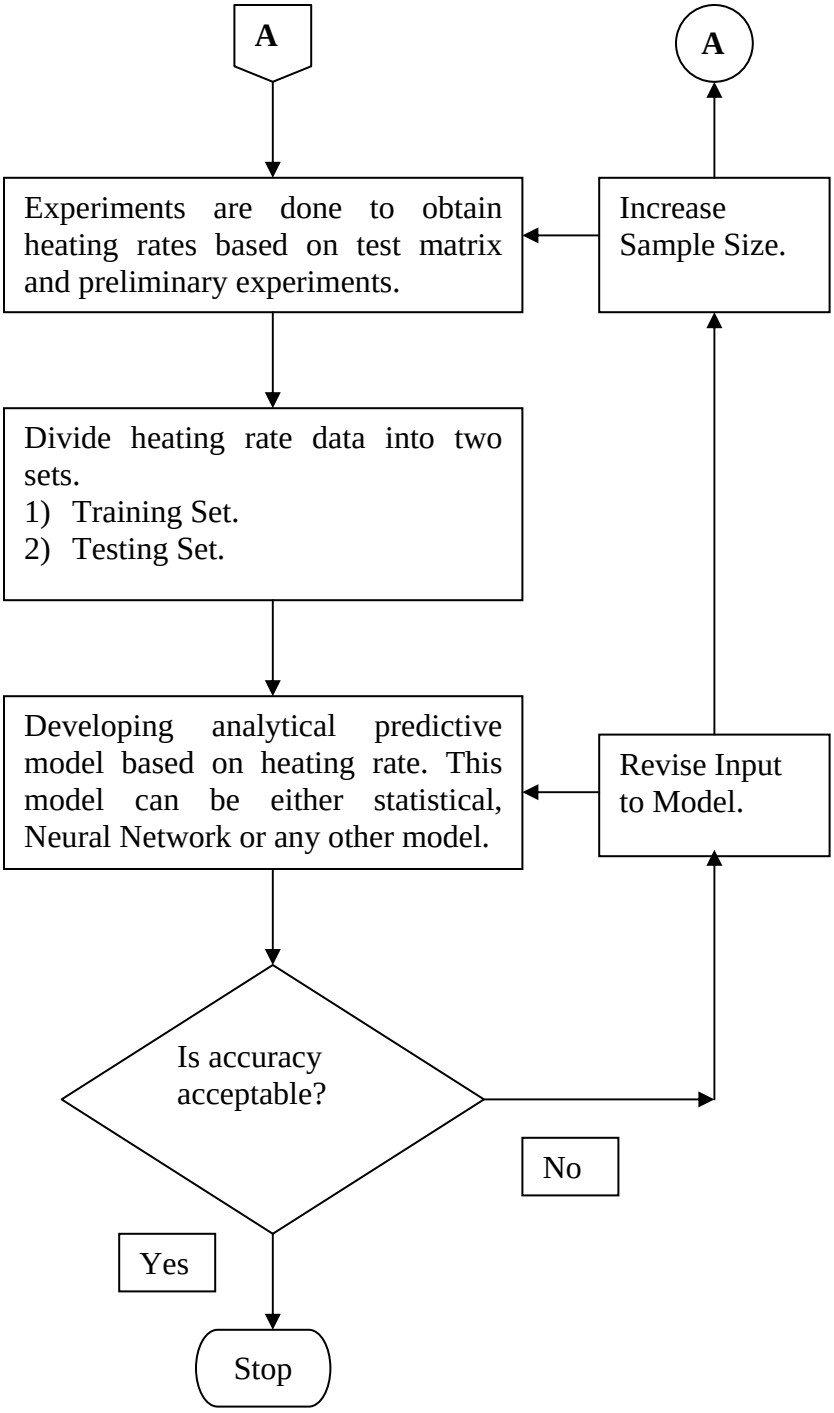

Figure 7.1 Continued

CHAPTER VIII
CONCLUSION AND FUTURE WORK

8.1 Introduction

The results from the tests are generic. As was stated earlier, the factors that determine the heating rate of the chip under test are current entering/exiting the chip, and its manufacturing method. If the chip is not CMOS for example, it should have higher heating rate when placed under the same conditions due to the fact that circuits are of the same make up and require a net larger voltage. Other factors, like changing the board chip is on, should play little or no roll in affecting the heating rate, as is seen in the tests in which the chip was placed on a completely different board simply to achieve an undisturbed heat measurement. Another factor that should not change results too significantly is the SRAM being tested. As long as it is CMOS, and the load of the code or the voltage stress is similar to that in the tests then the result would be comparable as well. This also holds true for testing a micro controller, though a micro controller will typically do much more work than a SRAM chip, and hence should heat up more, the results should still be proportional to the current load entering/leaving the chip.

For both voltage stress and the signal stress whole procedure involves designing experiments for stressing the chips. This is followed by obtaining heating rate using infrared camera, exploring the variance in heating rate data for different stress level using statistical tools, identifying the specific combination for heating rate which leads to significant difference in stress level. Finally that combination of data was used to develop NN model. The model was also tested for its noise tolerance and sensitivity.

Next two subsections give details of conclusions obtained from both kind of stresses that is signal stresses involving variation in duty cycle and frequency of chip usage, and voltage stress involving variation in operating voltage.

8.2 Conclusion from Signal Stressing

In this thesis work a methodology for stress level prediction due to variation in duty cycles and frequency on electronic chip was studied. This work can be extended to

other chips as well where effect of variation of frequency and duty cycles is prominent such as microprocessors. Results obtained suggested that

- Average heating rate from die area gives better NN model than heating rate for signal stress.
- Error rate for NN model is independent of iterations and the learning algorithms used.
- During signal stressing though the maximum stress level was reached but chip did not fail. In order to fail the chip using signal stress we might need a chip working at very high signal frequency such as microprocessors.
- For signal stress-I wherein codes were stored on SRAM and NOPs were used in codes to increase the heating rate, lowest MSE is for *TrainGD* (0.0107) for die area and *TrainCGF* (0.0630) for chip area using 3-3-1 topology. Similarly for signal stress-II lowest error for die area was obtained for *TrainRP* (0.0529) and for chip area, *TrainOSS* (0.1323) gave lowest MSE again using 3-3-1 topology.
- This proves that model was quite efficient as the error rate for DIE area was always less than 10% for both stresses.
- From the noise tolerance results we observed that error rate increases with standard deviation. Then it might become stagnant or increase suddenly. But over a range of increase in overlap ratio the increase in MSE rate is relatively small. For signal stress-I overlap ratio of generated data increased to 37.71 % from 21.47 % but the change in MSE error was just around 2% (0.0193 – 0.0319). Similarly for signal stress-II NN model showed pretty good noise tolerance. Overlap ratio for generated data overlap ratio increased from 29.26 % to 40.92% from Category A to B but error rate decreased from 12.28% to10.63%. Similarly moving from category B to C overlap ratio increased from 40.92% to 45.28% but there was just slight increase in error rate from 10.63%to 11.36%.

Thus in all NN model developed using signal stresses is pretty efficient and this methodology can be extended to other electronic components as well where effect of

frequency change is more prominent such as micro controller processor or for chips which crunches lots of information in relatively small time.

8.3 Conclusion from Voltage Stressing

Similar work on voltage stress was also done in this thesis work and a methodology was studied for stress level prediction due to voltage stress. Results obtained suggested that:

- Any topology can yield best results. But the accuracy depends on the accuracy of data obtained during experiments.
- For die area MSE for 3-2-1 topology was least for *TrainRP* (0.0342). For chip area it was least for *TrainGDA* (0.0449) using 3-3-1 topology.
- Neural Net model was noise tolerant. Though for above generated data overlap ratio was increased to 11.28% in category B the increase in error rate was from 3.8% to 4.4%. Similarly moving from category B to C overlap ratio increased from 11.28% to 14.93% but error rate decreases to 4.04% due to saturation.

The most important conclusion made during the research was to propose the generic methodology for stress level predictions.

The conclusion made clearly justifies the research work we tried to accomplish in our problem statement which was to build a model for stress level existing in chips. As the error rate is pretty small and the accuracy for the results are high (>90%), generic methodology given earlier can be used to build a model for other electronic components as well.

This work does not end over here but can be further performed on various other electronic chips and components and accuracy of the results can be compared to other predictive methodologies existing. Some of the future work that can be undertaken is mentioned in the next section as well.

8.4 Future Work

The work done in this research can be further extended to other models and we can finally build a predictive model for whole PCB board itself. The future recommendations can be summarized in following points:

- Developing the same model for different chips such as micro controller where the effect of variation in frequency and duty cycles are significant.
- Increasing sample size for the experimental chips to get more reliable and better results.
- Scope of similar work for different kind of signal stresses that can be caused by changing the clock frequency or using an incompatible micro controller, which increases the rate of data transfer significantly higher than normal rate and thus causes stress in the chips.
- Using components working at very high signal frequency which might result in the failure of the chip.
- Comparing the results with those obtained from statistical methods or using finite element approach.
- The Neural Network model can be developed based on two output nodes instead of just one. The idea behind it is that, as there are four stress levels, they can be divided into four binary outputs 00, 01, 10, 11.

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APPENDIX A
CODES USED

Codes 1-4 are essentially the same, the main difference in the codes is the values of data being placed in RAM as well as possibly varying delays.

Code 1 is 1206.asm – this code is similar the one shown in the diagram below. It functions by activating one LED at a time across the range of 8 LED's. Each time the next LED is lit up in the pattern the program will move a hex number, in this case FF, to R1, this is followed by placing the value 00 into R1 repeatedly until the comparison statement is reached. At this point the program loops and repeats these steps.

Code 2 is 1206ram2.asm – this code is the same as the previous with a slight change. Once the program enters the loop where it moves decimal 255 into R1, it will continual to loop here forever. Instead of exiting the loop, when R0 = 255, the loop will reiterate just as if R0 were any other value.

Code 3 is 1206ram3.asm – this code is also similar to the first with a subtle change. It moves decimal 0 into the location of the data pointer followed by moving 255 into the same location. It then loops infinitely performing this action repeatedly.

Code 4 is 1.asm – this code is the one shown in the diagram below. It works the exact same as the first one though instead of alternating FF, 00 into the R1 register, it instead just places FF into it repeatedly. This program follows the steps of the diagram and the flow laid out in the first code.

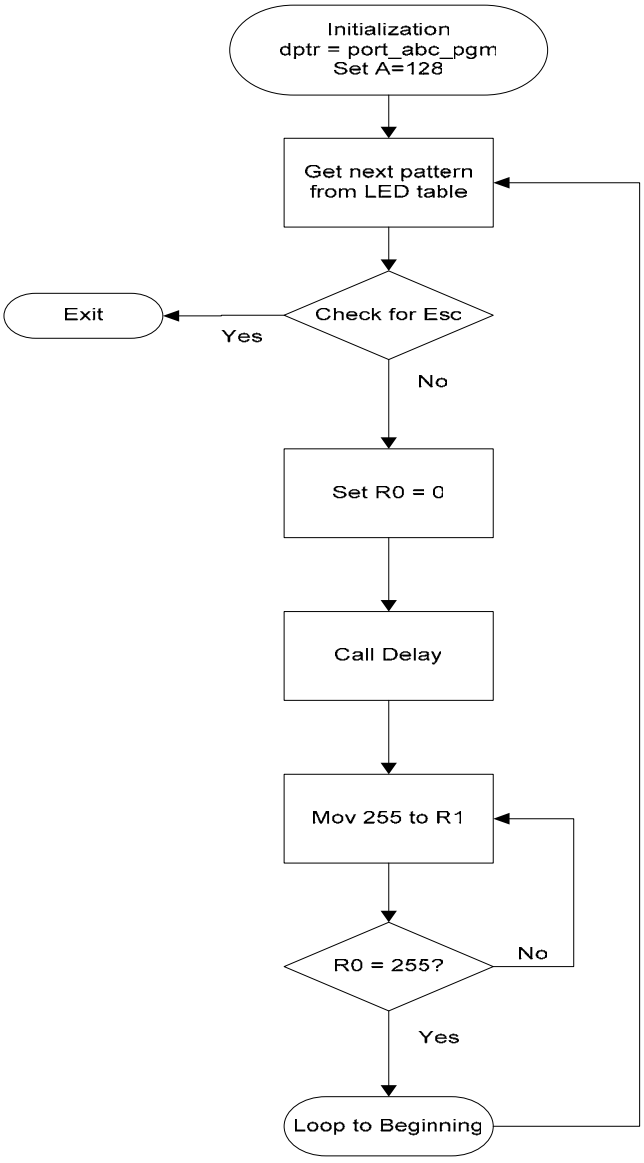

Figure A-1

Code 5-8 are used to both create a heat in the RAM but also to test the memory array of the chip for faults. The programs create a regularly visible data structure in the array which can easily be scanned to find faults in the memory.

Code 5 is IncrementsRAM.asm – this code worked by entering a loop where a pointer was placed at location 2100 and this was filled with hex value 00, the program then entered a loop where it went through each location in RAM and filled it with a value one higher than the location before it.

Code 6 is IncrementsRAMwdelay.asm – this program was the same except there was a delay built in which was filled with “nop” instructions. This came in at the end of the larger loop, and other than the delay performed the exact function of the previous code.

Code 7 is Zerosnfswesc.asm– this program was structured the same as the previous two programs but instead of placing incremental values in RAM it alternated by filling the RAM with all zeros, followed by filling the RAM with all FF’s

Code 8 is Zerosnfswescndelay.asm – this program is the same as the previous program but included a delay. This is analogous to the relationship of codes 6 and 7 in that it is the same code with the same function, but with a delay thrown in to allow the nop’s to increase the heating rate.

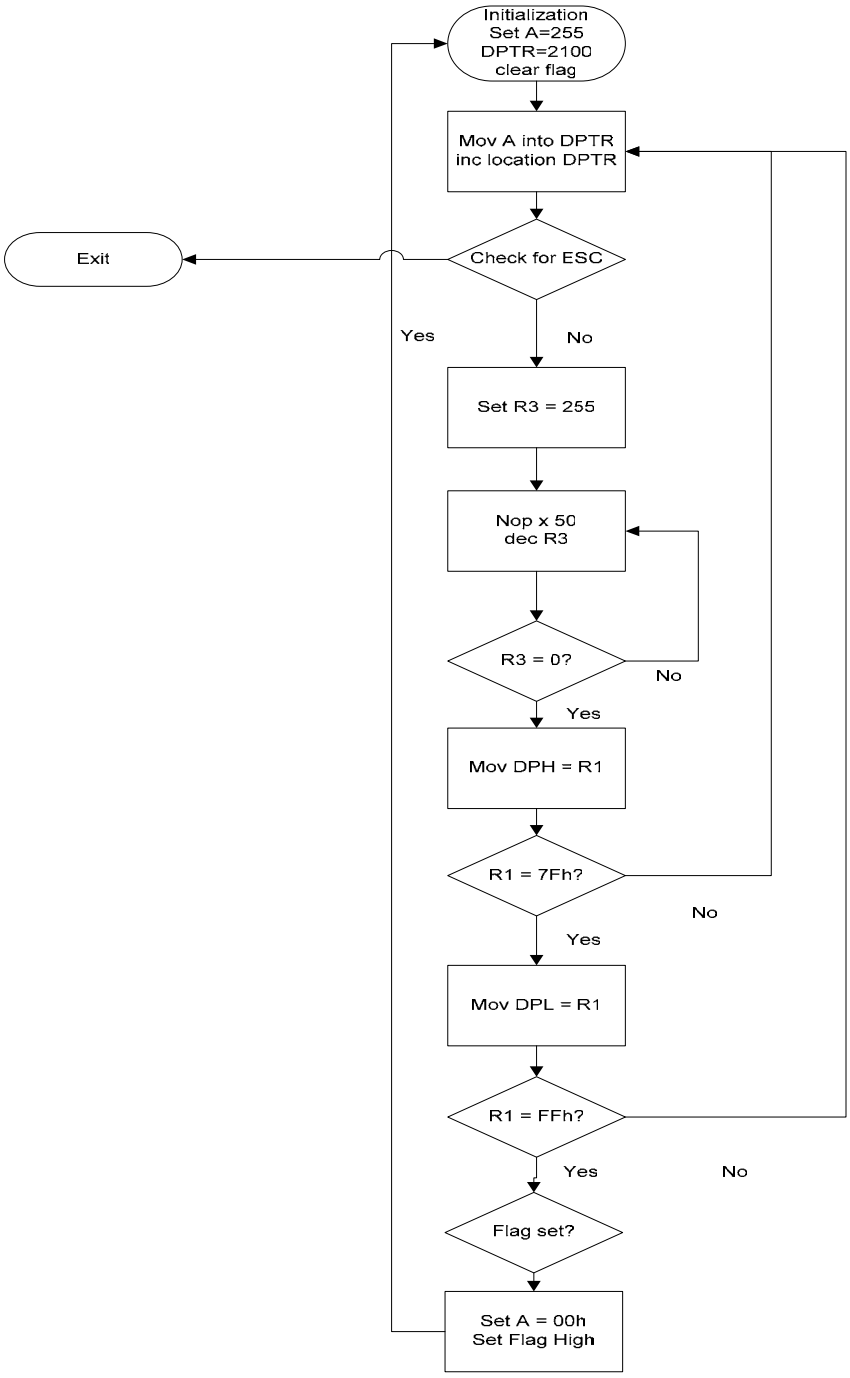
Initialization
Set A=255
DPTR=2100
clear flag
Mov A into DPTR
inc location DPTR
Exit
Check for ESC
Yes
No
Set R3 = 255
Nop x 50
dec R3
R3 = 0?
No
Yes
Mov DPH = R1
R1 = 7Fh?
No
Yes
Mov DPL = R1
R1 = FFh?
Yes
No
Flag set?
Set A = 00h
Set Flag High

Figure A-2

For code 9-12, there were two codes run, one in FLASH, one in SRAM. This structure allowed the user to have a greater control in how much time the code spent in use on either the SRAM chip of the FLASH. The programs functioned by starting one, which at termination, called the other program, and visa versa. This lead to a loop between the two programs that was easy to manipulate to get the test data desired.

Code 9 is SRAM_More & FLASH_Same - this code followed the diagram below with the exception that the delay loop on the SRAM has been increased so that the microcontroller spends 20times more time interfacing with the SRAM than the FLASH.

Code 10 is SRAM200k & FLASH_Same – this code was designed with a loop structure that left the SRAM getting used three times as often as the FLASH.

Code 11 is SRAM_Same & FLASH_Same – this code gives a 1:1 ratio of use between the SRAM and FLASH.

Code 12 is SRAM_Same & FLASH150k – this code function in the same manner as the previous codes and provides a 1:3 ratio of time for the microcontroller to spend on the FLASH instead of on the SRAM.

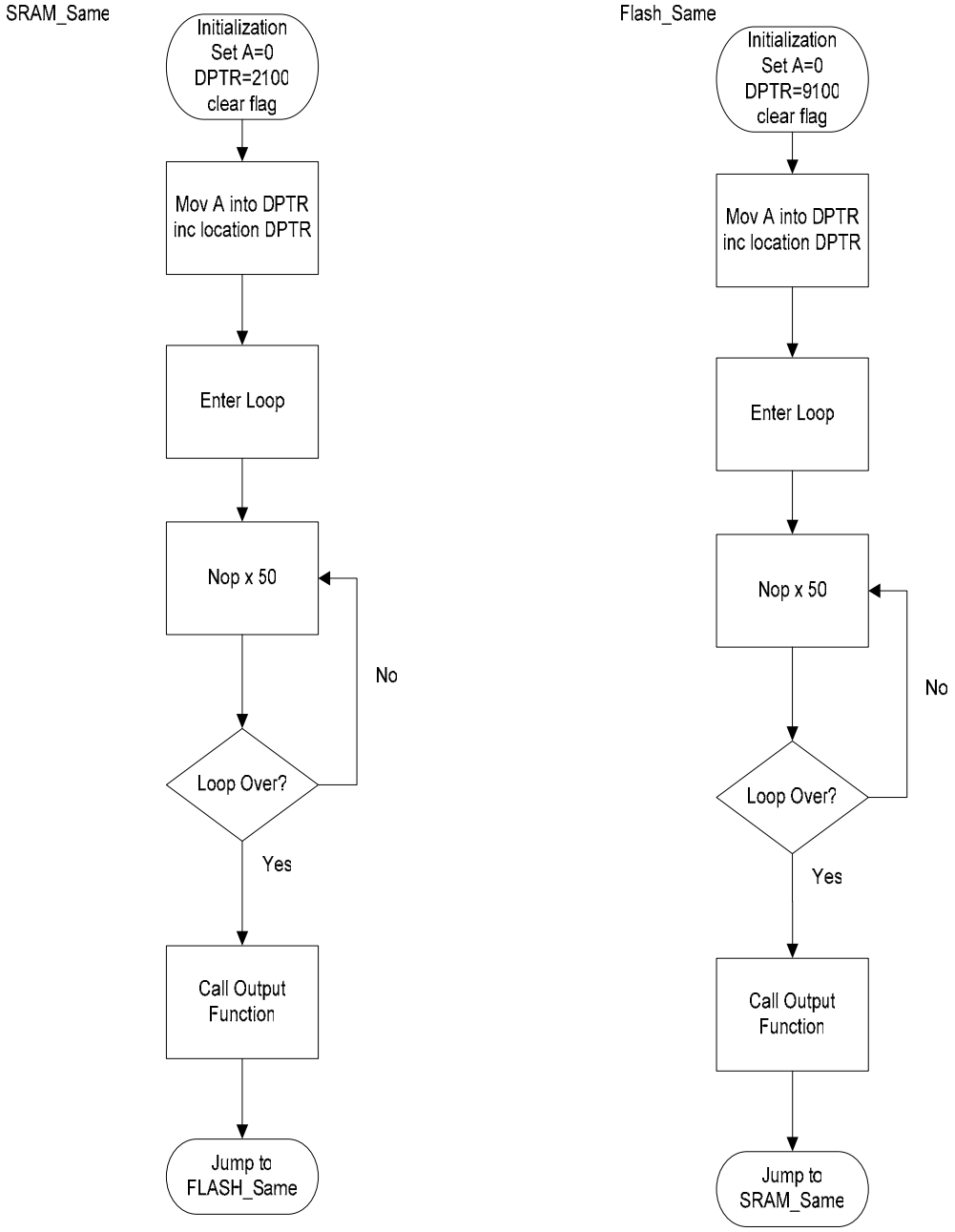
SRAM_Same
Initialization
Set A=0
DPTR=2100
clear flag
Mov A into DPTR
inc location DPTR
Enter Loop
Nop x 50
No
Loop Over?
Yes
Call Output
Function
Jump to
FLASH_Same
Flash_Same
Initialization
Set A=0
DPTR=9100
clear flag
Mov A into DPTR
inc location DPTR
Enter Loop
Nop x 50
No
Loop Over?
Yes
Call Output
Function
Jump to
SRAM_Same

Figure A-3

APPENDIX B

VB CODE USED FOR SYNCHRONIZATION

```
Option Explicit
Dim Darray() As String
Private Sub cmdSend_Click()
Dim buffer, Newline, SFile, FileName As String
Dim i As Integer
'*********************************************************************
SFile = "1.txt"            'Change "    " to a new file
'*********************************************************************
If txtFileName.Text = "" And SFile = "" Then
  MsgBox ("Pls enter a file name")
End If

If txtFileName <> "" Then SFile = txtFileName.Text

FileName = AppendFileToPath(App.Path, SFile)
' Buffer to hold input string
Dim Instring As String
' Use COM1.
MSComm1.CommPort = 1
' 1200 baud, no parity, 8 data, and 1 stop bit.
MSComm1.Settings = "1200,N,8,1"
' Tell the control to read entire buffer when Input
' is used.
MSComm1.InputLen = 0
' Open the port.
MSComm1.PortOpen = True
' Send the attention command to the modem.
```

```
'*****************************************************
' Send the attention command to the modem.

MSComm1.Output = Chr$(13) ' Ensure that
' MSComm1.Output = "ATV1Q0" & Chr$(13) ' Ensure that

' the modem responds with "OK".
' Wait for data to come back to the serial port.

Text1.Text = ""

Do
   DoEvents
   buffer = buffer & MSComm1.Input
   Text1.Text = buffer
Loop Until InStr(buffer, "PAULMON2 Loc:2000 >") '& vbCrLf)

' InStr(buffer, "2000 >" & vbCrLf)
' Read the "OK" response data in the serial port.
' Close the serial port.
'*****************************************************

On Error GoTo FileError
Open FileName For Input As #1


Text1.Text = ""
```

```
i = 0

Do Until EOF(1)

  i = i + 1
  ReDim Preserve Darray(i)
  Input #1, Darray(i)
     Text1.Text = Text1.Text & Darray(i) & vbNewLine
  MSComm1.Settings = "1200,N,8,1"
  MSComm1.Output = Darray(i)

Loop

 Dim PauseTime, Start, Finish, TotalTime
 PauseTime = 1   ' Set duration.
 Start = Timer   ' Set start time.
 Do While Timer < Start + PauseTime
   DoEvents   ' Yield to other processes.
 Loop

buffer = ""

Do
  DoEvents
  buffer = MSComm1.Input
  Text1.Text = Text1.Text & buffer
Loop Until buffer = ""

 PauseTime = 0.5   ' Set duration.
```

```
    Start = Timer   ' Set start time.
    Do While Timer < Start + PauseTime
      DoEvents   ' Yield to other processes.
    Loop

  MSComm1.Output = "r"

  buffer = ""

  Do
    DoEvents
    buffer = MSComm1.Input
    Text1.Text = Text1.Text & buffer
  Loop Until buffer = ""

    PauseTime = 0.5   ' Set duration.
    Start = Timer   ' Set start time.
    Do While Timer < Start + PauseTime
      DoEvents   ' Yield to other processes.
    Loop

  MSComm1.Output = "a"
    Exit Sub

FileError:
   MsgBox "File Error!"
MSComm1.PortOpen = False
End Sub
```

```
' Purpose: This function safely appends the passed file name
'          to the passed path by making sure the last character
'          in the path contains a "\"
Private Function AppendFileToPath(ByVal Path As String, _
    ByVal File As String) As String
    If Path = "" Then    ' the path is at the root
        AppendFileToPath = File
    ElseIf Right(Path, 1) = "\" Then
        AppendFileToPath = Path & File
    Else
        AppendFileToPath = Path & "\" & File
    End If
End Function

Private Sub cmdExit_Click()

   'MSComm1.Output = ""
   If MSComm1.PortOpen = True Then MSComm1.PortOpen = False
   Unload Me
   Exit Sub
End Sub

Private Sub Form_Load()
Dim i As Integer
i = 0
'txtFileName.SetFocus
End Sub
```

VITA

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