A CAPACITOR-LESS LOW DROP-OUT VOLTAGE REGULATOR WITH FAST TRANSIENT RESPONSE

A Thesis

by

ROBERT JON MILLIKEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2005

Major Subject: Electrical Engineering

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ABSTRACT

A Capacitor-less Low Drop-out Voltage Regulator
with Fast Transient Response. (December 2005)
Robert Jon Milliken, B.S., Iowa State University
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Power management has had an ever increasing role in the present electronic industry. Battery powered and handheld applications require power management techniques to extend the life of the battery and consequently the operation life of the device. Most systems incorporate several voltage regulators which supply various subsystems and provide isolation among such subsystems. Low dropout (LDO) voltage regulators are generally used to supply low voltage, low noise analog circuitry. Each LDO regulator demands a large external capacitor, in the range of a few microfarads, to perform. These external capacitors occupy valuable board space, increase the IC pin count, and prohibit system-on-chip (SoC) solutions.

The presented research provides a solution to the present bulky external capacitor LDO voltage regulators with a capacitor-less LDO architecture. The large external capacitor was completely removed and replaced with a reasonable 100pF internal output capacitor, allowing for greater power system integration for SoC applications. A new compensation scheme is presented that provides both a fast transient response and full range ac stability from a 0mA to 50mA load current. A 50mA, 2.8V, capacitor-less LDO voltage regulator was fabricated in a TSMC 0.35um CMOS technology, consuming only 65uA of ground current with a dropout voltage of 200mV.

Experimental results show that the proposed capacitor-less LDO voltage regulator exceeds the current published works in both transient response and ac stability. The architecture is also less sensitive to process variation and loading conditions. Thus, the presented capacitor-less LDO voltage regulator is suitable for SoC solutions.

To my parents for their encouragement, love, and support

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I. INTRODUCTION

Industry is pushing towards complete system-on-chip (SoC) design solutions including power management. The study of power management techniques has increased dramatically within the last few years corresponding to the vast increase in the use of portable, handheld battery operated devices [1]. Power management seeks to improve the device power's efficiency resulting in prolonged battery life and operating time for the device. A power management system contains several subsystems including linear regulators, switching regulators, and control logic. The control logic changes the attributes of each subsystem; turning the outputs on and off as well as changing the output voltage levels, to optimize the power consumption of the device.

The presented research focuses on low drop-out (LDO) voltage regulators. LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. LDO voltage regulators have several inherent advantages over conventional linear voltage regulators making them more suitable for on-chip power management systems [2].

A power management system usually contains several LDO regulators and switching regulators. The conventional LDO voltage regulator requires a relatively large output capacitor in the single microfarad range. Large microfarad capacitors can not be realized in current design technologies, thus each LDO regulator needs an external pin for a board mounted output capacitor. The presented research proposes to remove the large external capacitor, eliminating the need for an external pin. Removing the large output capacitor also reduces the board real estate and the overall cost of the design and makes it suitable for SoC applications.

A. LDO Regulator Applications

LDO voltage regulators compose a small subset of the power supply arena. LDO voltage regulators are used in analog applications that generally require low noise, high accuracy power rails. Voltage regulators provide a constant voltage supply rail under all loading conditions.

This thesis follows the style of the *IEEE Journal of Solid-State Circuits*.

These conditions include fast current transients and rapid changes in the load impedance. Most hand-held, battery-powered electronics feature power-saving techniques to reduce power consumption. Circuits that are not performing tasks are temporarily turned off lowering the overall power consumption. The LDO voltage regulator, therefore, must respond quickly to system demands and power up connected circuits within a few system clock cycles, typically 1 to 2 μs.

1. Cell Phones

A typical cell phone power management IC is shown in Fig. 1. The purposed LDO regulator topology would be used for the RF/Analog power supplies. These require ultra low noise and a linear output. The LDO regulators are usually placed after switching regulators to improve their efficiency. The RF/analog blocks require LDO regulators with output currents up to 50 mA. They also require turn-on settling times around 2 μs.

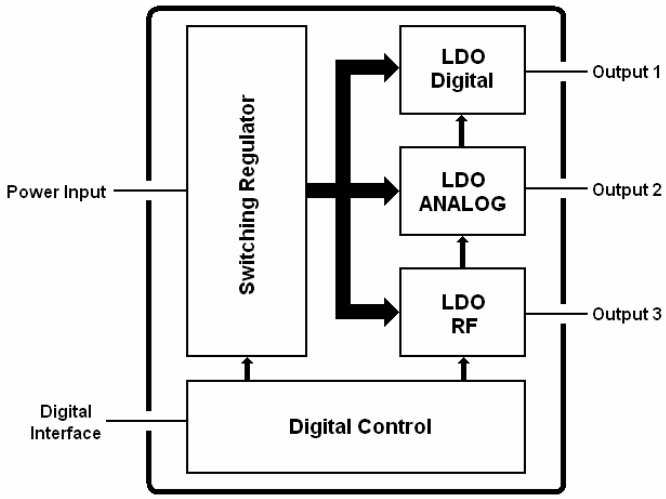

Fig. 1. Cell phone power management application.

Most cell phones use a 1 cell Li-ion battery supply. The maximum output voltage for a Li-ion battery is typically 4.2V at full charge. At the onset of battery dropout, the battery supplies 2.92V. Thus, the circuits must operate below roughly 3V. Fig. 2 shows the typical voltage

headroom at full battery discharge. To improve power efficiency, most system blocks are optimally design to operate with 2.8V power rails.

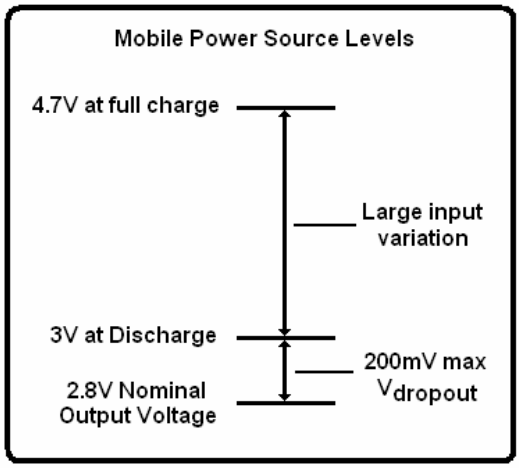

Fig. 2. Cell phone battery characteristics.

The proposed capacitor-less LDO was design to replace current RF/analog LDO regulators that require a large external output capacitor. These blocks operate at 2.8V and consume approximately 32 mA of current. Dropout voltage is a defining characteristic of an LDO regulator and defines the minimum voltage drop across the control element, usually a large common-source output transistor or pass transistor. The dropout voltage of the regulator can not exceed 200 mV to operate at the full battery discharge condition. The typical RF standby current is 50 μA and the RF/analog needs 65dB of power-supply-rejection-ratio (PSRR) at 217Hz.

2. High-Efficiency Linear Regulation

Linear regulators suffer from poor efficiency. The efficiency is inversely proportional to the voltage drop across the control element. Typically, linear regulators are cascaded after switching regulators. Switching regulators have the ability to buck or boost the input voltage to any desired output voltage with near 100% efficiency. Therefore, the voltage drop across the control element can be reduced which in turn increases the power efficiency of the linear regulator. Fig. 3 shows a linear regulator cascaded after a switching regulator.

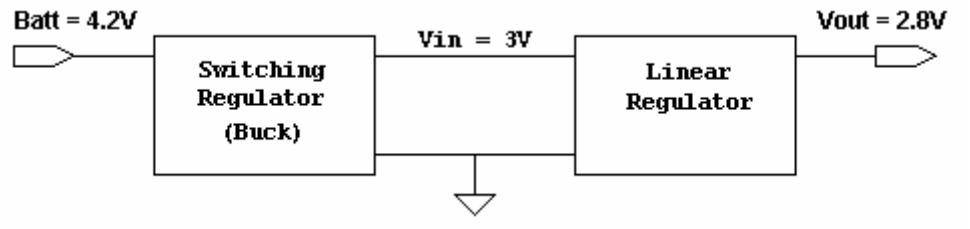

Fig. 3. High efficiency linear regulation.

Without the switching regulator, the voltage drop across the linear regulator ($V_{IN} - V_{OUT}$) would drastically increase. The switching regulator is designed to minimize the voltage drop across the linear regulator during loading conditions. Charge pumps can also be used to reduce the size and cost of the switching regulator.

B. Conventional Linear and LDO Regulator Architectures

Linear voltage regulators come in two different topologies: conventional linear regulators and LDO voltage regulators [3]. The only topological difference arises from the orientation of the pass element. The conventional linear voltage regulator uses a source follower in either a single transistor realization or a Darlington BJT configuration. The LDO regulator on the other hand uses a single transistor in a common-source configuration operating in saturation. The two configurations are shown in Fig. 4.

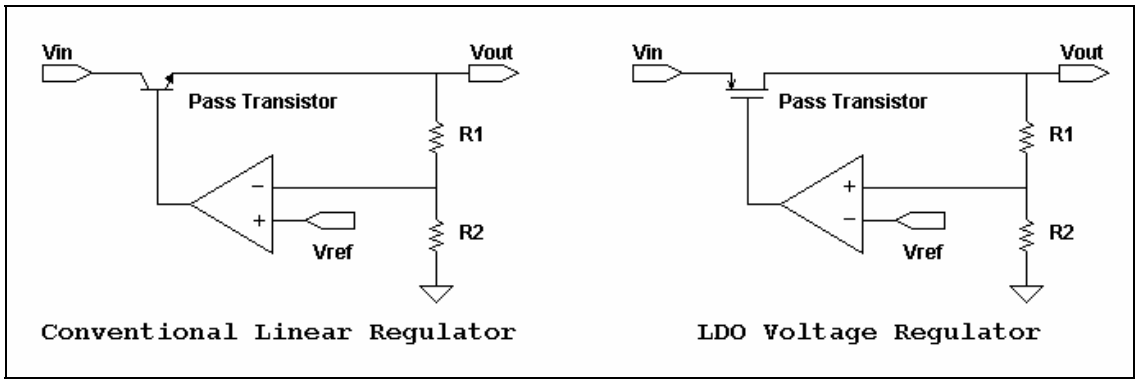

Fig. 4. Linear voltage regulator topologies.

Both linear regulators operate using the same feedback mechanism. The output voltage is sensed through feedback resistors R_1 and R_2. An error amplifier then compares the scaled output voltage to a reference voltage. The error signal is fed to the pass transistor and forms the negative feedback path.

Transistor orientation plays a major role in the operation and the stabilization of the linear voltage regulator. The conventional linear regulator requires gate drive voltages in excess of the input voltage making it cumbersome for low voltage applications. Conventional linear regulators are being used in some low-voltage applications but necessitate the use of charge pump gate drives. LDO voltage regulators overcome the necessary voltage headroom by operating the pass transistor in a common-source configuration. The V_{DS} saturation voltage of the pass transistor limits the regulator operation. The drop-out voltage or V_{DSAT} is a function of the maximum output current and the size of the pass transistor.

As mentioned earlier, the transistor orientation affects the stability of the regulator. Typical small signal AC responses for both architectures are shown in Fig. 5. The conventional linear regulator is inherently stable due to the low output impedance of the source follower. The first pole, P_1, acting as the dominant pole, is generated from the error amplifier output impedance. The output pole, P_2, moves with the load impedance but resides at much higher frequency.

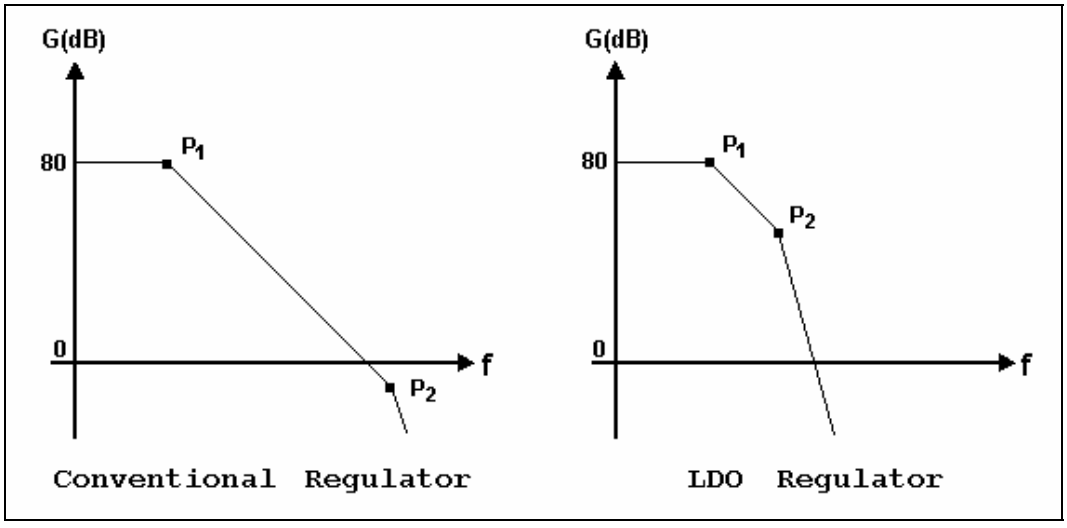

Fig. 5. AC pole locations without compensation.

LDO voltage regulators can operate in low voltage applications without the need of charge pumps, but they are inherently unstable. The large output capacitor and high output impedance create the dominant pole, P_1. This dominant pole, however, is located in close proximity to the error amplifier output pole, P_2. Thus, the LDO regulator's stability can not be guaranteed and will most likely be unstable. LDO regulators must be internally or externally compensated for guaranteed stability. Typical LDO regulators use the electro-static resistance (ESR) of the output capacitor to reach stability. The ESR creates a zero, that when placed in the vicinity of P_2, can add phase necessary to maintain stability. Fig. 6 shows the use of capacitor ESR.

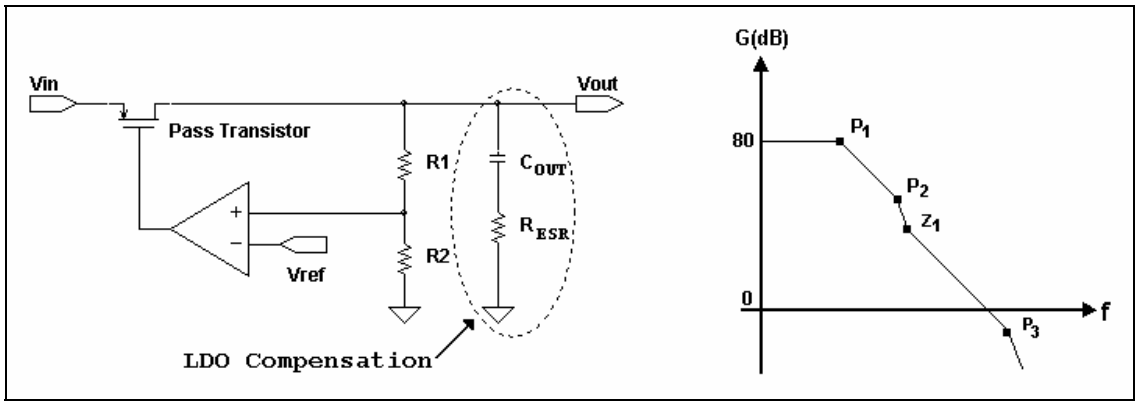

Fig. 6. Conventional LDO regulator compensation.

The ESR also creates a pole, P_3. The regulator stability depends heavily on the value of ESR. As ESR is decreased, the location of Z_1 moves to the right and consequently has no effect on phase margin. On the other extreme, when ESR is increased significantly, the associated pole, P_3, moves below the gain-bandwidth, and the LDO regulator becomes unstable. A given LDO regulator must be given a range of stable capacitor ESR, otherwise the LDO regulator will be unstable.

Several recent publications have sought to eliminate the dependence on ESR. They exploit the use of internal compensation, either by creating an internal zero or adaptively modulating the location of the dominate pole. The presented research seeks to push one step further by eliminating the large external output capacitor altogether. The research begins with

the basic fundamental properties of linear regulators. This forms the foundation and direction to realize capacitor-less LDO voltage regulators.

C. LDO Regulator Characterization

LDO voltage regulators and all other voltage regulators ideally have constant output voltage regardless of supply voltage or load current variations. Voltage regulator specifications generally fall into three categories: static-state or steady-state specifications, dynamic-state specifications, and high-frequency specifications [4]. All the equations presented consider only CMOS LDO voltage regulators, but the same basic principles relate to most other linear voltage regulators.

1. Static-state Specifications

The static-state parameters include the line regulation, the load regulation, and the temperature coefficient effects. The line and load regulation specifications are usually defined for a given LDO regulator and measure the ability to regulate the steady-state output voltage for given line and load steady-state values. The temperature coefficient defines the combined performance of the voltage reference and the error amplifier offset voltage.

Line Regulation defines the ratio of output voltage deviation to a given change in the input voltage. The quantity reflects the deviation after the regulator has reached steady-state. A general line regulation equation is given in equation 1.

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{g_{mp} r_{op}}{A\beta} + \frac{1}{\beta}\left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right) \tag{1}$$

Line regulation depends on the pass transistor transconductance, g_{mp}, the LDO output resistance, r_{op}, the LDO loop gain, $A\beta$, and the feedback gain, β. Fig. 7 below illustrates the LDO parameters.

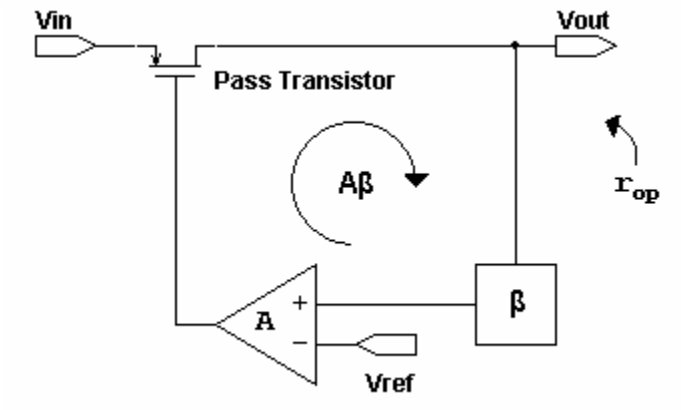

Fig. 7. LDO regulator parameters.

Smaller output voltage deviation for a given dc change in input voltage corresponds to a better voltage regulator. To increase the line regulation, the LDO regulator must have a sufficiently large loop gain. These quantities become clear in the LDO regulator design discussion.

Load regulation is a measure of output voltage deviation during no-load and full-load current conditions. The load regulation is related to the loop gain, Aβ, and the pass transistor output impedance, r_{op}. This relation is given in equation 2.

$$LR_{load} = \frac{\Delta V_O}{\Delta I_O} = \frac{r_{op}}{1 + A\beta} \tag{2}$$

The load regulation improves as the loop-gain increases and the output resistance decreases. The load regulation only applies to the LDO regulator steady-state conditions and does not include load transient effects.

The temperature coefficient defines the output voltage variation due to temperature drift of the reference and the input offset voltage of the error amplifier. The temperature coefficient is given in equation 3.

$$TC = \frac{1}{V_{OUT}} \cdot \frac{\partial V_{OUT}}{\partial Temp} \approx \frac{1}{V_{OUT}} \cdot \frac{\Delta V_{TC}}{\Delta Temp} = \frac{\left[\Delta V_{TC\,REF} + \Delta V_{TC\,VOS}\right] \cdot \frac{V_{OUT}}{V_{REF}}}{V_{OUT} \cdot \Delta Temp} \quad (3)$$

The output voltage accuracy improves as the error amplifier offset voltage is reduced and the reference voltage temperature dependence is minimized.

The LDO regulator's dropout voltage determines the maximum allowable current and the minimum supply voltage. These specifications, dropout voltage, maximum load current, and minimum supply voltage, all depend on the pass transistor parameters. A particular LDO design typically specifies the maximum load current and the minimum supply voltage it can tolerate while maintaining pass transistor saturation. Equation 4 relates the LDO dropout voltage to device parameters were I_{LOAD} is the maximum sustainable output current.

$$V_{dropout} = I_{LOAD} \cdot R_{ON} = V_{DSAT,PMOS} \quad (4)$$

The pass transistor dimensions are designed to obtain the desired V_{DSAT} at the maximum load current, I_{LOAD}.

2. Dynamic-state Specifications

The LDO regulator dynamic-state specifications specify the LDO regulator's ability to regulate the output voltage during load and line transient conditions. The LDO regulator must respond quickly to transients to reduce variations in output voltage. Dynamic-state specifications, unlike steady-state specifications, depend on the large signal LDO regulator capabilities. The most significant capability is the charging and discharging of parasitic capacitance and the parasitic capacitor feed-through.

Load transients define the LDO regulator's ability to regulate the output voltage during fast load transients. The largest variations in output voltage occur when the load-current steps from zero to the maximum specified value. The ability of the LDO to regulate the output voltage

during a large current transient depends on the closed-loop bandwidth, the output capacitance, and the load-current. The output voltage variation is modeled in equation 5.

$$\Delta V_{out} = \frac{I_{\max} \cdot \Delta t}{C_{out}} \tag{5}$$

I_{max} is the maximum specified output current, Δt is the LDO response time, and C_{out} is the LDO output capacitance. Δt is approximately the reciprocal of the LDO closed-loop bandwidth. A large output capacitor and large closed-loop bandwidth improve the load regulation. Conventional LDO regulators inherently have large output capacitors and therefore will have better load regulation verses capacitor-less LDO regulators.

Parasitic capacitors also cause slewing effects that degrade LDO regulator's load transient response. The gate capacitance of the pass transistor can be significant and places strain on the error amplifier. If the slew rate at the gate of the pass transistor is much slower than the gain-bandwidth product, significant transient voltage spikes appear at the output voltage node during fast load transients. This effect becomes more pronounced with capacitor-less LDO regulators.

Ripple-rejection-ratio specifies the ability for the regulator to rejected input signals from the output node. This parameter measures the small-signal gain from the input voltage to the output voltage. The ripple rejection ratio is given in equation 6.

$$ripple\ rejection = 20\log_{10}\frac{output\ ripple\ voltage}{input\ ripple} \tag{6}$$

The ripple-rejection-ratio is typically determined for lower frequencies within the gain-bandwidth product. Large input voltage transient spikes can cause larger output voltage variations than predicted by the ripple-rejection-ratio. The deviation is due to large signal effects, mainly capacitor slewing.

3. High-frequency Specifications

Power-supply-rejection-ratio (PSRR) and regulator output noise can be categorized as high-frequency specifications. Both parameters are small signal parameters and are plotted verses frequency. Most LDO regulators specify PSRR at certain frequencies as well as spot noise at a particular frequency greater than the gain-bandwidth product [5].

PSRR defines the LDO regulator's ability to reject high-frequency noise on the input line. PSRR is a function of pass transistor parasitic capacitances and is proportional to the reciprocal of the loop gain. The error amplifier plays a major role in improving PSRR [5]. The combined individual error amplifier PSRR and the individual pass transistor PSRR is desired to sum to zero at the output voltage node. The design techniques to minimize PSRR are studied later on in the text.

Output noise is primarily defined by the input stage transconductance. The subsequent stages do not add significant noise to the output. Maximizing the input transistors' size lowers the output noise. The optimal noise figure is dependent on each particular design and a general analysis lacks sufficient information.

4. LDO Regulator Efficiency

The LDO regulator efficiency is determined by three parameters: ground current, load current, and pass transistor voltage drop. The total no-load quiescent current consumption for the entire LDO regulator circuitry is defined as the ground current. Equation 7 relates the LDO regulator power efficiency.

$$Eff = \frac{V_{out} \cdot I_{LOAD}}{V_{in} \cdot (I_{GND} + I_{LOAD})} \tag{7}$$

There are two cases for power efficiency, one for small load currents and one for large load currents. The relation reduces to equation 8 for small load currents.

$$Eff \approx \frac{I_{LOAD}}{I_{GND} + I_{LOAD}} \tag{8}$$

Thus, ground current affects the LDO regulator efficiency much more at very low load currents. The longevity of battery life for low current applications can be significantly increased by reducing the quiescent ground current. At the other extreme, for very large load currents, the power efficiency is solely dependent on the pass transistor voltage drop, shown in equation 9.

$$Eff \approx \frac{V_{out}}{V_{in}} \tag{9}$$

The efficiency of the linear regulator approaches 100% as the output voltage approaches the input voltage. This scenario, however, requires an infinitely large pass transistor but would result in an infinite gate capacitance. Clearly, there is a trade-off between efficiency and the speed of the LDO regulator.

5. Specification Trade-offs

All the LDO regulator specifications are interrelated and lead to important tradeoffs. The largest among all other specifications is efficiency, stability, and transient response. The optimization, especially with tight constraints, becomes very convoluted. The tradeoffs will be more apparent when designing the LDO regulator.

D. Capacitor-Less LDO Voltage Regulators

The basic linear voltage regulator architectures and their properties have been discussed. Research continues on conventional LDO regulators but recent research is focusing on capacitor-less LDO voltage regulators [2]-[10]. As mentioned before, removing the output capacitor on LDO regulators allows SoC designs to fully incorporate power management systems with

multiple LDO voltage regulators. Removing the external capacitor also reduces board real estate and system costs. The basic capacitor-less LDO voltage regulator is shown in Fig. 8.

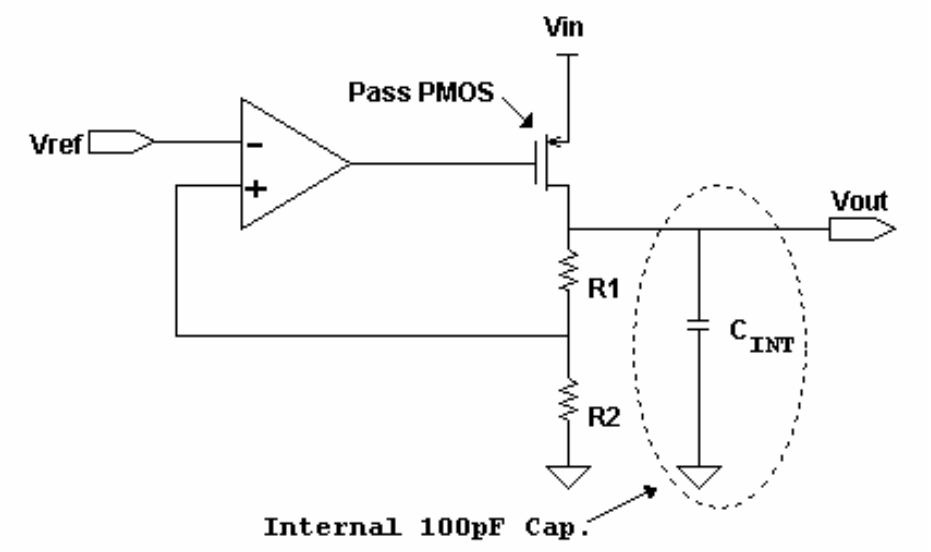

Fig. 8. Capacitor-less LDO voltage regulator.

The capacitor-less LDO regulator still has an internal output capacitor but it is much smaller than those used by conventional LDO voltage regulators. Current industrial capacitor-free LDO regulators decrease the required external capacitor by a factor of 10 or so, but they still use a 0.1 microfarad external capacitor. The presented research purposes the complete removal of the external capacitor and its replacement with a small internal capacitor. The internal capacitor is maximized as much as possible but is constrained by chip size dimensions and current CMOS technology. Typical capacitor values fall in the range of a few hundred picofarads.

1. Initial Capacitor-less LDO Regulators Pole Locations

Most of the conventional LDO specifications are greatly affected when the external capacitor is reduced by several orders of magnitude. The most significant side effect is stability degradation. The uncompensated capacitor-less LDO has two major poles, the error amplifier output pole, P_1, and the load dependent output pole, P_2. Fig. 9 shows the relative pole location.

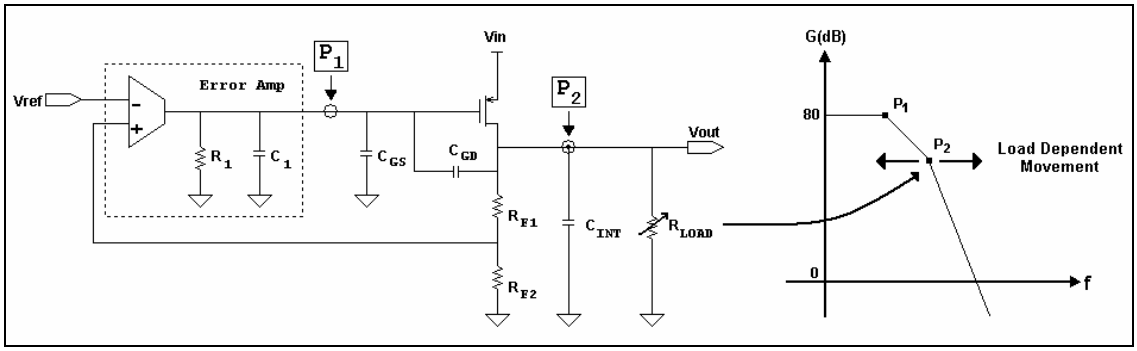

Fig. 9. Pole locations for uncompensated capacitor-less LDO voltage regulator.

The standalone error amplifier has a pole located at relatively high frequency. The equivalent pass transistor input capacitance adds significant capacitance to the error amplifier output impedance. The location of P_1 is given by equation 10.

$$\omega_{P1} = \frac{1}{R_1 \cdot (C_1 + C_{GS} + A_{Pass} C_{GD})} \tag{10}$$

The pass transistor is very large in order to reduce V_{DSAT}. Therefore, C_{GS} and C_{GD} are extremely large, in the tens of picrofarads. C_{GD} also forms a Miller capacitor which increases the effective input capacitance by the gain of the pass transistor. The pass transistor has a typical gain of 20dB or 10V/V at low load currents. The Miller capacitor can increase the effective pass transistor input capacitor to a few hundred picofarads. Thus, the pole, P_1, resides at low frequencies of typically a few kilohertz. The gain of the pass transistor changes with varying load current. P_1 is therefore load dependent but less so than P_2. The first tradeoff is between efficiency and stability. The large output current efficiency is inversely proportional to the pass transistor's V_{DSAT}. Smaller V_{DSAT} increases the effective input gate capacitance and consequently decreases the error amplifier pole frequency, increasing the burden on the error amplifier.

The second pole, P_2, is located at the LDO's output. The output resistance decreases for increasing load current. P_2 is directly proportional to the load current and is load dependent. The location of P_2 is given by equation 11.

$$\omega_{P2} = \frac{1}{(R_{OUT} \,//\, R_{LOAD}) \cdot C_{INT}} \tag{11}$$

High load current pushes the output pole, P_2, to higher frequency, and the capacitor-less LDO regulator is usually stable. At low currents, the effective load resistance increases significantly. P_2 is pushed to lower frequency in close proximity to the error amplifier pole. Stability cannot be guaranteed due to the decreased phase margin. The uncompensated capacitor-less LDO regulator is not stable at low currents, especially at the no-load condition.

2. Transient Response Attributes

The large external capacitor is used on conventional LDO regulators and linear regulators in general to improve the transient load regulation [2],[6] and [8]. The output capacitor stores potential energy equivalent to the output voltage. The ideal capacitor can deliver instantaneous current and has infinite bandwidth, assuming its source resistance in zero. The transfer of charge from the capacitor to the load corresponds to a drop in output voltage. Equation 12 gives a relationship for this voltage difference.

$$\Delta V_{OUT} = \frac{\Delta Q}{C_{OUT}} \tag{12}$$

Thus, the change in output voltage is inversely proportional to the output capacitance. The output voltage ripple for a given load transient is reduced by increasing the output capacitance. This relationship becomes much more apparent when the load transients are much faster than the

gain-bandwidth product, which is usually the case. Fig. 10 illustrates this situation in a conventional LDO voltage regulator.

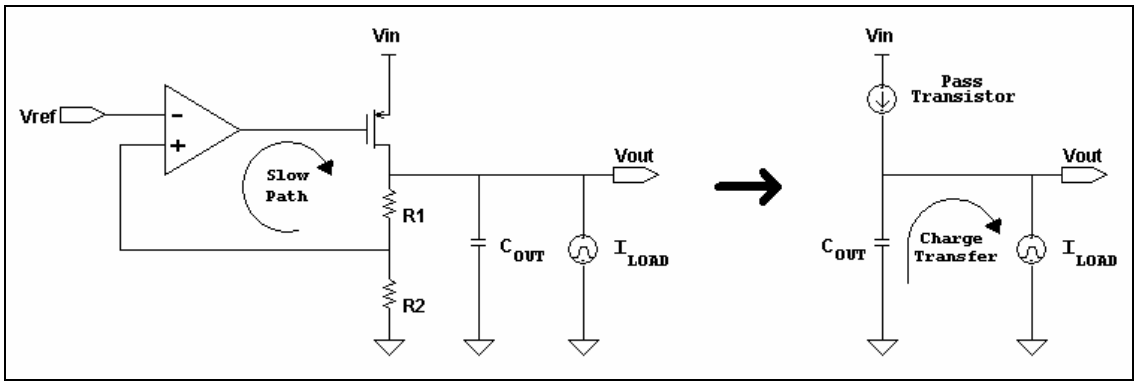

Fig. 10. Equivalent circuit for fast load transients.

The gain-bandwidth is much slower than the load transient and the pass transistor gate voltage can be assumed constant throughout the load transient. The circuit diagram to the right of Fig. 10 has substituted a constant current source for the pass transistor. Then the output voltage is only determined by equation 12 and equation 5. The capacitor-less LDO regulator does not have the advantages of a large external capacitor. Instead, the constant current source in Fig. 10 must be replaced with high speed adaptive current source.

The pass transistor has a very large transconductance, but the large effective input capacitance limits its transient speed. The effective input gate capacitance is driven by the error amplifier. In order for the error amplifier to drive large capacitive loads, the quiescent bias current must be increased. Slewing occurs at the pass transistor gate given by equation 13.

$$SR = \frac{I_{bias,error}}{C_{GS,eff}} \tag{13}$$

The error amplifier output stage bias current only effects the slew rate in equation 13, and the $C_{GS,eff}$ is the total effective input gate capacitance of the pass transistor. Conventional LDO

regulators typically use an error amplifier with a class AB output stage. This lowers the output impedance and increases the drive capability of the error amplifier. The fundamental problem still exists; the power must be increased to drive larger pass transistors. This forms the second inherent tradeoff, the power efficiency is directly proportional to the transient response. A third tradeoff exists between large-current power efficiency and low-current efficiency. The large current efficiency is improved by reducing V_{DSAT}. The effective pass transistor input gate capacitance is increased, however; the ground current or bias current must be increased for acceptable load transient response. The tradeoff is shown in Fig. 11.

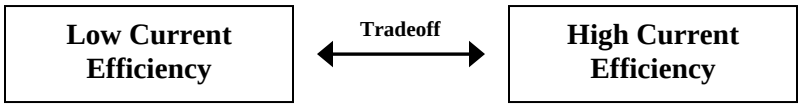

Fig. 11. Power efficiency tradeoff.

The capacitor-less LDO regulator is design for a specific application where the nominal operating point is known. Clearly, the pass transistor forms the backbone of the LDO regulator and consequently defines most of the design tradeoffs.

3. Previous Academic Works

Only a few works have been published in the IEEE regarding capacitor-less LDO regulators [4], [11], and [12]. To date, there have been no works published in IEEE journals that demonstrate a completely stable common-source LDO regulator with no external capacitor. They all have problems either tracking the output pole variation or have problems with high impedance loads. The first work used a DFC analog block to create a fix internal dominant pole [4]. The circuit architecture is shown in Fig. 12.

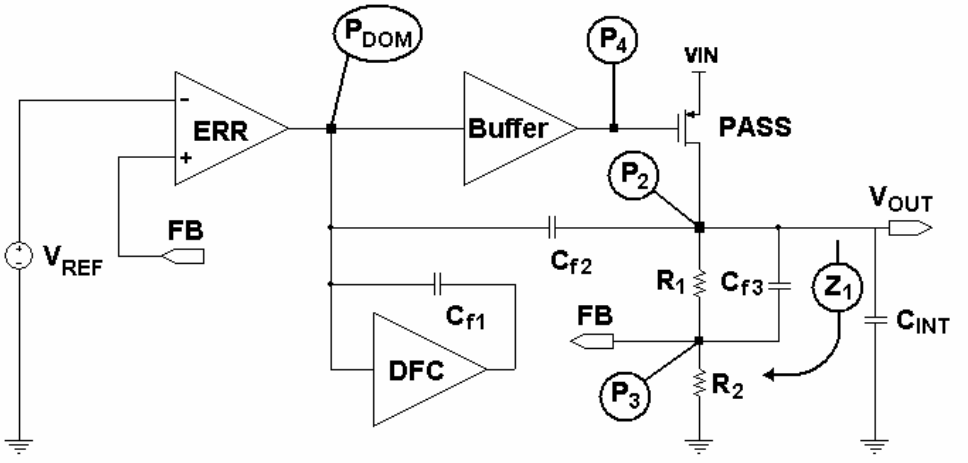

Fig. 12. Capacitor-free LDO voltage regulator.

A zero and a pole are created with compensation capacitor C_{F1}. The zero is used to cancel the output pole. The parasitic pole, P_f, must be placed past the unity-gain frequency. The compensation technique is shown in Fig. 13.

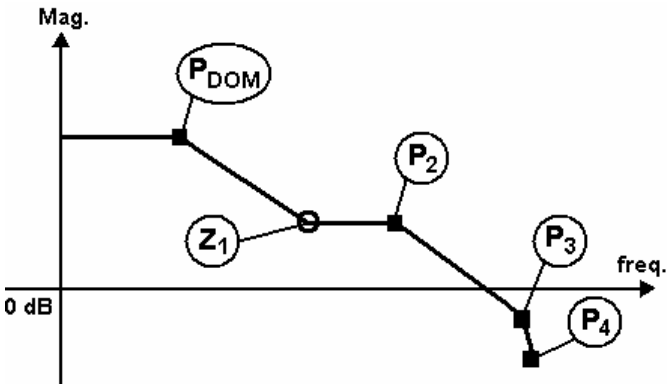

Fig. 13. LDO compensation with C_{F1}.

Two problems arise with this architecture. First, the pole created with C_{F1} is limited by the selection of feedback resistors and will most likely be relatively close to Z_f. This greatly reduces the effect of the cancellation zero. Second, the zero is fixed and does not move with the load dependent output pole. This pole moves well over a decade, and the stability at no-load

condition is most likely unstable. The capacitor-free LDO regulator using this concept was unstable for loads smaller than 5mA.

The second work [10] moves in the right direction using pole-zero tracking frequency compensation. The structure is shown in Fig. 14.

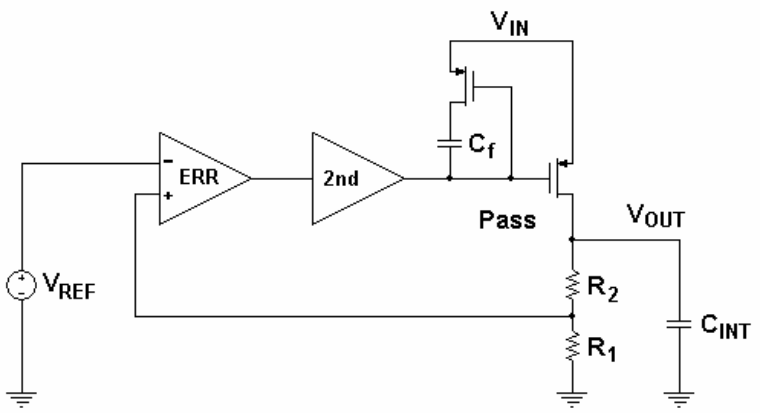

Fig. 14. LDO regulator with pole/zero tracking.

They use a variable zero created by a linear resistor. This structure is also not completely stable over the entire output current range. The resistance does not have enough tunable range due to its weak function of the load current.

4. Capacitor-less LDO Design Direction

A new structure was needed to compensate the capacitor-less LDO while maintaining good load transient response and stability at low load currents. The transient response is dependent on the speed of the pass transistor and not the output capacitor. A fast transient path from the LDO output to the gate of the pass transistor was required since the system gain-bandwidth was relatively low in frequency. The capacitor-less LDO stability at low load currents was the second major problem. The initial idea sought to apply adaptive techniques to compensate the output pole and possibly the error amplifier output pole. The basic concept is shown in Fig. 15.

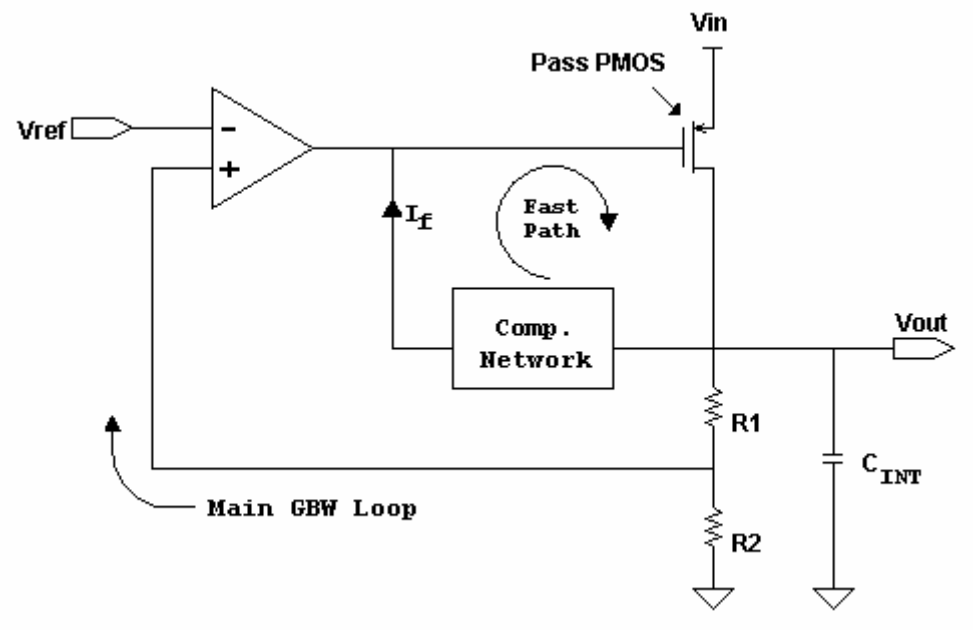

Fig. 15. Basic capacitor-less LDO concept.

The concept in Fig. 15 uses a fast path to improve the transient response. A compensation network is needed to stabilize the new fast transient system. The main feedback loop determines the capacitor-less LDO's gain-bandwidth product and is the main mechanism that replenishes the energy in the output capacitor, restoring the output voltage to the correct steady-state level. The fast path is an internal negative feedback loop with very high bandwidth, much greater than the overall gain-bandwidth product. The fast path senses any load current variation and mirrors and amplifies the signal directly into the gate of the pass transistor.

The concept in Fig. 15 formed the basis of research and design for the final capacitor-less LDO voltage regulator. A specific application was selected for the design, and the capacitor-less LDO was designed to approach most of the conventional LDO specifications. This leads to the formal design analysis discusses in Section II.

II. CAPACITOR-LESS LDO REGULATOR ANALYSIS

The capacitor-less LDO regulator design targets the cell phone and handheld device market. Each of these designs uses a power management IC to improve the battery life longevity and usually contain several LDO voltage regulators, shown in Fig. 1 in Section I. The proposed capacitor-less LDO voltage regulator would most likely replace the analog/RF and audio power supplies. Based on the current specification for these LDO regulator applications, the proposed capacitor-less LDO specification was developed as shown in Table I.

TABLE I

CAPACITOR-LESS LDO SPECIFICATION

PARAMETER	VALUE
Gain Bandwidth	1 ~ 2 MHz
Settling Time	< 2 μs
Loop Gain	~ 100 dB
GND Current	< 150 μA
Dropout Voltage	200 mV
Output Current	0 ~ 50 mA
PSRR	< -40dB @ 100kHz
Output Noise	< 20 μV
Line Regulation	0.01%
Load Regulation	0.02%
Technology	TSMC 0.35μ CMOS

The chosen capacitor-less LDO specification is competitive with current conventional LDO voltage regulators with the exception of the transient response and high frequency response, accounting for the reduced output capacitance. This formed the basis for the LDO design, and the device characterization soon followed.

The capacitor-less LDO design must incorporate two important criteria: stability and fast transient response. There were two possible angles of attack. The first method starts by stabilizing the LDO regulator and then optimizing the stability for fast transient response. The second method first optimizes the fast transient response and then stabilizes the fast transient

LDO regulator. It was found easier to apply the second method and start by adding a fast transient path.

The uncompensated capacitor-less LDO regulator had to be characterized first before any new topologies were developed. This included the complete characterization of poles, DC gains, and fixed device parameters. Also, the uncompensated transient response was needed to determine slewing issues and relative circuit speed. The capacitor-less LDO regulator was inherently unstable for DC output currents lower than approximately 5mA. However, a test circuit was constructed to measure the slewing effects. The pass transistor's subthreshold saturation region also played a major role in the LDO operation. These effects are all summarized in the following section, Uncompensated Device Characterization.

A. Uncompensated Device Characterization

The pass transistor determines the maximum output current and the dropout voltage. These parameters are essentially fixed throughout the LDO operation. The pass transistor could be designed before a new topology was constructed. Thus, the LDO compensation and the fast transient path are in place to compensate the effects of the large pass transistor.

The first section discusses the pass transistor design process. Following the design of the pass transistor, the LDO is characterized for both AC response and transient response. The results from the uncompensated device characterization were directly applied to the final proposed capacitor-less LDO topology.

1. Pass Transistor Design

The dropout voltage of the capacitor-less LDO was selected to be 200mV for a maximum load current of 50mA based on current LDO regulator requirements. In device parameters, the pass transistor is designed to deliver a drain current of 50mA while maintaining a saturation voltage, $V_{DS} \geq V_{GS} - V_T$, of 200 mV or less. The pass transistor stage is shown in Fig. 16.

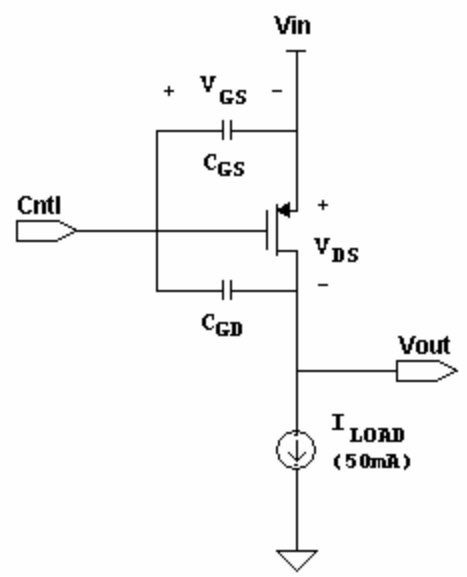

Fig. 16. Pass transistor design.

First order approximations were used to find the rough device dimensions. This relationship is shown in equation 14.

$$V_{dropout} = V_{DSAT} = \sqrt{\frac{2I_{MAX}}{\mu_p C_{OX} W / L}} \tag{14}$$

I_{MAX} defines the maximum output current, forcing the dimensions of the pass transistor, W/L, for a desired minimum $V_{DROPOUT}$. The variables μ_p, hole mobility, and C_{OX}, the gate capacitance per unit area, are device technology parameters and are given in Table II. The device parameters in Table II were used to design the pass transistor. Equation 14 was rearranged to find the pass transistor device dimensional ratio, W/L, shown in equation 15.

$$\left[\frac{W}{L}\right]_{PASS} = \frac{2I_{MAX}}{\mu C_{ox} V_{DSsat}^{\ 2}} = 37.8 \times 10^3 \tag{15}$$

TABLE II

TSMC 0.35 DATA: RUN T4CU

PARAMETER	VALUE
V_{TP}	0.58 V
V_{TN}	-0.74 V
$\mu_p C_{OX}$	180.2 $\mu A/V^2$
$\mu_n C_{OX}$	66.00 $\mu A/V^2$

The ratio found in equation 15 was very large. The channel length was minimized to reduce the gate capacitance C_{GS}. The minimum length is 400nm, set by the TSMC 0.35µm CMOS process. This forces the pass transistor width to 15,000µm or 15mm. BSIM3 computer simulations were used to verify and fine tune the pass transistor dimensions. Table III shows the calculated and simulated pass transistor parameters to yield a 200mV dropout voltage at 50mA load current.

TABLE III

PASS TRANSISTOR DIMENSIONS

CALCULATED	SIMULATED
W = 15mm	W = 16mm
L = 400nm	L = 400nm
C_{GS} = 19.1 pF	C_{GS} = 20.18 pF
C_{GD} = 5.0 pF	C_{GD} = 3.84 pF

CADENCE simulations show that the actual dimensional ratio of the pass transistor must be at least 40,000. Unfortunately, this means that for a device of minimum length, the required width must increase to 16mm instead of the calculated 15mm width. Such a large device introduces significant parasitic capacitances into the network, notably the gate-source capacitance C_{GS}. As mentioned previously in this report, large gate capacitance along with variable low-frequency load impedance makes stabilizing a capacitor-less LDO difficult. The gate-source capacitance of this PMOS pass-transistor measured 20pF. The Miller effect with C_{GD} further increases the effective gate capacitance. Equation 16 relates the total effective gate capacitance.

$$C_{GS,eff} \cong C_{GS} + (1 + A_{pass}) \cdot C_{GD} = C_{GS} + (1 + G_{m,pass} R_{O,pass}) \cdot C_{GD} \quad (16)$$

The effective pass transistor gate capacitance approaches 100pF. Thus, the Miller capacitor contributes most of the effective gate capacitance while varying with load conditions.

Pass transistor subthreshold operation is another major concern. For large variations in the load current, the PMOS transistor will undergo a transition from operating in the saturation region to operating in the subthreshold saturation region. The pass transistor exhibits an exponential relationship while operating in subthreshold in contrast to the nominal square law relationship. The relationship is shown in the equation 17.

$$I_D \cong I_{DO}\left[\frac{W}{L}\right] e^{(qV_{GS}/\ nkT)} \quad (17)$$

Subthreshold operation produces a significantly slower response. This may cause significant degradation in the voltage regulation for applications where the load current drops to low current levels in a short span of time. This degradation in load regulation can only be counteracted by providing more current to the LDO, improving the speed of the circuit. This is especially true during subthreshold operation.

The pass transistor constitutes the only fixed predetermined capacitor-less LDO component. The other components, including the error amplifier, feedback gain, fast transient path, and the compensation network, are molded around the fixed pass transistor. Next, the newly designed pass transistor was simulated using a generic control loop.

2. Uncompensated AC Response

The pole locations were determined over the entire desired operating range of 0 to 50mA, using the generic control loop. The pass transistor transconductance and output impedance were simulated in CADENCE over the output current operating range. The simulated pass transistor

data could then be used in MATLAB for a more robust AC simulation. The control loop is shown in Fig. 17.

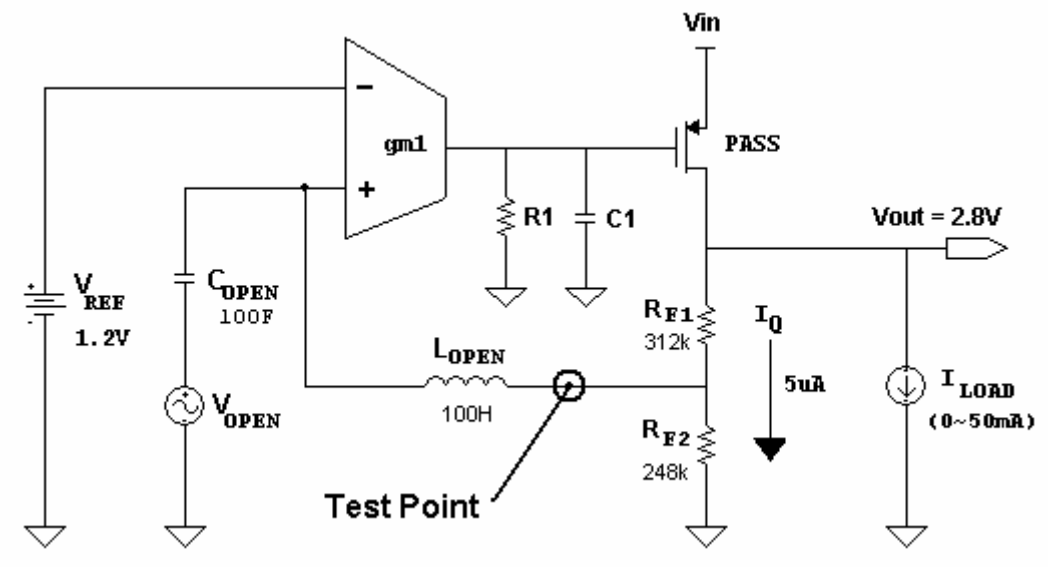

Fig. 17. AC open-loop simulation circuit.

The transconductance, gm1, and the output impedance, R_1 and C_1, form the error amplifier. The feedback resistors, R_{F1} and R_{F2}, were designed to yield an output voltage of 2.8V. Equation 18 relates the reference voltage, V_{REF}, to the output voltage assuming infinite loop gain.

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{F1}}{R_{F2}}\right) \tag{18}$$

The output voltage is defined by the feedback resistor ratio and the input reference voltage. The absolute resistance determines the pass transistor quiescent current, I_Q. Standard BiCMOS bandgap reference output is 1.24V in a range of -40°C to 80°C. Thus, the input reference voltage of 1.24V was used throughout the capacitor-less LDO regulator design.

L_{OPEN} forms a DC feedback path, blocking most of the AC components. This allows for an open-loop AC response measurement at the test point shown in Fig. 17. The DC feedback loop through L_{OPEN} sets the DC operating points for the LDO that would normally occur during closed-loop operation. C_{OPEN} couples the AC test signal to the amplifier loop without affecting the LDO's DC operating points. Both L_{OPEN} and C_{OPEN} are very large, 100H and 100F respectively. This allows the AC measurement down to very low frequencies.

A block diagram was used to simulate the open-loop LDO AC response. The uncompensated LDO was divided into separate amplifier blocks shown in Fig. 18.

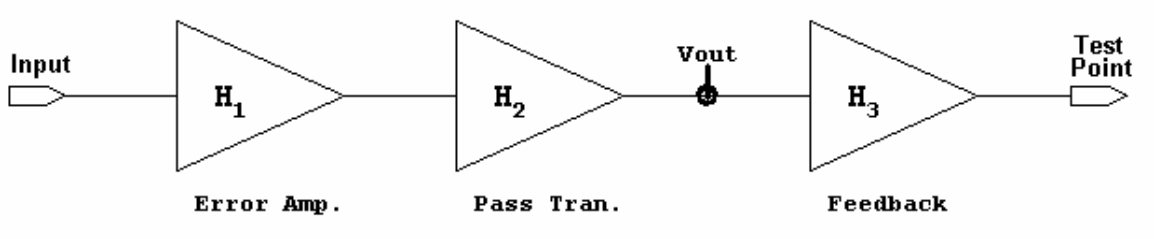

Fig. 18. AC open-loop block diagram test circuit.

H_1, H_2, and H_3 represent the error amplifier, the pass transistor, and the feedback gain, respectively. The pass transistor was already designed based on the desired dropout voltage and the maximum load current. This left the error amplifier and the feedback gain to be designed. Feedback resistors, R_{F1} and R_{F2}, were designed to draw 5μA of current through the pass transistor. The current through the series-connected feedback resistors is solely determined by the output voltage. Equation 19 defines the series relationship of R_{F1} and R_{F2}.

$$R_{F1} + R_{F2} = \frac{V_{OUT}}{I_{Q,pass}} = \frac{2.8V}{5\mu A} = 560k\Omega \tag{19}$$

Equation 20 was then used to find the absolute resistor values, combining equation 18 and the results from equation 19.

$$R_{F2} = \frac{V_{REF}}{V_{OUT}}\left(R_{F1} + R_{F2}\right) = \left(\frac{1.24}{2.8}\right) \cdot 560k\Omega = 248k\Omega \tag{20}$$

This forces the resistance of R_{F1} to 312k. A parasitic capacitor was also incorporated into the feedback gain section. This capacitor was used to simulate the effects of the error amplifier input capacitance and any parasitic capacitance associated with resistor layout. The addition of the capacitor is shown in Fig. 19.

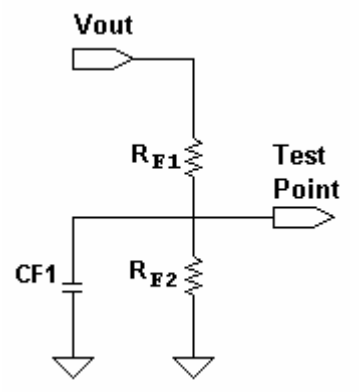

Fig. 19. Feedback circuit with parasitic capacitor, C_{F1}.

The feedback gain transfer function was divided into two components, the DC gain and the AC gain characteristics. Equation 21 gives the small signal transfer function for gain block H_3.

$$H_3 = \left[\frac{R_{F2}}{R_{F1} + R_{F2}}\right]_{DC} \cdot \left[\frac{1}{1 + s(R_{F1} \,//\, R_{F2}) \cdot C_{F1}}\right]_{AC} \tag{21}$$

Thus, the parasitic capacitor, C_{F1}, only contributes a pole. The location of the feedback pole resides at relatively high frequency. Nonetheless, C_{F1} can affect the phase margin and the fast transient response.

The pass transistor stage, H_3, forms a common source amplifier. Fig. 16 showed the complete pass transistor circuit including the parasitic capacitors, C_{GS} and C_{GD}. This circuit was used to form a small signal model, shown in Fig. 20.

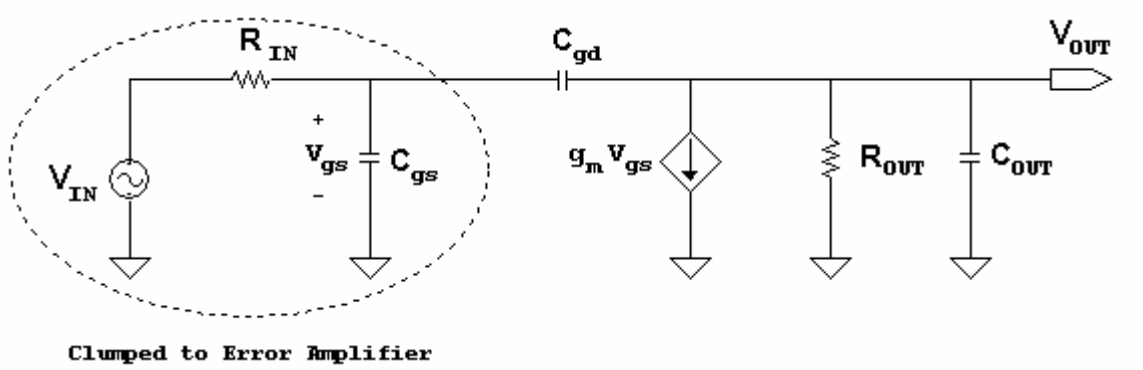

Fig. 20. Pass transistor small signal analysis.

The pass transistor input impedance was merged with the error amplifier. H_3 represents the rest of the pass transistor circuit elements. Preliminary inspection indicates H_3 had one pole and one zero. Equation 22 forms the nodal analysis at the pass transistor output with V_{GS} as the input.

$$v_{out}/R_{out} + sC_{OUT}v_{out} + (v_{out} - v_{gs})sC_{gd} + v_{in}g_m = 0 \tag{22}$$

Equation 22 was rearranged to form the output transfer function in equation 23.

$$\frac{v_{out}}{v_{gs}} = \frac{-g_m R_{out}\left(1 - s\frac{C_{gd}}{g_m}\right)}{s(C_{out} + C_{gd})R_{out} + 1} \tag{23}$$

Both a pole and a zero appeared in the transfer function reflecting the preliminary inspection. The transfer function for H_1 followed similar results as H_2 but without the feed-forward zero. Table IV lists the rest of the small signal characterization and the poles and zeros for the amplifier blocks given in Fig. 18.

TABLE IV

AMPLIFIER BLOCK SMALL SIGNAL TRANSFER FUNCTIONS

BLOCK	TRANSFER FUNCTION	POLE/ZERO
H_1	$TF = \frac{g_{m1}R_1}{1+sR_1C_1}$	$p_1 = \frac{1}{R_1C_1}$
H_2	$TF = \frac{-g_{mp}R_{out}\left(1-s\frac{C_{gd}}{g_{mp}}\right)}{s(C_{out}+C_{gd})R_{out}+1}$	$p_2 = \frac{1}{R_{OUT}C_{OUT}}$ $z_1 = \frac{g_{mp}}{C_{gd}}$
H_3	$TF = \left[\frac{R_{F2}}{R_{F1}+R_{F2}}\right]_{DC} \cdot \left[\frac{1}{1+s(R_{F1} // R_{F2})\cdot C_{F1}}\right]_{AC}$	$p_3 = \frac{1}{R_{F1} // R_{F2}\cdot C_{OUT}}$

Amplifiers H_1 and H_2 are characterized by a simple first order transconductance transfer function. H_1 forms the error amplifier module, where C_1 constitutes the error amplifier output capacitance in parallel with the effective pass transistor gate capacitance. The effective pass transistor gate capacitance was derived in equation 16. Equation 24 forms the complete error amplifier output pole.

$$\omega_{P1} = \frac{1}{R_1C_1} = \frac{1}{R_1[C_{error} + C_{GS} + (1+G_{m,pass}R_{O,pass})\cdot C_{GD}]} \tag{24}$$

H_3 forms the pass transistor common source amplifier with g_{mp} equaled to the pass transistor transconductance. R_{OUT} in pass transistor amplifier block, H_3, combines several circuit

parameters. There are two different methods of modeling R_{OUT} based on loading conditions. The load can either be modeled as a resistor or as a current source. Fig. 21 shows the two different methods for modeling the pass transistor output impedance.

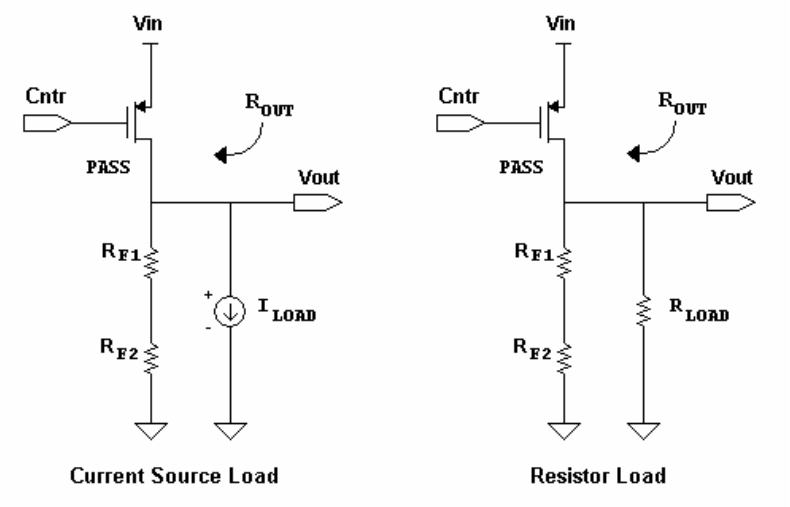

Fig. 21. Pass transistor output resistance models.

The pass transistor output resistance is formed from the parallel combination of the feedback resistors, R_{F1} and R_{F2}, the transistor output resistance, and the load resistance. Equation 25, using a current source load, and equation 26, using a resistor load, model the two forms of pass transistor output resistance.

$$R_{OUT} = (R_{O,pass} \,//\, R_{F1} + R_{F2} \,//\, R_{O,current}) \tag{25}$$

$$R_{OUT} = (R_{O,pass} \,//\, R_{F1} + R_{F2} \,//\, R_{L}) \tag{26}$$

Resistive loading decreases the output impedance with respect to a current source load, and effectively pushes the output pole to higher frequencies. Resistive loading was used for the simple uncompensated AC response but was later changed to a current source for the final design. The error amplifier was design to yield an overall gain of 100dB. Simulations showed

that the pass transistor provides roughly 20dB of gain at the zero load current condition. Thus, the error amplifier requires 80 dB of gain. The error amplifier was also design to produce the dominant system pole around 100Hz, yielding a gain-bandwidth product of 1MHz for a single pole system. Equation 27 exemplifies the procedure for determining R_1 and C_1.

$$C_1 = \frac{1}{R_1 p_1} = \frac{1}{10M\Omega \cdot (100Hz \cdot 2\pi)} = 0.159nF \tag{27}$$

R_1 was arbitrarily set to 10MΩ, forcing the effective error amplifier output capacitance, C_1, to 1.59nF. The error amplifier transconductance, g_{m1}, was determined by equation 28.

$$gm1 = \frac{A_{DC,error}}{R_1} = \frac{10{,}000V/V}{10M\Omega} = 1000\mu A/V \tag{28}$$

Finally, the pass transistor amplifier parameters were extracted from a BSIM3 simulation. Fig. 22 shows the simulation results. All the AC circuit parameters are tabulated in Table V.

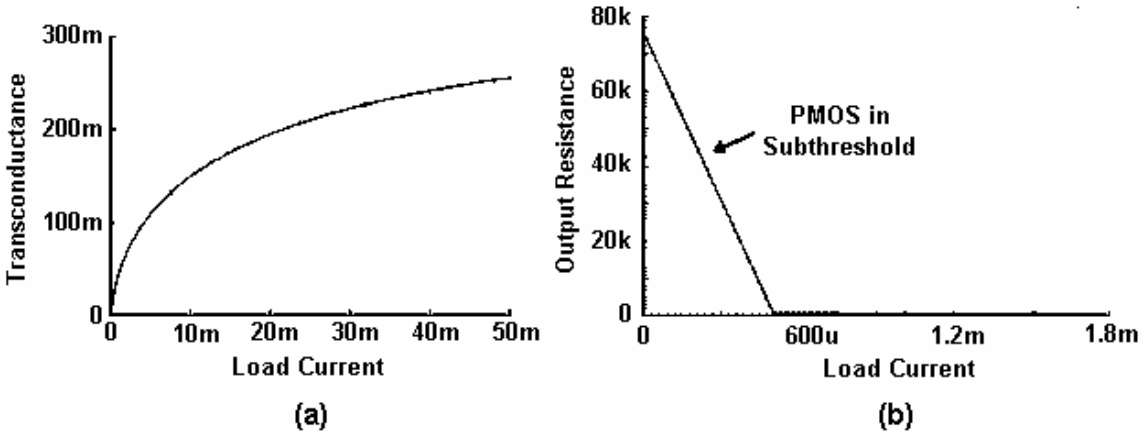

Fig. 22. Pass transistor load-dependent DC operating points: (a) transconductance (b) output resistance.

TABLE V

AC RESPONSE TEST CIRCUIT PARAMETERS

ERROR AMPLIFIER		PASS TRANSISTOR	
DC Gain	80 dB	W/L	16mm/400nm
Gm_1	1000μA/V	Gm	Variable
R_1	10MΩ	R_{out}	Variable
C_1	0.159nF	I_Q	5μA
Pole	100Hz	C_{OUT}	100pF
FEEDBACK		VOLTAGE LEVELS	
B	0.443	V_{REF}	1.24V
R_{F1}	312kΩ	V_{IN}	3.0V
R_{F2}	248kΩ	V_{OUT}	2.8V
C_{F1}	1pF	I_{OUT}	0 ~ 50mA

All the amplifier blocks were combined together to yield equation 29. A computer simulation determined the system poles and the AC Bode plots for various loading conditions. Fig. 23 illustrates the pole movement for the uncompensated capacitor-less LDO regulator. The AC bode diagram was simulated for both zero load current and a 50mA load current. The load dependent pass transistor gain adjusts the overall DC gain by roughly 10dB.

$$\frac{V_{out}}{V_{in}} = \left(\frac{g_{m1}R_1}{1+R_1C_1s}\right)\cdot\left(\frac{-g_{mp}R_{out}\left(1-s\frac{C_{gd}}{g_{mp}}\right)}{s(C_{out}+C_{gd})R_{out}+1}\right)\cdot\left(\frac{R_{F2}/(R_{F1}+R_{F2})}{1+s(R_{F1}//R_{F2})C_{F1}}\right) \tag{29}$$

In a single pole system, the DC gain adjustment changes the gain-bandwidth product. Very small load currents push the gain-bandwidth to higher frequency, increasing the difficulty in stabilizing the LDO regulator. Secondly, the output pole movement is very large. Thus, a pole-zero cancellation scheme becomes very tedious and cumbersome. Fig. 24 displays the pass transistor output pole and phase margin verses the LDO load current. The pass transistor output pole varies over several decades from 51kHz to 420MHz. This large variation in pole movement

causes large fluctuations in phase margin. Most of the variations are absorbed between zero load current and approximately 1mA of load current.

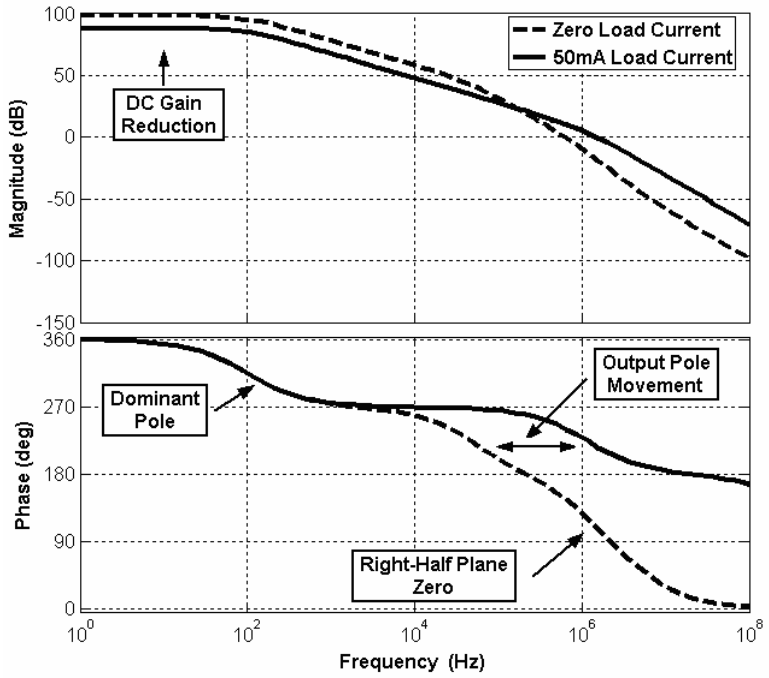

Fig. 23. Uncompensated LDO AC response.

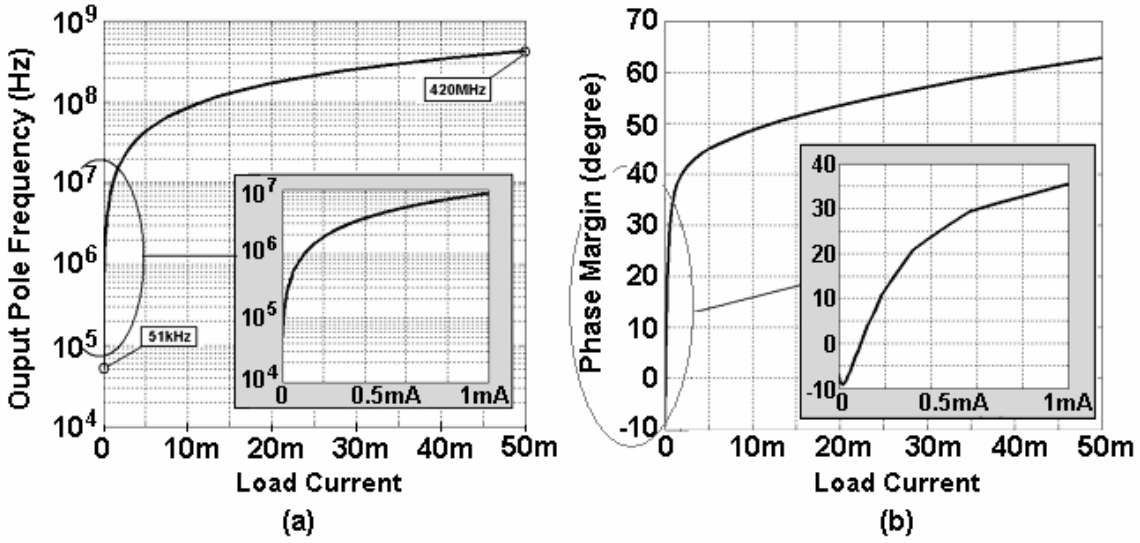

Fig. 24. Uncompensated LDO AC parameters verses I_{out}: (a) output pole frequency (b) phase margin.

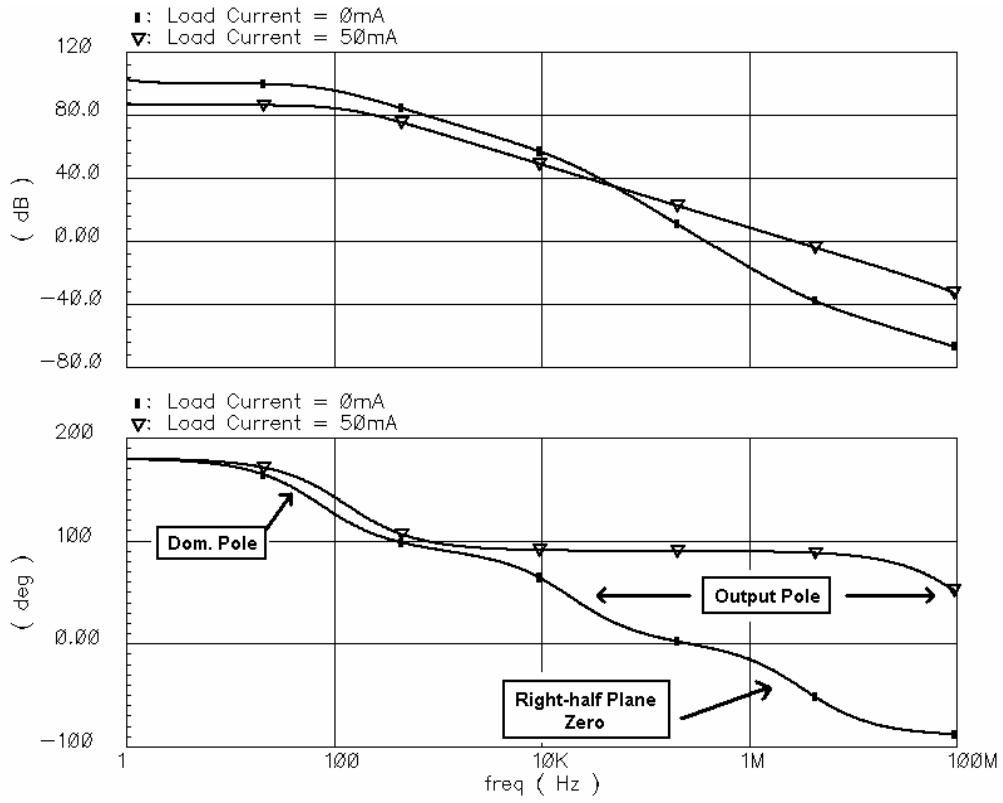

Fig. 25. Uncompensated AC response simulated in CADENCE.

The capacitor-less LDO regulator is inherently stable in the 1mA to 50mA range. The stability of the final capacitor-less LDO regulator took these facts into account. CADENCE simulations verify the mathematical models. Fig. 25 shows the uncompensated AC response simulated in CADENCE. Mathematical models and CADENCE simulations revealed three important load dependent AC characteristics. First, the LDO output pole moves with changing load conditions. Second, the DC loop gain decreases with increasing load current. Finally, a right-half plane zero created from the pass transistor parasitic capacitor, C_{GD}, increases in frequency with a corresponding increase in pass transistor transconductance. The variations are tabulated in Table VI. These properties were taken into account during the final capacitor-less LDO regulator design. Perhaps the most interesting discovery was the effects of the feed-forward zero. Conventional LDO regulator analysis ignores this feed-forward zero. The reason is related to the relative conventional LDO gain-bandwidth product, which typically ranges between 1kHz and 100kHz.

TABLE VI

LOAD DEPENDENT POLES AND ZEROS

PARAMETER	VARIANT	EFFECT OF INCREASED LOAD CURRENT	RANGE (0 ~ 50mA)
p_2 (output)	R_{OUT}	Increase	10kHz ~ 420MHz
z_1	g_{mp}	Increase	3.4MHz ~ 10GHz
A_{DC}	g_{mp}, R_{OUT}	Decrease	100dB ~ 92dB

Table VI shows that the feed-forward zero falls a decade past the typical LDO gain-bandwidth product, and therefore, does not typically surface during conventional LDO regulator analysis. The presented capacitor-less LDO regulator requires a gain-bandwidth product of 1MHz. At this frequency, the feed-forward zero has noticeable affects at low load currents.

3. Uncompensated Transient Response

The uncompensated capacitor-less LDO transient response showed the limitations of removing the large external output capacitor. The open-loop circuit shown in Fig. 17 was modified to a closed-loop circuit by removing the large inductor. A load current transient was introduced with an active load current mirror, shown in Fig. 26 with the transient response shown in Fig. 27.

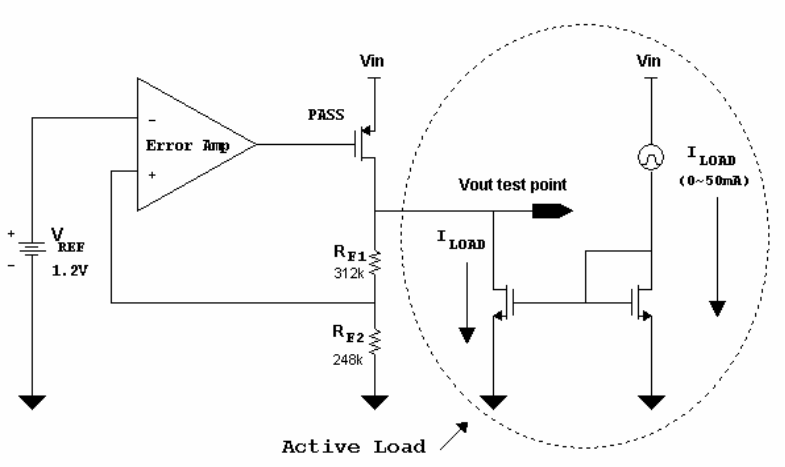

Fig. 26. Close-loop uncompensated LDO load transient test circuit.

Unfortunately, the uncompensated capacitor-less LDO regulator is inherently unstable at load currents below approximately 1mA. Above 1mA the capacitor-less LDO is stable and warrants a transient response investigation. Fig. 27 illustrates the problems associated with this type of LDO voltage regulator. The response was carried out with a 0 to 50mA square wave load current transient with 1μs rise and fall time. Clearly, the output voltage, bottom portion ofFig. 27, is unacceptable. The large voltage spikes are not due to a stability issue but are solely due to capacitor slewing at the gate of the pass transistor. The LDO output voltage can actually approach zero volts during a fast transient from 0mA to 50mA of load current. Pass transistor gate capacitor slewing requires the need of a fast transient path. Since the control loop contains the dominant low frequency pole at the output of the error amplifier, the large signal transient response suffers significantly. Results from this section lead to the initial capacitor-less LDO regulator research and development.

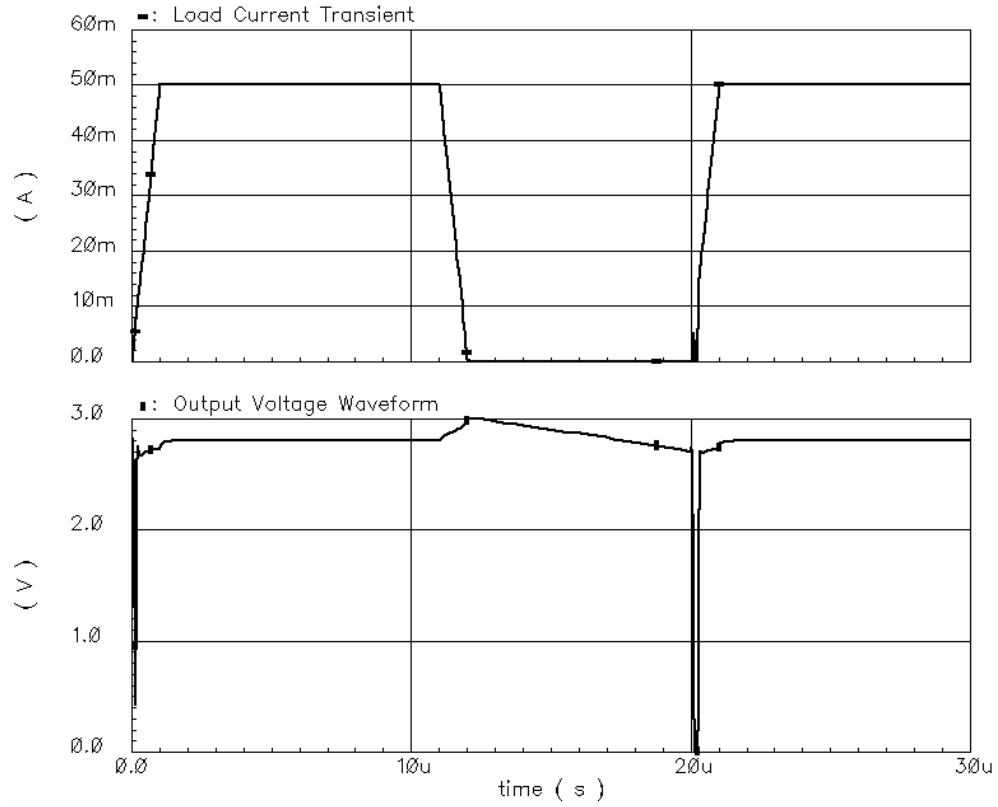

Fig. 27. 0 to 50mA load transient response.

B. Design Architecture Strategy

Capacitor-less LDO regulator research and development started with the results from the preliminary analysis. There were two major design considerations: transient response and regulator ac stability. The capacitor-less LDO has no beneficial value if only one of the design criteria was accomplished. This raised the question, were should the design process start. Intuitively, one would assume that stability is the foremost important LDO regulator attribute and that the design should first stabilize the circuit. This assumption, however, is the leading design flaw in most of the published professional papers with most designs having poor transient responses. The presented research strayed away from this approach and initiated the design with transient response in mind.

1. Transient Response Compensation

The pass transistor comprises the most important element in the LDO transient response. It supplies current to the load impedance and as a result develops the desired output voltage. Transistor gate capacitance acts as a current to voltage converter, and thus, has an equivalent propagation delay. The larger the gate capacitance is, the larger the propagation delay will be. In the case of the pass transistor, the effective input gate capacitance is extremely large. Fig. 28 illustrates the current to voltage conversion at the gate of the pass transistor.

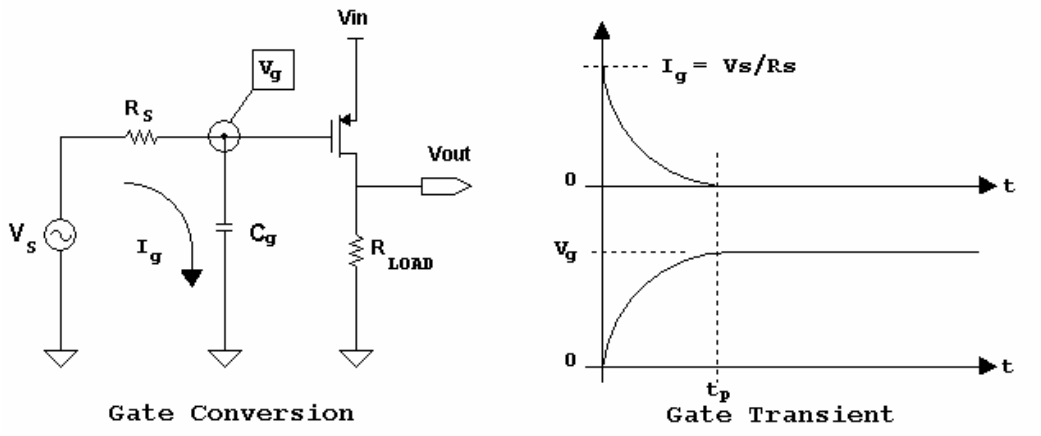

Fig. 28. Pass transistor gate transient effect.

Each transistor in the LDO voltage regulator had a propagation delay. The pass transistor contributes the most devastating propagation delay owing to the pass transistor gate capacitor slewing. The pass transistor can only supply the desired current to the load when the gate voltage, V_g, reaches steady-state after some time delay, t_p. The speed of the capacitor-less LDO voltage regulator is mainly determined by the pass transistor propagation delay, t_p, and not the gain-bandwidth product of the control loop.

Most LDO regulator designs attempt to reduce the source impedance, R_S, to increase the speed of pass transistor. Typically, a low output impedance buffer is used to drive the pass transistor [7]. This approach greatly improves the transient response in conventional LDO regulators were the external capacitor creates the dominant pole. The capacitor-less LDO voltage regulator does not have this luxury. The small internal output capacitor can not be used to create the dominant pole since the output pole resides at much higher frequencies. Thus, the dominant pole must be placed within the error amplifier control loop. The transient control signal must therefore propagate through a dominant pole before or at the gate of the pass transistor.

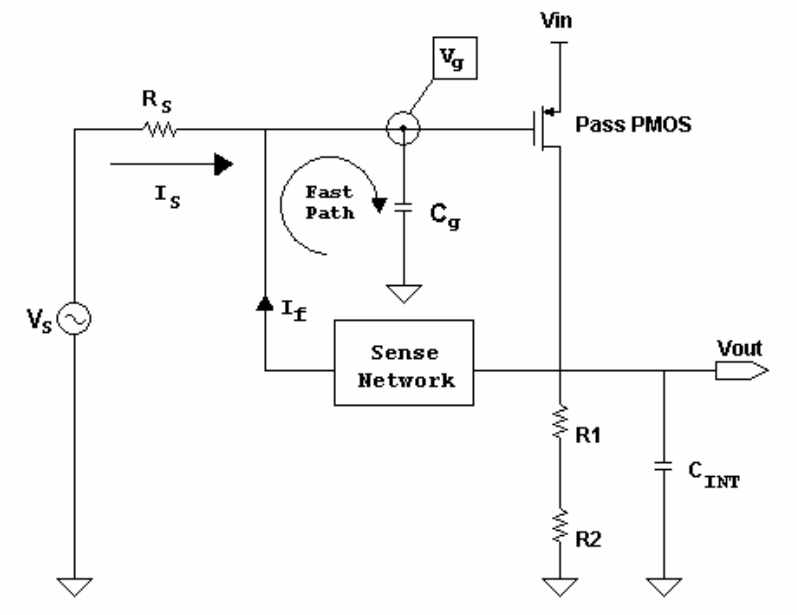

Fig. 29. Fast transient path general concept.

A new technique was needed to increase the speed of the pass transistor gate. The signal injected into the pass transistor gate capacitor is ideally a voltage. As shown in Fig. 28, the gate voltage is actually a secondary effect. Current must first flow into the gate capacitor. The gate capacitor then integrates the capacitor current to form the gate voltage. The fast path had to sense the change in output current with minimal delay and relay that information back to the pass transistor gate capacitor. This information had to be injected in the form of current, at the gate capacitor, in proportion to the change in output voltage. Fig. 29 shows the basic concept.

The ideal sensing network would relay the output voltage information to the gate capacitor without consuming any power or changing the DC operating points of the pass transistor. Several different topologies were developed for the sensing network. A differentiator sensing network, however, produced the best results. A basic capacitor differentiator is shown in Fig. 30.

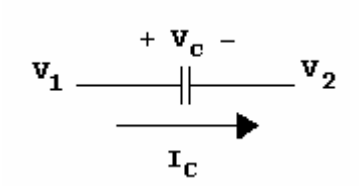

Fig. 30. Basic capacitive differentiator.

The differentiator senses any change in voltage difference between V_1 and V_2. Equation 30 equates the capacitor current to the two voltages.

$$i_C = C_f \cdot \left(\frac{v_1 - v_2}{dt} \right) \tag{30}$$

Fig. 27 showed that the worst case scenario is a large increase in load current, especially during fast load current transitions. The capacitor-less LDO output voltage sags due to the slow response of the control circuit and the pass transistor gate capacitance. The load demands a large

amount of current in short amount of time, but the pass transistor essentially acts as a constant current source shown in Fig. 25. If one end of the differentiator capacitor is attached to the output voltage node, the change in output voltage would induce a capacitor current proportional to the change in capacitor voltage. Fig. 31 shows the addition of the differentiating capacitor, C_f, and the typical uncompensated output voltage and output current waveforms. A capacitor current, I_f, is generated when the output voltage changes from the nominal 2.8V. The current through C_f is bi-directional, responding to both positive and negative voltage deflections. A coupling network was then designed to mirror this current into the pass transistor gate capacitor.

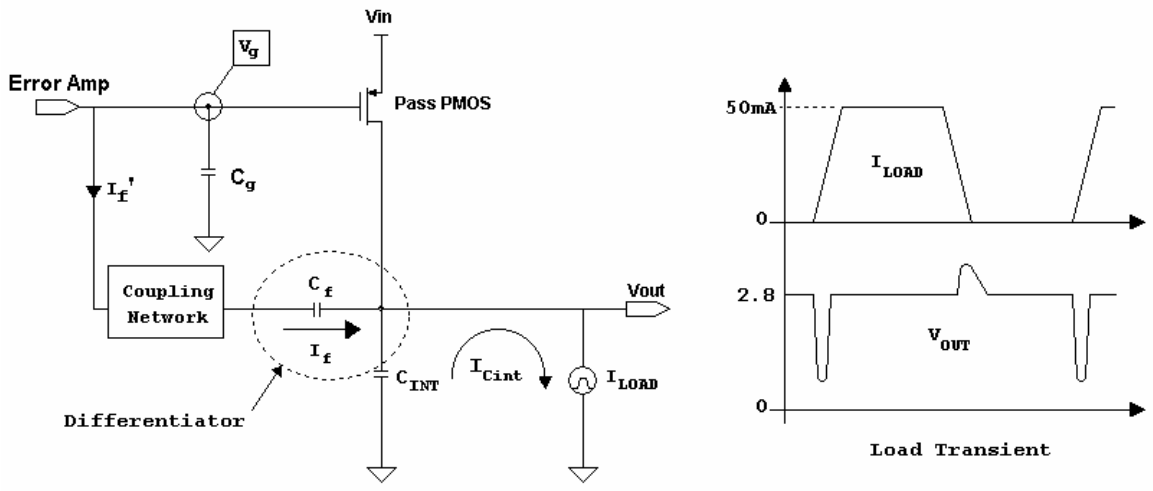

Fig. 31. Addition of differentiator fast path.

The speed of the differentiator is of particular interest. The instant the load demands current, both C_f and C_{INT} instantly respond by supplying current to the load. The output voltage is a secondary effect and does not change until charge is stripped away from C_f and C_{INT}. Thus, the capacitor current transient leads the output voltage transient. In essence, the differentiator capacitor predicts variations in the output voltage at the same time they exist, and the differentiator represents the fastest type of detector possible. The only limitation is the amount of current that can be supplied to differentiator capacitor. Ideally, the differentiator has an infinite bandwidth assuming that the voltage at the other capacitor terminal, V_1, remains constant

throughout the load current transient. If the voltage V_1 sags to an output voltage transient, the effect of the fast transient path is reduced.

The AC response of the differentiator is analyzed next. There were two different modes of operation, current mode and voltage mode. The differentiator in the voltage mode is referred to as an "AC coupled" connection and has a zero at 0Hz. Fig. 32 shows the voltage mode AC response from the output voltage to the coupling network, shown in Fig. 31.

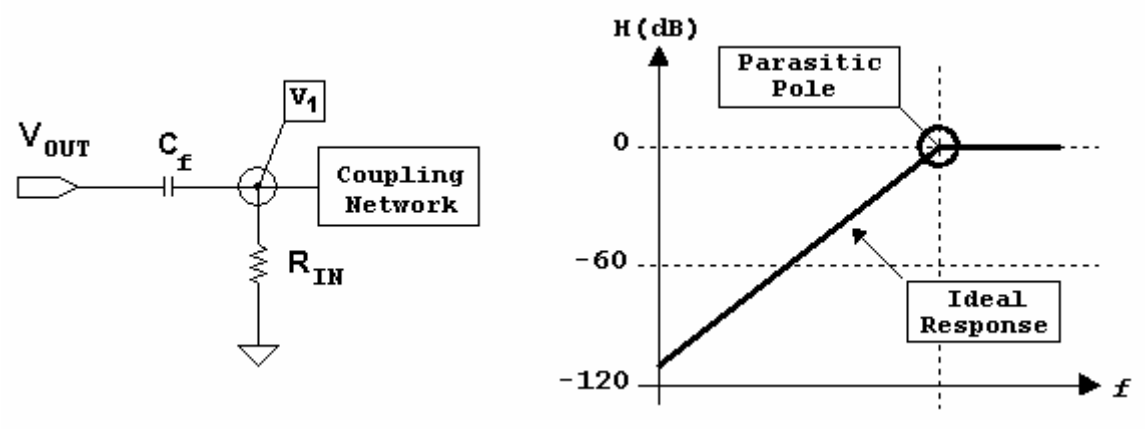

Fig. 32. Differentiator voltage mode AC response.

A parasitic pole was added to more realistic characterize the differentiator. An ideal differentiator has an ever increasing magnitude response since only a zero at dc should exist. The coupling network however will have some non-zero input impedance, introducing a pole into the system. Equation 31 expresses the voltage transfer function for the differentiator.

$$\frac{v_2}{v_{out}} = \frac{sC_f R_{IN}}{sC_f R_{IN} + 1} \tag{31}$$

The coupling network input impedance drastically affects the speed and fast transient response of the differentiator. The correct selection of C_f and the coupling network input impedance was

designed with careful consideration, placing the parasitic pole well passed the gain-bandwidth product.

C_f formed the load sensing mechanism, but the method to couple the sensed load variations posed the most difficult task. The coupling network forms a feedback loop, and the feedback loop gain must be negative. The most basic negative feedback coupling network is a straight wire, attaching the 2nd C_f node directly to the gate of the pass transistor, shown in Fig. 33. This method would work if C_f were made very large with respect to the pass transistor gate capacitance. There is one major problem with this approach, the pass transistor's RHP zero frequency is reduced.

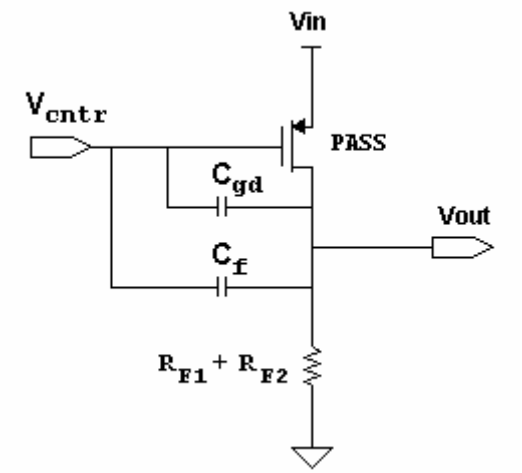

Fig. 33. Simplest coupling network.

Equation 32 reflects the addition of C_f to the pass transistor's right-half plane zero given in equation 23.

$$\omega_{z\,pass} = \frac{gmp}{C_{gd} + C_f} \tag{32}$$

The zero would move to much lower frequencies than the initial 3MHz, and would reside well within the gain-bandwidth product of the overall control loop. This would make the capacitor-less LDO regulator extremely hard to stabilize, if not almost impossible.

The previous analysis revealed an important design constraint; the coupling network must provide negative feedback only. The direct connection of C_f not only created a feedback path but also created an undesirable feed-forward path. Fig. 34 shows the proposed coupling architecture.

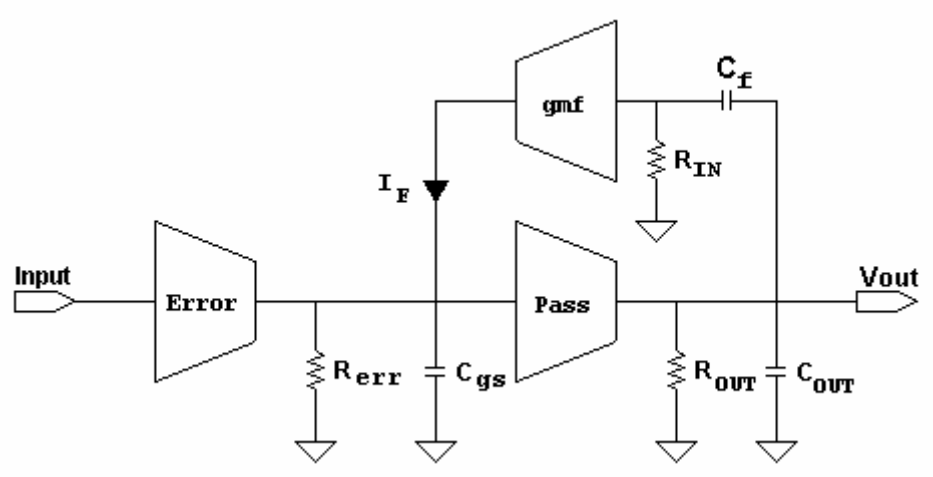

Fig. 34. Proposed coupling network.

Ideally, a current amplifier should be used to couple the output back to the pass transistor gate. Problems arise with the tradeoff between sufficient current gain and quiescent bias current. A current amplifier was replaced with a transconductance amplifier. The transconductance amplifier requires a voltage input, thus, a current to voltage conversion is needed, slowing down the response of differentiator. Nonetheless, the transconductance amplifier, g_{mf}, provided a negative feedback path while blocking the original feed-forward path. R_{IN} supplies the current for the differentiator capacitor and also provides the necessary current to voltage conversion.

The topology in Fig. 34 was analyzed to provide the appropriate level of feedback current gain. Fig. 35 shows the large signal capacitor and load charge analysis circuit. The goal of the pass transistor during a fast load current transient is to supply the load demanded

differential charge. Equation 33 relates the load demanded charge to the required pass transistor charge.

$$\Delta Q_{LOAD} = \Delta I_{LOAD} \cdot t_{R/F} = gm_{pass} \cdot \Delta V_{g,pass} \cdot t_{R/F} \tag{33}$$

The change in charge demanded by the load is quite obvious where $t_{R/F}$ is the rise or fall time of the current transient and ΔI_{LOAD} is the zero-load to full-load condition.

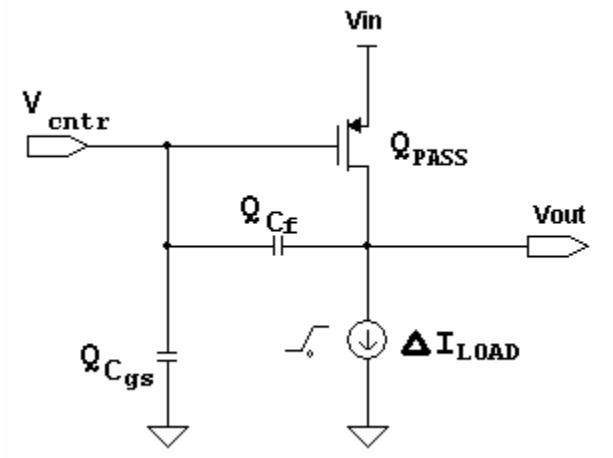

Fig. 35. Differentiator charge analysis.

The amount of charge required by the pass transistor is equal to the amount of current generated by its transconductance and the difference between the steady-state gate voltage required to regulate the output voltage for the low and high current transitions. The charge difference in the pass transistor could now be calculated based on the differential gate voltage, shown in Equation 34.

$$\Delta Q_{gs} = \Delta V_{g,pass} \cdot C_{gs} = \Delta I_{gs} \cdot t_{R/F} \tag{34}$$

The value of I_{gs} was substituted with the properties of coupling capacitor C_f yielding equation 35.

$$\Delta Q_{gs} = \Delta V_{g,pass} \cdot C_{gs} = \frac{C_f \cdot \Delta V_{OUT}}{t_{R/F}} \cdot t_{R/F} \tag{35}$$

The deflection voltage, Vg, was solved for in equation 35 and substituted into equation 34. Finally, equation 36 solves for C_f to determine the effective capacitance needed to minimize the output voltage transients.

$$C_f = \left(\frac{\Delta I_{LOAD}}{\Delta V_{OUT}}\right) \cdot \left(\frac{C_{gs}}{gm_{pass}}\right) = \left(\frac{50mA}{100mV}\right) \cdot \left(\frac{26pF}{365e-6}\right) = 35nF \tag{36}$$

Ironically, equation 36 does not contain any transition times. This is due to the ideally infinite bandwidth of a capacitor. An introduced pole in the differentiator will however produce a finite bandwidth system, and the output voltage deflections will increase. Equation 36 shows that the required size of C_f is proportional to the load current variations and the effective size of the pass transistor gate capacitance. On the other hand, C_f is inversely proportional to the desired output deflection voltage and the inherent transconductance of the pass transistor.

C_f was calculated based on the proposed design specifications. The output voltage deflection was set to 100mV for a load current variation of 50mA. The pass transistor transconductance was set to the lowest value, for a zero-load current condition, and C_f was found to be 35nF. The required 35nF is too large to integrate on chip if the capacitor, C_f, was directly connected between the output and the pass transistor gate. The proposed topology alleviates the requirement of a large internal compensation capacitor by introducing a transconductance gain amplifier, gm_f. The gm_f amplifier increases the effective size of C_f by the voltage gain of the amplifier or Miller effect. Thus, C_f can be made much smaller than the required single 35nF value. Equation 37 shows the affect of the added gm_f amplifier shown in Fig. 34.

$$\frac{v_g}{v_{out}} = \frac{s \cdot R_{IN} \cdot (C_f gm_f R_{err})}{(sR_{IN}C_f + 1)(sR_{err}C_{gs} + 1)} \tag{37}$$

The effective coupling capacitance, C_f, is then defined in equation 38. The poles in equation 37 were ignored at this point; the equivalent capacitor is computed as:

$$C_{f.eff} = C_f gm_f R_{err} = C_f \cdot A_{v,gmf} \tag{38}$$

Thus, the voltage gain of the gm_f amplifier was designed to yield the desired 35nF effective coupling capacitance but differ from the technique used in [9]. Typically gain values range between 40dB to 80dB with coupling capacitors in the range of 2pF to 15pF depending on the maximum desired output voltage transient. A noteworthy property is the variation in required coupling capacitance with respect to the change in pass transistor transconductance; the zero-load condition requires much more coupling capacitance due to the very small transconductance induced by the pass transistor dc operation point.

2. AC Stability Compensation

The fast transient path was created using a differentiator. Stabilizing the new capacitor-less LDO architecture is the next design stage. Components of the feedback network were analyzed, but the complete AC transfer function was overlooked when designing the large signal compensation. The overall control loop stability was the major concern, and the transfer function was synthesized for basic circuit shown in Fig. 36. Equation 39 represents a simplified version of the overall open-loop transfer function; the differentiator's parasitic poles are removed to simplify the analysis.

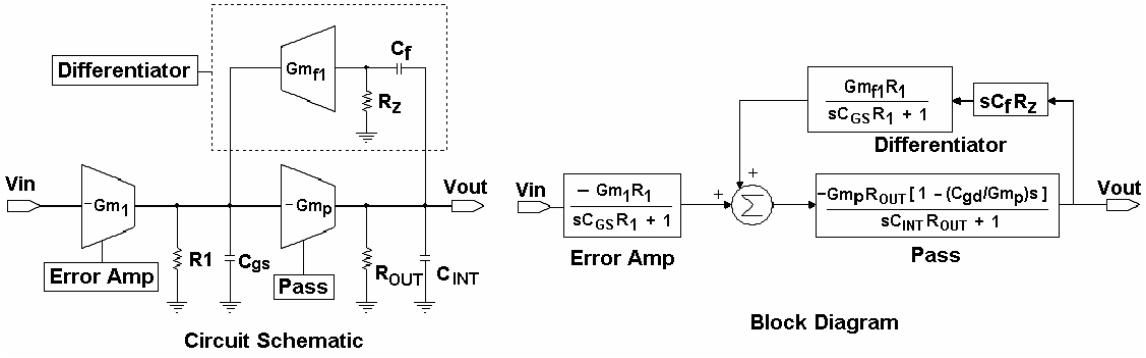

Fig. 36. Proposed topology: simplified circuit diagram.

The parasitic pole at $1/R_zC_f$ is ignored in this expression since it should be placed well above the loop's unity gain frequency.

$$\frac{v_{out}}{v_{in}} = \frac{(Gm_1R_1)\cdot(Gm_PR_{OUT})\left(1 - s\frac{Cgd}{Gm_p}\right)}{(sC_{GS}R_1 + 1)(sC_{INT}R_{OUT} + 1) + (sC_fR_zGm_{f1}R_1Gm_PR_{OUT})\left(1 - s\frac{Cgd}{Gm_p}\right)} \tag{39}$$

Equation 39 sheds light on the ideal affect of the differentiator and the use of a quasi-Miller compensation. The pole locations can be simplified by assuming the $C_fR_fA_{diff} \gg C_{INT}R_{OUT}C_{gs}R_1$ and are given in Equation 40 – 42.

$$\omega_{P1} = \omega_{P\,dom} \approx \frac{1}{C_fR_fA_{diff}} \tag{40}$$

$$\omega_{P2} \approx \frac{C_fR_fGm_{f1}Gm_p}{C_{INT}C_{gs}} \tag{41}$$

$$\omega_{Z1} = -\frac{Gm_p}{Cgd} \tag{42}$$

where $A_{diff} = Gm_{f1}R_1Gm_pR_{out}$. The differentiator splits the poles located at the input and output of the pass transistor. High differentiator gain ensures sufficient distance between the two poles to yield a stable AC response.

The macromodel of the final proposed solution is shown in Fig. 37 and adds additional circuitry from that of Fig. 36. The compensating differentiator is composed by the integrator and an additional amplifier Gm_{f2} to boost the feedback gain, resulting in higher equivalent capacitance. The input resistance is also modified from Fig. 36, reflecting the final transistor-level implementation, where R_Z is replaced with R_f. Unfortunately, the differentiator contains parasitic poles arising from the parasitic devices C_2 and R_f that affect the overall behavior of the AC stability, but they do not compromise the basic properties of the Miller pole splitting technique. Fig. 37 also adds a second error amplifier stage to emulate the final circuit implementation.

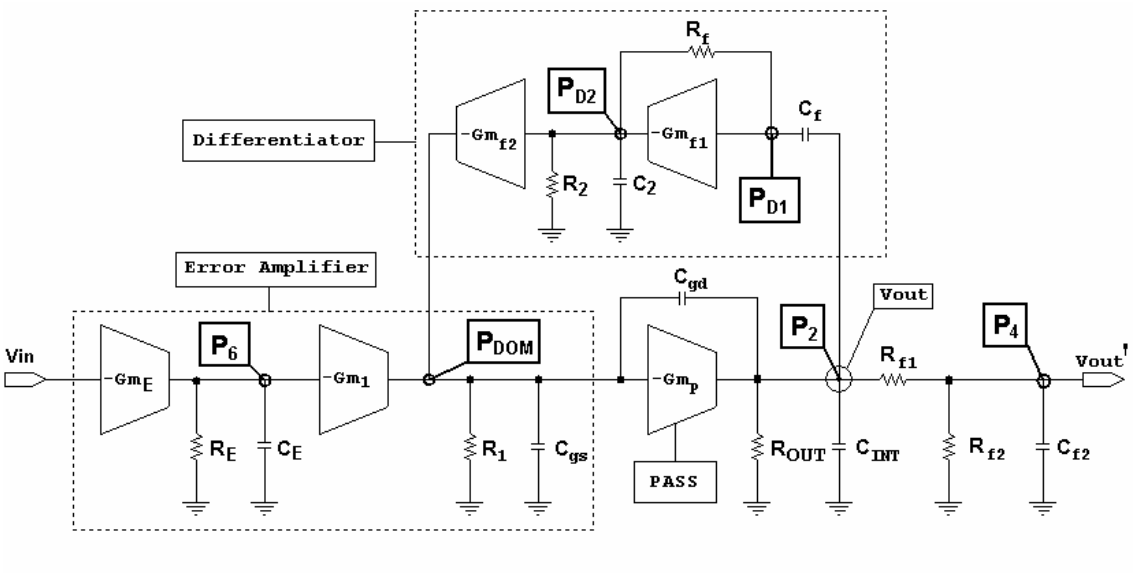

Fig. 37. Proposed capacitor-less LDO voltage regulator: Open-loop schematic.

The differentiator's parasitic poles have an important influence on the loop stability. Nodal analysis took all parasitic impedances into account to accurately model the final transistor-level design. Fig. 38 shows the circuit used to model the differentiator.

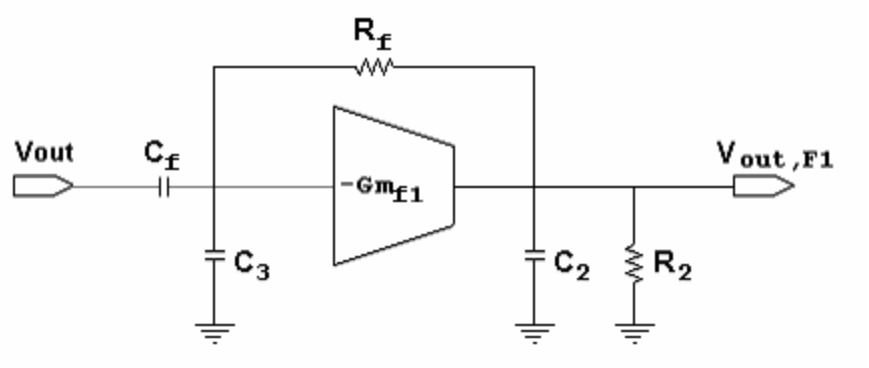

Fig. 38. Differential equivalent circuit diagram.

The voltage transfer function was determined for the circuit. Equation 43 shows the exact transfer function with out any simplifications.

$$\frac{v_{out,f1}}{v_{out}} = \frac{sC_f(g_{mf1}R_f - 1)R_2}{s^2R_fR_2C_fC_2 + s\cdot[C_f(R_f + R_2) + C_2R_2] + g_mR_2 + 1} \tag{43}$$

Several simplifications were used to reduce the transfer function complexity and expose the critical circuit elements. The simplifications are shown in Table VII.

TABLE VII

DIFFERENTIATOR SIMPLIFICATIONS

STEP	SIMPLIFICATION
1	$C_f >> C_2$
2	$[C_f(R_f + R_2) + C_2R_2]^2 >> 4\cdot R_fR_2C_fC_2\cdot[g_mR_2 + 1]$

The significant poles can be extracted from equation 44 and approximate locations can be found using the approximation in Table VII.

$$s = [C_f(R_f + R_2) + C_2R_2] \pm \frac{\sqrt{[C_f(R_f + R_2) + C_2R_2]^2 - 4 \cdot R_f R_2 C_f C_2 \cdot [g_m R_2 + 1]}}{2 \cdot R_f R_2 C_f C_2} \quad (44)$$

The high frequency transient response is solely determined by the location of the differentiator parasitic poles. Both poles were pushed out to the highest possible frequencies; however, other constraints limit the magnitude of the pole frequencies. The first parasitic pole, P_{D1}, shown in Fig. 39, was the most critical pole and to ensure good transient response, was located just past the gain bandwidth product. The parasitic poles also play an important role in the overall capacitor-less LDO stability.

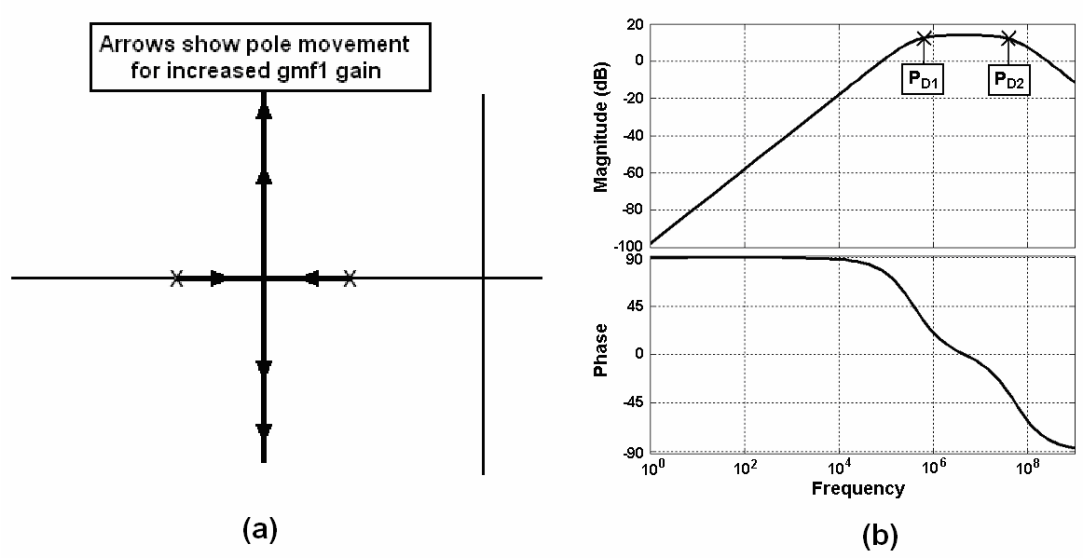

Fig. 39. (a) General differentiator pole movement with gm_{f1} (b) Differentiator open-loop AC response.

The differentiator's open-loop parasitic pole locations, ω_{PD1} and ω_{PD2}, are shown in equation 45 and 46. The differentiator's parasitic poles have an adverse effect when the loop containing both the differentiator and the pass transistor stage is closed.

$$\omega_{PD1} \approx \frac{1 + Gm_{f1}R_2}{C_f \cdot (R_f + R_2)} \tag{45}$$

$$\omega_{PD2} \approx \frac{1}{C_2(R_2 // R_f)} \tag{46}$$

Cardano's method [13] is used to decompose the 3rd order function in equation 47 into its roots, revealing one real pole and a complex pair given the value of its discriminant in equation 48.

$$(sR_{out}C_{INT} + 1) \cdot (s^2 R_f R_2 C_f C_2 + s \cdot [C_f (R_f + R_2) + C_2 R_2] + g_m R_2 + 1) + A_{diff} \tag{47}$$

$$\Delta \approx 4 \cdot A_{diff} \cdot \left(\omega_{pD1} \cdot \omega_{pD2} \cdot \omega_{POUT}\right) >> 1 \tag{48}$$

This discriminant moves closer to 1 as the load current increases, indicating that complex pole pair has a growing real component with larger load currents. The loop analysis does not contain ω_{Pdom} since this pole location is virtually unaffected by the differentiators parasitic poles, ω_{PD1} and ω_{PD2}. Fig. 40 shows the complex pole movement verses load current and the adverse effects ω_{PD1} and ω_{z1} which push or pull the complex pole pair into the right-half plane where the AC response becomes unstable. The root locus of Fig. 40 and ones hereafter represent the negative or 0˚ root locus [14], reflecting the special case when having a RHP zero. Thus, the normal rules for the root locus are reversed. The locations of the complex poles, ω_{P5}, and ω_{P6} are given in equation 49 – 51.

$$\omega_{Complex} \approx \omega_{P2} \tag{49}$$

$$\omega_{P5} \approx \omega_{PD2} \tag{50}$$

$$\omega_{P6} = \frac{1}{C_E R_E} \tag{51}$$

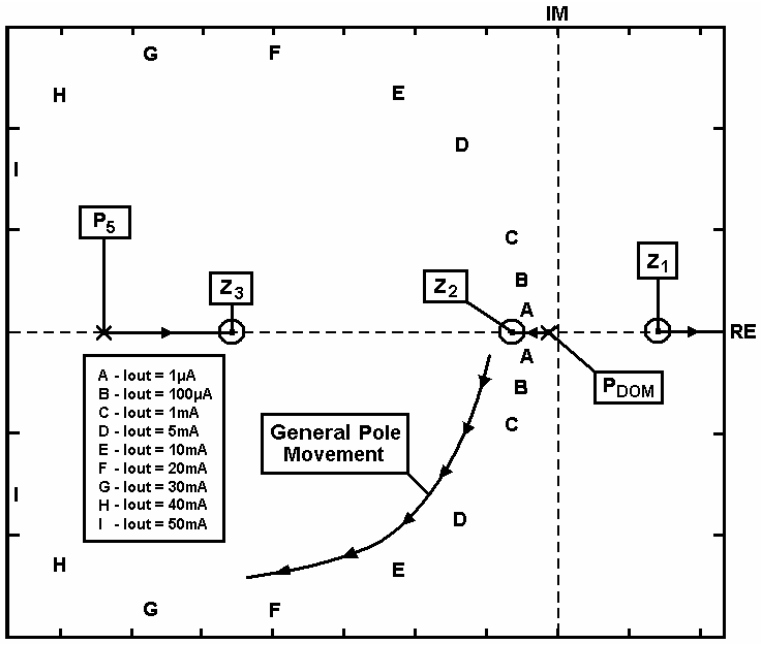

Fig. 40. Differentiator closed-loop pole movement with changing load current.

Fig. 41 shows the block diagram equivalent of the overall open-loop transfer function, where H_1 and H_2 represent the two-stage error amplifier, H_3' contains the closed-loop differentiator poles, and β represents the feedback gain factor formed from R_{F1} and R_{F2}. The closed-loop differentiator poles, P_5 and $P_{COMPLEX}$, represent the start of the open-loop poles for main control loop open-loop transfer function, shown in Fig. 42. The block diagram in Fig. 41 can be used to plot the all closed-loop pole locations and their movement verses load current and overall feedback gain for the capacitor-less LDO regulator.

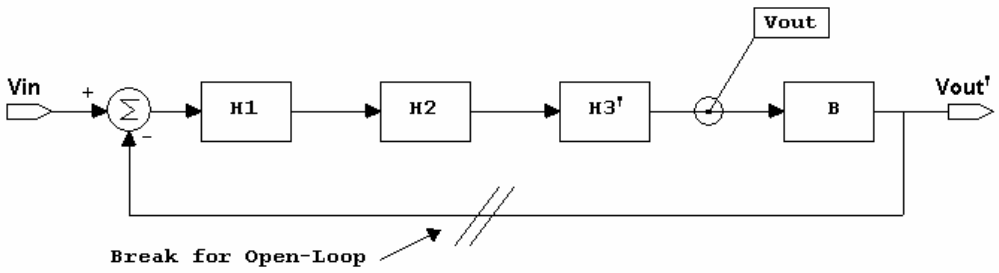

Fig. 41. Modified block diagram.

For each new load current level, a new root locus must be generated for the changes in overall feedback gain. Thus, Fig. 42 represents a two-dimensional root locus which arises from having two feedback loops in the entire system, one for the differentiator loop and one for the overall steady-state control loop.

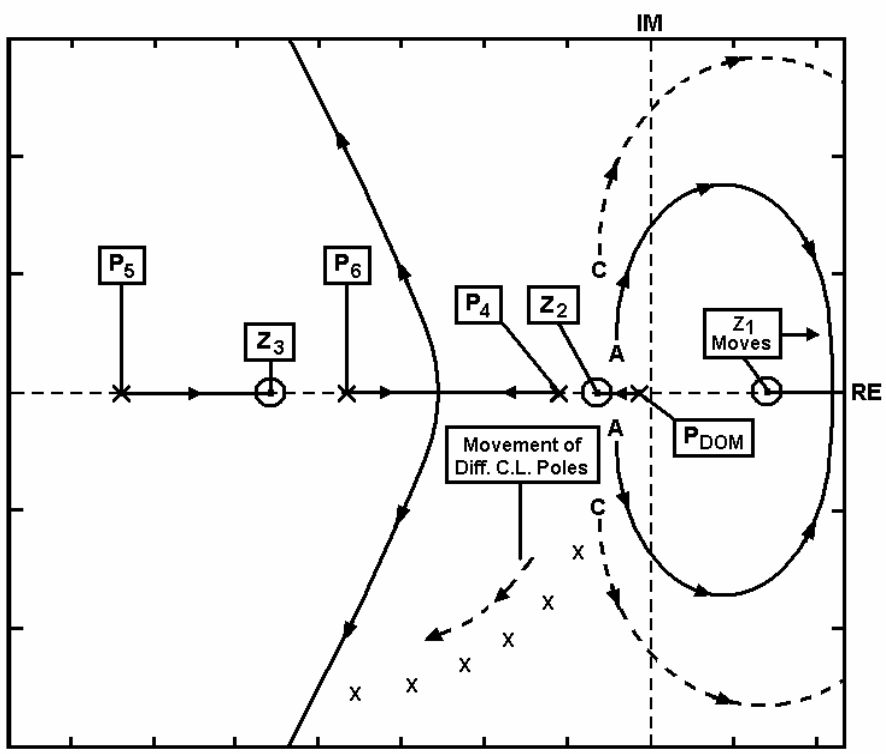

Fig. 42. Complete root locus showing closed-loop pole movement for both load current variations and feedback factor, β.

Fig. 42 shows that the imaginary axis forms a stability boundary for the differentiator's closed-loop complex poles. If the complex poles start in RHP as in Fig. 43, they will never leave the RHP in full closed-loop operation. Thus, the complex poles in Fig. 40 should never cross the imaginary axis. The condition for which there will be no RHP complex poles can be derived from equation 52 showing the differentiator's closed-loop transfer function in terms of poles and zeros. The zero, $\omega_{p,gate}$, is not shown in Fig. 40 since it is mathematically canceled by the error amplifier pole.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_{gmp}(1-s/\omega_{Z1})(s/\omega_{PD1}+1)(s/\omega_{PD1}+1)(s/\omega_{P,gate}+1)}{(s/\omega_{PD1}+1)(s/\omega_{PD2}+1)(s/\omega_{P,OUT}+1)(s/\omega_{P,gate}+1)+(s/\omega_{Z,diff})(1-s/\omega_{Z1})A_{loop}} \quad (52)$$

The RHP zero, ω_{Z1}, adds a negative s^2 term to the capacitor-less LDO's characteristic equation, allowing for the formation of two RHP poles. In this case, the two RHP poles will be complex. Equation 53 represents the condition to keep the complex poles in the LHP.

$$\left(\frac{\omega_{PD1}(\omega_{PD2}+\omega_{P,OUT}+\omega_{p,gate})+\omega_{PD2}(\omega_{P,OUT}+\omega_{p,gate})+\omega_{P,OUT}\omega_{p,gate}}{\omega_{P,OUT}\omega_{p,gate}\omega_{PD1}\omega_{PD2}}\right) > \left(\frac{\omega_{Z,diff}A_{loop}}{\omega_{Z1}}\right) \quad (53)$$

Equation 53 shows that the poles of the differentiator loop must be increased as much as possible or that the RHP zero, ω_{Z1}, much be increased. Since ω_{Z1}, $\omega_{P,OUT}$, and $\omega_{p,gate}$, are constrained by the size of the pass transistor, ω_{PD1} and ω_{PD2} must be pushed out to the highest possible frequencies.

Fig. 40 and Fig. 42 show that the differentiator feedback path also creates additional left-half plane zeros, located at the nodes that do not touch the feed-forward path. The most critical zero, ω_{z2}, is created by the differentiator's lowest frequency open-loop pole, $\omega_{PD1,}$ and typically resides around the LDO's unity gain frequency. C_{f2} was added outside the differentiator loop, creating an additional pole to cancel ω_{z2}. Equation 54 shows the desired selection of C_{f2}.

$$\omega_{Z2} \approx \frac{1+Gm_{f1}R_2}{C_f\cdot(R_f+R_2)} = \omega_{P4} = \frac{1}{C_{f2}\cdot(R_{F1}//R_{F2})} \quad (54)$$

The second closed-loop differentiator LPH zero, ω_{z3}, is not critical and rests well above the capacitor-less LDO's unity gain frequency with the second error amplifier pole, ω_{p6}, canceling its effect.

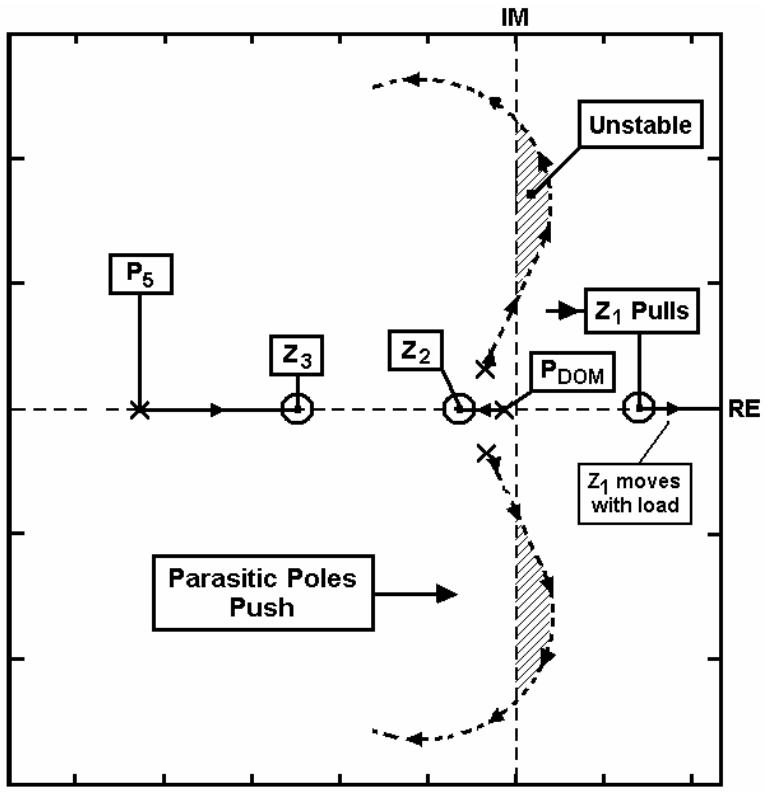

Fig. 43. Stability constraint for the differentiator's complex close-loop poles

The AC compensated capacitor-less LDO regulator has a Bode plot that resembles a first-order transfer function up to the complex conjugate pole pair, shown in Fig. 44. The approximate phase margin is given by equation 55. As R_{OUT} increases, the phase margin decreases, indicating that the worst phase margin occurs at the no-load condition.

$$PM \approx 90 + \tan^{-1}\left(\frac{A_{DC} C_{INT} R_{OUT} C_{GS} R_1}{(C_f R_f)^2 A_{diff}^2}\right) \tag{55}$$

AC stability requires that the complex pole pair does not cross the s-plane's imaginary axis, or the magnitude peaking of the complex conjugate pair does not peak over the 0dB threshold.

Both these problems are remedied by placing ω_{P5} at the highest possible frequency. The next section describes ω_{P5} placement and other methods to reach an optimized capacitor-less LDO regulator design.

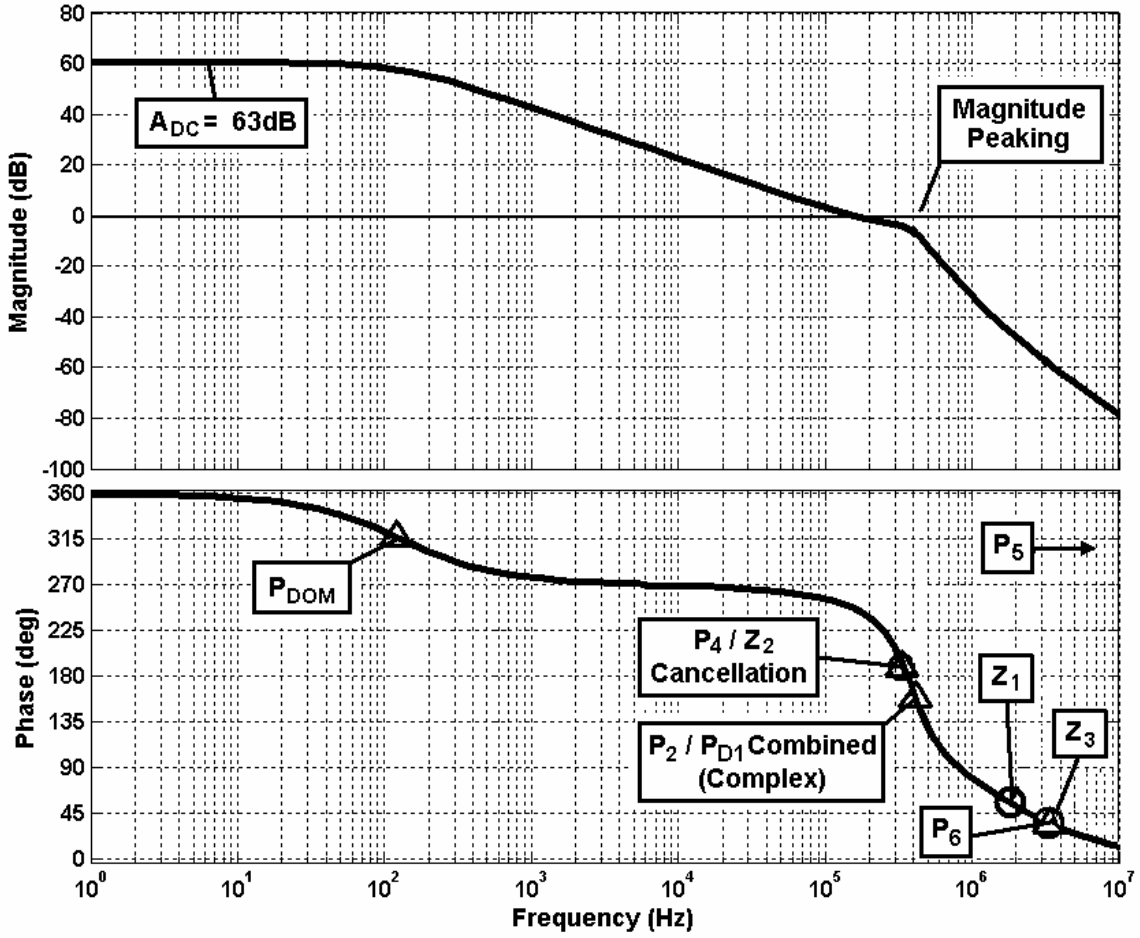

Fig. 44. MATLAB simulation: Open-loop AC response for I_{OUT} = 0mA.

III. TRANSISTOR-LEVEL DESIGN AND SIMULATION

The final transistor-level design is shown in Fig. 45 with a step-by-step design procedure illustrated in Table VIII. The design starts with the required dropout voltage, V_{DROP}, and the maximum current at dropout, I_{MAX}, which define the parameters of the pass transistor. The design then defines the differentiator parameters, followed by the error amplifier parameters, and ends with the selection of compensation capacitors, C_{f2} and C_{f3}.

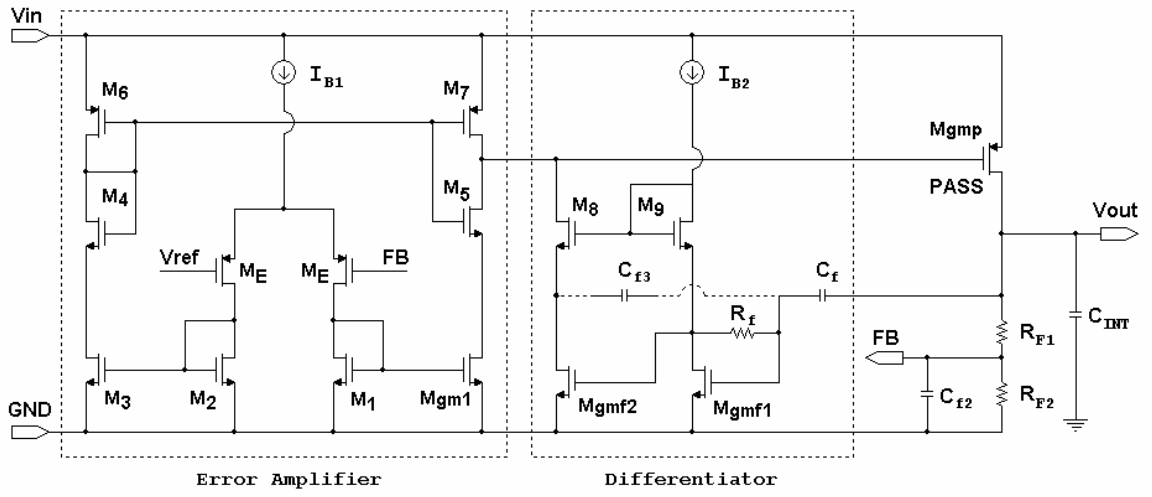

Fig. 45. Proposed capacitor-less LDO transistor-level design.

The differentiator is designed to yield the desired transient response while stabilizing the overall system transfer function. The input and output nodes of M_{gmf1}, forming the first stage amplifier in the inverting differentiator, are the most critical nodes. Enough gain must be developed to provide a sufficient transient response while generating very small parasitic capacitors to push the generated poles, ω_{PD1} and ω_{PD2}, to high frequency. Thus, the tradeoff between stability and transient response remains the most difficult design problem, and several iterations of the design procedure in Table VIII may be required.

TABLE VIII

DESIGN GUIDE

STEP	PARAMETER	CONSTRAINT	FINAL VALUE
1	Pass transistor	V_{DROP}, I_{MAX}	C_{GS} = 26pF, C_{GD} = 26pF Gm_p = 320uA/V
2	C_{INT}	Area	100pF
3	R_{OUT}	Area, power	280kΩ
4	A_{diff}	Equation 53, 55	~ 60dB
5	C_f	Equation 36, 38	2pF
6	R_f	ω_{PD1} > GBW	200kΩ
7	$Gm_{f2}\cdot R_2$	A_{diff}-A_{pass}-Agm_{f1}	~ 30dB
8	A_{DC}	Gain margin	≤ 68dB
9	Gm_E, Gm_1	A_{DC}-A_{pass}	~ 40dB
10	C_{f2}	Equation 54	1pF
11	C_{f3}	Trial and error	2pF

The inverting differentiator then sums into the error amplifier output through transistors M_{gmf2} and M_8. Resistor, R_f, performs three main tasks: transforms the current supplied by the capacitor, C_f, into a voltage during load current transients, provides the dc bias for both M_{gmf1} and M_{gmf2}, and helps to lower the differentiator's input impedance pushing the associated pole, ω_{PD1}, beyond the loops unity gain frequency.

A three-current mirror operational transconductance amplifier, M_1-M_7, M_E, and M_{gm1}, forms the error amplifier. The low impedance internal nodes of the three-current mirror OTA drive the parasitic poles out to high frequencies; well pass the desired gain-bandwidth product. The error amplifier's parasitic poles do not significantly affect the performance of the regulator as long as they are at least 2 to 3 times greater than the gain bandwidth product, and error amplifier can therefore be designed to meet any desired parameter such as the output noise, power consumption, and dc gain [2],[3],[5],[6],[8], and [9]. DC gain is the only stability constraint on the error amplifier, forced by the desired gain margin or the magnitude difference between the worst case complex pole magnitude peak and unity gain. This gain margin is a function of load current, and retains it lowest value in the load current range of 0mA to 5mA. The gain is adjusted by changing Gm_E and Gm_1, and typical ranges between 40dB and 60dB.

Each stage of the capacitor-less LDO regulator is biased from a current mirror: any inaccuracies and mismatches will cause large DC offsets at the output. M_4, M_5, M_8, and M9 are added to reduce the systematic offsets due to the drain-source voltage on M_1-M_3, M_{gm1}, M_{gmf1},

and M_{gmf2} and increase the current mirror accuracy as V_{IN} is increased. I_{B1} and I_{B2} currents are generated from an accurate internal reference.

Compensation capacitor, C_{f3}, in the range of 1 to 2 picofarads, is only used to improve the AC stability. C_{f3} uses the Miller effect to push the lowest frequency pole out to higher frequencies, and placed in positive feedback, shown in Fig. 45, pushes the pole at the input of the differentiator, ω_{PD1}, out to higher frequencies. C_{f3} does hinders the transient response of the differentiator, introducing slewing and discharging artifacts, and should only be used when the input pole causes the complex poles to enter the right-half plane. The final circuit parameters are given in Table IX with a spice simulated open-loop AC response shown in Fig. 46. The final capacitor-less LDO design had full range stability with a gain-bandwidth product of roughly 260kHz and phase margin greater than 80 degrees.

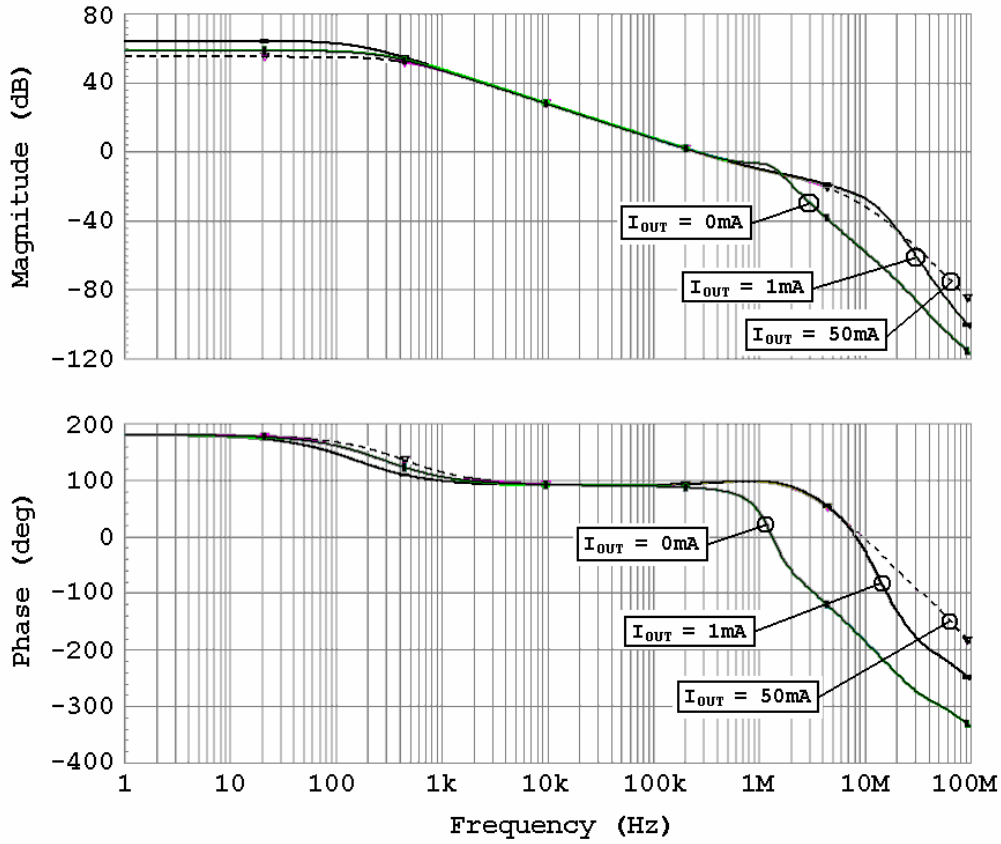

Fig. 46. Spice simulation: Transistor-level open-loop AC response.

TABLE IX

FABRICATED CIRCUIT PARAMETERS

TRANSISTOR	W(μm)	L(μm)	I_D(μA)	V_{REF}	1.24V
M_E	20	2	7.5	C_f	2pF
M_1, M_2	1	2	7.5	C_{f2}	1pF
M_3, Mgm_1	2	2	5	C_{f3}	2pF
M_4, M_5	5	2	5	R_f	200kΩ
M_6	2.9	2	5	R_{F1}	156kΩ
M_7	20.3	2	35	R_{F2}	124kΩ
M_9,Mgm_{f1}	3	0.4	30	C_{INT}	100pF
M_8,Mgm_{f2}	1	0.4	10	I_{B1}	5μA
PASS	16000	0.4	10	I_{B2}	10μA

A. Transistor-level Simulations

The design of the capacitor-less LDO voltage regulator sought to meet several initial parameters. Each pin of the LDO regulator affected several design constraints owing to the large number of simulations presented. The simulations are divided by the type of parameter, namely open-loop AC response, steady-state parameters, dynamic state parameters, and high frequency parameters.

1. Open-loop AC Response

The open-loop capacitor-less LDO voltage regulator's AC response was simulated at the transistor-level. The results are shown in Fig. 47 for 5 low output current conditions.

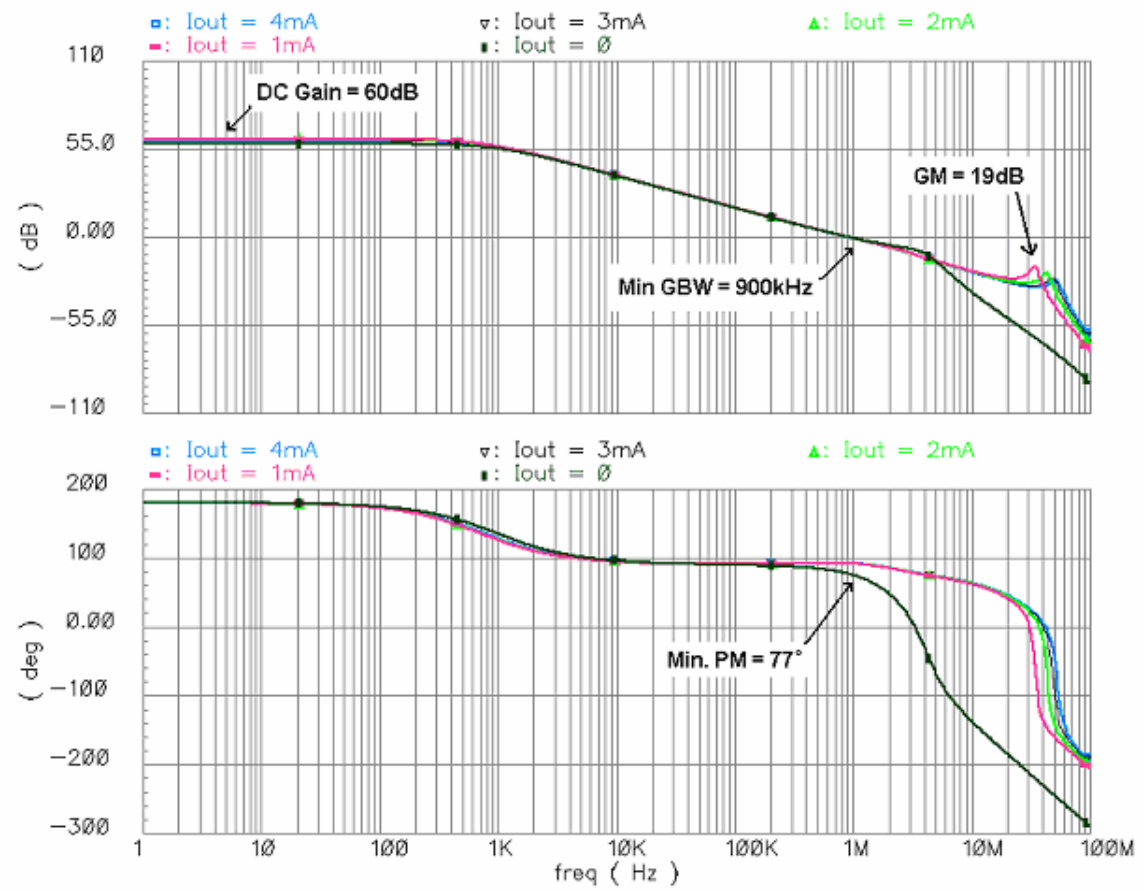

Fig. 47. Low output current open-loop AC response for I_{out} = 0 ~ 4mA.

The basic properties are illustrated with labels. First, the DC gain resides at roughly 60dB at low output currents. Next, the phase margin drops off at the zero-load current condition. This is due to the output pole moving to its lowest frequency as well as the right-half plane zero. More differentiator gain was required to push the complex poles out to higher frequency, regaining the loss in phase margin. The gain-bandwidth product was set at roughly around 900 MHz, but could have been lower since the GBW does not greatly affect the proposed LDO transient response; the transient response is determined by the fast transient path. Peaking did start to occur around 1mA. The gain margin of at least 10dB was desired and met, set by the value of C_{f2} or the added compensation capacitor at the feedback resistor node.

The ac response was also simulated over the entire range to verify that the capacitor-less LDO was indeed stable over the entire range. Fig. 48 shows the results.

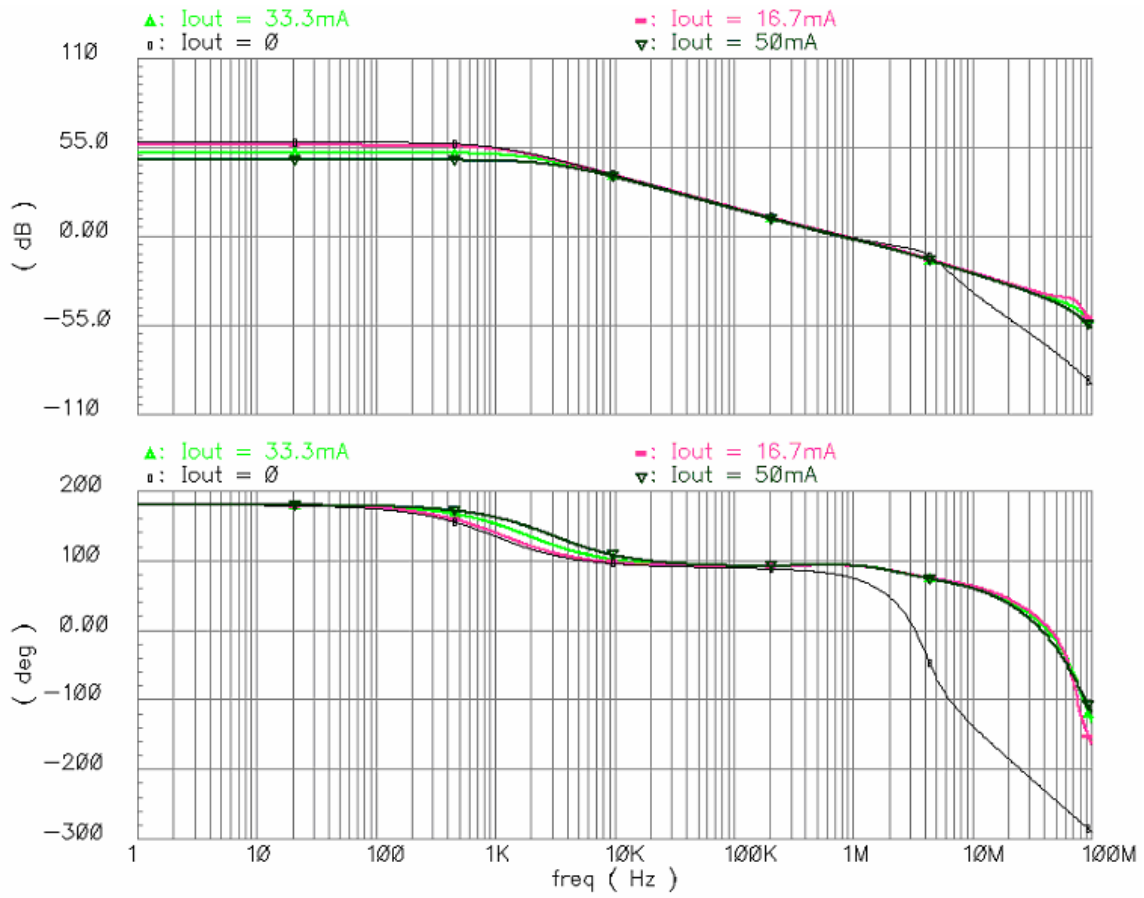

Fig. 48. Full range open-loop AC response for I_{out} = 0 ~ 50mA.

At higher currents, above 1mA, the capacitor-less LDO acts as a first order system with roughly 90 degrees of phase margin. Also, the gain-bandwidth remains relatively constant over the entire current range. This phenomenon is due to the corresponding reduction of gain verses the increasing dominant pole.

Both Fig. 47 and Fig. 48 represent the nominal ac response, excluding process variation and component mismatch. AC simulations were also used to find the range of compensation capacitance, C_f, and compensation resistance, R_f, that yields stable operation.

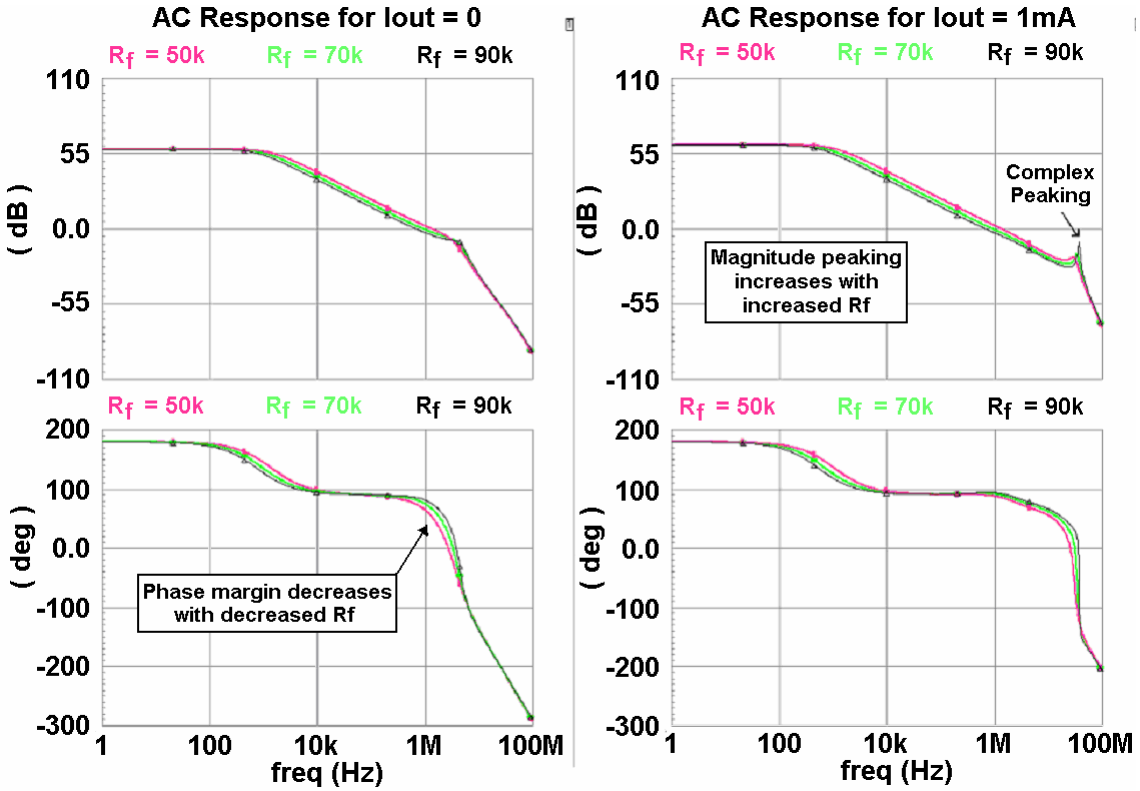

Fig. 49. Variation in compensation resistor, R_f.

Fig. 49 shows the general trend for increased and decreased compensation resistance, R_f. Clearly, there was a tradeoff between increased phase margin at low current conditions and complex peaking at the mid-range output currents. A teeter-totter approach was used to zero in on the best compensation resistance.

Likewise, the compensation capacitance, C_f, was tested for its general affects. Fig. 50 illustrates the general trends. The magnitude response has more peaking as the compensation capacitance is increased. However, if the peaking was to be reduced, the compensation capacitance was reduced but at the cost of decreased phase margin at low currents. The compensation capacitance in conjunction with the compensation resistance was selected based on a balancing act between the complex pole peaking in the mid-range output currents and the phase margin at the no-load current condition. These AC simulations only considered component mismatch and not temperature variations. The temperature variations were simulated in the statistical analysis section.

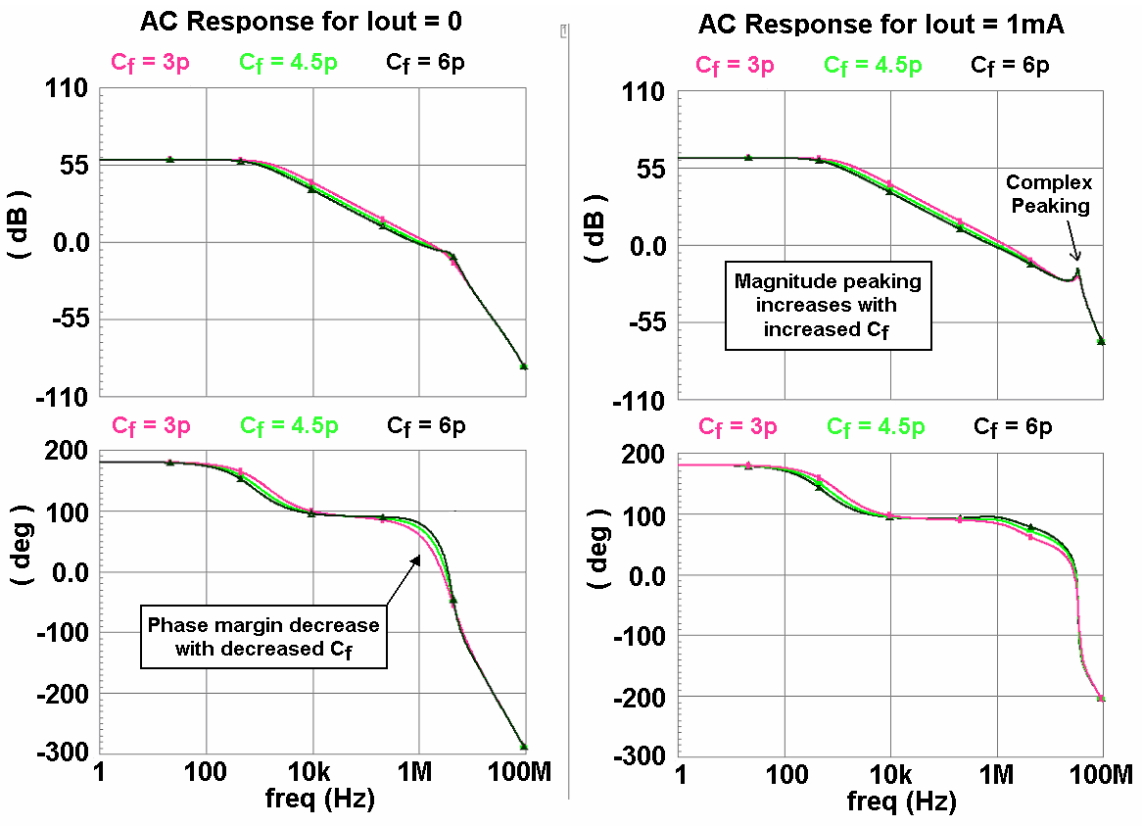

Fig. 50. Variation in compensation capacitor, C_f.

2. Steady-state Parameters

The steady-state parameters define the capacitor-less LDO's static state conditions. There were two important characteristics that defined the steady-state LDO parameters, the line regulation and the load regulation. The line regulation was simulated for 3 different loading conditions, 0mA, 1mA, and 50mA output current. The input voltage was varied from 3V to 4.8V and the corresponding steady-state output voltage was measured. The results are shown in Fig. 51. Like the line regulation simulation, the load regulation measured the steady-state output voltage. This time, however, the input voltage was fixed to 3V and the output current was varied from 0mA to 50mA or the full load condition. Fig. 52 shows the simulation results.

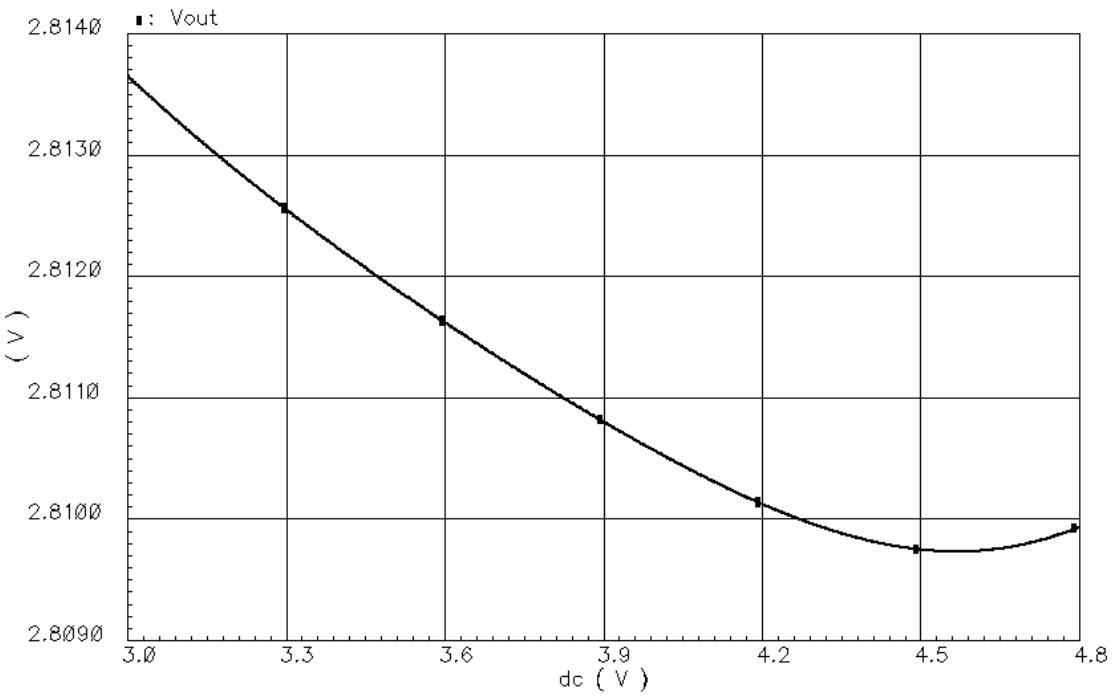

Fig. 51. Line regulation for I_{out} = 0mA.

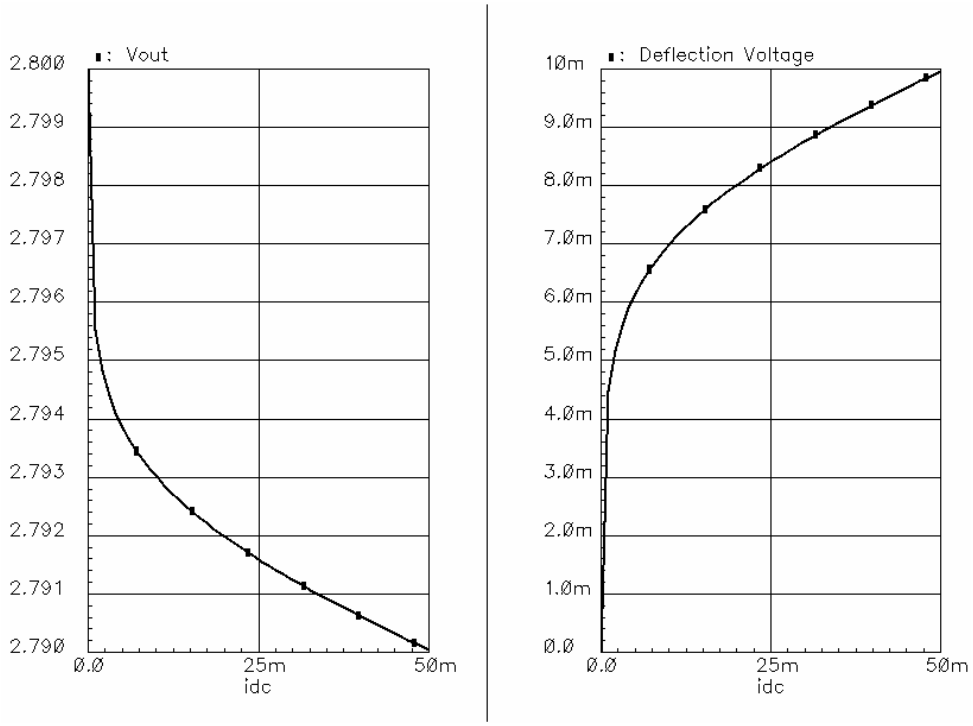

Fig. 52. Load regulation for Vin = 3V.

The output voltage deflects from the nominal 2.8V output as the load current changes. The deflection was due to the drop in DC voltage gain in the control-loop as both the pass transistor transconductance and output resistance change with load current. A higher DC voltage gain at the zero load condition improves the line and load regulation but at the expense of AC stability.

3. Dynamic-state Parameters

The capacitor-less LDO dynamic response was simulated for both load regulation and line regulation as well as the turn-on settling time. As the dynamic-state implies, the capacitor-less LDO is subjected to both line and load transients. The transistor-level design was first simulated without compensation capacitors, C_{f2} and C_{f3}. Fig. 53 shows the zero to full load response with these conditions.

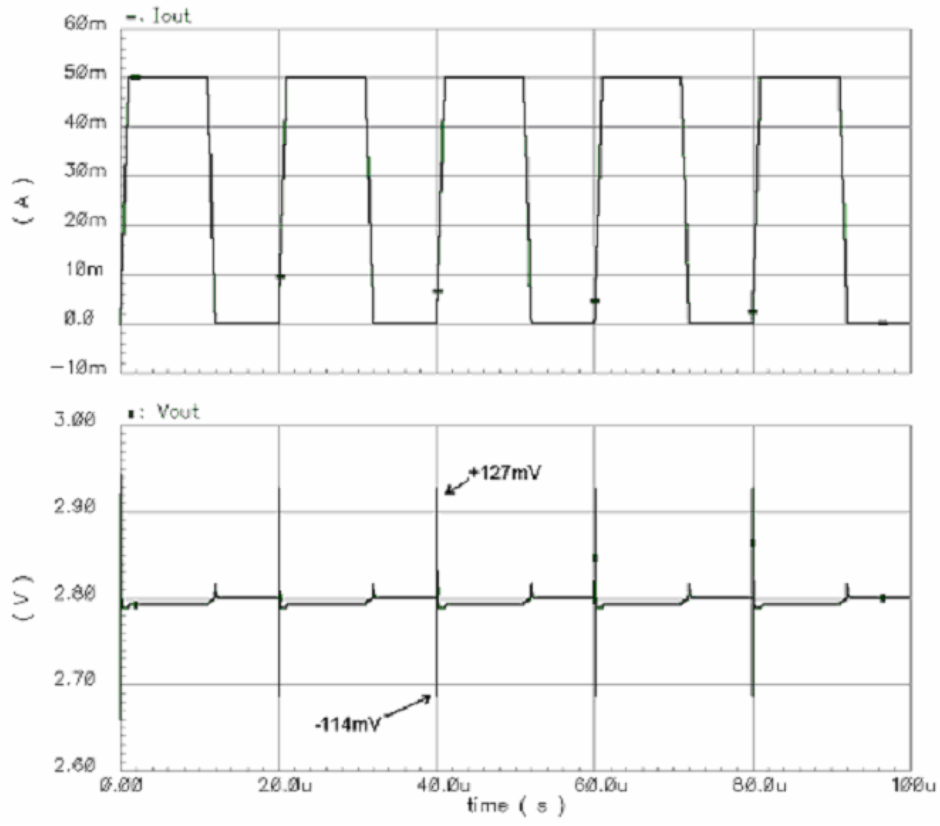

Fig. 53. Full load transient response (without C_{f2} and C_{f3}).

The output current slew rate was set to 50mA/μs with V_{IN} set to 3V. The capacitor-less LDO regulator's response is mainly determined by the fast transient path or the differentiator. The worst case scenario is a fast transition from low to high current, especially zero to full load conditions. The output voltage has a fast negative voltage spike at the onset of the positive change in current. The fast path responds quickly within few nanoseconds and forces the pass transistor to turn on hard. Unfortunately, the differentiator has too much compensation at high output currents, see Equation 36, as the pass transistor transconductance increases significantly. Thus, a large overshoot also appears in the output voltage waveform.

The transistor-level design was then simulated with the added compensation capacitors. These added compensation capacitors, C_{f2} and C_{f3}, degrade the capacitor-less LDO's transient response, but improve the LDO stability and sensitivity to process variations. The results are shown in Fig. 54.

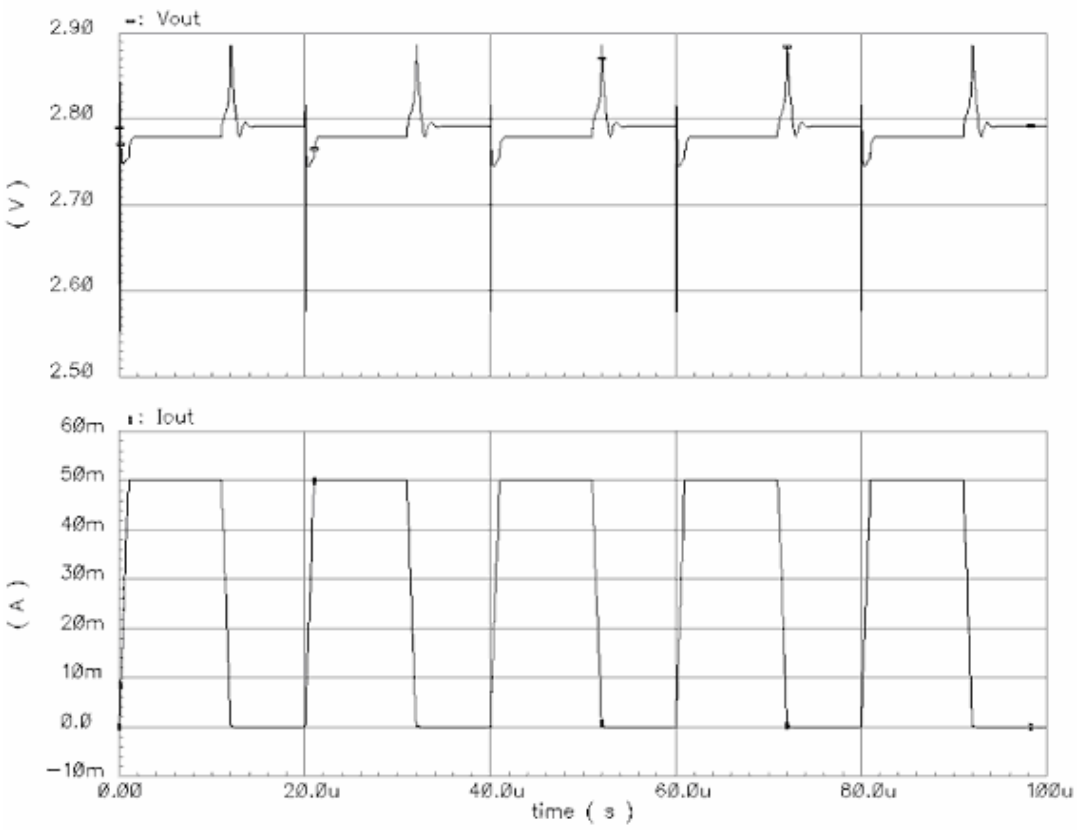

Fig. 54. Load transient response for zero to full load with C_{f2} and C_{f3}.

Line regulation simulations were carried out at both the zero load condition and at 1mA load condition. The input voltage was varied from 3V to 3.5V with a 1µs rise and fall time. The results for both the zero load condition and 1mA load condition are shown in Fig. 55.

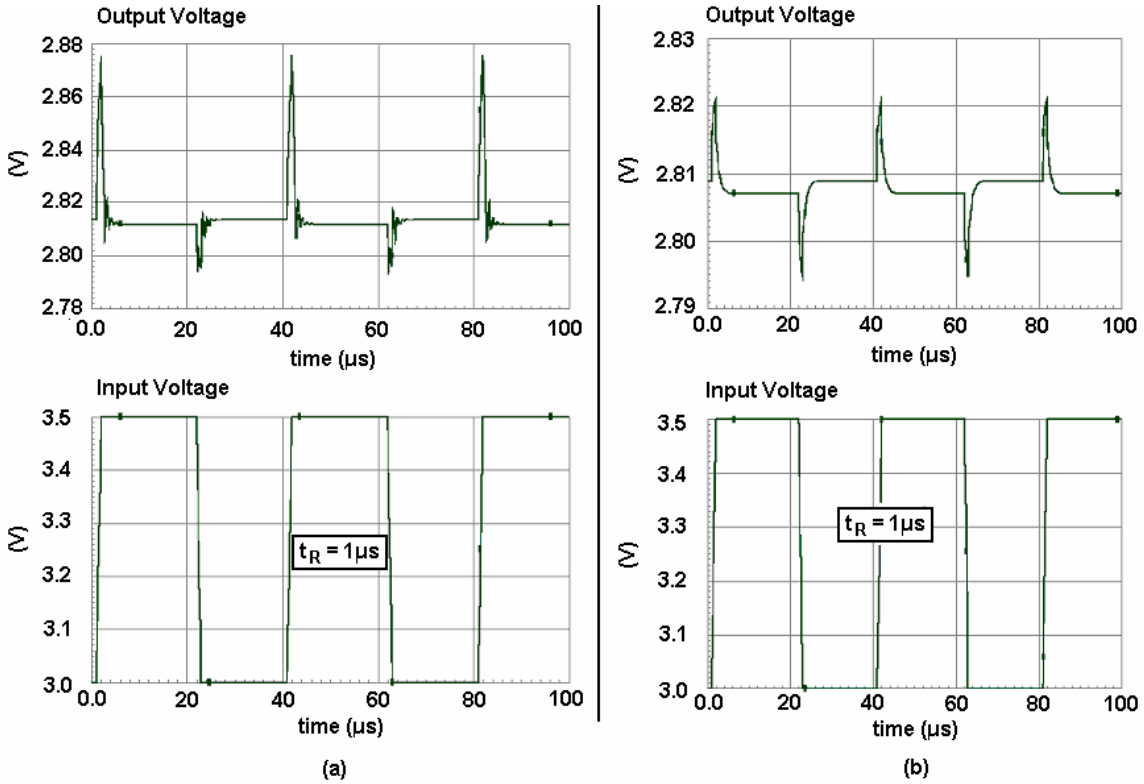

Fig. 55. Line transient response for I_{out} set to 0mA (a) and 1mA (b).

The line transient response improves with larger output currents, due to the decreased gain from the input line to the output voltage. At the zero load condition, the transfer function gain from input to output is at its maximum and corresponds to the worst case line transient response.

The final transient simulation measured the turn-on settling time. This measurement determines the maximum turn-on time required for the capacitor-less LDO to reach a steady-state output voltage. Thus, the input voltage is taken from 0V, turned off, to 3V, turned on, and the time is measured from the point at which the V_{IN} line reaches 3V to the time the output voltage reaches 1% of the nominal output voltage. The results are shown in Fig. 56.

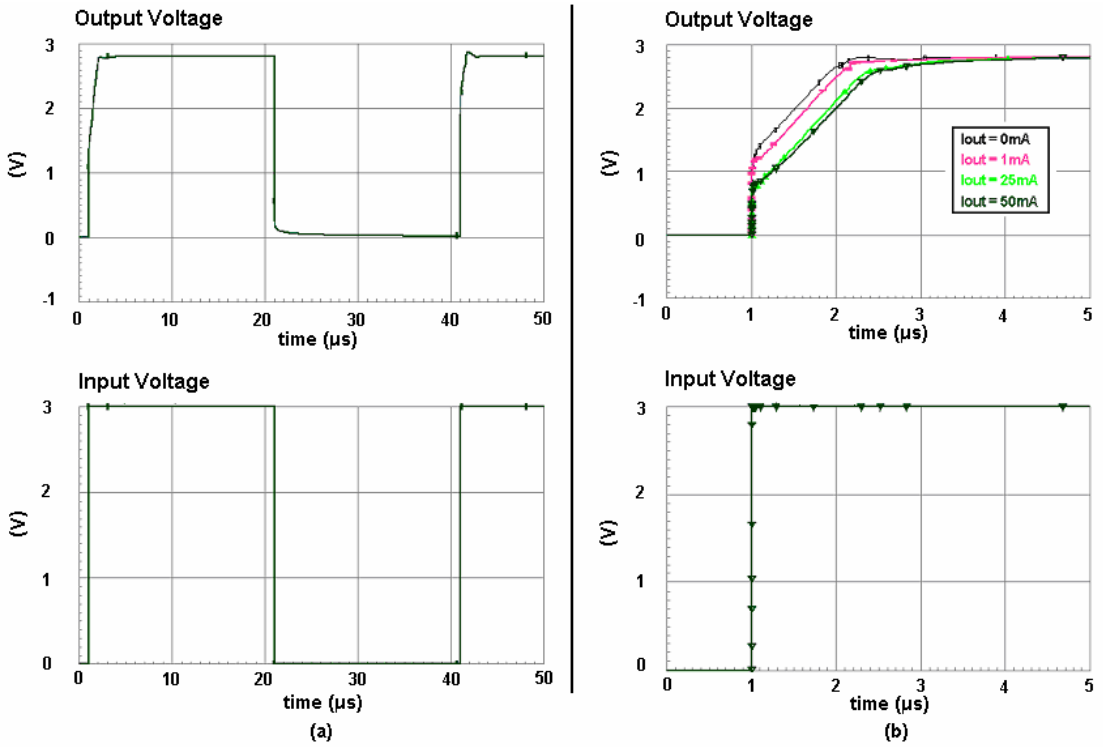

Fig. 56. Turn-on settling time for various output current conditions: (a) full pulse and (b) expanded view.

The worst case scenario occurs at high output current demands during turn on conditions. The initial turn-on condition is relative fast since the pass transistors gate is held to zero, turning the output device completely on. The output voltage begins to slew after tens of nanoseconds as the error amplifier comes online and pulls the pass transistor's gate voltage close to V_{IN}. The differentiator was the main limiting factor for the turn-on settling. The gates of the differential amplifier are tied to the compensation capacitor, C_f, through the compensation resistor, R_f and the turn-on time is related to the charge rate of the C_f through the differentiator's feedback resistor and the current source that feeds the differentiator circuit. The output voltage is solely determined by the rate or charge injected into the output capacitance. Higher output current demand reduces that rate at which the output capacitor can be charge and the maximum output level reached before the error amplifier turns on. Thus, the slope of the output voltage does not change and is entirely dependent on the slewing in the differentiator. However, the reduced initial charge level is lower for the high current conditions resulting in a longer turn-on settling time.

4. High Frequency Parameters

The final set of measurements included the capacitor-less LDO's output referred noise and the PSRR. The output referred noise was measured in closed-loop for different static output current conditions. Fig. 57 shows the output referred noise for various loading conditions.

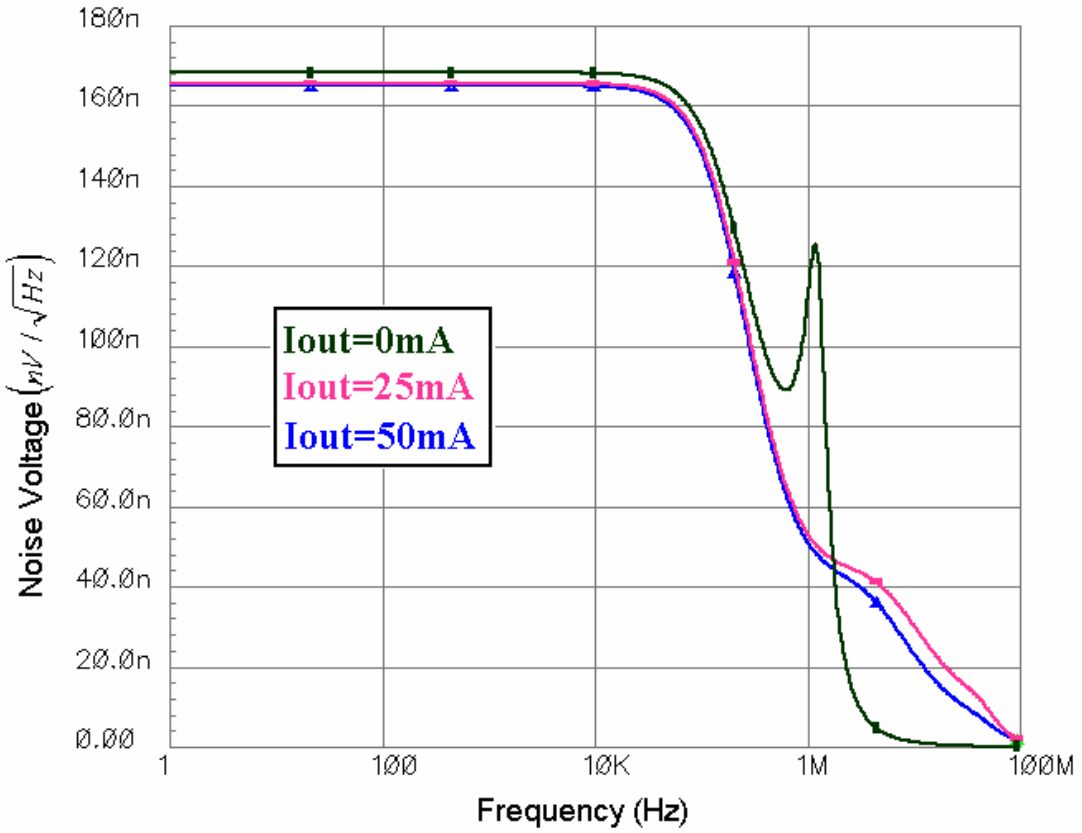

Fig. 57. Equivalent output noise for various loading conditions.

The low-frequency noise component is influenced by the DC loop gain and the output impedance of the output stage. As the output stage impedance decreases, the output referred noise is reduced. The noise is then filtered at high frequencies by the output pole. Most LDO regulators are characterized by the integrated noise over a 1Hz to 100 kHz bandwidth. The corresponding integrated noise is shown in Table X.

TABLE X

INTEGRATED OUPUT NOISE: 1Hz ~ 100kHz

LOAD CURRENT	NOISE
I_{OUT} = 0mA	51.7 μV
I_{OUT} = 25mA	50.6 μV
I_{OUT} = 50mA	50.3 μV

The average integrated output noise is roughly 50μV in the 1Hz to 100 kHz noise bandwidth. The error amplifier contributes to most of the noise although the differentiator adds noticeable effects. The noise specifications for the proposed capacitor-less LDO regulator compete with most standard LDO voltage regulators. Low noise LDO regulators typically have approximately 20μV or less in the measured bandwidth. The noise can be reduced by reduction of noise current in the error amplifier.

Power-supply-rejection-ratio defines the LDO regulator's ability to reject small-signal, high-frequency noise from the input line to the output voltage node. The capacitor-less LDO voltage regulator's PSRR was measured in closed-loop for various static state current conditions. The results are shown in Fig. 58. The proposed topology improves with increased load current. This is mainly due to the chosen structure for the error amplifier. The PSRR is improved by applying V_{IN} as a common-mode signal to both the pass transistors gate node and its source node. The PMOS differential input pair coupled by its NMOS active current mirror load decouples the V_{IN} rail from its output. Thus, better PSRR can come from a PMOS active current mirror where the output of the differential amplifier directly drives the pass transistor. The PMOS differential pair was chosen due to their lower flicker noise and output circuit protection to large transients.

The first knee in the PSRR plot is due primarily to the dominant pole at the gate of the pass transistor. The PSRR at higher frequencies is caused by the relative impedance at the output node. At the highest frequencies, the PSRR is a function of the output node impedance.

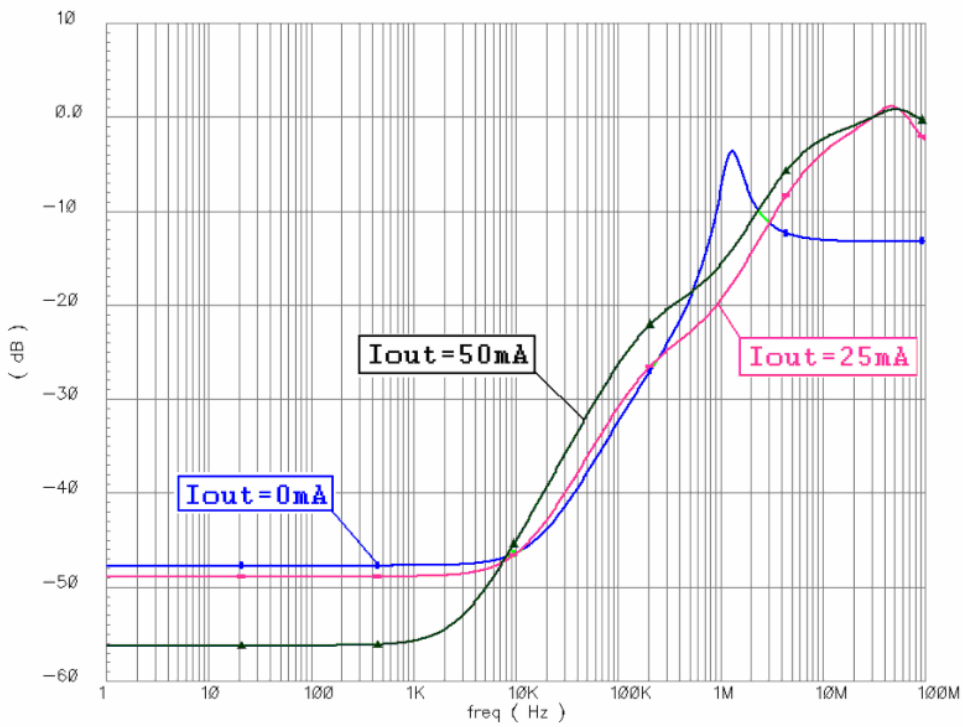

Fig. 58. PSRR measurement for various output current conditions.

5. Final LDO Specifications

The final capacitor-less LDO regulator simulated parameters are given in Table XI. The parameters indicate the worst case scenario assuming nominal values for both the threshold voltage and mobility. The capacitor-less LDO regulator was then tested for process variation.

TABLE XI

SIMULATED WORST CASE PARAMETERS

PARAMETERS	SPECIFICATION	PARAMETER	SPECIFICATION
GBW	704 kHz	Line transient	+64mV
Phase Margin	72°	Load transient	-211mV
Line regulation	2 mV/V	Settling time	4.7 µs
Load regulation	10mV (full load)	PSRR	47dB (at 0mA)
Power	65 µA	Noise	51.7 µV

B. Statistical Analysis

Monte Carlo analysis was performed to study the capacitor-less LDO's sensitivity to process variation such as carrier mobility and MOSFET threshold voltage. All the Monte Carlo simulations used a 10% variation in both threshold voltage and mobility per sigma. Thus, 99.7% of the fabricated IC would fall into the range of ± 30% of the nominal designed values. Fig. 59 shows process variation effects on the gain-bandwidth product and phase margin at the no-load condition.

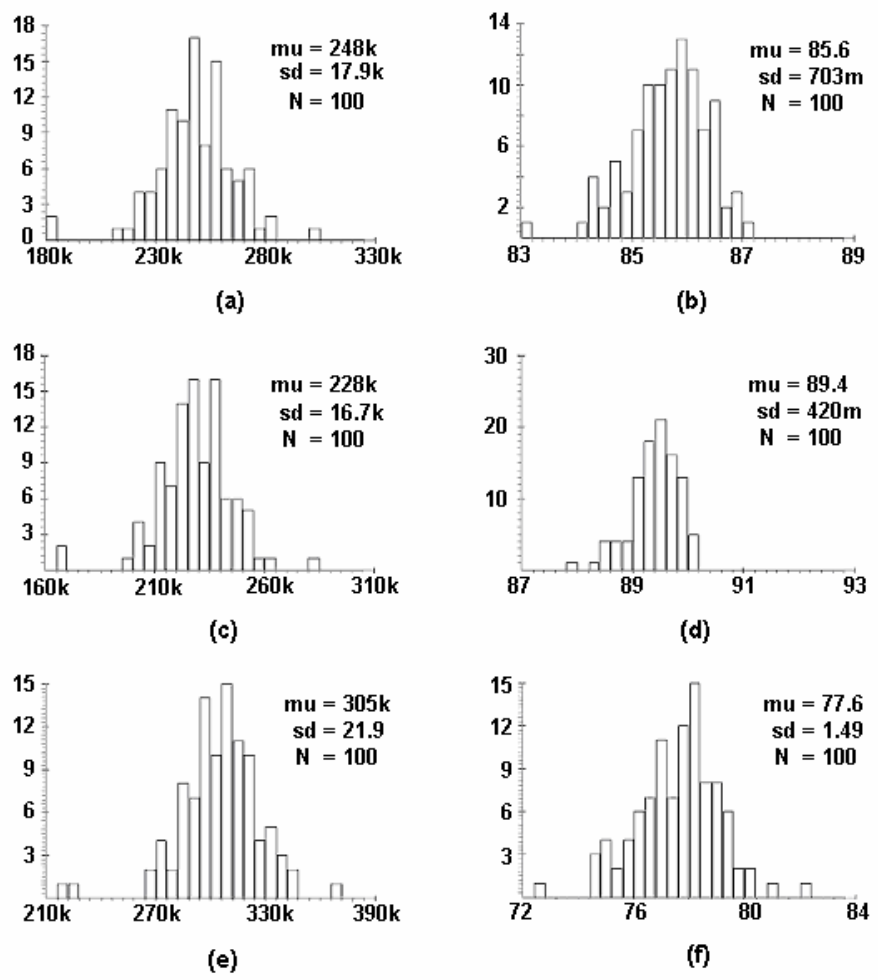

Fig. 59. Process variation for I_{OUT} = 0mA: nominal GBW (a) and phase margin (b), C_f and R_f +20% of nominal GBW (c) and phase margin (d), and C_f and R_f -20% of nominal GBW (e) and phase margin (f).

Fig. 59 shows that plenty of phase margin is obtained even with large variation in the compensation capacitor, C_f, and compensation resistor, R_f. Next, the dc gain and the ground current were simulated for process variation, shown in Fig. 60.

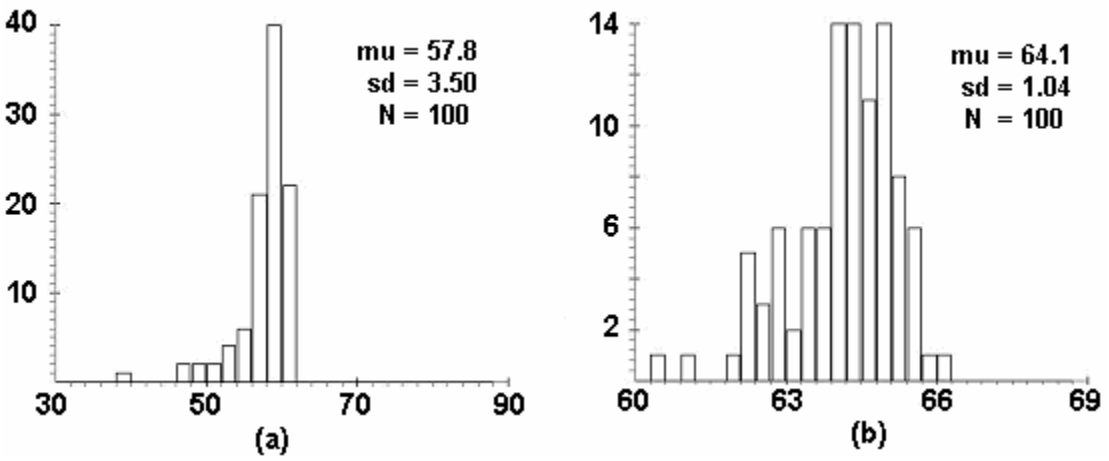

Fig. 60. Process variation on DC gain for I_{OUT} = 0mA (a) and 1mA (b).

The simulation showed that the low current dc gain was more susceptible to process variation with a standard deviation of 3.5dB compared to 1.0dB for the 1mA load condition. This was the main reason the gain margin was increased as much as possible. Fig. 61 shows process variation effects on the dc quiescent current. Since all the current branches within the capacitor-less LDO regulator were all generated from current mirrors, the overall quiescent ground current was virtually unaffected by process variation. The standard deviation was only 317nA. Finally, the PSRR was simulated for process variation. The results are shown in Fig. 62.

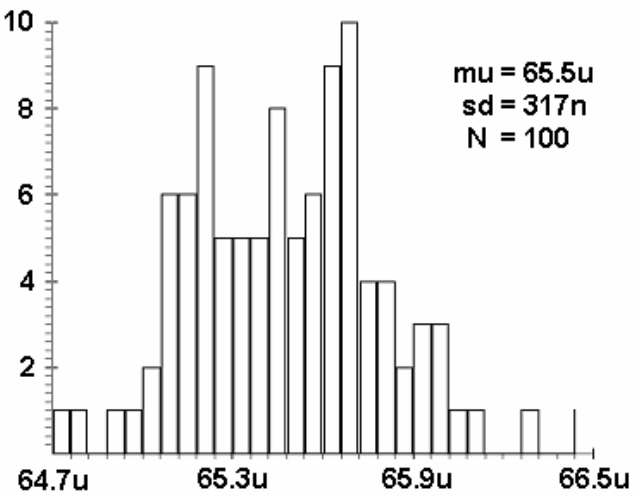

Fig. 61. Process variations effects on dc quiescent current.

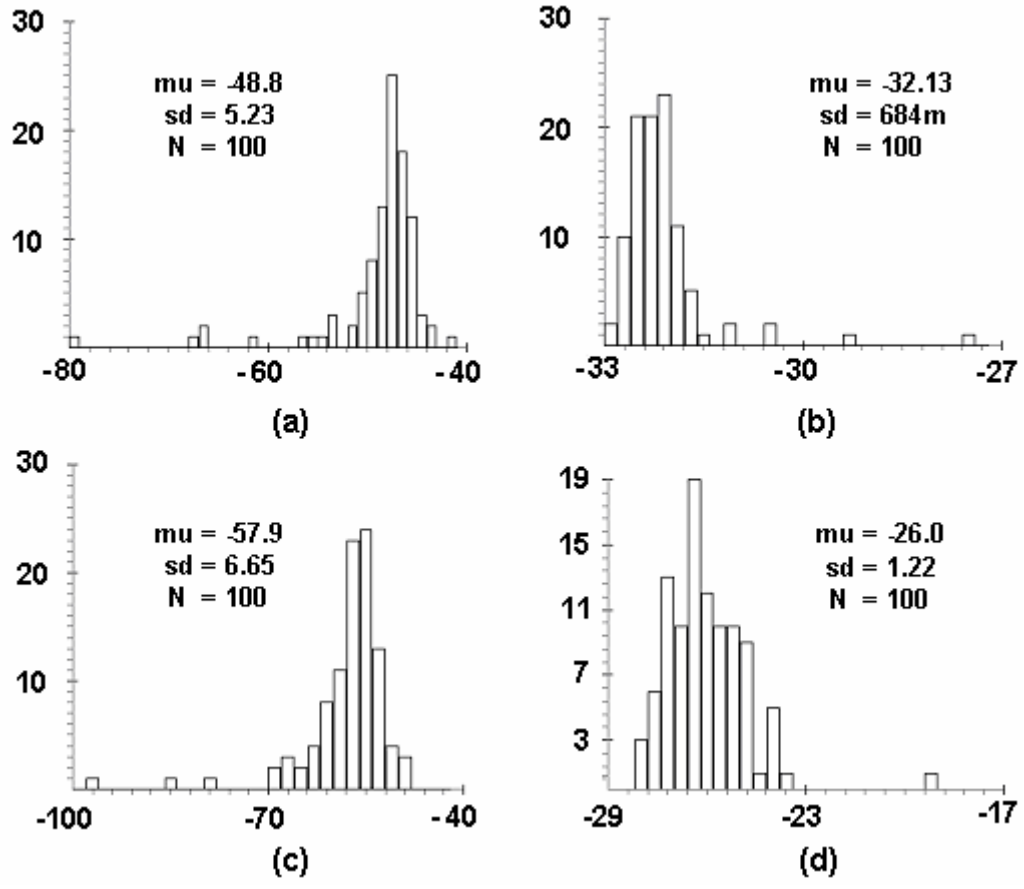

Fig. 62. Process variation on PSRR for I_{out} = 0mA at 1Hz (a) and 100kHz (b) and for I_{out} = 50mA at 1Hz (c) and 100kHz (d)

Finally, the dc steady-state output voltage was simulated for process variation effects. The variation was verified for four different output current conditions, 0mA, 1mA, 10mA, and 50mA. The results are shown in Fig. 63.

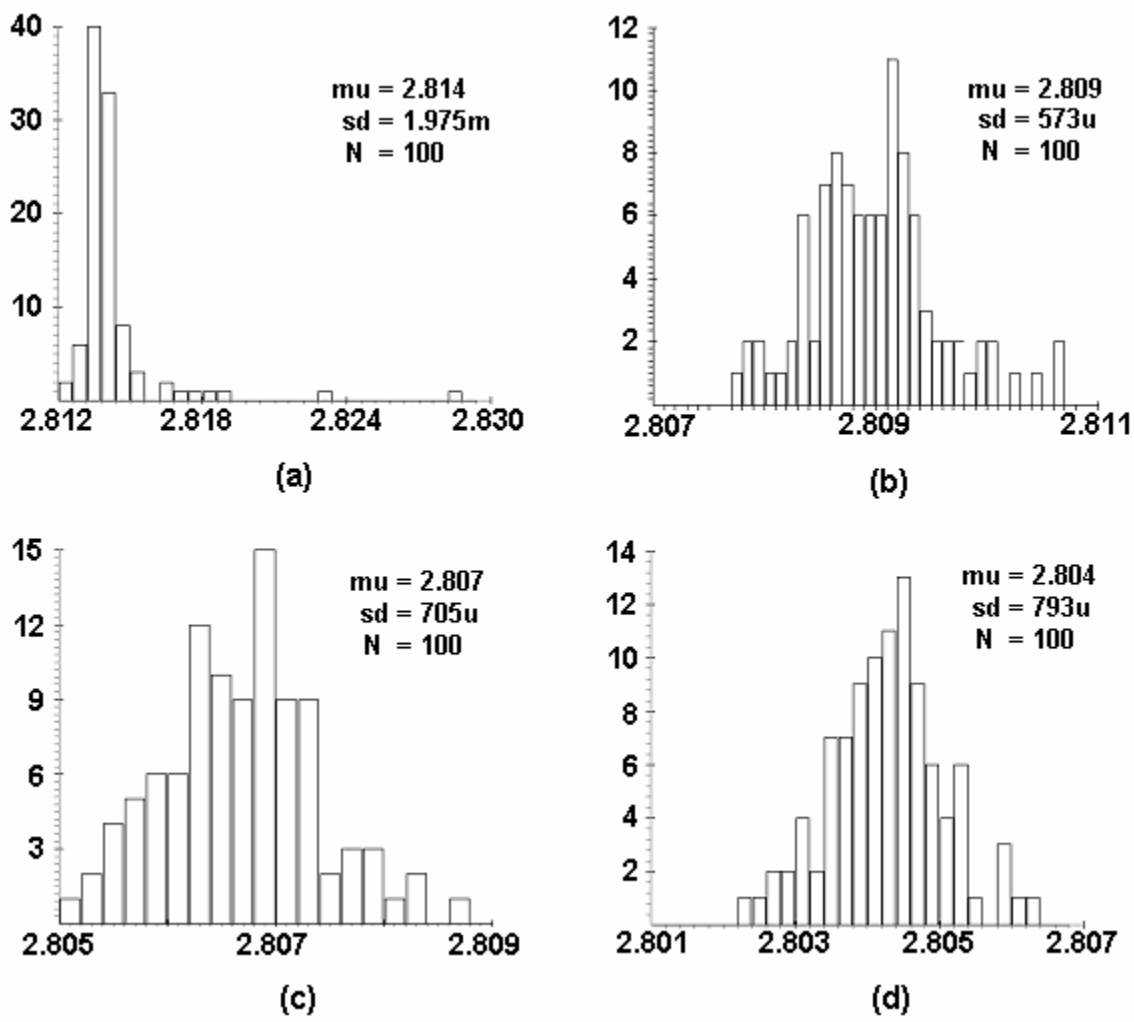

Fig. 63. Process variation on DC steady-state output voltage for I_{out} set to 0mA (a), 1mA (b), 10mA (c) and 50mA (d).

C. Final LDO Layout

The final capacitor-less LDO voltage regulator was laid out in a TSMC 0.35um CMOS technology through the MOSIS educational service. Common centriod layout techniques were used for all current mirrors which included all the transistors except for the large pass transistor. The 16mm pass transistor was split into 16 20x50µm transistor blocks. This allowed for extra n-well substrate contacts to prevent potential latch-up issues caused by induced bulk current. Careful matching was also used to between the two feedback resistors R_{F1} and R_{F2} by interweaving unit resistors to meet the desired ratio. Fig. 64 shows the final capacitor-less LDO voltage regulator layout.

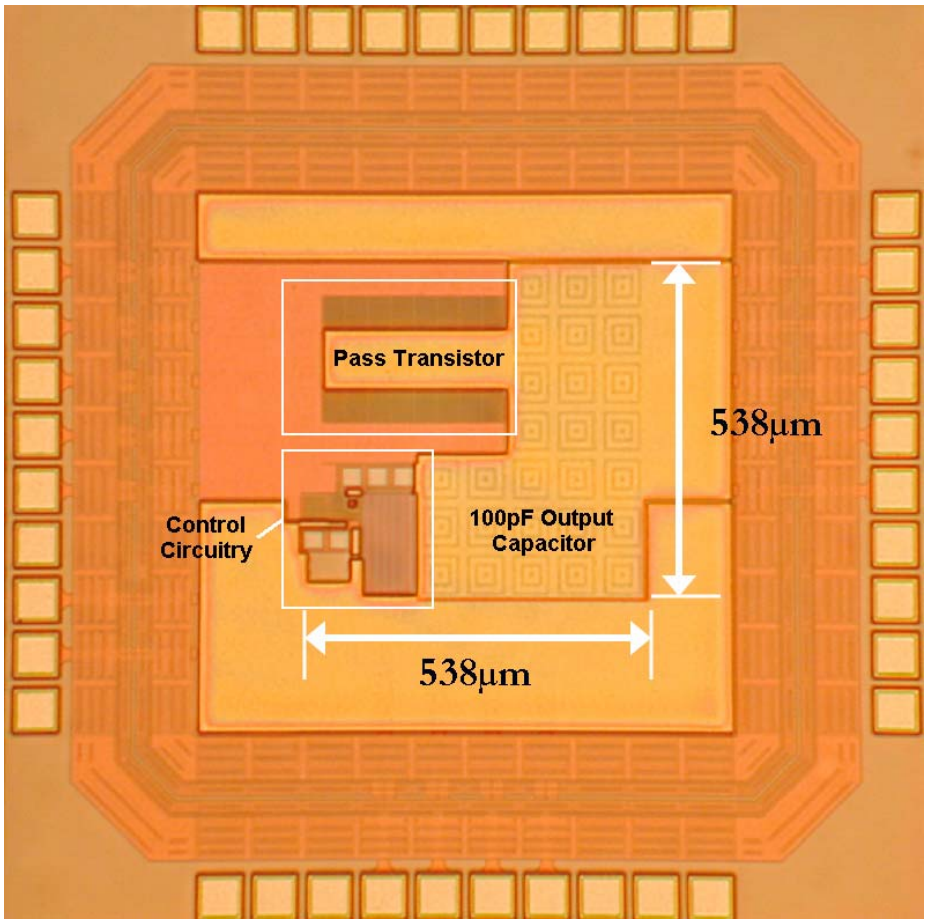

Fig. 64. Final layout in TSMC 0.35µm CMOS technology.

The capacitor-less LDO itself measures 538µm x 538µm while the pad frame measures 1.5mm x 1.5mm. The pass transistor and the 100pF internal output capacitor occupy approximately ¾ of the total effective area. The area surrounding the capacitor-less LDO is constructed of various layers to meet density constraints.

The control circuit contains the error amplifier, the differentiator, the feedback resistors, and extra compensation circuitry. The feedback resistors, R_{F1} and R_{F2}, and the compensation resistor, R_f, accounted for most of the control circuitry area. The feedback resistors were constructed using the second polysilicon layer or poly2. Vertical orientation was used so that the average temperature gradient due to the pass transistor radial heat dissipation pattern was felt equally across the two feedback resistors. The compensation resistor, R_f, was constructed with a n-well diffusion resistor. This allowed for lower parasitic capacitance per resistance and a better absolute accuracy.

Finally, the input and output nodes were connected to 5 external pins each. The pin inductance was reduced from roughly 30nH to 6nH and produced better fast current transients. The external pin capacitance did not hinder the capacitor-less LDO's transient response but actually improved the performance. Extra capacitance was added from V_{IN} to ground and helped to filter out higher frequency noise and ripple. The capacitor-less LDO voltage regulator was finally packaged in a 40 pin ceramic dual-inline package.

IV. EXPERIMENTAL RESULTS

The physical capacitor-less LDO voltage regulator was tested in the laboratory for all the simulated parameters except for the open-loop AC response. A test board was designed and fabricated to facilitate the experimental gathering for various tests. Each experiment has the testing apparatus clearly defined as well as other experimental and environmental parameters under which the experiment was carried out.

A. Test Board Design

The test board was fabricated on FR-4 glass epoxy double sided boards with tinned copper traces and plated trough holes. External circuitry was included to generate the desired reference voltage, V_{REF}, and the desired bias current, I_{BIAS}. These components were not included on chip, reducing the potential of circuit failure. A foil pattern and schematic are provided in Appendix I and II. Fig. 65 shows the finished and populated test board and setup.

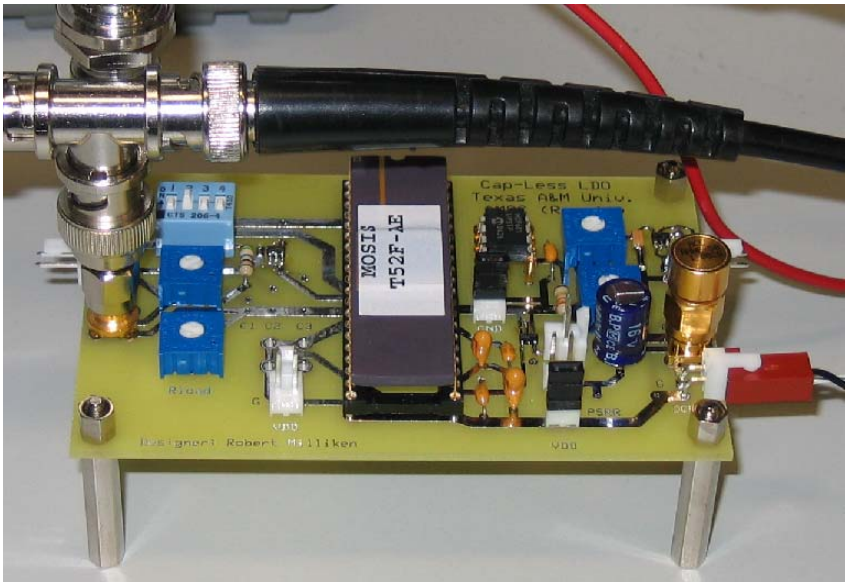

Fig. 65. Final populated test board and setup.

The circuit board contains both active and passive load elements. The active current mirror load used the Panasonic XNO2501 silicon NPN epitaxial planer transistor pair to provide load current transients via a waveform generator. The test board also contains a surface mount 100mA LDO voltage regulator that supplies the V_{REF} and I_{BIAS} circuits. The LDO can be either supplied directly from the V_{IN} of the capacitor-less LDO voltage regulator or a separate power supply. A potentiometer and several different passive elements can be switched in and out to test static load conditions. Finally, high-frequency signals can be coupled onto the V_{IN} rail via a large bipolar capacitor and 50 ohm DC supply resistor.

B. Transient Response

The transient response was tested for load and line transients and for the turn-on settling time. The experiments only require a waveform generator, an oscilloscope, and a dc power supply. The transient response results are given the next three subsections.

1. Load Transient Response

The load transient response was tested for the load current transient from 0mA to 50mA with a 1us rise and fall time. The load current was generated with a BJT NPN current mirror and a signal generator. The test circuit is shown in Fig. 66.

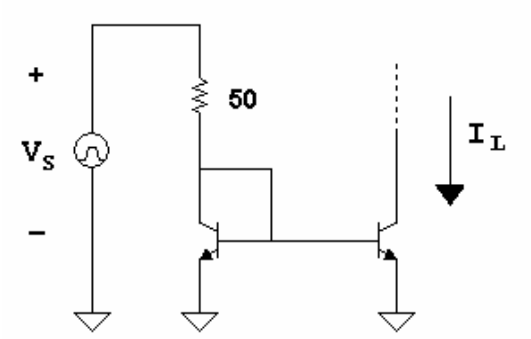

Fig. 66. Transient load current generator.

The input voltage waveform's minimum and maximum voltage levels for the current generator were finely tuned to yield a 0mA to 50mA load current. The capacitor-less LDO voltage regulator was then tested for its zero to full load response using a 500 MHz oscilloscope. The results are shown in Fig. 67.

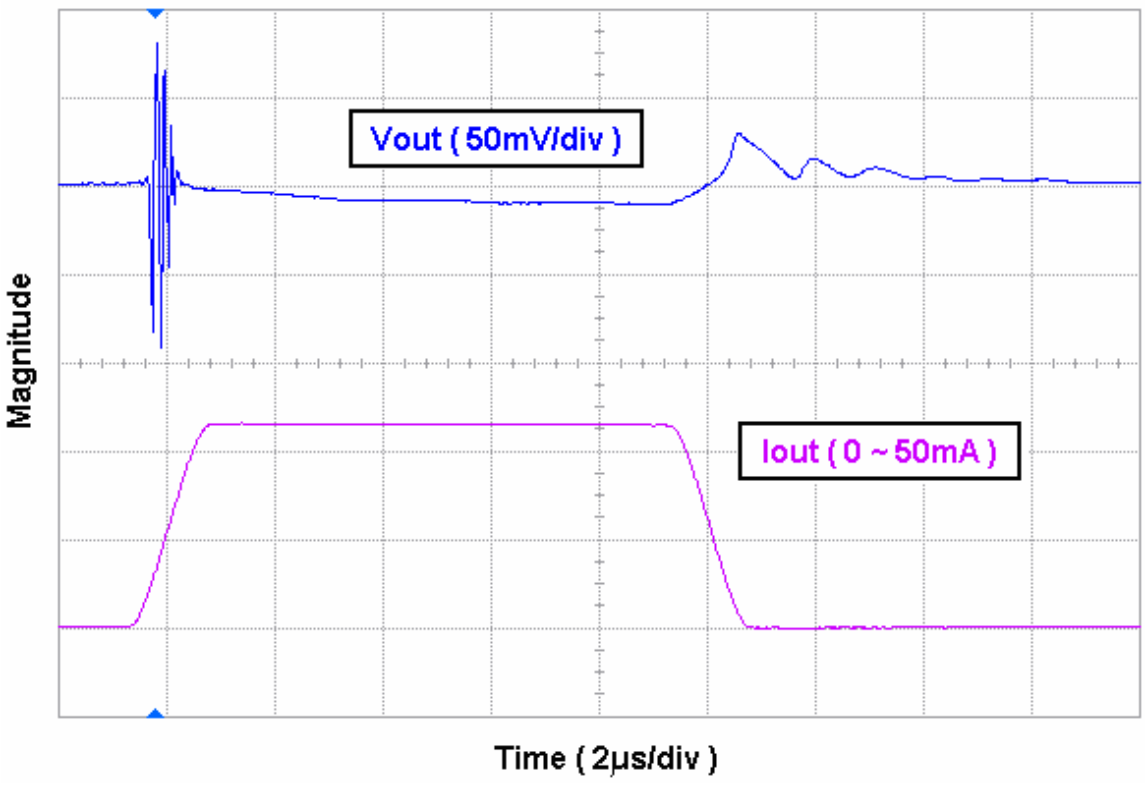

Fig. 67. Transient response for a 0mA to 50mA load transient with V_{IN} = 3V.

The capacitor-less LDO voltage regulator gave expected results that resemble the transistor-level circuit simulations. A little extra ringing was experienced for the positive load current transition and was sensitive to test cable movement. The ringing quickly subsided and a stable response was reached. Thus, the capacitor-less LDO internal compensation had produced stable operation from zero to full load.

2. Line Transient Response

The Line transient response was measured for a 3V to 4V step waveform with 1µs transition times. The I_{BIAS} and V_{REF} circuits were operated from a separate power supply through out the operation. An Agilent waveform generator was used to supply the transient step. Fig. 68 shows the capacitor-less LDO line transient response.

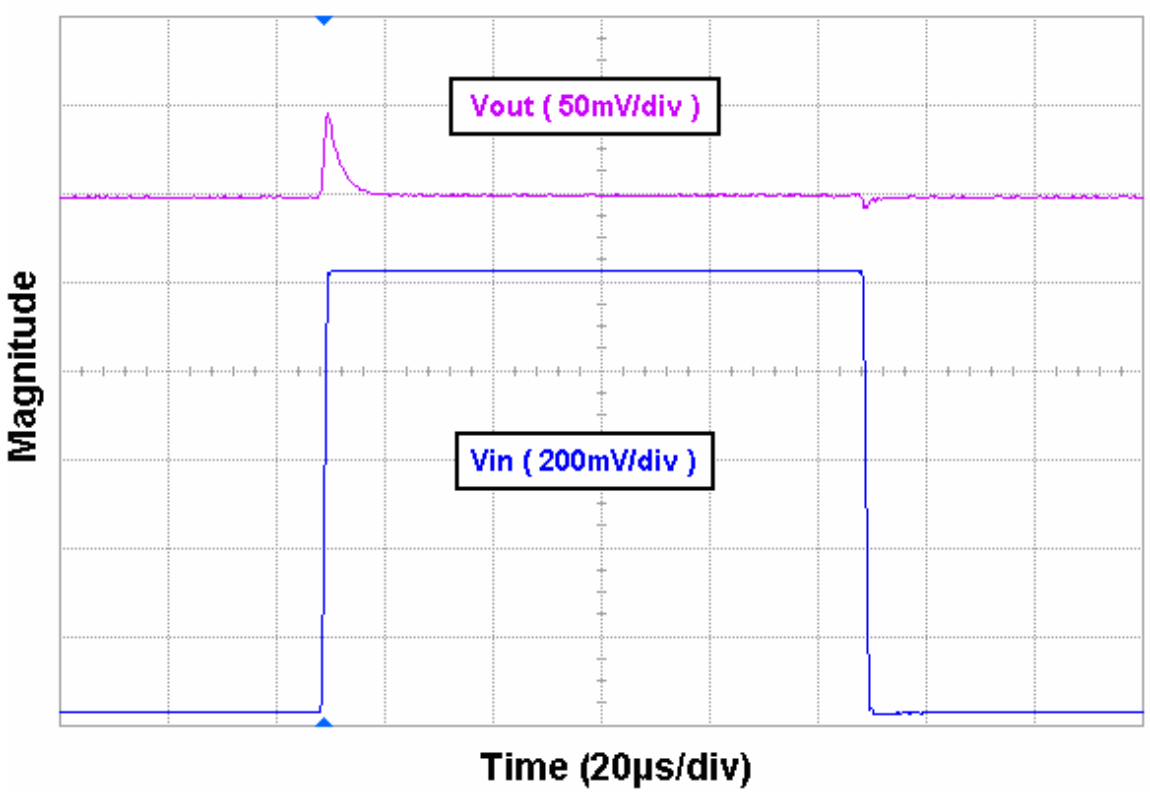

Fig. 68. Experimental line transient response with I_{out} = 0mA.

Fig. 68 illustrates the worst case line transient condition with capacitor-less LDO operating at the zero load condition. The output waveform, top trace, was ac coupled to the oscilloscope and does not reflect the dc component while the input rail waveform was directly coupled to the oscilloscope. The input voltage waveform was measured directly at the test board input voltage rail. All cables were BNC 50ohm assemblies. The experimental results closely matched the

predicted line transient behavior with approximately a 50mV output voltage spike. This was less than the simulation predicted since the simulation did not include the parasitic capacitance from V_{IN} to ground and other parasitic capacitances.

3. Turn-on Settling Time

The measurements for turn-on settling time are shown in Fig. 69 for no load current and Fig. 70 for I_{OUT} equaled to 10mA and 50mA.

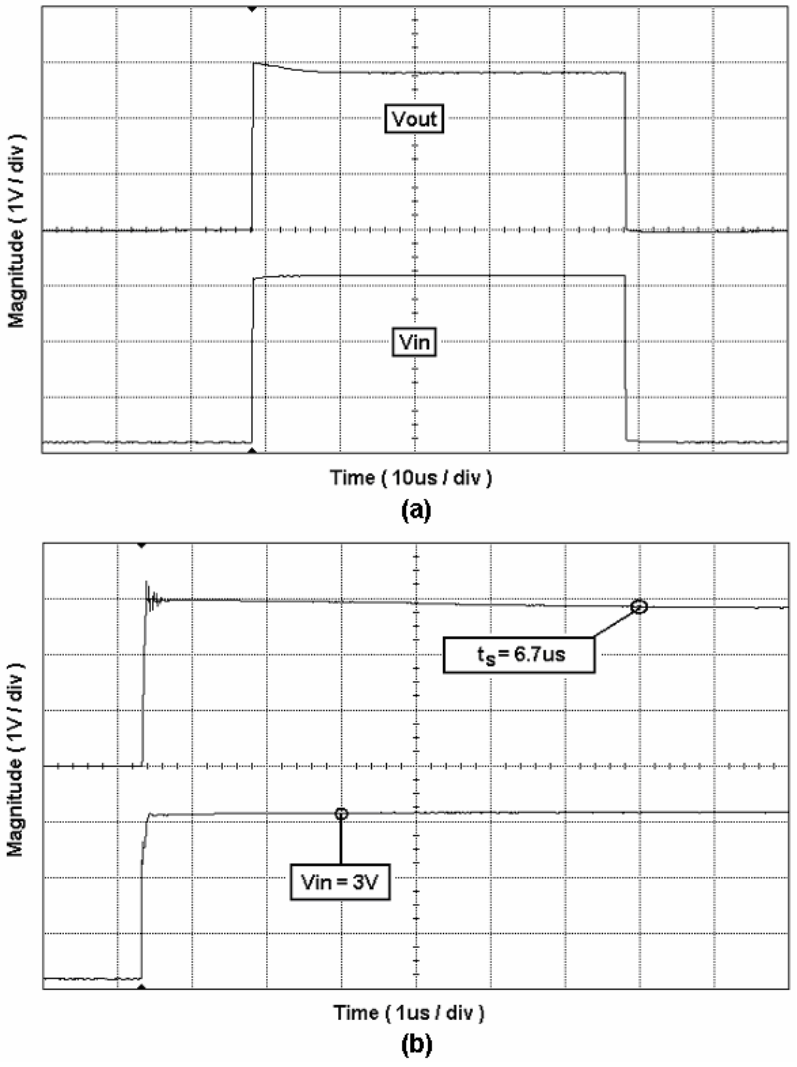

Fig. 69. Turn-on settling time for I_{OUT} = 0mA: full pulse (a) and expanded view (b).

The circuit board was modified to measure the capacitor-less LDO regulator's turn-on settling time. The actively regulated bias current generator used filter capacitors to remove any noise or ripple injected into the IC. The large filter capacitors drastically decreased the turn-on settling time by introducing slewing effects. The active current generator was replaced by a simple resistor trimmed to supply 7.5µA.

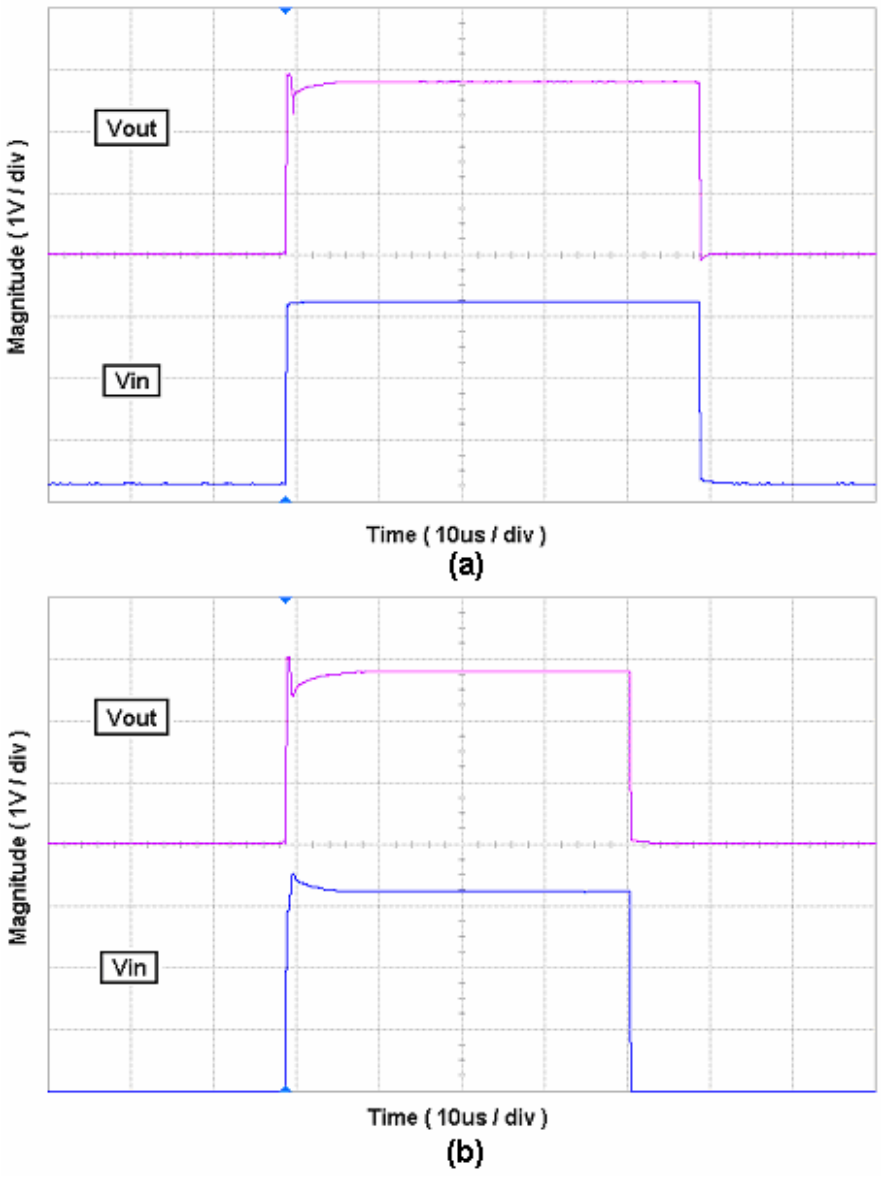

Fig. 70. Turn-on settling time for I_{OUT} = 10mA (a) and I_{OUT} = 50mA (b).

The settling time was measured from the input voltage pulse edge to the time the output voltage reached 0.2% of its steady-state value. The no-load condition had the shortest turn-on settling time at 6.7µs while the 10mA load condition had 7.5µs and the 50mA load condition had 8.7µs. The output voltage had a large initial overshoot. This was due to the circuit testing condition where the reference voltage was not stepped with the input voltage. This forced the pass transistor's gate to ground while the rest of the circuit charged up, causing the output voltage to rail out to the input voltage.

C. High-Frequency Response

The capacitor-less LDO regulator was tested for its high frequency characteristics. These measurements included the PSRR, ripple rejection ratio and the equivalent output noise. Measurements were taken for different load current conditions which included the zero, 1mA, and 50mA load current conditions.

1. Power-supply-rejection-ratio

The power-supply-rejection-ratio (PSRR) measured the transfer function from the capacitor-less LDO regulator's input voltage to its output voltage. A network analyzer was used to calculate the transfer function based on a known frequency swept input signal and the measured regulators output voltage. The PSRR tests used only small signals such that large signal effects did not influence the measurements, and the input signal was ac coupled through a large capacitor and small resistor. The zero created by the coupling network set below the frequencies of interest, roughly 5Hz. The results are shown in Fig. 71. The test results correspond closely to the predicted transistor-level simulations and shows that the PSRR improves with increased load current. The first knee or the effective dominant zero resides at approximately 100kHz. The low frequency PSRR for three different load currents were -71dB for a 50mA load, -48dB for a 1mA load, and -71dB for a no load condition. A few interesting artifacts surfaced that were not predicted by the simulations. First, the PSRR plots rolled off at very low frequencies. This was due to the coupling of the input signal superimposed on the dc power supply through a coupling capacitor and resistor, and a low frequency zero was created. Second, the PSRR for a 50mA load increased drastically.

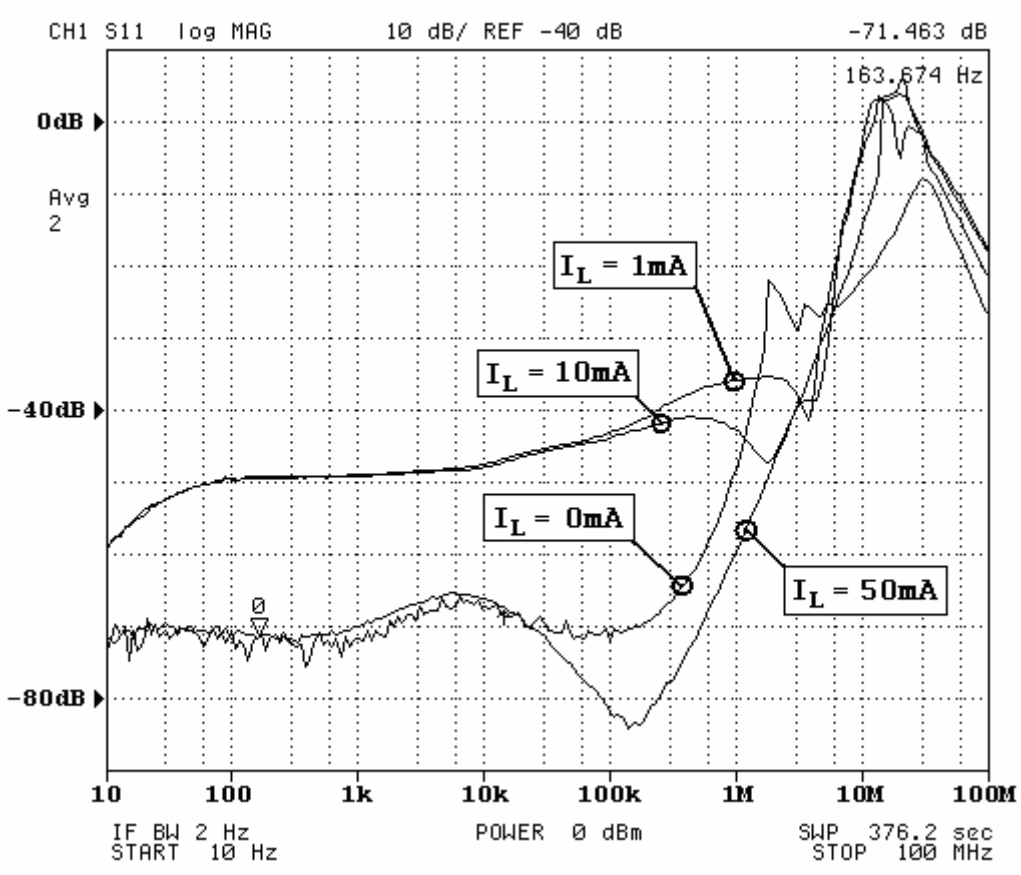

Fig. 71. PSRR for various loading conditions.

This was due to the frequency dependant impedance in the forward path such that a near perfect common signal appeared to the gate and source of the pass transistor.

2. Ripple Rejection Ratio

The ripple rejection ratio was measured at low frequency. The rise and fall times were reduced such that slewing did not occur. The line regulation could also be determined from such a measurement since the time period was much greater that the settling time of the capacitor-less LDO regulator. Fig. 72 shows the measurement.

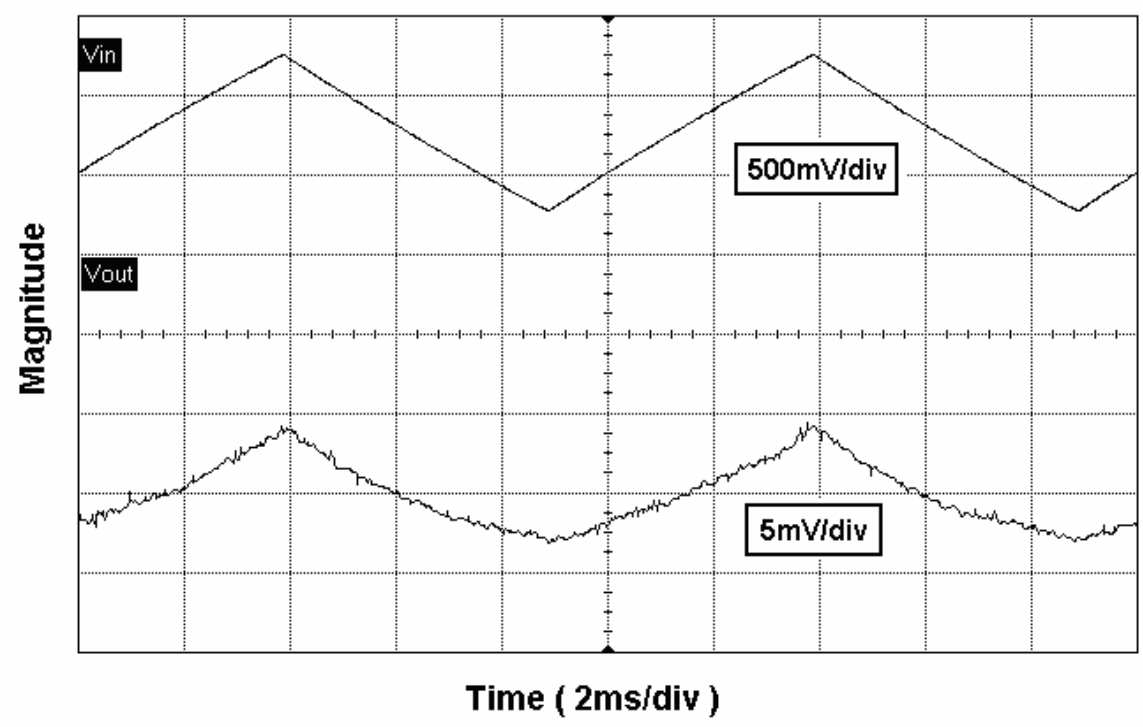

Fig. 72. Line ripple rejection at 100Hz.

The magnitude scales differ between the input voltage and output voltage. The ripple rejection at 100Hz is roughly 43dB. The measurement was taken for the zero load condition. The ripple rejection is directly related to the PSRR and the measurement in Fig. 72 matches the results shown in Fig. 71.

3. Equivalent Output Noise

The equivalent output noise was measured at 50mA of load current, and was measured from 1kHz to 1MHz, shown in Fig. 73. The results show that flicker noise dominates most of the usable bandwidth. The spot noise at 100kHz was roughly 720 nV/sqrt(Hz). This value was higher than the predicted model, suggesting that the model parameters for flicker noise were perhaps too conservative. This concluded the experimental results.

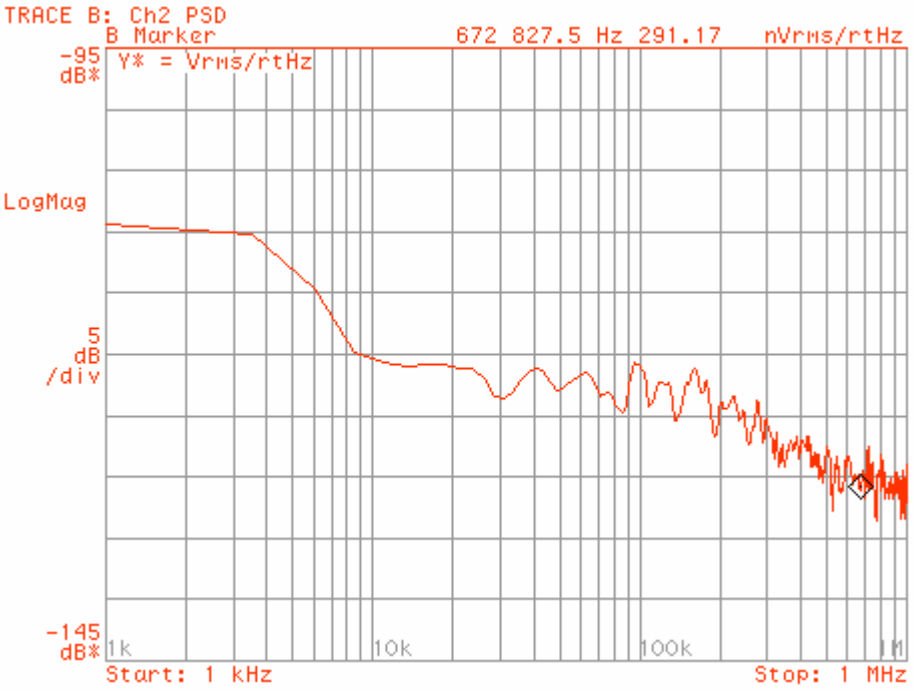

Fig. 73. Noise Spectrum for 50mA output current.

D. Comparison of Results

There have been three significant works in the area of capacitor-less LDO voltage regulators [4],[11], and [12]; however, each work uses a different device for the pass transistor. Work [4] most closely resembles the proposed design, using a MOSFET in the common-source configuration, but it does not have full range stability, losing controllability at low current loads. Work [11] uses a MOSFET in the common-drain configuration which closely resembles classic linear regulators, but [4] requires a much larger voltage headroom and bias current. The latest work, [12], uses a composite transistor to reduce the voltage headroom but at the cost of significant bias current.

Experimental results show that the proposed capacitor-less LDO voltage regulator exceeds current work in the area of capacitor-less LDO regulators in both transient response and AC stability while consuming only 65µA of quiescent current. A comparison is made among the other output capacitor-less designs [4], [11], and [12], shown in Table XII, illustrating the significance of the proposed capacitor-less LDO regulator. Not only does the proposed

regulator consume low power, but it provides a low dropout voltage and fast settling time. SoC designs would benefit from the reduced board real estate, pin count, and cost achievable with the proposed capacitor-less LDO regulator.

TABLE XII

FINAL LDO COMPARISON

PARAMETER	[4]	[11]	[12]	THIS WORK
Process (µm)	CMOS 0.6	CMOS 0.5	CMOS 0.09	CMOS 0.35
Pass Element	CS	CD	Composite	CS
I_{MAX} (mA)	100	300	100	50
V_{OUT}	1.3	3.3	0.9	2.8
V_{DROP} (V)	0.20	1.7	0.30	0.20
I_Q(mA)	0.038	0.75	6	0.065
C_{INT}(pF)	0	180	600	100
Area (mm^2)	0.307	1	0.098	0.289
Δv_{out} (Full load transient)	Unstable at low currents	400mV	90mV	183mV
Settling (µs)	1.6	300	N/A	7.8
PSRR (1kHz)	60 dB	N/A	N/A	57 dB
Loop gain (dB)	90 ~ 110	N/A	>43	55 ~ 62
Noise	60 µV	N/A	N/A	250 µV

V. CONCLUSION

A novel design has been presented that allows for the removal of the large external capacitor normally found on LDO voltage regulators. The new capacitor-less LDO only requires three small internal capacitors for good transient response and AC stability. A thorough analysis was preformed in Section II on the uncompensated capacitor-less LDO as well as the proposed compensation technique. The uncompensated analysis showed that most of the properties of the capacitor-less LDO change with varying load current, making it difficult to guarantee stability and good transient response over the entire output current range of 0mA to 50mA.

The proposed topology uses a differentiator to sense changes is the output voltage and provides a fast negative feedback path for load transients. The differentiator loop also doubles as the AC stability compensation network, using the properties of the Miller capacitor pole splitting technique. Farther analysis showed the bounds of stability for the proposed capacitor-less LDO compensation technique. The differentiator's parasitic poles play a major role in the design, and for a stable system, they must be placed at the highest possible frequencies. A properly designed capacitor-less LDO using the proposed technique resembles a 1^{st} order system up to the gain bandwidth product and remains as such throughout the entire output current range.

The proposed capacitor-less LDO voltage regulator was designed and fabricated in the TSMC 0.35um CMOS technology through the MOSIS educational service. Experimental results showed that the proposed technique can be used to make a fully stable capacitor-less LDO voltage regulator. A comparison was made in Section IV with other works [4], [11], and [12] where the proposed design clearly had the best balanced specification. It only consumed 65µA of ground current while providing a 50mA output with a dropout voltage of 200mV. The transient response came in second to [12] but with a little more the $1/100^{th}$ of the ground current required by [12]. With these specifications, the proposed capacitor-less LDO voltage regulator provides a viable solution for low-voltage, power-efficient, SoC applications, while reducing board real estate, pin count, and overall cost.

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APPENDIX A

TEST BOARD FOIL PATTERN

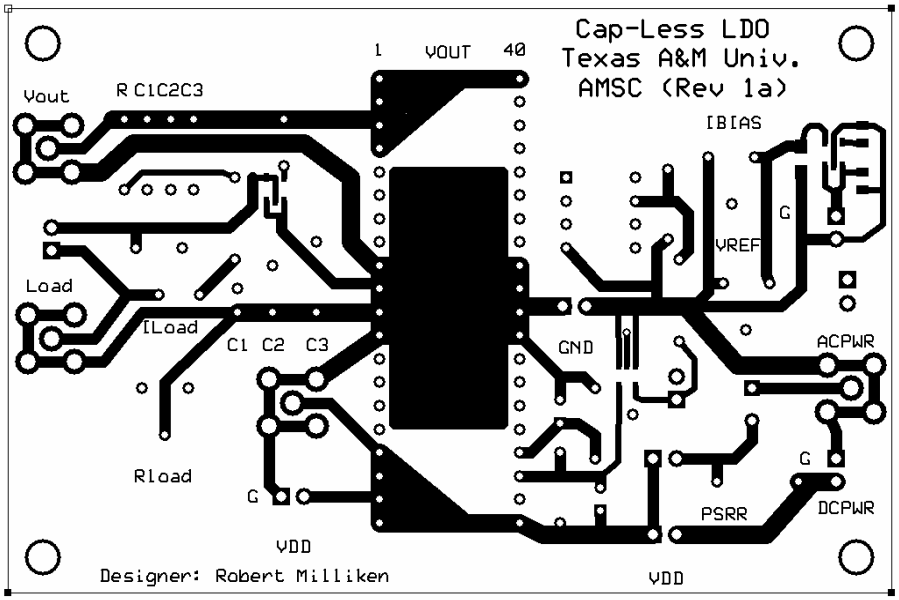

Fig. 74. Top layer of PCB.

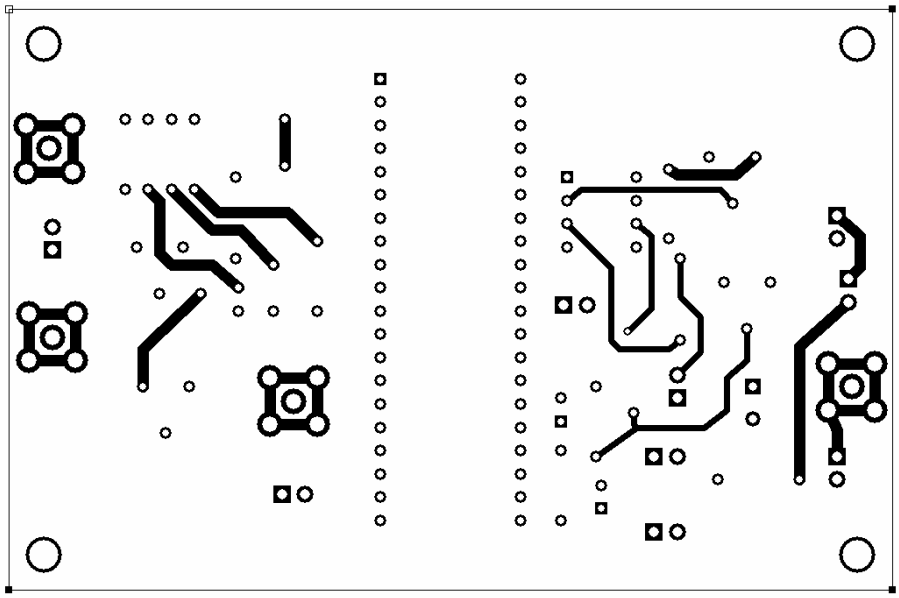

Fig. 75. Bottom layer of PCB from top view.

APPENDIX B
TEST BOARD SCHEMATIC

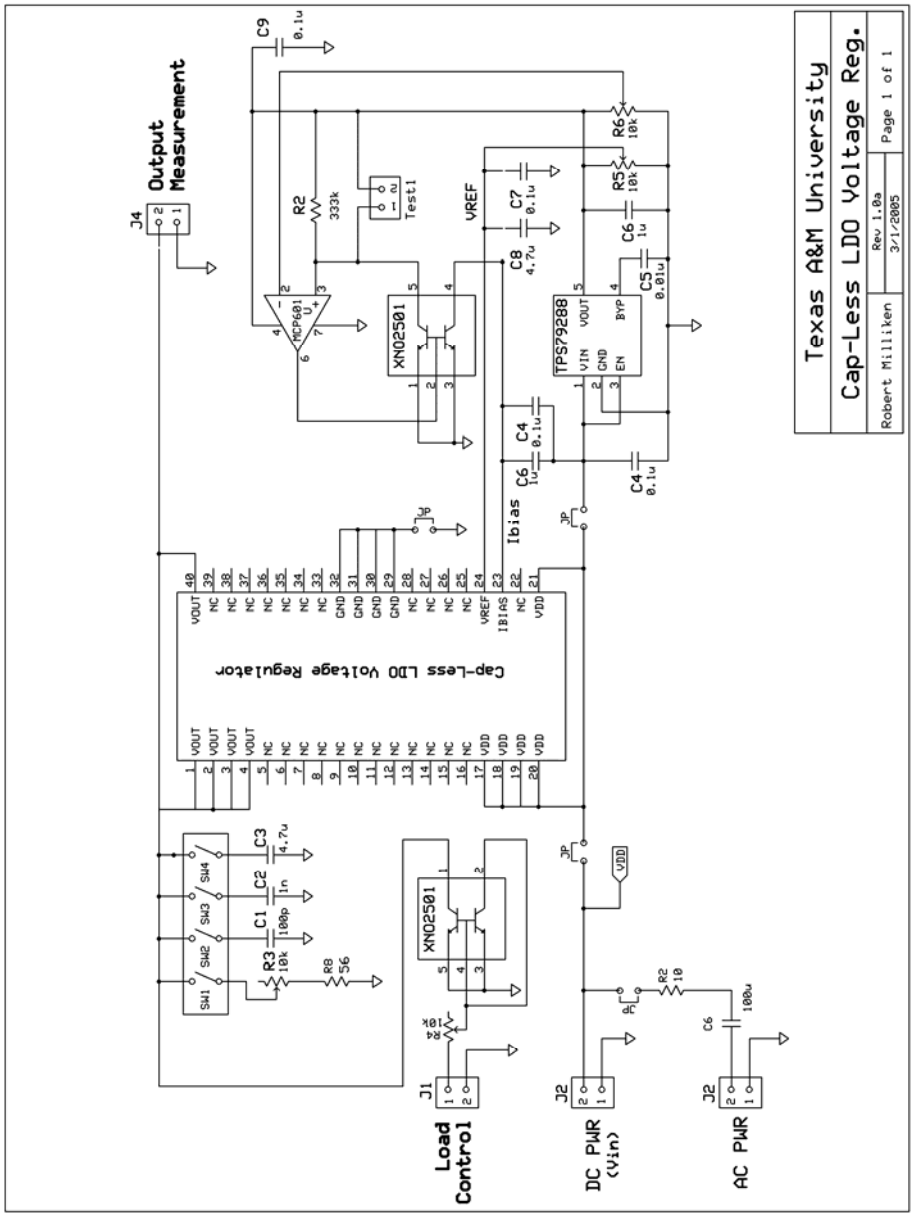

Fig. 76. Test board schematic diagram.

VITA

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