DESIGN OF A VARIABLE GAIN AMPLIFIER FOR AN ULTRA WIDEBAND RECEIVER

A Thesis

by

SIVASANKARI KRISHNANJI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2005

Major Subject: Electrical Engineering

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ABSTRACT

Design of a Variable Gain Amplifier for an Ultra Wideband Receiver.

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A fully differential CMOS variable gain amplifier (VGA) has been designed for an ultra-wideband receiver. The VGA comprises of two variable gain stages followed by a post amplifier stage. The interface between the digital control block and the analog VGA is formed by a digital-to-analog converter and an exponential voltage generator. The gain of the VGA varies dB-linearly from 0 to 52 dB with respect to the control voltage. The VGA is operated in open loop with a bandwidth greater than 500 MHz throughout the gain range to cater to the requirements of the ultra-wideband system. The noise-to-power ratio of the VGA is -23.9 dB for $1V_{p-p}$ differential input signal in the low gain setting, and the equivalent input referred noise is 1.01 V^2 for the high gain setting. All three stages use common mode feedback to fix and stabilize the output DC levels at a particular voltage depending on the input common-mode requirement of the following stage. DC offset cancellation has also been incorporated to minimize the input referred DC offset caused by systematic and random mismatches in the circuit. Compensation schemes to minimize the effects of temperature, supply and process variations have been included in the design. The circuit has been designed in 0.18μm CMOS technology, and the post layout simulations are in good agreement with the schematic simulations.

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CHAPTER I

INTRODUCTION

Variable gain amplifiers (VGAs) have a wide range of applications in electronic systems, especially in those requiring an automatic gain control loop. In communication systems, they play an indispensable role in receivers by controlling the incoming signal's power level and normalizing the average amplitude of the signal to a reference value. This helps in optimizing system capabilities and reducing the complexity of circuits designed to extract the correct timing information and data at the receiving end.

The current thesis work is directed towards the design of a variable gain amplifier for an ultra-wideband (UWB) system [1]. The need to extract the maximum out of the finite and increasingly valuable spectrum prompted the development of UWB systems with very low power spectral densities. These systems share the spectrum already allocated to certain established technologies without causing significant interference. The Federal Communications Commission (FCC) defines UWB as a signal that occupies more than 500 MHz of bandwidth in the 3.1 to 10.6 GHz frequency band. The main application of UWB products is in the consumer electronics industry for Personal Area Networks (PAN), enabling wireless connectivity between different devices such as computers, personal digital assistants, handheld personal computers, printers, digital-imaging systems, speakers, pagers and cellular phones. UWB technology is currently being explored as a very promising solution for the IEEE 802.15.3a standard. This standard provides specifications for low-complexity, low cost, low power, high-data rate wireless connectivity among devices in a PAN. Data rates of 110, 200 and 480 Mb/s impose stringent requirements that are expected to be met by the UWB technology.

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Fig. 1 shows the block diagram of a UWB transceiver. The VGA takes its position between the notch filter and the analog to digital converter in the receiver portion of the transceiver.

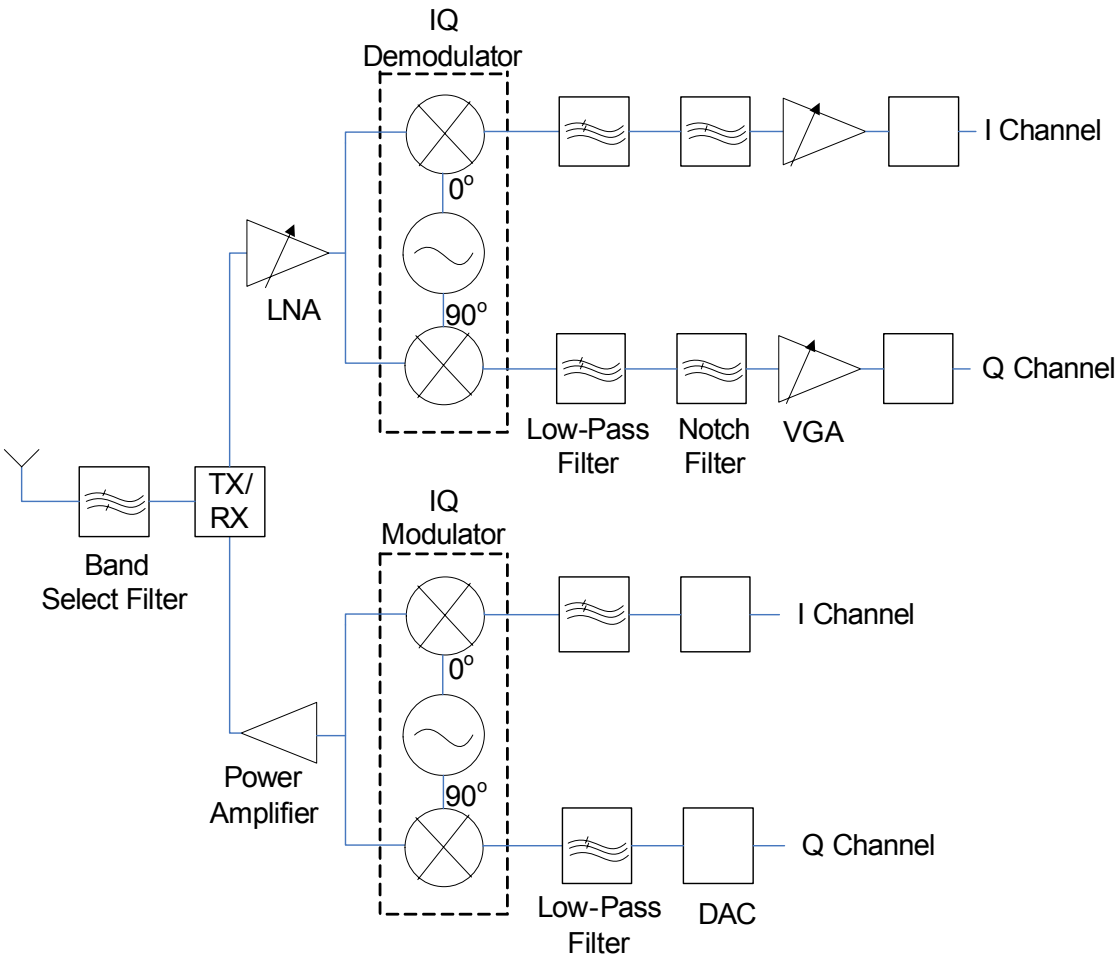

Fig. 1. Block diagram of a UWB transceiver

Selection of the UWB receiver architecture is a major decision that directly affects the overall cost, power, number of external components, receiver sensitivity and selectivity [2]. The analog front end of the transceiver plays a very important role with

respect to the above mentioned issues. The main signal processing operations involved before demodulation are frequency translation to the baseband, signal amplification and filtering to strengthen the received signal and eliminate the surrounding interferers, and digitization for further demodulation of the signal in the DSP. Normally, filtering and amplification operations are done in the baseband after downconverting the signal. The variable gain amplifier takes its position in the baseband section after the filters and before the analog-to-digital converter, in order to provide appropriate gain settings depending on the required amplification of the incoming signal. The gain of the VGA is controlled by the DSP section. It is shown in Ref.[3] that if the VGA gain varies exponentially with respect to the control voltage, the settling time of the AGC loop is constant and independent of the absolute gain. This improves the efficiency of the AGC loop and enables it to operate over a wide dynamic range. The linearity and the dynamic range of the VGA affect the overall third order input intercept point (IIP3) and noise Fig. of the receiver. Hence one of the main requirements of the VGA is to provide good linearity for a wide range of signal swing. Other important aspects of the VGA design include bandwidth, group delay, DC offset cancellation, power supply and common mode rejection ratios, temperature and supply independence and power consumption. For optimum performance, the bandwidth, group delay response and the output noise should remain relatively constant over the entire gain range of the VGA. Dynamic DC offset compensation has to be incorporated in the design since a small DC offset can be amplified by the VGA to a level that saturates the following stages or may cause the output signal to be clipped.

A number of VGA topologies that incorporate an exponential gain control characteristic have been reported previously [4]-[7]. In Ref.[4], to achieve a gain that varies dB-linearly with respect to the control voltage, a VGA that implements the following pseudo exponential function is proposed:

$$gain = \left(\frac{1+x}{1-x}\right)^n \tag{1}$$

However, the region over which the polynomial approximates the logarithmic function is limited. To overcome this limitation, [5] uses a Taylor series approximation of the log function

$$e^x = 1 + x + \frac{x^2}{2} \tag{2}$$

This method increases the range over which the gain is dB-linear with respect to the control voltage, but at the cost of reduced bandwidth and increased design complexity. The pseudo-exponential gain control method is analyzed in detail in Ref.[7], but the VGA designed for the same suffers from poor frequency response. A VGA with a simple and effective technique for DC-offset cancellation is described in Ref.[8]. A very wide bandwidth has been achieved with a 53-dB gain range. A disadvantage of this solution is the linear-in-magnitude gain control, which increases the settling time of the AGC loop in which the VGA is used. A VGA based on the Gilbert cell multiplier is proposed in Ref.[9]. The gain range of the VGA is only 36 dB, varying from -17 dB to 19 dB.

In this thesis, a fully differential VGA has been developed in 0.18μm CMOS technology. The VGA has a dB-linear gain range of 0-53 dB while maintaining a bandwidth greater than 500 MHz for all gains. Various issues that have been addressed in the work are linearity, noise performance, power consumption, DC offset cancellation and minimization of temperature, supply and process variations.

The thesis is organized as follows. The fundamental concepts involved in the design of the VGA are discussed in detail in Chapter II. The various techniques implemented in the circuit to improve its performance are described and analyzed in the same chapter. The proposed VGA is presented in Chapter III. Simulation results of the schematic and the layout are included in Chapter IV, followed by some conclusions in Chapter V.

CHAPTER II

FUNDAMENTALS OF VGA DESIGN

The design of an amplifier requires a detailed analysis of the trade-offs involved in meeting the specifications. For instance, the higher the gain of the amplifier, the lower its bandwidth and the higher its non-linearity. Hence, selection of a particular topology is based upon the feasibility of the design meeting most of the specifications, as well as a careful consideration of the compromises that need to be made for certain parameters while ensuring that the system still works as expected.

A. Gain and Bandwidth Specifications

A simple differential amplifier is given in Fig. 2. The gain of this amplifier is given by

$$A_v = g_m (r_{o2} \| r_{o4}) \tag{3}$$

where g_m is the transconductance of the input transistors M1 and M2. The -3dB bandwidth of the amplifier is given by

$$\omega_{-3dB} = \frac{1}{C_L (r_{o2} \| r_{o4})} \tag{4}$$

Equations (3) and (4) indicate that the gain of the amplifier is directly proportional and the -3 dB bandwidth is inversely proportional to its output resistance, leading to a trade-off between the maximum gain that can be achieved and the speed of the amplifier. Two

stage amplifiers could be implemented to obtain higher gain, at the cost of additional poles and increased power consumption.

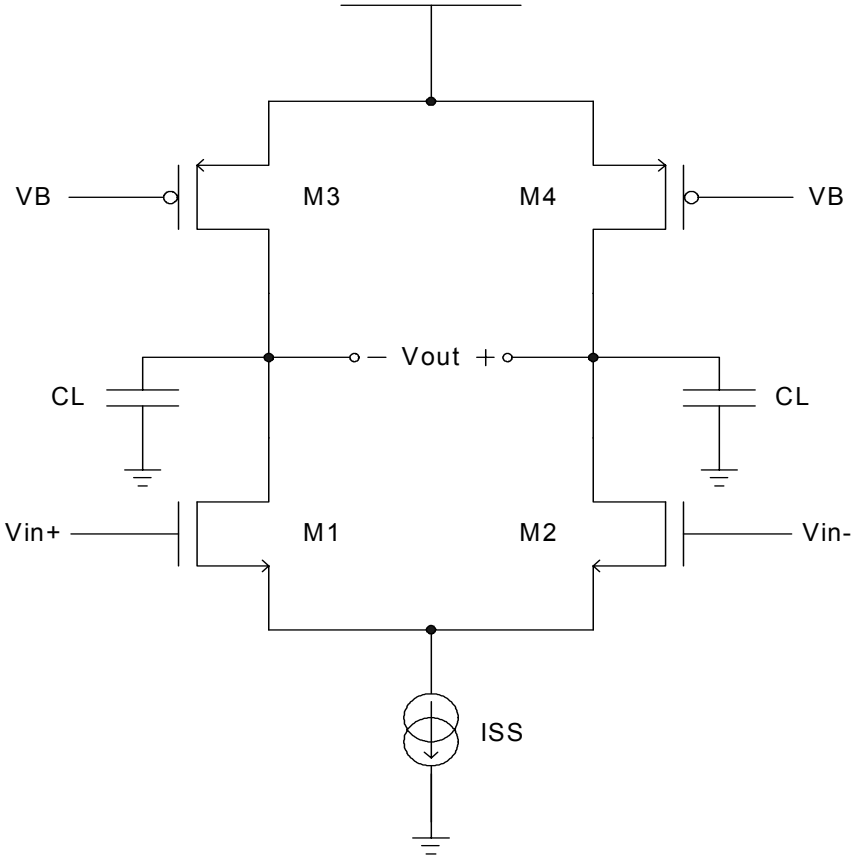

Fig. 2. Differential amplifier with active load

1. Cascoding

By compromising the output voltage swing, the same gain as a two stage amplifier could be obtained by using a cascode structure with lower power dissipation. The gain of the cascode stage shown in Fig. 3 is given by

$$A_v = g_{m1} r_{o1} [(g_{m2} + g_{mb2}) r_{o2} + 1] \tag{5}$$

$$A_v \approx g_{m1} g_{m2} r_{o1} r_{o2} \tag{6}$$

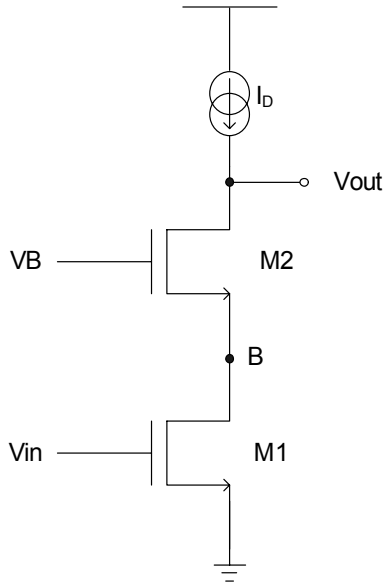

Fig. 3. Cascode amplifier

An advantage of the cascode structure over a common-source stage is the significant reduction in the Miller effect observed by the gate-drain capacitor C_{GD1} due to the low impedance seen by the capacitor, looking into node B, for small values of R_D [10]. The pole associated with the capacitors at node B is given approximately by

$$\omega_{-3dB} \approx \frac{g_{m2} + g_{mb2}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}} \tag{7}$$

This normally results in a better frequency response of the cascode structure as compared to a simple common-source amplifier. A disadvantage of the cascode structure

is its limited output voltage swing, as a result of which it is not used frequently in low voltage applications. Higher voltage swing can be obtained by using a folded cascode structure as shown in Fig. 4. The primary advantage of this topology is the availability of more headroom for the transistors, hence avoiding stacking of the cascode transistor on top of the input device. However, the folded cascode amplifier generally provides lower gain at lower bandwidth (due to lowering of the pole at the folding point) while consuming higher power.

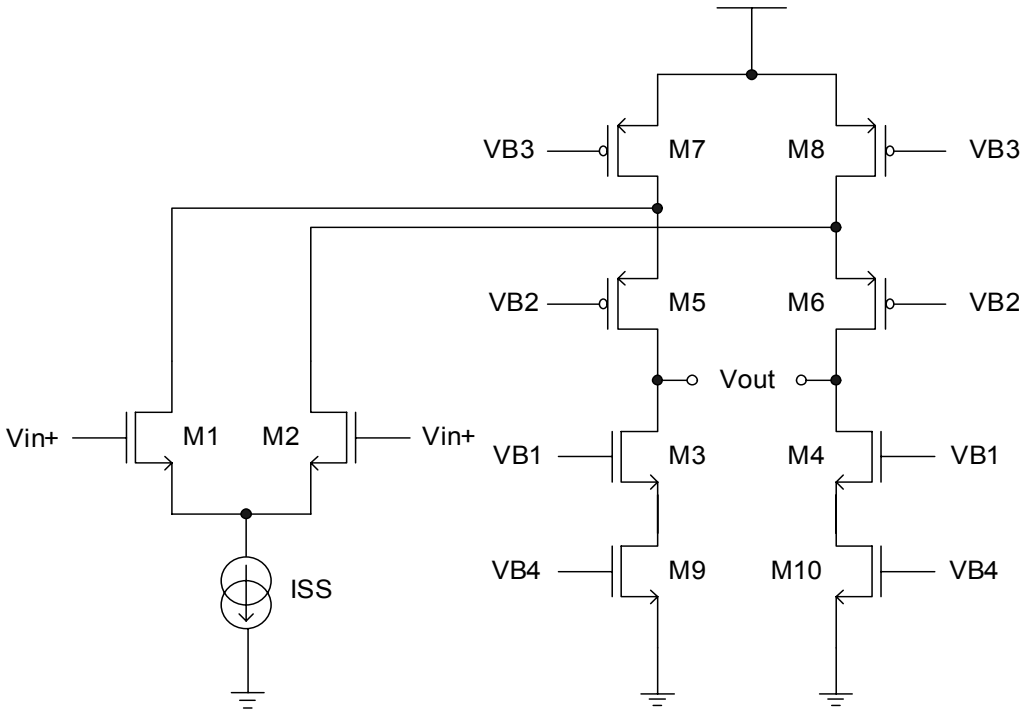

Fig. 4. Folded cascode amplifier

2. Gain boosting in differential amplifiers with diode connected loads

In differential pair amplifiers with diode-connected loads, the loads consume voltage headroom, limiting the output voltage swing, gain and the input common mode

range. In order to obtain a higher gain, the transconductance of the load transistor has to be decreased. This can be done by decreasing the W/L value of the load. However, a disadvantage of this solution is the corresponding increase in the overdrive voltage, which in turn lowers the output common mode level as well as the voltage swing. This problem can be avoided by adding PMOS current sources [10] in parallel to the load transistors, as indicated in Fig. 5. Since the current is now split between the load and the current source, the W/L value of the load transistor can be decreased without changing the overdrive voltage. Hence, the transconductance of the load can be decreased without compromising the output voltage swing.

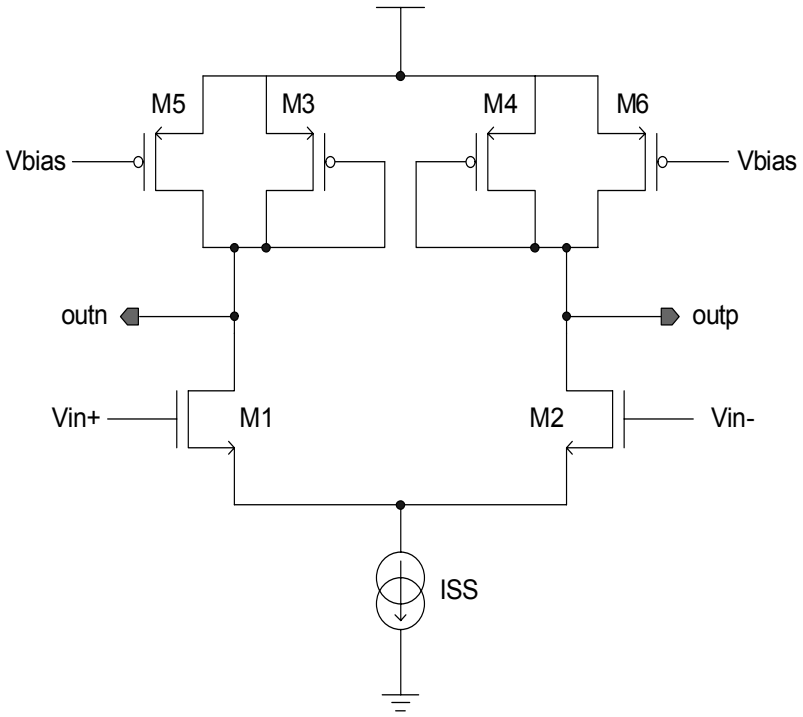

Fig. 5. Addition of current sources to increase the gain of differential amplifier with diode connected load

If transistors M5 and M6 of Fig. 5 carry 40% of the drain current of M1 and M2, and the load transistors M3 and M4 carry the remaining 60%, their transconductance

decreases by a factor of 2/5 since the W/L ratios of M3 and M4 can also be decreased by the same amount without affecting their overdrive voltage. Thus, the differential gain increases by approximately 5/2 times that of the gain when the PMOS current sources are not included in the circuit. A disadvantage of this method of increasing the gain is that the current sources add parasitic capacitances to the output node of the circuit, slightly lowering the -3dB bandwidth.

3. Capacitive neutralization to increase bandwidth

One of the commonly used techniques other than cascoding to reduce the Miller effect experienced by the gate-to-drain capacitor of the input transistors in a fully differential amplifier is capacitive neutralization [11], which is illustrated in Fig. 6. This technique is sometimes used in wideband circuits to increase the bandwidth of multi-stage amplifiers [12].

Without including capacitance C_{GDN}, the capacitance seen at the gate of transistor M1 is given by:

$$C_{in} = C_{GS1} + C_{GD1}(1 - A_v)\,, \tag{8}$$

where A_v is the gain from the gate to the drain of M1. Since the amplifier is perfectly balanced, the gain from the gate of M1 to the drain of M2 is $-A_v$. As a result, the total capacitance at the gate of M1 after including capacitor C_{GDN} in the circuit is given by

$$C_{in} = C_{GS1} + C_{GD1}(1 - A_v) + C_{GDN}(1 + A_v) \tag{9}$$

If the value of C_{GDN} is selected such that $C_{GDN} = C_{GD1}$, equation (9) simplifies to

$$C_{in} = C_{GS1} + 2C_{GD1} \tag{10}$$

This is very similar to the input capacitance of a cascode configuration.

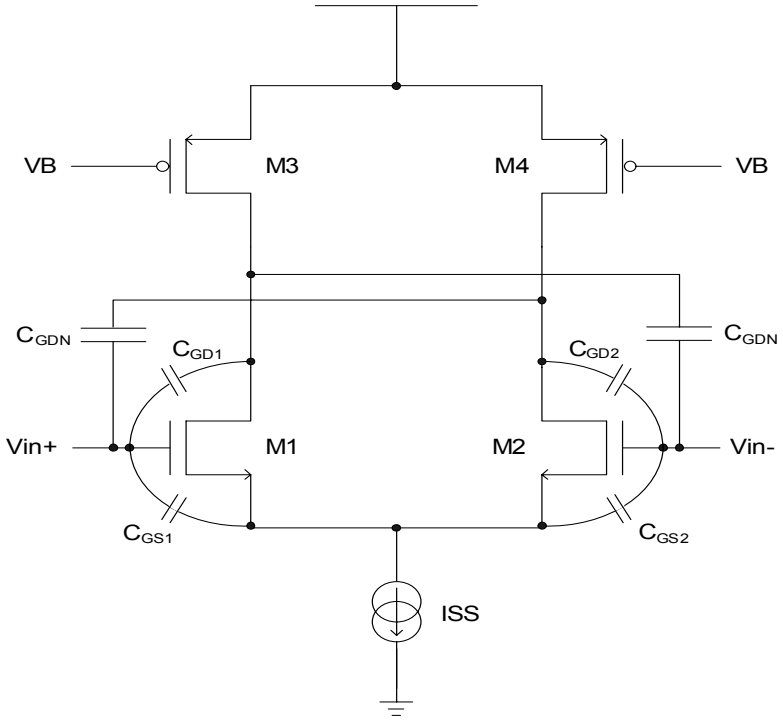

Fig. 6. Differential amplifier with capacitive neutralization

Capacitors C_{GDN} are implemented as transistors M21 and M22 as shown in Fig. 7. Since M1 and M2 are in the saturation region,

$$V_{DS}(M1, M2) \geq V_{GS}(M1, M2) - V_{T1} \tag{11}$$

$$\Rightarrow V_{GD}(M1, M2) \leq V_{T1} \tag{12}$$

$$\Rightarrow V_{GS}(M21, M22) \leq V_{T1} \tag{13}$$

Hence, transistors M21 and M22 operate in the cut-off region, with C_{GDN} being equal to the sum of their gate-to-drain and gate-to-source overlap capacitances.

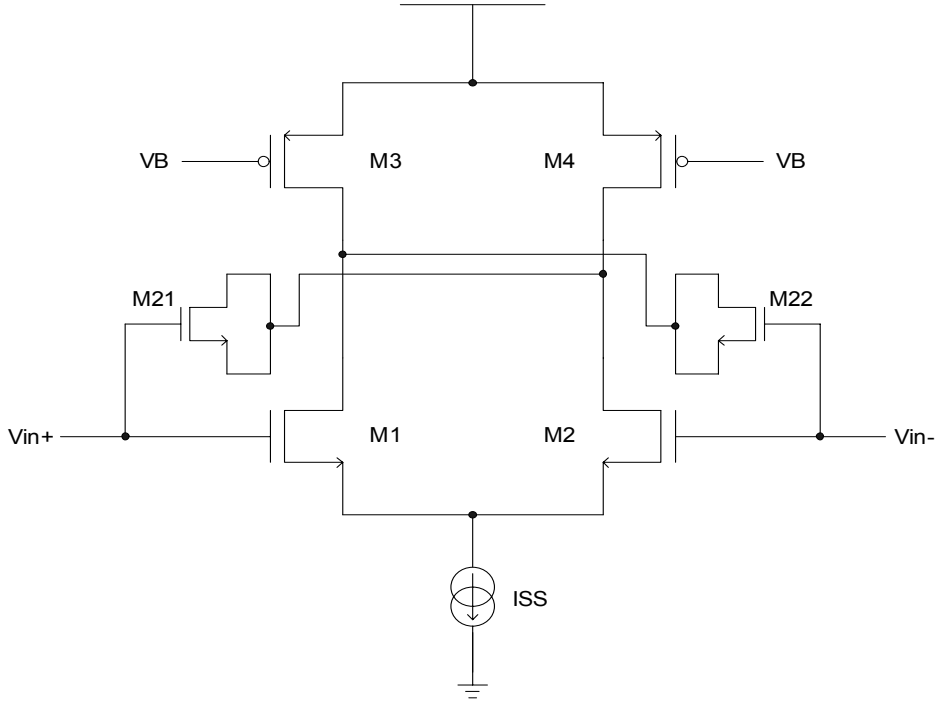

Fig. 7. Capacitive neutralization with MOS transistors as capacitors

A disadvantage of the capacitive neutralization technique is that the junction capacitances of transistors M21 and M22 in Fig. 7 load the nodes to which their drains are connected. This results in a lowering of the pole associated with that node.

B. Group Delay

Group delay is an important parameter for the VGA, and it is defined as the rate of change of phase with respect to frequency. It is the measure of the slope of the phase

shift versus linear frequency plot, and is expressed in seconds. For a circuit or a system, constant group delay indicates that all frequencies experience the same delay through the system.

Group delay distortion occurs when different frequencies propagate through a component at different speeds. This type of distortion affects the output significantly especially in audio systems where higher audio frequencies tend to travel faster than lower frequencies. If there is a difference in the speed of propagation of various frequencies, the output becomes less coherent with a sense of 'smear'[1] in the generated waveform.

C. Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

A fully differential structure has the advantages of high CMRR and PSRR, and higher output voltage swing compared to the single ended structures.

1. Small signal characteristics of differential amplifiers

Differential amplifiers are normally considered to have three input terminals (v_{i1}, v_{i2} and ground) and three output terminals (v_{o1}, v_{o2} and ground). Each output can be represented as follows:

$$v_{o1} = A_{11}v_{i1} + A_{12}v_{i2} \tag{14}$$

$$v_{o2} = A_{21}v_{i1} + A_{22}v_{i2} \tag{15}$$

For the given loading conditions, A_{11}, A_{12}, A_{21} and A_{22} are the small signal voltage gains as defined below:

[1] http://www.udel.edu/Biology/rosewc/msp_biomech/html/notes/Filter%20Design%20Guide.html

$$A_{11} = \left.\frac{v_{o1}}{v_{i1}}\right|_{v_{i2}=0} \tag{16}$$

$$A_{12} = \left.\frac{v_{o1}}{v_{i2}}\right|_{v_{i1}=0} \tag{17}$$

$$A_{21} = \left.\frac{v_{o2}}{v_{i1}}\right|_{v_{i2}=0} \tag{18}$$

$$A_{22} = \left.\frac{v_{o2}}{v_{i2}}\right|_{v_{i1}=0} \tag{19}$$

The differential output, v_{od} and the common mode output v_{oc} are respectively given by:

$$v_{od} = v_{o1} - v_{o2} \tag{20}$$

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2} \tag{21}$$

From equations (14) – (19), v_{od} and v_{oc} can be represented as follows:

$$v_{od} = \left(\frac{A_{11} - A_{12} - A_{21} + A_{22}}{2}\right) v_{id} + \left(A_{11} + A_{12} - A_{21} - A_{22}\right) v_{ic} \tag{22}$$

$$v_{oc} = \left(\frac{A_{11} - A_{12} + A_{21} - A_{22}}{4}\right) v_{id} + \left(\frac{A_{11} + A_{12} + A_{21} + A_{22}}{2}\right) v_{ic} \tag{23}$$

where v_{id} and v_{ic} are the differential and common mode input signals respectively, given by:

$$v_{id} = v_{i1} - v_{i2} \tag{24}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} \tag{25}$$

From equations (22) – (25), v_{od} and v_{oc} can be rewritten as follows:

$$v_{od} = A_{dm} v_{id} + A_{cm-dm} v_{ic} \tag{26}$$

$$v_{oc} = A_{dm-cm} v_{id} + A_{cm} v_{ic} \tag{27}$$

where A_{dm} is the differential mode gain - the change in the differential output voltage per unit change in the differential input, A_{cm} is the common-mode gain – the change in the common mode output voltage per unit change in the common-mode input, $A_{dm\text{-}cm}$ is the differential to common mode gain – the change in the common mode output per unit change in the differential input, $A_{cm\text{-}dm}$ is the common mode to differential mode gain – the change in the differential output per unit change in the common mode input.

The main advantage of differential amplifiers over single ended amplifiers is that they amplify only changes in the differential input while they reject changes in the common mode input. Hence, for a perfectly balanced differential amplifier, when the input is purely differential, the output will also be purely differential. Therefore, such structures exhibit a high CMRR since the same common mode change appears at both outputs due to symmetry. CMRR is defined as:

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| \tag{28}$$

For the same reason, differential structures also exhibit a higher PSRR, which represents the ability of amplifiers to reject noise in the supply lines.

Due to non-ideal behavior, differential amplifiers usually have a certain common mode gain (A_{cm}) as a result of which the output common mode voltage changes when there is a change in the input common mode, though it does not affect the differential output voltage if the circuit is perfectly balanced. If the output DC level changes by such an extent that it changes the operation region of certain transistors in the same stage or the input transistors of the following stage, the amplifier would fail to function as required. Hence, to fix the output DC level to a certain value and minimize its variation due to changes in the input common mode, common mode feedback circuits are normally employed for this purpose.

2. Common mode feedback circuit

In differential amplifiers with resistive loads, the output common mode voltage is clearly defined as $V_{DD} - I_R R$ where I_R is the current through the load. However, in high gain amplifiers with active current source loads, the common mode voltage is usually not very well defined. The main problem with high gain amplifiers is that normally, a small difference exists in the currents through the PMOS loads and the NMOS input transistors, which flows through the output resistance, creating an output voltage change,

$$\Delta V = (I_{PMOS} - I_{NMOS}) R_{out} \tag{29}$$

Since the output impedance is quite high and the current error depends on mismatches, the voltage error may be large, pushing certain transistors into the triode region. To avoid this problem and fix the common mode voltage to a certain value which would maximize the output voltage swing and also ensure that all the transistors are in the saturation region, a common mode feedback (CMFB) circuit is designed. This circuit, with a high loop gain, introduces negative feedback and adjusts the output DC level to a

specific value irrespective of the changes in the input common mode voltage. It also decreases the variation of the output DC voltage with temperature, supply and process.

A CMFB circuit primarily consists of three blocks; a CM sense block that detects the change in the common mode level, an error amplifier that amplifies the difference between the detected common mode voltage and a reference voltage (V_{CM}) and thirdly, a CM control block which is part of the main amplifier. By varying some parameter of the CM control block such as a voltage or current, the common mode voltage is forced back to the value of V_{CM}. The block diagram of a differential amplifier with a CMFB loop is given in Fig. 8.

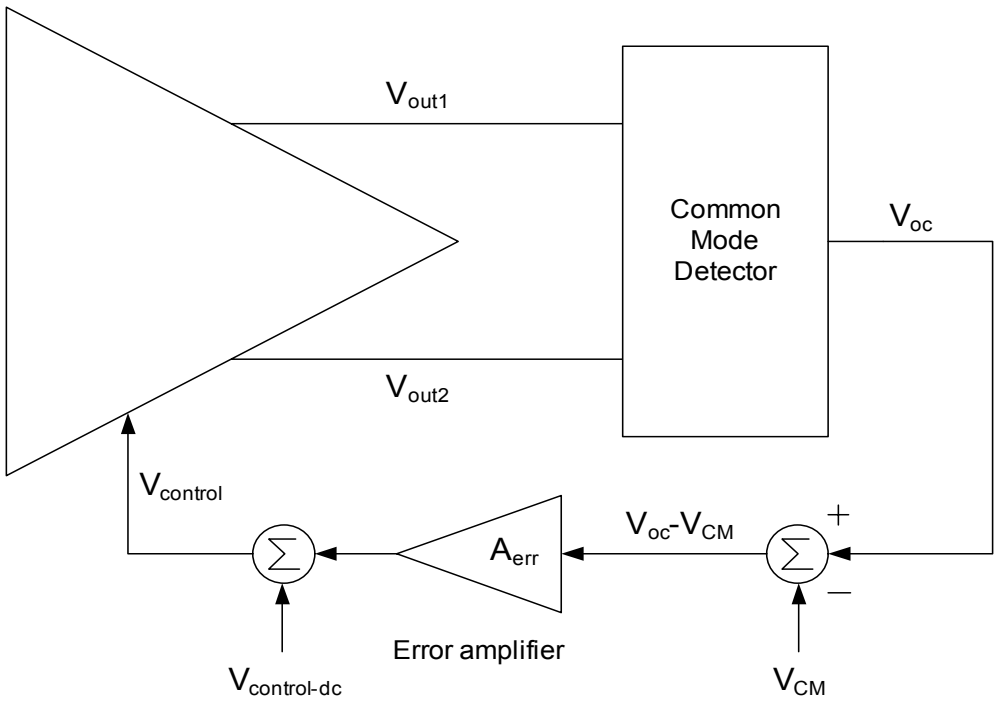

Fig. 8. Block diagram of a CMFB loop

D. Noise-to-Power Ratio

In communication systems, linearity of amplifiers is normally measured by evaluating the third order input intercept point (IIP3). Due to the inherent non-linearity of amplifiers, an input signal *x(t)* results in an output as given below:

$$y(t) = k_0 + k_1 x(t) + k_2 x^2(t) + k_3 x^3(t) \tag{30}$$

The above relation is based on the assumption that the circuit is memoryless and is driven by a small signal excitation reasonably below the 1 dB compression point (1 dB compression point is the point at which the gain deviates from its ideal small signal value by 1dB). It follows from equation (30) that when the input signal is of the form $x(t) = x\cos(\omega_1 t) + x\cos(\omega_2 t)$, the in-band output of interest is [13]:

$$y_{in-band}(t) = k_1 x[\cos(\omega_1 t) + \cos(\omega_2 t)] + \frac{k_3}{4} x^3 \begin{Bmatrix} 9\cos(\omega_1 t) + 9\cos(\omega_2 t) + \\ 3\left[\cos(2\omega_2 - \omega_1)t + \cos(2\omega_1 - \omega_2)t\right] \end{Bmatrix} \tag{31}$$

It can be observed from the above equation that the third order distortion components include nine new mixing products at ω_1 and ω_2 and three at frequencies $2\omega_1$-ω_2 and $2\omega_2$-ω_1. The components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 are the intermodulation distortion components.

The fundamental component in equation (31) increases with a slope of 1dB/dB while the third order intermodulation component rises at a rate of 3dB/dB with respect to the input power. The third order input intercept point is defined as the input power for which the distortion power at $2\omega_1$-ω_2 (or $2\omega_2$-ω_1) is the same as the linear output power at ω_1 (or ω_2). Normalized to a 1Ω load resistance, the IIP3 is given by:

$$X_{IIP3}^2 = \frac{4}{3}\frac{k_1}{k_3} \tag{32}$$

Intermodulation distortion ratio (IMR) is defined as the ratio between the linear output power per tone and the output power of adjacent channel tones. The value of the two-tone IMR normalized to the total linear output power is:

$$IMR_{two-tone} = \frac{\frac{k_1^2}{2}X^2}{9\frac{k_3^2}{32}X^6} = \frac{16}{9}\frac{k_1^2}{k_3^2}\frac{1}{X^4} \tag{33}$$

With increasing complexity of communication systems, the two-tone standard is no longer a sufficient test for the linearity of amplifiers used in such systems. More robust figures of merit which give a better representation of the system's final operation are used to characterize circuits [13], [14]. The measurement setup includes excitation of the circuit with a multi-tone signal in which all the tones are equally spaced and have uncorrelated phases. These figures of merit include:

1. Adjacent Channel Power Ratio (ACPR) – This is the ratio between the adjacent channel (upper or lower) integrated output power and the total linear output power of the useful signal band.
2. Noise-to-Power Ratio (NPR) – NPR is the ratio between the in-band distortion and the useful signal power per tone when the circuit is excited with a multi tone signal that has a prelocated notch (i.e. a slice of the signal spectrum is removed).
3. M-IMR – This is the ratio between the linear output power and the highest distortion tone power outside but close to the useful band. M refers to the number of tones used in the input signal.
4. Co-channel Power Ratio (CCPR) – CCPR is the ratio between the total distortion power collected in the input bandwidth and the total linear output power. CCP cannot be directly measured because the in-band distortion components are normally

masked by the circuit's linear output component. Unlike the NPR test, the CCPR does not involve shutting down of any tone, and the distortion in that particular band is measured in the presence of the corresponding input spectral line. Hence, the CCPR is a more accurate estimate of the in-band distortion due to the non-linear components that arise when the circuit is excited by a multi tone input. The measured value of NPR is normally lower than the actual value by about 6dB.

E. DC Offset

There are two types of offsets in analog circuits that affect the performance of the circuits:

1. Random offset
2. Systematic offset

Systematic offset occurs due to the non-idealities of a circuit even when all the elements of the circuit are perfectly matched. Random offset occurs due to mismatches in supposedly matched devices. For example, the threshold voltage variation in matched devices in the same chip gives rise to differences in their overdrive voltages, resulting in random mismatch. These mismatches give rise to a nonzero input offset voltage in amplifiers. The input offset voltage is the differential input voltage that has to be applied to force the differential output to zero. In multistage amplifiers with high gain in each stage, the input-referred offset voltage mainly depends on the design of the first stage.

1. Systematic offset voltage

Systematic offset voltage is closely related to the DC power supply rejection ratio of amplifiers. Its dependence on the supply voltage is a more realistic problem in circuits in which the bias currents depend on the supply voltage. In the two stage amplifier shown in Fig. 9, the two stages have been disconnected to explain the concept of input referred DC offset.

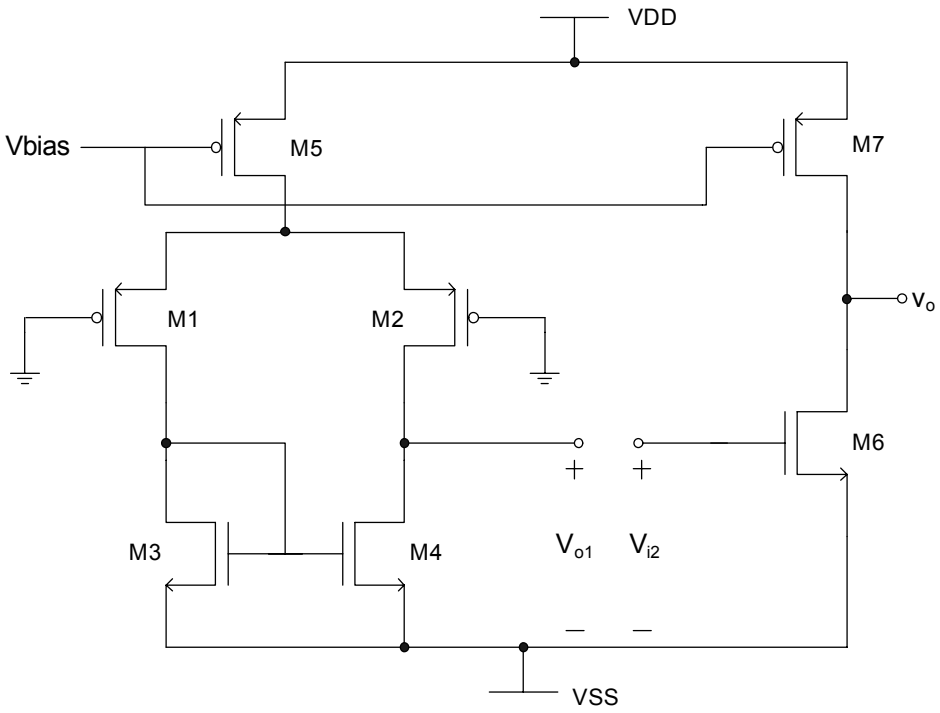

Fig. 9. Input referred offset of a two stage amplifier

If the input voltages are set to zero and perfect matching is assumed, the V_{DS} of M3 (also equal to its V_{GS}) will be equal to the V_{DS} of M4. Then, $V_{DS1} = V_{DS2}$ and $I_1 = I_2 = I_{SS}/2$. Since M3, M4 and M6 are perfectly matched and $V_{GS3} = V_{DS4} = V_{GS6}$, the overdrive voltages of all three transistors are the same. Hence the ratio of their currents to W/L values should also be the same. Therefore:

$$\frac{I_{D3}}{(W/L)_3} = \frac{I_{D4}}{(W/L)_4} = \frac{I_{D6}}{(W/L)_6} \tag{34}$$

$$\Rightarrow \frac{I_{D5}}{2(W/L)_3} = \frac{I_{D5}}{2(W/L)_4} = \frac{I_{D6}}{(W/L)_6} \tag{35}$$

Since
$$\frac{I_{D5}}{I_{D7}} = \frac{(W/L)_5}{(W/L)_7}; \quad I_{D6} = I_{D7}, \tag{36}$$

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_7} \tag{37}$$

The output DC voltage is given by:

$$V_{O,DC} = V_{DS6} - V_{SS} = V_{GS3} - V_{SS} = V_{T3} + V_{ov3} - V_{SS} \tag{38}$$

The systematic offset is obtained by calculating the difference between the value of $V_{O,DC}$ in equation (38) and half the value of the supply voltage. If A_v is the gain of the opamp,

$$V_{OFFSET}(sys) = \frac{V_{T3} + V_{ov3} - V_{SS} - \frac{V_{DD} - V_{SS}}{2}}{A_v} \tag{39}$$

2. Random offset voltage

Random offset could occur due to process variations. There could be mismatch in the loads (active or passive) of amplifiers, channel length and width mismatches between transistors, threshold voltage mismatch and many other such variations. Mismatch in the threshold voltage results in a constant offset component independent of the bias current, and is a strong function of process cleanliness and uniformity. The circuit has to be laid out as symmetrically as possible to minimize random offset.

CHAPTER III

DESIGN OF THE VARIABLE GAIN AMPLIFIER

The design of all the blocks of the UWB receiver was based on specifications derived through system-level simulations in Matlab. Detailed analysis was performed on each block's effect on the various parameters that characterize the behavior of the receiver, and block level specifications were decided after examining the feasibility of designing the blocks to achieve them. The specifications determined for the VGA are listed in Table I.

TABLE I
VGA SPECIFICATIONS

Parameter	Specification
Gain range	0 - 60 dB
-3dB bandwidth	> 600 MHz for the given gain range
NPR (for low gain setting)	-25 dB
Integrated input referred noise	$< 9\ nV^2$
Output voltage swing	$1\ V_{p-p}$

In order to achieve the given specifications, a fully differential CMOS VGA consisting of the following blocks has been designed:

1. Digital to Analog Converter – This unit acts as the interface between the digital control block of the system and the analog core of the VGA.
2. Exponential Voltage Generator – This block converts the linear output voltage of the DAC to an exponentially varying control voltage. The aim of this conversion is to obtain a VGA gain that exhibits a dB-linear characteristic with respect to the control voltage. The gain can be varied linearly in steps of 1dB, reducing its sensitivity to unwanted variations in the control voltage.
3. VGA core comprising of three gain stages, the first two being the variable gain stages and the third, a fixed gain amplifier.

A. Blocks of the VGA

This section gives a description of all the blocks of the VGA and discusses the issues involved in the design of these blocks.

1. Digital-to-analog converter

To reduce the complexity of the DAC, an R-2R ladder as shown in Fig. 10 is used to convert the incoming bits to an analog voltage. The DAC takes six input bits and generates an output based on a reference voltage of 300mV. The output of the binary ladder is given by the following equation:

$$V_{out} = \frac{1}{2^n}\left[2^{n-1}d_1 + 2^{n-2}d_2 + \ldots\ldots + 2^1 d_{n-1} + d_n\right]V_{ref} \tag{40}$$

This equation can be derived using the principle of superposition. The current flowing in each leg is given by:

$$I_1 = \frac{d_1 V_{ref} - V_{out}}{2R} \tag{41}$$

$$I_i = \frac{d_i V_{ref} - [V_{out} - R\sum_{k=1}^{i-1}(i-k)I_k]}{2R}, \qquad i = 2,3,...n+1; \quad d_{n+1} = 0 \tag{42}$$

The power consumed by the binary ladder is the power supplied by the reference voltage source. The power dissipated is given by:

$$P_{dissipated} = \sum_{i=1}^{n} d_i I_i V_{ref} \tag{43}$$

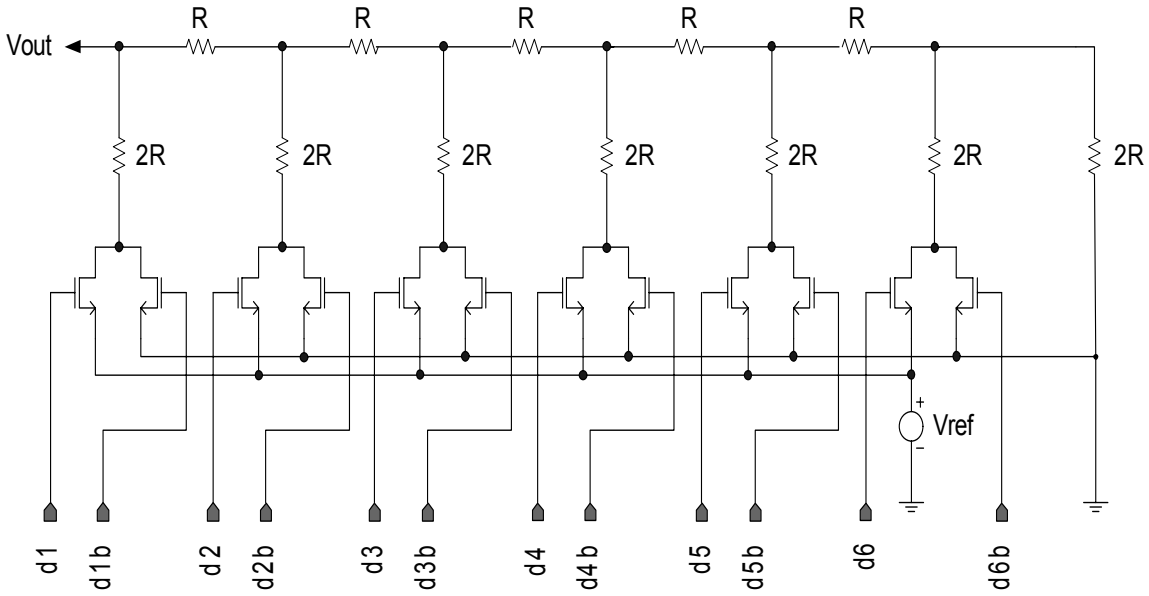

Fig. 10. Schematic of the DAC

The R-2R binary ladder requires switches that will pass either the reference voltage or ground depending on whether the input bit is a 1 or a 0. Since the reference

voltage is 300mV, NMOS switches are used since they pass low voltages at the input properly to the output.

The primary issues concerning the design of the DAC are noise, resistance mismatches and power consumption for this application. According to TSMC mismatch datasheet, the width of the resistor has to be at least 5μm in order to minimize mismatch between resistors. Mismatches in the binary ladder resistors result in differential and integral non-linearity [15]. Differential nonlinearity is the maximum deviation in the output step size from the ideal value of one least significant bit, while integral nonlinearity is the maximum deviation of the input and output characteristics from a straight line passed through its end points. The nonlinearity of a ladder comprising of a large number of segments is smaller than that with a small number of segments. This is because random errors in the value of the resistors tend to average out when many segments are connected in series. Since the DAC is used to generate the voltage that is eventually converted to an exponential voltage and is used as the control voltage of the VGA, the noise of the DAC influences the overall noise-to-power ratio (NPR) of the VGA. Also, the power consumption has to be kept low, for which high values of resistor need to be used. These imply a trade-off between the noise level of the DAC and the power consumed by it.

2. Exponential voltage generator

There are different ways of generating an exponential voltage. In CMOS technology, parasitic bipolar transistors can be used for this purpose since the collector current is an exponential function of the base-to-emitter voltage. The more commonly used methods of obtaining an exponential curve are to approximate the exponential function by using Taylor's series:

$$e^x \approx \frac{1+x}{1-x}, \ |x| < 0.32 \tag{44}$$

$$e^x \approx 1 + x + \frac{x^2}{2},\ -0.575 \le x \le 0.815 \tag{45}$$

A simple way of generating the first expression is shown in Fig. 11. The circuit, comprising of a back to back connection of two current mirrors, is a current to voltage converter with a pseudo exponential characteristic.

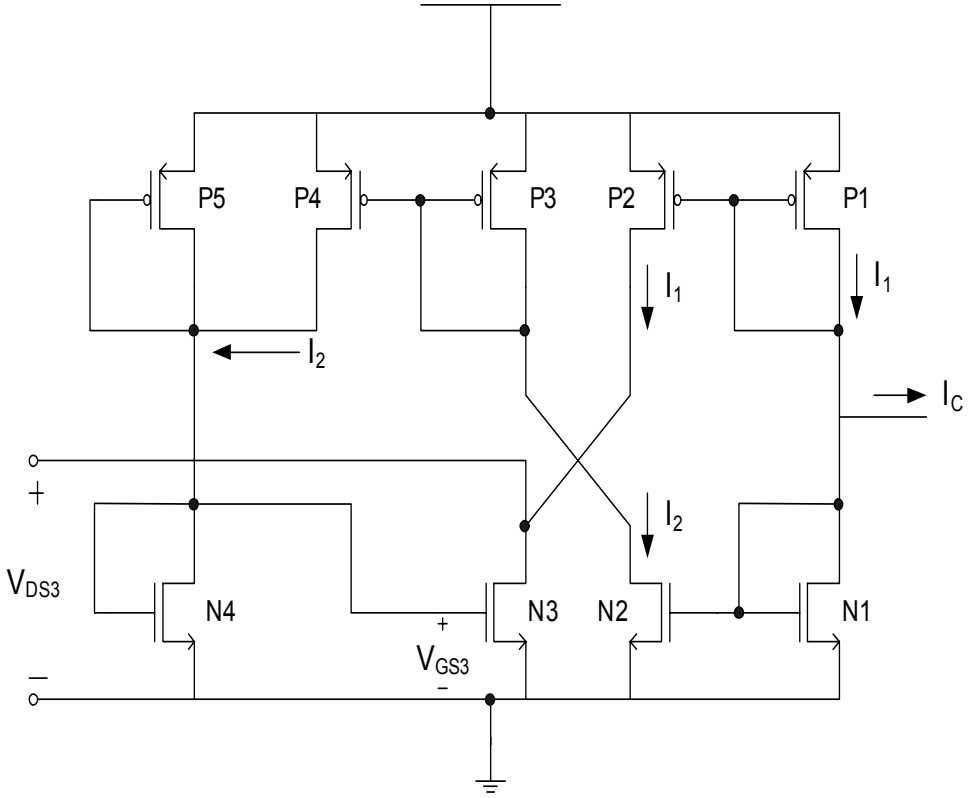

Fig. 11. Generation of the pseudo exponential function given by equation (44)

Currents I_1 and I_2 are given by:

$$I_1 = \frac{K}{2}\left(V_{DD} - V_C - \left|V_{TP}\right|\right)^2 \tag{46}$$

$$I_2 = \frac{K}{2}(V_C - V_{TN})^2 \tag{47}$$

Since $I_C = I_1 - I_2$,

$$V_C = \frac{V_{DD} - |V_{TP}| + V_{TN}}{2} - \frac{I_C}{K(V_{DD} - |V_{TP}| - V_{TN})} \tag{48}$$

Hence,

$$I_1 = \frac{K}{2}\left(\frac{V_{DD} - |V_{TP}| - V_{TN}}{2} + \frac{I_C}{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)}\right)^2 \tag{49}$$

$$I_2 = \frac{K}{2}\left(\frac{V_{DD} - |V_{TP}| - V_{TN}}{2} - \frac{I_C}{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)}\right)^2 \tag{50}$$

The ratio of the two currents is given by:

$$\frac{I_1}{I_2} = \left(\frac{1+y}{1-y}\right)^2; \qquad y = \frac{2I_C}{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)^2} \tag{51}$$

The above ratio corresponds to an approximation of the exponential function exp (2*2y). In the circuit in Fig. 11, transistors P4, P5 and N4 perform the same function as transistors P1, P2 and N1 while the current I_2 that is mirrored into P4 by transistor P3 generates a voltage V_{GS3} across a resistance of value R_{in} seen at the drains of P5 and N4.

$$R_{in} = \frac{1}{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)} \tag{52}$$

This voltage V_{GS3} can be represented by the same equation as V_C with I_C replaced by I_2. Transistor N3 operates in the triode region with a resistance given by:

$$R_{DS} \approx \frac{1}{K\left(V_{GS3} - V_{TN}\right)} \tag{53}$$

With current I_1 flowing through this resistance, the voltage across it is given by

$$V_{DS} = R_{DS} I_1 , \tag{54}$$

which is proportional to I_1/I_2.

Another circuit which realizes equation (45) is given in Fig. 12. The circuit comprises of three blocks – a linear V-I converter, a constant current source and a current squaring circuit (CSC).

The output current of the V-I converter is given by

$$I_{V-I} = 2G_m V_{in} \tag{55}$$

where G_m is the effective transconductance of the V-I converter. The input current of the current squaring block is the sum of I_{V-I} and a constant current $I_{CS} = 4I_o$.

The output of the CSC is:

$$I_{out} = 2I_O + \frac{\left(I_{V-I} + 4I_O\right)^2}{8I_O} \tag{56}$$

After appropriate simplification of the above expression, the output of the exponential function generator can be expressed as:

$$I_{out} \approx 4I_o \exp\left(\frac{G_m}{2I_o} V_{in}\right) \tag{57}$$

This current is converted to a voltage output by passing it through a resistor *Re*.

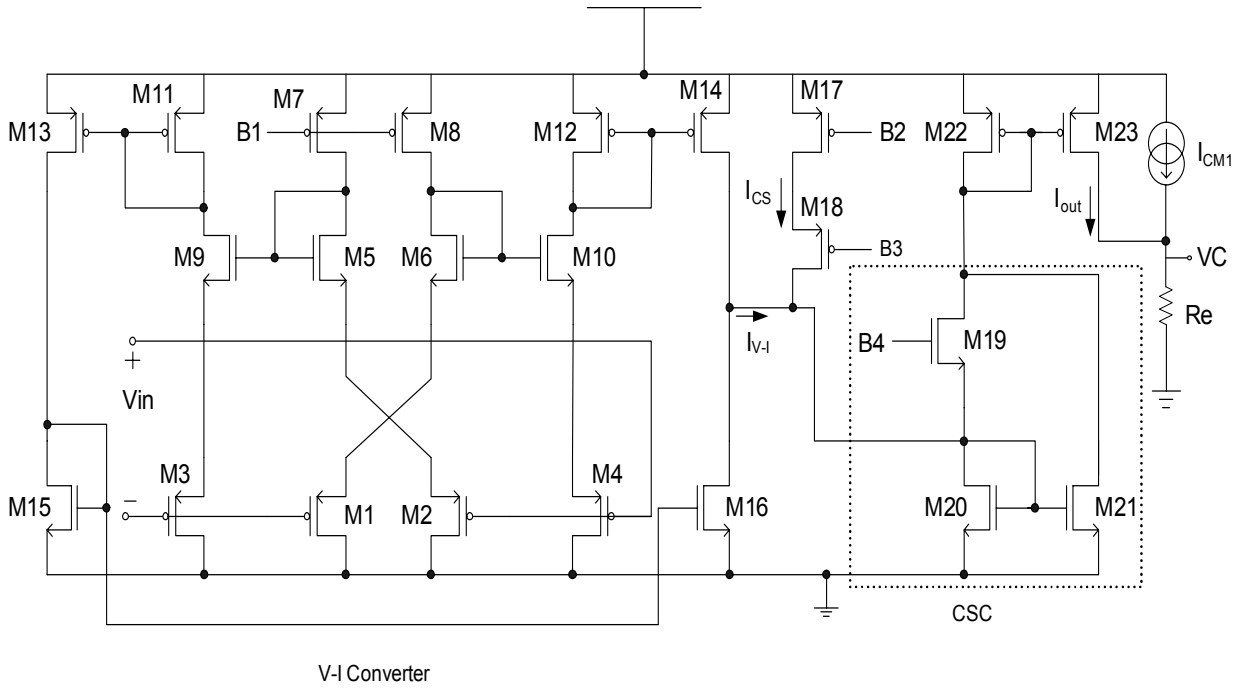

Fig. 12. Generation of the pseudo exponential function given by equation (45)

In this thesis, the square-law relation between the current and the gate-to-source voltage of the MOS transistor has been used to generate the Taylor series expansion. The circuit in Fig. 13 generates the function given by equation (45), where x is the output of the DAC. The output of the DAC, V_x, is level-shifted by the gate-to-source voltage of PMOS M3. This voltage appears at the gate of NMOS M4, generating a current given by:

$$I = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_X + V_{GSP} - V_{TN}\right)^2 \tag{58}$$

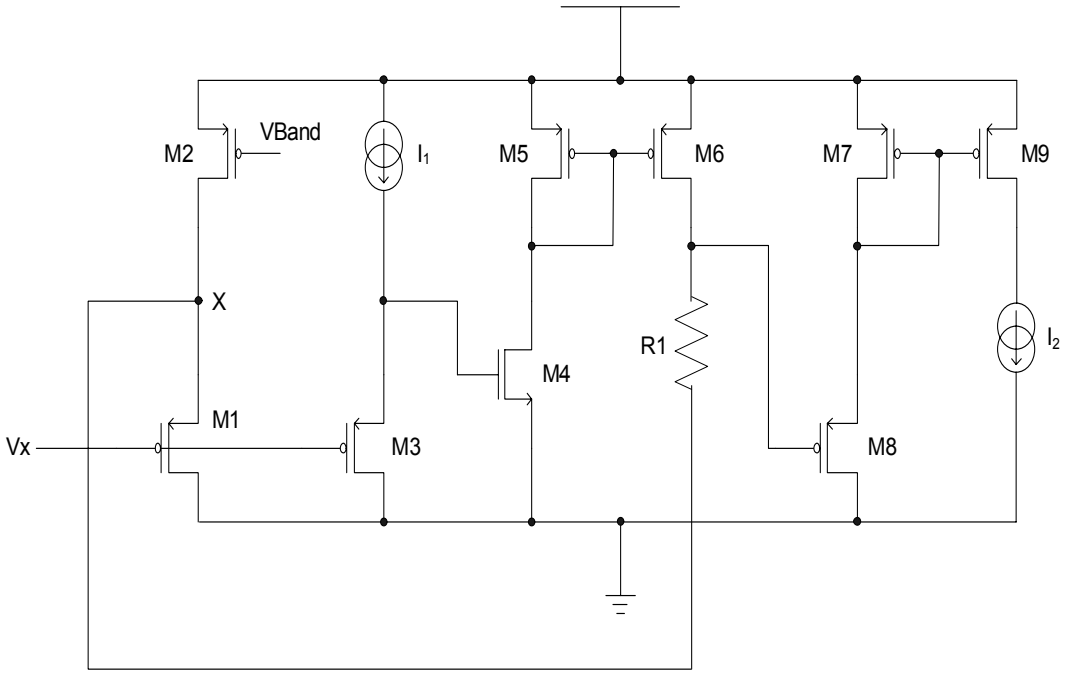

Fig. 13. CMOS exponential voltage generator

The current given by equation (58) is mirrored into a resistor of value

$$R = 1/\left(\mu_n C_{ox}\left(\frac{W}{L}\right)\right), \tag{59}$$

generating a voltage V_R across it, given by

$$V_R = 0.5\left(V_X + V_{GSP} - V_{TN}\right)^2 \tag{60}$$

If $V_{GSP} - V_{TN} = 0.5$, then

$$V_R = \frac{V_x^2}{2} + \frac{V_x}{2} + 0.125 \tag{61}$$

The required output is obtained by level shifting this voltage by $\frac{V_x}{2} + 0.875$.

The output of the exponential voltage generator is shown in Fig. 14. It can be observed from the graph that the output voltage closely follows the ideal exponential curve.

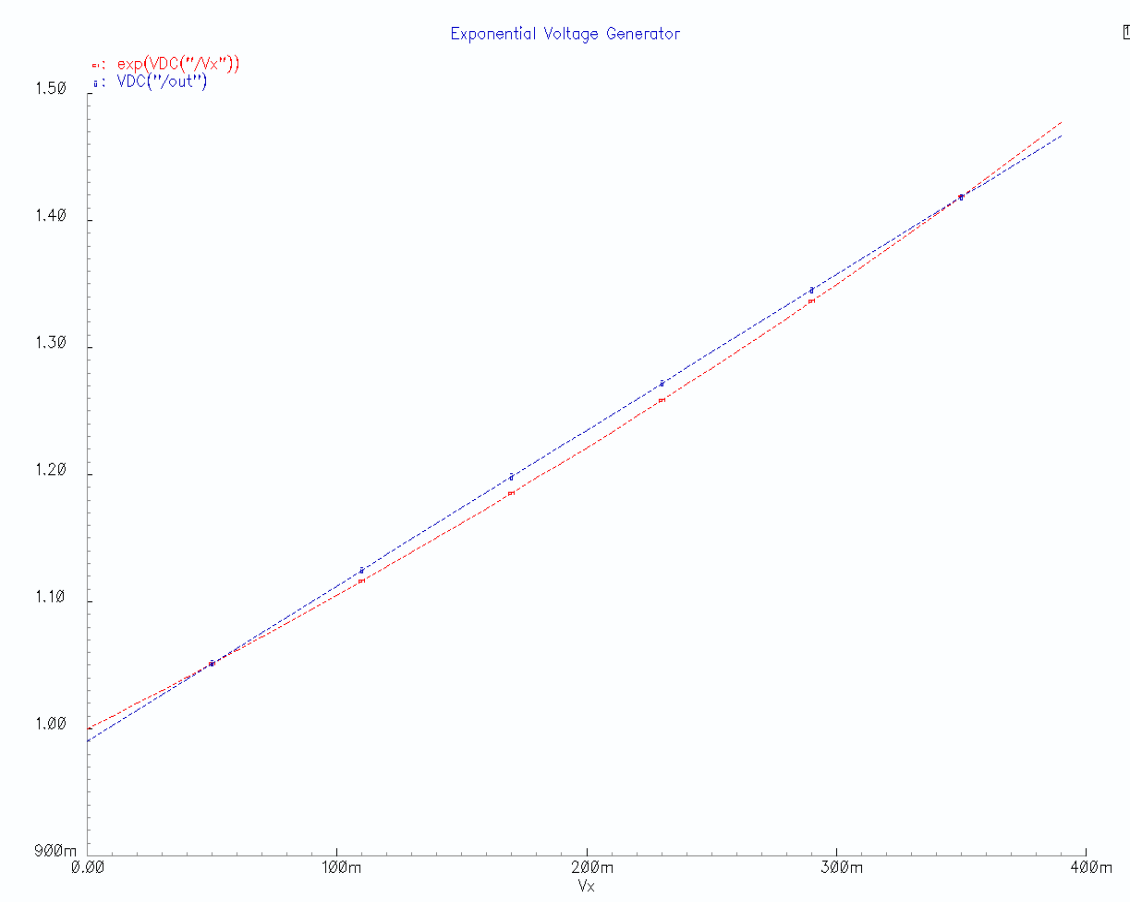

Fig. 14. Output of the exponential voltage generator vs the ideal curve

A problem with the circuit in Fig. 13 was that the transient response indicated slight oscillations in the range of 4-5 mV in the control voltage due to the action of two different branches controlling the voltage at node X. This problem was further accentuated by a kick back through the gate-to-source capacitance of the cascode transistor in the VGA's first and second stages. The control voltage is tied to the gate of these transistors (for reasons described in the following section) and hence is directly affected due to capacitive coupling of the high frequency variations at the source of these transistors.

Another disadvantage of this circuit was that the voltage across resistance R1 changed considerably with process and temperature variations, making the control voltage generated very sensitive to these parameters. These problems were overcome by modifying the circuit as indicated in Fig. 15.

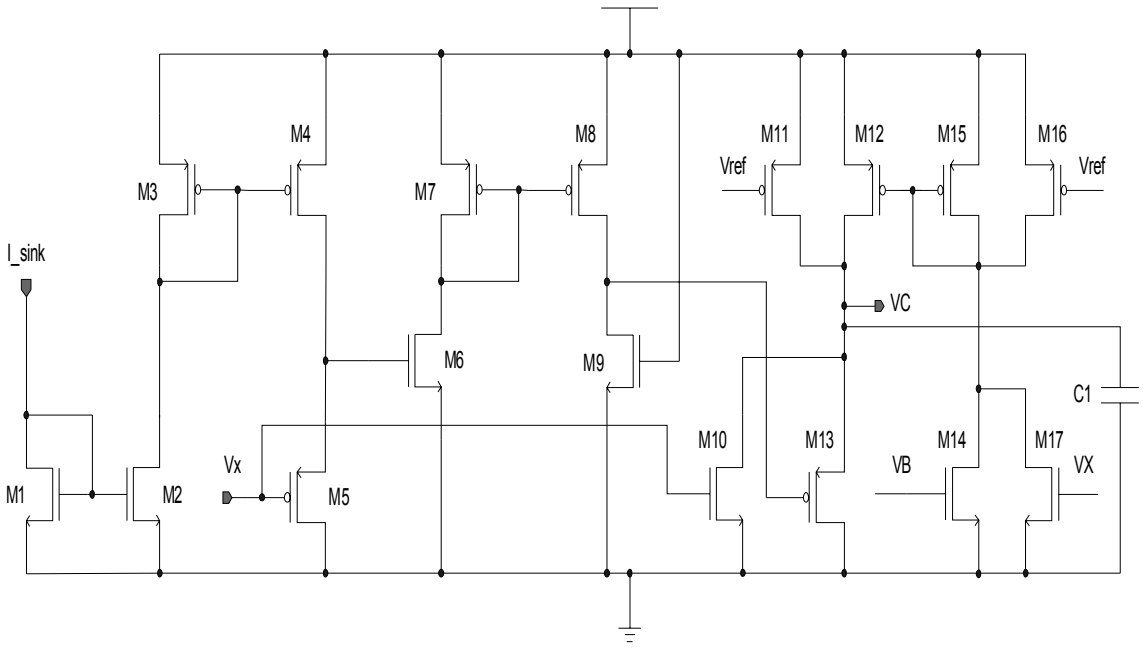

Fig. 15. Exponential voltage generator used in the VGA

In Fig. 15, transistors M10, M11, M16 and M17 are used to compensate for variations in the control voltage with temperature, supply and process. Transistors M10 and M17 are in the on-state only for higher values of Vx and higher supply voltage. Transistors M11 and M16 are in moderate inversion for a supply voltage of 1.8V and in strong inversion for a supply voltage of 2V. Capacitor C1 is used to suppress the high frequency spikes in the control voltage that occur due to the kick back through the gate-to-source capacitance of the cascode transistor in the VGA's first and second stages.

3. VGA core – stages 1 and 2

Based on the specifications provided, the architecture proposed in Ref.[16] has been selected as the basic block of the VGA. The same architecture has been used for both variable gain stages of the amplifier, with some minor differences. The schematic is given in Fig. 16. The main advantages of this topology are wide bandwidth due to the cascode structure and inductive peaking at high frequencies, large gain range and relatively constant bandwidth across the gain range due to the current sharing scheme used in the design. The problem of ensuring sufficient headroom for all the transistors in the cascode is ameliorated by using active load. Operation of the input transistors in the linear region for low gain settings not only increases the dynamic range but also prevents DC voltage stack. A common-mode feedback circuit is added to set the output DC voltage to a desired value and to improve the CMRR of the VGA.

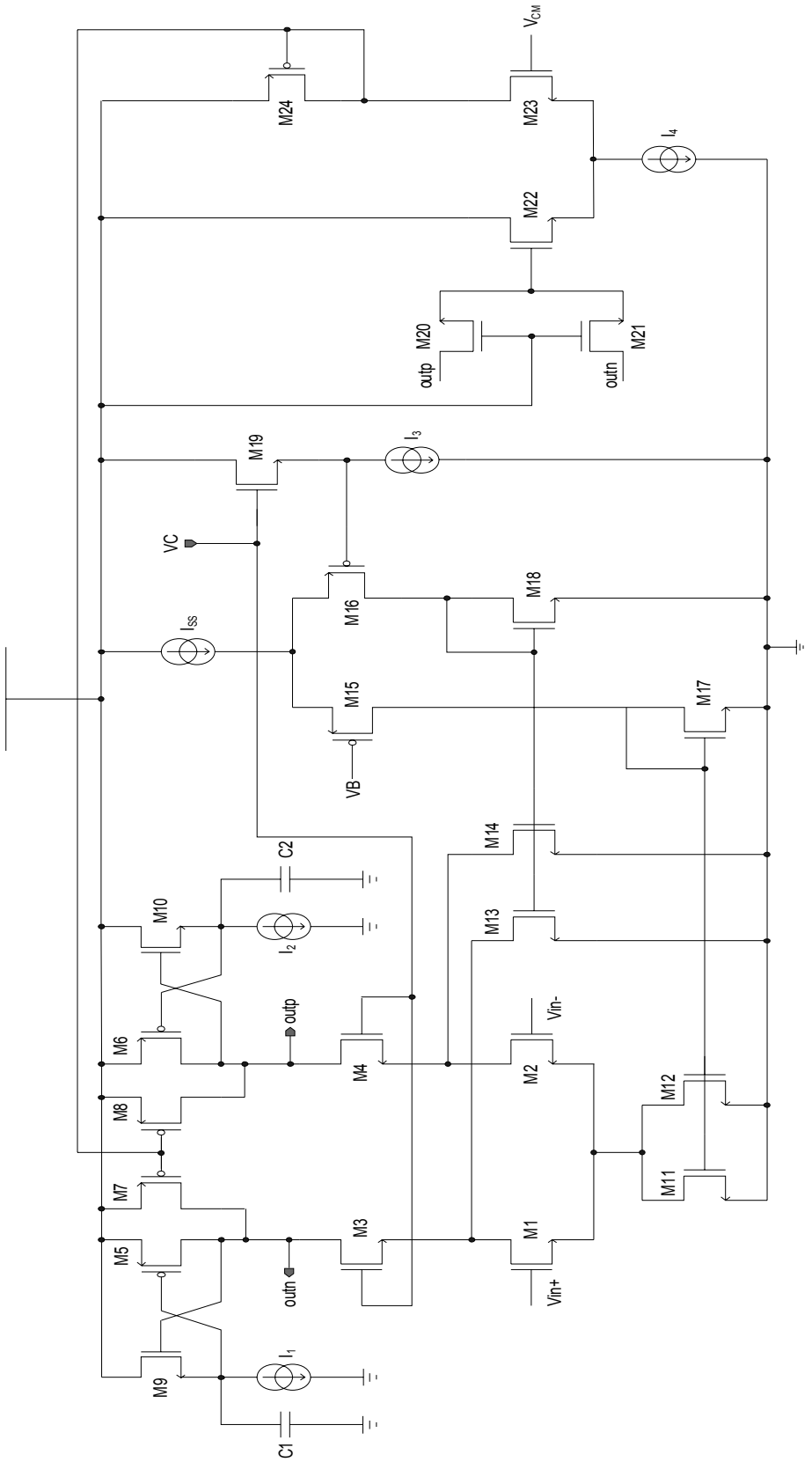

Fig. 16. Schematics of stages 1 and 2 of the VGA

a) Inductive Peaking

Active inductive peaking is one of the methods employed to increase the bandwidth of circuits used in wideband applications. The structure used is shown in Fig. 17, and comprises of a PMOS transistor (which acts as the load for the main amplifier), an NMOS transistor with its gate and source connected to the drain and gate respectively of the load as shown, a capacitor and a current source.

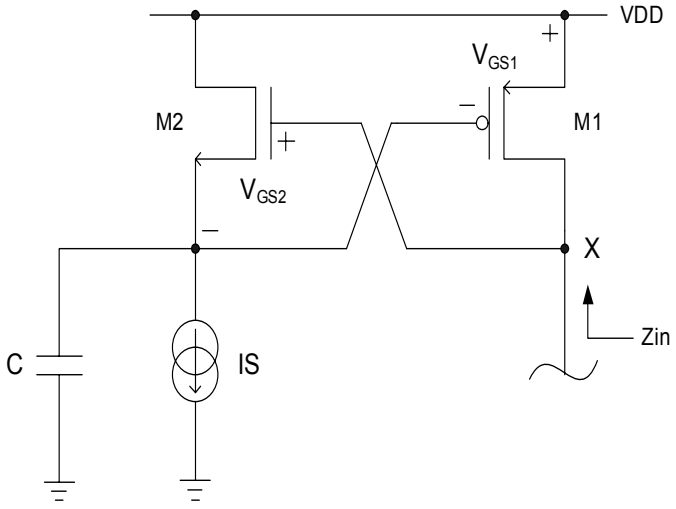

Fig. 17. Active inductive peaking

The small signal model for calculating the impedance of this structure looking into the drain of the PMOS transistor is given in Fig. 18.

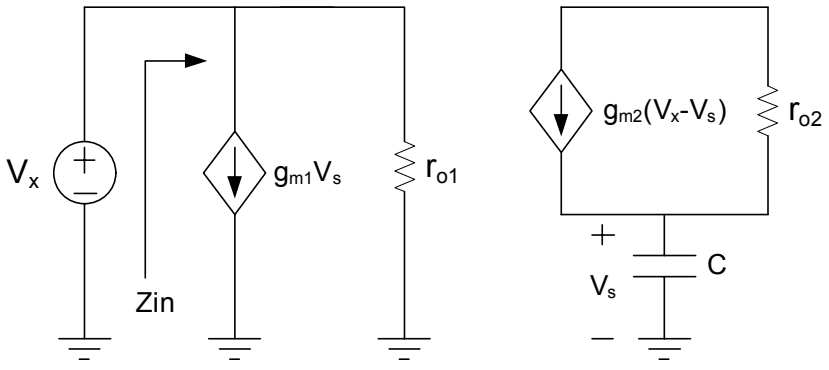

Fig. 18. Small signal model to calculate the input impedance of the active load

From Fig. 18, neglecting channel length modulation,

$$g_{m2}(V_x - V_s) = sCV_s \tag{62}$$

$$g_{m2}V_x = (sC + g_{m2})V_s \tag{63}$$

$$\Rightarrow V_s = \left(\frac{g_{m2}}{g_{m2} + sC}\right)V_x \tag{64}$$

$$i_x = g_{m1}V_s \tag{65}$$

From (64),

$$i_x = g_{m1}\left(\frac{g_{m2}}{g_{m2} + sC}\right)V_x \tag{66}$$

$$\frac{V_x}{i_x} = \frac{g_{m2} + sC}{g_{m1}g_{m2}} \quad \Rightarrow \; Zin = \frac{C}{g_{m1}g_{m2}}\left(s + \frac{g_{m2}}{C}\right) \tag{67}$$

The expression for *Zin* indicates that the low frequency input impedance of the structure is approximately $1/g_{m1}$ but a zero is introduced at a frequency g_{m2}/C, giving rise to high frequency peaking in the gain of the VGA in which this structure is used as an active load. At high frequencies, the inductance forms a parallel resonant circuit with the parasitic capacitances associated with the drain of the PMOS transistor. The -3dB bandwidth of the VGA can be extended by properly adjusting the value of the capacitance *C* and the transconductance of transistor M1. However, the peaking should be limited to a maximum of 1.5 to 2dB in order to ensure stability of the amplifier and to maintain reasonable settling time. Fig. 19 gives the input impedance of the active load used in the first stage of the VGA, and illustrates the inductive peaking at high frequencies.

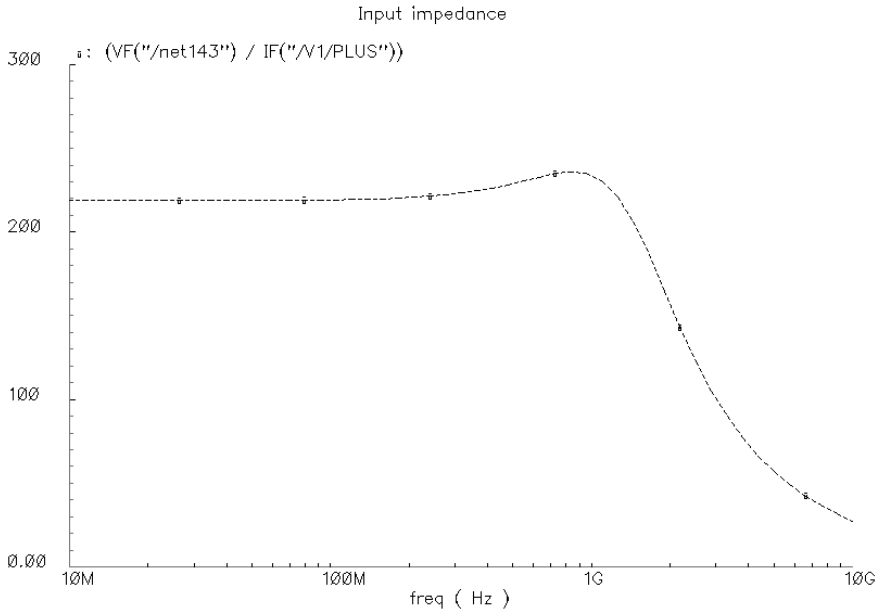

Fig. 19. Input impedance of the structure in Fig. 17

The voltage at node X in Fig. 17 is given by:

$$V_x = V_{DD} - V_{GS2} + V_{GS1} \tag{68}$$

Hence, when this structure is used as the load of the VGA, the DC output voltage is ideally well defined, obviating the need of a CMFB circuit. However, in this thesis, a CMFB circuit has still been used to fix the output common mode to a particular value and to stabilize the output voltage against variations in temperature, process and supply, throughout the gain range of 0-52 dB. The overdrive voltage of the PMOS transistor is kept low by minimizing the gate-to-source voltage ($V_{GS1} \sim V_{TN}$) of the NMOS transistor. This is achieved by using a medium V_T NMOS transistor for M1 and normal V_T PMOS transistor for M2.

b) Current Sharing

The -3dB bandwidth of the VGA is given by

$$\omega_{-3dB} = \frac{g_{mLoad}}{C} \tag{69}$$

In order to maintain a constant bandwidth throughout the gain range of 0-53 dB, the transconductance of the load transistor should be maintained constant for a given load capacitance. To achieve this, a method of current sharing is used as shown in Fig. 20. When $V_1 = V_2$, current I_1 flows through transistor M3, and I_2 flows through transistor M4. The aspect ratios of transistors M5 (M6) and M7 (M8) are K times that of transistors M3 and M4 respectively. Hence, the current through M5 (M6) is KI_2 and the current through M7 (M8) is KI_1. For any variation of the voltage V_1 with respect to V_2, assuming ideal mirroring action between transistors M3 and M5 (M6) and between transistors M4 and M7 (M8), the same amount of current, KI_{SS}, flows through transistors M13 and M14, maintaining their transconductance the same for all values of gain.

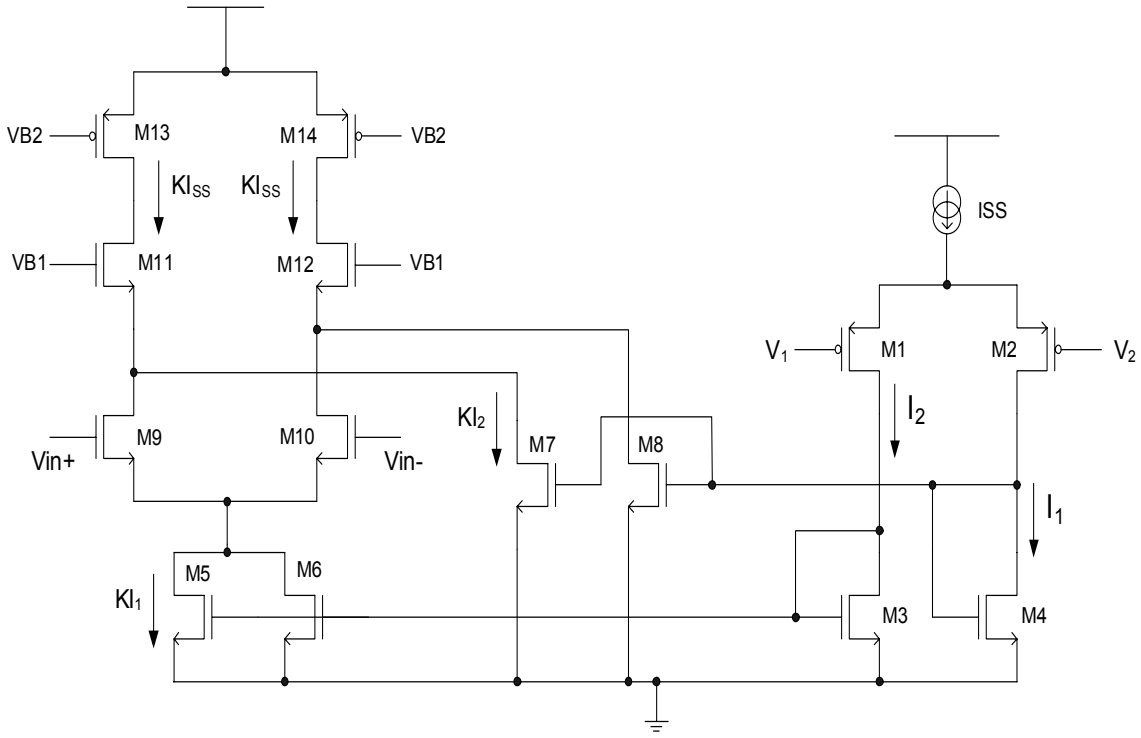

Fig. 20. Current sharing technique

c) Addition of PMOS Current Sources to the Load

This method has been used in all three stages of the VGA to increase its gain. The output common mode voltages of the first two stages could also be increased and set to a value of 1.2 V by adjusting the currents carried by the current sources. These PMOS transistors are included in the common mode feedback circuit of the first two stages, and the output common mode voltage is fixed and stabilized at the desired value by controlling their gate voltages. Fig. 21 and Fig. 22 illustrate the difference in the gain of the first stage of the VGA without and with the PMOS current sources respectively.

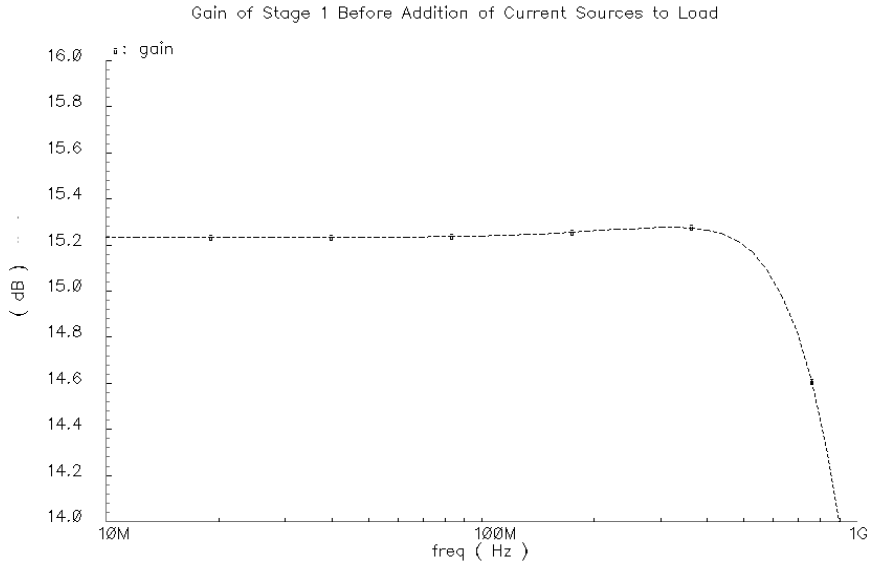

Fig. 21. Gain of stage 1 without the PMOS current sources

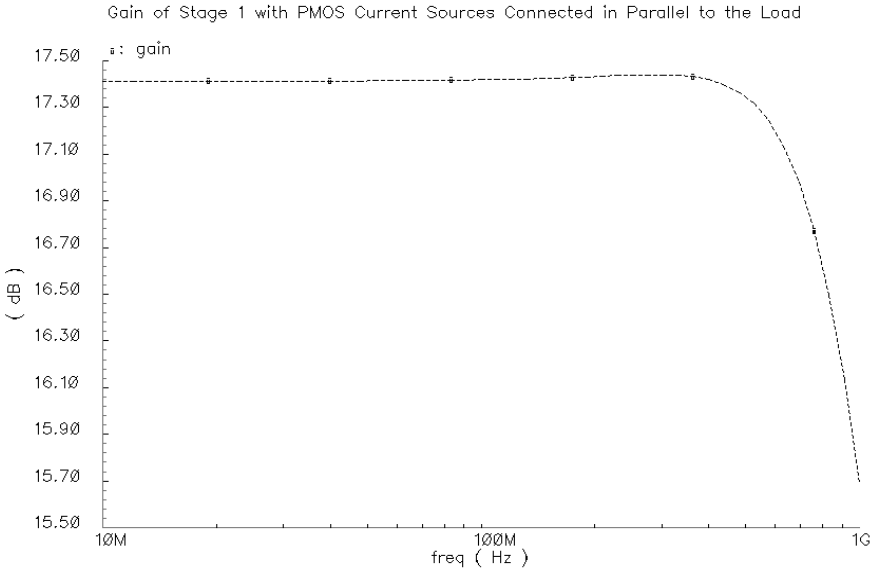

Fig. 22. Gain of stage 1 with the PMOS current sources

d) Simulation Results for Stages 1 and 2

AC response of stage 1 in the low and high gain settings is illustrated in Fig. 23 and Fig. 24.

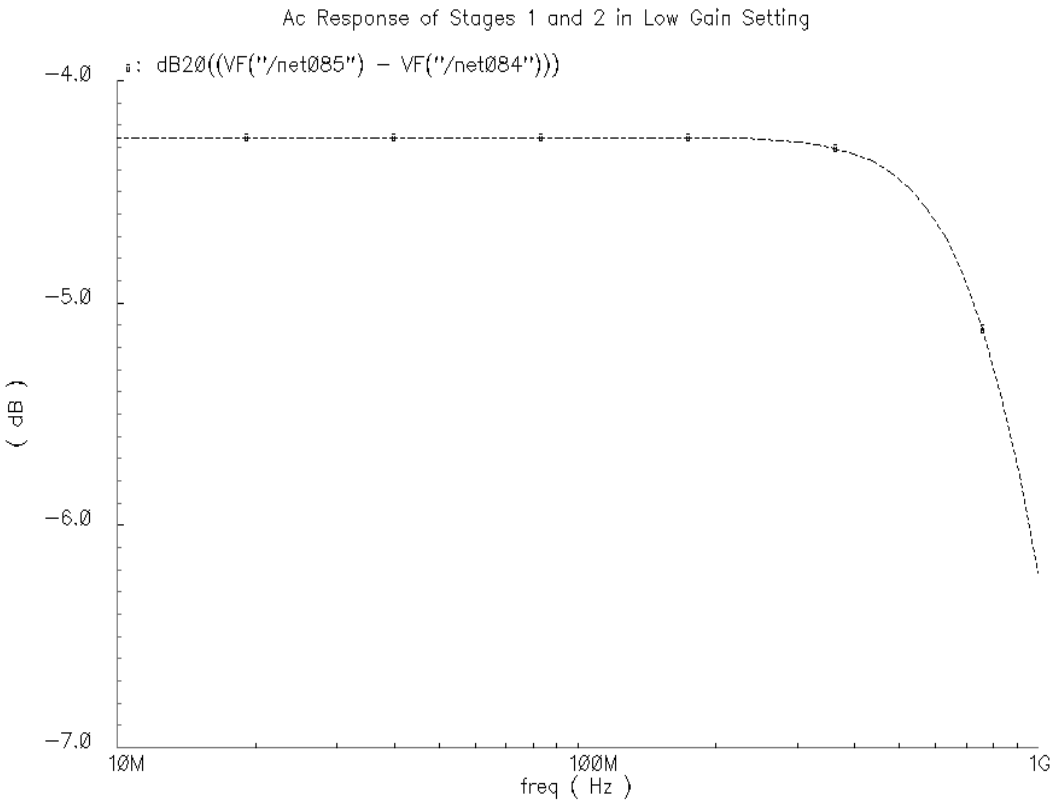

Fig. 23. AC response of stage 1 (and stage 2) in the low gain setting

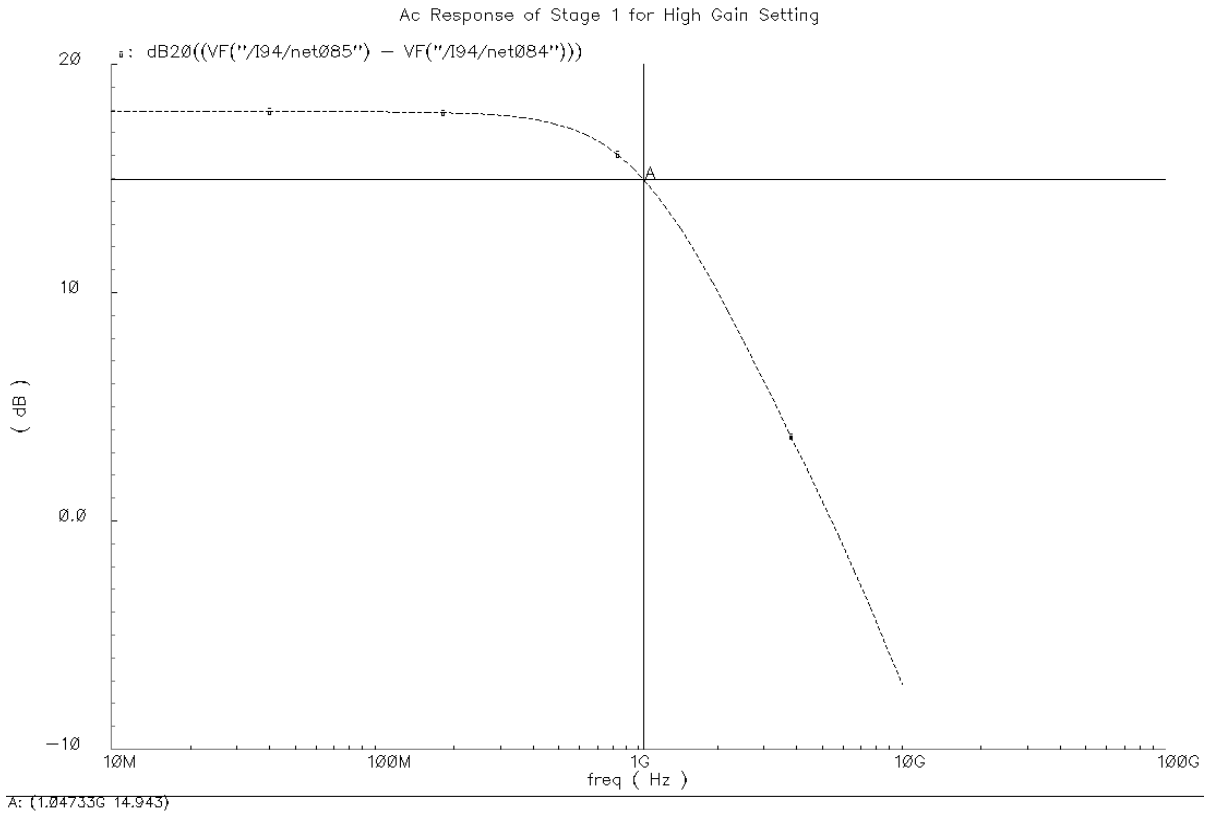

Fig. 24. AC response of stage1 (and stage 2) in the high gain setting

Transient response of the two stages to an input signal of frequency 150MHz and amplitude 500mV peak to peak is given in Fig. 25.

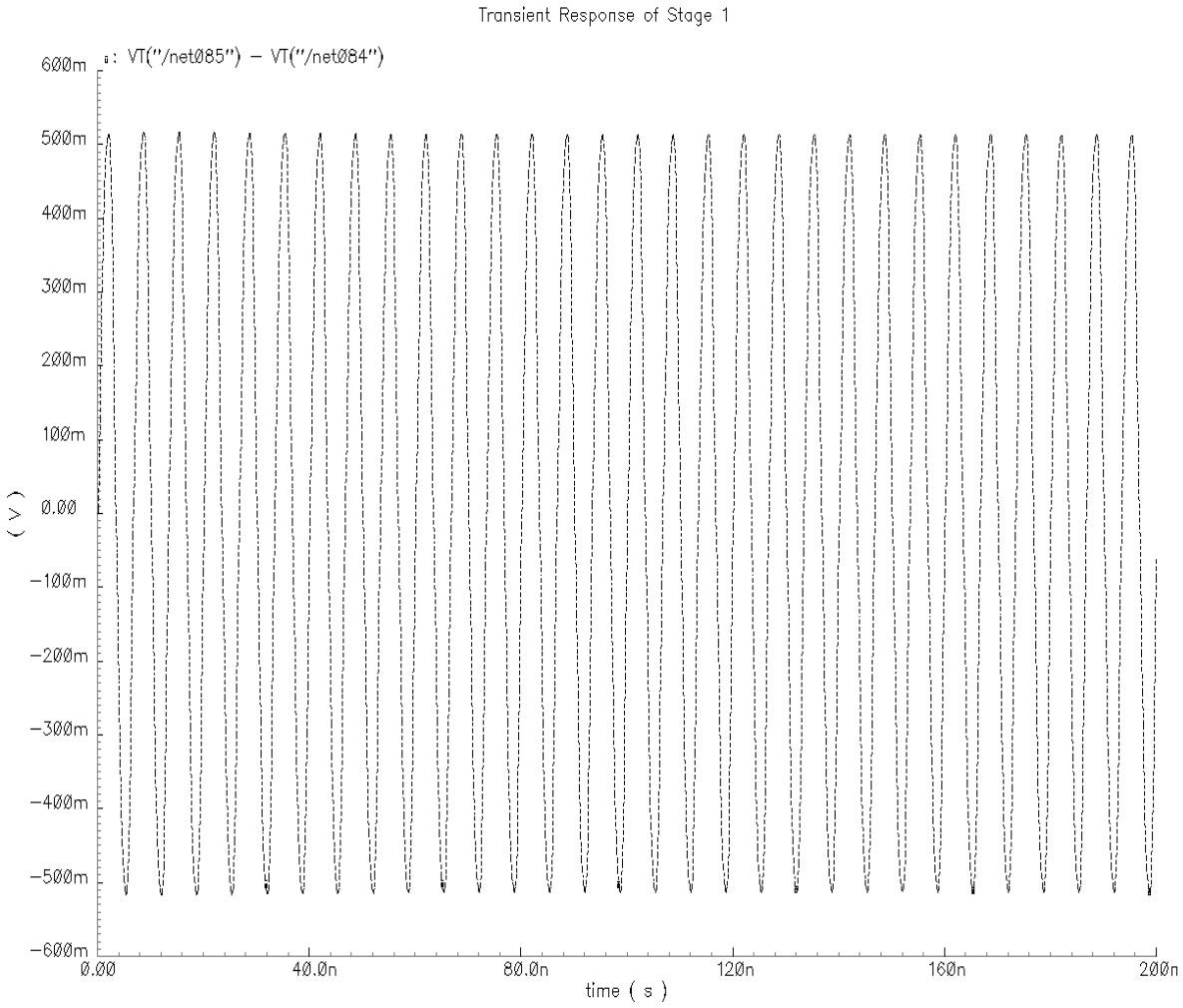

Fig. 25. Transient response of stage 1 (and stage 2) in the low gain setting

Graphs of the equivalent input referred noise of stage 1 are given in Fig. 26 and Fig. 27.

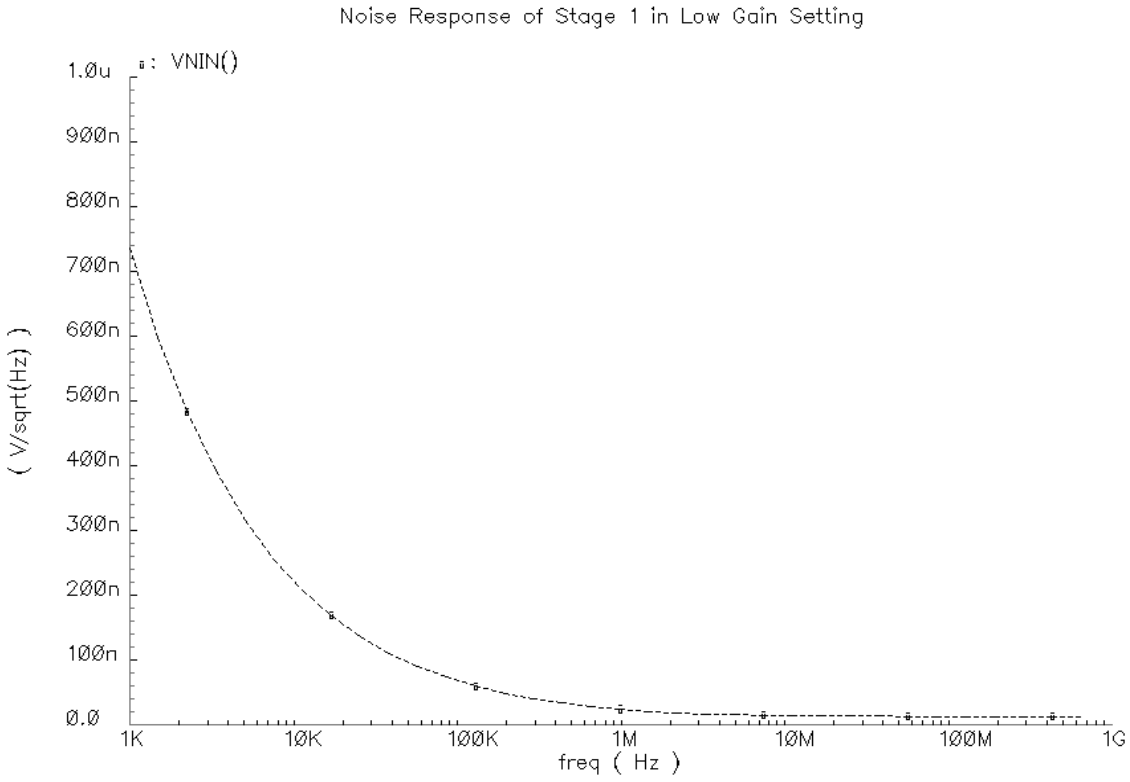

Fig. 26. Input referred noise response of stage 1 in the low gain setting

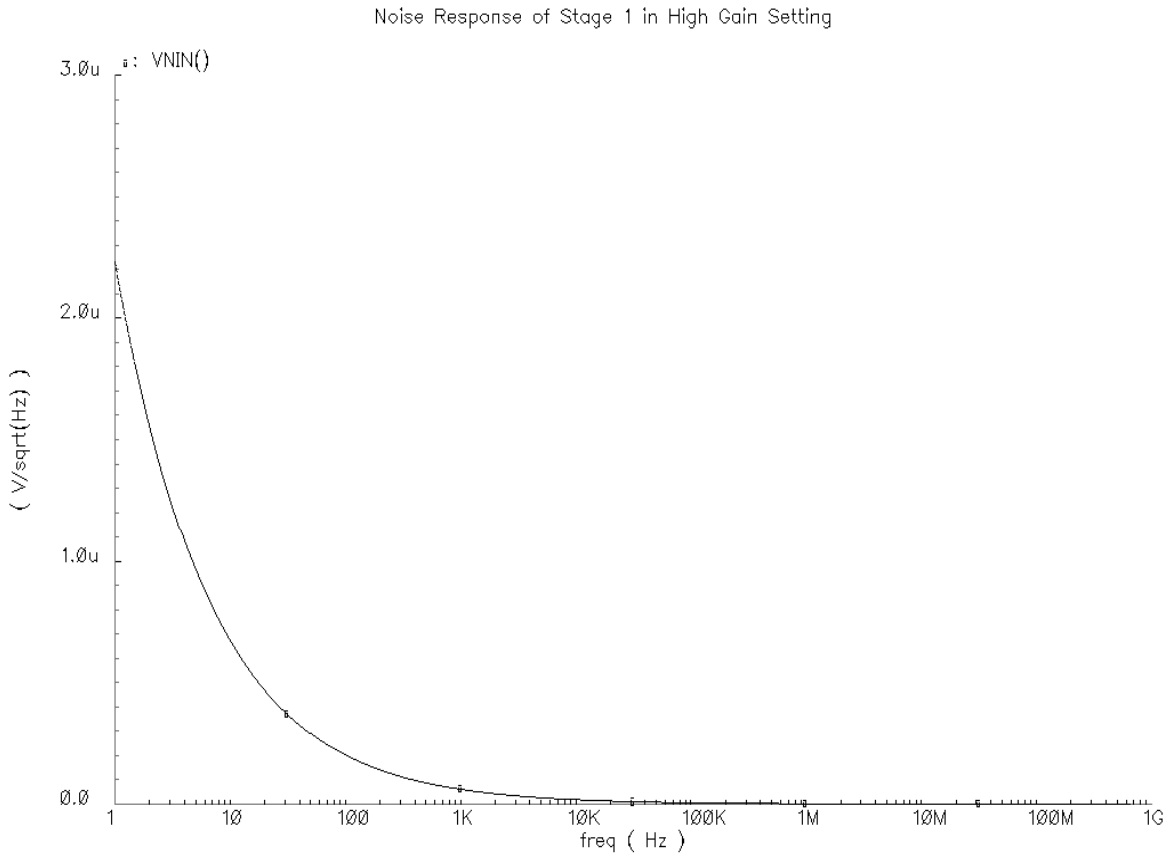

Fig. 27. Input referred noise response of stage 1 in the high gain setting

4. VGA core – stage 3

A fixed gain amplifier is used for stage 3. This stage is optimized to provide lower gain compared to the maximum gain of the other two stages but a much wider output swing. Active inductive load is also used in this stage to increase the bandwidth. An addition to this circuit is the cross-coupled NMOS transistor used for capacitive neutralization, as shown in the circuit in Fig. 28.

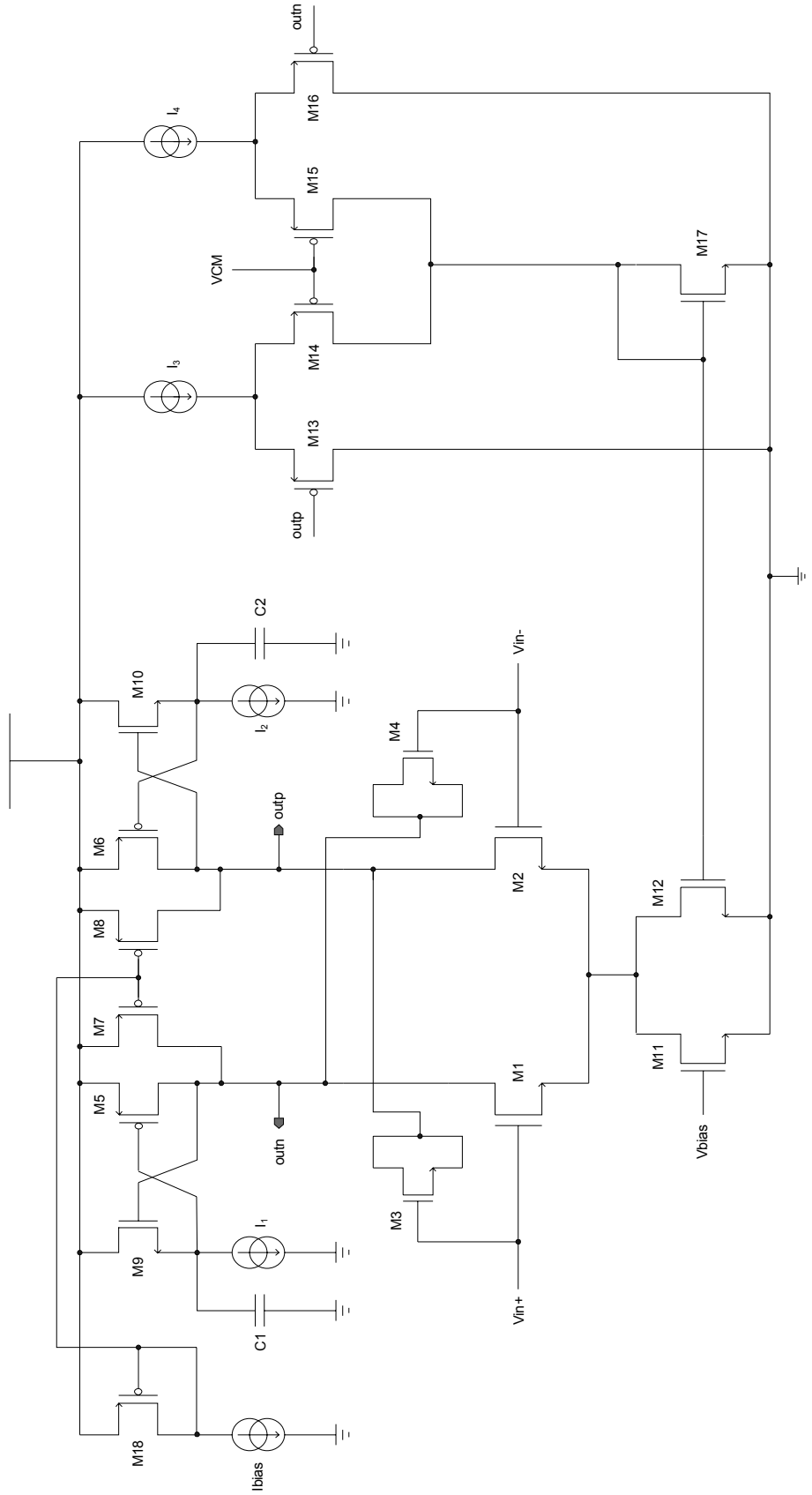

Fig. 28. Schematic of stage 3 of the VGA

The AC response of stage 3 is illustrated in Fig. 29.

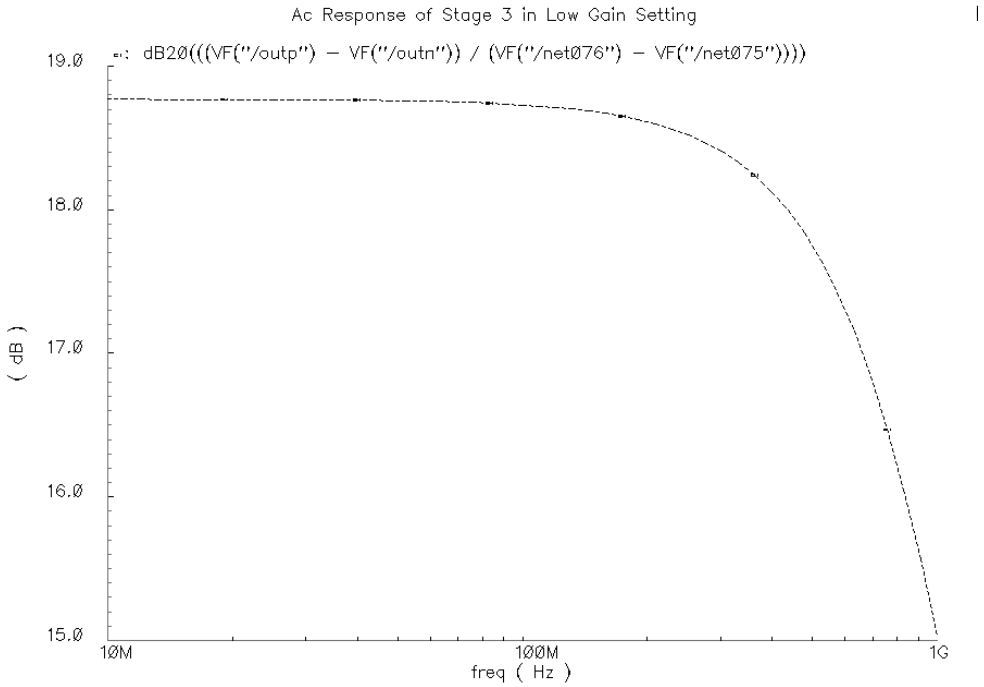

Fig. 29. AC response of stage 3

5. DC offset cancellation circuit

A systematic offset of around 10mV was observed in the output DC levels of the VGA designed, necessitating the addition of a DC offset cancellation circuit. The first stage alone contributed approximately 8mV out of the total 10mV offset. To overcome this problem, two types of DC offset cancellation circuits were designed and analyzed. The first method uses a negative feedback loop to correct the offset while the second circuit is based on digital offset correction. A brief description of both circuits follows.

a) Negative Feedback

The block diagram of the amplifier with the feedback loop is given in Fig. 30. A low pass filter with a transfer function $H(s)=\frac{G_m}{1+sCR}$ is used in the feedback loop. Its input comes from the output of the VGA while its output is subtracted from the input of the VGA.

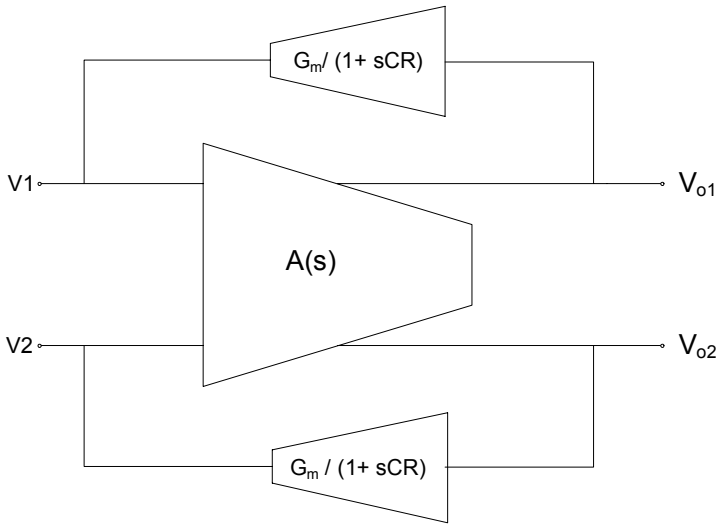

Fig. 30. Block diagram of the DC offset cancellation circuit

The transfer function of the loop can be derived as follows:

$$T(s)=\frac{A(s)}{1+A(s)H(s)} \tag{70}$$

$$T(s)=\frac{A(s)}{1+A(s)\left(\frac{G_m}{1+sCR}\right)}=\frac{A(s)}{1+A(s)\frac{1}{CR}\left(\frac{G_m}{s+1/CR}\right)} \tag{71}$$

$$T(s) = \frac{A(s)(s + 1/CR)}{s + 1/CR + G_m A(s)/CR} \tag{72}$$

At DC,
$$\left|T\right| = \frac{A(0)}{1 + G_m A(0)} \tag{73}$$

At higher frequencies,

$$T(s) \approx A(s) \tag{74}$$

The DC offset cancellation circuit is shown in Fig. 31.

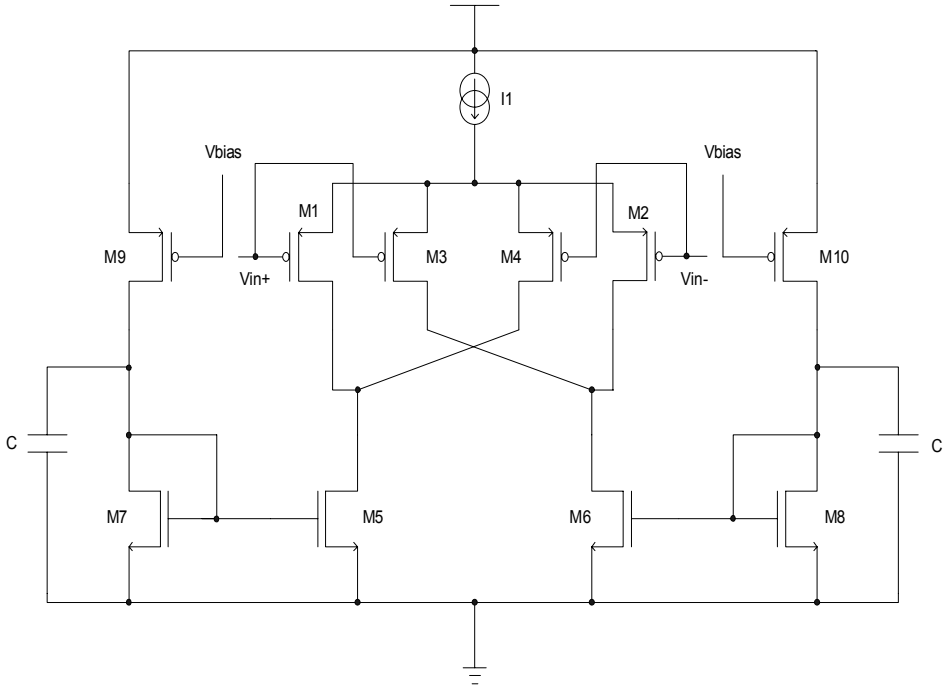

Fig. 31. DC offset cancellation circuit with negative feedback

A current cancellation scheme is used in the circuit in order to achieve a low transconductance. The small signal model of the half-circuit for calculating the effective transconductance of the error amplifier is given in Fig. 32.

The effective transconductance is given by:

$$G_m = g_{m1} - g_{m4} \tag{75}$$

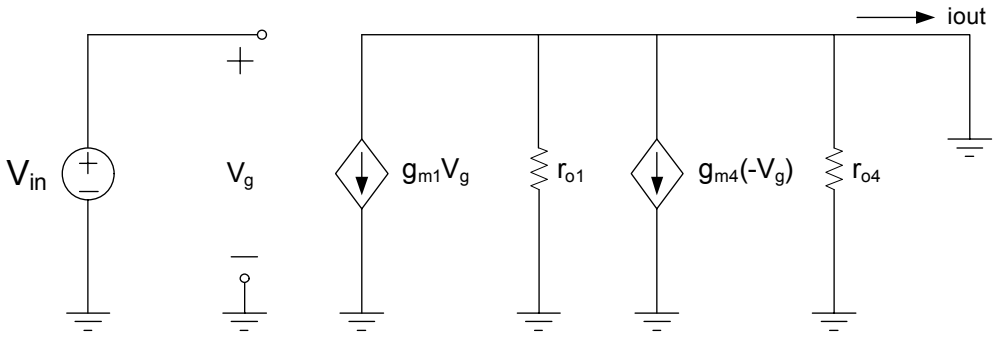

Fig. 32. Small signal analysis to calculate the effective transconductance

If transistors M1 and M4 in Fig. 31 have the same drain currents and are sized such that the aspect ratio of M4 is only slightly smaller than that of M1, the effective transconductance can be minimized to the desired value. The cut-off frequency can be further minimized by using a large load capacitance C.

The unity gain frequency of the circuit is given by:

$$\omega_u = \frac{G_m}{C} \tag{76}$$

The effective transconductance G_m of the circuit should be minimized due to the following reasons:

1. A large transconductance value results in a higher unity gain frequency (and a higher 3dB bandwidth) for the DC offset cancellation circuit as per equation (76), which in turn affects the AC response of the VGA.

2. From equation (72), a zero is introduced in the transfer function at a frequency of $1/CR$. The DC gain of the VGA decreases by a factor of $1+ G_mA(0)$ after inclusion of the offset cancellation circuit. Hence, the loop gain, given by $G_mA(0)$, cannot be made very high since this causes the gain at frequencies close to the first tone in the UWB system to drop below the specified value. Fig. 33 illustrates these trade-offs in the AC response of the VGA after inclusion of the offset cancellation circuit.

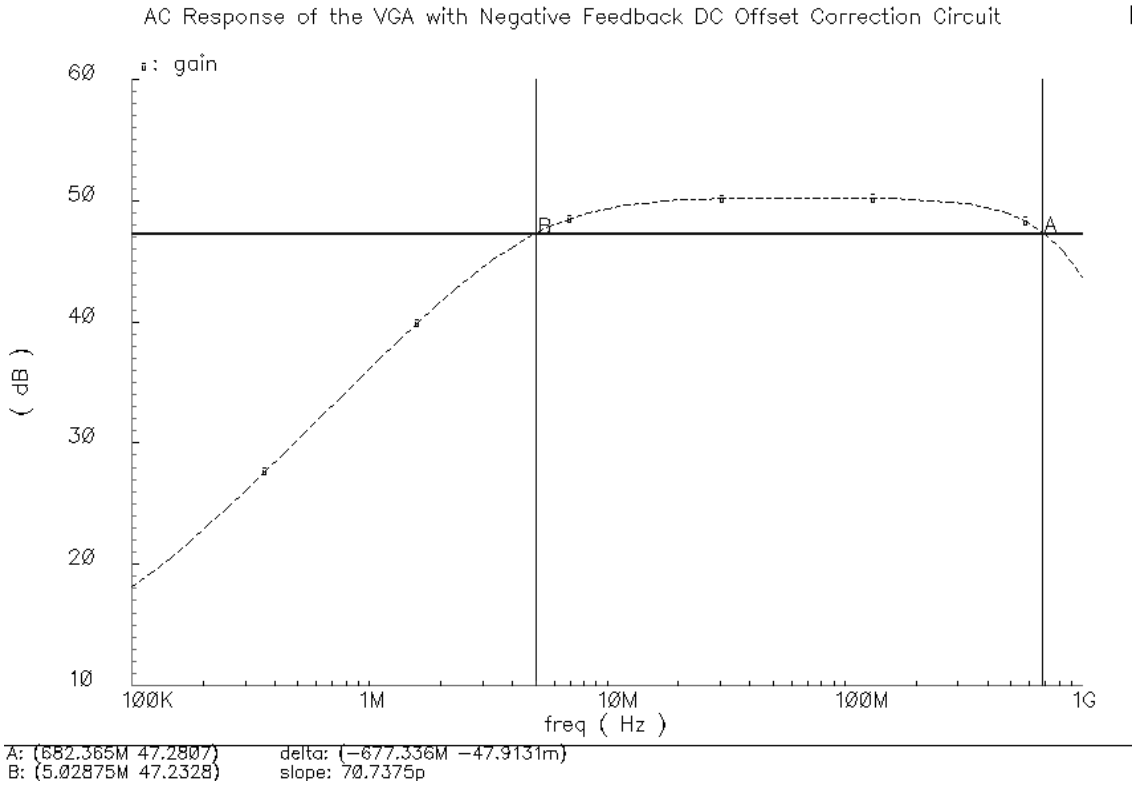

Fig. 33. AC response of the VGA after including the offset cancellation circuit

For a mismatch of 5% between the input differential pair transistors of the VGA, this method of DC offset cancellation results in an offset of less than 15 mV between the output voltages. Fig. 34 and Fig. 35 illustrate the difference in the output DC voltages without mismatch and with 5% mismatch respectively.

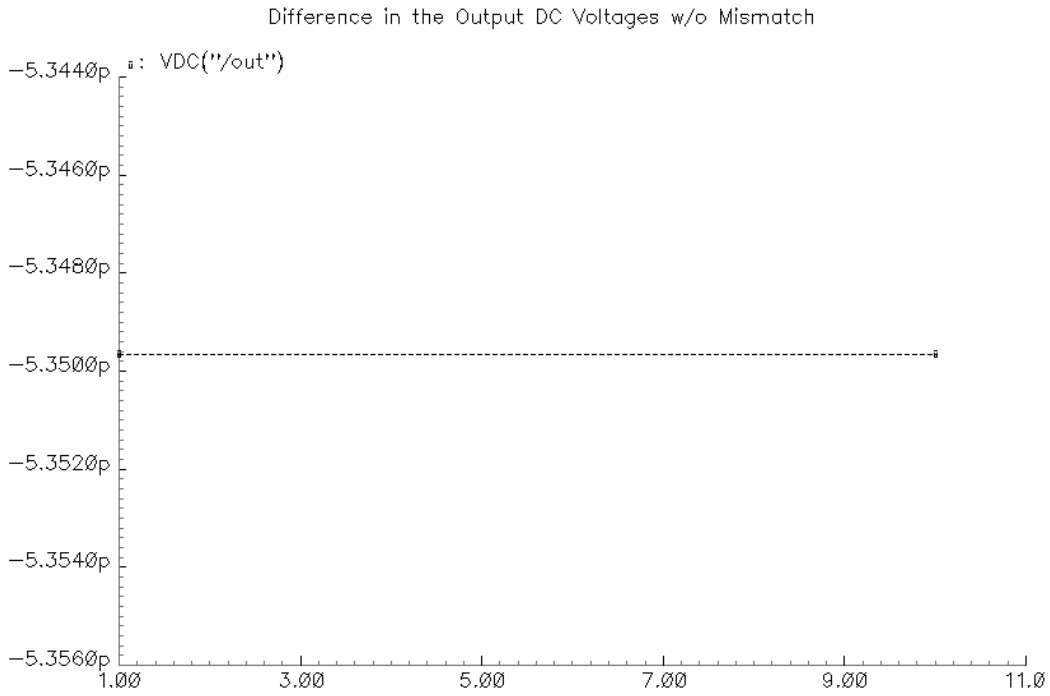

Fig. 34. Difference in the output DC voltages of the VGA without mismatch

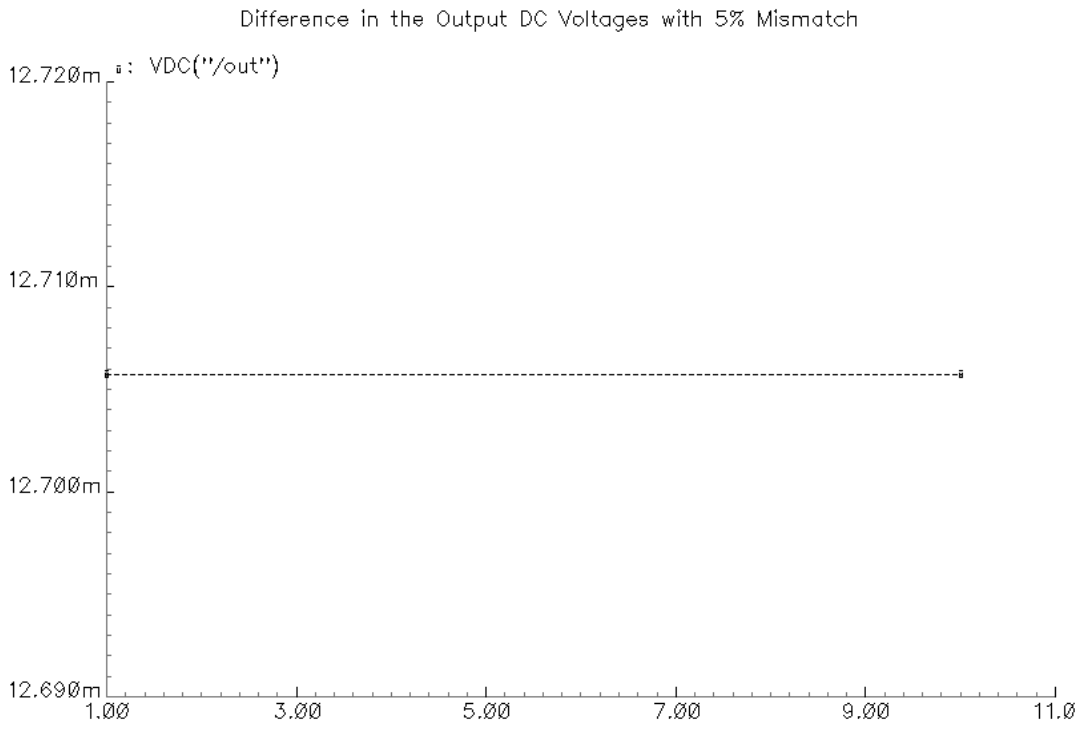

Fig. 35. Difference in the output DC voltages of the VGA with 5% mismatch

The disadvantage of this circuit is that unlike digital offset correction, it does not offer programmability and also causes lowering of the VGA gain at certain frequencies of interest. Further, the input transistors of the feedback circuit capacitively load the output of the VGA, requiring an increase in the current of the third stage in order to maintain the specified bandwidth. Addition of this circuit improves the NPR of the VGA while degrading its noise performance. Stability of the circuit is of concern due to the partial positive feedback in the current cancellation scheme. Also, a zero that is dependent on the output resistance of the circuit tends to vary a lot with process and temperature.

b) Digital DC Offset Correction

An efficient and easily programmable method of minimizing the input referred DC offset of the VGA is through digital offset correction. Offset correction circuitry as shown in Fig. 36 is included in all three stages of the VGA. In this method, the offset voltage is sensed at the output of the ADC and a corresponding sequence of control bits is generated by the digital control block. This sequence causes injection of different amounts of current in each of the branches of the three amplifiers used in the VGA core, depending on the value of the offset between the output voltages. Different amounts of current are sunk in each stage depending on the contribution of the stage to the offset voltage. For example, higher current is injected in the first stage for a particular offset voltage compared to the other two stages due to its more significant role in creating an input referred offset voltage. Offset due to mismatch in the ADC is also corrected by this circuit.

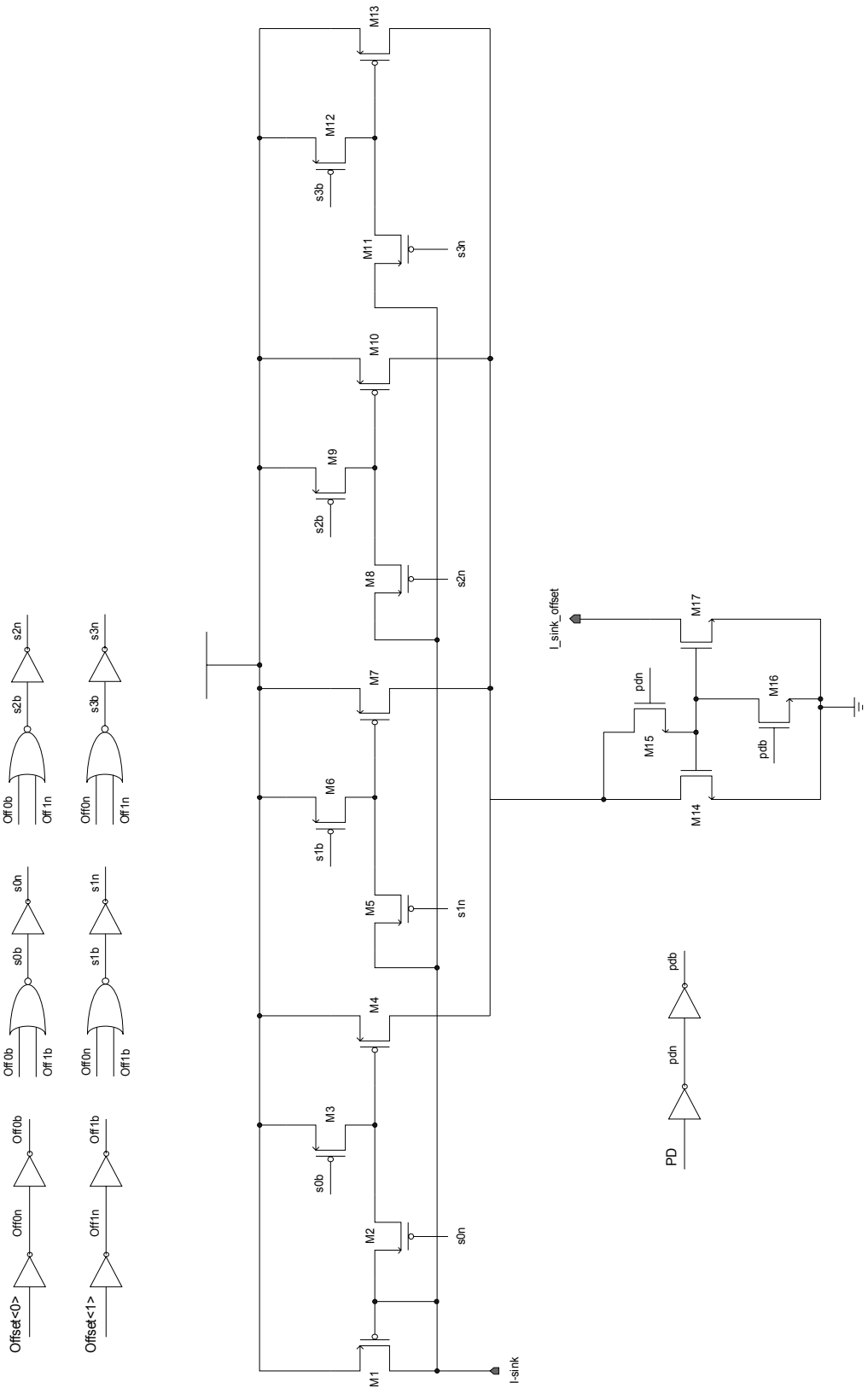

Fig. 36. Digital DC offset correction circuit

A power-down (PD) mode is incorporated in each offset correction block with the PD bit set to 1 when there is no offset between the output voltages of the ADC. This ensures that in the absence of offset, the same amount of current flows in both branches of each stage of the VGA. Figures 37 and 38 illustrate the difference in the output DC voltages without mismatch and with 5% mismatch respectively.

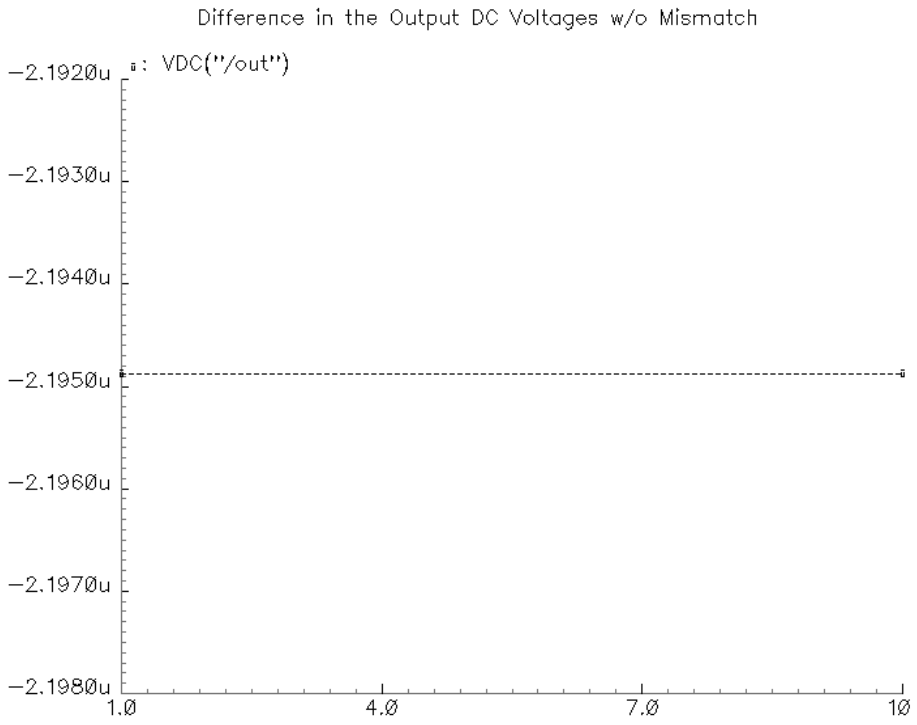

Fig. 37. Digital offset correction - Difference in the output DC voltages of the VGA without mismatch

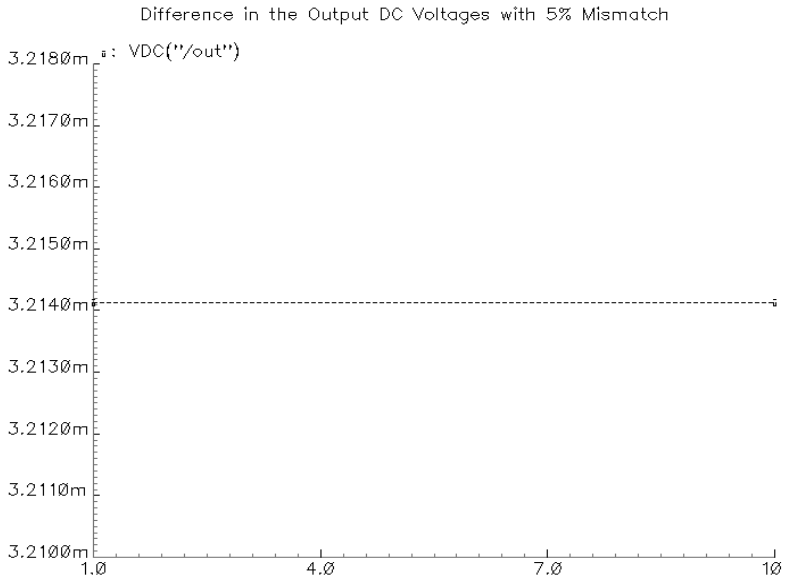

Fig. 38. Digital offset correction - Difference in the output DC voltages of the VGA with 5% mismatch

As can be observed from figures 35 and 38, the digital offset correction circuit performs offset correction better than the circuit using negative feedback and can handle larger mismatches. Other than programmability, an additional advantage of this technique is that it does not load the VGA much and hence does not affect its AC response. It can accurately correct offset for over 10% mismatch in the input transistors. A disadvantage is that it requires a slightly complex offset sensing circuit and control bit generating algorithm, both of which have currently not been developed for this thesis. Control bits will be manually generated and applied depending on the offset observed at the outputs of the VGA during testing.

6. Common mode feedback circuit

In the first two stages of the VGA, the CM sense block consists of a resistor divider which generates a voltage that is the average of the DC levels of the two outputs

V_{o1} and V_{o2} as shown in Fig. 39. Care is taken to make sure that the resistors do not load the outputs too much to cause degradation in the performance of the VGA. This is done by using MOS transistors that operate in the triode region. The resistance of these transistors is given by:

$$R_{on} = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_{Tn})} \tag{77}$$

Hence, by using a large channel length L and a small width W, the resistance of the NMOS transistors can be increased to a value that minimizes loading of the output of each stage. Following on these lines, the value of R_{on} was set to approximately 4kΩ. This is much greater than the load of the main amplifier (~ 350Ω), and hence does not degrade the gain of the amplifier. A differential pair with diode connected loads as shown in Fig. 39 acts as the error amplifier. The drain of M3 is connected to the gate of the PMOS current sources discussed in section A.3.c.

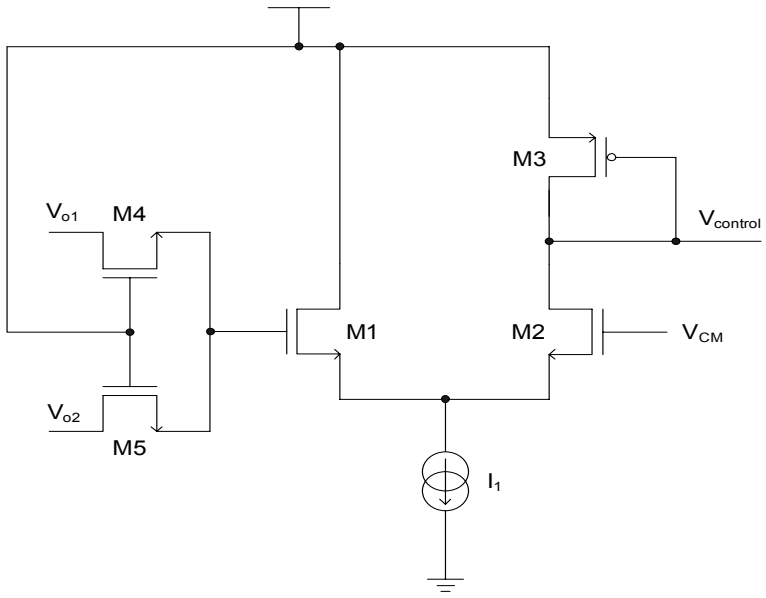

Fig. 39. CMFB circuit of stages 1 and 2 of the VGA

When the output common mode voltage increases more than V_{CM}, the voltage at the drain of M3 increases, thereby reducing the gate-to-source voltage and hence the current of the PMOS transistor M5. According to the description in section A.2 of Chapter II, more current flows through the load transistor of the main amplifier, lowering its drain voltage (which is also the output common mode voltage). Fig. 40 shows the transient response of the first two stages of the VGA when the CMFB loop is perturbed by a current source of 100 μA connected to the drain of transistor M3 as indicated. This is one of the methods for testing the stability of the CMFB loop. The node which sees the perturbation settles to its final value in approximately 6ns and does not oscillate. A very slight ringing is observed.

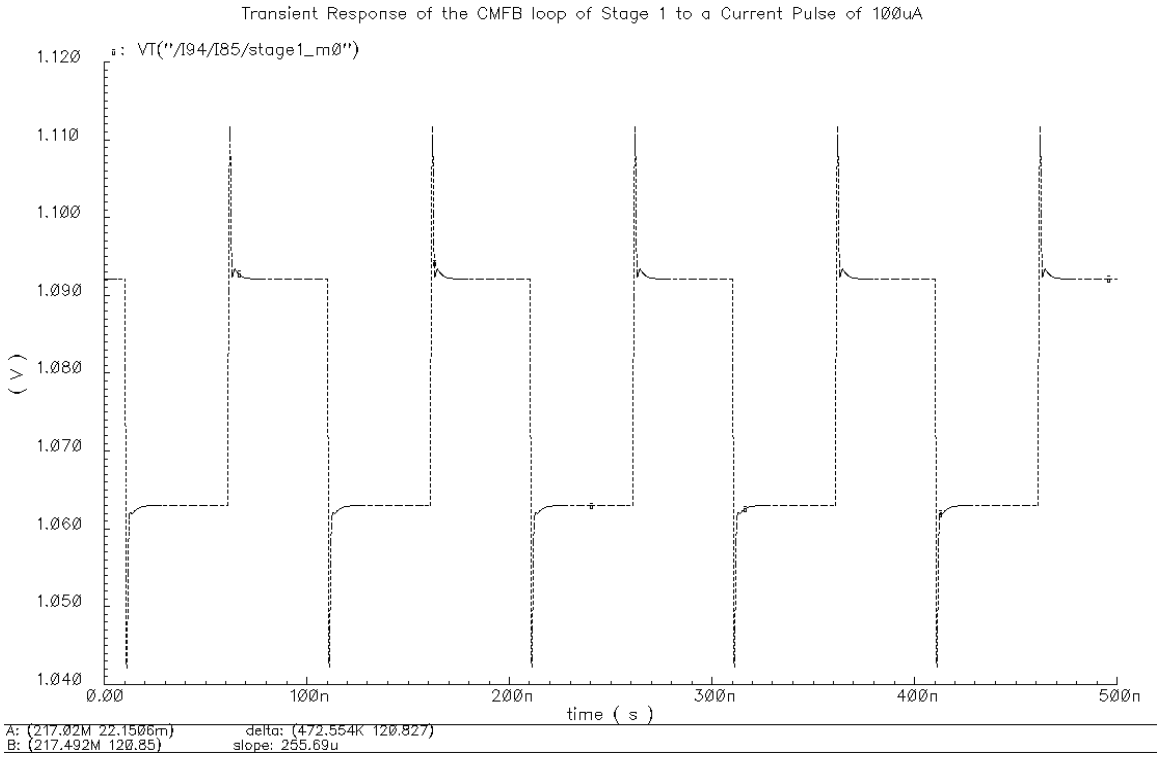

Fig. 40. Transient response of the CMFB loop of stage 1 to a current pulse of 100uA

A disadvantage of the CMFB circuit in Fig. 39 is that the resistors connected to the output nodes, along with the input capacitance of the error amplifier introduce a pole in the transfer function of the CMFB loop, given by

$$\omega_P = \frac{1}{RC_{in}} \tag{78}$$

$R = 4k\Omega$ and $C_{in} \sim 200fF$. Hence $\omega_P \approx 2GHz$. This degrades the phase margin of the loop and might lead to potential instability. One way of reducing the effect of the pole at high frequencies is to connect a capacitor in parallel to each of the resistors. This introduces a left half plane zero in the transfer function of the loop, partially compensating for the pole. However, these capacitances decrease the bandwidth of the DM amplifier since they add to the capacitance at the output nodes.

Fig. 41 shows the settling behavior of the output nodes of stage 1 when both outputs are disturbed by current pulses of 100uA. The output DC level settles to the common mode reference value of ~1.2 in less than 7s and indicates good stability without much ringing. This shows that the CMFB circuit is stable with sufficient phase margin.

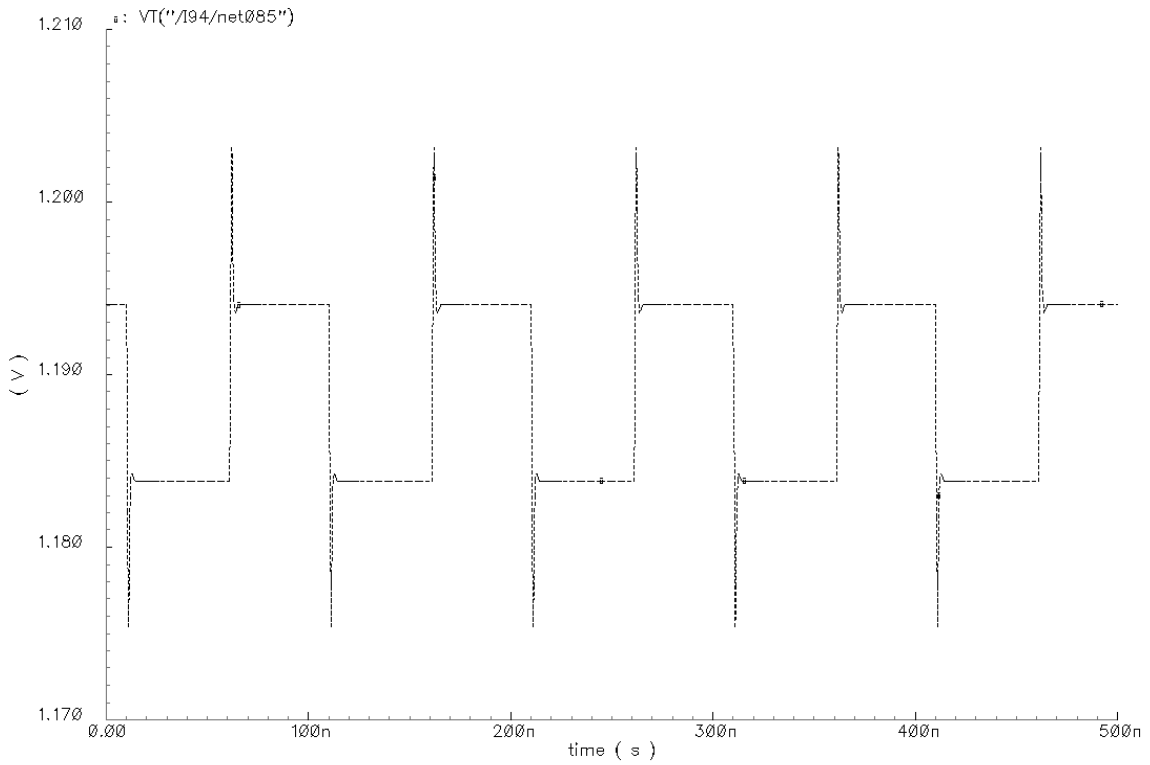

Fig. 41. Transient response of the outputs of stage 1 to a current pulse of 100uA

In the third stage, since the gain of the amplifier is fixed and the current sharing method is not used, the current source of the amplifier needs to be biased independently. Instead of using a CMFB circuit similar to the one in the first two stages, a circuit which adjusts the output common mode level by varying the current in the amplifier performs the function of a CMFB circuit as well as sets the bias voltage for the current source. The basic idea is shown in Fig. 42. By properly biasing the gate voltage of transistor M5, the common mode level is fixed at 900 mV, which is the input common mode required for the ADC circuit that follows the VGA.

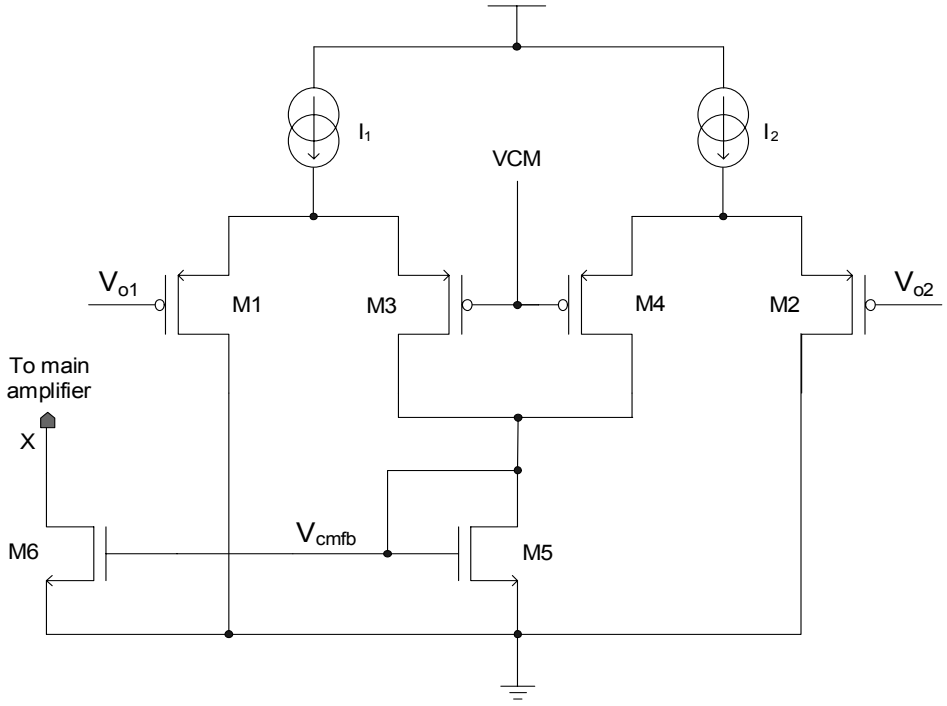

Fig. 42. CMFB circuit stage 3 of the VGA

The CMFB circuit in Fig. 42 does not resistively load the DM amplifier and cause a drop in the DM gain, but capacitively loads it. Also, for the circuit to function properly, transistors M1 to M4 should always be in the saturation region. This imposes a constraint on the output voltage swing of the main amplifier since a large output voltage might push the transistors into the cut-off region. The overdrive voltages of these transistors have to be high in order to overcome this problem, trading off with the gain of the CMFB loop. The CMFB circuit used for the first two stages does not have this disadvantage since the input to the error amplifier consists of only the common mode component of the output voltages and not the differential component too.

A non-dominant pole is introduced in the CMFB loop due to the capacitance seen at node X in Fig. 42. In order to have a high loop gain and hence lower sensitivity to changes in the input common mode voltage, transistor M6 should have high transconductance, $g_{m,M6}$, since the loop gain is directly proportional to the

transconductance. $g_{m,M6}$ cannot be increased by increasing the current through M6 since it decreases the resistance of the current source, leading to reduction of the CMRR. The other way of increasing the transconductance of M6 is to increase the (W/L) ratio of the transistor. However, this trades-off with the phase margin (PM) of the CMFB loop's transfer function due to lowering of the value of the non-dominant pole. Phase margin of is defined as:

$$PM = 180^0 + phase(A_{loop}(j\omega_u)) \tag{79}$$

where ω_u is the unity gain frequency, given by

$$\omega_u = \frac{g_{m,M6}}{C_L}, \tag{80}$$

where C_L is the load capacitance of the main amplifier and is also the load capacitance of the CMFB loop. The phase margin can be improved by decreasing the unity gain frequency of the CMFB loop, which is directly proportional to the transconductance of M6 as given by equation (80). ω_u can be decreased by splitting transistor M6 into two parallel transistors M11 and M12 as shown in Fig. 28. M11 is biased by a voltage source and carries a constant current. It does not appear in the CMFB loop except as a capacitive load at node X. M12 is part of the loop with its gate acting as the common mode control input. The currents through M11 and M12 sum up to the current initially flowing through the single transistor M6. The transconductance of each of the transistors is also approximately half that of M6.

$$g_{m,M12} = \frac{g_{m,M6}}{2} \tag{81}$$

The unity gain frequency of the loop after M6 is split into two transistors is given by

$$\omega_u = \frac{g_{m,M12}}{C_L} = \frac{g_{m,M6}}{2C_L} \tag{82}$$

Hence the unity gain frequency decreases to half its initial value, improving the phase margin. A disadvantage of this method is the reduction in loop gain since the loop gain is proportional to the transconductance of transistor M6.

Fig. 43 shows the settling behavior of the output nodes of stage 3 when both outputs are disturbed by current pulses of 100µA. The CMFB circuit is observed to be stable due to the absence of ringing and oscillations at the output. The output voltage settles to the expected common mode value in less than 6ns.

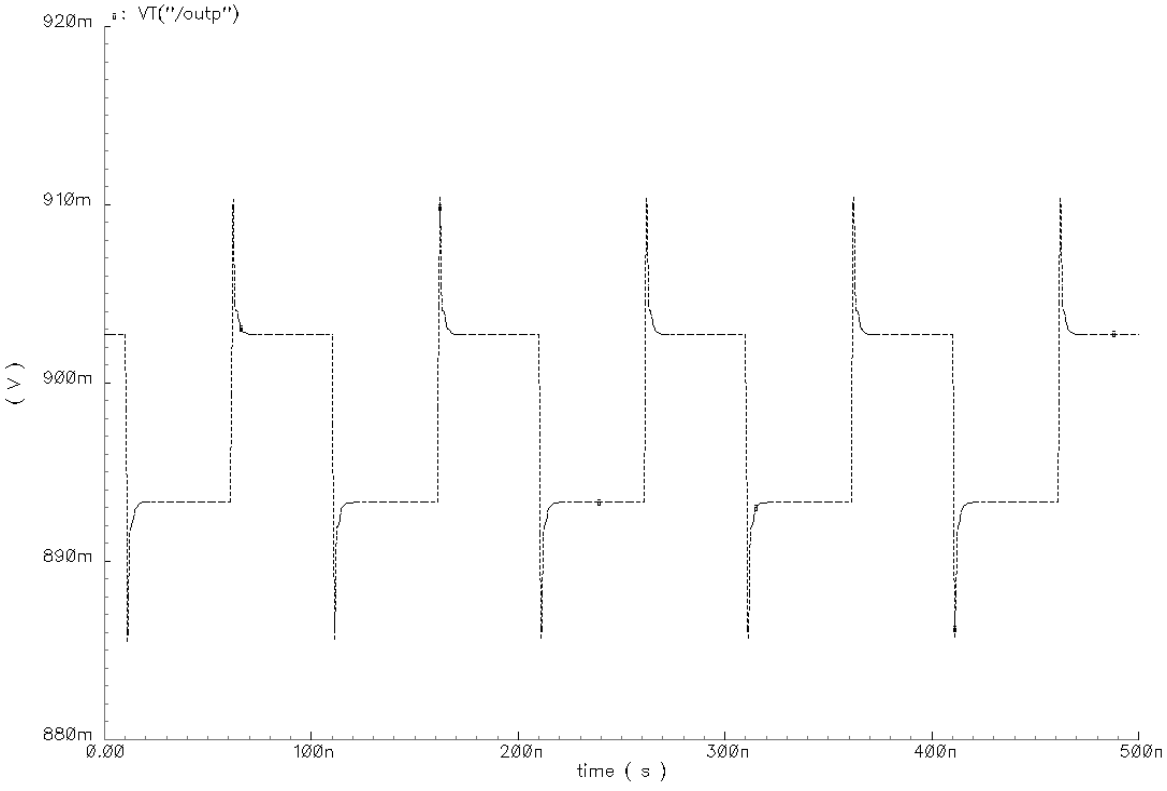

Fig. 43. Transient response of the output of stage 3 to a current pulse of 100uA

7. Bias generator

The circuit used for generating the bias currents for each of the blocks of the VGA is given in Fig. 44.

Transistors M1, M2, M4 and M6 are used to decrease the sensitivity of the circuit to process, temperature and supply voltage variations. M1, M2 and M4 are in the subthreshold region for supply voltages ranging from 1.6V to 1.8V and conduct negligible amount of current in the range of nano-Amperes. However, they operate in the strong inversion region for higher supply voltages. Resistor R1 and capacitor C1 form a low pass filter that eliminates high frequency variations in the signal from the gate of M9 to the gate of M10. Multiple branches like the one in Fig. 44 (comprising of transistors M8, M9 and M10, resistor R1 and capacitor C1) are used to generate the bias currents for each block of the VGA.

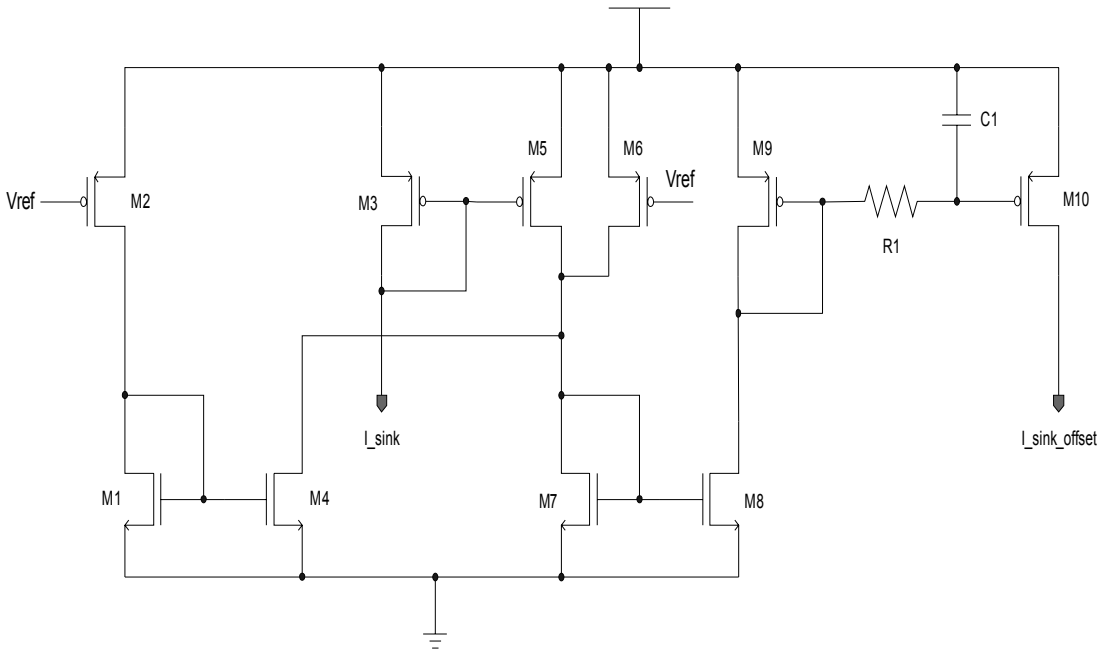

Fig. 44. Bias generator for the VGA

B. Layout

Layout in 0.18µm technology requires careful attention to the effects of parasitics that can heavily affect the performance of the circuits. Symmetry and minimization of area are other important layout considerations for any circuit. The layout of the VGA in this thesis has been developed to meet all these factors as closely as possible. Some of the techniques that have been employed for creating a good layout [10] are described below.

1. Multi-finger transistors

When very wide transistors need to be laid out, the use of multiple fingers is common practice. The number of fingers is decided based on the drain current of the transistor and the gate resistance of each finger. TSMC lists a certain maximum value of current density that can be tolerated per unit width of each of the six metal lines in 0.18µm technology, at $110^{\circ}C$. For example, the maximum current density in metal 1 at $110^{\circ}C$ is 1mA/µm. So, if the drain current of a transistor is 2mA at $110^{\circ}C$, and the width of the metal line carrying current to the drain of each of the fingers is 0.23µm (the default value in tsmc18rf), a minimum of 2/0.23 = 8.69 ~9 fingers are needed to ensure that the current densities are not exceeded in the metal lines at that temperature. If the drains are shared by two fingers, the number of fingers needed would approximately be double the calculated value. Fingers are normally used in even numbers. In low noise applications, the gate resistance of a finger should be around one-fifth to one-tenth of $1/g_m$. Hence the width of each finger is determined based on the requirement that the resistance of the finger be much lower than the inverse transconductance associated with the finger [10]. A trade-off involved in using a large number of fingers to minimize gate resistance is the increase in the capacitance associated with the perimeter of the source and drain areas.

2. Symmetry

It is essential to have a very symmetric layout in order to minimize mismatches and the resulting input referred offset voltage. Other advantages of symmetry are better common mode and power supply noise rejection and reduced even-harmonic distortion. The use of dummy transistors (or resistors and capacitors depending on the component under consideration) on either side of a matched pair of transistors helps prevent asymmetries by ensuring that both sides of the two transistors see approximately the same environment. To achieve very good matching between two components, it is very important that they be laid out in the same orientation. This is because certain steps in lithography and wafer processing behave differently along different axes, giving rise to mismatches if two components are not oriented along the same axis. Using very wide transistors also increases the probability of mismatch due to the gradients along a certain axis. To ameliorate this problem, common centroid configurations are used in cases requiring a high degree of matching. However, routing of interconnects becomes very tedious if the circuit is large, often giving rise to systematic mismatches.

3. Voltage and current routing

These are the two methods that are commonly used to distribute the bias currents and voltages. A stable reference independent of temperature and supply voltage variations is generated using a bandgap reference circuit and distributed to different parts of the circuit. In Fig. 45, voltage V_{ref} is generated using a diode-connected transistor M1 sinking a constant current I_{IN}. Transistors M2 and M3 sink currents I_2 and I_3 which are specific multiples of I_{IN}.

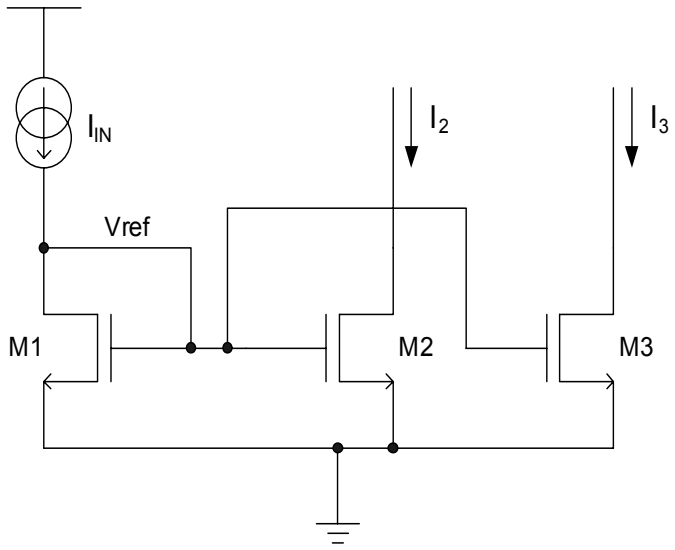

Fig. 45. Bias generation

One way of generating I_2 and I_3 is to place transistor M1 near the current source I_{IN}, while transistors M2 and M3 are placed close to the circuits they bias. Then, the gate and source of M1 are routed to the gate and source of M2 and M3 respectively, generating I_2 and I_3. The advantage of this method is that by routing just two voltages, any number of currents can be generated. A disadvantage of this method is the increase in the possibility of mismatch between M1 and the output transistors of the current mirror due to the large distances that might separate them in the chip. Also, as the voltage propagates through the long metal lines, it might suffer significant attenuation by the time it reaches transistors M2 and M3 due to the resistance in the metal lines. This causes the currents generated to be lower than the desired value, and they become more susceptible to variations in the supply resistances. Another technique of reference distribution which alleviates these problems is current routing. In this method, transistors M2 and M3 are placed close to M1, and currents I_2 and I_3 are carried to other parts of the circuit as required. The advantage of this is that better matching can be achieved between the input and output transistors of the current mirror by positioning them close to each other. Greater programmability can also be built in to control the current in each

branch individually (in voltage routing, if the reference voltage is varied, it affects the current in all the branches that use the voltage for current generation). Current routing however has its own disadvantages. One is that it requires one node to be routed for each bias signal, thereby resulting in a large number of interconnects to distribute the bias currents. Another disadvantage is that it increases the parasitic capacitances on the drains of M2 and M3, degrading the high frequency performance of the circuit to which these nodes are connected. In the layout of the VGA, both methods of routing have been used depending on the requirements.

4. Passive devices

Different types of resistors have different values of sheet resistance, temperature coefficients, variation of resistance with process and capacitance to substrate. The choice of the resistor depends on all these factors. Polysilicon resistors with a silicide block have high linearity (which also depends on their length), low capacitance to substrate and small mismatches compared to those without a silicide block. The sheet resistance of poly resistors is a function of temperature and process while their temperature coefficient is a function of the doping type and level. The sheet resistance of resistors without a silicide block exhibits a strong dependence on process. Such resistors can be made of n-well, source/drain p^+ or n^+ material or metal. These resistors suffer from non-linearity and a poor definition of the value of the resistors, as well as large mismatches. Large resistors are usually laid out in serpentine form or as parallel resistors connected in series. Inter-digitizing and common centroid techniques can be used for creating perfectly matched resistors.

The top level layout of the VGA is given in Fig. 46.

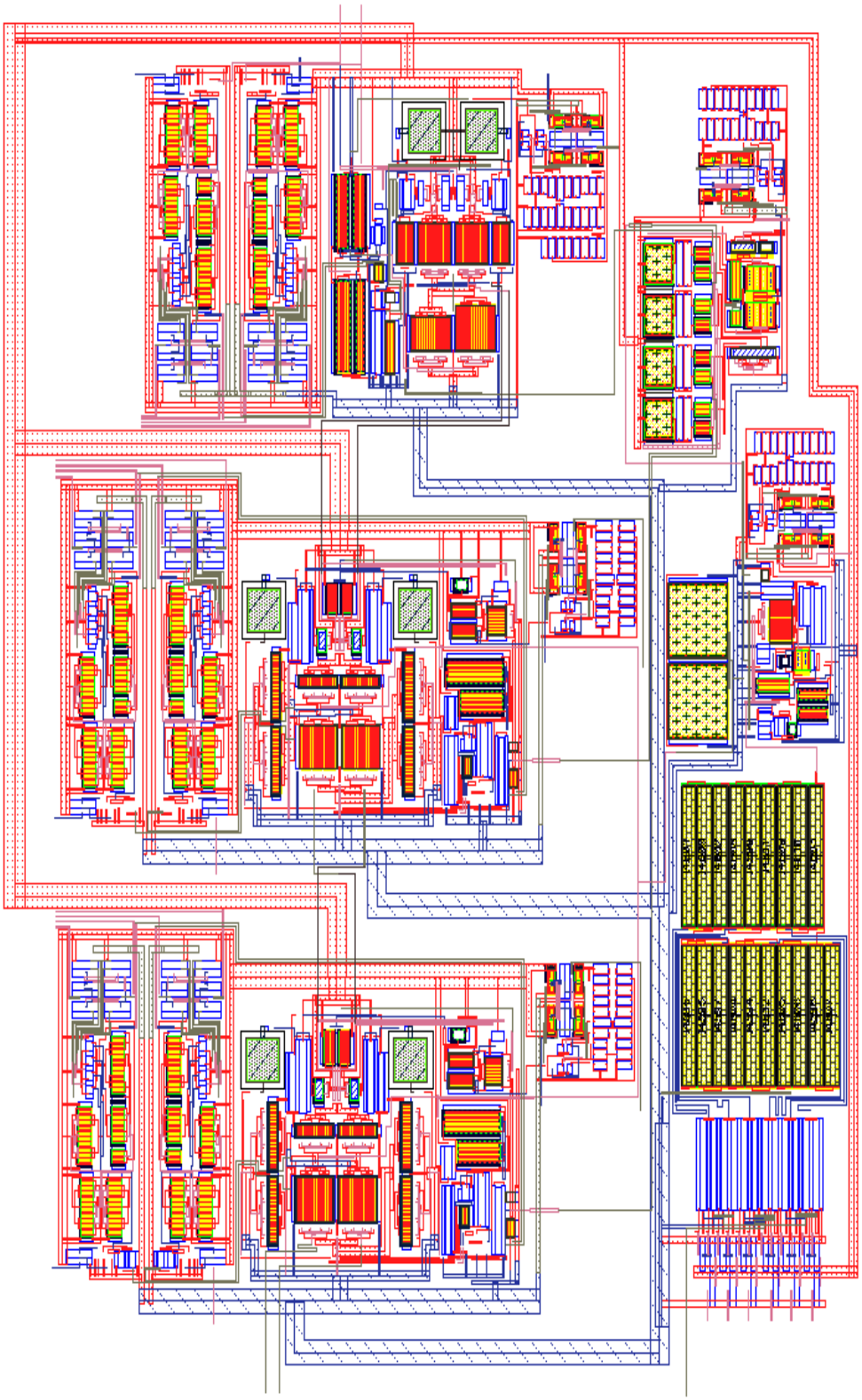

Fig. 46. Top level layout of the VGA

CHAPTER IV

SIMULATION RESULTS

A. Schematic Simulations

Simulation results are provided for the VGA designed in 0.18µm CMOS technology. The graphs provided are collected from the schematic simulations, and do not account for the parasitics of the interconnects between the circuit components.

The AC response of the VGA for the low and high gain settings are shown in Fig. 47 and Fig. 48, respectively.

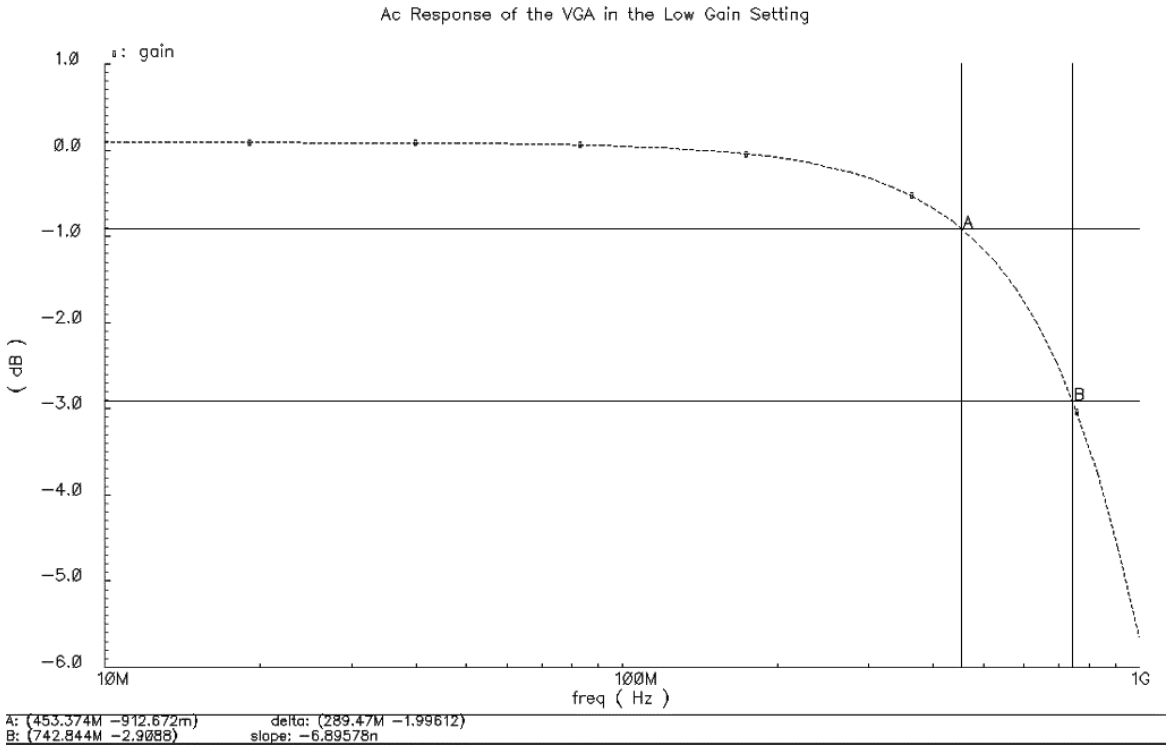

Fig. 47. AC response of the VGA in the low gain setting

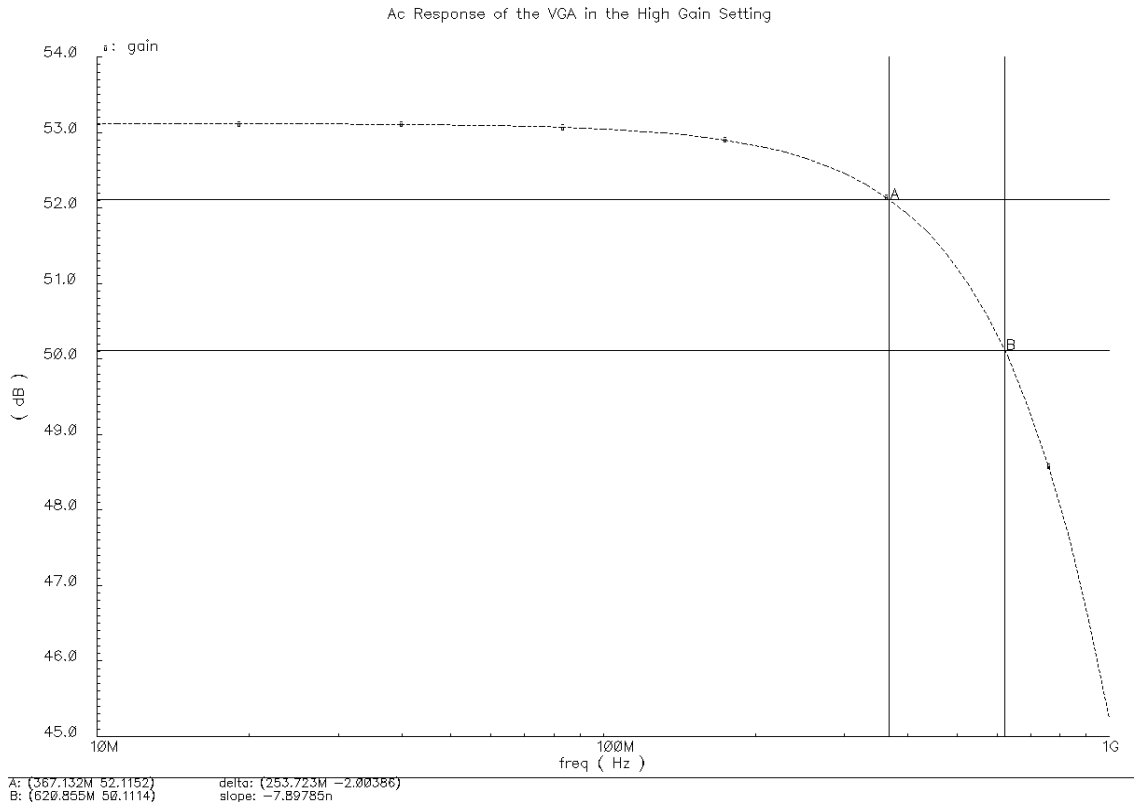

Fig. 48. AC response of the VGA in the high gain setting

Figures 47 and 48 indicate that a gain range of 0-53 dB has been achieved with a bandwidth greater than 600 MHz throughout the gain range. Figures 49 and 50 illustrate the variation of the DC gain with respect to the control voltage. It can be observed that the gain varies linearly in dB with respect to the control voltage till $V_{control} \sim 180mV$ and then increases slowly. It saturates for $V_{control}$ greater than 250 mV. This is because the cascode transistors in the first two stages of the VGA start nearing the triode region of operation for higher control voltages. As a result, increase in the transconductance of the input transistors of each variable gain stage is compensated by reduction in the transconductance of the cascode transistors, and the gain saturates. Since the automatic gain control loop adjusts the control voltage to the value that would give the desired gain and the corresponding output power level, it is not imperative to have a gain that varies

in certain specific steps with respect to the control voltage. In the VGA designed, due to exponential gain control, the gain increases in steps of 1.5 dB with control voltage.

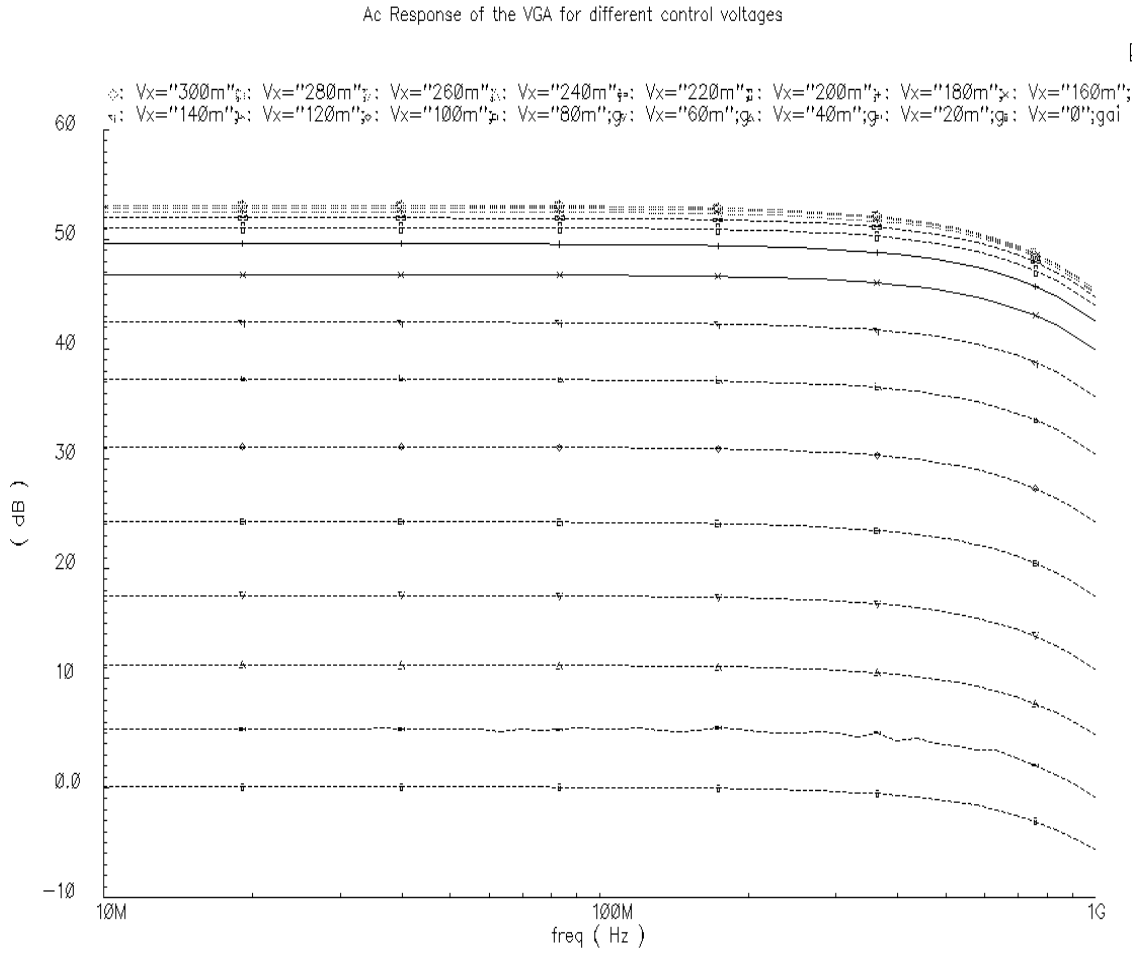

Fig. 49. AC response of the VGA for different control voltages

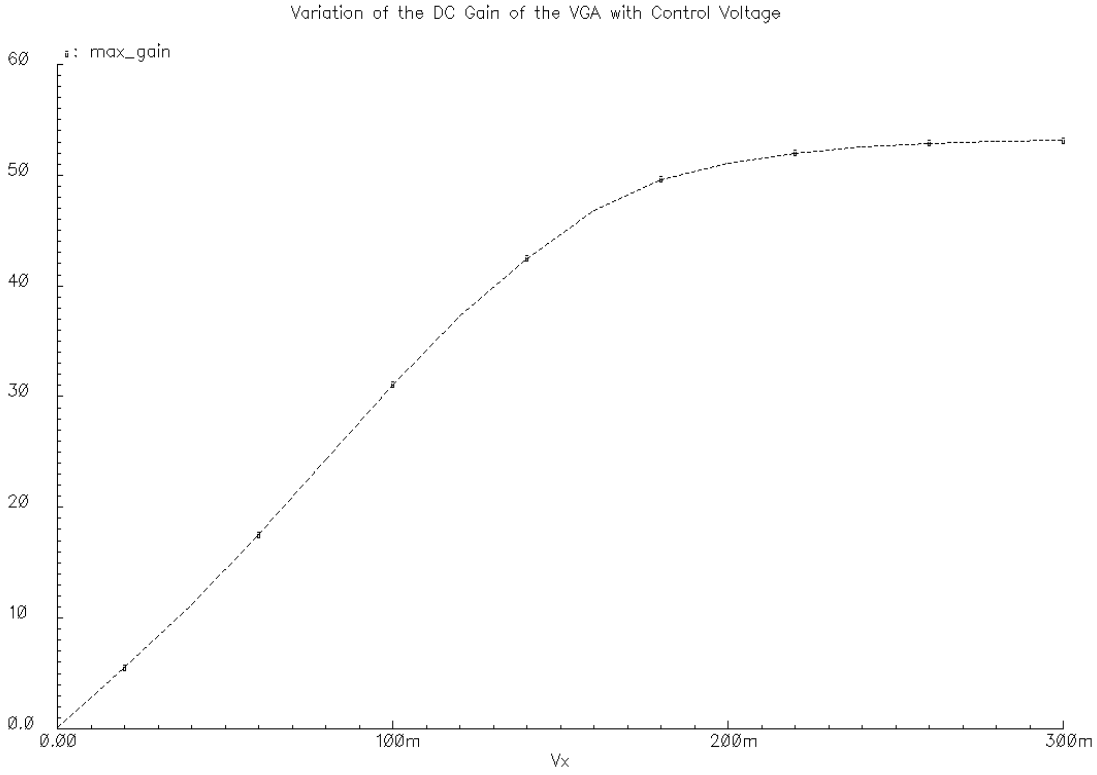

Fig. 50. Maximum DC gain vs control voltage

The transient response of the VGA is given in Fig. 51. This test was performed as part of the mutli-tone test in which the circuit was excited by a multi-tone input signal with one band eliminated in order to observe the intermodulation distortion components in the missing band. The input signal had components with varying amplitudes, the maximum being 500mV. The gain of the VGA was set to 0dB because the noise-to-power ratio has higher significance for lower gain settings. This is because low gain setting implies that the VGA is excited with an input signal of high amplitude. As explained in section D of chapter II, the higher the amplitude of the input signal, the higher the power of the intermodulation components and hence the greater the distortion.

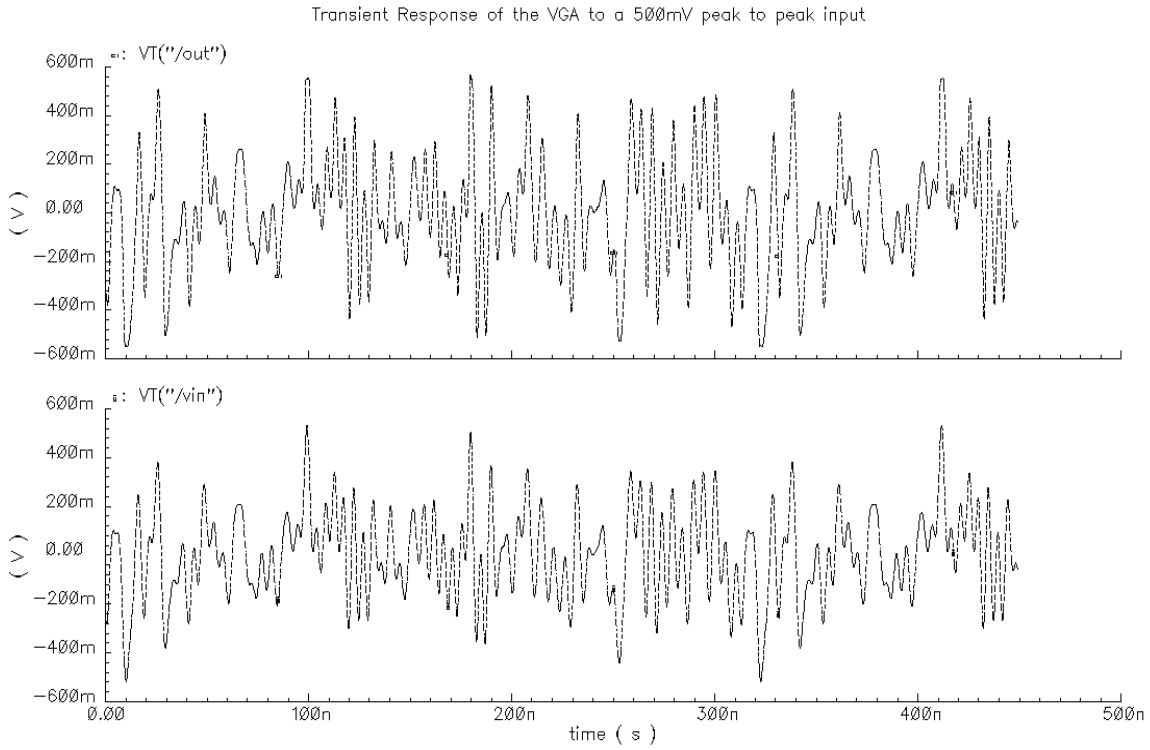

Fig. 51. Transient response of the VGA

Graphs of the equivalent input referred noise of the VGA are given in figures 52 and 53.

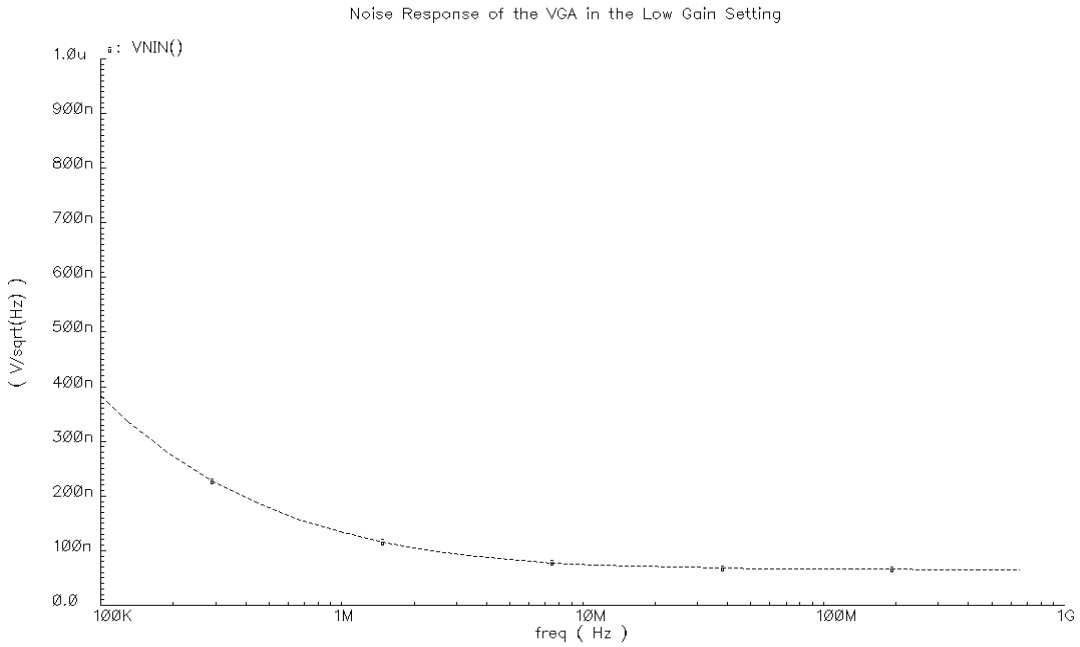

Fig. 52. Input referred noise response of the VGA in the low gain setting

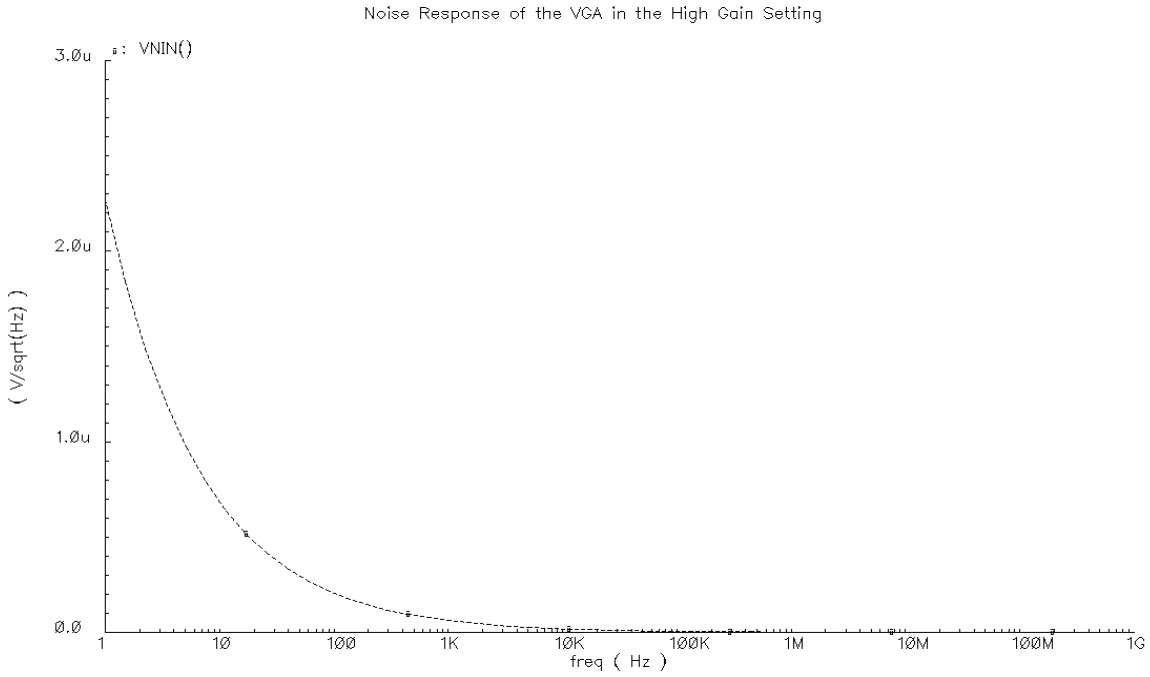

Fig. 53. Input referred noise response of the VGA in the high gain setting

The plots for the CMRR of the VGA in both gain settings are shown in figures 54 and 55. The CMRR is observed to be very high due to the absence of mismatches.

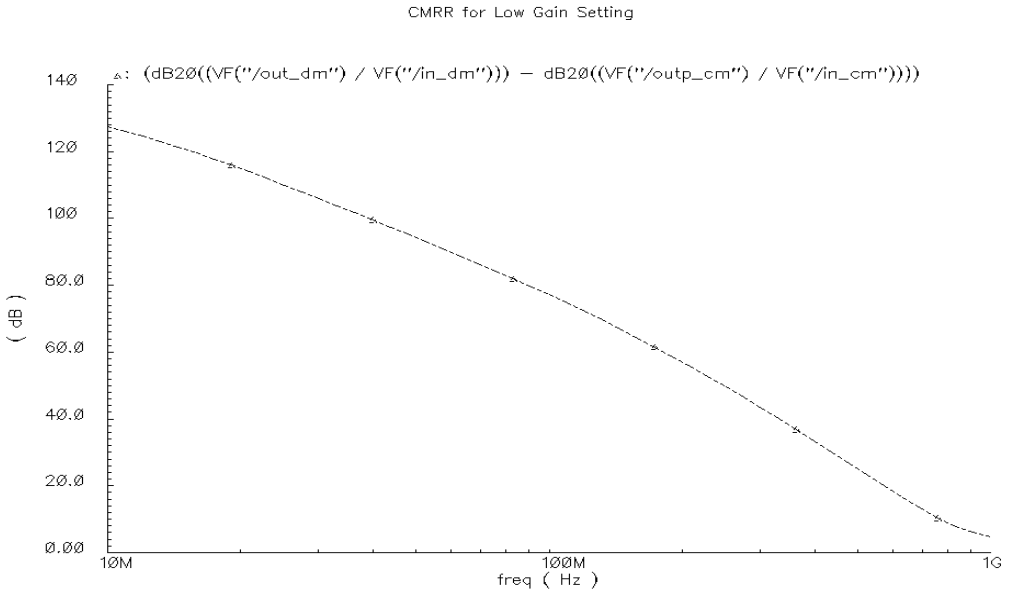

Fig. 54. CMRR of the VGA in the low gain setting

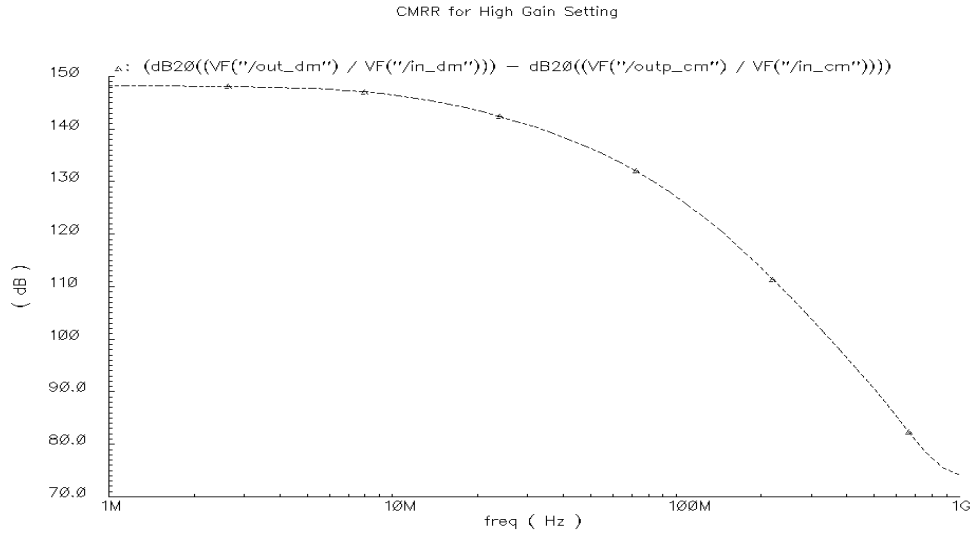

Fig. 55. CMRR of the VGA in the high gain setting

The CMRR of the VGA with 5% mismatch in the input transistors of the first stage is given in figures 56 and 57.

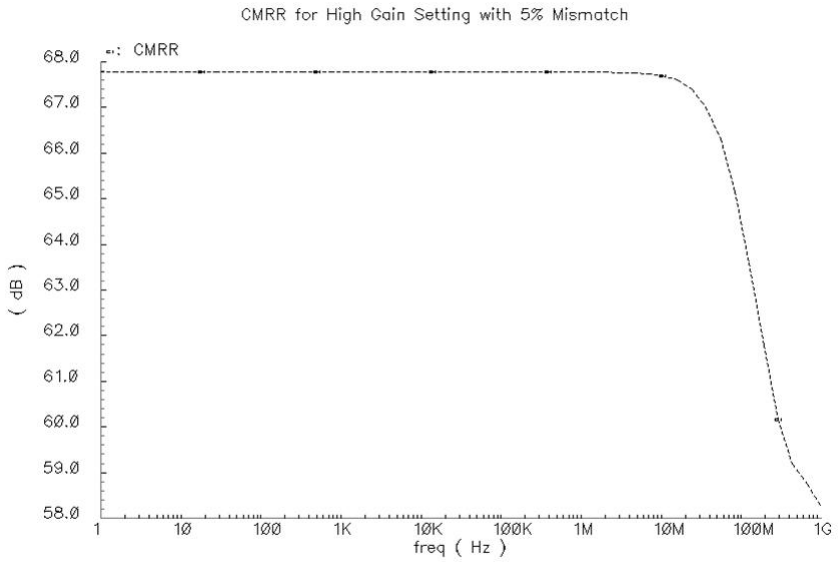

Fig. 56. CMRR of the VGA in the high gain setting with 5% mismatch

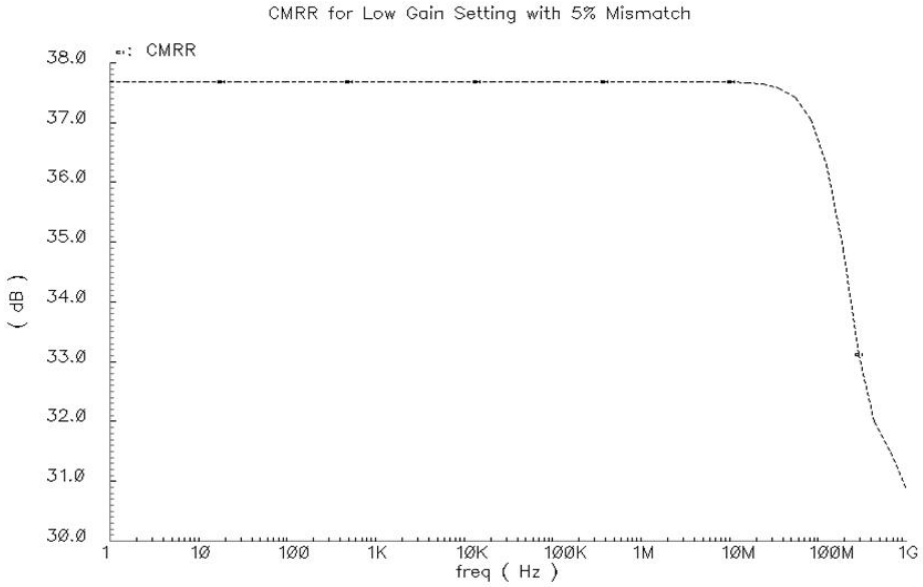

Fig. 57. CMRR of the VGA in the low gain setting with 5% mismatch

The PSRR of the VGA with 5% mismatch in the input transistors of the first stage is given in figures 58 and 59.

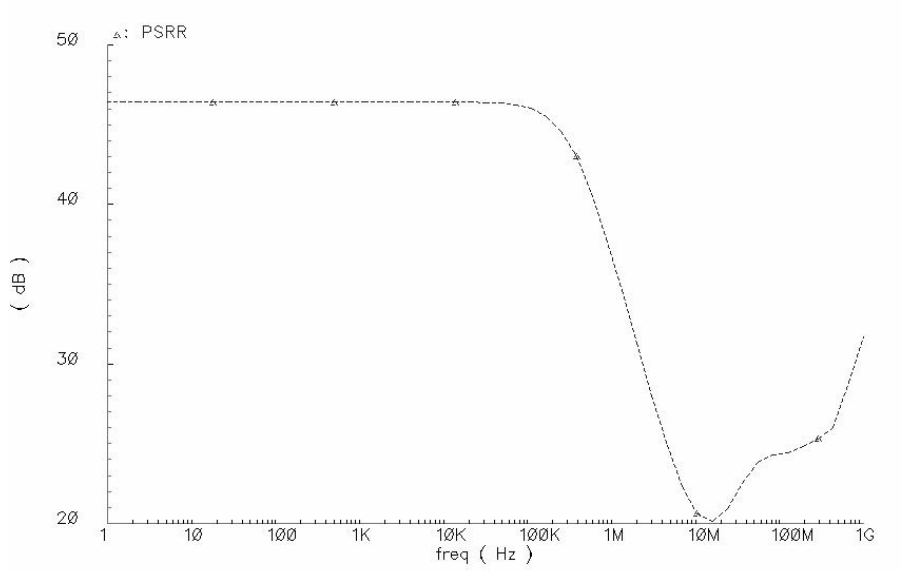

Fig. 58. PSRR of the VGA in the low gain setting with 5% mismatch

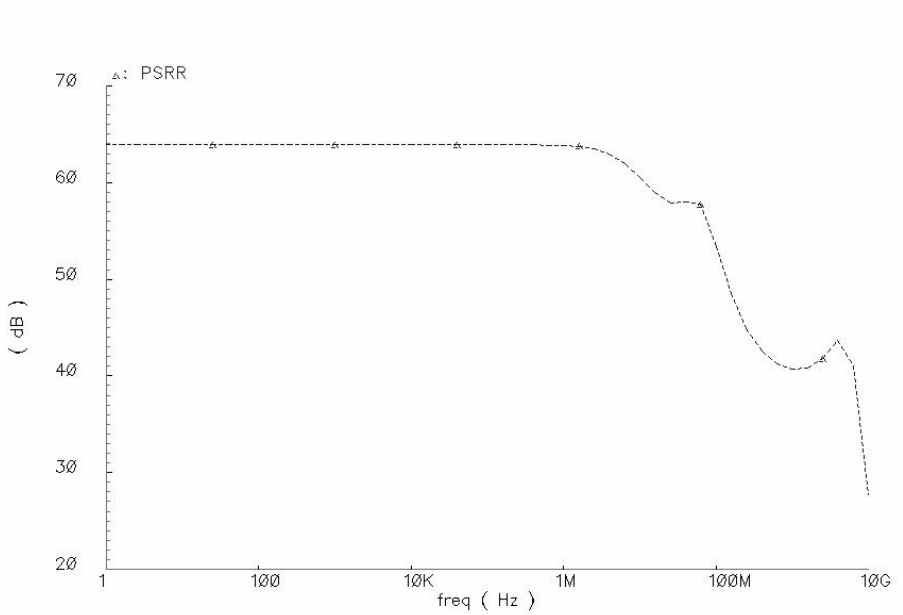

Fig. 59. PSRR of the VGA in the high gain setting with 5% mismatch

B. Post-Layout Simulations

Post-layout simulation results are provided for the VGA designed in 0.18µm CMOS technology. The effects of parasitic capacitances are observed in these simulations, as a result of which the specifications achieved are slightly different from those of the schematic.

The AC response of the VGA for the low and high gain settings is shown in figures 60 and 61 respectively. Due to parasitics, the bandwidth of the VGA dropped significantly post-layout, with a difference of over 120MHz between the schematic and post-layout simulations.

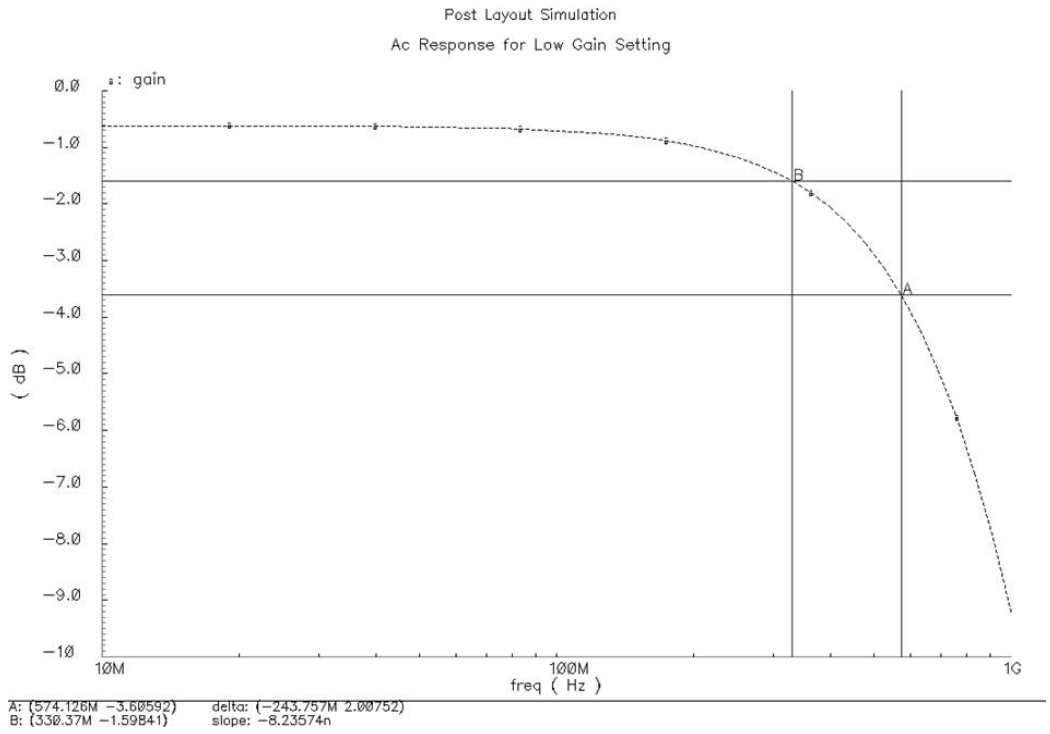

Fig. 60. Post-layout simulation - AC response of the VGA in the low gain setting

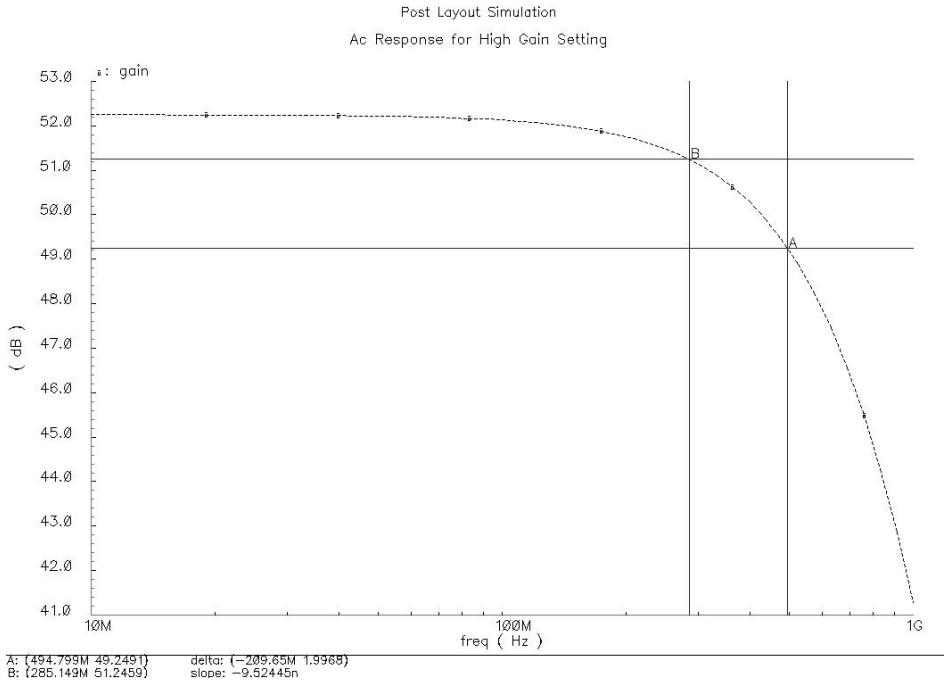

Fig. 61. Post-layout simulation - AC response of the VGA in the high gain setting

Graphs of the equivalent input referred noise of the VGA are given in figures 62 and 63.

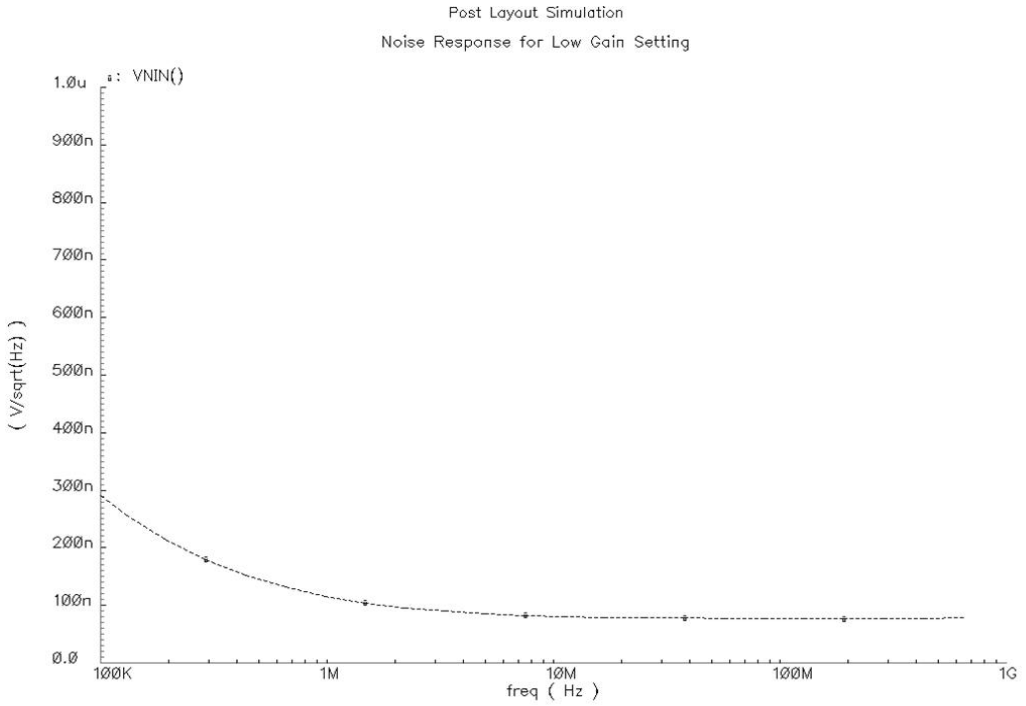

Fig. 62. Post-layout simulation - Input referred noise response of the VGA (low gain)

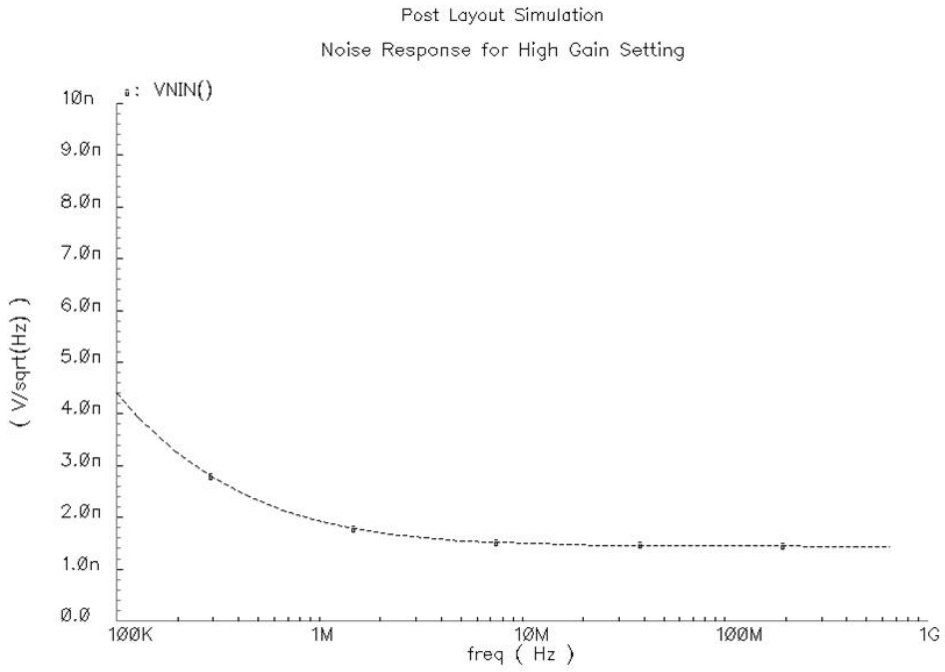

Fig. 63. Post-layout simulation - Input referred noise response of the VGA (high gain)

The plots for the CMRR of the VGA in both gain settings are shown in figures 64 and 65.

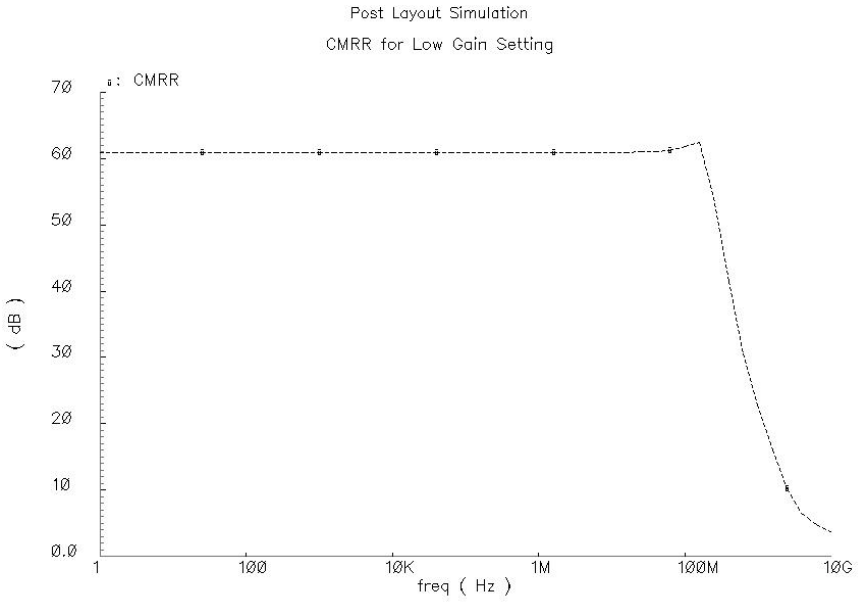

Fig. 64. Post-layout simulation - CMRR of the VGA in the low gain setting

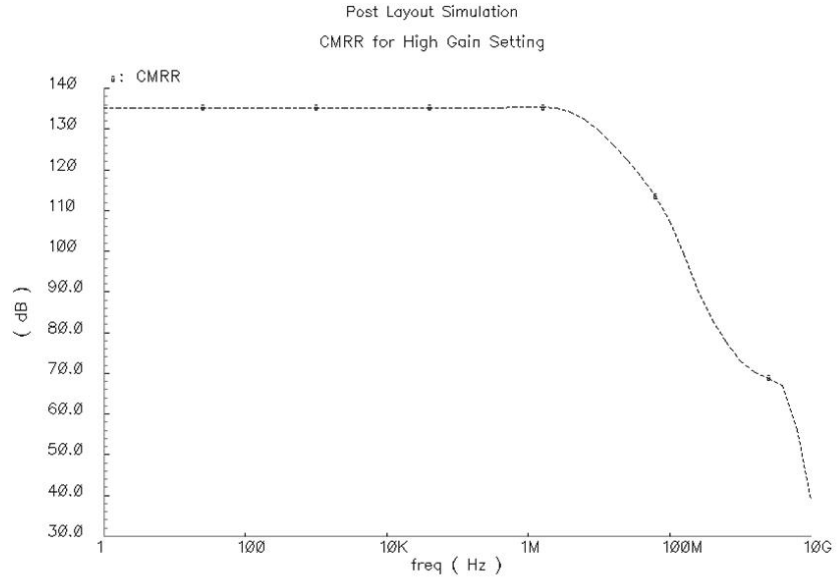

Fig. 65. Post-layout simulation - CMRR of the VGA in the high gain setting

The transient response of the VGA to a multi-tone input signal is given in Fig. 66.

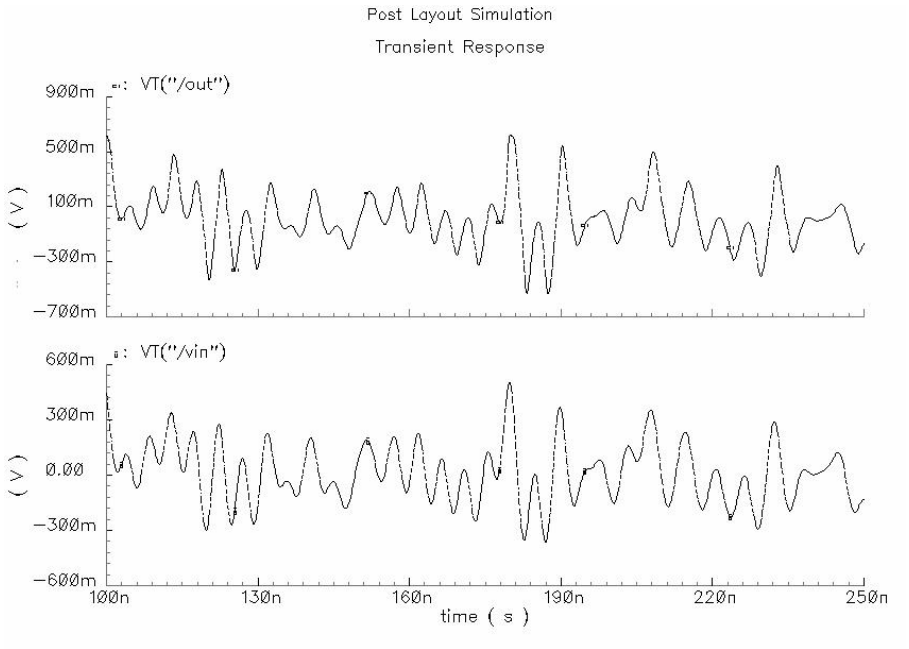

Fig. 66. Post-layout simulation - Transient response of the VGA to a multi-tone input

Summaries of the schematic and post-layout simulations are given in tables II and III. It can be observed from both the tables that there is not much difference between the results of the schematic and the layout simulations, except in the case of the bandwidth of the VGA. The input referred noise has increased marginally while the gain range remains approximately the same. The output voltage swing is $1V_{p\text{-}p}$ in the schematic simulation and 0.95 $V_{p\text{-}p}$ in the post-layout simulation.

TABLE II
RESULTS OF SCHEMATIC SIMULATIONS

Parameter	Low Gain Setting	High Gain Setting
Gain	0.089 dB	53.12 dB
-1dB bandwidth	452.6 MHz	366.53 MHz
-3dB bandwidth	742.6 MHz	619.14 MHz
NPR	-22.5 dB	-
Integrated input referred noise	3.52 μV^2	0.98 nV^2
Power consumption	27 mW	28.5 mW
Output voltage swing	$1V_{p-p}$	-

TABLE III
RESULTS OF POST-LAYOUT SIMULATIONS

Parameter	Low Gain Setting	High Gain Setting
Gain	-0.62 dB	52.25 dB
-1dB bandwidth	330.4 MHz	285 MHz
-3dB bandwidth	575.2 MHz	495 MHz
Integrated input referred noise	3.732 μV^2	1.075 nV^2
Power consumption	25.74 mW	26.9 m
Output voltage swing	950 mV_{p-p}	-

Table IV presents a comparison between the specifications achieved by the VGA in this thesis and the different VGA topologies reported previously. The bases of comparison are the gain and the -3dB bandwidth, taking into account the technology used. It can be observed from the table that in most cases, either the bandwidth is high or the gain range is high, and only in a few topologies are both reasonably high. The proposed VGA shows a very promising performance and it consumes lower power than the other VGAs to achieve a good gain range and a wide bandwidth.

TABLE IV

PERFORMANCE COMPARISON OF VGA ARCHITECTURES

Ref	Principle	Gain-range (dB)	Bandwidth (MHz)	Power (mW)	Supply Voltage (V)	Tech. (μm)
[4]	Pseudo exponential gain control	15 (-5 ~ 10)	150	12.5	3.3	0.5
[7]	Pseudo exponential gain control	25 (6 ~ 31)	85	10	NA	2
[8]	Folded Gilbert Cell with DC offset cancellation	50 (-16 ~ 34)	2000	40	1.8	0.18
[15]	Source degeneration	17 (0 ~ 17)	> 360	N.A	3	0.25
[17]	Signal summing VGA with gain compensation	81 (-70 ~ 11)	380	64	2.5	0.25
[18]	Source degeneration	60 (-15 ~ 45)	246 (0.2 dB)	27	3	0.35
[19]	Folded cascode opamp with current feedback	18 (1.5~19.5)	300	22	3.3	0.5
[20]	Source degeneration	70 (-20 ~ 50)	110	18	3	0.6
This work	Cascode amplifier with frequency compensation	53 (0 ~ 53)	500	27	1.8	0.18

CHAPTER V

CONCLUSION

A wideband CMOS VGA in 0.18 μm technology is presented in this thesis. The gain of the VGA is varied by changing the current and hence the transconductance of the input transistors of each of the two variable gain stages, while maintaining the transconductance of the load constant in order to achieve a constant bandwidth through out the gain range. The VGA exhibits a very low input referred integrated noise and good linearity, both of which are important for its robust performance in the ultra wideband system. Common mode feed back and D.C. offset cancellation circuits have been included in the design to achieve high CMRR and PSRR and to minimize input referred offset respectively.

The gain control system involves conversion of the digital input to the VGA from DSP into an exponential analog voltage. A total variable gain range of 0-53 db is achieved with low power consumption. Digital control has been used wherever possible to increase the programmability of the VGA. Frequency compensation techniques such as capacitive neutralization of Miller effect, cascoding and inductive peaking greatly improve the VGA's bandwidth. The use of cascoding to increase the gain range of the VGA as well as its bandwidth has trade-offs with the linearity and output voltage swing.

However, the circuitry for detecting the DC offset at the output of the ADC and subsequent generator of control bits to automatically correct the offset has not been developed. Hence this process requires manual variation of the control bits to overcome the offset problem.

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