Design and Stability Analysis of 6T and 7T SRAM Cells

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Introduction

The aim of this research was to compare different designs of Static Random Access Memory (SRAM) cells and determine if the 6 Transistor (6T) variant is superior the 7 Transistor (7T) variant at small scales. Furthermore, it aims to provide a detailed analysis of effective SRAM cell design and which parameters engineers should aim to prioritize. As the demand for smaller and more power efficient devices grows, it is important for engineers working in industry to know this information.

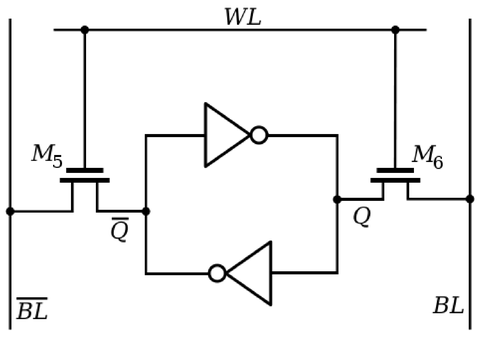

Figure 1. Block diagram model of typical SRAM cell.

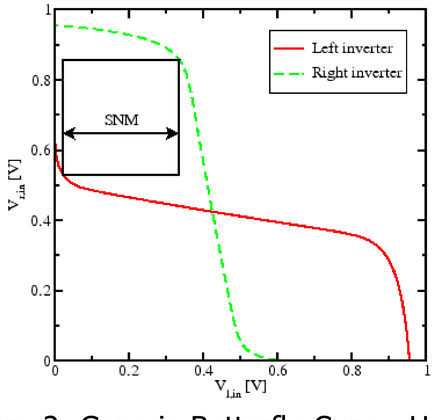

Figure 2. Generic Butterfly Curve. Used to determine the Static Noise Margin (SNM).

Methods/Materials

Previous research done on the topic was selected to be analyzed. Information regarding SRAM performance at scale as well as design techniques was extracted and compiled into conclusions. To be considered, a paper was required to discuss SRAM design or performance. In total, 5 papers were analyzed and are listed below

1. Stability and Static Noise Margin Analysis of Low-Power SRAM
2. A New 7-Transistor SRAM Cell Design with High Read Stability
3. Characterization of a Novel Low Leakage Power-Efficient Asymmetric 7T SRAM Cell
4. Static Noise Margin Analysis of SRAM Cell for High Speed Application
5. SNM Analysis of Sram Cells at 45nm, 32nm and 22nm Technology

Results

$$\mathrm{CR} = \frac{Gate\ Transisor\ Size}{Inverter\ Transistor\ Size}$$

Figure 3. Definition of CR ratio as Gate Transistor size to Inverter Transistor size. [2]

Voltages		SRAM 6T	SRAM 7T
V_{DD}	V_{SS}	Read Delay (ps)	Read Delay (ps)
1.2	0	10.5	5.6
1.08	0	16.3	10.22
1.08	0.12	25.94	15.36
0.96	0.12	47.65	27.62
0.96	0.24	55.68	33.02
0.84	0.24	64.13	58.53
0.84	0.36	-	68.36
0.72	0.36	-	80.4

Figure 4. Comparison of 6T, 7T cell's SNM operating at differing supply voltages. [1]

- ✓ Supply voltage impacts a cell's SNM concurrently to transistor size.
- ✓ Asymmetrical transistor selection can improve cell SNM by upwards of 20% in some cases.
- ✓ This asymmetry can be calculated using what is known as the Cell Ratio.
- ✓ 6T data suggests it might perform better than 7T at smaller scales.

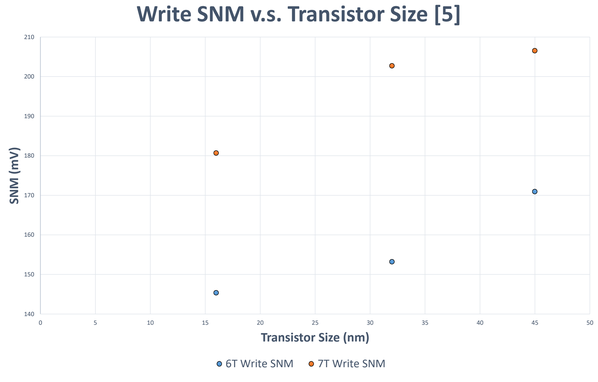

Fig. 5. Comparison of 6T and 7T cells write SNM at different sizes.

Conclusion and Future Research

Insufficient data was collected to determine if the 6T variant holds any significant advantage over the 7T. Furthermore SRAM cell design can be implemented successfully by using techniques of Transistor Asymmetry as well as selecting appropriate supply voltages. Limited research has been published on small scale SRAM design, but contacting companies such as AMD and Intel may provide the needed information.

References

[1] R. Keerthi and C. H. Chen, "Stability and Static Noise Margin Analysis of Low-Power SRAM"
[2] D. Shashidhar, V. Sharma, G. R. Prashanth, Y. B. N. Kumar and M. H. Vasantha, "Characterization of a Novel Low Leakage Power-Efficient Asymmetric 7T SRAM Cell"
[3] Mukherjee, Debasis. (2010). Static Noise Margin Analysis of SRAM Cell for High Speed Application.

All are available upon request

Acknowledgement

I would like to thank Dr. Prabha Sundaravadivel for encouraging me to take on this project. I learned many fascinating pieces of information that have given me a new perspective on the Semiconductor industry, and what "going smaller" actually entails.