May 2021

Thermally Enhanced Stacked Inductor Design for Voltage Regulator Modules

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ABSTRACT

ASIC power requirements have gone up exponentially due to the demand from IoT computing, AI and big data. The VRM (Voltage regulator module) needs to have high power capabilities and efficiency in order to satisfy the TDP (Thermal Design Power) requirement. High peak power operation mode, has also become an industry practice to improve the ASIC instantaneous throughput. This requires more phase count to support the peak current needed during transient. ASIC chips have also increased in size due to the higher pin count for HSIO (High Speed I/O) and interconnects. In order to fit within the limited VRM placement area, a higher power density VRM design is required.

In order to minimize the VRM solution size, and keep good thermal performances, a stacked inductor with a thermal band wrapped around to make contact with the Power Stage (Driver MOS) underneath is introduced. This solves both the space issue and thermal problems from a conventional stacked inductor design. The thermal band, can be either assembled during the inductor manufacturing stage, or can be clipped on to a regular inductor before the SMT stage. This provides a cost effective, reliable and compact VRM structure. Simulation and test results are verified the effectiveness of the proposed structure.

KEYWORDS

- Multi-phase voltage regulator
- Buck converter
- Inductor on top
- Stacked Inductor
- Power module

- Thermal band
- Pulse width modulation (PWM)

BACKGROUND

Modern ASIC have increased in size, TDP, and TDC (Thermal Designed Current). An integrated power management unit also enables the ASIC to consume higher peak power than the TDP in order to improve transient throughput. The TDP of the ASIC has been limited to around 300W due to cooling methods and I^2R losses in a traditional 12V VIN air cooled environment. However, as water/immersion cooling and 48 (54) V power delivery becomes widely available, the TDP of a typical ASIC can reach up to 700W in a modern datacenter. Thus, VRM density has become a bottle neck for ASIC performance.

In order to support peak power mode operation, a high phase count VRM is needed in order to satisfy the efficiency, slew rate and thermal requirements. However, due to the high pin count, HSIO, HBM (High Bandwidth Memory) and chip interconnect SI (Signal Integrity) requirements, the VRM needs to be compact in both the width and length. This allows the VRM to be placed as close to the ASIC as possible, optimize the PDN (Power Distribution Network), but also compact enough to be far away from the HSIO routing channels.

In summary, below are the challenges for future ASIC load requirements:

- Peak current increasing for burst workloads.
- Sustained current increasing as thermal solution improves and VRM input voltage increase.
- f_{sw} going to 1.5MHz range for faster and tighter regulation tolerance.
- Load and PDN split into more quadrants to optimize Amps/pin for large MCM (Multi Chip Module) packages.
- VRM area reduced unless pushed out further from the ASIC, which decreases efficiency and transient response

- Cavity size decreasing because higher pin density needs stronger mounting hardware, thus fewer cavity caps and more phases needed for transient power operation

There are two major drawbacks by putting the inductor on top of the power stage. (1) The power stage will suffer from thermal issues because the entire device is covered by the inductor. (2) The assembly house may need to reflow the board twice in order to have both the power stage and inductor reflowed correctly. This will create thermal stress on the entire motherboard. In order to implement a flexible design while satisfy both the power density and thermal performance, a new structure is introduced based on the popular inductor on top of power stage architecture:

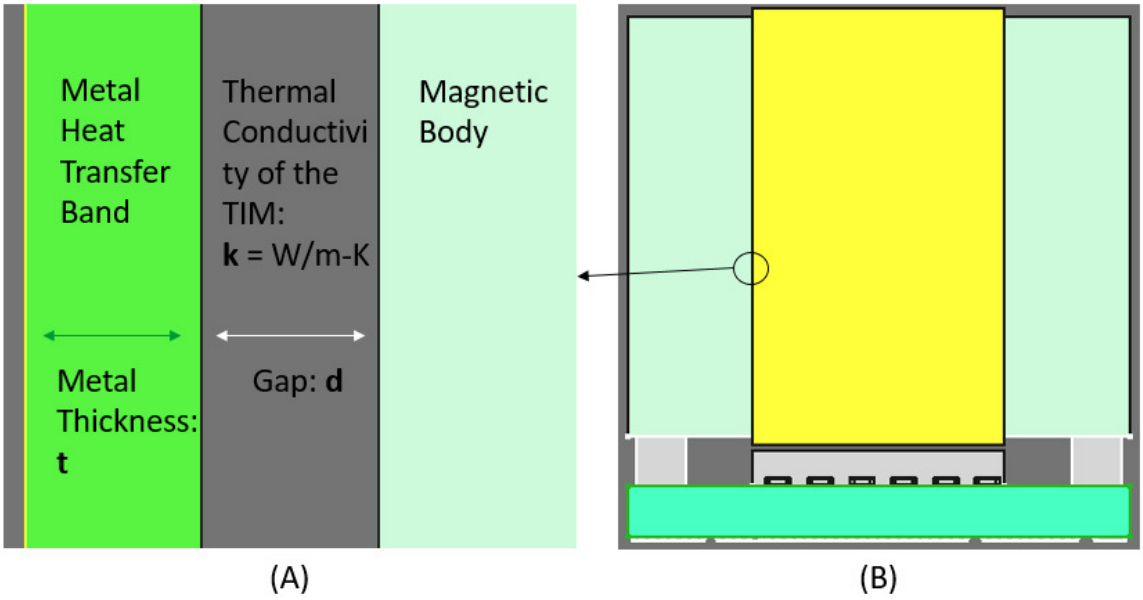


***Fig. 1*: General structure of the thermally enhanced stack inductor design for voltage regulator modules (code name: Musubi). (A) The thermal interface between the magnetic core and thermal band. (B) The structure of the proposed inductor in a power module design.**

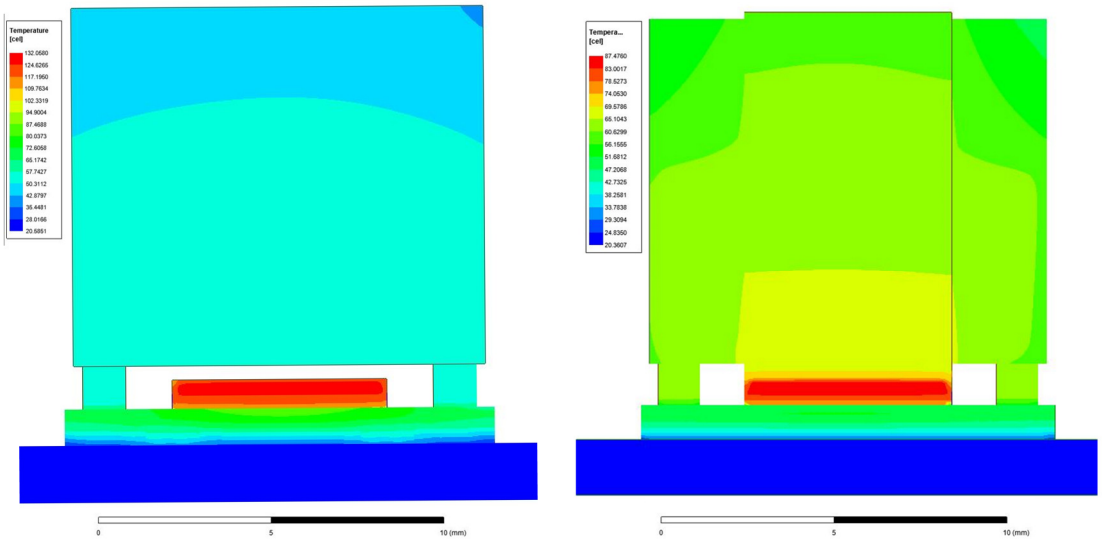
Fig. 1A illustrates the thermal interface between the magnetic body and the thermal band from a side view. The material used for the metal band can be copper, or aluminum, or other metals.

The thicker the wall **t**, the better the thermal flow rate to the top (dual side). The gap **d**, between the metal band and magnetic body will determine air flow. The thermal conductivity of the TIM **k** can range from 0.024 (Air) to 385 (Cu) [Direct Contact], to adjust the cooling priority. Fig. 1B illustrates the general structure of the power module. The thermal band around the inductor will be placed in contact with the power devices at bottom via a thermal interface material (TIM). The thermal band reaches all the way to the top of the inductor. Depending on the air flow and thermal requirements, an optional heatsink can be added to further improve the cooling effect. The thermal band is electrically natural, and can provide certain amount of EMI shielding. It can be made from stamped copper, which is the same process of making a winding of the inductor.

DESCRIPTION

The proposed module solution is easy and flexible in manufacturing, either PCB or substrate can be applied. The thermal band can be installed by inductor manufacturer, or by assembly house using a clip around the traditional inductor. The overall cost increase for the module from discrete solution is moderate, and no special process is required during both the manufacturing of the module and assembly house.

To verify the proposed module solution, thermal simulations are employed using a virtual chassis, 50% +/- x and +/- y direction extension, 200% +z direction extension and 100% -z direction extension. 400CFM air flow is defined on the +X surface. As a result, 32m/s air flow is generated in the defiend tunnel. The estimated loss on the power device is about 2.4W and the inductor is about 0.8W, based on 12V Vin, 1.8V Vout and 30A TDC.



(A) **(B)**

Fig. 2: **Simulation results with temperature distribution, (A) Power module with traditional inductor-on-top design, (B) Power module with thermally enhanced inductor design and thermal interface materials in the gap between device top and inductor bottom.**

According to the simulation results as shown in Fig. 2, with Cu band on the inductor and thermal interface materials filled in the gap between device and inductor, the junction temperature is 45°C lower than that in the traditional module design, indicating that the proposed inductor and entire module architecture can significantly improve thermal performance, which is critical for server applications. To further verify the simulation model, and also investigate the thermal performance of the proposed module, several variables are applied in additional simulations, such as air flow speed, Cu band thickness. Further Thermal simulation has been conducted based on the model from Fig. 2, the corresponding simulation conditions and results are summarized in Table I.

Table I: **Summary of simulation results with different model and boundary conditions.**

Model	Air flow	Tj_max	T_casetop_max	T_inductor_max	T_band_max
No Cu Band	400CFM	132.07 ºC	128 ºC	66.83 ºC	/
0.2mm Cu Band	100CFM	105.34 ºC	105.29 ºC	88.47 ºC	88.50 ºC
0.2mm Cu Band	400CFM	87.84 ºC	72 ºC	70.62 ºC	70.65 ºC
1.0mm Cu Band	400CFM	71.06 ºC	70.99 ºC	53.71 ºC	60.54 ºC

Based on the thermal simulations results, experiments were conducted in order to further verify the concept. In the experiments, a regular inductor was equipped with 0.05mm copper foil, and 3 different setup are studied:

(1) Inductor with copper tape in discrete (original) placement.

(2) Inductor with copper tape turned 180 degrees, sitting on top of power stage with TIM.

(3) Inductor with copper tape on top of power stage with heatsink on top.

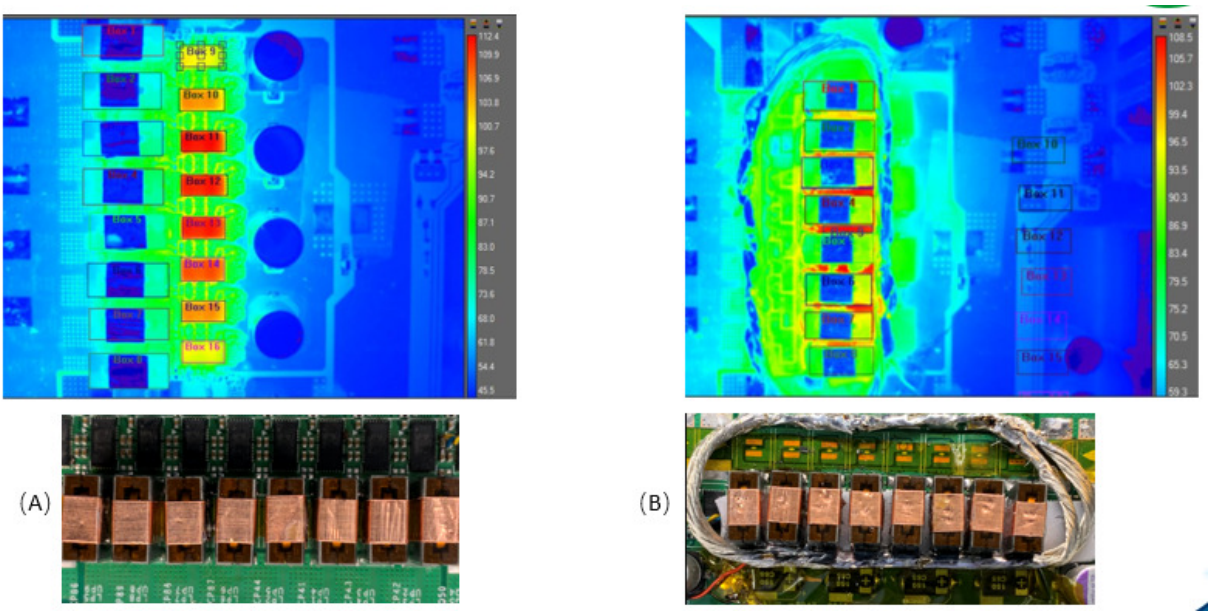


Fig. 3: **Thermal imaging results for both the discrete arrangment(A) and stacked inductor with thermal band (B) to an 8 phase internal VR test vehicle. The test was performed at 12V in, 1.8V out with 240A DC current and 15 minute soak time. The Air flow is measured around 200 CFM.**

From the above thermal imaging results, after inductors are reworked, the power stages are covered with a 17W/mK thermal interface materials. With no air flow to the device, and with 240A TDC, the device will usually hit OTP within 1 minute without adequate cooling. However, from Fig. 3B we can see that the new arrangement has passed the 15 min soak in test, and thermal band is providing passive cooling to the power stage underneath.

Finally, the Efficiency comparison was done to further verify this idea. The test used the same set of inductors, performed at 30C ambient temperature. Each setup was tested 3 times with 5 minutes cooling in between. The end result is then averaged. The test condition is 12V in, 1.8V out, with 800 KHz switching frequency and 70nH inductors.

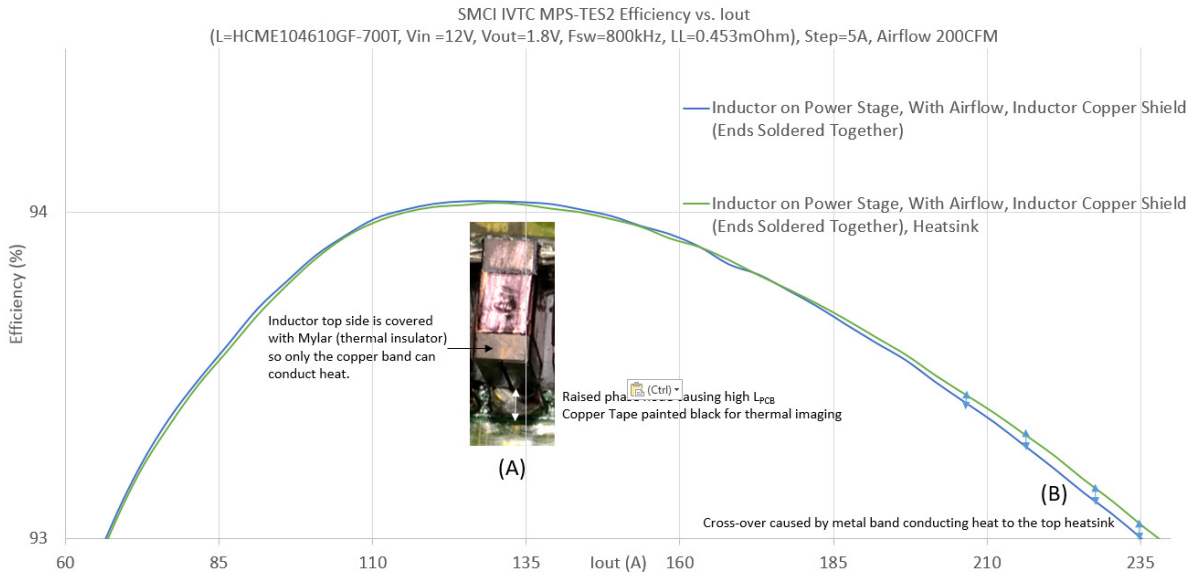


Fig. 4: **Efficiency results for the 3 arrangements. (A) The reworked device. (B) Cross over at higher current load indicates the thermal band heat conduction effectness.**

From efficiency chart Fig. 4B, we have added a heatsink on top of the arrangement, and observed efficiency curve cross over, and sepration at high current loads. The surface of the inductor is covered with mylar, so the only heat transfer path is from the thermal band.

A design of module footprint is demonstrated in Fig. 5. The module can be either with traditional two terminal inductor, or with TLVR inductor for improved transient performance. The footprint is 4.4x12mm, which is super-slim for high density ASIC power applications.

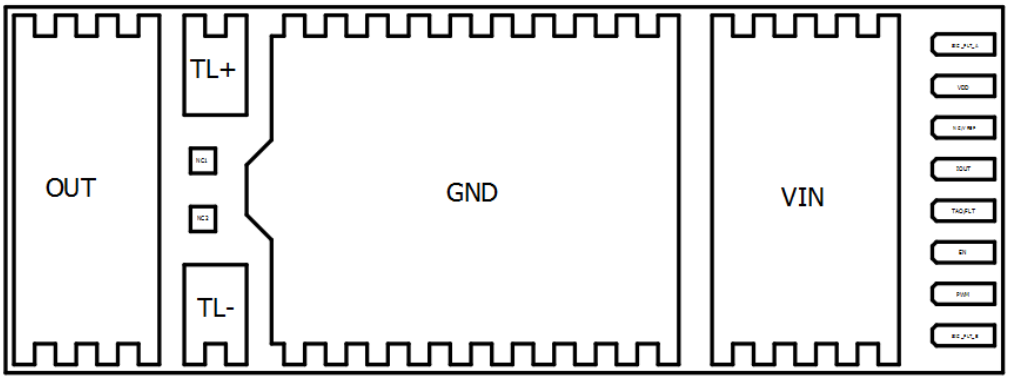


Fig. 5: **Example land pattern and pinout for a 4.4mm * 12mm * 13mm module that supports TLVR.**

CONCLUSIONS

The paper proposed an innovative thermally enhanced super slim module design, with inductor on top 3-dimensional solution, for high density ASIC power applications. The proposed module solution features very slim form factor, which is compact in both length and width, allowing more spaces on the ASIC motherboard for high density interconnections while remaining high power rating based on modernized ASIC power requirement.

A metal band structure is proposed on the surface of the inductor. Together with TIM applied at the gap between power ICs and inductors, the thermal performance of the proposed module solution is significantly improved compared with traditional module solution. It is also compatible with TLVR solution for improved transient performance while maintaining great efficiency as required by server applications.

The proposed module solution is also easy to manufacture with limited cost increase. It can be used as a standard unit for future ASIC power design.