CMOS FRONT-END AMPLIFIER FOR BROADBAND DTV TUNER

A Thesis

by

GUANG ZHANG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2005

Major Subject: Electrical Engineering

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ABSTRACT

CMOS Front-End Amplifier for Broadband DTV Tuner.

(May 2005)

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In this work, the design of a CMOS broadband low noise amplifier with inherent high performance single-to-differential conversion is presented. These characteristics are driven by the double quadrature single conversion digital television tuner which requires accurately balanced differential signals to perform its function and to improve image rejection.

A three-stage amplifier is designed to satisfy several requirements of front-end circuits at the same time. The resistive shunt-feedback topology is adopted to implement a single-ended broadband low-noise amplifier as the first stage. The second stage is an on-chip single-to-differential converter, which employs a novel method to improve its balancing performance. A fully differential buffer capable of driving heavy loads is used as the third stage to further suppress the phase and magnitude errors of output differential signals.

Fabricated in 0.35μm TSMC standard CMOS technology, the designed broadband front-end amplifier manages to limit the phase error to within ±1.5° and magnitude error ±0.75dB over 50~850 MHz frequency range, with 16dB gain and a noise figure of 4dB.

To my parents, my brother, and my beloved wife …

ACKNOWLEDGMENTS

Upon finishing my graduate study at Texas A&M University, I would like to take this opportunity to express my most sincere appreciation to Dr. Jose Silva-Martinez, for his guidance, encouragement, his academic foresight and technical insight, and also his patience in directing this work. As my advisor, he has been the sole support for my research and study in the past several years. His great personality made my academic life more enjoyable.

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Almost all my research time was spent with DTV Tuner group. The contribution and cooperation of the team members made the learning and research a great experience for my life. Here I would like to thank Jianhong Xiao, and Tianwei Li, for the great team environment we created together. Special thanks go to my best friend, Shanfeng Cheng, who gives me much needed academic knowledge. I will keep in my memory all the days and nights we spent together.

I wish to express my deep appreciation to my parents and my brother Cheng. Also, the last but not least one I want to give thankfulness is my dear wife Ping, for her love and support. They have been extremely important not only in making me who I am, but also in helping me through the highs and lows that have accompanied my life.

TABLE OF CONTENTS

Page

ABSTRACT iii

DEDICATION iv

ACKNOWLEDGMENTS v

TABLE OF CONTENTS vii

LIST OF FIGURES ix

LIST OF TABLES xi

CHAPTER

I INTRODUCTION 1

1.1 Application Background 1
1.2 Double-Quadrature Single-Conversion Architecture for DTV Tuner 2
1.3 Objectives and Challenges of Front-End Amplifier Design 5
1.4 Previous Work 7
1.5 Organization of Thesis 8

II SINGLE-TO-DIFFERENTIAL SIGNAL CONVERSION 9

2.1 Traditional Solution 9
2.2 The Imbalance Problem 11
2.2.1 Errors Due to Parasitic Capacitors and Finite Resistance at the Common-Source Node 13
2.2.2 The Effect of Gate-to-Drain Capacitors 16
2.3 Novel Balancing Method 21
2.3.1 Step One: Adding A Bypass Capacitor 21
2.3.2 Step Two: Adding A Load Balance Capacitor 23
2.4 The Benefits of Adding Another Differential Stage 27

III A CMOS BROADBAND FRONT-END AMPLIFIER FOR DTV TUNER 35

3.1 The Specifications of the Front-end Amplifier 35
3.2 Design Considerations 35
3.3 Gain/Noise Budget Link 37
3.4 Design of the CMOS Broadband LNA 38

CHAPTER Page

3.4.1 Topology Selection 38
3.4.1.1 Common-Gate Topology 38
3.4.1.2 Common-Source Topology 40
3.4.1.3 Shunt-Feedback Topology 41
3.4.2 Shunt Feedback Topology Circuit Analysis 42
3.4.2.1 Circuit Model and Transfer Function 42
3.4.2.2 Frequency Response 43
3.4.2.3 Impedance Matching 45
3.4.2.4 Noise Performance of Shunt Amplifier 46
3.4.3 Design Procedure of Shunt-Feedback Broadband LNA 51
3.5 Whole Front-End Amplifier Circuit 53

IV SIMULATION AND EXPERIMENTAL RESULTS 56

4.1 Layout Considerations 56
4.2 Post Layout Simulation Results 59
4.2.1 Broadband Input Impedance Matching, Power Gain and Noise Performance 59
4.2.2 Balance Accuracy of the Differential Output Signal 60
4.3 Simulation Performance Summary 63
4.4 Test and Measurement 64
4.4.1 Measurement of the Magnitude and Phase of Differential Output Voltage 66
4.4.2 The Other Performances of the Whole Front-End Amplifier 69
4.5 Summary of the Experimental Results 74

V CONCLUSIONS 75

REFERENCES 76

VITA 78

LIST OF FIGURES

FIGURE		Page
Fig. 1.1	Dual Conversion TV Tuner	3
Fig. 1.2	Double-Quadrature DTV Tuner Configuration	5
Fig. 2.1	Differential Amplifier With Inherent Single-to-Differential Conversion	10
Fig. 2.2	Differential Amplifier With Non-Ideal Current Source & Parasitic Capacitances	11
Fig. 2.3	Small Signal Model of Conventional Single-to-Differential Converter	12
Fig. 2.4	Traditional Single-to-Differential Converter	18
Fig. 2.5	Output Voltages in Conventional Single-to-Differential Converter	20
Fig. 2.6	Single-to-Differential Converter With Bypass Capacitor	22
Fig. 2.7	Single-to-Differential Converter With Bypass and Load Balancing Capacitor	24
Fig. 2.8	Error Cancellation Results With Bypass and Load Balancing Techniques	26
Fig. 2.9	Fully Differential Buffer	31
Fig. 2.10	Errors Suppression With Differential Buffer	33
Fig. 3.1	Cascade Systems for Computation of Noise Figure	36
Fig. 3.2	Three-Stage Front-End Amplifier	37
Fig. 3.3	Simplified Schematic of a Common-Gate Amplifier	39
Fig. 3.4	Common-Source Amplifier With Resistive Termination	40
Fig. 3.5	Common-Source Amplifier With Shunt Resistive Feedback	41
Fig. 3.6	Small Signal Equivalent Circuit for Shunt Resistive Feedback	42
Fig. 3.7	Simplified Small Signal Circuit of Shunt Feedback Amplifier	45

FIGURE Page

Fig. 3.8 Noise Model of Resistor……...47

Fig. 3.9 Simplified Noise Model for MOSFET in the Active Region…….. 47

Fig. 3.10 Shunt-Feedback Amplifier Circuit for Noise Analysis…… 49

Fig. 3.11 Circuit Configuration of CMOS Front-End Amplifier for DTV Tuner……55

Fig. 4.1 Layout of CMOS Front-End Amplifier for DTV Tuner……. 58

Fig. 4.2 S-Parameter Simulation Results……... 59

Fig. 4.3 Differential Errors at 50°C Using Typical Technology Parameters…….60

Fig. 4.4 Differential Errors With Process Variation and Mismatches……... 61

Fig. 4.5 Errors With Temperature Variation……. 62

Fig. 4.6 Errors Using Fast Corner and Slow Corner……. 63

Fig. 4.7 Die Micro-Photograph of Front-End Amplifier……... 65

Fig. 4.8 Schematic of the PCB…….. 65

Fig. 4.9 Photograph of Printed Circuit Board for Testing……. 66

Fig. 4.10 Experimental Setup for S-Parameter Measurement……. 67

Fig. 4.11 The Phase Error Between Two Output Signals…… 68

Fig. 4.12 The Magnitude Error Between Two Output Signals…… 69

Fig. 4.13 S11 of the Broadband Amplifier…….. 70

Fig. 4.14 Experiment Setup for Noise Figure Measurement……... 71

Fig. 4.15 Gain-Noise Spectrum……... 72

Fig. 4.16 Simplified Package Model……73

Fig. 4.17 Frequency Response Considering Package Model……...73

LIST OF TABLES

Page

Table 2.1 The Circuit Parameters of the Traditional Single-to-Differential Converter 19

Table 2.2 Error Comparison Before and After Compensation 27

Table 2.3 Parameters of Fully Differential Buffer 32

Table 2.4 Error Comparison Before and After Differential Buffer 34

Table 3.1 Target Specifications for Front-End Amplifier 36

Table 3.2 Gain/Noise Budget Link 38

Table 3.3 The Design Specifications for Broadband LNA 51

Table 3.4 Circuit Parameters Summary 53

Table 4.1 Post Layout Simulation Performance Summary 64

CHAPTER I

INTRODUCTION

This chapter starts with a brief introduction on the digital television tuner. Then by discussing the double-quadrature single-conversion DTV tuner architecture, the requirements of the front-end amplifier are obtained. Thirdly, previous work on on-chip single-to-differential conversion is discussed, followed by an elaboration on the organization of the thesis.

1.1 Application Background

Digital Television (DTV) is a new type of broadcasting technology that will transform the television viewing experience. It will allow broadcasters to offer television with movie-quality picture and CD-quality sound, along with a variety of other enhancements, including the transmission large amounts of interactive data accessible from either a computer or television set.

A DTV tuner is typically a broadband RF receiver that can perform signal amplification and demodulation in order to satisfy the requirements of signal reception and compatibility for different communication standards. Functioning as the radio frequency (RF) broadband “gateway”, the basic role of a tuner is to receive all available channels in the input bandwidth. These TV tuners operate over a frequency range of 50M to 850 MHz, taking into consideration those frequencies used by broadcast television and cable operators.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*

The broadband DTV tuner market has been growing explosively in recent years due to the transition from analog television to digital television. Federal Communications Commission (FCC) introduced a phase-in plan for DTV, which mandated that off-air digital TV tuners would be required on nearly all new TV sets in the US market by 2007. Low-cost, high-performance DTV Tuners are in very high demand today.

Until the end of the 1900s, most TV tuners were bulky collections of discrete components. Currently, most manufacturers are integrating the entire functionality of these "canned" tuning systems into a single chip. As applications become more sophisticated, tuners with higher performance are required. New concerns were brought on by the latest tuner applications including smaller form factors, higher reliability, compliance with standards (data over cable system interface specification [DOCSIS], OpenCable, PacketCable), and ease of manufacture.

1.2 Double-Quadrature Single-Conversion Architecture for DTV Tuners

Television tuner technology has changed very little during the past two decades of the last century. Two types of tuners have been in existence during this period: the traditional single-conversion tuner that is typically used in consumer television sets [1], and the dual-conversion tuner in cable television receivers [2].

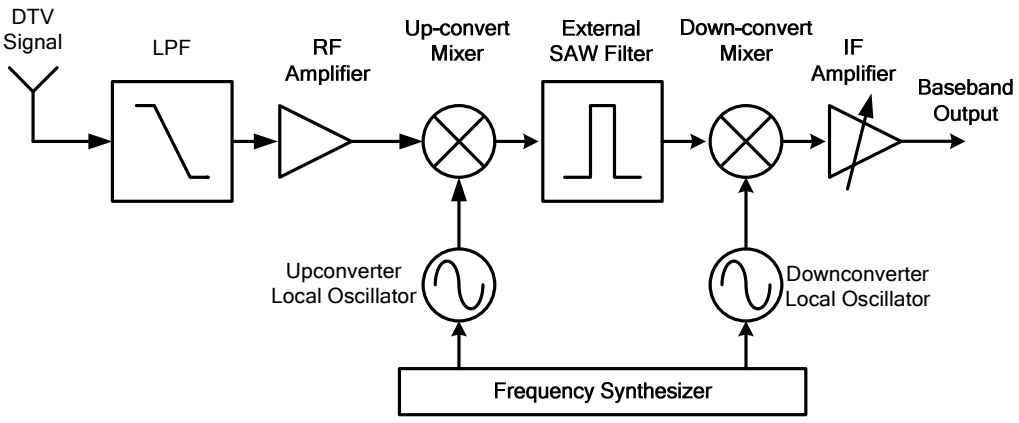


Fig. 1.1 Dual Conversion TV Tuner.

The dual-conversion tuner [3, 4, 5] differs from the single–conversion tuner in that it employs an additional conversion. It first up-converts the entire input spectrum to a high IF, then uses an expensive external SAW filter to achieve the high selectivity, and finally down-converts back to the standard low IF as shown in Fig. 1.1. Until recently, dual-conversion tuners were used for most applications because of its high image rejection and superior selectivity. However, the single down-conversion architecture has been attracting considerable attention in recent years. It has obvious advantages in terms of reductions in complexity and power consumption, and also the possibility to integrate all functions into a single chip [6]. The bottleneck of the traditional single-conversion architecture is poor image rejection, especially at UHF frequencies (higher than 400MHz). The image signal is generated during the tuning process which involves translating signals in frequency. It interferes with the desired channel and has to be suppressed. Traditional quadrature mixing with poly-phase filter can attenuate the image

signal if properly designed. The ultimate image rejection is limited by the quadrature accuracy of the mixer input phase, gain matching of the mixers, and the accuracy of the phase shifters within the poly-phase filter [7]. Without alignment, the image rejection of a quadrature mixer consisting of two multipliers, followed by a poly-phase filter is limited to about 40dB [7]. To obtain image suppression better than 50dB, a double-quadrature architecture [6] [7][8] is needed. Instead of two, it uses four mixers with both RF and LO (local oscillator) inputs with quadrature phases. This structure is shown to be much less susceptible to the imbalance in the phase and amplitude of the mixer's RF and LO inputs [7]. The quadrature RF signals are generated with an RF poly-phase filter, while the quadrature LO signals are generated with a frequency divider by four. While the classic quadrature mixer requires less than 0.1% amplitude and phase error for the quadrature inputs of the mixer, the requirement for both LO and RF inputs of the double-quadrature mixer is only 3% for the same performance [7]. For RF input signals, the 3% amplitude and phase error are spread over the front-end amplifier and the following poly-phase filter. From system spectrum simulations and given the technology limitations, the mismatches for the differential output signal of the front-end amplifier must be limited to ±1.5° phase error and 1.5% magnitude error. Combined with the usage of passive poly-phase filters, it is sufficient to provide the required accuracy for the RF input signal of the double-quadrature mixer.

The configuration of a double-quadrature DTV tuner is shown in Fig. 1.2. The RF signal coming from a single-ended antenna or cable is roughly selected by an external passive band-pass filter (BPF). The signal of interest will be applied to the input of the front-end

amplifier, which is the main focus of this work. The signal will be amplified to satisfy the gain/noise requirements and converted from a single-ended to differential signal. The passive poly-phase filter creates quadrature signals from the differential inputs. After that, the signal is mixed with a quadrature LO signal and translated to a standard intermediate frequency (IF) by the double-quadrature mixer. After the IF poly-phase filter, channel-select filter, and IF variable gain amplifier (VGA), the signal will be sent to the analog-to-digital converter (ADC) and digital-signal-processor (DSP) for further signal processing.

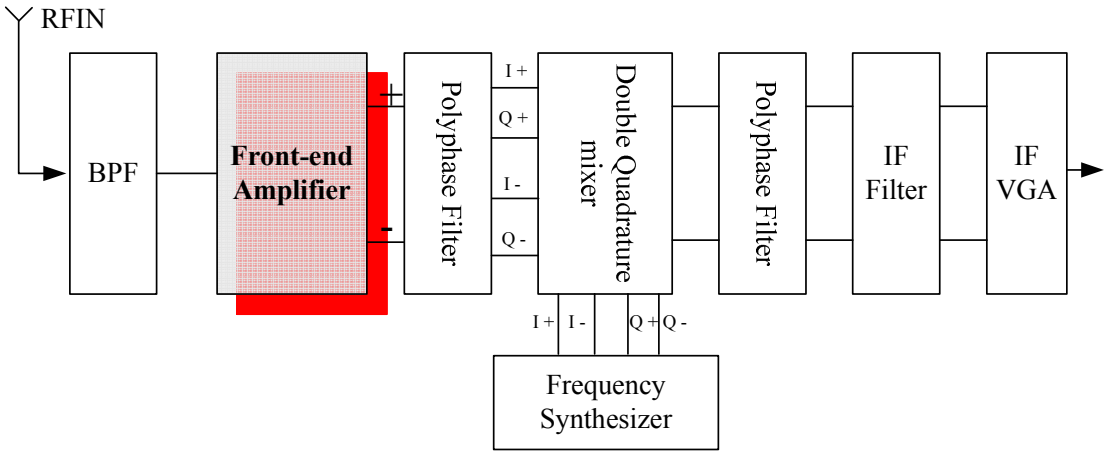


Fig. 1.2 Double-Quadrature DTV Tuner Configuration.

1.3 Objectives and Challenges of Front-End Amplifier Design

For double-quadrature conversion operation, pure differential signals are needed before they are fed to the quadrature signal generator, and the matching accuracy of the

differential signal is highly demanding. Hence, a stage able to convert the single-ended signal into a differential signal with restrained imbalance of phase and magnitude is needed. To obtain differential signal from single-ended signal source such as an antenna or a cable, distributed passive baluns (transformer) or phase shift network are the most popular methods, which have been adopted in the RF/microwave tradition. The disadvantages are the signal loss (usually 2~3dB if the operating frequency range is from DC to 1GHz), occupancy of on-board space and additional cost. Compared with those distributed baluns or phase shift networks, inherent active single-to-differential conversion exhibit some important advantages, i.e., full integration to achieve a system-on-chip (SOC) solution and proper amplification gain rather than loss. The shortcoming of the traditional active single-to-differential converter is that the imbalance of phase and magnitude is relatively large due to parasitic capacitances. Although the techniques to convert differential signals to single-ended one have been well developed, effective solutions for the inverse conversion are still missing, especially for demanding balance accuracy between the two output signals over a broad signal band. Developing circuit techniques that provide single-to-differential conversion with high balance accuracy over a broad frequency range is one of the major goals of this work.

On the other hand, based on the architecture shown in Fig. 1.2, the front-end amplifier block has to satisfy several other requirements as well, which make the design further challenging. Generally speaking, we need to retrieve information from all the channels. Every specification must be satisfied within the entire bandwidth. Signals coming from antennas are very weak; their magnitude can be as low as –80dBm (27μV for 75Ω TV

systems). Therefore, signal amplification is needed for the following stages. The signals received need to be processed to satisfy certain signal-noise ratio (SNR) so that they can be properly detected. Hence it is important to reduce the noise that is produced by the circuit. For a cascade of building blocks, the noise figure and the gain of the low noise amplifier (LNA) are two of the most important factors for the entire signal chain. This is especially true when the next stage is a down-converter with many passive components which introduce a significant amount of noise. In order to maximize the power transfer, good impedance matching over the entire signal band is required. At the output of the front-end amplifier, the capability of driving small load impedance is needed as well. Even more, reasonable power consumption is a major requirement.

1.4 Previous Work

As mentioned before, single-to-differential conversion is realized by external passive components in most traditional RF applications. The only solution reported [9] to improve the balance accuracy of on-chip single-to-differential conversion is designed and fabricated in a GaAs MESFET process. It employs an RLC feedback balancing circuit with external tuning to optimize the balance accuracy of the output signals at two frequencies respectively for dual-band communication applications. This solution is not compatible with CMOS technology. The RLC feedback method, especially the on-chip inductance, is not suitable for the low frequency end of the TV band, which is only 50MHz.

1.5 Organization of Thesis

The chapters are organized as follows:

In Chapter II, a novel single-to-differential signal conversion, the main contribution of this work, is presented. The conventional single-to-differential converter is analyzed and the imbalance problems are further discussed. A novel method is proposed to overcome the inherent limitations exhibited by the traditional circuit. An additional stage is added to improve the balance accuracy, reduce the effect of process variations, and drive the heavy load of the following passive poly-phase filter. Chapter III addresses the design of the three-stage cascaded front-end amplifier for the DTV tuner. The broadband low noise amplifier serves as the first stage, followed by the improved single-to-differential converter and a fully differential buffer as the second and the third stage, respectively. Chapter IV presents the simulation and experimental results, which verify the performances of the new method proposed for the phase splitter amplifier. Conclusions are given in Chapter V.

CHAPTER II

SINGLE-TO-DIFFERENTIAL SIGNAL CONVERSION

Single-to-differential converters are basic cells required in RF circuits, such as balanced mixers, multipliers, and phase shifters. An ideal single-to-differential converter generates a pair of differential output signals from a single input, which have balanced amplitude and phase space (equal gain and 180° phase difference). In practical analog circuits, there are always some inherent non-ideal factors that limit their accuracy. In this chapter, the major factors which cause the imbalance problem in traditional single-to-differential circuit are investigated. A novel compensation method is proposed to improve the balance accuracy of the differential signals. With an additional fully differential stage, the magnitude and phase error are further suppressed. This stage works as a buffer which is used to drive heavy loads as well. Circuit examples are designed and simulated to verify the performance of the proposed solution.

2.1 Traditional Solution

The simplest single-to-differential converter, which is also capable of providing substantial voltage gain, is made up of a differential stage with one of the two inputs grounded. Fig. 2.1 illustrates the traditional solution with load impedance and bias current.

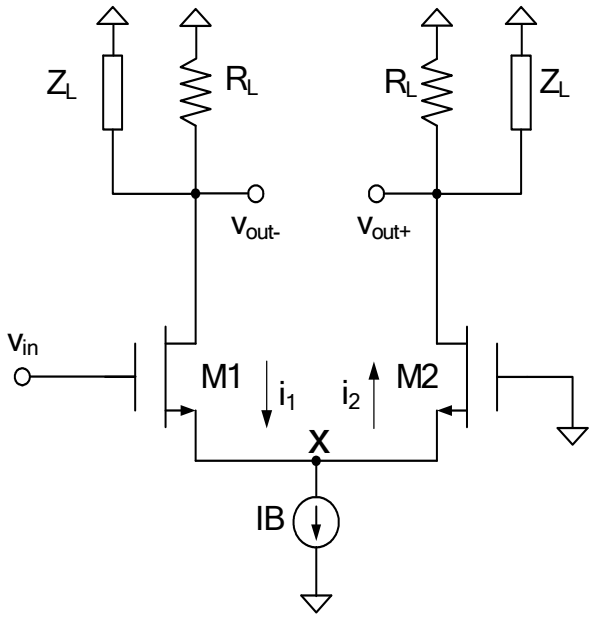


Fig. 2.1 Differential Amplifier With Inherent Single-to-Differential Conversion.

If the bias current source (IB) is an ideal current source with infinite output impedance, and the parasitic capacitances are neglected, the current generated by the input voltage signal v_{in} at the gate of M1 will flow through the two symmetric branches with the same magnitude and in an inverse direction. In other words, assuming that the two branches are identical (there are no mismatches between them) and that the parasitic capacitors are neglected, we will have $V_X = \frac{V_{in}}{2}$ when only a small signal is considered.

So the load currents can be expressed as $i_1 = g_m v_{gs1} = g_m \frac{v_{in}}{2}$, $i_2 = g_m v_{gs2} = -g_m \frac{v_{in}}{2}$.

Here g_m is the trans-conductance of the main transistor M1/M2, $v_{gs1,2}$ is the gate-source voltage of M1/M2. With the same load, the balanced differential output voltages are generated.

2.2 The Imbalance Problem

However, components in analog circuits are not ideal in practice. The bias current source is usually implemented by an active device. Considering the effects of the non-ideal current source and parasitic capacitors, the differential signal is not accurately balanced. The major non-ideal factors in traditional single-to-differential converter are shown below in Fig. 2.2.

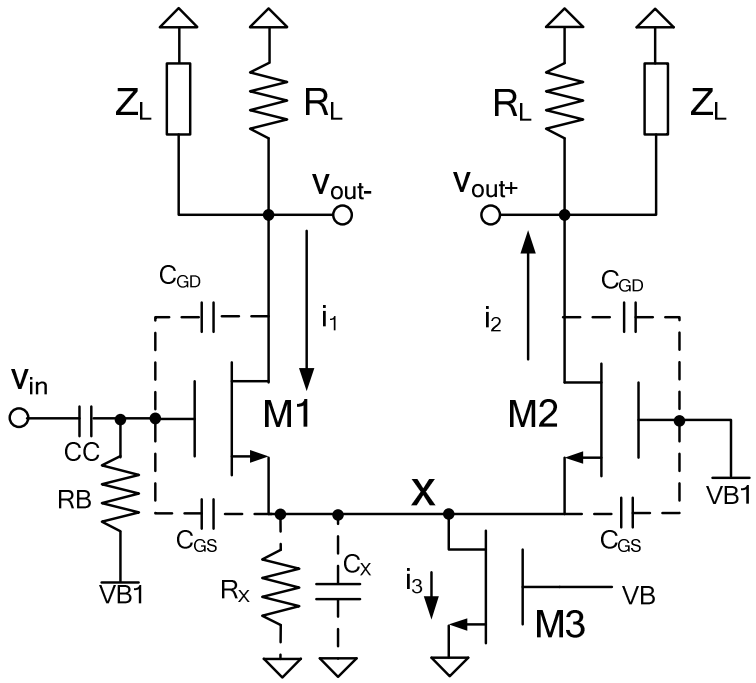


Fig. 2.2 Differential Amplifier With Non-Ideal Current Source & Parasitic Capacitances.

Using transistor M3 as the current source, the resistance R_X, which is the output resistance of the transistor M3, is not infinite at common-source node (node X). Also, there are parasitic capacitors at the common-source node. It can be modeled as the

capacitance C_X , which mainly consists of the source-to-substrate capacitance of M1/M2, the drain-to-bulk capacitance of M3, and other small parasitic capacitors associated with common-source node. In addition, the gate-to-drain capacitors of the differential pair transistors M1 and M2 also create slight errors.

To gain more insight into the performance of this circuit, the small signal model of the conventional single-to-differential converter with non-ideal current source and parasitic capacitances is shown in Fig. 2.3.

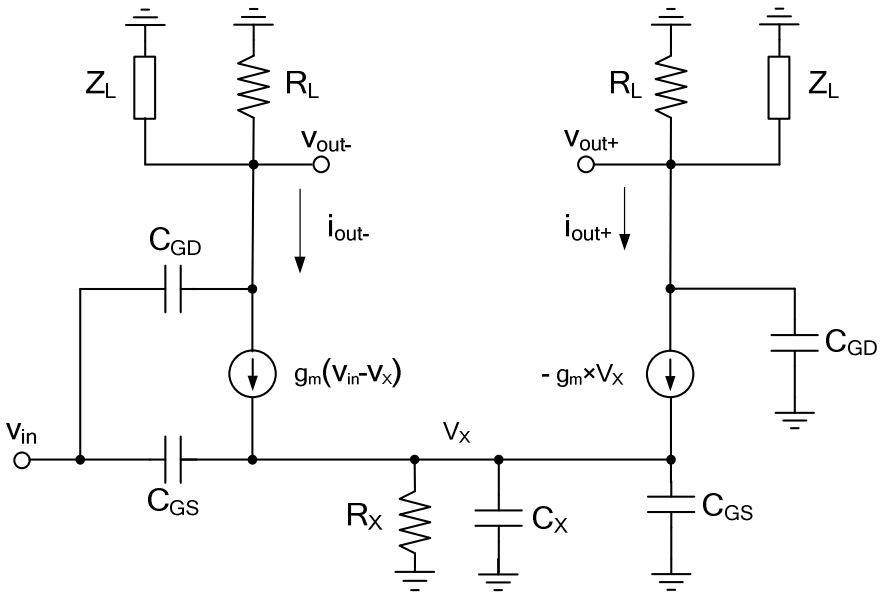


Fig. 2.3 Small Signal Model of Conventional Single-to-Differential Converter.

To simplify the analysis, the imbalance effects are split into two parts according to their different contributors. One part is due to the parasitic capacitors at the common-source

node and the finite resistance of current source. The other part is due to the gate-to-drain capacitors of the differential pair. These effects are analyzed separately in the following section.

2.2.1 Errors Due to Parasitic Capacitors and Finite Resistance at the Common-Source Node

Assuming that the circuit is symmetric and neglecting transistor mismatches, if the gate-to-drain capacitors are not taken into account, by using typical circuit analysis techniques, the output currents can be obtained as follows

$$v_{out-} = -\frac{g_m}{2}\frac{\left(1+\frac{g_X}{g_m}\right)\left(1+s\frac{C_{GS}+C_X}{g_m+g_X}\right)}{\left(1+\frac{g_X}{2g_m}\right)\left(1+s\frac{C_X+2C_{GS}}{g_X+2g_m}\right)\left(g_L+\frac{1}{Z_L}\right)}\cdot v_{in} \qquad (2\text{-}1)$$

$$v_{out+} = \frac{g_m}{2}\frac{\left(1+s\frac{C_{GS}}{g_m}\right)}{\left(1+\frac{g_X}{2g_m}\right)\left(1+s\frac{C_X+2C_{GS}}{g_X+2g_m}\right)\left(g_L+\frac{1}{Z_L}\right)}\cdot v_{in} \qquad (2\text{-}2)$$

Comparing equations (2-1) and (2-2), it is seen that there are two mismatches between the differential output voltages. One is the mismatch on the low frequency magnitude; the other is the difference in the locations of the zeros.

At low frequency, the magnitude error is mainly determined by the ratio of the finite output resistance of the current source over the trans-conductance of the differential pair. By increasing the transistor length, which correspondingly decreases the short channel

effects, the output resistance of current source can be managed to be large enough. If $\frac{g_X}{g_m} << 1$, the low frequency imbalance problem caused by this factor can be minimized.

If the low frequency error is ignored, equation (2-1) and (2-2) can be expressed as

$$v_{out-} = -\frac{g_m}{2} \frac{\left(1 + s\frac{C_{GS} + C_X}{g_m}\right)}{\left(1 + s\frac{C_X + 2C_{GS}}{2g_m}\right)\left(g_L + \frac{1}{Z_L}\right)} \cdot v_{in} \qquad (2\text{-}3)$$

$$v_{out+} = \frac{g_m}{2} \frac{\left(1 + s\frac{C_{GS}}{g_m}\right)}{\left(1 + s\frac{C_X + 2C_{GS}}{2g_m}\right)\left(g_L + \frac{1}{Z_L}\right)} \cdot v_{in} \qquad (2\text{-}4)$$

Comparing equation (2-3) and (2-4), the parasitic capacitor at common-source node shifts the zero of the inverting output to a lower frequency than does that of the non-inverting output. It creates phase and magnitude errors at the medium and high frequency ranges.

The phase error due to C_X can be expressed as

$$\Delta\phi = \phi_{out+} - \phi_{out-} - 180° = \phi\left(\frac{v_{out+}}{v_{out-}}\right) - 180°$$

$$= \arctan\left(\frac{\omega(C_{GS} + C_X)}{g_m}\right) - \arctan\left(\frac{\omega C_{GS}}{g_m}\right) \qquad (2\text{-}5)$$

In the DTV signal band (50M~850MHz), with proper design, $\frac{\omega(C_{GS}+C_X)}{g_m} << 1$. For very small values of x, $\arctan(x) = x$ is a very good approximation. The phase error can be approximated by

$$\Delta\phi \approx \frac{\omega(C_{GS}+C_X)}{g_m} - \frac{\omega C_{GS}}{g_m} = \frac{\omega C_X}{g_m} \qquad (2\text{-}6)$$

This phase error is determined by the trans-conductance of M1/M2 and parasitic capacitance at common-source node. It increases linearly with frequency for low and intermediate frequency band.

In addition, the parasitic capacitors at the common-source node create a pole present at both branches, which reduces the amplifier's bandwidth.

From the transfer functions (2-3) and (2-4), the magnitude error due to the zero mismatch can be expressed as (the magnitude of x is denoted by $|x|$)

$$\Delta v = |v_{out+}| - |v_{out-}|$$

$$= \frac{g_m}{2} \cdot |Z_L + R_L| \cdot |v_{in}| \cdot \frac{1}{\left|1 + s\frac{C_X + 2C_{GS}}{2g_m}\right|} \cdot \left(\sqrt{1 + \frac{\omega^2 (C_{GS}+C_X)^2}{{g_m}^2}} - \sqrt{1 + \frac{\omega^2 {C_{GS}}^2}{{g_m}^2}} \right)$$

By using Taylor series expansion and taking the first two terms, we get

$$\Delta v \cong \frac{g_m}{2} \cdot |Z_L + R_L| \cdot |v_{in}| \cdot \frac{1}{\left|1 + s\frac{C_X + 2C_{GS}}{2g_m}\right|} \cdot \frac{\omega^2 C_X (C_X + 2C_{GS})}{2{g_m}^2} \qquad (2\text{-}7)$$

Here, the average magnitude of the differential output voltages is $\frac{g_m}{2}\cdot|Z_L+R_L|\cdot|v_{in}|$. In the DTV signal band (50M~850MHz), with proper design, the high frequency errors are further reduced if $\omega^2 C_X(C_X+2C_{GS}) << 2{g_m}^2$.

2.2.2 The Effect of Gate-to-Drain Capacitors

From Fig. 2.3, the gate-to-drain capacitance of M1 creates a feed forward path from input to the inverting output, whereas the gate-to-drain capacitance of M2 is added to the non-inverting output directly. This introduces imbalance between the two amplifier's output voltages.

For the imbalance caused by the gate-to-drain parasitic capacitance of the differential pair, if other non-ideal factors are not considered (assuming C_X=0, C_{GS}=0, $g_X = 0$), the output voltages are

$$v_{out-} = -\frac{\frac{g_m}{2} - sC_{GD}}{g_L + \frac{1}{Z_L} + sC_{GD}} v_{in} \tag{2-8}$$

$$v_{out+} = \frac{\frac{g_m}{2}}{g_L + \frac{1}{Z_L} + sC_{GD}} v_{in} \tag{2-9}$$

Comparing equations (2-8) and (2-9), a zero is introduced at the inverting output voltage, but not in the non-inverting output voltage. The phase error due to gate-to-drain parasitic capacitance is approximated by

$$\Delta\phi = \arctan\left(\frac{2\omega C_{GD}}{g_m}\right) \approx \frac{2\omega C_{GD}}{g_m} \qquad (2\text{-}10)$$

As expected, the phase error due to the gate-to-drain parasitic capacitors increases with frequency. It is also determined by the trans-conductance of M1/M2, which is under the control of the bias current and transistor size. On the other hand, the gate-to-drain parasitic capacitors add additional load capacitance that reduces the bandwidth.

Compared to the parasitic capacitance at the common-source node C_X, the gate-to-drain capacitance C_{GD} is much smaller ($C_{GD} << C_X$). Simulation result shows that for a design example, the phase error due to C_{GD} is only 1.3° at 850MHz, while the total phase error is 16°, including the error due to C_X and C_{GD}.

The magnitude error due to gate-to-drain parasitic capacitance is

$$\Delta v = |v_{out+}| - |v_{out-}|$$

$$= \frac{g_m}{2} \cdot |Z_L + R_L| \cdot |v_{in}| \cdot \frac{1}{\left|1 + s\frac{C_{GD}}{2g_m}\right|} \cdot \left(\sqrt{1 + \frac{\omega^2 C_{GD}^{\ 2}}{g_m^{\ 2}}} - 1\right)$$

By using Taylor series expansion and taking the first two terms, we get

$$\Delta v \cong \frac{g_m}{2} \cdot \left|Z_L + R_L\right| \cdot \left|v_{in}\right| \cdot \frac{1}{\left|1 + s\frac{C_{GD}}{2g_m}\right|} \frac{\omega^2 C_{GD}{}^2}{2g_m{}^2} \qquad (2\text{-}11)$$

The nominal magnitude error due to C_{GD} is very small, since $\omega^2 C_{GD}{}^2 << 2g_m{}^2$ in the DTV signal band.

In order to get an idea about how large the mismatches could be, a conventional single-to-differential converter shown in Fig. 2.4 is designed with 3dB differential gain, driving 250fF capacitors on both sides. The 250fF capacitor load is an estimation of the input capacitance of the next stage (e.g., a buffer).

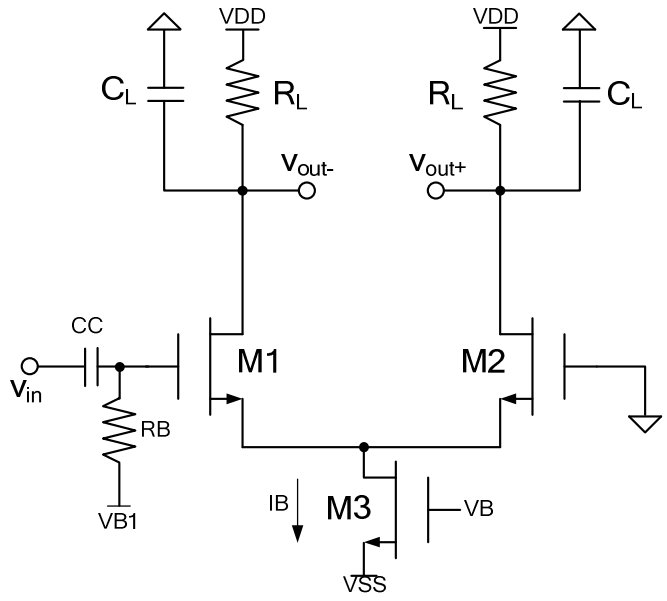


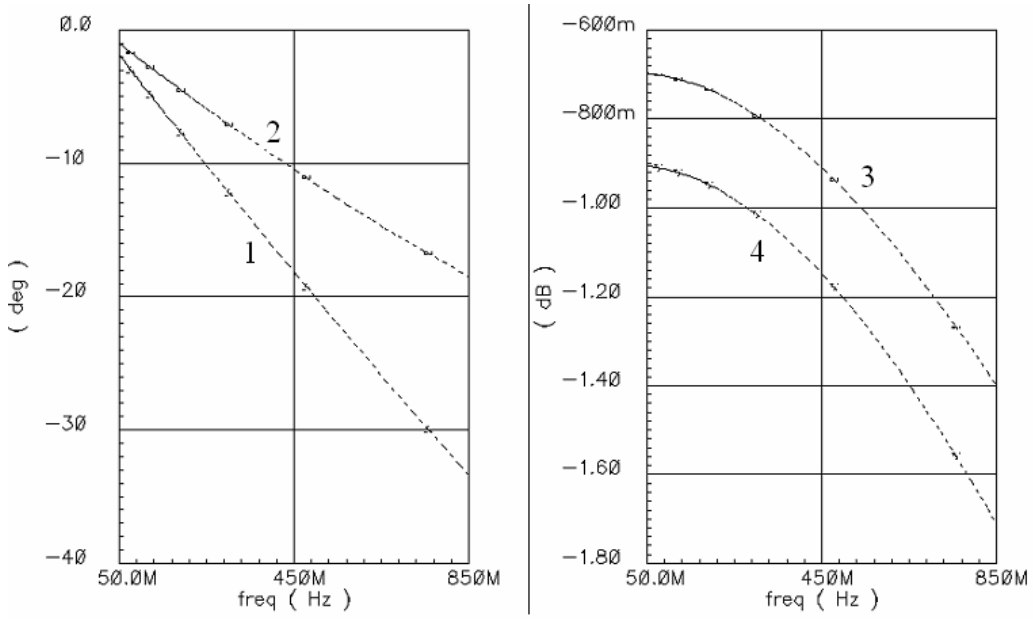
Fig. 2.4 Traditional Single-to-Differential Converter.

The load impedance is chosen to be 200 Ω based on the bandwidth requirement. Then with the gain specification, the trans-conductance of M1/M2 is calculated as 10mA/V. Together with the selected 300mV effective voltage (V_{DSAT}) required for linearity, the bias current and transistor sizes are obtained. To connect with the previous single end stage and provide proper bias, a coupling capacitor CC of 10pF and bias resistor RB of 100kΩ are used at the input node. The component parameters are listed in Table 2.1.

Table 2.1 The Circuit Parameters of the Traditional Single-to-Differential Converter.

Components	Parameters
M1, M2	72μm/0.4μm
M3	288μm /0.8μm
C_L	250pF
RB	100KΩ
VB1	1.0 V
IB	5.6 mA

To demonstrate the errors of phase and magnitude between the differential output voltages, AC frequency response over the signal band of 50M~850MHz is obtained using Cadence Spectre simulation tools. Fig.2.5 illustrates the simulation results of the phase and magnitude of the differential output voltages. Fig.2.5(a) is the phase of the output voltages in degrees (the 180 degree offset is subtracted beforehand for better illustration), and Fig.2.5(b) is the magnitude of the output voltages in dB.



Curve 1: Phase of non-inverting output

Curve 2: Phase of inverting output minus 180^{o}

(a)

Curve 3: Magnitude of inverting output

Curve 4: Magnitude of non-inverting output

(b)

Fig.2.5. Output Voltages in Conventional Single-to-Differential Converter.

(a) Phase (in degree) of output voltages

(b) Magnitude (in dB) of output voltages

As shown in Fig. 2.5(a), the phase of the non-inverting output voltage (Curve 1) drops faster than the inverting one with 180° shift (Curve 2) does, which makes the phase error increase up to 16° at 850MHz. That is because the zero in the inverting output transfer function is located at relatively a lower frequency than that in the non-inverting one.

The magnitude of the non-inverting output voltage is smaller than that of the inverting one due to the signal leakage at the common-source node. The magnitude error is less than 0.2 dB at 50 MHz, and increases to 0.3dB at 850 MHz.

Based on our phase and magnitude error requirements, it is essential to suppress those errors with some circuit techniques, especially the phase error.

2.3 Novel Balancing Method

To overcome the inherent shortcomings in the traditional single-to-differential converter, a novel compensation method is proposed based on the investigation done in the previous section. Since the cause for the error is the zero of inverting output voltage transfer function is at relatively low frequency, the circuit technique that shifts the zero of the non-inverting output voltage to lower frequency is considered to compensate this effect. For simplicity of analysis, only the dominant factor causing the phase errors, i.e., the parasitic capacitance at the common-source node (C_X), is taken into consideration in the following analysis.

2.3.1 Step One: Adding A Bypass Capacitor

To compensate the effect of the lower frequency zero in the inverting output voltage, a bypass capacitor that produces a feed forward signal path between the input node and the non-inverting output node is employed. It is used to shift the zero of non-inverting output voltage to a lower frequency. The single-to-differential converter with bypass capacitor CF is shown in Fig. 2.6.

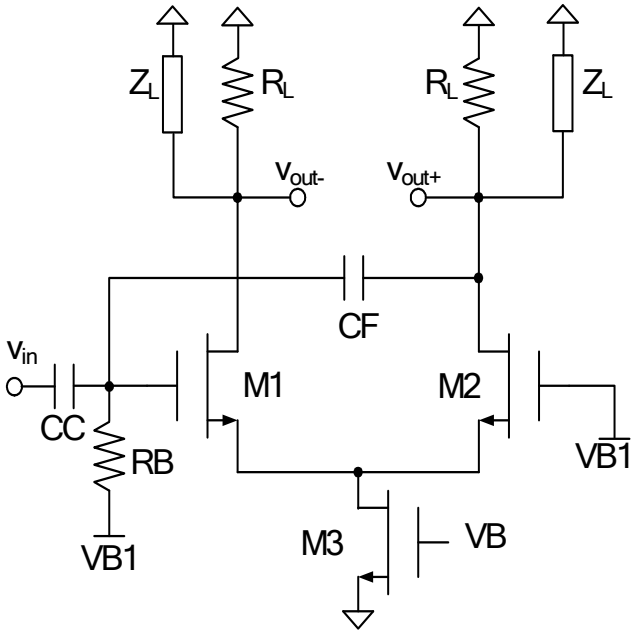


Fig. 2.6 Single-to-Differential Converter With Bypass Capacitor.

By employing the typical circuit analysis techniques, the output voltages can be obtained from the small signal model equivalent circuit as follows,

$$v_{out-} = -\frac{g_m}{2}\frac{\left(1+s\frac{C_{GS}+C_X}{g_m}\right)}{\left(1+s\frac{C_X+2C_{GS}}{2g_m}\right)\left(g_L+\frac{1}{Z_L}\right)}\cdot v_{in} \tag{2-12}$$

$$v_{out+} = \frac{\frac{g_m}{2}\left(s^2\frac{CF(2C_{GS}+C_X)}{g_m{}^2}+1+s\frac{(2CF+C_{GS})}{g_m}\right)}{\left(1+s\frac{C_X+2C_{GS}}{2g_m}\right)\left(g_L+\frac{1}{Z_L}+sCF\right)}v_{in} \tag{2-13}$$

The second-order term in the numerator of equation (2-13) adds very small phase and magnitude error in DTV frequency range and thus can be neglected. Then the non-inverting output voltage can be expressed as

$$v_{out+} = \frac{\frac{g_m}{2}\left(1 + s\frac{(2CF + C_{GS})}{g_m}\right)}{\left(1 + s\frac{C_X + 2C_{GS}}{2g_m}\right)\left(g_L + \frac{1}{Z_L} + sCF\right)} v_{in} \qquad (2\text{-}14)$$

Comparing equation (2-12) and (2-14), if bypass capacitance CF is selected to be $\frac{1}{2}C_X$, the bypass capacitance will shift the zero of non-inverting output voltage to the frequency exactly the same as that of the inverting one. However, it can be seen from equation (2-14) that the bypass capacitance will also shift the pole of the non-inverting voltage to a lower frequency. This introduces additional phase and magnitude errors. Circuit techniques that can compensate this error will be considered in the following section.

2.3.2 Step Two: Adding A Load Balance Capacitor

To eliminate the additional error introduced by the bypass capacitor, a load balance capacitor CB at the inverting output node is employed. It can shift the pole at the inverting output voltage to a lower frequency and fully balance the circuit. The complete circuit with both load balance capacitor and bypass capacitor is illustrated in Fig. 2.7.

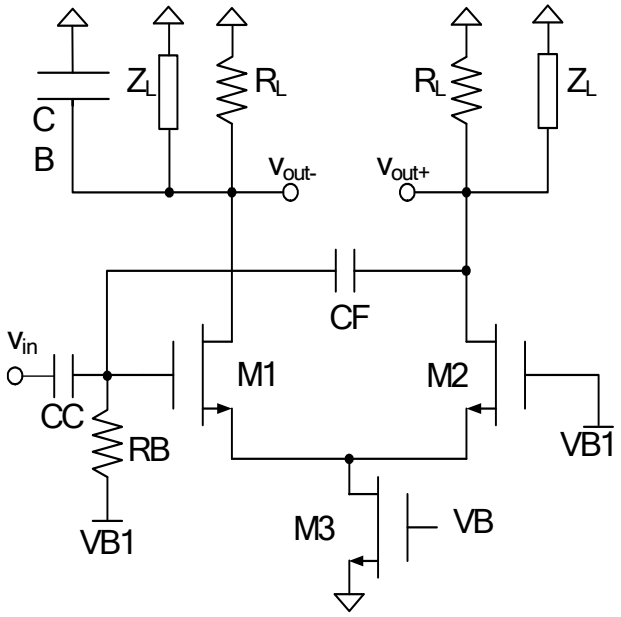


Fig. 2.7 Single-to-Differential Converter With Bypass and Load Balancing Capacitor.

For the fully balanced circuit, the output voltages can be obtained from the small signal model equivalent circuit shown in Fig. 2.6 as follows,

$$v_{out-} = -\frac{g_m}{2}\frac{\left(1+s\frac{C_{GS}+C_X}{g_m}\right)}{\left(1+s\frac{C_X+2C_{GS}}{2g_m}\right)\left(g_L+\frac{1}{Z_L}+sCB\right)}\cdot v_{in} \tag{2-15}$$

$$v_{out+} = \frac{\frac{g_m}{2}\left(1+s\frac{(2CF+C_{GS})}{g_m}\right)}{\left(1+s\frac{C_X+2C_{GS}}{2g_m}\right)\left(g_L+\frac{1}{Z_L}+sCF\right)}v_{in} \tag{2-16}$$

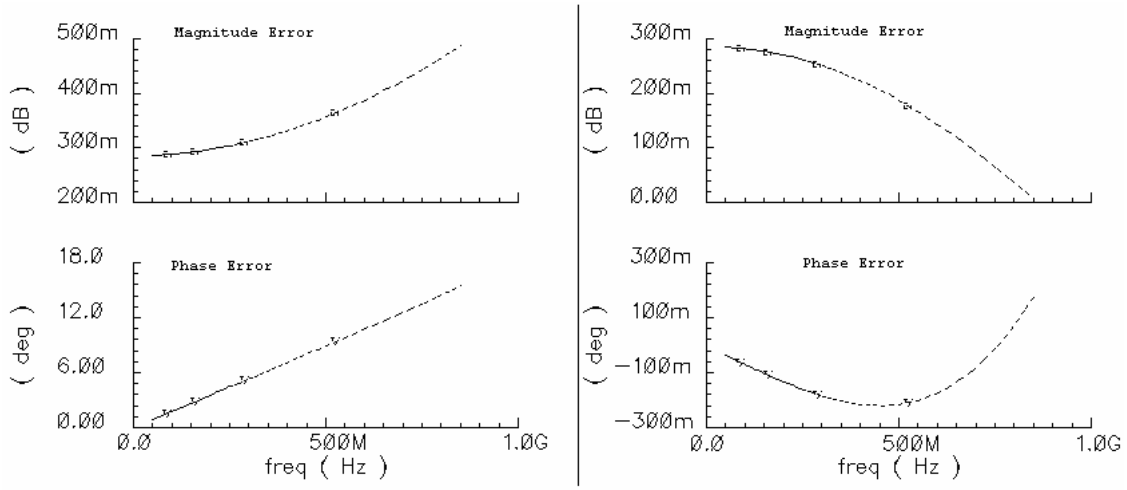
Comparing equation (2-15) and (2-16), if $CB = CF = \frac{1}{2}C_X$, in a first approximation, the output voltages are fully balanced with the same magnitude and 180° phase difference.

In practical design, the value of the compensation capacitance can be finely adjusted to compensate the error due to other non-dominant factors. For the low frequency magnitude error, without any compensation, the inverting output voltage is higher than the non-inverting one due to current leakage though the output resistance of current source R_X. This can be compensated in the medium frequency range by slightly increasing the load balance capacitance CB. It shifts the pole of the inverting output voltage to a lower frequency and degrades the magnitude of the inverting output voltage faster. For the error introduced by the gate-to-drain capacitance, the zero shifting in the inverting output voltage can be compensated by the pole shift as well, which is carried out by increasing the load balance capacitance.

This novel compensation method features simplicity and excellent accuracy improvement. It does not change the bias conditions of the traditional circuit and no additional power is consumed.

In order to demonstrate the performance improvement of the novel compensation method, a single-to-differential converter with compensation capacitors as shown in Fig. 2.7 is designed and simulated. All the circuit parameters except the compensation capacitors CF and CB remain the same as the previous ones given in Table 2.1. The parasitic capacitance at the common-source node C_X is obtained from the simulations of

the circuit in Cadence Spectre tools. It is the sum of the parasitic capacitance at the source of the differential pair M1/M2 and at the drain of the current source M3, $C_X = C_{SS,M1} + C_{SS,M2} + C_{DD,M3} \cong 188\,fF$. CF and CB are calculated as $CF = CB = \frac{1}{2} C_X = 99\,fF$. After fine tuning, CB is adjusted to 118fF. For sake of comparison, magnitude error and phase error before and after compensation are obtained from AC response over the whole 50M~850MHz range. The simulation results are shown in Fig. 2.8.



(a) Errors without compensation (b) Errors with bypass and load capacitor

Fig. 2.8 Error Cancellation Results With Bypass and Load Balancing Techniques.

In Fig. 2.8, the magnitude error in dB is defined as $MagError = dB20\left(|v_{out-}| - |v_{out+}|\right)$ and the phase error in degree is presented as $PhaseError = Phase(v_{out+}) - Phase(v_{out-}) + 180^{\circ}$

Fig. 2.8(a) illustrates the errors before compensation, and Fig. 2.8(b) illustrates the errors after compensation.

With compensation, the maximum magnitude error is reduced from 0.5dB to 0.3dB, the maximum phase error is reduced from 16° to 0.3°.The simulation results verify that the novel compensation methods can achieve excellent phase accuracy. Both phase and magnitude errors are reduced significantly.

Table 2.2 summarizes the comparison of the simulation results before and after compensation.

Table 2.2 Error Comparison Before and After Compensation.

	Before compensation	After compensation
Magnitude Error (dB)	0.3~0.5 dB	<0.3 dB
Phase Error (Deg)	16°	<±0.3°

2.4 The Benefits of Adding Another Differential Stage

Though the proposed compensation method can significantly improve the accuracy of the differential signals, the parameters process variations and transistor mismatches should be taken into consideration as well. In this section, it is shown that using an additional fully differential stage can further suppress the mismatches and increase the tolerance of the process variations.

The two output signals of the single-to-differential signal converter can be expressed as $v_{01} = A_1 e^{j\phi_1}$ and $v_{02} = A_2 e^{j\phi_2 + 180^\circ}$.

If they are ideal differential signals, we will have $A_1=A_2$ and $\Phi_1=\Phi_2$. If mismatches are presented, the magnitude error is defined as $\Delta A = |A_1 - A_2|$, and the phase error is defined as $\Delta\phi = \phi_1 - \phi_2$. The average amplitude can be expressed as $A = (A_1 + A_2)/2$ and the average phase can be expressed as $\phi = (\phi_1 + \phi_2)/2$. The output signals v_{o1} and v_{o2} can always be expressed as the combination of differential and common mode components.

The differential component is presented as

$$
\begin{aligned}
&v_{01} - v_{02} = A_1 e^{j\phi_1} - A_2 e^{j\phi_2 + 180^\circ} = A_1 e^{j\phi_1} + A_2 e^{j\phi_2} \\
&= \frac{A_1 - A_2 + A_1 + A_2}{2} e^{j\phi_1} + \frac{A_2 - A_1 + A_1 + A_2}{2} e^{j\phi_2} \\
&= \frac{A_1 + A_2}{2}\left(e^{j\phi_1} + e^{j\phi_2}\right) + \frac{A_1 - A_2}{2}\left(e^{j\phi_1} - e^{j\phi_2}\right) \\
&\cong \frac{A_1 + A_2}{2} e^{j\phi}\left(e^{j\Delta\phi/2} + e^{-j\Delta\phi/2}\right) + \frac{\Delta A}{2}\cdot e^{j\phi}\left(e^{j\Delta\phi/2} - e^{-j\Delta\phi/2}\right)
\end{aligned}
$$

Using Taylor series expansion and taking the first three terms only, we get

$$
\begin{aligned}
v_{01} - v_{02} &\cong A e^{j\phi}\left(1 + j\Delta\phi/2 - \Delta\phi^2/8 + 1 - j\Delta\phi/2 - \Delta\phi^2/8\right) + \frac{\Delta A}{2}\cdot e^{j\phi}\cdot j\Delta\phi \\
&= 2Ae^{j\phi} - Ae^{j\phi}\Delta\phi^2/4 + \frac{\Delta A}{2}\cdot e^{j\phi}\cdot j\Delta\phi \qquad \text{(2-17)}
\end{aligned}
$$

From equation (2-17), it can be seen that the first term is the ideal differential signal. The 2nd and 3rd terms cause errors in the differential signal due to phase and magnitude mismatches, respectively. Both of them are 2nd order terms and usually they are quite small.

The common mode component is

$$\begin{aligned} v_{01} + v_{02} &= A_1 e^{j\phi_1} + A_2 e^{j\phi_2 + 180^\circ} = A_1 e^{j\phi_1} - A_2 e^{j\phi_2} \\ &= \frac{A_1 - A_2 + A_1 + A_2}{2} e^{j\phi_1} - \frac{A_2 - A_1 + A_1 + A_2}{2} e^{j\phi_2} \\ &= \frac{A_1 + A_2}{2}\left(e^{j\phi_1} - e^{j\phi_2}\right) + \frac{A_1 - A_2}{2}\left(e^{j\phi_1} + e^{j\phi_2}\right) \\ &\cong \frac{A_1 + A_2}{2} e^{j\phi}\, j\Delta\phi + \frac{\Delta A}{2} e^{j\phi}\left(e^{j\Delta\phi/2} + e^{-j\Delta\phi/2}\right) \end{aligned}$$

By using Taylor series expansion and taking the first two terms, we get

$$\begin{aligned} v_{01} + v_{02} &\cong A e^{j\phi} \cdot j\Delta\phi + \frac{\Delta A}{2} e^{j\phi}\left(2 - \Delta\phi^2/4\right) \\ &\cong A e^{j\phi} \cdot j\Delta\phi + \Delta A e^{j\phi} - \Delta A e^{j\phi}\Delta\phi^2/8 \end{aligned} \qquad (2\text{-}18)$$

Compared to the second order differential mode error, the common mode error dominates since it has two first order terms. Fortunately, the main property of fully differential amplifiers is to reject the common-mode signals. This means that the dominant error in the output signal of the single-to-differential converter can be further suppressed by the fully differential buffer.

On the other hand, for the single conversion DTV tuner, the front-end amplifier is expected to drive a poly-phase quadrature signal generator. The poly phase filter consists

of passive networks. The fully differential buffer is used not only to reduce the common mode error signals but also to drive the poly-phase filter.

Assuming that the fully differential amplifier shown in Fig. 2.9 is symmetric, and the current source M3 has finite output impedance, the common mode gain yields

$$A_{v,CM} = \frac{v_{out,CM}}{v_{in,CM}} = -\frac{\frac{g_m}{Y_L}}{1+\frac{2g_m}{Y_X}} \tag{2-19}$$

where Y_L is the total load admittance and $Y_X = g_{DS,M3} + sC_X$ is the admittance at common-source node.

And the differential gain is:

$$A_{v,DM} = \frac{g_m}{Y_L} \tag{2-20}$$

To evaluate the effect of common mode suppression, we use the common mode rejection ratio (CMRR) as the figure of merit [10]. CMRR is defined as the ratio of the differential and common mode gain, yielding

$$CMRR = \left|\frac{A_{v,DM}}{A_{V,CM}}\right| = 1+\frac{2g_m}{Y_X} \tag{2-21}$$

From equation (2-21), CMRR is determined by the trans-conductance of the differential pair and the overall impedance at the common-source node.

To demonstrate the performance improvement with an additional fully differential stage, a classic fully differential buffer is designed and simulated. The voltage gain is selected to be 0dB. The load is a 200Ω resistance and a 0.5pF capacitance connected in parallel. It is the simplified model of the poly-phase quadrature signal generator. The whole circuit is shown in Fig. 2.9.

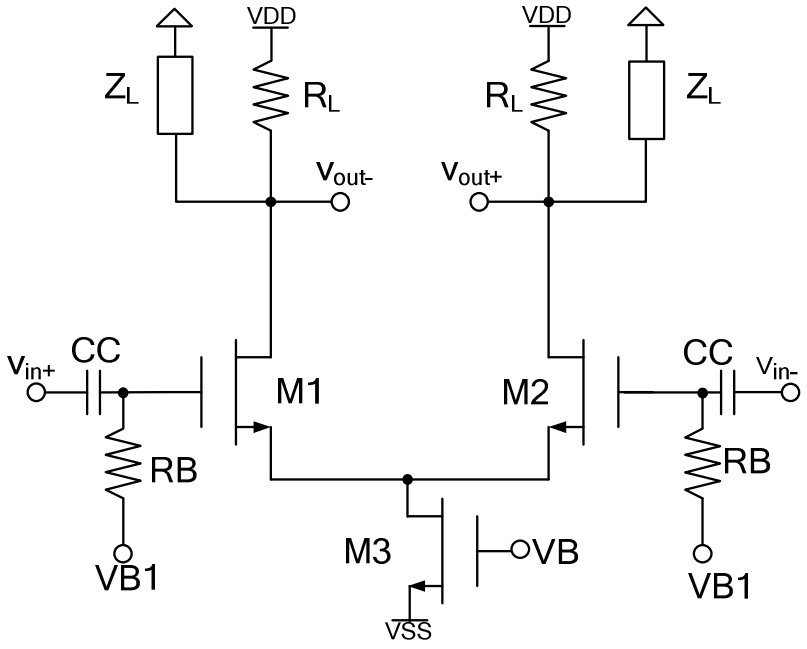


Fig. 2.9 Fully Differential Buffer.

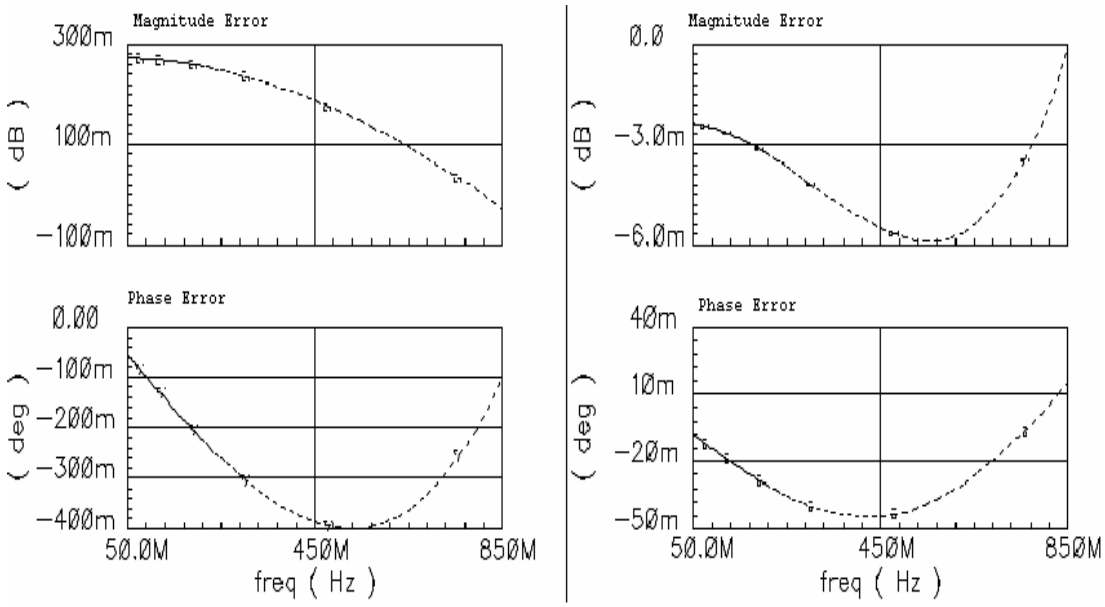
In order to drive the small impedance load, R_L is selected as 50 Ohm. Then from the gain requirement, the trans-conductance of the differential pair is calculated to be 20mA/V. Together with a 300mV effective voltage, the bias current and transistor sizes are obtained. To connect this topology with the previous single-to-differential converter

and provide proper bias, a coupling capacitor CC of 10pF and bias resistor RB of 100kΩ are used at the input nodes. For the sake of simplicity, the same bias voltages as the previous stage are used. The circuit parameters are listed in Table 2.3.

Table 2.3 Parameters of Fully Differential Buffer.

Components	Parameters
M4, M5	200μm/0.4μm
M6	600 μm /0.8 μm
CC	10 pF
RB	100 kΩ
R_L	50 Ω
VB1	1.2 V
IB	10.8 mA

To demonstrate the performance improvement, the fully differential buffer with load is connected with the single-to-differential converter previously discussed. The magnitude and phase error obtained before and after the differential buffer are compared in Fig. 2.10.



(a) Errors before differential buffer (b) Errors after differential buffer

Fig. 2.10 Errors Suppression With Differential Buffer.

Fig. 2.10(a) illustrates the errors before the fully differential buffer, and Fig. 2.7(b) illustrates the errors after the fully differential buffer. With the additional fully differential stage, the magnitude error is reduced from 0.3 dB to 0.006 dB, the phase error is reduced from 0.4° to 0.05°. Both magnitude and phase error are suppressed significantly and the differential output signal achieves excellent balancing accuracy after the buffer.

The errors before and after the differential buffer are summarized in Table 2.4.

Table 2.4 Error Comparison Before and After Differential Buffer.

	Before differential buffer	After differential buffer
Maximum Magnitude Error (dB)	0.3 dB	0.006 dB
Maximum Phase Error (Deg)	0.4	0.05

CHAPTER III

A CMOS BROADBAND FRONT-END AMPLIFIER FOR DTV TUNER

In this chapter, a three-stage front-end amplifier for DTV tuner is designed using TSMC 0.35μm CMOS processing technology. The design considerations for cascading three stages are presented. For the building block of the high performance broadband low noise amplifier, several circuit configurations are compared and the resistive shunt-feedback topology is chosen. The design procedure is presented based on the detailed circuit analysis. For the second stage, the accurate single-to-differential converter with novel compensation technique discussed in Chapter II is used. A classic fully differential buffer as the output stage is used to provide capability to drive heavy load and to further improve the balance of differential output signals.

3.1 The Specifications of the Front-end Amplifier

Considering the overall DTV tuner system requirements and technology limitations, the specifications for the broadband front-end amplifier are given in Table 3.1.

3.2 Design Considerations

For N cascade noisy stages as shown in Fig. 3.1, the total noise figure can be calculated with the following expression [11]

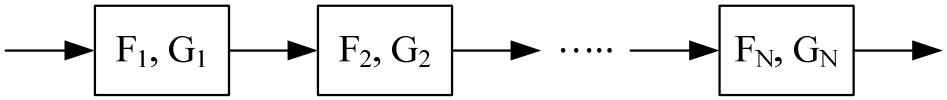


Fig. 3.1 Cascade Systems for Computation of Noise Figure.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \tag{3-1}$$

where G_i is the power gain of the *i*th stage and F_i is the noise factor of the *i*th stage.

Table 3.1 Target Specifications for Front-End Amplifier.

Power Supply	3.3 V
Input Impedance	75 Ω
Bandwidth	50MHz~850MHz
Gain	16 dB
Noise Figure (NF)	3 dB
S_{11}	-10 dB
Load resistance	200 Ω
Load capacitance	0.5 pF
Differential Phase error	±2º
Differential Magnitude	±1%

To achieve the critical specifications, a three-stage cascade architecture is used as shown in Fig. 3.2.

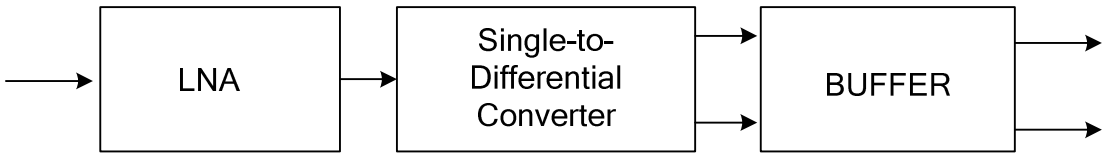


Fig. 3.2 Three-Stage Front-End Amplifier.

From equation (3-1), it can be seen that the noise of subsequent stages is less important due to the gain of the preceding stages. As a result, the first stage, the low-noise amplifier, should dominate the system's noise performance if it provides enough power gain.

The second stage is an active single-to-differential converter. Here the magnitude and phase compensation methods described in the previous chapter are used to improve the accuracy of the differential output signals.

The third stage is the output stage, which operates as a buffer to drive the low input impedance of the next stage. As mentioned in Chapter II, due to high common mode rejection ratio (CMRR), it can further improve the balancing of differential signals and suppress the effect of process variation and transistor mismatches.

3.3 Gain/Noise Budget Link

In the double-quadrature DTV tuner, noisy stages, such as the poly-phase filter implemented with passive RC networks, have losses (around -6dB) instead of amplification. This imposes better gain/noise performances for the front-end amplifier.

From equation (3-1), a number of solutions exist. After system simulations and evaluation of technology parameters, the gain/noise budget can be calculated for the cascade three-stage amplifier as shown in Table 3.2.

Table 3.2 Gain/Noise Budget Link.

	LNA	Converter	Buffer	Total
Gain	18dB	3dB	0dB	21dB
NF	2.8dB	8dB	6dB	3dB

3.4 Design of the CMOS Broadband LNA

In this section, a broadband low noise amplifier is designed to fulfill the requirements of high gain, low noise figure and broadband impedance matching.

3.4.1 Topology Selection

For broadband low noise amplifiers, the impedance matching requirement over the entire frequency range (50MHz~850MHz) has limited our choice of topologies. Applicable topologies are discussed here.

3.4.1.1 Common-Gate Topology

The simplified schematic of the common-gate topology is illustrated in Fig. 3.3.

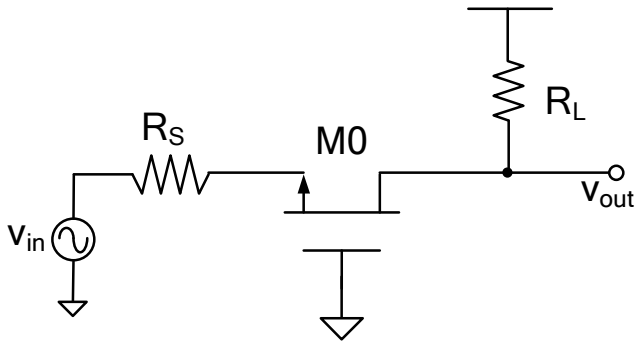


Fig. 3.3 Simplified Schematic of a Common-Gate Amplifier.

In this schematic, R_S is the source resistance and R_L is the load resistance. The major advantage of this topology is that it can achieve input impedance matching in the entire band by properly selecting the bias current and transistor size.

However, noise figure and gain are limited because the trans-conductance of the transistor is fixed approximately to 1/RS. Since $g_m \approx \frac{1}{R_S}$, noise figure is greater than 3dB for 75Ω, and the voltage gain is then limited to $R_L / 2R_S$. Unfortunately, R_L can not be increased further because the bandwidth decreases inversely proportional to R_L.

3.4.1.2 Common-Source Topology

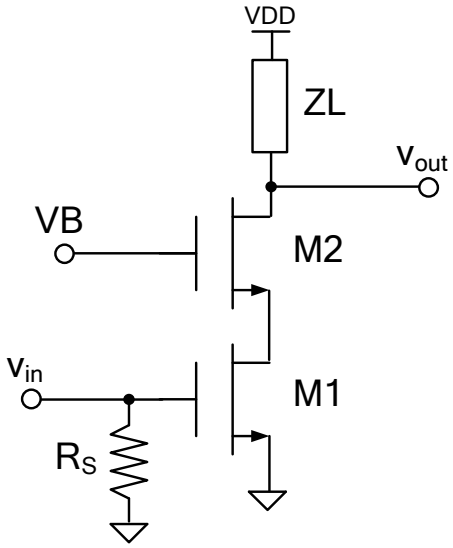


Fig. 3.4 Common-Source Amplifier With Resistive Termination.

Another topology that can be used is the common-source amplifier, which is the most popular configuration used in low noise narrow band applications. It can also be used for broadband applications. The most straightforward method for impedance matching is to add a termination resistor at the gate of the input transistor as shown in Fig. 3.4. The main drawback of this topology is its relatively large noise figure. The achievable noise figure is around 4-5 dB due to the noise contribution of terminal resistor R_S and the noise of the transistors.

3.4.1.3 Shunt-Feedback Topology

To improve the noise and linearity performances without compromising the gain and impedance matching, negative feedback can be used for the design of broadband amplifiers. Since it does not reduce the signal with a noisy attenuator before amplifying, the noise figure is expected to be substantially better than that of the topologies mentioned above. A simplified schematic is shown in Fig. 3.5. In this configuration, a shunt feedback resistor is connected between the gate and drain of the main transistor.

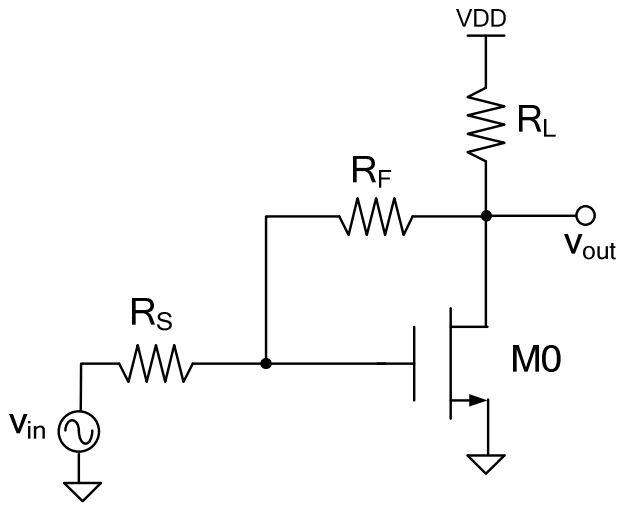


Fig. 3.5 Common-Source Amplifier With Shunt Resistive Feedback.

After comparing the topologies discussed above, the third topology (Shunt-Feedback topology) is selected for the broadband low noise amplifier. Detailed analysis of this

topology follows. It is verified through the analysis that the high gain, low noise and impedance matching requirements can all be satisfied.

3.4.2 Shunt Feedback Topology Circuit Analysis

3.4.2.1 Circuit Model and Transfer Function

To get an exact transfer function, all major parasitic capacitances are taken into consideration. The small signal model of the common-source amplifier with resistive feedback is shown in Fig. 3.6:

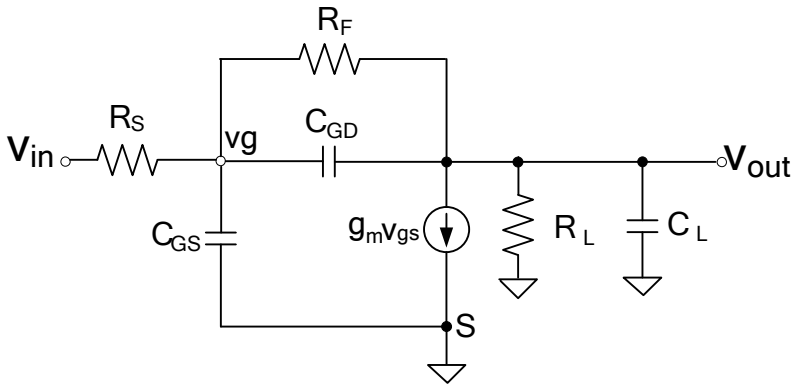


Fig. 3.6 Small Signal Equivalent Circuit for Shunt Resistive Feedback.

In Fig. 3.6, R_S is the source resistance whose corresponding admittance is $g_S = \frac{1}{R_S}$.

Based on Kirchoff's current law, we have

$$(v_g - v_{out})(g_F + sC_{GD}) = v_{out}(g_L + sC_L) + v_g \cdot g_m \quad (3\text{-}2)$$

$$(v_{in} - v_g)g_S = (v_g - v_{out})(g_F + sC_{GD}) + v_g \cdot sC_{GS} \quad (3\text{-}3)$$

where v_g is the signal voltage at the gate of the transistor. Solving these two equations, the overall transfer function is obtained as follows.

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{g_S(g_F - g_m + sC_{GD})}{a \cdot s^2 + b \cdot s + c} \quad (3\text{-}4)$$

Where

$a = C_{GS}C_{GD} + C_{GS}C_L + C_{GD}C_L$,

$b = C_{GD}(g_S + g_m + g_L) + C_{GS}(g_F + g_L) + C_L(g_S + g_F)$,

$c = g_F(g_S + g_m + g_L) + g_L g_S$.

3.4.2.2 Frequency response

From the output voltage transfer function (3-4), the low frequency voltage gain yields,

$$Av = \frac{v_{out}}{v_{in}} = \frac{g_S(g_F - g_m)}{g_F(g_S + g_m + g_L) + g_L g_S} = \frac{R_L(1 - g_m \cdot R_F)}{(R_F + R_S + R_L + g_m \cdot R_S \cdot R_L)} \quad (3\text{-}5)$$

It can be rewritten as

$$Av = -\frac{R_F}{R_S}\left(\frac{1-\frac{1}{g_m R_F}}{1+\frac{1}{g_m R_L}\left(1+\frac{R_F}{R_S}+\frac{R_L}{R_S}\right)}\right) \tag{3-6}$$

If a high input impedance circuit is driven, that is, $R_L >> R_F >> R_S$, and $g_m R_L >> 1$, $g_m R_F >> 1$, the low frequency gain is approximately

$$Av = \frac{v_{out}}{v_{in}} \cong -\left(\frac{R_F}{R_S}\right)\left(\frac{1}{1+\frac{1}{g_m R_S}}\right) \tag{3-7}$$

Though the denominator of the transfer function (3-4) appears complicated, it can yield the intuitive expressions for the two poles, ω_{p1} and ω_{p2}. Writing the denominator of the two poles system as

$$D(s) = \left(\frac{s}{\omega_{p1}}+1\right)\left(\frac{s}{\omega_{p1}}+1\right) = \frac{s^2}{\omega_{p1}\omega_{p1}} + s\left(\frac{1}{\omega_{p1}}+\frac{1}{\omega_{p2}}\right)+1 \tag{3-8}$$

If we assume that there is one pole ω_{p1} dominates [12], and another pole ω_{p2} is much farther from ω_{p1}, the coefficient of the first order term is approximately equal to $1/\omega_{p1}$. From the full transfer function (3-4), it follows that

$$\omega_{p1} \cong \frac{c}{b} = \frac{g_F(g_S+g_m+g_L)+g_L g_S}{C_{GD}(g_S+g_m+g_L)+C_{GS}(g_F+g_L)+C_L(g_S+g_F)} \tag{3-9}$$

If the system is designed such that $g_L << g_m$, $g_L << g_S$, and $g_m(R_F // R_L) >> 1$, the dominant pole can be approximated by

$$\omega_{p1} \cong \frac{g_F(g_S + g_m + g_L) + g_L g_S}{C_{GD}(g_S + g_m + g_L) + C_{GS}(g_F + g_L) + C_L(g_S + g_F)} \tag{3-10}$$

And the amplifier's -3dB bandwidth is determined by this dominant pole.

3.4.2.3 Impedance Matching

Ignoring the effects of the parasitic capacitors, the equivalent low frequency small signal model of the low noise amplifier is represented as Fig. 3.7.

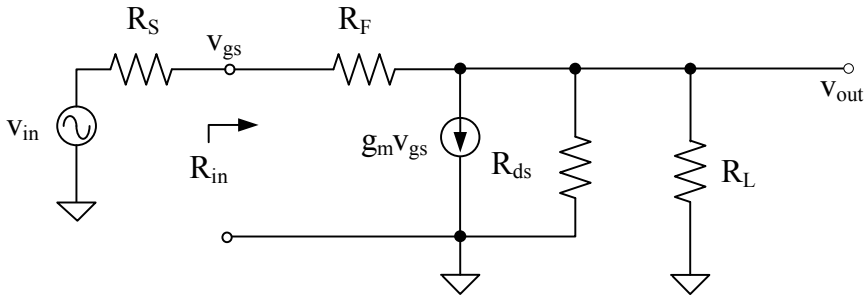


Fig. 3.7 Simplified Small Signal Circuit of Shunt Feedback Amplifier.

At low and medium frequencies, the input impedance R_{in} is obtained from Fig. 3.7 as

$$R_{in} = \frac{R_F}{1 - \dfrac{g_F - g_m}{g_F + g_{ds} + g_L}} \tag{3-11}$$

where g_m and $R_{ds} = \frac{1}{g_{ds}}$ are the small signal trans-conductance and output resistance of the transistor, respectively. If R_{ds} is much larger than R_L and R_F and $g_m >> g_F$. Then equation (3-11) can be expressed as follows.

$$R_{in} \cong \frac{R_F}{1+\frac{g_m}{g_F+g_L}} = \frac{R_F}{1+g_m(R_F \,//\, R_L)} = \frac{R_F}{1+g_m R_L\left(\frac{R_F}{R_F+R_L}\right)} \qquad (3\text{-}12)$$

For proper input impedance matching, we have to make $R_{in} = R_S$. Solving equations (3-7) and (3-12), the feedback resistance and g_m can be determined to get reasonable impedance matching and enough voltage gain at low frequencies.

3.4.2.4 Noise Performance of Shunt Amplifier

- Noise Figure

The noise performance of an RF amplifier is represented by its noise factor or noise figure (expressed in dB). It is defined as the signal to noise ratio (SNR) at the input stage of the network divided by the SNR at the output stage of the network [8]:

$$F = \frac{SNR_{in}}{SNR_{out}} \qquad (3\text{-}13)$$

For RF amplifiers, all noise sources can be referred to the input source. Therefore, the noise factor can be represented as [8]:

$$F = \frac{Total\ input\ referred\ noise}{Noise\ of\ \ source\ resistor} \qquad (3\text{-}14)$$

- Noise model

The noise model for a resistor is shown in Fig. 3.8.

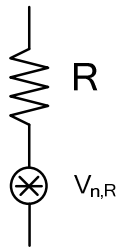


Fig. 3.8 Noise Model of Resistor.

The thermal noise of a resistor can be simplified as a noise voltage source [8]. The thermal noise power density of a resistor is $v^2_{n,R}(f) = 4kTR$ and the noise voltage is

$$v_{n,R}(f) = \sqrt{4kTR}\,. \qquad (3\text{-}15)$$

The noise model for a transistor used here is shown below in Fig. 3.9 [8].

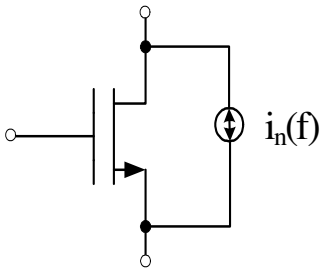


Fig. 3.9 Simplified Noise Model for MOSFET in the Active Region.

The thermal noise of a transistor is simplified as a noise current source at the output terminal which is

$$I_n(f) = \sqrt{4KT\gamma g_m} \qquad (3\text{-}16)$$

where γ is about 2/3 for long channel devices in the saturation region. For short channel devices, γ is typically 2-3 or even larger [8]. Among a number of other reasons, this increased value of γ is due to the carrier heating by large electric fields developed across drain and source. Thus, keeping the drain-source bias voltage as low as possible will reduce the value of γ.

- Noise analysis of the circuit

There are four noise sources in this circuit: source resistor, MOSFET transistor, feedback resistor and load resistor as shown in Fig. 3.10. They are uncorrelated, and because the circuit is linear, superposition can be used for their analysis. To calculate the overall input referred noise, the output referred noise components are obtained from the linear small signal model with input shorted to the ground. Then they are added up and referred back to the input.

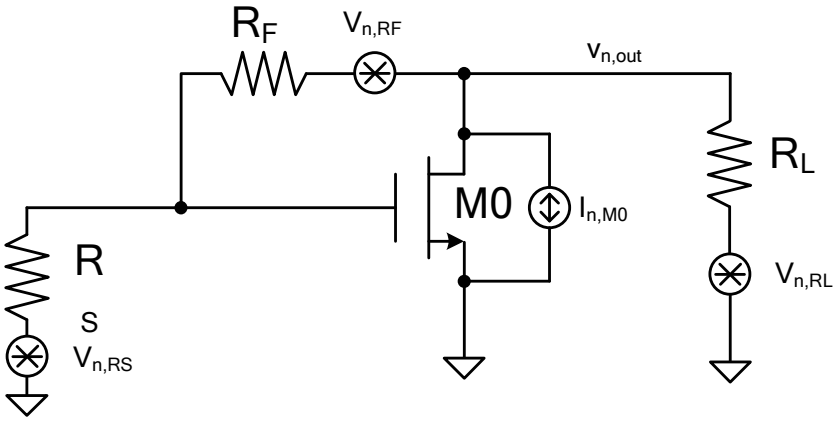


Fig. 3.10 Shunt-Feedback Amplifier Circuit for Noise Analysis.

For the MOSFET transistor M0, its output referred noise is:

$$v_{n,out,M0}^2 = \left(\frac{R_L (R_F + R_S)}{R_F + R_S + R_L + g_m R_S R_L} \right)^2 \cdot 4kT\,\gamma\, g_m \tag{3-17}$$

In this case, $g_m R_S R_L >> R_F + R_S + R_L$, (3-17) can be expressed as

$$v_{n,out,M0}^2 \approx \left(\frac{R_F + R_S}{g_m R_S R_L} \right)^2 \cdot 4kT\,\gamma\, g_m \tag{3-18}$$

The thermal noise from the transistor will be reduced by using large trans-conductance.

For the feedback resistor R_F, the output referred noise is obtained as

$$v_{n,out,RF}^2 \approx 4kTR_F \tag{3-19}$$

This noise is inherently presented due to the resistive feedback. It can not be reduced since R_F has a fixed value determined by AC gain and input impedance matching conditions.

The output referred noise voltage due to the load resistor is computed as follows:

$$v_{n,out,RL}^2 = \left(\frac{\mathrm{R_F} + \mathrm{R_S}}{\mathrm{R_F} + \mathrm{R_S} + \mathrm{R_L} + \mathrm{g_m R_S R_L}} \right)^2 \cdot 4kTR_L$$

$$\approx \left(\frac{R_F + R_S}{g_m R_S R_L} \right)^2 \cdot 4kTR_L \qquad (3\text{-}20)$$

Increasing the load resistor will reduce this noise component.

From equations (3-3) and (3-7), voltage gain is given by

$$Av = \frac{\mathrm{R_L}(1 - \mathrm{g_m R_F})}{\mathrm{R_F} + \mathrm{R_S} + \mathrm{R_L} + \mathrm{g_m} \cdot \mathrm{R_S} \cdot \mathrm{R_L}} \cong -\frac{\mathrm{R_L g_m R_F}}{\mathrm{R_F} + \mathrm{R_S} + \mathrm{R_L} + \mathrm{g_m} \cdot \mathrm{R_S} \cdot \mathrm{R_L}}$$

Therefore, the total input referred noise is then given by:

$$v_{n,in}^2 = v_{n,RS}^2 + \frac{1}{Av^2}\left(v_{n,out,M}^2 + v_{n,out,RF}^2 + v_{n,out,RL}^2 \right)$$

$$= 4kTR_S + \frac{\left((\mathrm{R_L}(1 + \mathrm{g_m R_S}))^2 4kTR_F + (\mathrm{R_L}(\mathrm{R_F} + \mathrm{R_S}))^2 \cdot 4kT\gamma g_m + (\mathrm{R_F} + \mathrm{R_S})^2 4kTR_L \right)}{(\mathrm{R_L g_m R_F})^2}$$

(3-21)

If $g_m R_F >> 1$, $g_m R_S >> 1$, $g_m R_L >> 1$, the input referred noise is given as

$$v^2{}_{n,in} \cong 4kTR_S + 4kTR_S \cdot \frac{R_S}{R_F} + 4kT\gamma \frac{1}{g_m}\left(1+\frac{R_S}{R_F}\right)^2 + 4kT\frac{1}{g_m{}^2 R_L}\left(1+\frac{R_S}{R_F}\right)^2$$

(3-22)

If $R_F >> R_S$ and $g_m R_L >> 1$, the noise factor is approximately

$$F \cong 1+\frac{R_S}{R_F} + \gamma\frac{1}{g_m R_S}\left(1+\frac{R_S}{R_F}\right)^2 + \frac{1}{g_m{}^2 R_L R_S}\left(1+\frac{R_S}{R_F}\right)^2$$

$$\cong 1+\frac{R_S}{R_F} + \gamma\frac{1}{g_m R_S} \qquad (3\text{-}23)$$

To optimize the noise performance of the low noise amplifier, R_F needs to be increased as much as possible. However, the feedback resistance is determined by the input impedance matching condition.

3.4.3 Design Procedure of Shunt-Feedback Broadband LNA

The design specifications for the broadband LNA are listed in Table 3.3.

Table 3.3 The Design Specifications for Broadband LNA.

Input Impedance	75 Ω
Gain	18 dB
Noise Figure (NF)	2.5 dB

For the sake of convenience, the relevant design equations are repeated here.

$$Av = \frac{v_{out}}{v_{in}} \cong -\frac{R_F}{R_S}\frac{1}{1+\frac{1}{g_m R_S}} \tag{3-24}$$

$$R_{in} \cong \frac{R_F}{1+g_m R_L\left(\frac{R_F}{R_F+R_L}\right)} \tag{3-25}$$

$$F \cong 1+\frac{R_S}{R_F}+\gamma\frac{1}{g_m R_S} \tag{3-26}$$

Based on Table 3.2 and considering some design margin, we can choose $R_{in} = 75\ \Omega$, $A_V = 8$, $F = 1.7$. If γ is estimated as 2, solving the equations (3-24), (3-25) and (3-26), we can get,

R_F =780 Ω, g_m =44mA/V, R_L =293Ω.

From the trans-conductance of the transistor and selecting V_{DSAT} to be 300mV based on linearity consideration, we can derive that the bias current is 6.6 mA and the transistor size is 440µm/0.4µm.

There are other restrictions, such as the bandwidth. It is determined by the two poles which are related to the transistor size and the load capacitance. The final circuit parameters are obtained from slight adjustment during the simulations with RF Spectre tools in Cadence.

3.5 Whole Front-End Amplifier Circuit

After the design of each stage, all of them are connected together and the overall performances are verified. The amplifiers are connected by using of coupling capacitors which are selected to be 10pF to isolate the DC voltages between two adjacent stages. The bias resistor RB is selected to be 100kΩ.

Table 3.4 Circuit Parameters Summary.

Component	Parameters	Unit
M0	480/0.4	μm/μm
R_F	780	Ω
R_{L0}	300	Ω
M1, M2	72/0.4	Ω
M3	300/0.8	μm/μm
R_{L1}	200	Ω
CF	98	fF
CB	118	fF
M4, M5	200/0.4	μm/μm
M6	600/0.8	μm/μm
M7	200/0.8	μm/μm
IB	3.5	mA
R_L	50	Ω
CC	10	pF
RB	100	kΩ
VB	1.2	V

The whole 3-stage front-end amplifier circuit is shown in Fig. 3.11. All the circuit parameters are listed in Table 3.4.

All the simulation results are presented in Chapter IV.

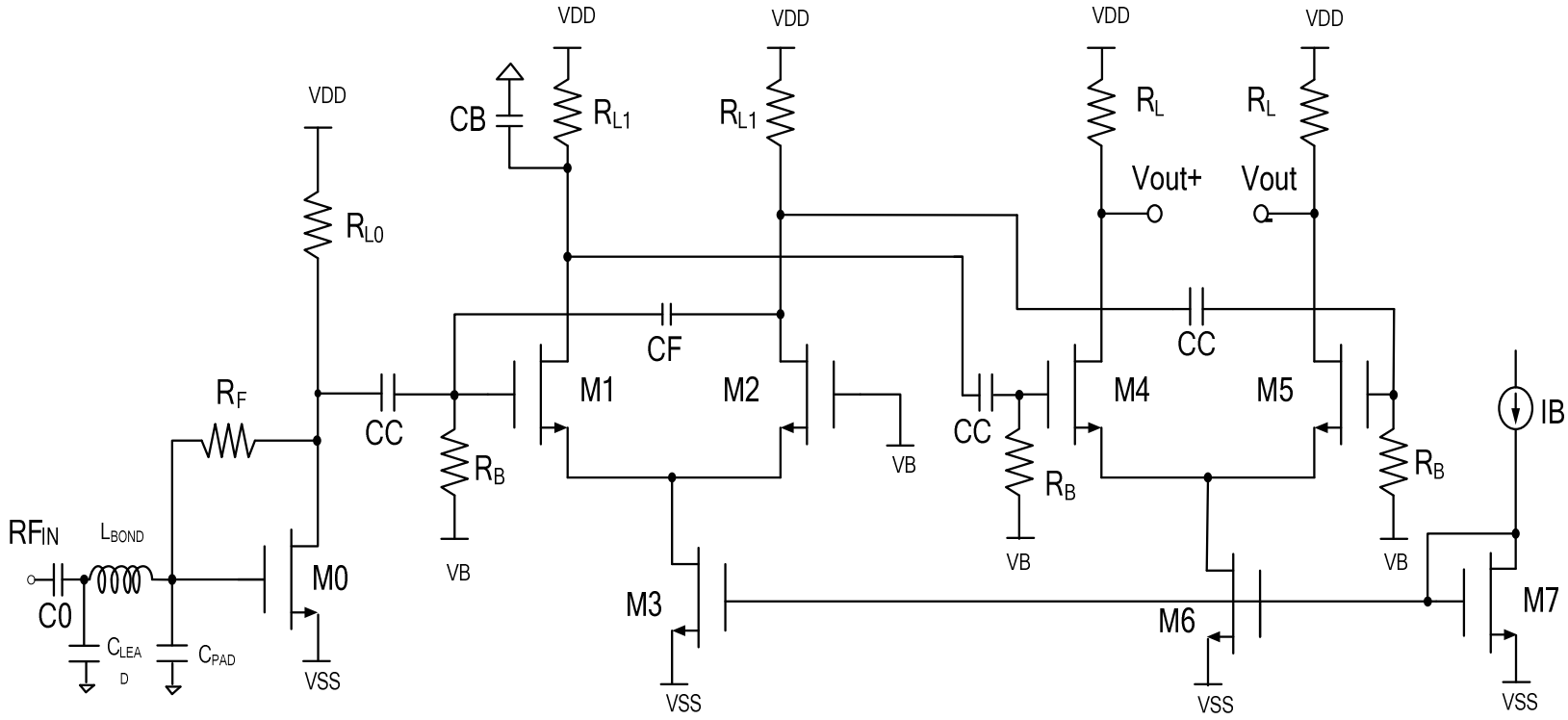


Fig. 3.11 Circuit Configuration of CMOS Front-End Amplifier for DTV Tuner.

CHAPTER IV

SIMULATION AND EXPERIMENTAL RESULTS

The CMOS broadband front-end amplifier for DTV tuner is designed and fabricated using TSMC 0.35μm CMOS technology. This chapter mainly presents simulation results and experimental results of the front-end amplifier. The post-layout simulations considering process parameter variations, temperature gradients and different process corners are carried out. Experimental results show that excellent balancing performance of single-to-differential conversion can be achieved by using the novel compensation methods together with another fully differential stage.

4.1 Layout Considerations

Special attention should be given when the layout of the entire amplifier is made. The basic concerns are as follows.

- To minimize mismatches, layout techniques such as common centroid and inter-digitized pattern are applied to all the transistors, load resistors and capacitors.
- For the transistors in the first stage (broadband low noise amplifier), to minimize the gate resistance (large gate resistance will degrade the noise performance), the length of the poly gate is kept short. The transistor is split into 32 fingers and the width of each finger is 15μm.
- Metal wires are kept wide enough to carry the corresponding current. For the technology used, the allowed current density through metal is about 1mA/μm.

- Guard rings are placed around the circuits to improve isolation from other blocks on the same die and prevent latch up effects. To prevent signal interference between stages, guard rings between each stage are also placed.
- Resistors are implemented with poly. The sheet resistance is 5.8 Ω/square. Small resistors, under 100Ω, are implemented with two or more larger resistors connected in parallel.
- For poly-poly capacitors, if the bottom plates are not grounded, the parasitic capacitances from the bottom plates to the substrate are considered, which are estimated as 10% of the nominal capacitance. For the first DC isolation capacitor, the bottom plate is connected to the output node of the LNA, since there is no such capacitor connected with the other input.
- To minimize the signal interferences between all the stages via bonding wire parasitics, different pins are used for the power supply of each stage.

The layout of the whole amplifier is shown in Fig. 4.1. It occupies a 980μm×368μm die area.

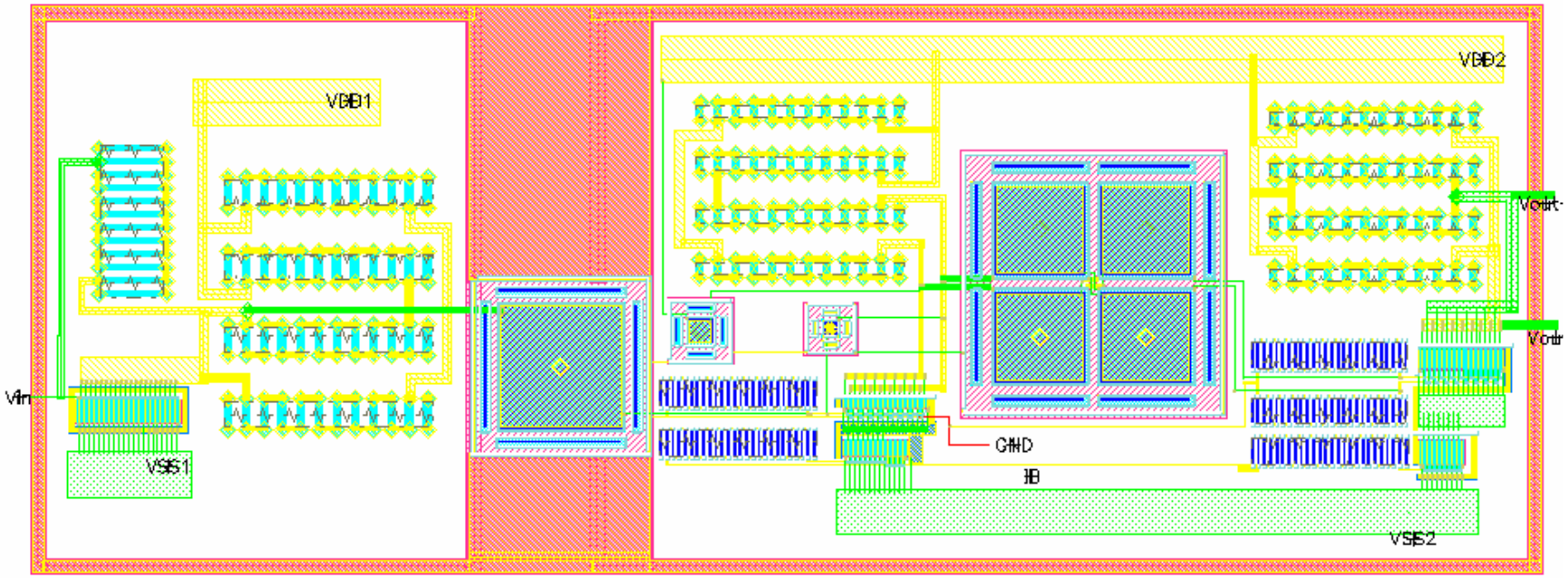


Fig. 4.1 Layout of CMOS Front-End Amplifier for DTV Tuner.

4.2 Post Layout Simulation Results

4.2.1 Broadband Input Impedance Matching, Power Gain and Noise Performance.

S-parameter analysis is used to measure the power gain, input impedance matching and noise performance of the whole circuit. Cadence simulations at 50°C with typical technology parameters were carried out; the results are shown in Fig. 4.2. From Fig. 4.2, over 50M~850MHz, S11 is less than -11.6dB and the noise figure is less than 2.74 dB. The power gain (S21) drops from 18.1dB at 50MHz to 16.1dB at 850MHz.

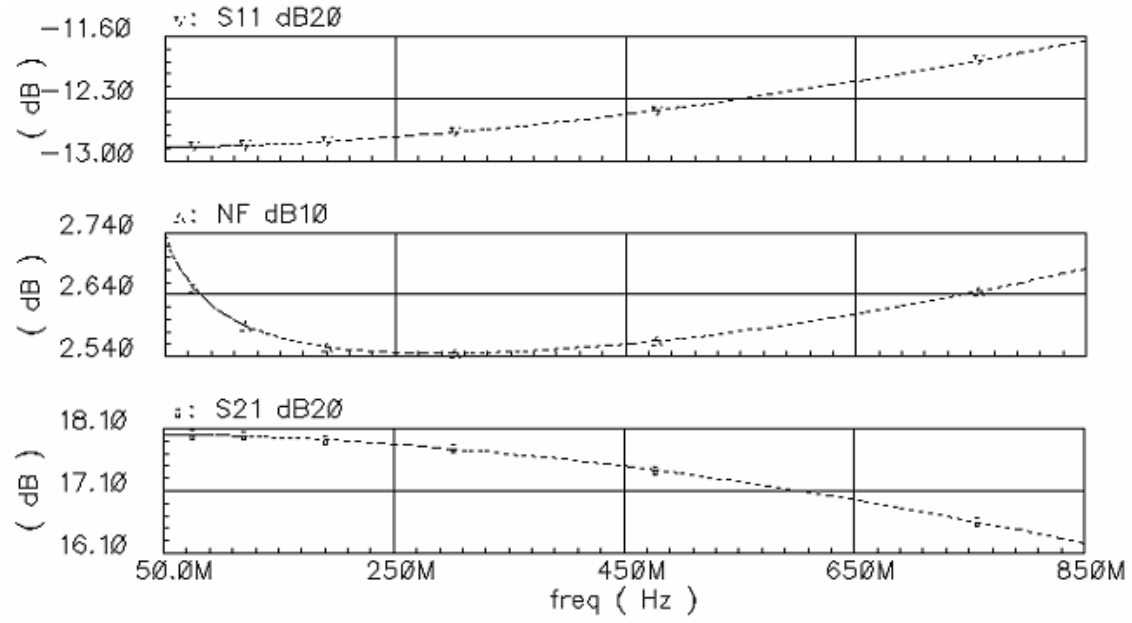


Fig. 4.2 S-Parameter Simulation Results.

4.2.2 Balance Accuracy of the Differential Output Signal

Fig. 4.3 shows the differential output signal errors of the whole front-end amplifier from the post layout simulation. Magnitude error in percentage is measured as the magnitude difference over the average magnitude of the differential output voltages.

$$Magnitude\ Error(\%) = \frac{|v_{out+}| - |v_{out-}|}{\frac{|v_{out+}| + |v_{out-}|}{2}} \times 100\%$$

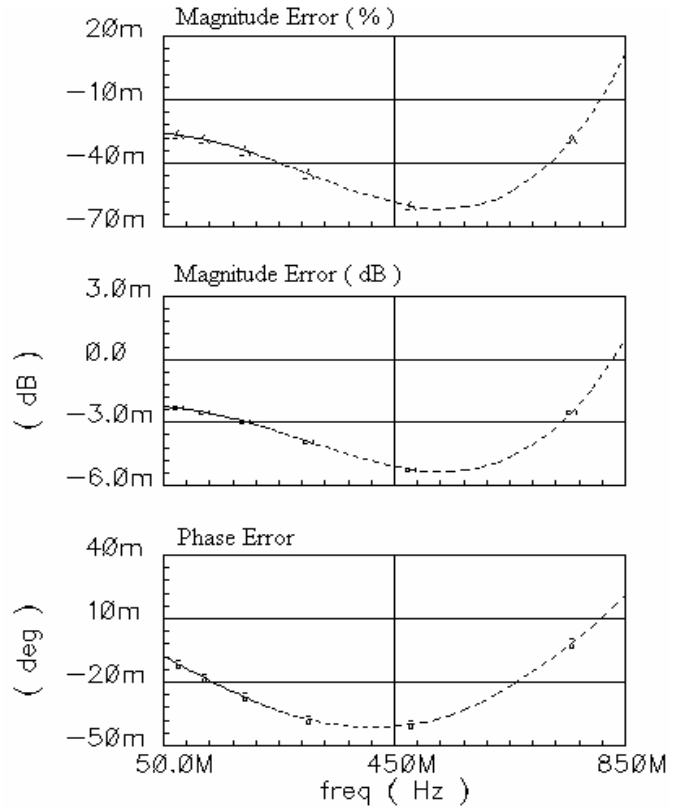


Fig. 4.3 Differential Errors at 50°C Using Typical Technology Parameters.

From Fig. 4.3, over 50M~850MHz, the magnitude error is less than 0.07%, while the absolute difference between two differential output voltage magnitudes is less than 0.006dB. The phase error is less than 0.05°. The differential output voltages achieve excellent balance.

Simulations are also carried out to verify the robustness of the circuit, i.e., the sensitivity to variations such as process variation, environment temperature and the process parameter corners.

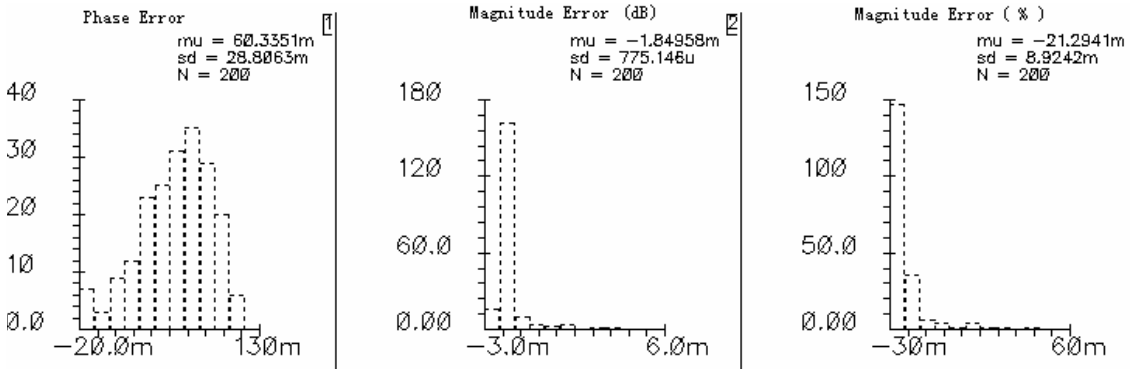


Fig. 4.4 Differential Errors With Process Variation and Mismatches.

Monte Carlo simulation in Cadence Spectre tools is done to check the process variation and mismatching effect. For MOSFET transistor, we assume threshold voltage and channel mobility follow a Gaussian distribution with the standard deviation equal to 15% of the mean value. This assumption is based on data available from other technologies. Fig. 4.4 shows the histogram of the maximum phase error and magnitude

error distribution. With 200 samples, most of the maximum overall phase errors fall into the range between -0.02 and 0.13 degrees. For magnitude errors, more than 75% of 200 runs are within the range of 0.03%.

The parameter simulation with gradient temperature is used to check the environment effect. Fig. 4.5 shows the magnitude and phase errors variation when environment temperature varies. The variation range is selected to be from 0°C to 65°C, which covers the in-door operation range. From Fig. 4.5, at 0°C, the phase errors of the differential output signals is from -0.03° to 0.06°, at 65°C , it is from -0.01° to -0.06°C. The maximum phase error in this temperature range is less than 0.06°. For magnitude error, it is from -0.85 to -0.002dB at 0°C and from -0.005 to 0.003dB at 65°C. The maximum magnitude errors are less than 0.1%.

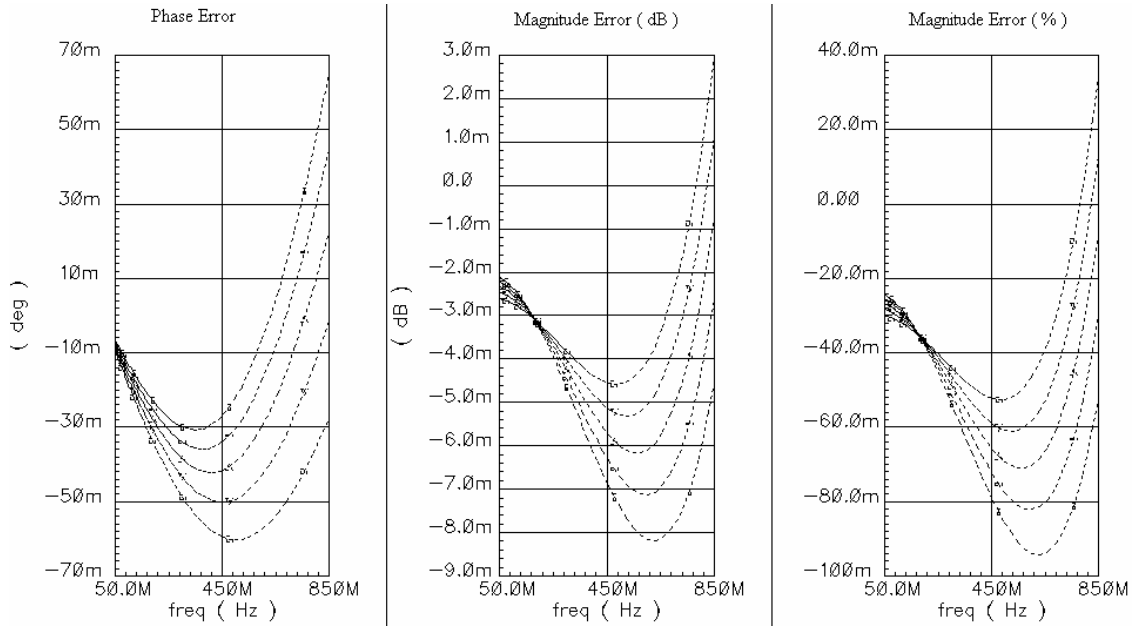


Fig. 4.5 Errors With Temperature Variation.

Fig. 4.6 shows the magnitude error and phase error simulation results using corner parameters. Fast corner and slow corner are both used in the simulations.

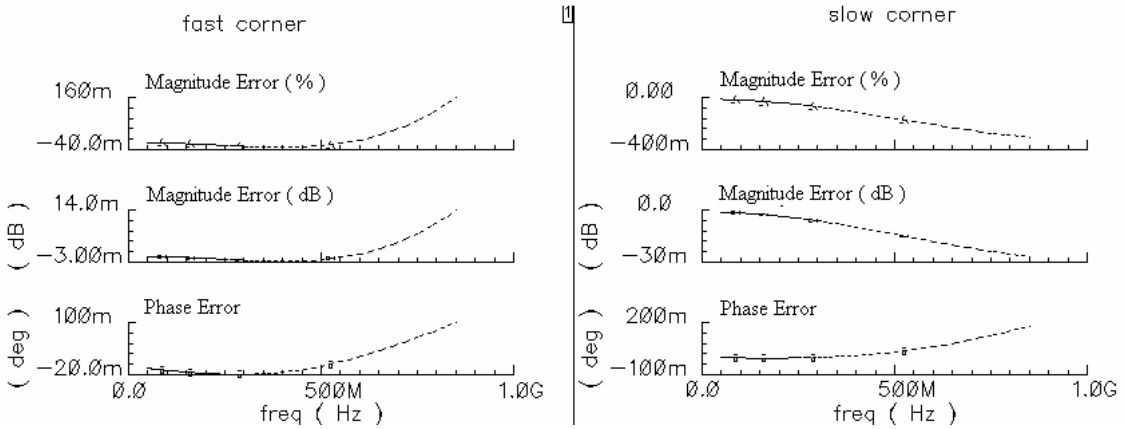


Fig. 4.6 Errors Using Fast Corner and Slow Corner.

It can be seen from Fig. 4.6, the worst case is the slow corner. With slow corner parameters, magnitude error is less than 0.4%, and phase error is less than 0.2 degree.

4.3 Simulation Performance Summary

From post-layout simulation results, the performances of the CMOS RF amplifier are summarized in Table 4.1

Table 4.1 Post Layout Simulation Performance Summary.

Performance	Value	Unit
Power Supply	1.65~-1.65	V
Phase error	< ± 0.3	degree
Magnitude error	< 0.4%	
Gain	16	dB
NF	2.8	dB
S11	-11	dB
Total current consumption	26	mA
Die area	980×368	μm×μm

4.4 Test and Measurement

The DTV tuner IC is fabricated using TSMC 0.35μm standard CMOS process through the MOSIS service and sealed in a 100-pin TQFP plastic package. The die micro-photograph of the front-end amplifier is shown in Fig. 4.7

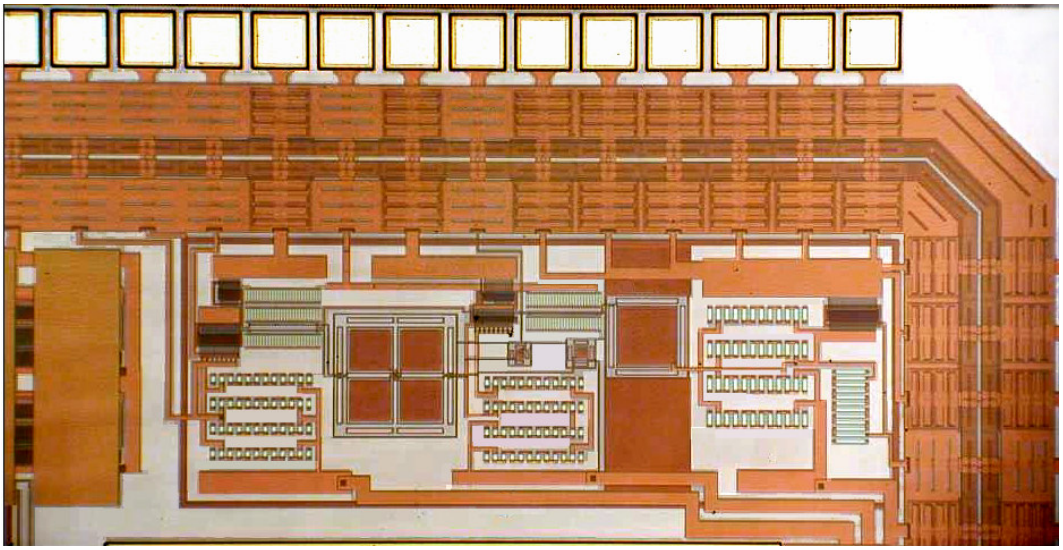


Fig. 4.7 Die Micro-Photograph of Front-End Amplifier.

A printed circuit board is designed to test and verify the performance of the three-stage front-end amplifier. The schematic of the PCB is shown in Fig. 4.8.

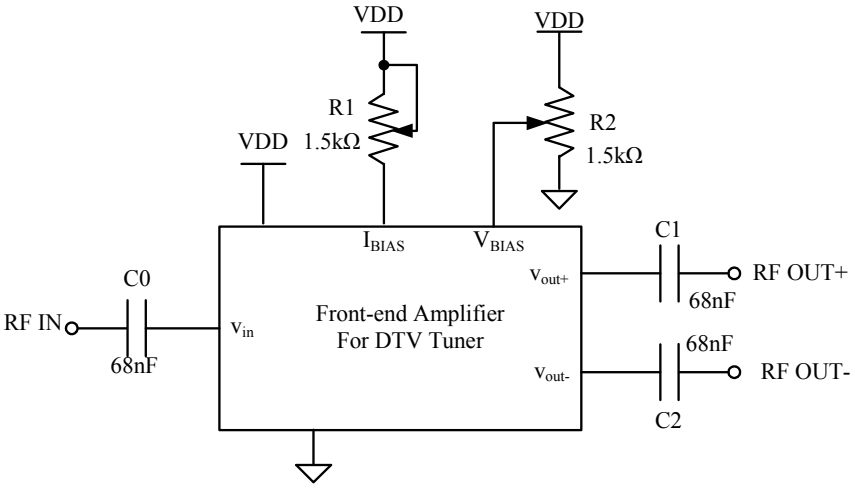


Fig. 4.8 Schematic of the PCB.

Surface-mount DC blocking capacitors (C0, C1, C2) are used at both input and output terminals. Two variable resistors (R1, R2) are used to provide bias. The test board is shown in Fig. 4.9. The whole front-end amplifier is tested as a single block since there is no access to the internal node within the cascaded three stages.

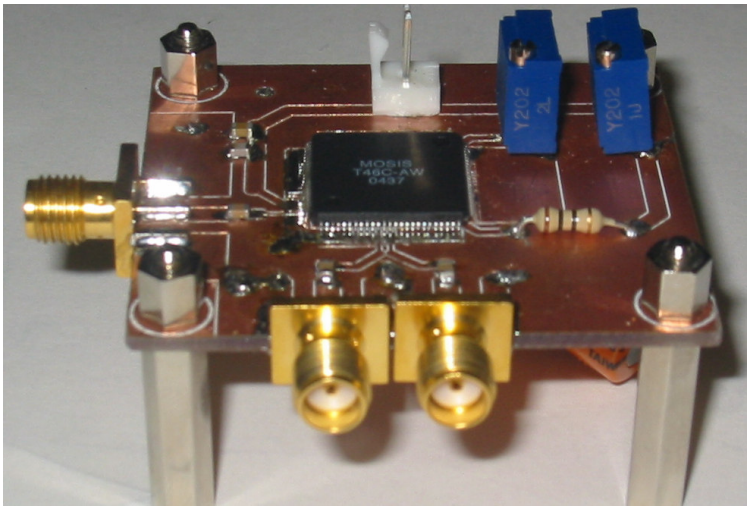


Fig. 4.9 Photograph of Printed Circuit Board for Testing.

4.4.1 Measurement of the Magnitude and Phase of Differential Output Voltage

A Hewlett Packard 8719ES S-parameter network analyzer is used to measure the magnitude and phase of differential output voltages. It is calibrated using a standard terminal before the measurement. The output signals are measured one by one. One output signal is fed into the analyzer and measured with another output port terminated with a standard 50Ω broadband resistor.

Fig. 4.10 shows the experimental setup for S-parameter measurement.

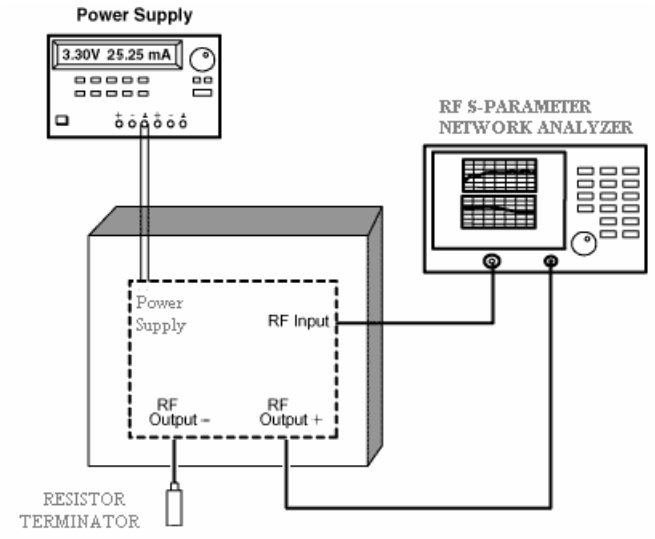


Fig. 4.10 Experimental Setup for S-Parameter Measurement.

Fig. 4.11 shows measurement results for the differential phase error between two output signals. Here the phase error of differential output signal is measured as [Phase(vout+)-Phase(vout-)]. The reference point is 180°, and the scale is 0.5°/div. Over 50MHz~1GHz frequency range, the phase error is within -1.5°~1.2° range.

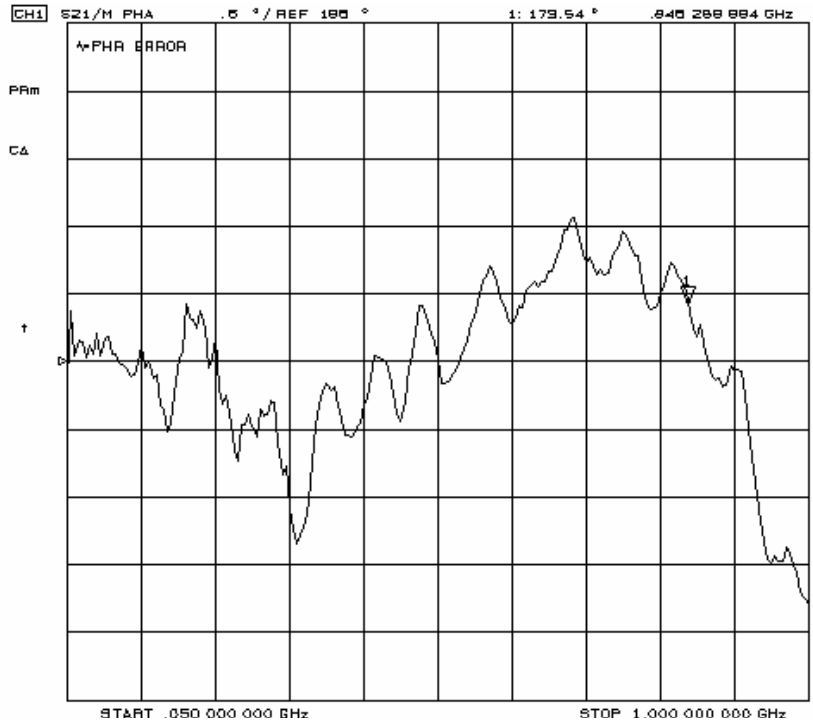


Fig. 4.11 The Phase Error Between Two Output Signals.

Fig. 4.12 shows the magnitude error between two output signals. The magnitude of signal is measured using the S21 parameter. In Fig. 4.12, the reference gain is 0dB, and the scale is 0.25dB/div. Over the 50MHz~850MHz frequency range, the magnitude error is between -0.75dB~0.5dB.

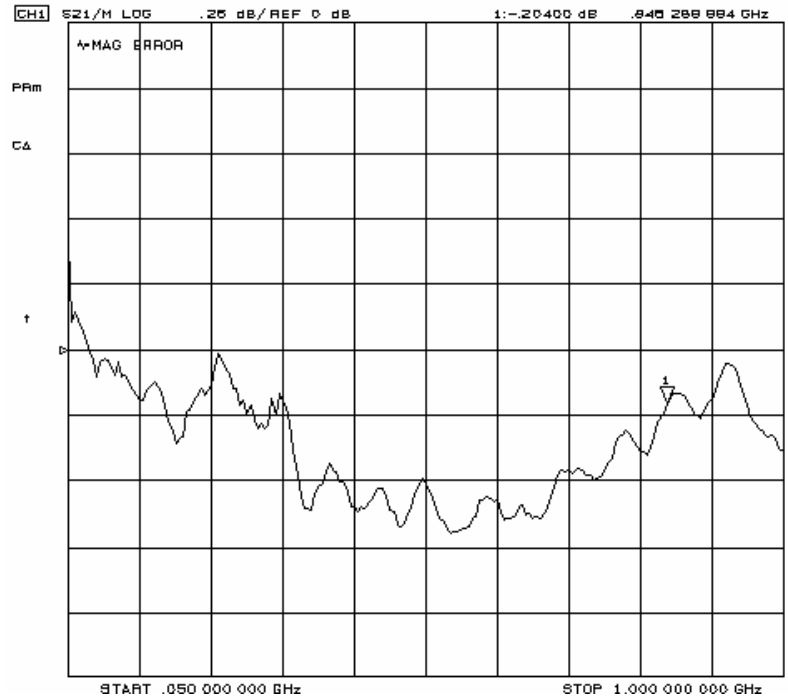


Fig. 4.12 The Magnitude Error Between Two Output Signals.

The testing and measurement results for the differential errors are higher than the simulation results. In practice, the mismatches for the signal traces, the mold contact resistors and other parasitic components on board degrade the performance. Notwithstanding that, the experimental results are still able to verify that the excellent differential signal balance is achieved by using the novel compensation method together with the additional fully differential stage.

4.4.2 The Other Performances of the Whole Front-End Amplifier

Fig. 4.13 shows the impedance matching performance measured with an S-parameter network analyzer.

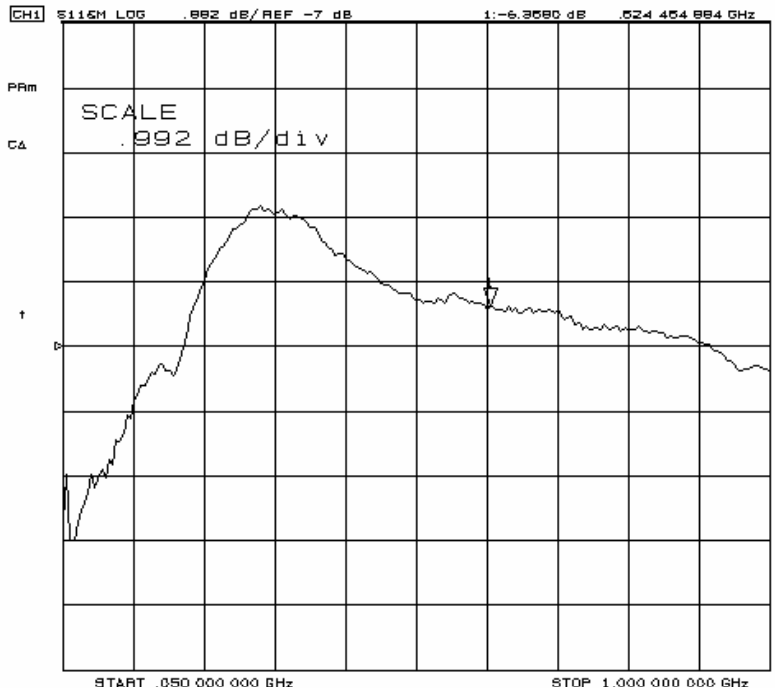


Fig. 4.13 S11 of the Broadband Amplifier.

In Fig. 4.13, the reference point is -7dB, the scale is 1dB/div. The S11 is -10dB at low frequency. It goes up to -5dB around 200Mhz, and then drops down to -6dB around 300MHz, and continues to -7dB until 850MHz.

The gain and noise figure is measured using the RODHE&SCHWARZ spectrum analyzer.

A broadband noise source is used for noise figure measurement. It is calibrated before the measurement. The equipment setup of the test is shown in Fig. 4.14.

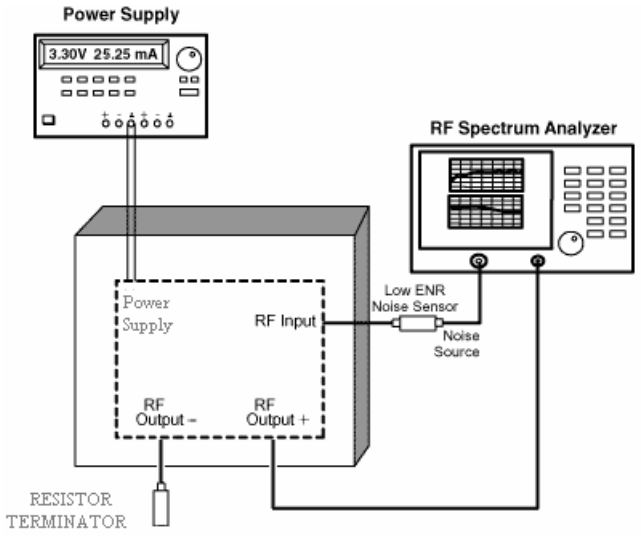


Fig. 4.14 Experiment Setup for Noise Figure Measurement.

Fig. 4.15 shows the measurement results of gain-noise performance from the spectrum analyzer.

In Fig. 4.15, the frequency is swept from 10MHz to 900MHz. The low frequency differential gain is 24.2dB. The noise figure is around 4.6 dB over the whole signal range from 50MHz to 850MHz.

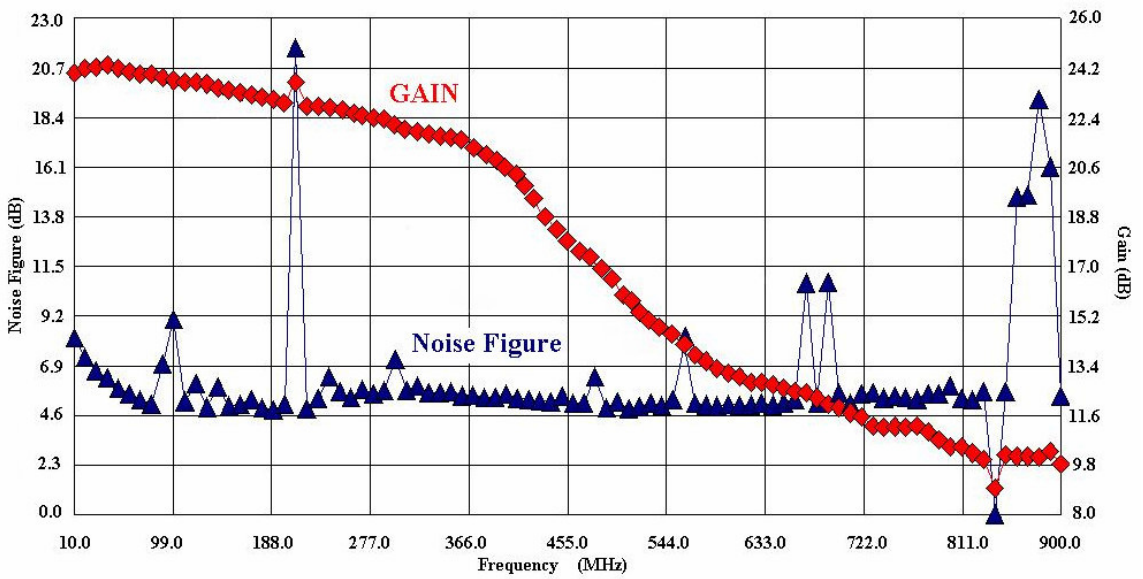


Fig. 4.15 Gain-Noise Spectrum.

The bandwidth is lower (around 350MHz) than the simulation results. This is due to the strong package parasitic effect. The package is 10mm×10mm due to the large pad frame determined by the total number of pins. The die area is only 3mm×3mm. The bonding wire inductance can be 4nH if they are estimated as more than 1nH/mm, for both input and output signals. The extended leads, the parasitic capacitors for each lead can be up to 3pF. On the other side, the pad capacitance is added to the input/output terminal as well, which is around 1pF. Also there are some parasitic components on the board. All these effects degrade the frequency response of the whole amplifier.

For a rough estimation, the package is modeled as shown in Fig. 4.16.

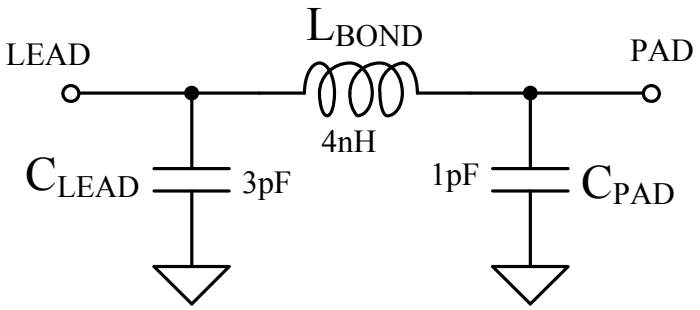
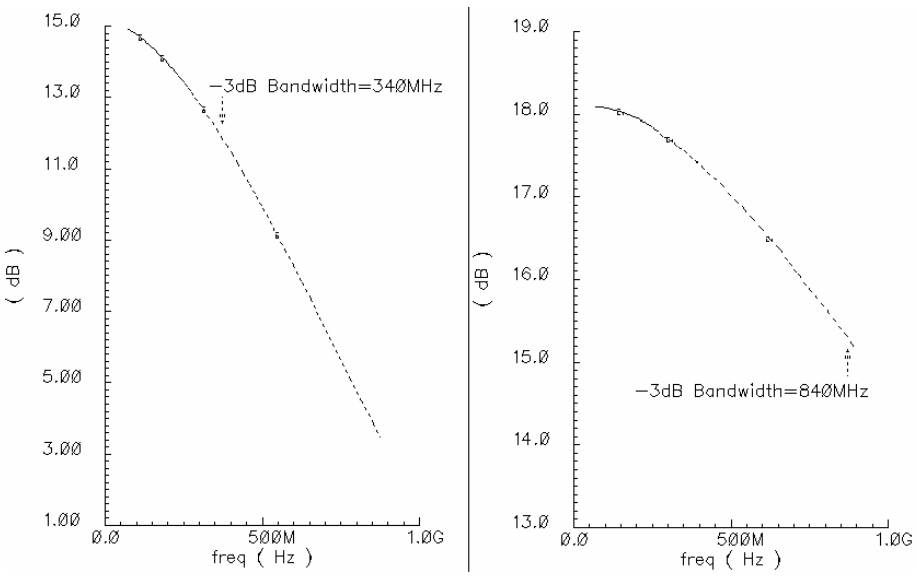


Fig. 4.16 Simplified Package Model.

To estimate the effect of frequency response from the package, AC response is obtained from simulation with a simplified package model added to the input and output of the circuit. The simulation is under the circumstance temperature 50°C and slow corner model. The simulation result is shown in Fig. 4.17.



(a) (b)

Fig. 4.17 Frequency Response Considering Package Model.

Fig. 4.17 (a) illustrates the frequency response with package model and slow corner processing parameter at 50°C. Fig. 4.17 (b) illustrates the frequency response without package model using typical corner processing parameter at 25°C. It can be seen that the -3dB bandwidth of the amplifier drops from 840MHz to 340MHz. Also the low frequency gain drops from 18dB to 15dB. It shows that large package, temperature and process variation can be the reasons for a degradation frequency response of the testing results.

Actually, the package model used in the simulation is not accurate, especially for broadband application. And the NCSU design kits in Cadence for 0.35μm technology can not extract all the parasitic components, especially the resistors of the metal wire. This will also cause some deviations between the simulation results and the measurement results.

4.5 Summary of the Experimental Results

The CMOS broadband front-end amplifier is fabricated and tested. The experimental results verified that using the novel compensation method together with a fully differential stage, the on-chip single-to-differential conversion can achieve excellent balance accuracy. Over 50M~850MHz frequency range, the phase error is less than 1.5° and the magnitude error is less than 0.75dB.

CHAPTER V

CONCLUSIONS

Traditional active single-to-differential converters usually have a large differential mismatch especially for broadband applications. For those applications that require accurate differential signals, such as high image rejection single-conversion DTV tuner, a novel compensation method is proposed to reduce the phase and magnitude errors. An additional fully differential buffer is used to further improve the performance and drive the following heavy load. A broadband low noise amplifier is also designed as the first stage to complete the front-end amplifier design.

The new compensation method proposed for the single-to-differential converter features simplicity, accuracy and robustness. Together with the fully differential stage, it achieves excellent balance for the differential output signals. The circuit is fabricated in 0.35μm CMOS technology. The experimental results show that the phase error is less than ±1.5°. The magnitude error is less than ±0.75dB from 50MHz to 850MHz.

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