

SELF-CALIBRATING RANDOM ACCESS LOGARITHMIC PIXEL
FOR ON-CHIP CAMERA

A Thesis

by

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Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2005

Major Subject: Electrical Engineering

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ABSTRACT

Self-calibrating Random Access Logarithmic Pixel
for On-chip Camera.

(May 2005)

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CMOS active pixel sensors (APS) have shown competitive performance with charge-coupled device (CCD) and offer many advantages in cost, system power reduction and on-chip integration of VLSI electronics. Among CMOS image sensors, sensors with logarithmic pixels are particularly applicable for outdoor environment where the light intensity varies over a wide range. They are also randomly accessible in both time and space. A major drawback comes from process variations during fabrication. This gives rise to a considerable fixed pattern noise (FPN) which deteriorates the image quality. In this thesis, a technique that greatly reduces FPN using on-chip calibration is introduced. An image sensor that consists of 64×64 active pixels has been designed, fabricated and tested. Pixel pitch is $18 \mu\text{m} \times 19.2 \mu\text{m}$ and is fabricated in a $0.5\text{-}\mu\text{m}$ CMOS process. The proposed pixel circuit considerably reduces the FPN as predicted in theoretical analysis. The measured FPN value is 2.29% of output voltage swing and column-wise FPN is 1.49% of mean output voltage over each column.

DEDICATION

To my family, especially Michael, Catherine and Tina who have extended great love and support throughout my life

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TABLE OF CONTENTS

	Page
ABSTRACT	iii
DEDICATION	iv
ACKNOWLEDGEMENTS	v
TABLE OF CONTENTS	vi
LIST OF FIGURES	viii
LIST OF TABLES	xi
 CHAPTER	
I INTRODUCTION.....	1
1.1 Motivation.....	1
1.1.1 Why CMOS pixels?.....	1
1.1.2 Pixel circuits	2
1.1.3 Previous works	6
1.2 Contributions.....	16
II DESCRIPTIONS.....	18
2.1 Self-calibrating random-access logarithmic pixel.....	18
2.1.1 Topology.....	18
2.1.2 Realization.....	22
2.1.3 Spice simulation.....	28
2.2 MATLAB tool for analog circuit design.....	38
2.2.1 Objective.....	38
2.2.2 Extractor.....	38
2.2.3 Analog equations.....	39
2.2.4 Functions.....	39
2.3 Peripheral circuits.....	43
2.3.1 Overall chip schematic.....	43

CHAPTER	Page
2.3.2	6 to 64 decoder.....44
2.3.3	64 to 1 multiplexer.....47
2.3.4	Low voltage cascoded current mirror.....50
2.3.5	Source follower.....56
2.3.6	Unity-gain buffer.....60
2.4	Layouts.....68
2.4.1	Pixel.....68
2.4.2	Unity-gain buffer.....70
2.4.3	Overall chip.....72
III	TEST AND EVALUATIONS.....75
3.1	Test setup.....75
3.2	Qualitative analysis.....76
3.3	Quantitative analysis.....81
IV	CONCLUSIONS.....84
	REFERENCES.....86
	APPENDIX A.....89
	VITA.....92

LIST OF FIGURES

	Page
Figure 1-1	Passive pixel schematic.....2
Figure 1-2	Photodiode-type active pixel schematic.....3
Figure 1-3	Photogate-type active pixel schematic.....4
Figure 1-4	Logarithmic pixel schematic.....5
Figure 1-5	Conventional logarithmic pixel.....6
Figure 1-6	Logarithmic pixel on-chip calibration with reference current.....7
Figure 1-7	Schematic of on-chip calibration with column amplifier10
Figure 1-8	On-chip calibration with column amplifier when Φ_1 off, Φ_2 on.....11
Figure 1-9	On-chip calibration with column amplifier when Φ_1 on, Φ_2 off.....12
Figure 1-10	Logarithmic pixel with in pixel calibration amplifier13
Figure 1-11	Logarithmic pixel with leakage current calibration.....15
Figure 2-1	Topology of self-calibrating random access logarithmic pixel18
Figure 2-2	Clock signal ϕ19
Figure 2-3	Realization of SRL pixel22
Figure 2-4	Scheme of clock signal ϕ for SRL pixel operation22
Figure 2-5	SRL pixel operation when $t = 0^-$23
Figure 2-6	SRL pixel operation when $0^+ \leq t \leq t_1^-$24
Figure 2-7	Transient column voltage V_C at readout mode.....30

	Page
Figure 2-8 Transient gate voltage of load transistor M1	31
Figure 2-9 Transient currents flowing through M1 when $I_{\text{photo}}=1\text{pA}$	32
Figure 2-10 Transient column voltage V_C when $I_{\text{photo}}=0.1\text{p}\sim 1\text{nA}$	33
Figure 2-11 Transient column voltage V_C when $I_{\text{photo}}=1\text{n}\sim 1\mu\text{A}$	34
Figure 2-12 Transient currents flowing through M1 when $I_{\text{photo}}=0.1\text{p}\sim 1\text{nA}$	35
Figure 2-13 Transient currents flowing through M1 when $I_{\text{photo}}=1\text{n}\sim 1\mu\text{A}$	36
Figure 2-14 Column voltage V_C according to reference voltage V_B ($I_{\text{photo}} = 1\text{pA}$)	37
Figure 2-15 Spice simulation of column voltage VS photocurrent (10p to 1u).....	38
Figure 2-16 Overall chip schematic	43
Figure 2-17 2 to 4 decoder	45
Figure 2-18 6 to 64 decoder	46
Figure 2-19 2 to 1 multiplexer schematic using transmission gates	47
Figure 2-20 Schematic of 64 to 1 multiplexer.....	49
Figure 2-21 Low voltage cascoded current mirror.....	50
Figure 2-22 Output current as a function of output voltage.....	53
Figure 2-23 Output resistance characteristic as a function of output voltage	54
Figure 2-24 Output resistance characteristic as a function of frequency	55
Figure 2-25 Source follower.....	56
Figure 2-26 Voltage transfer characteristic.....	59
Figure 2-27 Gain as a function of input voltage.....	59

	Page
Figure 2-28 Two-stage operational amplifier for unity gain buffer.....	60
Figure 2-29 Magnitude & phase response of operational amplifier.....	66
Figure 2-30 Gain versus common mode input in unity-gain buffer configuration.....	67
Figure 2-31 Output voltage in response to rail-to-rail differential input pulse	67
Figure 2-32 SRL pixel layouts	69
Figure 2-33 Layout of unity-gain buffer with source follower	70
Figure 2-34 Output voltage versus input common mode range	71
Figure 2-35 Gain versus input common mode range	72
Figure 2-36 Overall chip schematic for SRL pixel	73
Figure 3-1 Block diagram for testing.....	75
Figure 3-2 Chip microphotograph.....	76
Figure 3-3 Column output voltage V_C when $V_B=2.5V$	77
Figure 3-4 Column output voltage V_C when $V_B=3V$	78
Figure 3-5 Column output voltage V_C when $V_B=4V$	78
Figure 3-6 Column output voltage V_C when $I_R = 0.5 \mu A$	79
Figure 3-7 Column output voltage V_C when $I_R = 2 \mu A$	80
Figure 3-8 Column output voltage V_C when $I_R = 3 \mu A$	80
Figure 3-9 Transient scope view of V_C when irradiance = $25\mu W/cm^2$	81
Figure 3-10 Transient scope view of V_C when irradiance = $250\mu W/cm^2$	82
Figure 3-11 Response of sensor as a function of light intensity at sensor level.....	83

LIST OF TABLES

	Page
Table 2-1. Truth table of 2 to 4 decoder	45
Table 2-2. Truth table for 4 to 1 multiplexer	48
Table 2-3. Target specifications for a lead-compensated two-stage opamp	60
Table 2-4. Device dimensions for opamp	65
Table 2-5. Simulation results	65
Table 2-6. Specifications	69
Table 2-7. Pins & notations for operation	74

CHAPTER I

INTRODUCTION

1.1 Motivation

1.1.1 Why CMOS pixels?

Today, there are many kinds of electronic cameras for various purposes. Camcorders are probably the most well known camera for capturing images with television resolution. In spite of these varieties, they are also known to have the same basic functions according to Fossum's paper [1]. These are 1) optical collection of photons, i.e., a lens; 2) wavelength discrimination of photons, i.e., filters; 3) detector for conversion of photons, e.g., photodiode; 4) a method to readout the detectors, e.g., a CCD; 5) timing, control and drive electronics for the sensor; 6) signal processing electronics for correlated double sampling, color processing, etc.; 7) analog-to-digital conversion ; and 8) interface electronics. In order to read out the electrical signal from the detector, charge coupled device (CCD) method still captures higher resolution images at slower frame rate. Despite high quality of images, CCD has several drawbacks. First, cameras based on CCD are presently expensive for consumer applications. Secondly, a CCD based system often consumes several watts of power which becomes a

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major drain on a power resource, i.e., battery.

Thirdly, the volume and mass of electronics constrains the level of miniaturization achievable with the system. Because of customer demand for miniaturization, low-power consumption and cost effectiveness of imaging systems, CMOS image sensors have been developed over the past few years. CMOS image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip which called “camera-on-a-chip” and reduce component packaging cost. Such a camera-on-a-chip will operate with standard logic supply voltages and consume power measured in the tens of miliwatts [2],[3].

1.1.2 Pixel circuits

There are several ways to implement pixel in CMOS. However, four main approaches to this are as follows [1].

A. Passive pixel

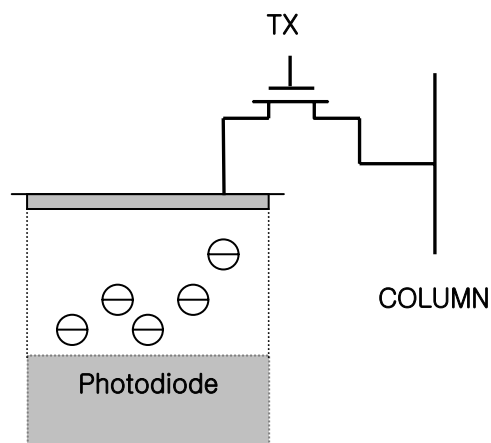


Figure 1-1 Passive pixel schematic.

Basic concept of the passive pixel is shown in Fig.1-1. It consists of a photodiode, a access transistor and a charge integrating amplifier (CIA) readout circuit at the bottom of the column bus. If the photodiode is accessed by activating transistor, the voltage on the photodiode is reset to the column bus voltage, and the charge from photosignal is converted to a voltage a voltage by the CIA. This kind of configuration allows very high fill factor for a given pixel size. But relatively high readout noise level and bad scalability are known to be the major problems with the passive pixel.

B. Photodiode-type active pixel

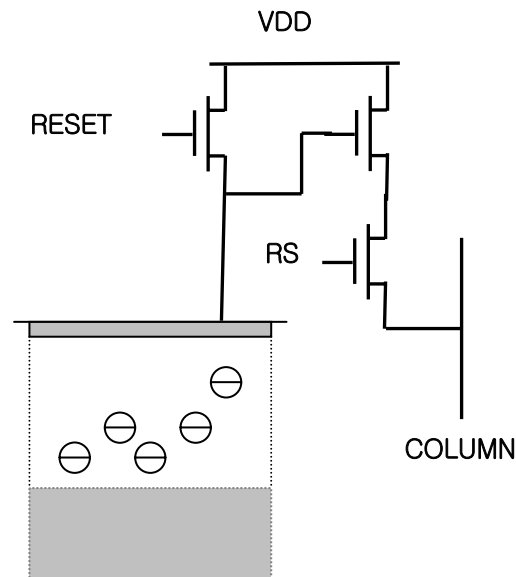


Figure 1-2 Photodiode-type active pixel schematic.

Shortly after the passive pixel was invented, it came upon with the idea that the insertion of a buffer/amplifier into the pixel could potentially improve the performance of the pixel. Therefore, a sensor with an active amplifier within each pixel called active

pixel sensor (APS) was invented. The photodiode-type active pixel was described by Noble in 1968 [4]. The basic concept of photodiode-type APS is shown in Fig.1-2. The voltage on the photodiode is buffered.

C. Photogate-type active pixel

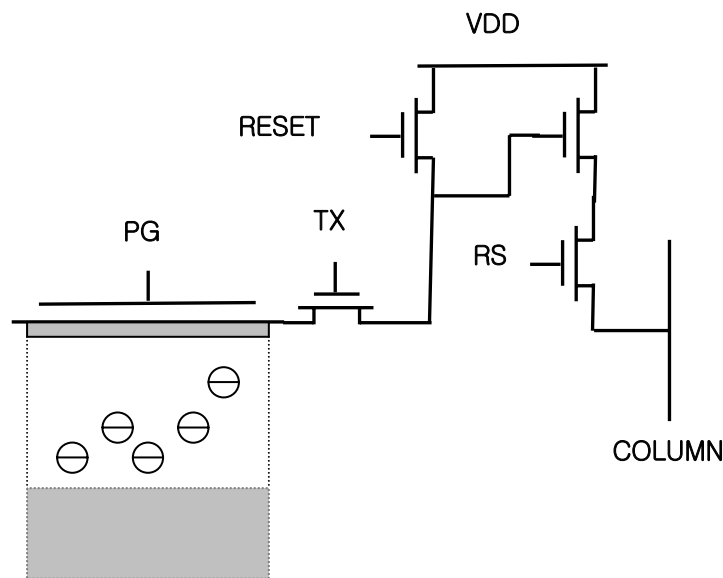


Figure 1-3 Photogate-type active pixel schematic.

The photogate-type active pixel was introduced by JPL in 1993 [5]-[7] for high performance scientific imaging and low-light applications. This configuration combines CCD benefits and X-Y readout. Schematic is shown in Fig.1-3. There are two output levels in operating the sensor. One is the reset level which means the voltage measured by the source follower when an output floating diffusion is reset during readout. The other is the signal level which means the new voltage sensed when the integrated charge

is transferred to the output diffusion by pulsing the photogate. The difference between these two levels is the output of the sensor which called “correlated double sampling”.

D. Logarithmic pixel

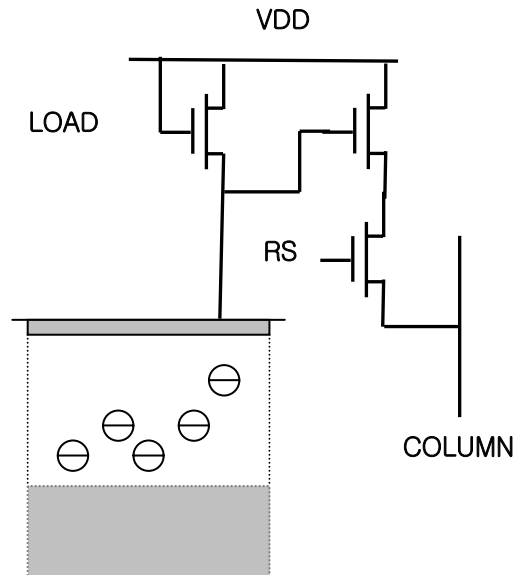


Figure 1-4 Logarithmic pixel schematic.

In a typical scene encountered in an outdoor environment, the light intensity can vary over a wide range, as, for instance, wide as six decades (120dB). For this case, logarithmic pixel can offer an solution which has the non-linear output of the sensor. An example of logarithmic pixel circuit [8] is shown in Fig.1-4. The photodiode voltage self-adjusts to a level that the load transistor current is equal to the photo current collected by the photodiode. This results in a logarithmic transformation of the photosignal for typical light levels and wide intra-scene dynamic range. Additional to the wide dynamic range, random accessibility of logarithmic pixel in both time and space is

another strong point of this pixel. Drawbacks to this non-integrating aspect are known to be slow response time for low light levels and large fixed pattern noise (FPN) due to process variations. In this work, newly developed logarithmic pixel is introduced which minimizes the fixed pattern noise.

1.1.3 Previous works

Many good works have been done to improve drawbacks of logarithmic pixels. Here we would like to introduce some of good works about logarithmic pixels and evaluate them analytically to know how each work different from others.

A. Conventional logarithmic pixel

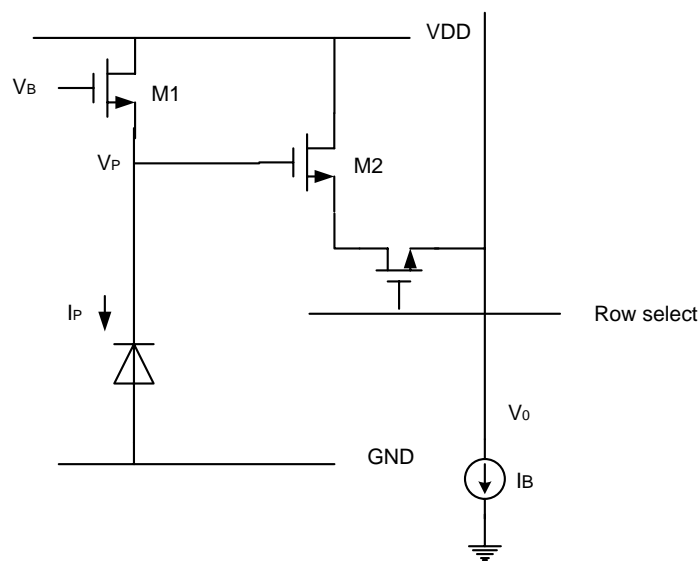


Figure 1-5 Conventional logarithmic pixel.

Conventional logarithmic pixel schematic is shown in Fig.1-5. This circuit has several advantages. First, it is very simple circuit and has a compact layout because it consists of NMOS and photodiode is just an extension of M1 source. Secondly, this circuit has highest possible dynamic range up to 120 dB due to logarithmic compression. Thirdly, it has random accessibility [9] which is important in view of speed. But low signal to noise ratio unlike the integrating pixels and FPN (Fixed Pattern Noise) due to M1 and M2 are the main disadvantages of conventional logarithmic pixel. There is no reset mode to apply conventional CDS (Correlated Double Sampling) technique for calibration. In order to suppress the FPN, several techniques such as off-chip memory-based techniques (Refs [10], [11]), on-chip solution based on floating-gate or hot-carrier injection [12], [13] and on-chip calibration with reference current [14].

B. On-chip calibration with reference current

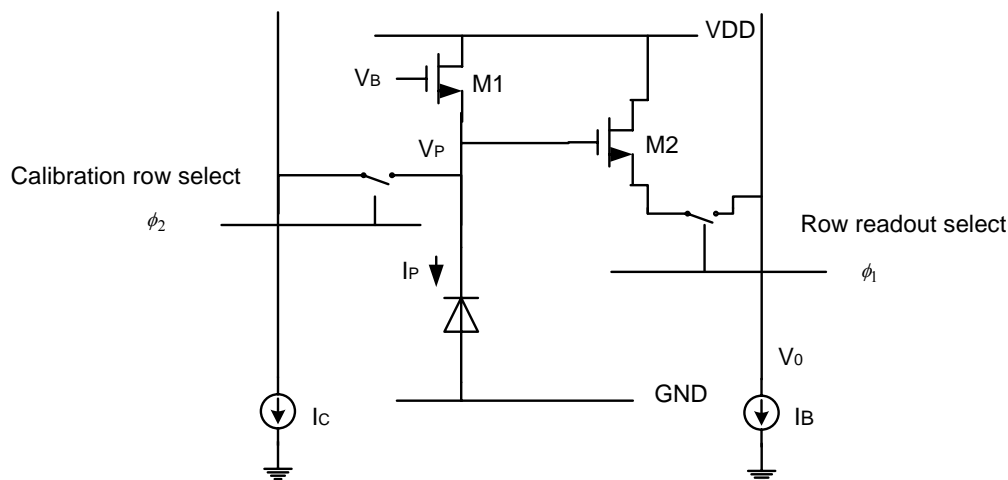


Figure 1-6 Logarithmic pixel on-chip calibration with reference current.

Schematic of logarithmic pixel on-chip calibration with reference current is shown in Fig. 1-6. Analytical approach to circuit behavior is described as follows;

First Φ_1 is turned on; V_p is read out (as V_0) and stored. Then, Φ_2 is turned on and a large I_C is imposed on M1, and new V_p is read out and subtracted from the I_p generated V_p . Then here is an evaluation of FPN performance:

a) Φ_1 on, Φ_2 off

$$I_p = I_{01(V_{p1})} e^{\frac{q}{kT} \frac{V_B - V_{p1}}{n(V_{p1})}} \quad (1-1)$$

Note that I_{01} depends on V_{p1} due to body effect

$$V_{p1} = V_B - n_{(V_{p1})} \frac{kT}{q} \ln \frac{I_p}{I_{01(V_{p1})}} \quad (1-2)$$

$$I_B = \frac{\beta_2}{2} [V_{p1} - V_{01} - V_{T(V_{01})}]^2 \quad (1-3)$$

$$V_{01} = V_{p1} - V_{T(V_{01})} - \sqrt{\frac{2I_B}{\beta_2}} \quad (1-4)$$

$$V_{01} = V_B - n_{(V_{p1})} \frac{kT}{q} \ln \frac{I_p}{I_{01(V_{p1})}} - V_{T(V_{01})} - \sqrt{\frac{2I_B}{\beta_2}} \quad (1-5)$$

b) Φ_1 on, Φ_2 on

$$I_P = I_{01(V_{P1})} e^{\frac{q \cdot V_B - V_{P2}}{kT} n_{(V_{P2})}} \quad (1-6)$$

$$V_{02} = V_B - n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_P + I_C}{I_{01(V_{P2})}} - V_{T(V_{02})} - \sqrt{\frac{2I_B}{\beta_2}} \quad (1-7)$$

Difference: assuming $I_P \ll I_C$

$$V_{01} - V_{02} = n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_C}{I_{01(V_{P2})}} - n_{(V_{P1})} \frac{kT}{q} \ln \frac{I_P}{I_{01(V_{P1})}} - V_{T(V_{01})} + V_{T(V_{02})} \quad (1-8)$$

Even if M1 goes out of subthreshold operation, the exponential I-V characteristic can be retained provided that n is adjusted to yield the correct current. See appendix.

$$\begin{aligned} \ln \frac{I_C^{n_{(V_{P2})}}}{I_{01(V_{P2})}^{n_{(V_{P2})}}} - \ln \frac{I_P^{n_{(V_{P1})}}}{I_{01(V_{P1})}^{n_{(V_{P1})}}} &= \ln \frac{I_C^{n_{(V_{P2})}}}{I_P^{n_{(V_{P1})}}} \frac{I_{01(V_{P1})}^{n_{(V_{P1})}}}{I_{01(V_{P2})}^{n_{(V_{P2})}}} \\ &= \ln \frac{I_C^{n_{(V_{P1})}} \cdot I_C^{n_{(V_{P2})} - n_{(V_{P1})}}}{I_P^{n_{(V_{P1})}}} \frac{I_{01(V_{P1})}^{n_{(V_{P1})}}}{I_{01(V_{P2})}^{n_{(V_{P1})}} \cdot I_{01(V_{P2})}^{n_{(V_{P2})} - n_{(V_{P1})}}} \quad (1-9) \\ &= \ln \left[\left(\frac{I_C}{I_P} \right)^{n_{(V_{P1})}} \cdot \left(\frac{I_{01(V_{P1})}}{I_{01(V_{P2})}} \right)^{n_{(V_{P1})}} \cdot \left(\frac{I_C}{I_{01(V_{P2})}} \right)^{n_{(V_{P2})} - n_{(V_{P1})}} \right] \end{aligned}$$

Therefore;

$$V_{01} - V_{02} = \left\{ n_{(V_{P1})} \ln \frac{I_C}{I_P} + n_{(V_{P1})} \ln \frac{I_{01(V_{P1})}}{I_{01(V_{P2})}} + [n_{(V_{P2})} - n_{(V_{P1})}] \cdot \ln \frac{I_C}{I_{01(V_{P2})}} \right\} \frac{kT}{q} - V_{T(V_{01})} + V_{T(V_{02})} \quad (1-10)$$

which can be explained as four terms as follows;

$$\#1 \frac{kT}{q} n_{(V_{P1})} \ln \frac{I_C}{I_P} : \text{Signal}$$

$$\#2 \frac{kT}{q} n_{(V_{P1})} \ln \frac{I_{01(V_{P1})}}{I_{01(V_{P2})}} : \text{Offset due to body effect in M1}$$

$$\#3 \frac{kT}{q} [n_{(V_{P2})} - n_{(V_{P1})}] \cdot \ln \frac{I_C}{I_{01(V_{P2})}} : \text{Offset due to slope variation}$$

$$\#4 V_{T(V_{02})} - V_{T(V_{01})} : \text{Offset due to body effect in M2}$$

FPN results primarily from n-mismatch (on signal), secondarily from n-mismatch/ I_{01} -mismatch/ V_{T2} -mismatch (on offset terms).

C. On-chip calibration with column amplifier [15]

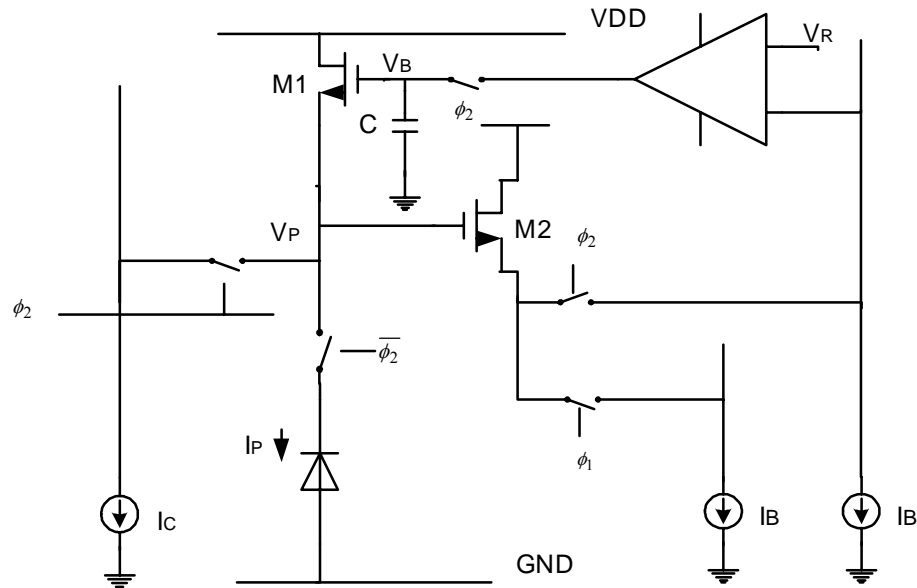


Figure 1-7 Schematic of on-chip calibration with column amplifier.

Reduction of FPN using a column amplifier is shown in Fig. 1-7. An evaluation for this configuration follows.

a) Calibration: Φ_1 off, Φ_2 on

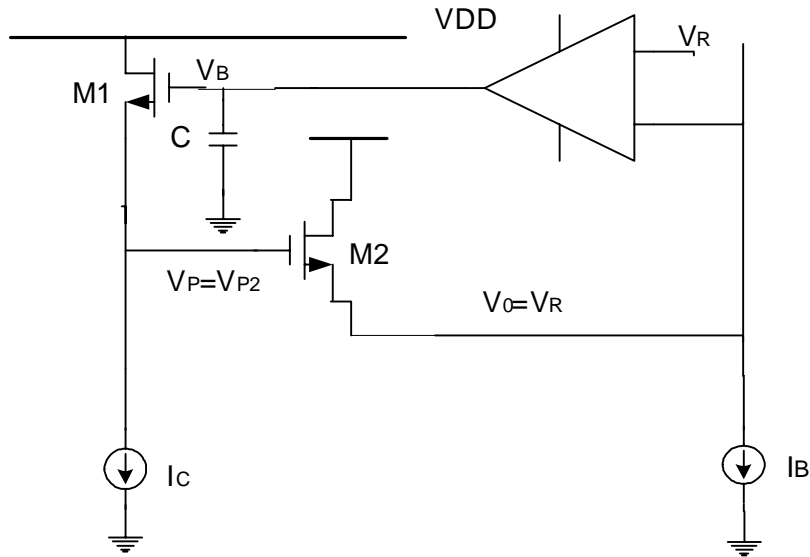


Figure 1-8 On-chip calibration with column amplifier when Φ_1 off, Φ_2 on.

Figure 1-8 shows calibration mode when Φ_1 is off and Φ_2 on. Now, we are going to derive what the output column voltage looks like at this particular mode.

$$V_B = V_R + V_{T2(V_R)} + \sqrt{\frac{2I_B}{\beta_2}} + V_{GS1} \quad (1-11)$$

$$V_{GS1} = n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_C}{I_{01}(V_{P2})}$$

$$V_B = V_R + V_{T2(V_R)} + \sqrt{\frac{2I_B}{\beta_2}} + n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_C}{I_{01(V_{P2})}} \quad (1-12)$$

This V_B is stored at node C.

b) Readout: Φ_1 on, Φ_2 off

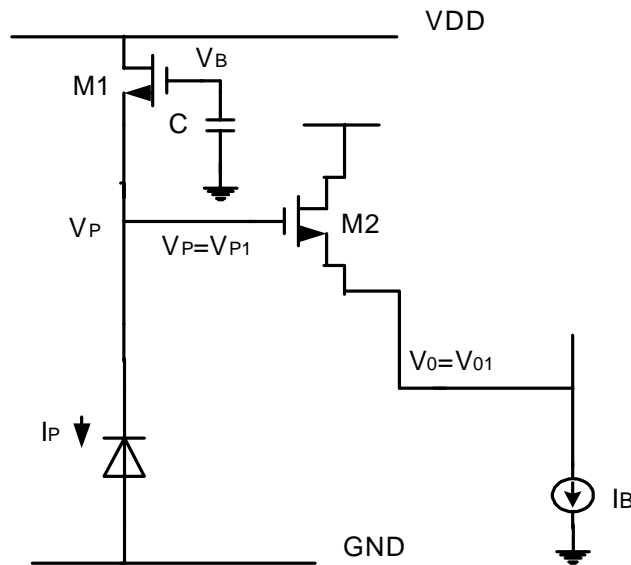


Figure 1-9 On-chip calibration with column amplifier when Φ_1 on, Φ_2 off.

Figure 1-9 shows calibration mode when Φ_1 is off and Φ_2 on. Derivation of output voltage at this mode follows.

$$V_{01} = V_B - n_{(V_{P1})} \frac{kT}{q} \ln \frac{I_P}{I_{01(V_{P1})}} - V_{T(V_{01})} - \sqrt{\frac{2I_B}{\beta_2}} \quad (1-13)$$

Therefore

$$V_{01} = V_R + V_{T2(V_R)} + \sqrt{\frac{2I_B}{\beta_2}} + n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_C}{I_{01}(V_{P2})} - n_{(V_{P1})} \frac{kT}{q} \ln \frac{I_P}{I_{01}(V_{P1})} - V_{T(V_{01})} - \sqrt{\frac{2I_B}{\beta_2}}$$

$$V_{01} - V_R = n_{(V_{P1})} \frac{kT}{q} \ln \frac{I_C}{I_P} + \frac{kT}{q} \left\{ n_{(V_{P1})} \ln \frac{I_{01}(V_{P1})}{I_{01}(V_{P2})} + [n_{(V_{P2})} - n_{(V_{P1})}] \ln \frac{I_C}{I_{01}(V_{P2})} \right\} + V_{T2(V_R)} - V_{T(V_{01})}$$
(1-14)

which is essentially the same as the preceding case. However, the input offset of the column amplifier adds directly to the signal ($V_R + V_{off}$ instead of V_R). A mismatch between the two column current sources also results in a signal offset. These appear as additional column wire FPN.

D. Calibration with in-pixel amplifier [16]

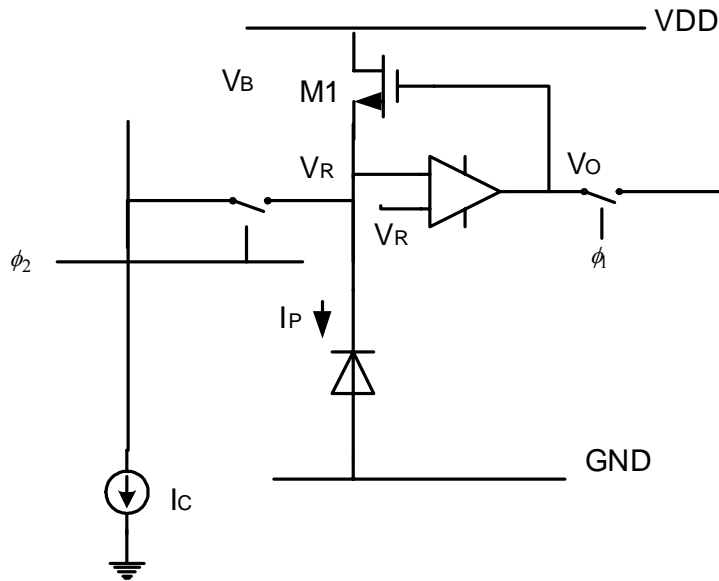


Figure 1-10 Logarithmic pixel with in pixel calibration amplifier.

Figure 1-10 shows a logarithmic pixel with in pixel calibration amplifier. Calibration procedure follows.

a) Φ_1 on, Φ_2 off

$$V_{01} = V_R + V_{GS1} = V_R + n_{(V_{01})} \frac{kT}{q} \ln \frac{I_P}{I_{01(V_R)}} \quad (1-15)$$

b) Φ_1 on, Φ_2 off

$$V_{02} = V_R + n_{(V_{02})} \frac{kT}{q} \ln \frac{I_C + I_P}{I_{01(V_R)}} \quad (1-16)$$

Therefore

$$V_{01} - V_{02} = \frac{kT}{q} n_{(V_{01})} \ln \frac{I_C}{I_P} + \frac{kT}{q} [n_{(V_{02})} - n_{(V_{01})}] \cdot \ln \frac{I_C}{I_{01(V_R)}} \quad (1-17)$$

Comparing this with the previous two techniques, we observe a better FPN performance in that #2 and #4 offsets of the previous are absent. Their matching is no more required.

E. Calibration with leakage current [17] (A clearly related precursor to [18])

Figure 1-11 shows another example of a logarithmic pixel with calibration technique. In this case, output voltage is calibrated by leakage current. Calibration procedure using this particular scheme is explained.

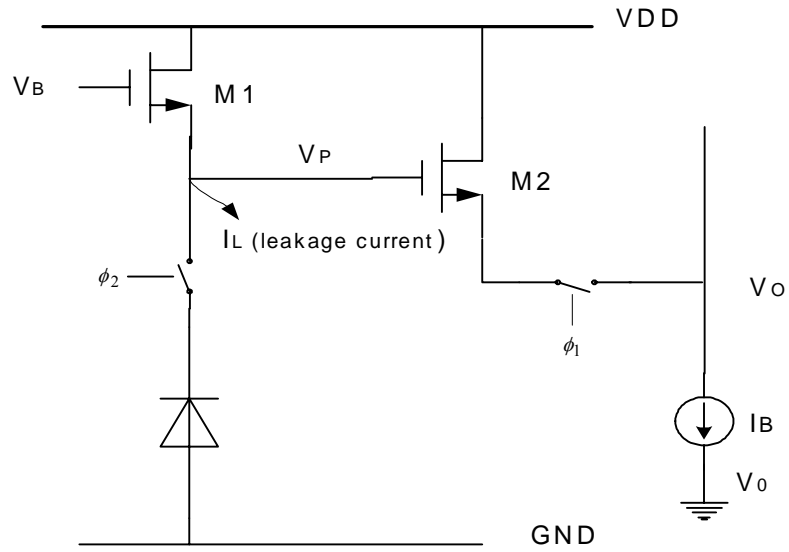


Figure 1-11 Logarithmic pixel with leakage current calibration.

a) Φ_1 on, Φ_2 on

$$V_{01} = V_B - n_{(V_{P1})} \frac{kT}{q} \ln \frac{I_P}{I_{01(V_{P1})}} - V_{T(V_{01})} - \sqrt{\frac{2I_B}{\beta_2}} \quad 1-18$$

b) Φ_1 on, Φ_2 off

$$V_{02} = V_B - n_{(V_{P2})} \frac{kT}{q} \ln \frac{I_L}{I_{01(V_{P2})}} - V_{T(V_{02})} - \sqrt{\frac{2I_B}{\beta_2}} \quad 1-19$$

$$V_{01} - V_{02} = \left\{ n_{(V_{P2})} \ln \frac{I_L}{I_{01(V_{P2})}} - n_{(V_{P1})} \ln \frac{I_P}{I_{01(V_{P1})}} \right\} \frac{kT}{q} - V_{T(V_{01})} + V_{T(V_{02})}$$

Therefore,

$$V_{01} - V_{02} = \left\{ n_{(V_{P1})} \ln \frac{I_L}{I_P} + n_{(V_{P1})} \ln \frac{I_{01(V_{P1})}}{I_{01(V_{P2})}} + [n_{(V_{P2})} - n_{(V_{P1})}] \cdot \ln \frac{I_L}{I_{01(V_{P2})}} \right\} \frac{kT}{q} - V_{T(V_{01})} + V_{T(V_{02})} \quad 1-20$$

This is a terrible compensation procedure because the I_L mismatch is very high.

1.2 Contributions

In this work, we focus on minimizing FPN which is known to be the major drawback to deteriorate the resolution of image sensor made by logarithmic pixels. We are going to show how our proposed circuit contributes to FPN reduction. To verify the FPN reduction performance of our circuit, mathematical analysis, spice simulation and testing results will be shown. Comparing previous works with respect to FPN, outputs of B, C, D and E provide first-order FPN reduction. The remaining signal FPN is due to slope (n) mismatch (term#1). In E, the first-order FPN reduction is expected to be the worst because term#1 depends not only on n but also I_L , which is a highly mismatching parameter. Outputs of B, C, D and E contain an offset term due to slope (n) variation (term#3). Mismatch of I_{01} and /or slope difference $[n_{(V_{P2})} - n_{(V_{P1})}]$ results in a secondary FPN. Outputs of B, C, and E also contain two affect terms due to body effect of M1 and M2 (term#2 and term#4). These result in additional secondary FPN due to mismatch. F doesn't have this additional FPN.

Another aspect of FPN performance, our proposed circuit consists of only two terms which are signal FPN (term#1) due to slope (n) mismatch and the offset term

(term#3) due to slope (n) variation. This kind of performance is shown by Graupner et. al. which is explained in section 1.1.3, example E. But our circuit has another advantage that it uses only one transistor in logarithmic transformation of photons which means more compact layout is available. Also it has random accessibility in both space and time as is common with sensors with logarithmic pixels. But slow response time still remains challenging problem to this circuit.

CHAPTER II

DESCRIPTIONS

2.1 Self-calibrating random-access logarithmic pixel

2.1.1 Topology

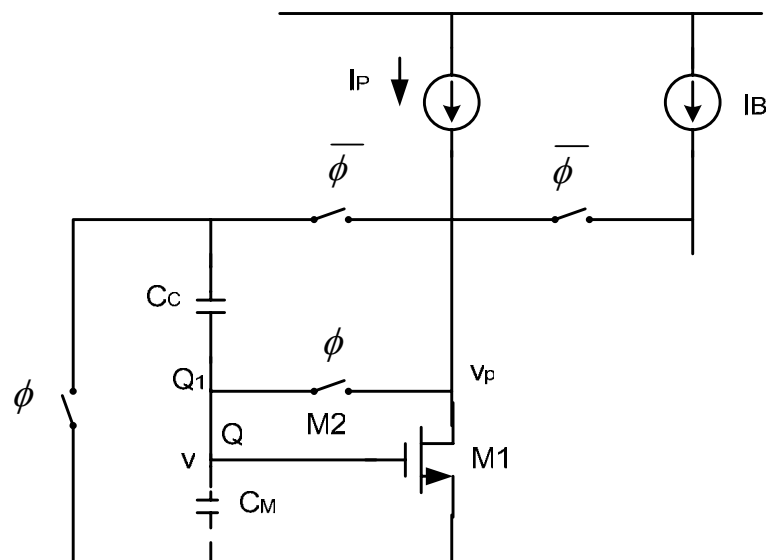
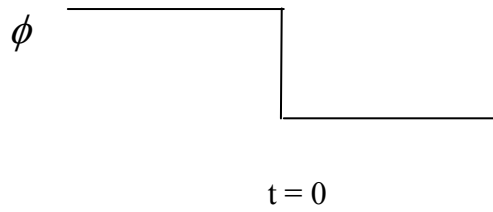


Figure 2-1 Topology of self-calibrating random access logarithmic pixel.

Figure 2-1 shows the original idea of our proposed pixel circuit. ϕ means a clock signal for switch and $\bar{\phi}$ is its complement. Clock signal for pixel operation is shown in Figure 2-2.

Figure 2-2 Clock signal ϕ

a) $t = 0^-$: Image acquisition mode

When clock is at high level, we call this state “image acquisition mode”. At this moment, column output voltage V_P can be expressed as equation (2-1). In the equation (2-1), n_1 is the value of n for $v_{GS1} = v_1(0^-) = v_P(0^-)$.

$$v_P(0^-) = v(0^-) = \frac{kT}{q} n_1 \ln \frac{I_P}{I_{O1}} \quad (2-1)$$

$$Q(0^-) = v(0^-)[C_{M1} + C_C] + [v(0^-) - V_{DD}] C_{OV2} \quad (2-2)$$

$$Q(0^-) = v(0^-)(C_{M1} + C_C + C_{OV2}) - V_{DD} C_{OV2}$$

We can also formulate the amount of charge at node P as equation (2-2) where C_{M1} is the value of C_M for $v_{GS1} = v_1(0^-) = v_P(0^-)$.

b) $t = 0^+$: Readout

When clock is at low level, we call this state “readout mode”. At this moment, charge at the gate of load transistor M1 can be expressed as equation (2-3).

$$Q(0^+) = v(0^+)C_{M2} + [v(0^+) - v_P(0^+)]C_C + v(0^+)C_{OV2}$$
(2-3)

$$Q(0^+) = v(0^+)(C_{M2} + C_C + C_{OV2}) - v_P(0^+)C_C$$

From charge conservation, we can relate two modes as equation (2-4).

$$Q(0^+) = Q(0^-) - \Delta Q$$
(2-4)

Substituting the results of (2-2) and (2-3) in equation (2-4) then we get equation (2-5).

$$\begin{aligned} & v(0^+)(C_{M2} + C_C + C_{OV2}) - v_P(0^+)C_C \\ &= v(0^-)(C_{M1} + C_C + C_{OV2}) - V_{DD}C_{OV2} - \Delta Q \end{aligned}$$
(2-5)

Also, $V(0^+)$ can be expressed as the equation (2-6)

$$v(0^+) = \frac{kT}{q} n_2 \ln \frac{I_P + I_B}{I_{O1}}$$
(2-6)

Replacing (2-5) with (2-6) for $v(0^+)$ and (2-1) for $v(0^-)$, we get the formulation for output voltage $V_P(0^+)$ as the equation (2-7).

$$\begin{aligned} v_P(0^+) &= \frac{C_{M2} + C_C + C_{OV2}}{C_C} \frac{kT}{q} n_2 \ln \frac{I_P + I_B}{I_{O1}} \\ &- \frac{C_{M1} + C_C + C_{OV2}}{C_C} \frac{kT}{q} n_1 \ln \frac{I_P}{I_{O1}} + \frac{C_{OV2}}{C_C} V_{DD} + \frac{\Delta Q}{C_C} \end{aligned}$$
(2-7)

C_{M2} is slightly smaller than C_{M1} because $v(0^+)$ is slightly larger than $v(0^-)$, and M1 is essentially in depletion. Ignoring this difference ($C_{M2} \cong C_{M1}$), we can reduce equation (2-7) to (2-8).

$$v_P(0^+) = \frac{CM_2 + C_C + C_{OV2}}{C_C} \frac{kT}{q} \left[n_2 \ln \frac{I_P + I_B}{I_{01}} - n_1 \ln \frac{I_P}{I_{01}} \right] + \frac{C_{OV2}}{C_C} V_{DD} + \frac{\Delta Q}{C_C} \quad (2-8)$$

Therefore, final result will be expressed as equation (2-9). This final result is composed of term#1 and term#3.

$$v_P(0^+) = \frac{CM_2 + C_C + C_{OV2}}{C_C} \frac{kT}{q} n_1 \ln \frac{I_P + I_B}{I_{01}} \quad (2-9)$$

$$- \frac{CM_1 + C_C + C_{OV2}}{C_C} \frac{kT}{q} (n_2 - n_1) \ln \frac{I_P + I_B}{I_{01}} + \frac{C_{OV2}}{C_C} V_{DD} + \frac{\Delta Q}{C_C}$$

2.1.2 Realization

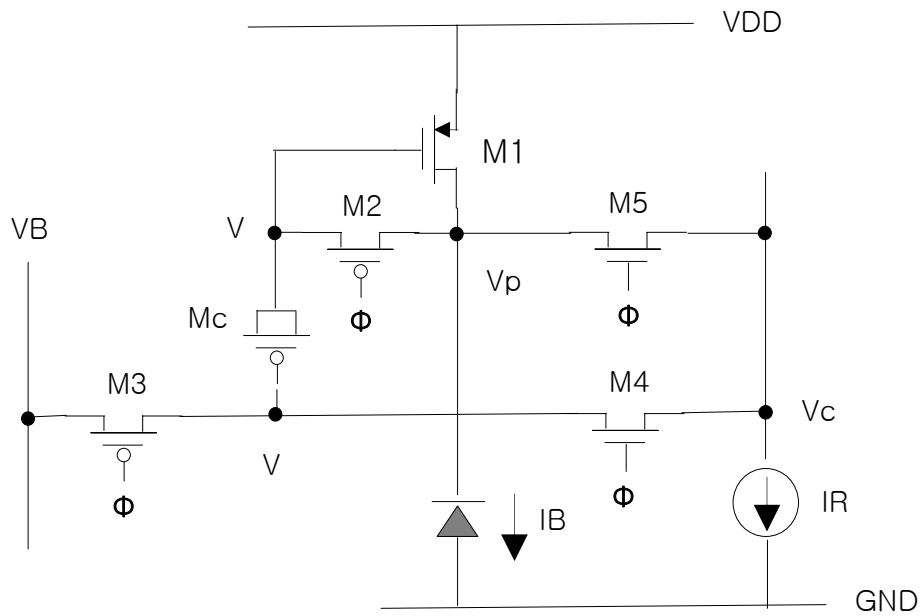


Figure 2-3 Realization of SRL pixel

In realizing pixel circuit as Figure 2-3, we decide to use sink type photodiode n+/p which has better efficiency than other photodiodes available in the CMOS process. Therefore, a PMOS transistor is used for the load transistor which is M1. Analytical aspects of how this pixel operates are shown below;



Figure 2-4 Scheme of clock signal ϕ for SRL pixel operation.

Figure 2-4 shows clock signal ϕ for the pixle operation which divides pixel operation into two different modes.

a) Image acquisition mode

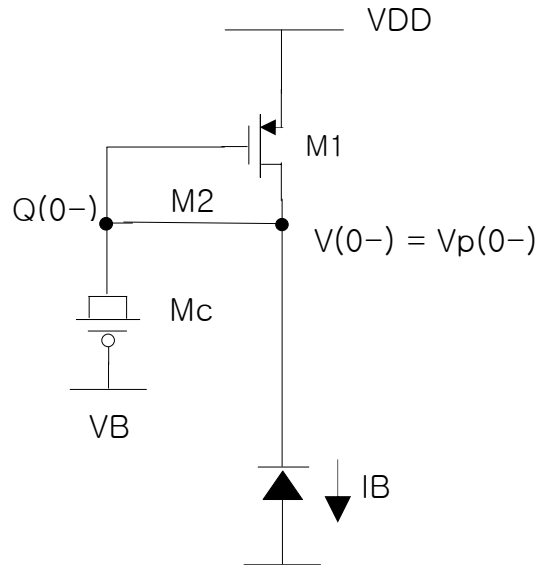


Figure 2-5 SRL pixel operation when $t = 0^-$.

From Figure 2-5, we can formulate the equation (2-10) and equation (2-11).

$$V(0^-) = V_p(0^-)$$

$$V_s(0^-) = V_B \quad (2-10)$$

$$I_B = I_0 e^{\frac{q}{nkT}[V_{DD} - V(0^-)]}$$

$$V(0^-) = V_p(0^-) = V_{DD} - n \frac{kT}{q} \ln \frac{I_B}{I_0} \quad (2-11)$$

$$Q(0^-) = -\overline{C_{oxc}}[V_B - V(0^-) - V_{TC}] + CV(0^-) \quad (2-12)$$

Also, the charge at the gate of load transistor M1 can be expressed as equation (2-12). Notice that we should guarantee MOSFET capacitor MC is in the inversion condition which means $V_B - V(0^-) - V_{TC} \leq 0$. Using the fact that the charge at the gate node of M1 should be conserved and ignoring charge injection, we can equate $Q(0^+)$ and $Q(0^-)$ which means $V(0^+) = V(0^-)$.

b) Readout mode

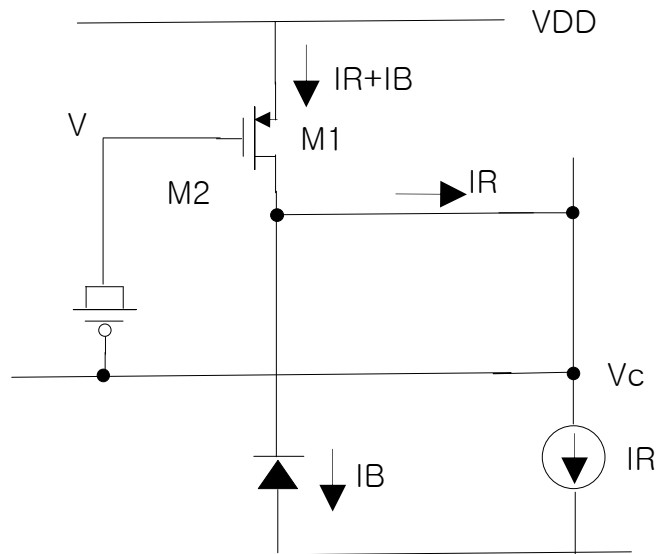


Figure 2-6. SRL pixel operation when $0^+ \leq t \leq t_1^-$.

Figure 2-6 shows a SRL pixel operation at readout mode. Here again, we can formulate the charge at the gate node of M1 as equation (2-13).

$$Q(t) = \overline{C_{oxc}}[V(t) - V_c(t) + V_{TC}] + CV(t) \quad (2-13)$$

Charge is conserved, hence $Q(t) = Q(0^+) = Q(0^-)$. This fact enables us to relate equations (2-12) and (2-13), which results in equations (2-14) and (2-15).

$$\overline{C_{oxc}}[V(t) - V_c(t) + V_{TC}] + CV(t) = \overline{C_{oxc}}[V(0^-) - V_B + V_{TC}] + CV(0^-) \quad (2-14)$$

$$V(t)[\overline{C_{oxc}} + C] - \overline{C_{oxc}}V_c(t) + \overline{C_{oxc}}V_{TC} = V(0^-)[\overline{C_{oxc}} + C] - \overline{C_{oxc}}V_B + \overline{C_{oxc}}V_{TC} \quad (2-15)$$

C and V_{TC} on the left-hand side are actually $C(t)$ and $V_{TC}(t)$ which is slightly different from $C(0^-)$ and $V_{TC}(0^-)$ which are C and V_{TC} on the right-hand side of equation (2-13). Also from exponential I-V characteristic in the subthreshold condition, we can formulate (2-16).

$$I_R + I_B = I_0 e^{\frac{q}{kTn}(V_{DD} - V(t))} \quad (2-16)$$

$$V(t) = V_{DD} - \frac{nkT}{q} \ln \frac{I_R + I_B}{I_0} \quad (2-17)$$

This n in equation (2-17) is slightly different from n appearing in (2-11) because VGS1's are different. Substitute (2-11)+(2-17) to equation (2-15) then we get equation (2-18).

$$\begin{aligned} & [V_{DD} - \frac{nkT}{q} \ln \frac{I_R + I_B}{I_0}][\overline{C_{oxc}} + C] - \overline{C_{oxc}}V_c(t) \\ & = [V_{DD} - \frac{nkT}{q} \ln \frac{I_B}{I_0}][\overline{C_{oxc}} + C] - \overline{C_{oxc}}V_B \end{aligned} \quad (2-18)$$

Therefore, final form of output column voltage can be expressed as equation (2-19).

$$V_B - V_C(t) = \frac{\overline{C_{OXC}} + C}{C_{OXC}} \frac{nkT}{q} \ln \frac{I_R + I_B}{I_B} \quad (2-19)$$

As seen from the analytical result above, we can obviously see that column voltage of each pixel results only from the signal (photocurrent). This is tremendous result because other previously made logarithmic pixels have several offset terms due to body effects of transistors and slope n variations which are main causes of fixed pattern noise. So our pixel possibly minimizes the FPN than any other logarithmic pixels ever made.

In order to operate MOSFET capacitor M_C in the inversion condition, checking inversion condition of M_C is needed. At image acquisition mode, inversion condition will be maintained as long as equation (2-20) is satisfied. For readout mode, we can formulate equation (2-21) in the same way as equation (2-20).

$$V_B - V(0^-) - V_{TC} \leq 0 \quad (2-20)$$

$$V_C(t) - V(t) - V_{TC} \leq 0 \quad (2-21)$$

$$V_B \leq V(0^-) + V_{TC} \quad (2-22)$$

Now, substituting (2-9) in (2-20), we get the condition to guarantee an inversion condition of M_C at image acquisition mode as equation (2-23). Worst case is when

$$I_B = I_{BMAX} \cdot$$

$$V_B \leq V_{DD} + V_{TC} - \frac{nkT}{q} \ln \frac{I_B}{I_0} \quad (2-23)$$

Substitute (2-11) to (2-22) then we get the equation (2-24) and equation (2-25).

$$\begin{aligned} V_C(t) - V(t) &= V_B - \frac{\overline{C_{OXC}} + C}{C_{OXC}} \frac{nkT}{q} \ln \frac{I_R + I_B}{I_B} - V_{DD} + \frac{nkT}{q} \ln \frac{I_R + I_B}{I_0} \\ &= V_B - V_{DD} - \frac{nkT}{q} \ln \frac{I_R + I_B}{I_B} \left(\frac{\overline{C_{OXC}} + C}{C_{OXC}} - 1 \right) \end{aligned} \quad (2-24)$$

$$V_C(t) - V(t) = V_B - V_{DD} - \frac{nkT}{q} \frac{C}{C_{OXC}} \ln \frac{I_R + I_B}{I_B} \quad (2-25)$$

Substitute (2-25) to (2-21) then we get the condition to guarantee inversion condition of M_C at readout mode as equation (2-28). At readout mode, worst case happens when

$$I_B = I_{B\min}$$

$$V_C(t) - V(t) = V_B - V_{DD} - \frac{nkT}{q} \frac{C}{C_{OXC}} \ln \frac{I_R + I_B}{I_B} \quad (2-26)$$

$$V_B - V_{DD} - \frac{nkT}{q} \frac{C}{C_{OXC}} \ln \frac{I_R + I_B}{I_B} - V_{TC} \leq 0 \quad (2-27)$$

$$V_B \leq V_{DD} + V_{TC} - \frac{nkT}{q} \frac{C}{C_{OXC}} \ln \frac{I_R + I_B}{I_B} \quad (2-28)$$

2.1.3 Spice simulations

Now we have so far proved analytically how our proposed pixel operates better than other logarithmic pixels. To further support and verify the analytical results, Spice simulation is done using winspice. Netlist for winspice simulation is as follows;

```
.include t3cu-n&pmos.txt

m1 2 3 5 10 cmosp w=1.5u L=1.5U ad=1.35p pd=3.3u as=2.48p ps=6.3
m2 2 9 3 10 cmosp w=1.5u L=0.6U ad=1.35p pd=3.3u as=1.35p ps=3.3u
m3 4 6 13 10 cmosp w=1.5u l=0.6u ad=2.48p pd=6.3u as=2.48p ps=6.3u
m4 1 7 4 0 cmosn w=1.5u l=0.6u ad=2.48p pd=6.3u as=2.48p ps=6.3u
m5 1 8 2 0 cmosn w=1.5u L=0.6U ad=2.48p pd=6.3u as=2.48p ps=6.3u
m6 1 11 0 0 cmosn w=60u l=2u
m7 11 11 0 0 cmosn w=60u l=2u
m8 13 12 1 10 cmosp w=60u l=0.6u
m9 3 4 3 10 cmosp w=1.5u l=1.65u ad=1.35p pd=3.3u as=0 ps=0

*cc 3 4 10f

cp 2 0 50f

ib 2 0 1p

ir 10 11 1u

vb 13 0 2.5

vs 10 5 0
```

```

CL 1 0 2000f
vdd 10 0 5
v1 9 0 pulse 0 5 10n 2n 2n 10u
v2 6 0 pulse 0 5 10n 2n 2n 10u
v3 7 0 pulse 0 5 10n 2n 2n 10u
v4 8 0 pulse 0 5 10n 2n 2n 10u
vr 12 0 pulse 0 5 8n 2n 2n 10.02u
.tran 200p 11u
.options gmin=1e-18 itl5=1000000 itl1=300
.plot tran V(1)
.plot tran V(3)
.plot tran I(vs)
.END

```

This netlist includes simple current mirror (M6, M7) to copy reference current to column. Also, pmos switch (M8) is added which makes reference voltage V_B same with column voltage V_C when it's closed. Clock signal at the gate of M8 goes high at 8n and clock signal for other switches in pixel goes high at 10n second. This means that column voltage (V_C) and reference voltage (V_B) are initially same. Simulation results are as follows;

Fig.2-7 shows transient plot of column voltage when photocurrent is 1pA. As mentioned previously, column voltage starts from the reference voltage (2.5V this case)

and settle down to certain level which results from logarithmic transformation of photo current to voltage. This pixel is self-calibrating because output column voltage is calibrated in pixel by reference current. Also this pixel is randomly accessible because logarithmic pixels are non-integrating pixels.

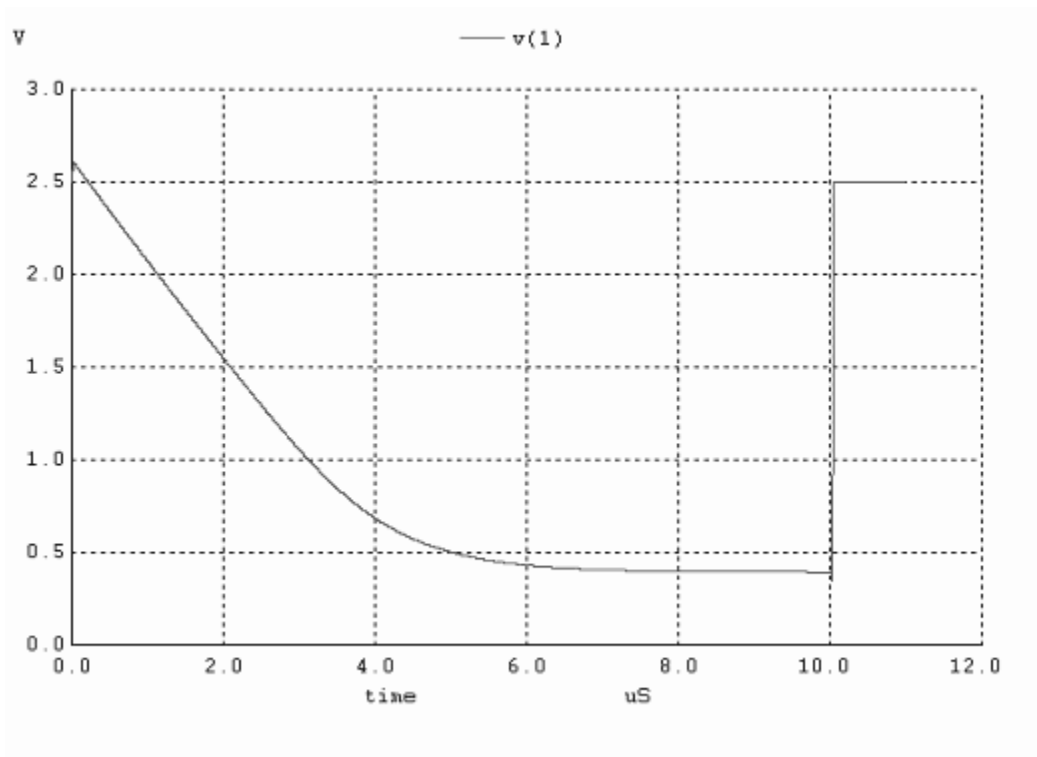


Figure 2-7 Transient column voltage V_C at readout mode.

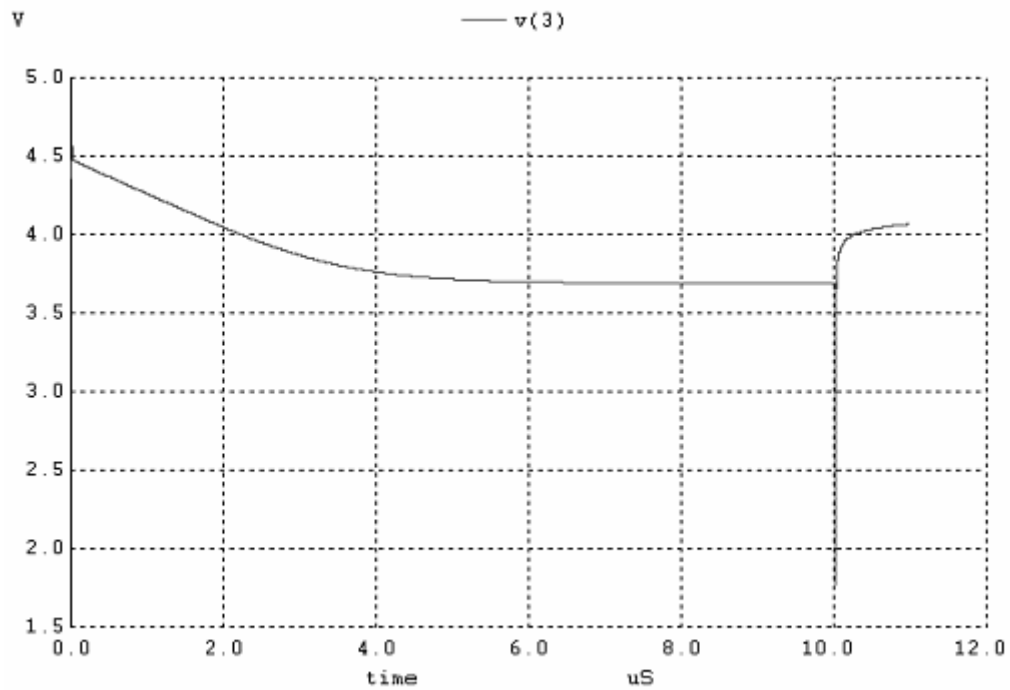


Figure 2-8 Transient gate voltage of load transistor M1.

From Fig. 2-8, we can guarantee the Mc operates at strong inversion condition which means Mc acts as a capacitor which has constant capacitance of $C_{ox} \times AREA$ (10fF).

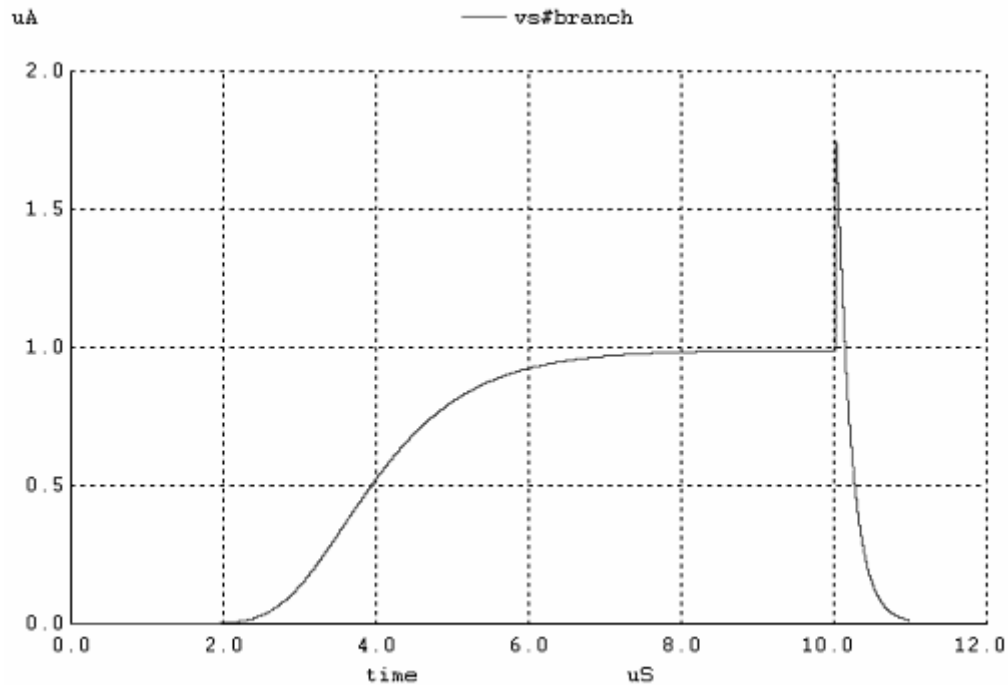


Figure 2-9 Transient currents flowing through M1 when $I_{\text{photo}}=1\text{pA}$.

Figure 2-9 shows transient currents flowing through load transistor M1. As we expected, currents change from 1pA to 1uA as clock goes high. Because of load capacitance of column itself ($C_L=2\text{pA}$ in this simulation), we can see some delays to reach desired values of column voltage or currents. So the actual capacitance of column in final layout will limit the speed of pixel circuit. Comparison to simulation results will be shown in Chapter III. Now, we know that pixel behaves as expected. There are two important tasks that we have to further look into. One is to check out dynamic range of this pixel which is the biggest advantage of logarithmic pixels and the other is to show how much the Fixed Pattern Noise can be reduced, which is the main purpose this research as mentioned. For FPN performance, we already showed its possible superiority

over other logarithmic pixels by theoretical analysis in previous sections. But this possibilities can only be verified by testing and evaluating the real chip and it will be shown in chapter III

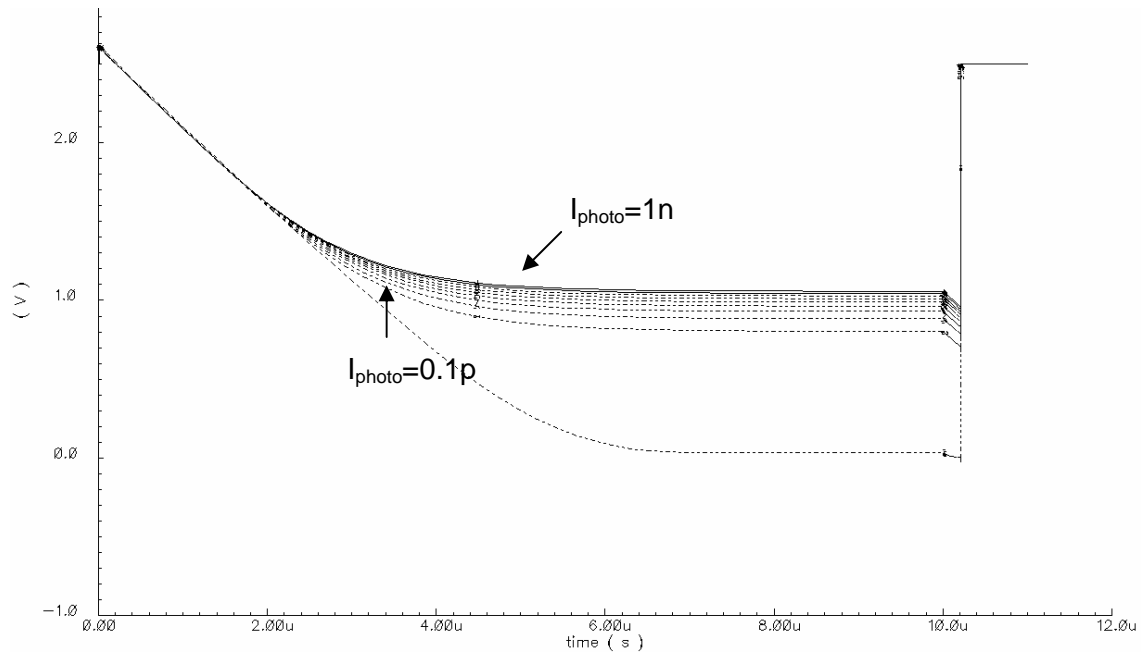


Figure 2-10 Transient column voltage V_C when $I_{\text{photo}}=0.1\text{p}\sim 1\text{nA}$.

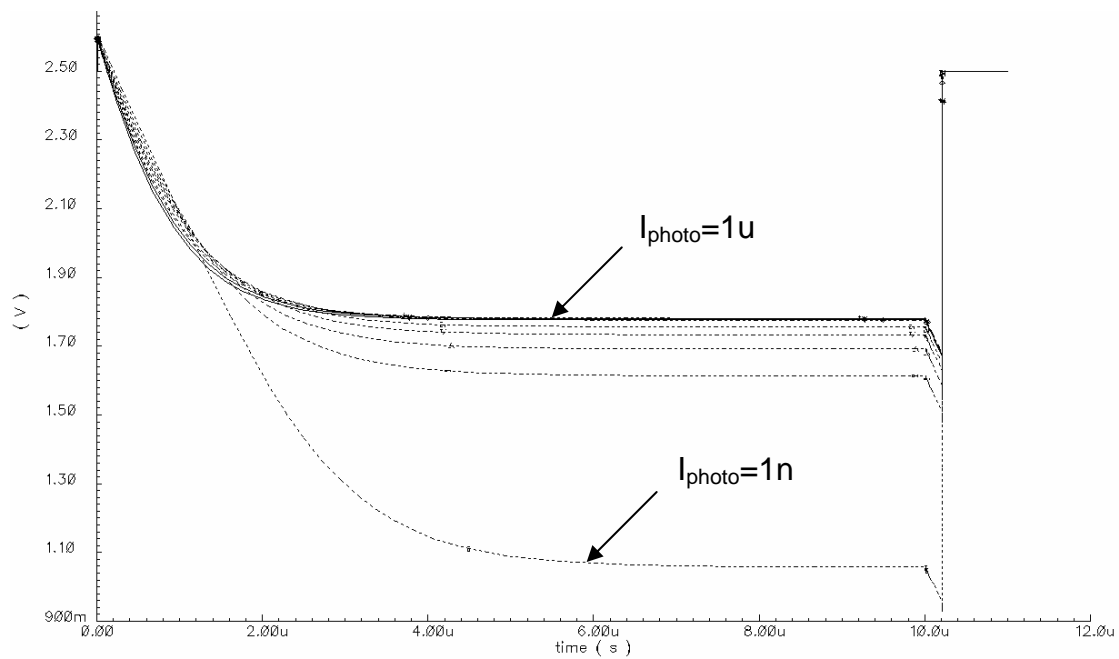


Figure 2-11 Transient column voltage V_C when $I_{\text{photo}}=1\text{n}\sim 1\mu\text{A}$.

Figure 2-10 and 2-11 show parametric simulation results using cadence. Column voltage V_C change from 0.1V to 1.8V as photocurrent changes from 0.1pA to 1uA. This means that our proposed pixel has dynamic range of more than six decades (120dB) which is an important feature to be used for outdoor environment.

Figure 2-12 and 2-13 shows transient currents flowing through M1 when photocurrents change from 0.1pA to 1uA (140dB). This shows that pixel behaves as we expected from theoretical analysis.

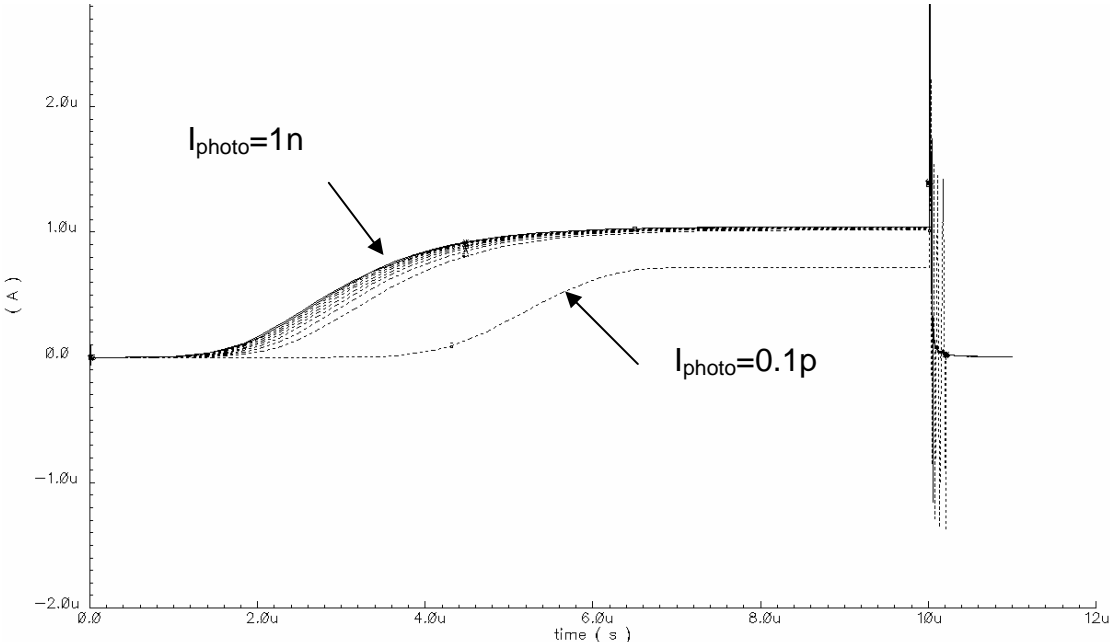


Figure 2-12 Transient currents flowing through M1 when $I_{\text{photo}}=0.1\text{p}\sim 1\text{nA}$

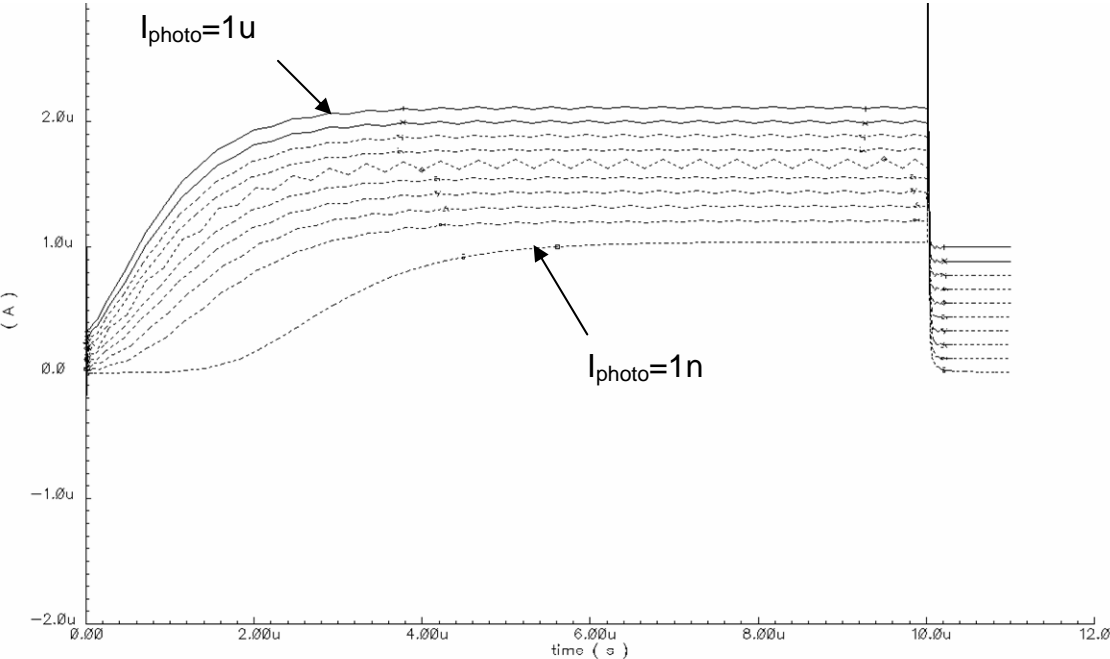


Figure 2-13 Transient currents flowing through M1 when $I_{\text{photo}}=1\text{n}\sim 1\text{uA}$.

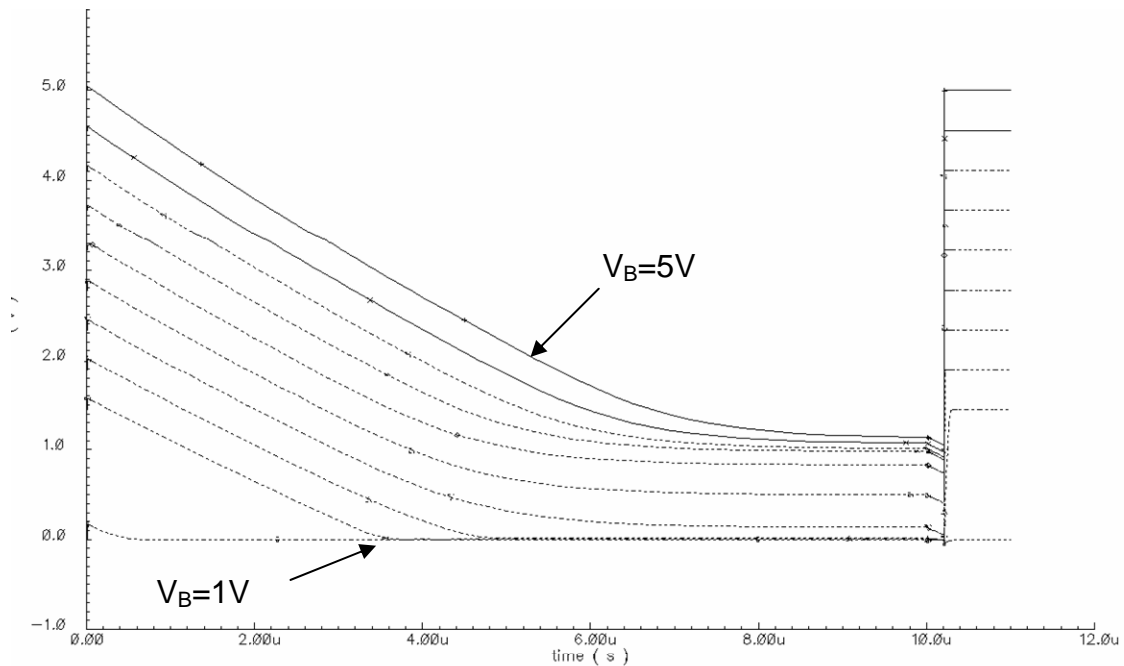


Figure 2-14 Column voltage V_C according to reference voltage V_B ($I_{\text{photo}} = 1\text{pA}$)

Figure 2-14 shows that column voltage is also influenced by reference voltage V_B and we know this intuitively from equation (2-19) in section 2.1.2. Note that V_B must be carefully chosen to make sure M_C is in strong inversion condition which makes upper limit of V_B according to equation (2-28) at read out mode.

Actually in the real chip, initial V_C is not set to V_B value as shown in Fig. 2-10 and Fig. 2-11 but GND because of current mirror attached to column. So transient V_C will be like Fig. 2-15 below.

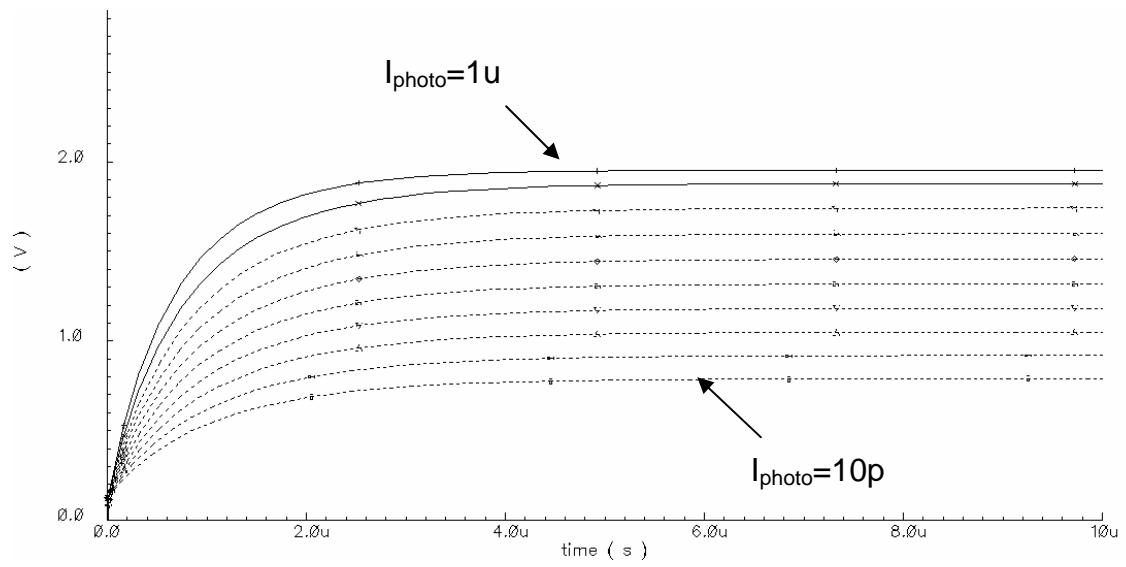


Figure 2-15 Spice simulation of column voltage VS photocurrent (10p to 1u).

2.2 MATLAB tool for analog circuit design

2.2.1 Objective

In designing analog circuits, one determines process variables (W, L, C, R, V, I etc.) by first doing analytical performance and secondly doing simulated performance. This helps reducing mismatch or underperformance of physical performance which otherwise can be extremely cost ineffective. A skillful and competitive designer should be able to interpret BSIM3 outputs and make an analytical model close to a simulated one. Here, I am supposed to invent a MATLAB tool that enables me to do analytical performance as fast and as close to simulated one as possible.

2.2.2 Extractor

First, I have been come up with the idea that “the tool must be universal to any process”. So I started from making a MATLAB tool that can read and process text files and actually store the parameter values which we want to use later in analog equations (ex. U0,K0,TOX etc.). I call this tool as an “extractor”.

One can easily see how this extractor works by simply running “extractor.m” file in the MATLAB. Once file is run, one can see all the variables at workspace and their values by clicking them. Notice that there is discernment between NMOS variables and PMOS variables (ex. nXJ and pXJ). This enables us to make analog equations for NMOS and PMOS separately. We will talk about these equations in next section. Here I

use “t3af-params.txt” which we are supposed to use in this class. But one may test any other process text and see results.

2.2.3 Analog equations

Open the file “analogequations.m”. I put NMOS equations and PMOS equations separately because we already have separate parameter names and values from “extractor”. Remember that all parameters that are used in these equations should have same names with parameters from “extractor”. Also notice that important variables (not parameters) are denoted as “syms” which means storing string as “symbol”.

2.2.4 Functions

For the automation and speeding up of the analytical performance. I made 3 kinds of functions as follows;

- solver
- nmulti & pmulti
- nev & pev

A) solver

For equations like below, we can solve this by using solver function.

$$VDSsat = (VGSTeff+0.0516)/1.27$$

Suppose we know V_{DSsat} and want to have V_{GSTeff} value. In MATLAB, we can't have V_{GSTeff} simply replace V_{DSsat} by certain value. So solver is very simple function that can solve this kind of situation. Solver function is simple but it is very useful. Later I become to know that there is function named "solve" given by MATLAB. But we don't feel any inconvenience using this so we will stick to this function.

Here is what solver looks like

```
function y=solver(a1,a2,a3);
```

```
f=a1-a2;
```

```
y=fzero(inline(char(f)),a3);
```

a_3 is the initial value of the y .

For example, V_{GSTeff} is calculated by above equations when $V_{DSsat}=0.10$. We can have V_{GSTeff} simply using solver as follows.

```
VGSTeff= solver(VDSsat,0.10,0)
```

which results in $V_{GSTeff}= 0.074939$

B) nmulti & pmulti

Once one gets V_{GSTeff} value, 5 variable values can be obtained which are V_{DSsat} , u_{eff} , V_{GS} , W_{eff}/L_{eff} , $g_m \cdot ID$. Here, nmulti or pmulti are supposed to be used to calculate 5 variables at once according to MOS type (nmulti for NMOS, pmulti for PMOS).

Here is the nmulti form:

```

function [oVDSsat, oueff, oVGS, oWLeff, ogmID] = nmulti(arg_VGSTeff, arg_ID)
    extractor
    analogequations
    oueff = subs(mueffn, VGSTeff, arg_VGSTeff);
    oVGS = solver(VGSTeffn, arg_VGSTeff, 1);
    oVDSsat = subs(VDSsatn, VGSTeff, arg_VGSTeff);
    temp = subs(IDn, {mueff, VGSTeff, VDSsat}, {oueff, arg_VGSTeff, oVDSsat});
    oWLeff = solver(temp, arg_ID, 1);
    ogmID = subs(gmIDn, VGSTeff, arg_VGSTeff);

```

pmulti function has exactly same form with nmulti except all 'n' notes being replaced to 'p' notes. Note that nmuli or pmulti itself doesn't give any results. We will see how to apply this in circuit design examples.

C) nev & pev

We know ueff, VGSTeff, VDSsat from nmulti or pmulti and we usually can determine VDS of device from specifications given for particular design. Then one should focus on the fact that now VAsat, VACLm, VADIBL, VA & rdsID are function of only Leff !!. So nev & pev function is made to relate VAsat, VACLm, VADIBL, VA & rdsID to Leff automatically for NMOS or PMOS. This function is important because in the circuit design, we have target value for output resistance (which means output resistance is given). And this output resistance consists of gm and rds. We know gm/ID

during design procedure and thanks to n_{ev} or p_{ev} , r_{ds} consists of only L_{eff} which means L_{eff} can be calculated from output resistance equation. We will see the practical example soon.

Here is the n_{ev} form:

```
function [VAsato, VACLMo, VADIBLo, VAo, rdsIDo] = nev(aVDS, aVGSTeff)
    extractor
    analogequations
    temp_ueff = subs(mueffn, VGSTeff, aVGSTeff);
    temp_VDSsat = subs(VDSsatn, VGSTeff, aVGSTeff);
    VAsato=subs(VAsatn,mueff,temp_ueff);
    VACLMo=subs(vACLMn,{VDS,VDSsat},{aVDS,temp_VDSsat});
    VADIBLo=subs(vADIBLn,VGSTeff,aVGSTeff);
    VAo=subs(vAn,{VAsat,vACLM,vADIBL},{VAsato,VACLMo,VADIBLo});
    rdsIDo=subs(rdsnIDn,{vA,VAsat,vACLM},{VAo,VAsato,VACLMo});
```

p_{ev} has the same form with n_{ev} except for using different notations to distinguish PMOS and NMOS.

2.3 Peripheral circuits

2.3.1 Overall chip schematic

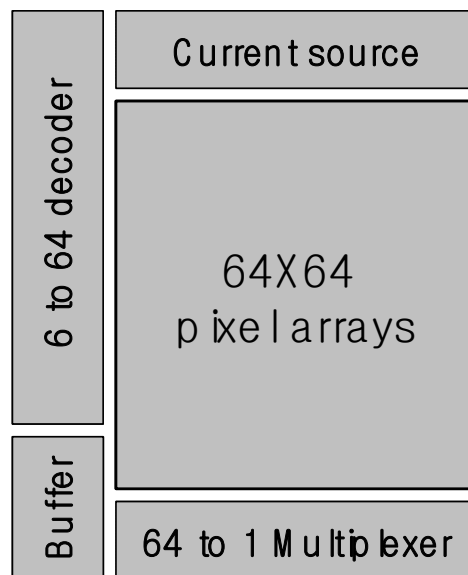


Figure 2-16 Overall chip schematic.

As we can see from Figure 2-16, our chip consists of five parts which are pixels, a Multiplexer, a decoder, current sources and a unity-gain buffer. Decoder and multiplexer are needed for the sake of X-Y addressing. By using these simple digital circuits, we can access to every single pixel and measure the column voltage that is critical to evaluate performance of each pixel. Here we are using 64 by 64 pixel arrays and digital circuits according to that because that is the maximum arrays possible for ami06 technology

provided by MOSIS educational runs. Eventually, the output that is supposed to be measured is output of multiplexer and we insert a unity gain buffer because usually probes used to measure outputs have capacitance of 10 to 20pF and we can't see the actual performance of the chip without buffer.

2.3.2 6 to 64 decoder

In order to be able to access one row at a time, I designed a 6 to 64 decoder. For digital parts like 6 to 64 decoder and 64 to 1 multiplexer in next section, we are not dealing with speed of these digital circuits. So I'm not going to show transistor level designs of these circuits because dimensions of transistors or the way of laying out circuits do not affect the performance of digital parts in this case. But I verified using cadence that all digital circuits operate properly in both schematics and final layouts. That is to say, transistor level schematic simulation, layout versus schematic (LVS) simulation and post layout simulations are executed for all peripheral circuits including analog parts. For the analog peripheral circuits, cascoded current mirror, source follower, unity gain buffer, detailed explanations in design procedures will be made because dimensions of every single transistor in analog circuits has influence on performance. Decoder consists of unit decoders which are 2 to 4 decoders. Schematic of 2 to 4 decoder is also given in Fig. 2-17.

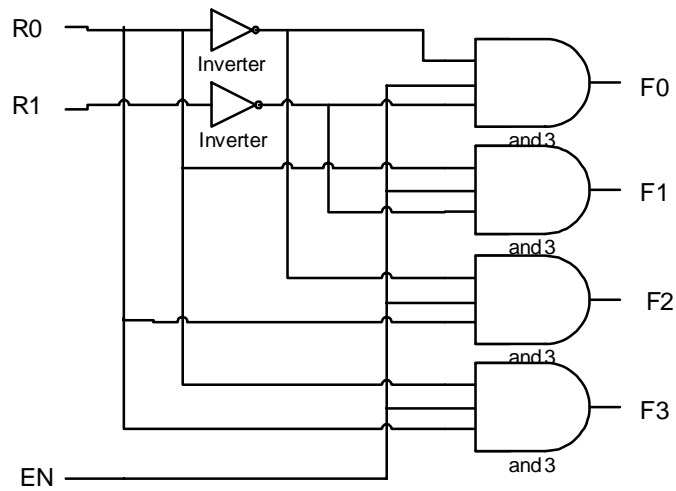


Figure 2-17 2 to 4 decoder.

As seen from the schematic, decoder has enable/disable logic because pixel needs to reset before being accessed. Logic of this circuit is obvious and simple as is given in Table 2-1.

Table 2-1 Truth table of 2 to 4 decoder.

EN	R0	R1	F0	F1	F2	F3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	X	X	0	0	0	0

Schematic of 6 to 64 decoder using 2 to 4 decoders is shown in Fig. 2-18.

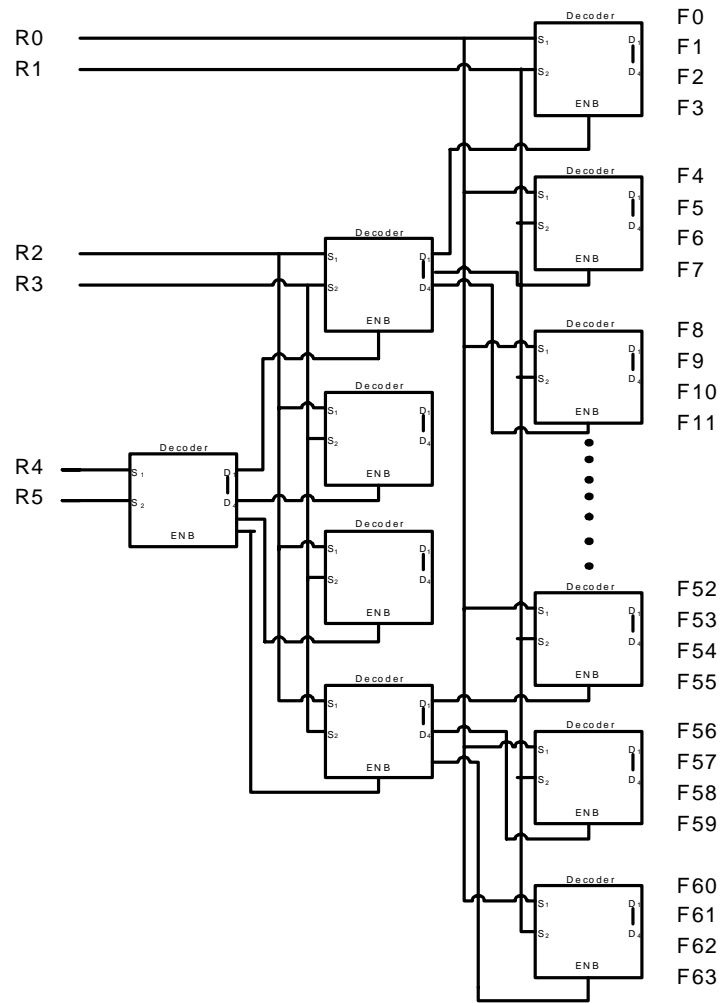


Figure 2-18 6 to 64 decoder.

2.3.3 64 to 1 multiplexer

Once one row is taken by decoder, clock signal is given and we have to measure the output column voltage V_C . In order to measure each column voltage at a time, I designed 64-to-1 multiplexer which consists of 4-to-1 unit multiplexers.

A multiplexer circuit has a number of data inputs to the output. The data input is selected by the values of the select inputs. Figure 2-19 shows a 2-to-1 multiplexer. I used multiplexer constructed with transmission gates because it is more compact in layout point of view than Sum-of-products form which consists of one NOT gate, two AND gates and one OR gate. Using three of this 2-to-1 multiplexer, 4-to-1 multiplexer can be made whose truth table is shown in Table 2-2. I used this 4-to-1 multiplexer as a unit cell for designing 64-to-1 multiplexer and schematic is shown in Figure 2-20.

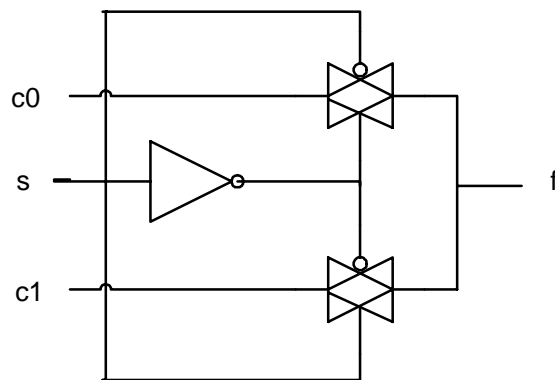


Figure 2-19 2-to1 multiplexer schematic using transmission gates.

Table 2-2 Truth table for 4-to-1 multiplexer.

S1	S0	f
0	0	C0
0	1	C1
1	0	C2
1	1	C3

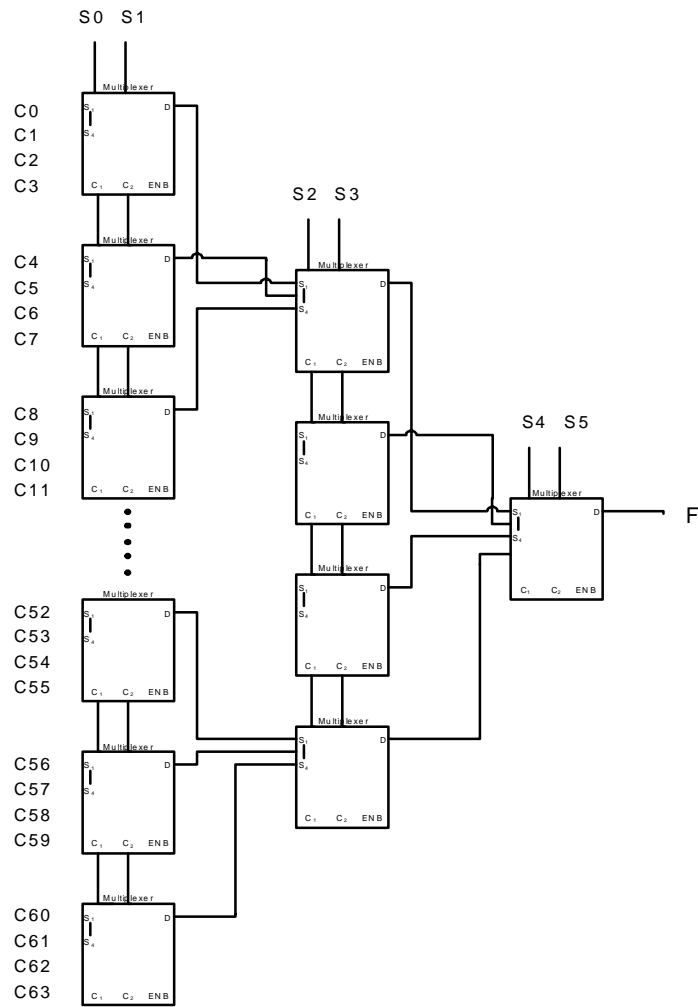


Figure 2-20 Schematic of 64-to-1 multiplexer

2.3.4 Low voltage cascoded current mirror

For exact copies of reference current (1 μ A) to every columns, I designed low voltage cascoded current mirror with 1G Ω output resistance at $V_{DC}=2.5V$ and 200mV compliance voltage when $I_D=1e-6$ as Figure 2-21. This kind of current mirror is needed where accurate copy of current and high output swing is required.

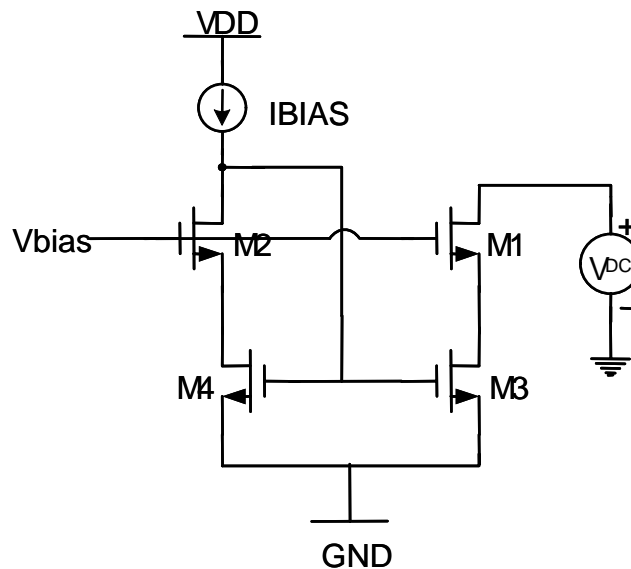


Figure 2-21 Low voltage cascoded current mirror.

In determining transistor dimensions, I would like to demonstrate how MATLAB tool introduced in section 2.2 can be used to design analog circuit. M-file with brief explanations of every design step are as follows;

M-file

% extracting parameter from the text file

extractor

% Include general analog equations for NMOS & PMOS

analogequations

ID1 = 1e-6;

% Calculate VGSTeff using solver and VDSsat value of 0.10

VDSsatn=(VGSTeff+0.0516)/nAbulk;

VGSTeff1= solver(VDSsatn,0.10,0);

% Calculate VDSsat, ueff,VGS, gmID using nmulti

subs(mueffn,VGSTeff, VGSTeff1);

[VDSsat1, ueff1, VGS1, WLeff1, gmID1] = nmulti(VGSTeff1, ID1)

% Calculate Leff using nev and solver

VDS3=0.100001;

[VAsat3, VACLM3, VADIBL3, VA3, rdsID3] = nev(VDS3, VGSTeff1);

VDS4=2.40;

[VAsat4, VACLM4, VADIBL4, VA4, rdsID4] = nev(VDS4, VGSTeff1);

roID=(1+gmID1*rdsID3)*rdsID4;

Leff1=solver(roID,1000,1e-6)

MATLAB results are as follows;

$$VDSsat1 = 0.1000$$

$$ueff1 = 0.0447$$

$$VGS1 = 0.7591$$

$$WLeff1 = 2.4367$$

$$gmID1 = 14.8007$$

$$Leff1 = 1.5688e-006$$

From this results I could determine all four device dimensions as $W=4.35\mu$, $L=1.65\mu$. Same dimensions resulted from the assumption that $VDSsat$ for both M1 and M3 (due to compliance voltage limit) are 0.1V which means same $VGSTeff$ and same VGS. But same VGS only applies when there is no body effect. Actually in this case there is body effect for M1 and M2. So threshold voltage should be bigger and we've got to give bigger gate voltage to M1 and M2 in order to establish same $VGSTeff$ value as expected which I give 1.2V for bias voltage. Assuming VGS and VDS for M4, eventually all four transistors have dimension of $W=4.35\mu$, $L=1.65\mu$. Simulation results are shown in Fig. 2-22 to Fig. 2-24.

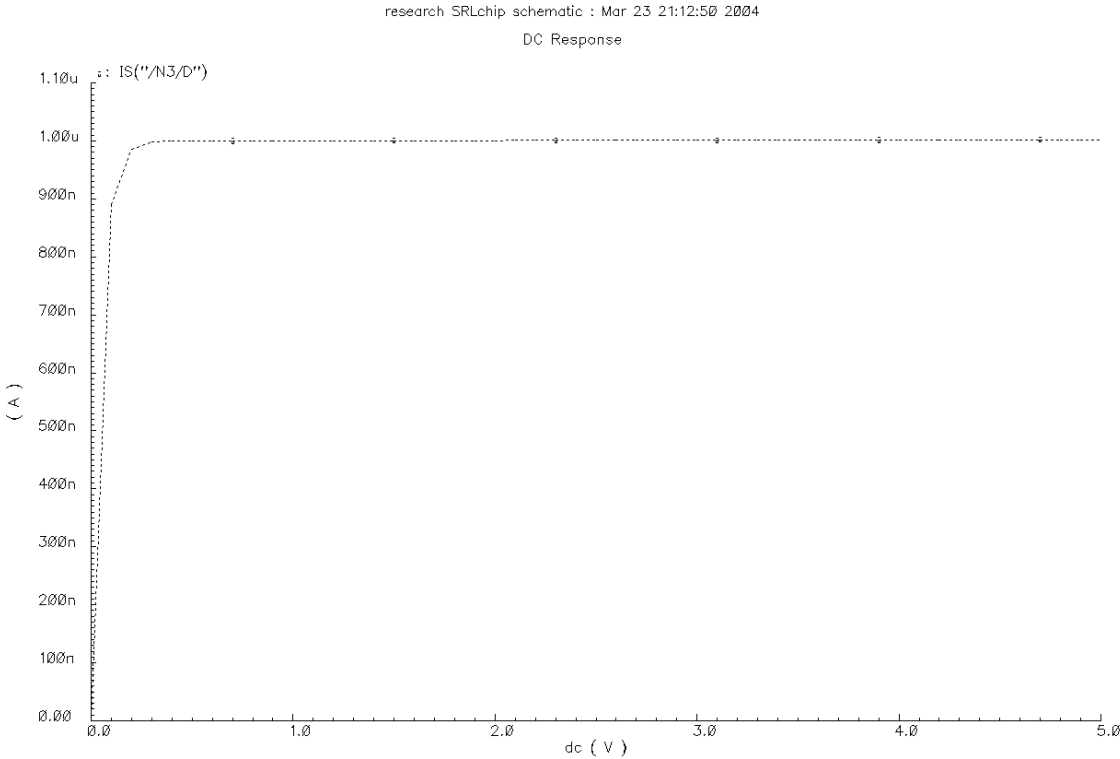


Figure 2-22 Output current as a function of output voltage.

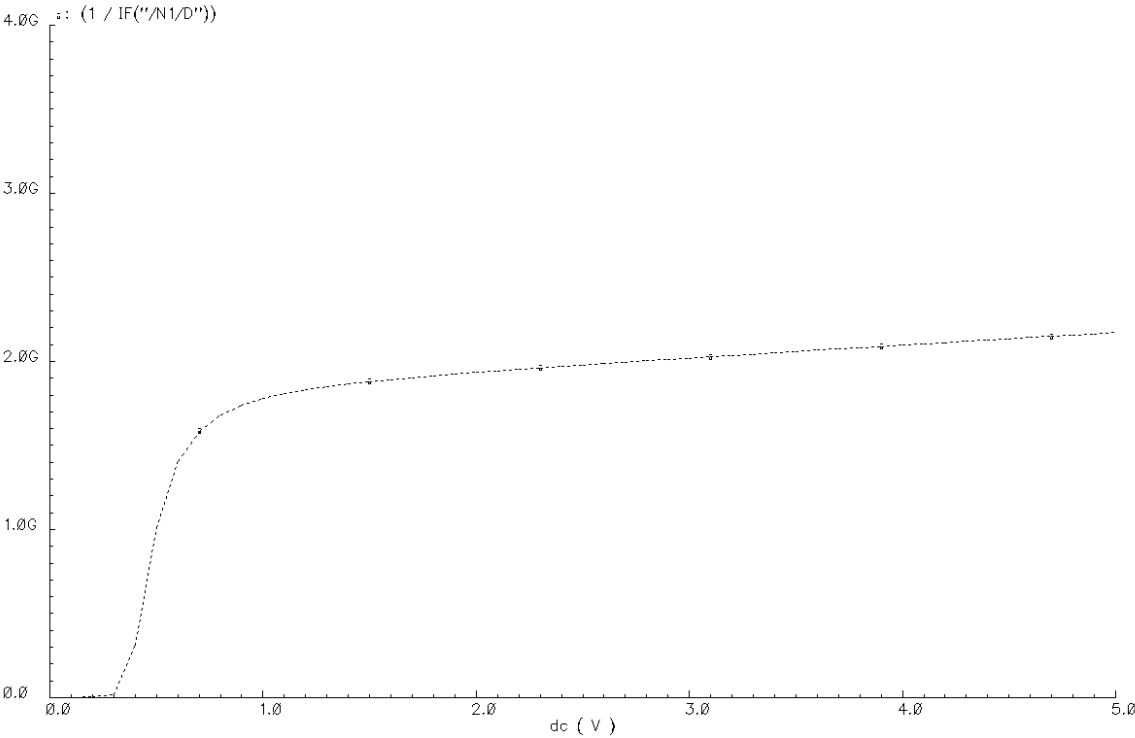


Figure 2-23 Output resistance characteristic as a function of output voltage.

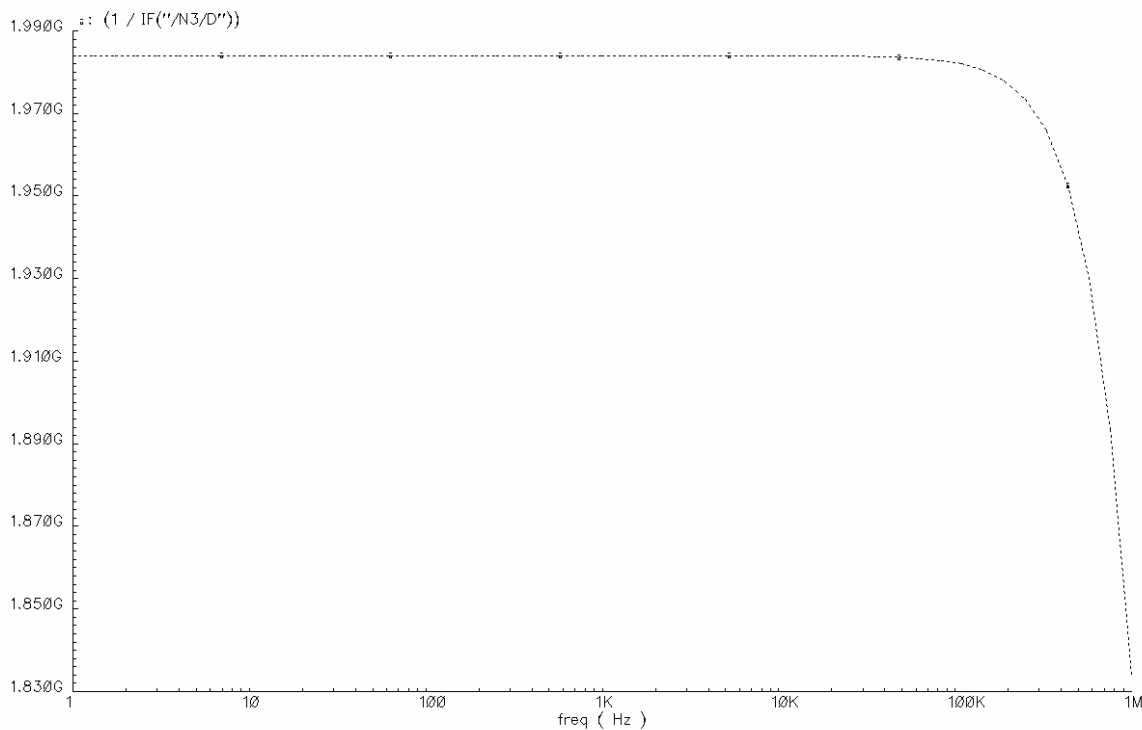


Figure 2-24 Output resistance characteristic as a function of frequency.

According to simulation results, compliance voltage is close to the target value (200mV). Actual V_{DSsat} of M1 is 91.87mV and 93.29mV for M3 which means compliance voltage is 185.16mV. Output resistance is 1.98G Ω at $V_O=2.5V$. Actual performance of current mirror is different with specifications we made. This might be caused from the different bias voltage we gave to gate of M1 and M2. But we leave it to that because all the results are better than what we expected.

2.3.5 Source follower

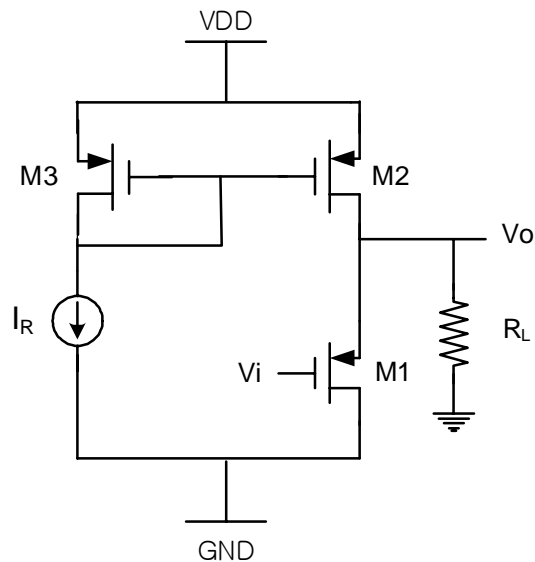


Figure 2-25 Source follower.

A PMOS source follower operating with $V_{DD}=5V$ and $V_{SS}=0V$, driving a load resistance of $R_L=1T\Omega$ is shown in Fig. 2-25. We select a huge value of R_L because the output of the source follower will be fed into the input of unity gain buffer which has huge resistance. M1 is driver whose bias current I_R is provided by mirroring from M3. The voltage gain which deteriorates as the input and output voltage increases, is specified as no less than $0.75V/V$ at $V_{in} = 2V$. Here, we demonstrated designing a source follower using MATLAB tool again. This source follower is used as boosting up the input DC level so that the signal with low input DC level can drive the buffer stage

without deteriorate the ac signal. And also by this example I could test the equations and functions for PMOS in MALAB tool whether it is working properly or not. And it really did work. What we did in this example was to give VGS value of p2 and VDSsat value of p1 and determines dimensions of devices. Here are M-file, MATLAB results and simulation results.

M-file

extractor

analogequations

VGS1=-1.5;

ID1=50e-6;

VGSTeff1 = subs(VGSTeffp,VGS,VGS1);

[VDSsat1, ueff1, VGS1, WLeff1, gmID1] = pmulti(VGSTeff1, ID1)

VDSsatp=(VGSTeff+0.0516)/pAbulk;

VGSTeff2= solver(VDSsatp,-1.0,-1);

subs(mueffp,VGSTeff, VGSTeff2);

[VDSsat2, ueff2, VGS2, WLeff2, gmID2] = pmulti(VGSTeff2, ID1)

MATLAB results;

$$V_{DSsat1} = -0.4061$$

$$u_{eff1} = 0.0139$$

$$V_{GS1} = -1.5000$$

$$W_{Leff1} = 13.0055$$

$$g_{mID1} = 3.2304$$

$$V_{DSsat2} = -1.0000$$

$$u_{eff2} = 0.0127$$

$$V_{GS2} = -2.2356$$

$$W_{Leff2} = 2.4856$$

$$g_{mID2} = 1.4758$$

Final device sizes are $W_1=5.1\mu$, $L_1=1.95\mu$ and $W_2=6.3\mu$ $L_2=0.6\mu$ and simulation results are shown in Fig. 2-26 and Fig. 2-27. Simulated voltage transfer characteristic is shown in Fig. 2-26, which indicates a input compliance voltage of 3.25V. Input voltage for the source follower will be the column voltage of SRL pixel which will vary between 0V to 2V according to photocurrent. So compliance voltage of 3.25V will be enough. Gain versus input voltage is given in Fig. 2-27, according to which, the gain at $V_{in} = 2V$ is 0.968.

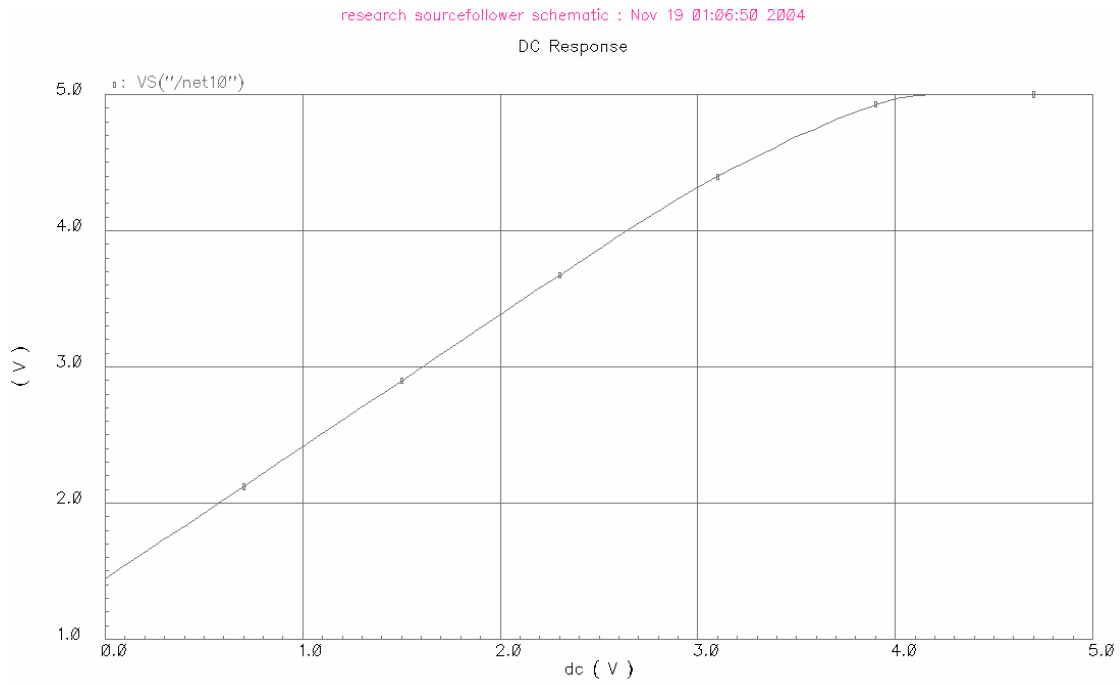


Figure 2-26 Voltage transfer characteristic

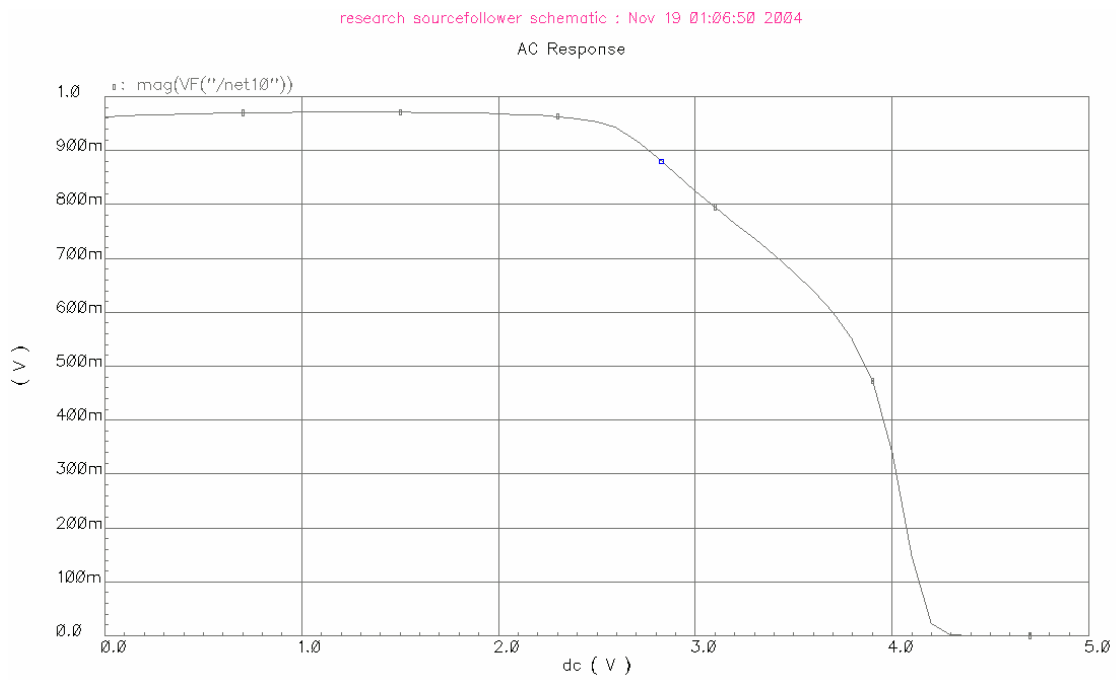


Figure 2-27 Gain as a function of input voltage.

2.3.6 Unity-gain buffer

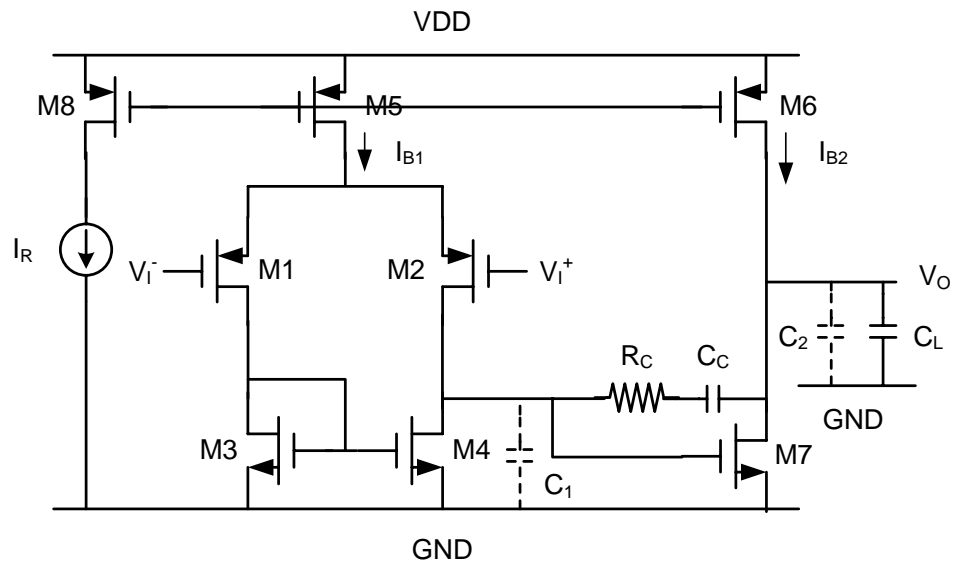


Figure 2-28 Two-stage operational amplifier for unity-gain buffer.

A lead-compensated two-stage opamp driving 20pF capacitive load is shown in Figure 2-28. Power supply levels are $V_{DD}=5V$ and $V_{SS}=0V$ (GND). Target specifications are in Table 2-3.

Table 2-3 Target specifications for a lead-compensated two-stage opamp.

Power consumption: $PD=1mW$	Phase margin: $PM=60^\circ$
Slew rate: $SR^+=SR^-=5V/\mu s$	Common-mode range: $CMR=\pm 1.0V$
Gain \times bandwidth: $GBW=8MHz$	DC voltage gain: $A_{V0}=85dB$

In designing this two stage opamp, exact dimensions of all transistors are calculated by using MATLAB tool as previously designed analog circuits. Unlike other analog circuits introduced in previous sections, I would like to introduce design strategy of this opamp so that one can understand how each device dimension is determined. This design strategy follows.

$$P_D = V_{DD}(I_{B1} + I_{B2}) \quad (2-29)$$

$$SR^+ = \frac{I_{B2} - I_{B1}}{C_2} \quad (2-30)$$

$$SR^- = \frac{I_{B1}}{C_C} \quad (2-31)$$

First, we determine I_{B1} , I_{B2} and C_C from equations (2-29), (2-30) and (2-31). Note that (2-30) contains the total output-node capacitance C_2 , which is the sum of the output capacitance associated with M5 and M7 and the load capacitance. The output capacitance of M5 and M7 can't be ascertained until the design is complete; so, we need to use an estimated value for it. Considering the fact that these are usually wide devices, a 1pF estimated value is reasonable. Calculated C_C value is 5pF with estimated C_2 value of 1pF. Next, we move to (2-32)

$$GBW = \frac{gm_{(1,2)}}{2\pi C_C} \quad (2-32)$$

Rewriting this equation as

$$\frac{gm_{(1,2)} I_{B1}}{I_{B1} / 2} = 2\pi \times GBW \times C_C \quad (2-33)$$

Use this equation to calculate $gm_{(1,2)} / (I_{B1} / 2)$, which enables us to determine $V_{GSTeff(1,2)}$, $V_{DSsat(1,2)}$, $\mu_{eff(1,2)}$, $V_{GS(1,2)}$ and $W_{eff(1,2)} / L_{eff(1,2)}$.

From equation (2-33), we calculate $gm_{(7)} / I_{B2}$ and then determine $V_{GSTeff(7)}$, $V_{DSsat(7)}$, $\mu_{eff(7)}$, $V_{GS(7)}$ and $W_{eff(7)} / L_{eff(7)}$. Here an estimated value for C_1 , again 1pF, is used.

$$\tan(90^\circ - PM) = \frac{C_1 C_2}{C_C^2} \frac{gm_{(1,2)}}{gm_{(7)}} \quad (2-34)$$

In order to avoid systematic offset, M3 and M4 must operate with the same drain-source voltage. Since $V_{DS(3)} = V_{GS(3,4)}$ and $V_{DS(4)} = V_{GS(7)}$, we need to design for $V_{GS(3,4)} = V_{GS(7)}$, hence $V_{GSTeff(3,4)}$ and $\mu_{eff(3,4)} = \mu_{eff(7)}$. Having already calculated $I_{B1} / 2$ flowing in M3 and M4, we can now determine $W_{eff(3,4)} / L_{eff(3,4)}$.

Note that M5, M6 and M8 have the same drain-source saturation voltage $V_{DSsat(5,6,8)}$ because their gate-source voltage is common. In this opamp configuration, CMR is limited from specification. For this reason, CMR specification is translated into $v_I|_{MAX}$ spec.

$$v_I|_{MAX} = V_{DD} + V_{GS(1)} + V_{DSsat(5)} \quad (2-35)$$

Since $v_I|_{MAX}$ is specified and $V_{GS(1)}$ has been calculated, we determine $V_{DSsat(5,6,8)}$ and set the width $W_{eff(8)}$ and current (I_R) of M8 to be identical to the dimensions and current of either M5 or M6. Up to this stage we have determined the effective aspect of all devices. Now, using gain specifications, we can determine the dimensions.

$$A_{V0,IN} = \frac{gm_{(1,2)}}{I_{B1}/2} \frac{I_{B1}}{2} (r_{ds(1,2)} // r_{ds(4)}) \quad (2-36)$$

$$A_{V0,OUT} = \frac{gm_{(7)}}{I_{B2}} I_{B2} (r_{ds(7)} // r_{ds(6)}) \quad (2-37)$$

Since $gm_{(1,2)}/(I_{B1}/2)$ and $gm_{(7)}/I_{B2}$ have already been calculated, we need to partition the overall gain into individual gains $A_{V0,IN}$ and $A_{V0,OUT}$ first, and use these two equations to determine the current \times resistance products, which will yield all channel lengths from the following equation in BSIM3 model.

$$rdsI_D = \frac{V_A}{1 - \frac{(V_A - V_{Asat})^2}{V_A V_{ACLM}}} \quad 2-10$$

where,

$$V_A = V_{Asat} + \frac{1}{\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}}} \quad 2-11$$

$$V_{Asat} = \frac{2 \times VSAT \times L_{eff}}{\left(\frac{2}{A2} - 1\right) \mu_{eff}} \quad 2-12$$

$$V_{ACLM} = \frac{L_{eff}}{PCLM \times l} (V_{DS} - V_{DSsat}) \quad 2-13$$

$$V_{ADIBL} = \frac{VGST_{eff} + 2 \frac{kT}{q}}{2 \times PDIBLC2} \quad 2-14$$

Note that the only variable in equation (2.) becomes L_{eff} . Once L_{eff} is calculated, we can finally determine dimensions of each device from aspect ratio we already have.

Gain partitioning has no primary effect on any target specification, but it can significantly affect the final size of the layout. For the gain partitioning, I proceeded with $A_{V0,IN} = 45\text{dB}$ and $A_{V0,OUT} = 40\text{dB}$. Needless to say, it is preferable to design for

$$\frac{I_{B1}}{2} r_{ds(1,2)} = \frac{I_{B1}}{2} r_{ds(4)} \quad \text{and} \quad I_{B2} r_{ds(6)} = I_{B2} r_{ds(7)}. \quad \text{Then from equation (2-8) and (2-9),}$$

$$\frac{I_{B1}}{2} r_{ds(1,2)} = \frac{I_{B1}}{2} r_{ds(4)} = 35.6\text{V} \quad \text{and} \quad I_{B2} r_{ds(6)} = I_{B2} r_{ds(7)} = 45\text{V}.$$

Compensation resistor R_C is given by

$$R_C = \left[1 + \frac{C_1 C_2 + (C_1 + C_2) C_C}{C_C^2} \right] \frac{1}{I_{B2} (g_{m(7)} / I_{B2})} \quad 2-15$$

Calculated compensation resistance is $15\text{k}\Omega$.

Final drawn width and length of all devices are shown in Table 2-5.

Table 2-4 Device dimensions for opamp.

	W (μm)	L (μm)	Gate area(μm^2)
M1	238.05	3.45	821.27
M2	238.05	3.45	821.27
M3	2.4	2.4	5.76
M4	2.4	2.4	5.76
M5	52.05	2.55	132.73
M6	158.85	2.55	405.07
M7	4.2	0.9	3.78
M8	52.05	2.55	132.73

Table 2-5 Simulation results.

Power consumption: PD=1mW	Phase margin: PM=59.36°
Slew rate: SR ⁺ =4.738V/ μs , SR ⁻ =3.437V/ μs	Common-mode range: CMR= $\pm 1.0\text{V}$
Gain \times bandwidth: GBW=6.76991MHz	DC voltage gain: A _{V0} =81.25dB

Simulation results are listed in Table 2-5. Actually, simulation results are close but not the same with target specifications. This is because trimming has not been done on the opamp which is general procedure for analog circuit. But fortunately, all results are seemed to be endurable for our application. Our pixel deals with low frequency signal and doesn't require high slew rate (more than 3V/ μs will be enough). So important specification will be the common mode input range which is identical with pixel output column voltage V_C . CMR of $\pm 1.0\text{V}$ will do for driving V_C . This work clearly shows how

important the analytical approach to analog design. Figure 2-29 shows magnitude and phase response of opamp. Figure 2-30 shows common mode range and slew rate can be obtained from the pulse response in Figure 2-31.

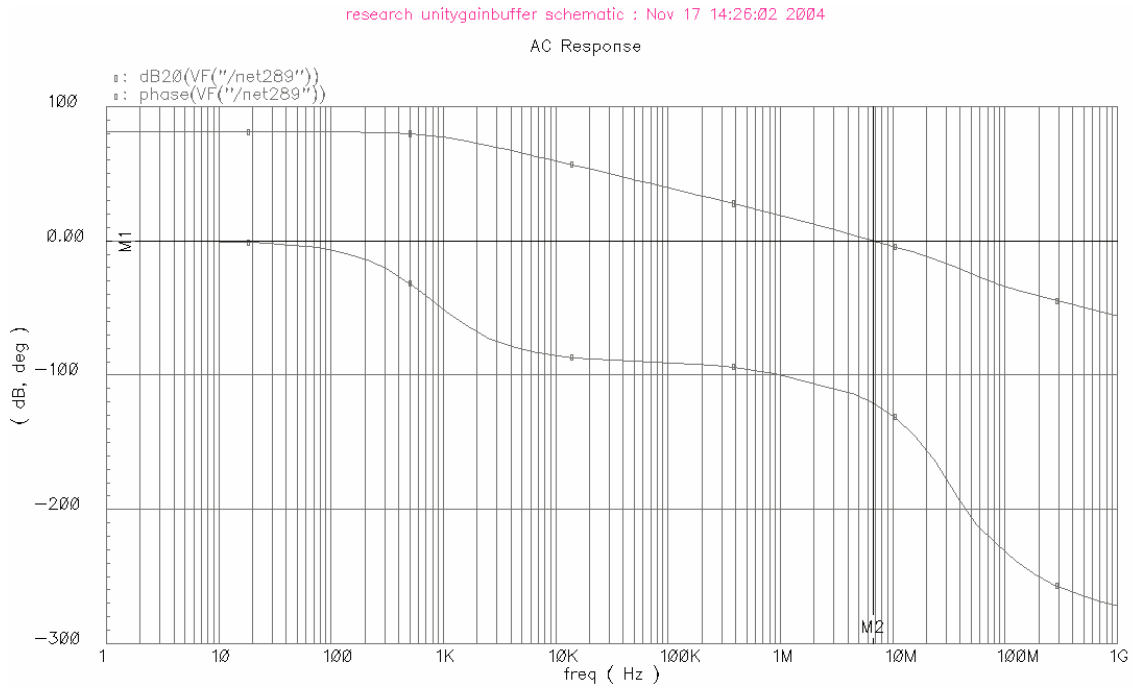


Figure 2-29 Magnitude & phase response of operational amplifier.

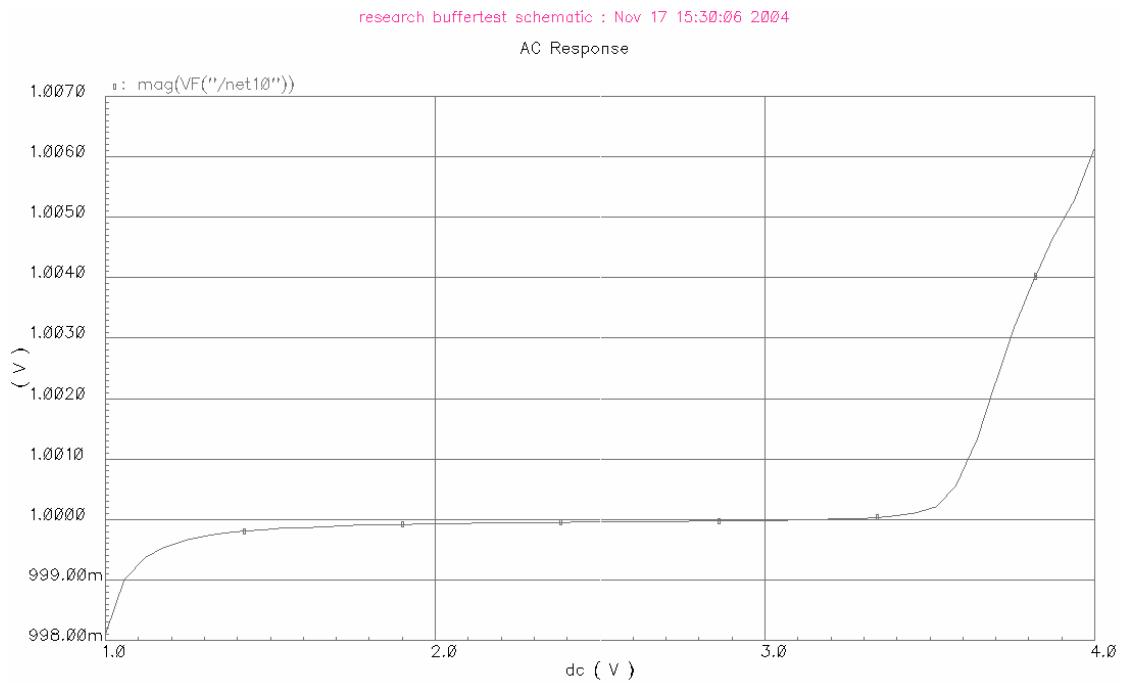


Figure 2-30 Gain versus common mode input in unity-gain buffer configuration.

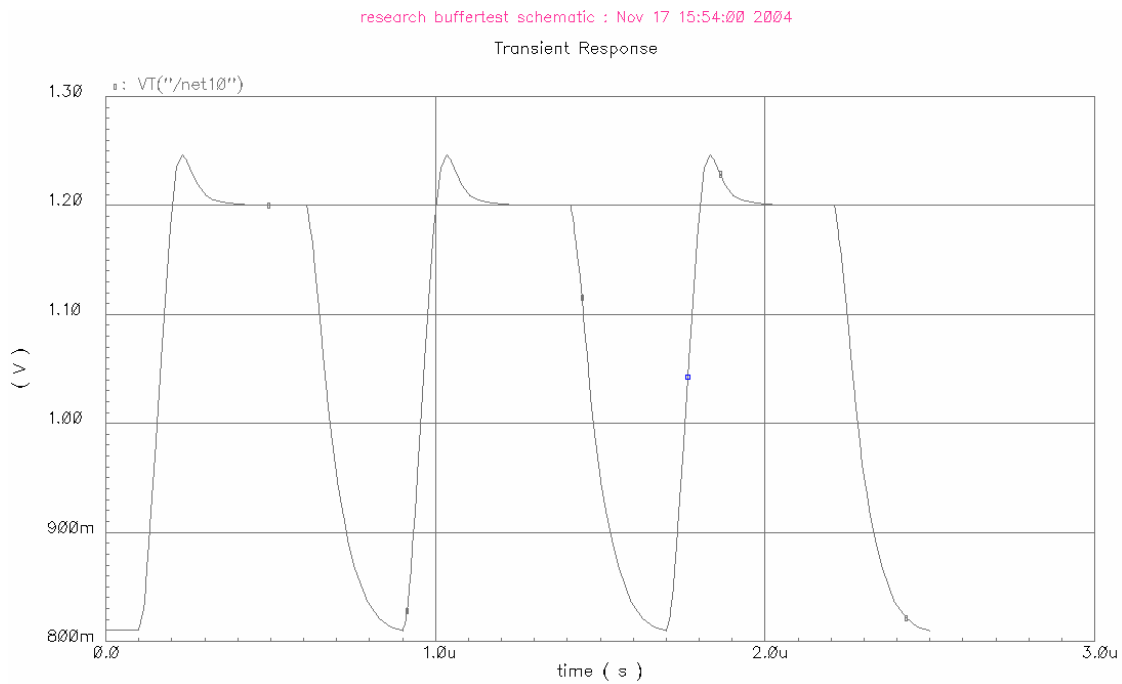


Figure 2-31 Output voltage in response to rail-to-rail differential input pulse.

2.4 Layouts

2.4.1 Pixel

The pixel layout is shown in Fig. 2-32. For the pixel, compactness is very important issue so the layout is completely customized to minimize the entire pixel layout. Two NMOS transistors (M4, M5) with common source are located in upper side of photodiode. Four PMOS transistors including load transistor (M1) placed in right side of photodiode. Note that to reduce dramatically the space occupied by poly to poly capacitor, we used the transistor (Mc) with source and drain tied together. Capacitance can be calculated from the C_{ox} value in testing results of particular process (AMIC5F this case) and area it occupies. We draw the layout to have a capacitance value of 10f F. But we also have to notice that Mc should always be in strong inversion condition to have constant value of $C_{ox} \times \text{area}$. Specifications for the pixel layout is shown in table 2-6.

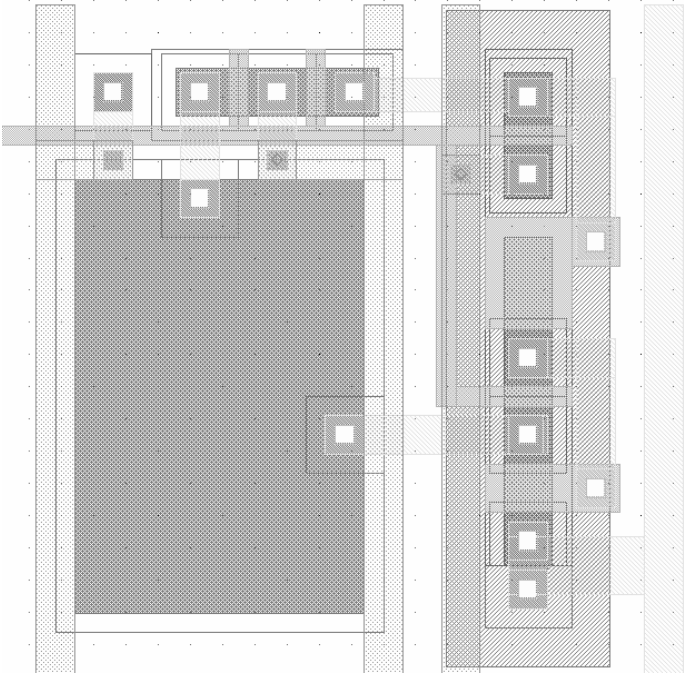


Figure 2-32 SRL pixel layouts.

Table 2-6 Specifications.

Total area	$18 \mu\text{m} \times 19.2 \mu\text{m}$
Photo Diode area	$9 \mu\text{m} \times 13.5 \mu\text{m}$
Fill factor (PD area/Total area)	35.156 %

2.4.2 Unity-gain buffer

For Unity-gain buffer layout in Figure 2-33, I used the poly1 to poly2 capacitor whose capacitance amounts to 5 p F for compensation and poly2 compensation resistor of 15K resistance. Next, post-layout simulations results are demonstrated in Figure 2-34 and Figure 2-35.

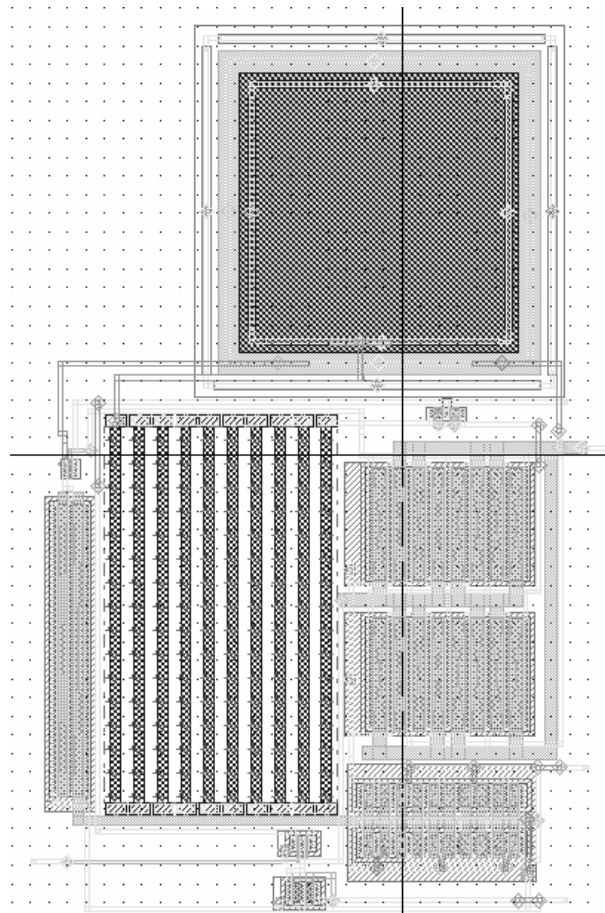


Figure 2-33 Layout of unity-gain buffer with source follower.

From simulation results, we can see that buffer works as we expected within common mode range we need (0~2V).

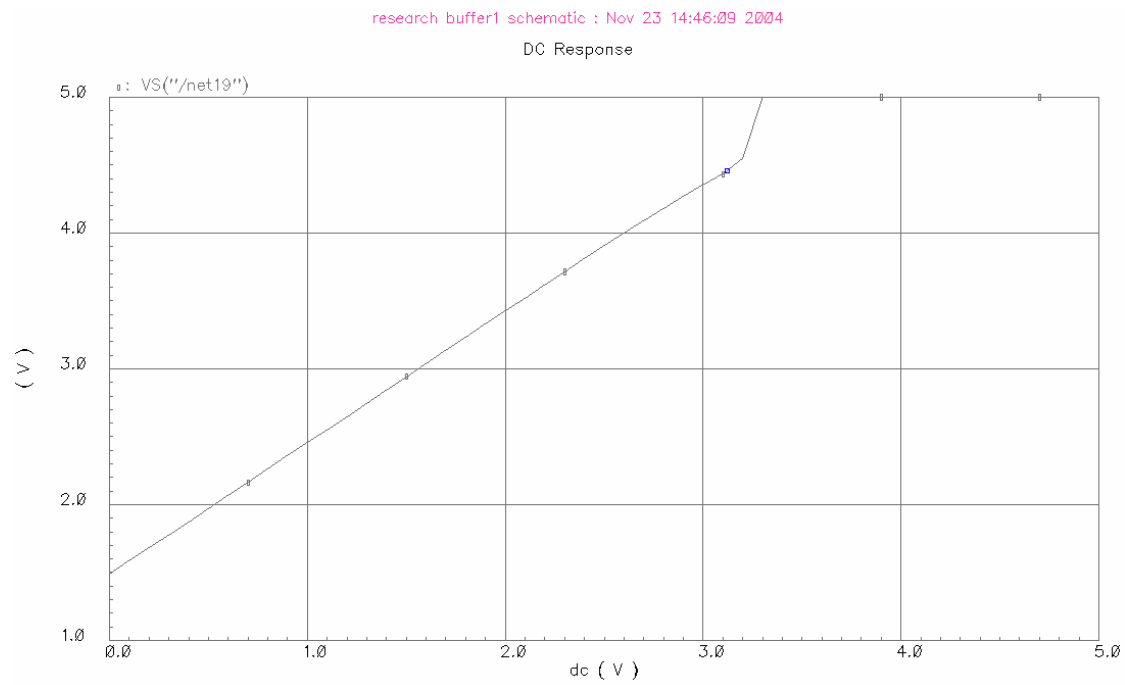


Figure 2-34 Output voltage versus input common mode range.

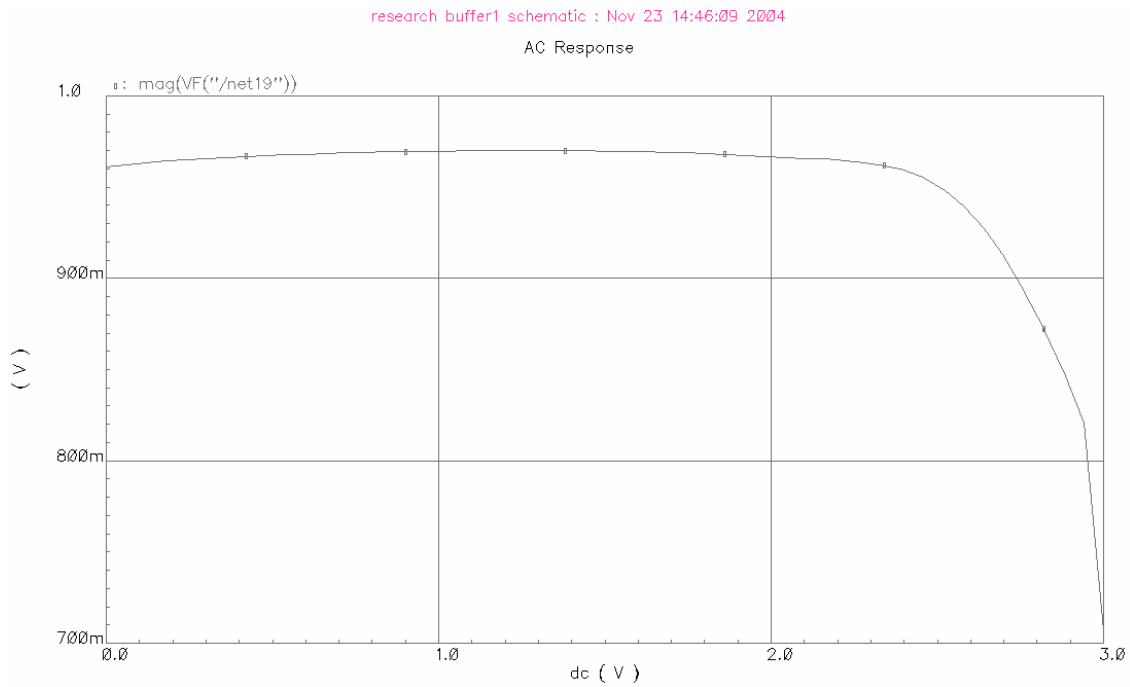


Figure 2-35 Gain versus input common mode range.

2.4.3 Overall chip layout

As mentioned in section 2.3.1, overall layout consists of Multiplexer, decoder, current source, current mirrors and unity-gain buffer. Addition to these features, a layout of a single pixel with current source is placed separately to see the behavior of a single pixel. In this separate pixel, simple source follower is used as buffer and a exact same source follower is also placed in actual layout in order to calibrate the actual column voltage of the pixel. Overall chip layout is shown in Figure 2-36.

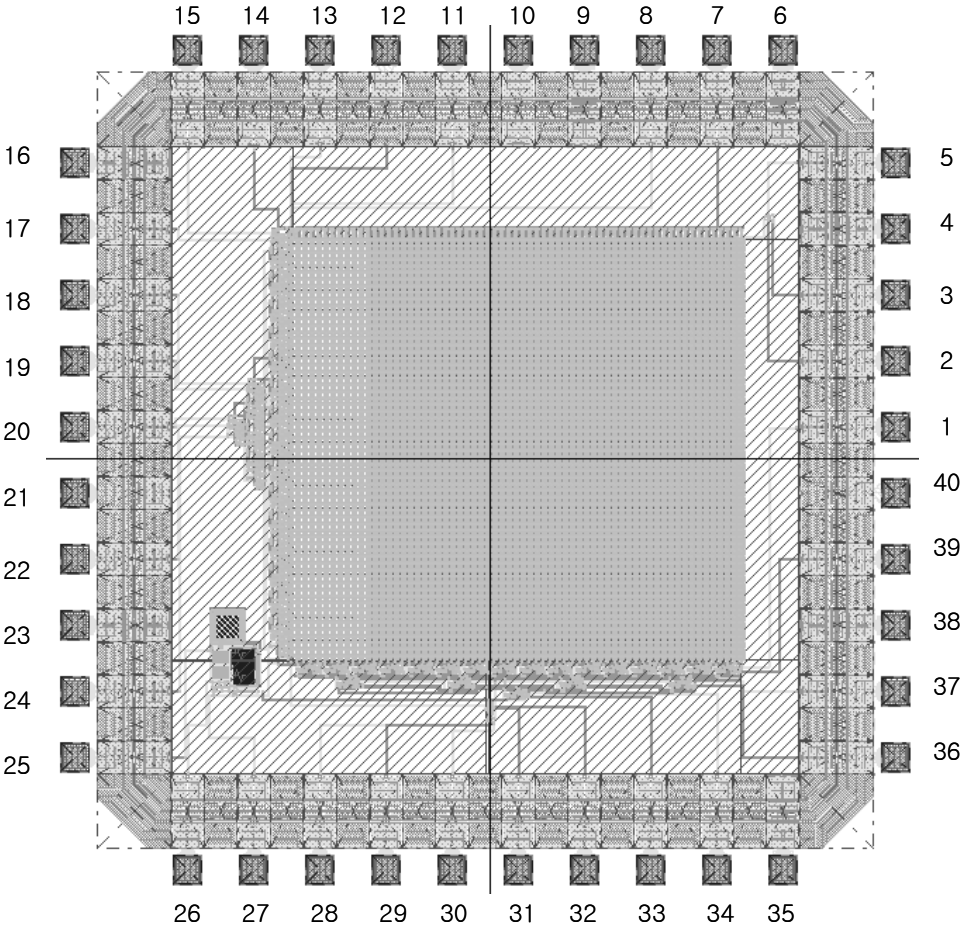


Figure 2-36 Overall chip schematic for SRL pixel.

The notations of pins are shown in Table 2-8.

Table 2-7 Pins & notations for operation.

Pin	Notation	
1,39,37,36,34,33	S0 ~ S5	Column select
15, 17 ~ 20, 22	R0 ~ R5	Row select
2	Vout2	Calibrating source follower output voltage
3	IBIAS6	Bias current for calibrating source follower
5	Vin	Input voltage for calibrating source follower
7	VB	Reference voltage for whole pixels
8	IBIAS3	Reference current for whole pixels
11	Vbias	Bias voltage for current mirror
12	GND	
13	Φ	Clock signal
14	VDD	
24	En	Enable for decoder
25	Vout	Column output voltage
26	IBIAS	Bias current for buffer
27	IBIAS2	Bias current for source follower
28	VC2	Column output voltage of separate pixel
29	VB2	Reference voltage for separate pixel
30	IBIAS4	Bias current for source follower (separate pixel)
31	Vbias2	Bias voltage for current mirror (separate pixel)
32	IBIAS5	Reference current for separate pixel

CHAPTER III

TEST AND EVALUATIONS

3.1 Test set up

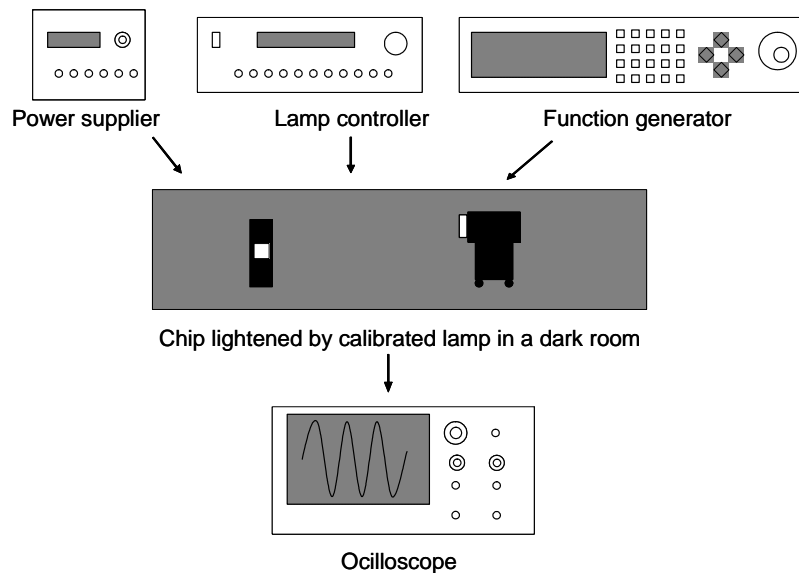


Figure 3-1 Block diagram for testing.

Figure 3-1 shows experimental set up for testing. Six power sources are used for properly biasing circuits. In order to calculate and generate exact amount of photocurrent, we have used a calibrated lamp and controller (GAMMA SCIENTIFIC, Model: RS-5) in a dark room. For input signal, a pulse generator is used for imposing pulse signal with $2n$ seconds rising and falling time and $10n$ seconds width. Output voltage is viewed through oscilloscope.

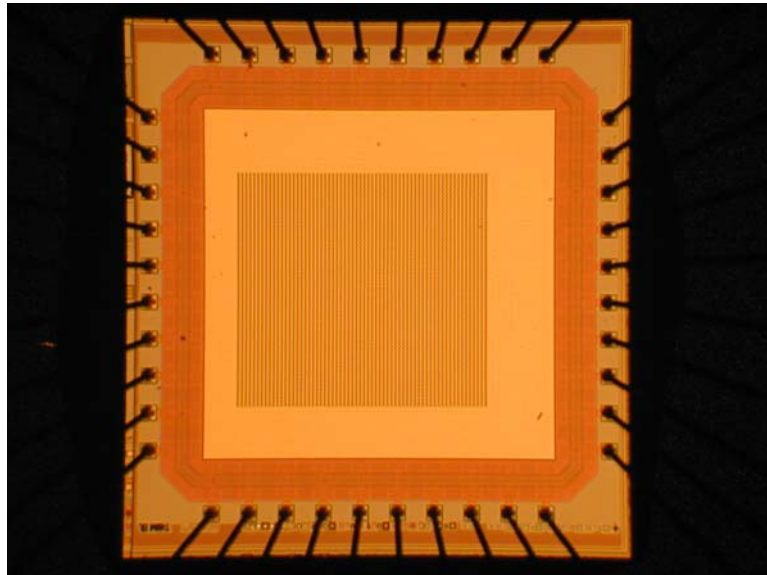


Figure 3-2 Chip microphotograph.

Chip microphotograph is shown in figure 3-2. Chip is fabricated by AMI_06 with 3 metal 2 poly technology (SCN3ME_SUBM, lamda=0.3). Layout size is 2311 x 2310 microns and each chip has bonding pad with 40 pins. DIP40 process is used for packaging. Here, we can only see photodiodes because rests of circuit are shielded by top level metal.

3.2 Qualitative analysis

In this section, we are going to show qualitative analysis of the chip in order to confirm whether it works as we expected in equation (2-19). Fig. 3-3 to Fig. 3-5 shows column output voltage change when reference voltage V_B is increasing. Note that V_c is

also increasing linearly as V_B increases which is expected in equation and simulation.

Reference current and photocurrent are fixed as $1\mu\text{A}$ and 10pA each.



Figure 3-3 Column output voltage V_C when $V_B=2.5\text{V}$.

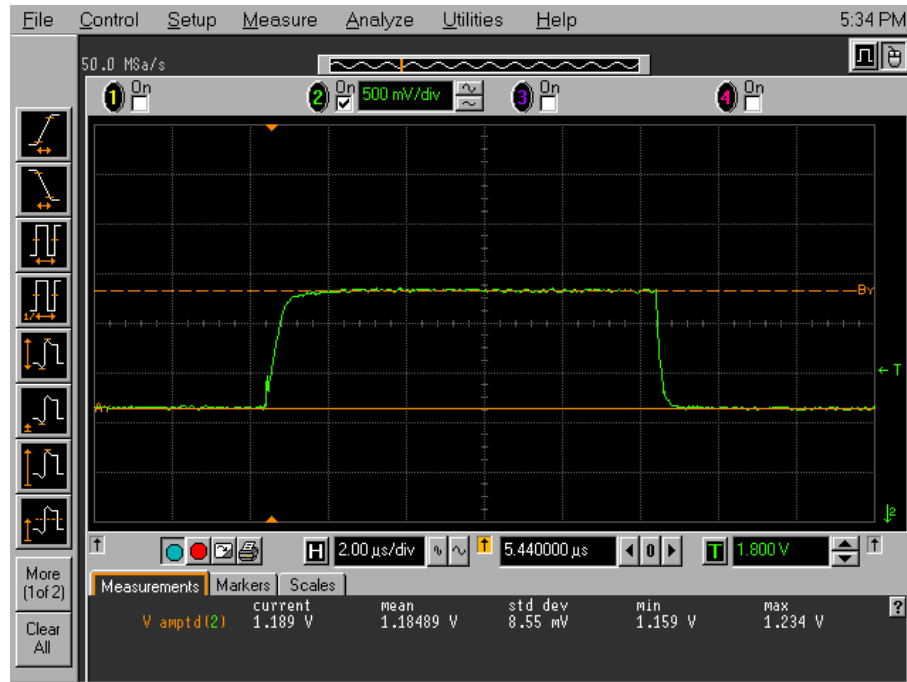


Figure 3-4 Column output voltage V_C when $V_B=3V$.

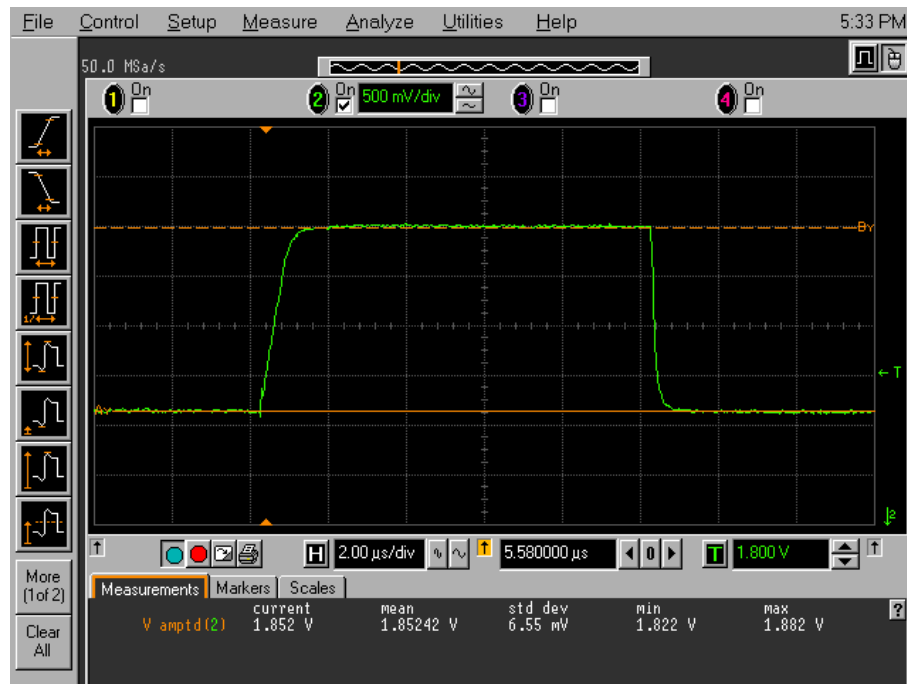


Figure 3-5 Column output voltage V_C when $V_B=4V$.

Fig. 3-6 to Fig.3-8 shows column output voltage behavior when reference current I_R increases. As we expected in equation (2-19), column output voltage V_C decreases logarithmically. From Fig. 3-3 to Fig 3-8, we have seen that pixel circuit works in compliance with theoretical result. In equation (2-19), the only parameter to be controlled is photocurrent I_B which is the most important variable. We will show the circuit behavior according to photocurrent qualitatively and quantitatively in next section.

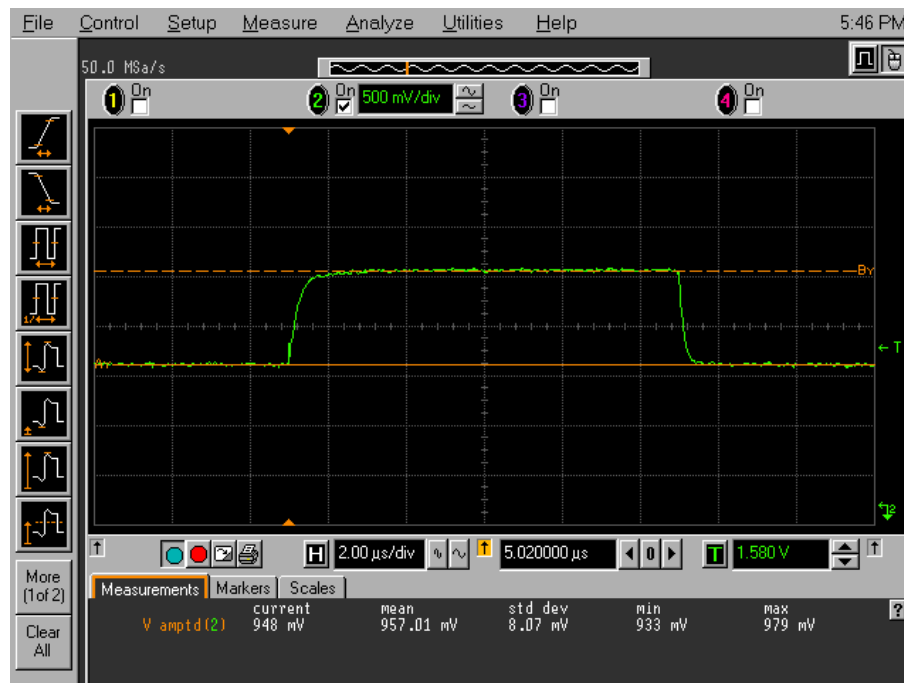


Figure 3-6 Column output voltage V_C when $I_R = 0.5 \mu\text{A}$.

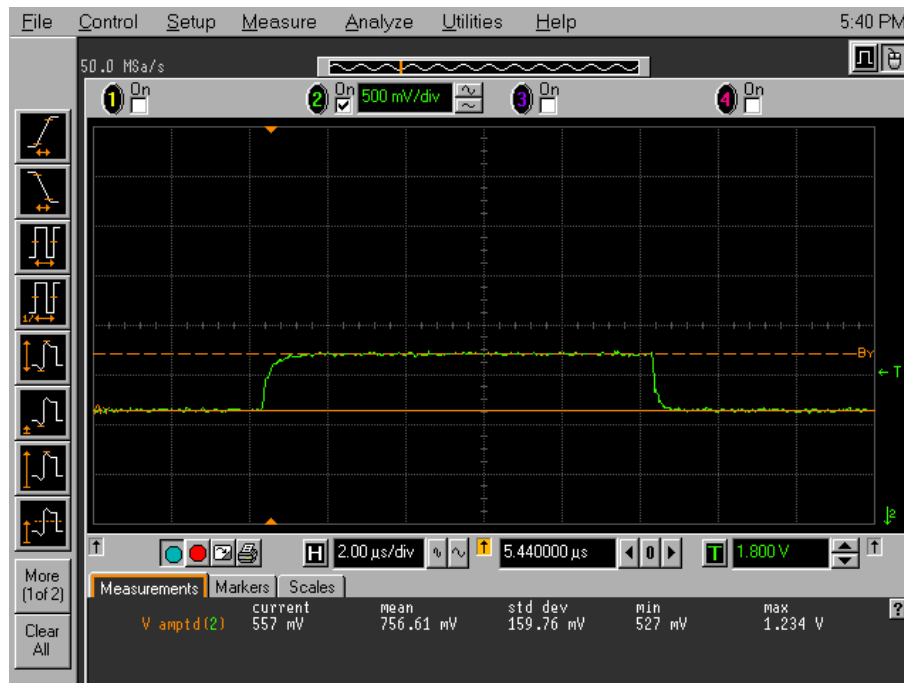


Figure 3-7 Column output voltage V_C when $I_R = 2 \mu\text{A}$.

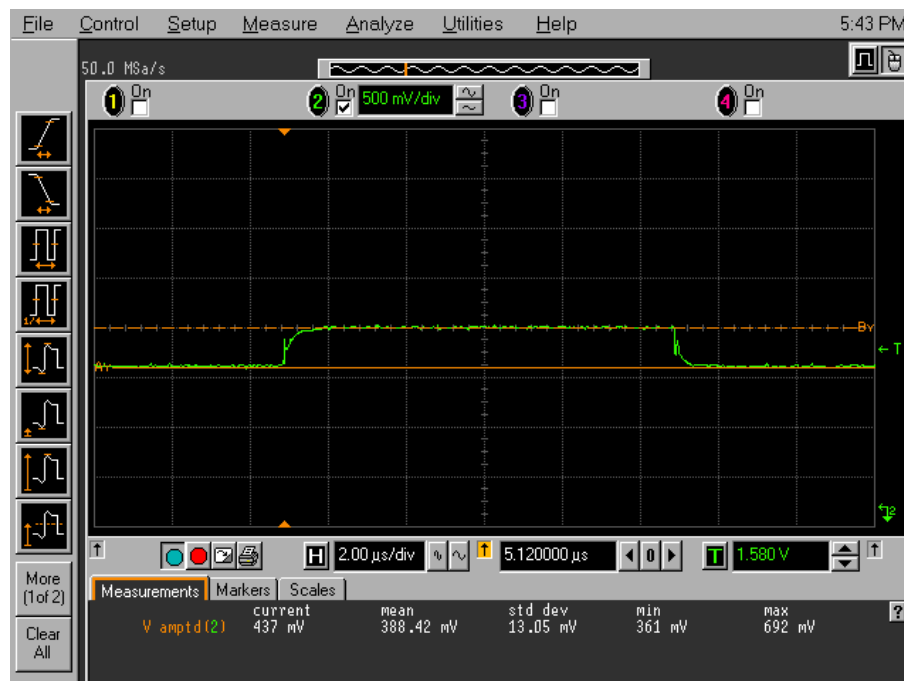


Figure 3-8 Column output voltage V_C when $I_R = 3 \mu\text{A}$.

3.3 Quantitative analysis

To verify further that chip works in compliance with theoretical analysis, quantitative analysis is presented in this section. In order to calculate photocurrent at particular light intensity, photosensitivity of 0.3A/W is used, which is typical maximum value for CMOS with 750nm wavelength light. By multiplying photosensitivity with photodiode area ($9\ \mu\text{m} \times 13.5\ \mu\text{m}$) and irradiance ($\mu\text{W}/\text{cm}^2$), we can calculate the amount of photocurrent generated by the light. In quantitative analysis, reference voltage and reference current are fixed as $V_B=2.5\text{V}$ and $I_R=1\ \mu\text{A}$.



Figure 3-9 Transient scope view of V_c when irradiance = $25\ \mu\text{W}/\text{cm}^2$.

Fig. 3-9 shows transient response of V_c when light intensity is equal to $25\mu\text{W}/\text{cm}^2$. In this case, output voltage level is 769mV. Then this amount of irradiance generates photocurrent of 9pA. This result is very close to the spice simulation result when $I_B=10\text{pA}$ in Fig. 2-13.



Figure 3-10 Transient scope view of V_c when irradiance = $250\mu\text{W}/\text{cm}^2$.

Fig. 3-10 shows transient response of V_c when irradiance is equal to $250\mu\text{W}/\text{cm}^2$. In this case, output voltage level is 910mV. Then this amount of irradiance generates photocurrent of 90pA. Again this result is very close to the spice simulation result in Fig. 2-13.

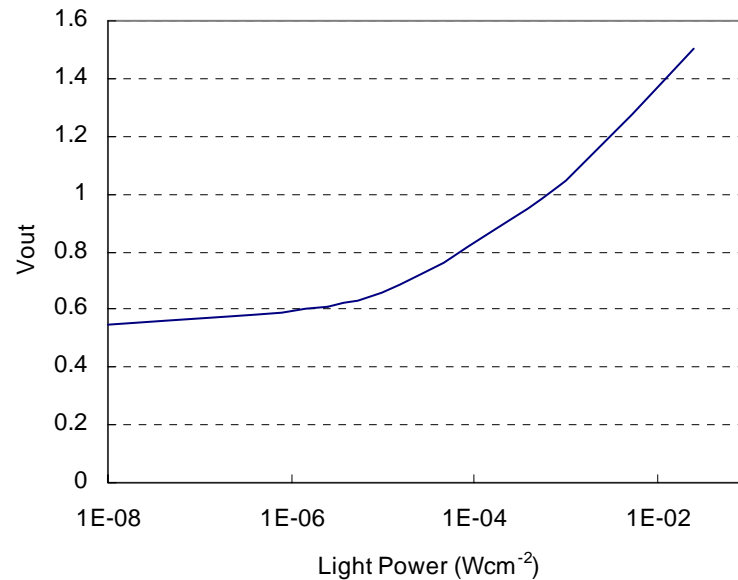


Figure 3-11 Response of sensor as a function of light intensity at sensor level.

Figure 3-11 shows the response as a function of the light intensity at the sensor. The sensor is sensitive for more than 6 decades (120dB) of light intensity which is one of the design objective. The lower part of the curve is limited due to the reverse current of the photodiode. The FPN is estimated as the standard deviation of the pixel output across the array when the sensor is exposed to uniform illumination [14]. This is measured as 2.29 % of the mean output voltage level. Now, we can conclude that the better FPN performance of SRL pixel has been shown comparing to previous logarithmic pixels. In our measurement for FPN, mean output voltage is 599.77mV. Also, the contribution of the column wise FPN can be estimated by calculating the standard deviation of the mean value over each column [14]. This results in 1.49% of the mean output voltage level.

CHAPTER IV

CONCLUSIONS

Logarithmic response image sensors can be used in high ranges of light intensities but they suffer from sensitivity to variations in pixel parameters introduced during fabrication. Due to the continuous nature of the light conversion into voltage, double sampling techniques in order to suppress FPN are not directly applicable as in the case of sensors with integrating pixels. This has the effect of increased FPN compared with sensors having a linear response, which makes non-calibrated images useless.

In this thesis, a newly designed logarithmic pixel has been presented employing an on-chip self-calibrating technique. It makes use of five MOS transistors, thus high resolution is achievable while keeping the total chip area reasonable. The chip is realized using a CMOS technology with $0.5 \mu\text{m}$ minimum feature size. The calibration is performed by sampling two pixel output levels, a level corresponding to the reference current and a level corresponding to the photocurrent. By subtracting these two levels, a significant suppression of FPN is achieved. This method removes the FPN due to variations in threshold voltages across the pixel array, body effect and slope n . An image sensor that consists of 64×64 active pixels has been designed, fabricated and tested. Pixel pitch is $18 \mu\text{m} \times 19.2 \mu\text{m}$ and is fabricated in a $0.5\text{-}\mu\text{m}$ CMOS process. From test results, we have proved that the proposed pixel circuit greatly reduces the FPN in

compliance with theoretical analysis. Measured FPN value 2.29% of output voltage swing and column wise FPN is 1.49% of mean output voltage over each column. Also, this is a self-calibrating pixel, which means that an additional column amplifier to remove offsets is not needed. Therefore, significant amount of chip area can be saved.

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APPENDIX A

Determination of $n(V_{GS})$ and I_0 with spice simulation

$$i = I_0 e^{\frac{q}{kT} \frac{V_{GS}}{n(V_{GS})}} \quad \text{A-1}$$

Therefore,

$$n(V_{GS}) = \frac{q}{kT} \frac{\log e}{\log \frac{i}{I_0}} V_{GS} \quad \text{A-2}$$

Then

$$\frac{d \log i}{dV_{GS}} = \frac{q}{kT} (\log e) \frac{n(V_{GS}) - \frac{dn(V_{GS})}{dV_{GS}} V_{GS}}{n^2(V_{GS})} \quad \text{A-3}$$

Suppose $\frac{dn}{dV_{GS}} = 0$ for a particular V_{GS} (or a range of V_{GS} values).

Then, A-3 reduces to

$$\left. \frac{d \log i}{dV_{GS}} \right|_{V_{GS}=V_{GS1}} = \frac{q}{kT} (\log e) \frac{1}{n(V_{GS})} \quad \text{A-4}$$

Now follow the procedure below;

- 1) Run a dc sweep of V_{GS} (Figure A-1).

- 2) Plot $\frac{q}{kT}(\log e)$ as a function of V_{GS} (Figure A-2).
- 3) Determine V_{GS1} and the corresponding $n(V_{GS1})$ from the extension of the plot ($V_{GS1}=310\text{mV}$, $n(V_{GS1})=1.647$ from Figure A-2).
- 4) Determine $i(V_{GS1})$ from the plot of $i=f(V_{GS})$ ($i(V_{GS1})=88.88\text{pA}$ from Figure A-1).
- 5) Use V_{GS1} , $n(V_{GS1})$ and $i(V_{GS1})$ in 1) to determine I_0 where $I_0 = i(V_{GS1})e^{\frac{q}{kT} \frac{V_{GS1}}{n(V_{GS1})}}$ ($6.03 \times 10^{-14}\text{A}$).
- 6) Now plot $n(V_{GS})$ as a function of V_{GS} after substituting into 2) the numerical value of I_0 found in the preceding step.

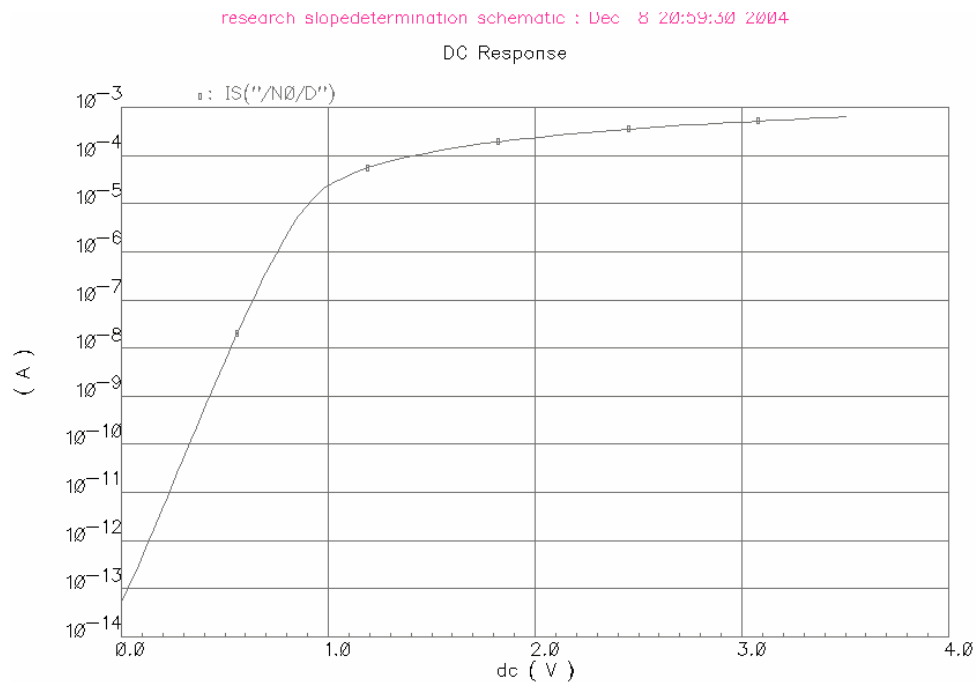


Figure A-1 Drain current (I_D) as a function of V_{GS}

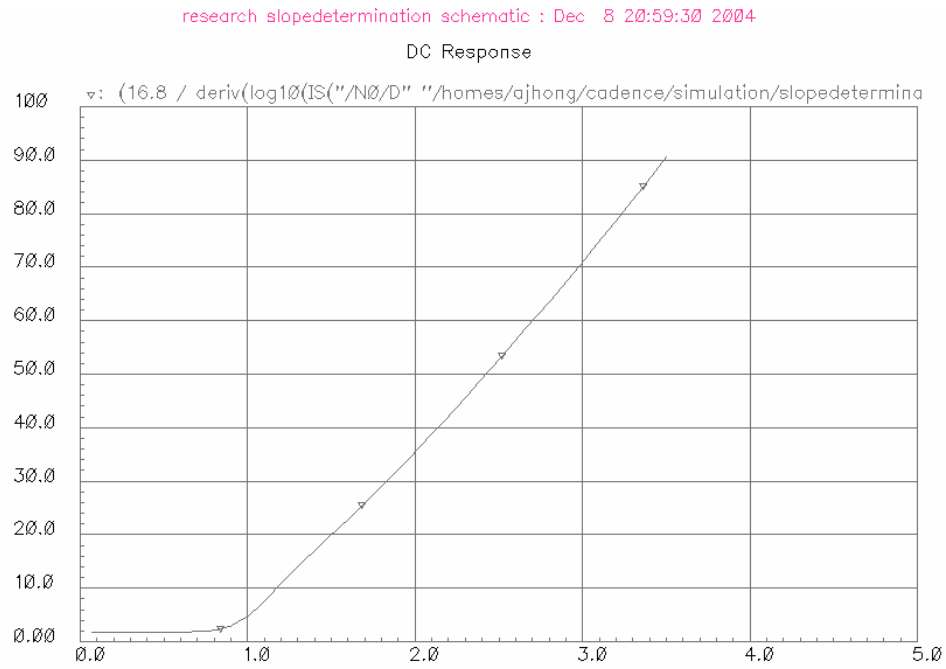


Figure A-2 $\frac{q}{kT}(\log e)$ as a function of V_{GS}

VITA

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