A Step-Down ZVS Power Converter with Self-Driven Synchronous Rectifier

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***Abstract*—In this paper a step-down ZVS power converter with a self-driven synchronous rectifier (SDSR) for a low-voltage high-current applications is proposed. A transformer leakage inductance, a resonant capacitor and a diode make up the active resonant network. To improve the performance of the converter, a SDSR with a center-tapped transformer is used at the secondary side of the converter. Consequently, due to transformer leakage inductance in secondary side, the output section requires no additional inductor, leading to a major size reduction of the circuit. For verification purposes, a laboratory prototype of the proposed converter is manufactured. Experimental results are presented for waveforms to validate the theoretical outcomes. Additionally, to substantiate the design of the proposed converter, a laboratory prototype is manufactured.**

Keywords—Power converter, zero-voltage switching (ZVS), self-driven synchronous rectification (SDSR).

I. Introduction

Improving power density and efficiency is essential for modern power supply. To reduce switching losses Soft-switching techniques are developed. At zero-voltage switching (ZVS) conditions, not only the switch voltage-current overlap is eliminated, but also the turn-on losses created due to the MOSFET output capacitance (C_{oss}) and reverse recovery of the PN junctions are removed properly [1]. In resonant converters, passive LC circuits are adopted to provide soft switching conditions. In ZVS resonant converters, the switching frequency is increased significantly while the switching, conducting and thermal losses are kept low suitably. Therefore, a ZVS resonant converter is one of the best candidates for a modern power supply [2].

Synchronous rectifiers (SR) present much lower conduction losses than the conventional PN/Schottky rectifying diodes [3]. The traditional methods use integrated circuits (IC) and self-driven synchronous rectifiers (SDSR). A major problem is the short-circuit condition occurred at the transition intervals created due to reverse-recovery of the PN junctions and the transformer secondary side leakage inductance [4]. In the SDSR, the gate signals are generated directly by the transformer auxiliary windings [5], [6]. Compared with gate driving methods which are using ICs, SDSR decreases the design complexity, production cost, elements number and gate driving loss [7], [8], [9]. A problem is the malfunction of SDSR in converters using dead time to regulate output voltage. This is because within dead-time intervals, the induced voltage on the auxiliary winding is reduced and consequently the SR may not be driven properly [10].

Integration of ZVS condition and SR is a challenging topic in many researches for different applications [11], [12].

This paper presents a novel converter which benefits from zero-voltage switching, resonance, isolation, integrated transformer and self-driven synchronous rectifier for low-voltage high-current applications. Profiting from advantages of high efficiency, low switching, conducting and thermal losses, low EMI and gate driver loss, small size, high switching frequency range and isolation, this converter can be applied in various applications such as domestic electronic appliances, LED power sources, battery charging purposes, inductively-heated appliances, wireless power charging of portable electronics, transcutaneous power transfer systems, biomedical implants, photovoltaic power optimizer, telecom and other centralized modular and distributed power applications [2], [7]. Furthermore, low-voltage high-current power electronic converters have received huge interest of both industry and academia for their application in stand-alone electric power generating systems.

The transformer leakage inductance (used as L_r) in conjunction with a resonant capacitor and a diode form an active resonant network (active resonant tank) showing a remarkable difference of the proposed converter from LLC [13]. Thereby, the transformer leakage inductance reflected on the transformer primary side is not problematic as it is used as resonant inductor. The employed active resonant tank decreases switching-frequency deviation over the whole range of load variations as well as provides ZVS operation for all switches [14], [15]. An inherent mechanism of this converter, due to its active resonant tank, drastically limits the switching frequency variations to appropriate small values (typically, 10% variations from zero-load to full-load). Thus, components can be designed optimally. A self-driven synchronous rectifier with center-tapped transformer is employed. The output section does not need any additional inductor; therefore, the converter size is greatly reduced.

The paper is organized as follows: Section II provides information about our proposed converter and its operational modes. Section III describes experimental results and finally, section IV concludes the paper.

II. Proposed Converter

The proposed converter is presented in Fig. 1. The converter has seven operating modes in case of using diode rectifier [16] and ten modes in case of using SDSR shown in Fig. 2. The

switches Q_1 and Q_2 constitute an inverter leg. The capacitors C_1 and C_2 (along with the MOSFET parasitic output capacitance C_{oss}) are set in parallel with the switches to provide ZVS condition at class D [1],[2]. An active resonant tank including L_r, C_r and D_r is employed. The transformer leakage inductance is designed to be used as resonant inductor L_r. The diode D_r stabilizes the converter operation. Its junction capacitance is absorbed by C_r and therefore its reverse-recovery time is not problematic. The switches SR_1 and SR_2 are the output synchronous rectifiers driven by the transformer auxiliary windings. In Eq. (1),(2),(3) we define various parameters which will be used in the following discussion. The parameters α and β are used to simplify the equations and B is the converter normalized voltage gain "$B = nA = nV_o/V_s$, φ_1 and φ_2 are the conduction angles of Q_1 and Q_2 respectively. In each operation mode $I_{number} = i_r(t_{number})$.

$$\omega_r = 2\pi f_r = \frac{2\pi}{T_r} = \frac{1}{\sqrt{L_r C_r}} \quad , \quad R_o = \frac{n^2 V_o^{\,2}}{P_{out}} \tag{1}$$

$$B = n\frac{V_o}{V_S} = nA \quad , \quad Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2}$$

$$\alpha = \frac{C_r}{C_1 + C_2} \quad , \quad \beta = \frac{1+\alpha}{\alpha} \quad , \quad \omega_\alpha = \sqrt{1+\alpha}\,\omega_r \tag{3}$$

Mode I (t_0<t < t_1): prior to t_0, the diode d_1 was conducting and the gate signal for Q_1 has been set. Therefore, at t_0, the Q_1 is turned on under the ZVS condition. The voltage of the resonant capacitor (called resonant voltage v_r) is zero at t_0. Due to L_r, v_r starts increasing in a resonant fashion when Q_1 conducts. Then, a positive voltage applies on the primary side of the transformer which reflects to the secondary and auxiliary windings (which provide gate voltage signal for SR_1). Then the switch SR_1 is turned on and power is delivered to the output.

$$t_1 - t_0 = T_1 \quad , \quad T_1 = \frac{\varphi_1}{\omega_r} \tag{4}$$

$$v_r(t) = V_S(1-B)\left[1 - \cos(\omega_r(t-t_0))\right] \tag{5}$$

$$i_r(t) = \frac{V_S}{Z_r}\left[(1-B)\sin(\omega_r(t-t_0))\right] \tag{6}$$

Mode II (t_1 < t < t_2): by reaching v_r to V_S the voltage across the primary winding is reduced. Therefore, the auxiliary voltage applied on the gate of SR_1 is also decreased to less than the threshold voltage which causes the MOSFET turned off. However, due to the transformer leakage inductance at the secondary side, L_{SS2}, the anti-parallel diode of SR_1 remains ON and continues the current.

At the end of this mode, Q_1 is turned off. Due to C_1, Q_1 is turned off at ZVS condition. The durations of this mode along with the previous mode, in which Q_1 is conducting, is defined as φ_1/ω_r. To provide the phase lag needed to maintain ZVS turn-off, i_r should be positive at t_2, or in other words φ_1<180. All equations of this mode are identical to those of the previous interval.

Mode III (t_2 < t < t_3): since t_2 is prior to the zero-crossing instant of the resonant current, i_r; by turning Q_1 off at t_2, the remaining current of L_r flows through C_1 and C_2. Then, the middle voltage (the voltage of node M in Fig. 1 which is denoted by v_M), is reduced to zero through a resonant with L_r at t_3.

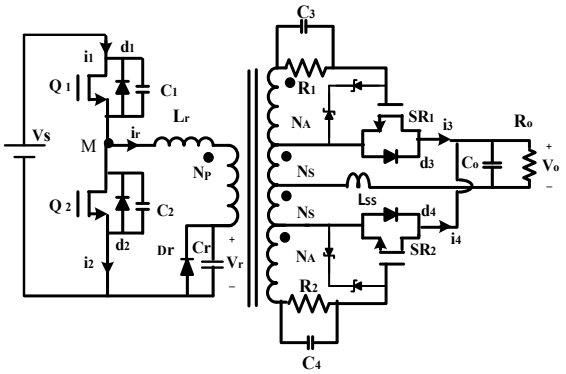

Fig. 1. Proposed resonant ZVS converter

$$\frac{i_r(t)}{V_s/Z_r} = \frac{(1-B)\cos\varphi_1}{\sqrt{1+\alpha}}\sin(\omega_\alpha(t-t_1)) + (1-B)\sin\varphi_1\cos(\omega_\alpha(t-t_1)) \tag{7}$$

$$\frac{v_r(t)}{V_S} = \frac{(1-B)\cos\varphi_1}{\sqrt{1+\alpha}}\sin(\omega_\alpha(t-t_1)) - \frac{(1-B)\sin\varphi_1}{1+\alpha}\cos(\omega_\alpha(t-t_1)) \tag{8}$$

Mode IV (t_3 < t < t_4): at t_3, the diode d_2 is forward biased and i_r flows through it until t_4, when the resonant current i_r becomes zero. The auxiliary winding applies a positive voltage on the gate of SR_2 and turns it on. In this mode, the gate signal for Q_2 is set to turn it on at ZVS. At t_3 the current of I_r is called I_3 which is used in Eq. (10). Here, $\varphi(t_4<t<t_5)$ and $\varphi(t_5<t<t_6)$ are called φ_{x1} and φ_{x2}. Considering $\frac{-B}{\sin\varphi_2} = \gamma$ the equations are as below.

$$\frac{i_r(t)}{V_s/Z_r} = (2B - \gamma)\sin(\omega_r(t - t_3)) \tag{9}$$

$$\frac{v_r(t)}{V_S} = V_s[I_3\sin(\omega_r(t - t_3)) + B] \tag{10}$$

$$\varphi_{x1} + \varphi_{x2} = \varphi_d \tag{11}$$

Mode V (t_4 < t < t_5): at t_4 the current of Q_2 becomes positive and then the MOSFET of Q_2 conducts. Due to the transformer secondary side leakage inductance L_{SS2}, the diode d_3 remains ON until t_5, when the current of L_{SS2} is reversed and d_3 is turned OFF at ZCS condition. During this mode, the energy stored in C_r is transferred to the output, but v_r is still positive at t_5.

$$\frac{i_r(t)}{V_s/Z_r} = (2B - \gamma)\sin(\omega_r(t - t_4)) \tag{12}$$

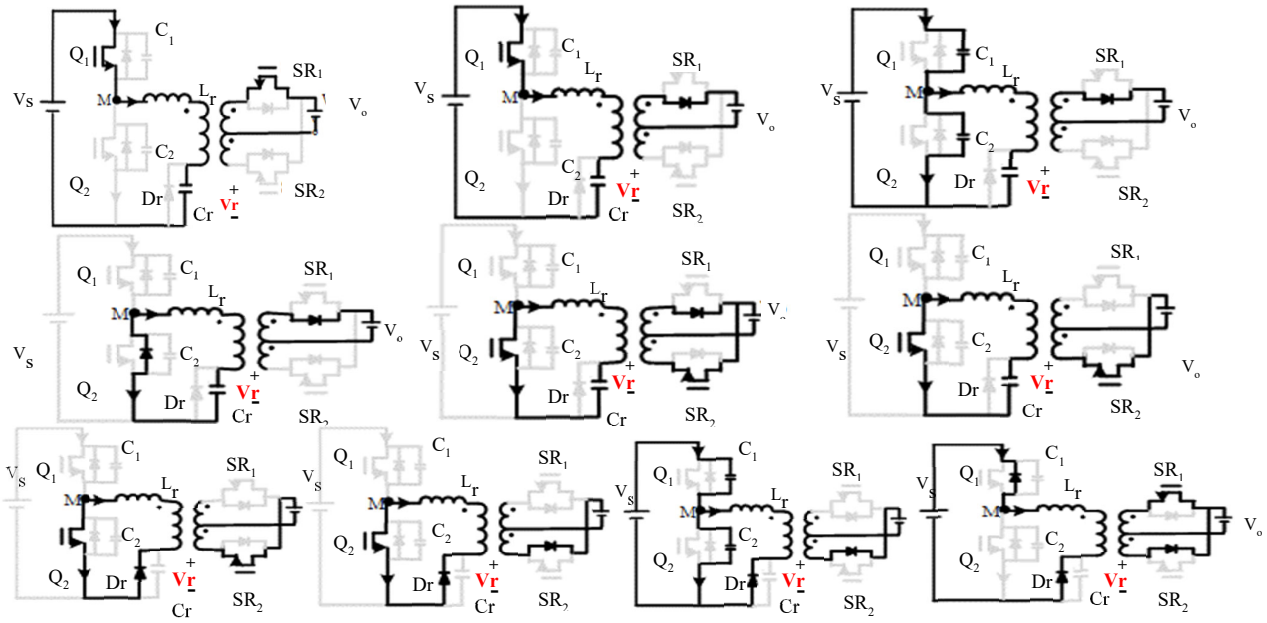

Fig. 2. Schematic circuit of the proposed high efficiency isolated resonant converter using a self-driven synchronous rectifier

$$\frac{v_r(t)}{V_s} = -(2B-\gamma)\cos(\omega_r(t-t_4)) + B \tag{13}$$

Mode VI ($t_5 < t < t_6$)**:** during this mode, remaining energy stored in C_r is transferred to the output until v_r reaches zero at t_6. The interval from t_4 to t_6 is defined as φ_d which indicates the conduction angle of D_r.

$$\frac{v_r(t)}{V_s} = (2B-\gamma)\left[\frac{(\cos\varphi_{x2})}{(\sin\varphi_{x1})}\sin(\omega_r(t-t_5)) + \cos(\omega_r(t-t_5))\right] \tag{14}$$

$$\frac{i_r(t)}{V_s/Z_r} = (2B-\gamma)\left[-\frac{(\cos\varphi_{x2})}{(\sin\varphi_{x1})}\cos(\omega_r(t-t_5)) + \cos(\omega_r(t-t_5))\right] + \frac{(\sin\varphi_{x2}\cot\varphi_{x1})}{C_r} + \frac{\cos\varphi_{x2}}{C_r}] \tag{15}$$

$$T_5 + T_6 = \frac{\varphi_d}{\omega_r}, \quad \varphi_d = \cos^{-1}\left(\frac{B}{2B-\gamma}\right) \tag{16}$$

Mode VII ($t_6 < t < t_7$)**:** by setting v_r to zero at t_6, the diode D_r is forward biased at ZVS. Then the resonant current i_r continues through it and the voltage of v_r is clamped at zero. During this mode, the magnetic energy stored in L_r is transferred to the output and the magnitude of i_r decreases linearly.

$$\frac{i_r(t)}{V_s/Z_r} = B\omega_r(t-t_6) + r_r(t_6) \tag{17}$$

Mode VIII ($t_7 < t < t_8$): at t7 the voltage of auxiliary winding of SR2 is reduced to less than the threshold voltage. Hence, SR2 is turned off while its anti-parallel diode d3 is still conducting. The preceding equations are remained valid for this period, since the substitution of SR2 with its anti- parallel diode applies no changes.

$$T_x = T_7 + T_8 = \frac{\varphi_3}{\omega_r} \tag{18}$$

$$i_x = i_7 + i_8 \tag{19}$$

$$\frac{v_r(t)}{V_s} = V_s\left[\left(-I_x\sqrt{\alpha}\right)\sin(\omega_r\sqrt{\alpha}(t-t_x)) + B\cos(\omega_r\sqrt{\alpha}(t-t_x)) - B\right] \tag{20}$$

$$\frac{i_r(t)}{V_s/Z_r} = \left[\frac{B}{\sqrt{\alpha}}\sin(\omega_r\sqrt{\alpha}(t-t_x)) + I_x\cos(\omega_r\sqrt{\alpha}(t-t_x))\right] \tag{21}$$

Mode IX ($t_8 < t < t_9$)**:** by turning Q_2 off at t_8, the flow of the remaining current in L_r continues through C_1 and C_2 resulting that v_M increases until it reaches V_S at t_9.

$$\frac{i_r(t)}{V_s/Z_r} = \omega_r(t-t_9) + i_r(t_9) \tag{22}$$

$$t_{10} - t_9 = \frac{i_r(t_9)}{\omega_r} \tag{23}$$

Mode X ($t_9 < t < t_{10}$)**:** by reaching v_M to V_S at t_9, the diode d_1 is turned on at ZVS and i_r flows through it until it becomes zero at t_{10}. Then, d_1 and D_r are turned off at ZCS conditions. It should be mentioned here that no additional mode will be added by C_3 and C_4.

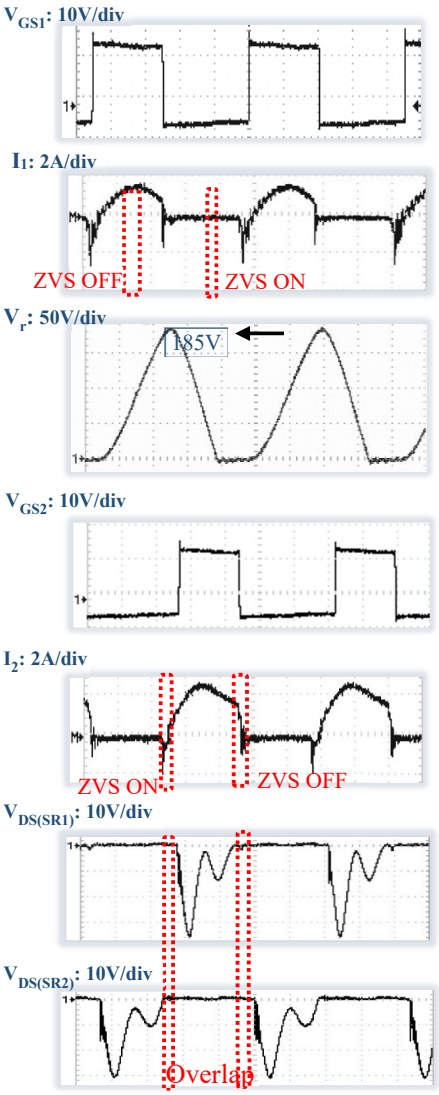

Fig. 3 Practical waveforms fo the converter in full load mode (Pout=100 W, Fs=220 kHz, 1 us/div, Period=4.54 us)

III. Experimental Results

A prototype of the proposed converter has been made in laboratory with specifications such as: input voltage V_s=150V, output voltage V_o=5V, output current I_o=20A, switching frequency $F_{s\text{-}full}$=220kHz for full-load waveforms. The parameters of this converter is given in table I (overdesign=1.2, α=6 (obtained by the simulation in PSPICE)).

Also, the efficiency of this converter is 94.5%. Figure. 3 shows practical waveforms for primary side of transformer in full-load case, where both "ZVS turn-on" and "ZVS turn-off" are obtained for Q_1 and Q_1. In addition, the currents of Q_1 and Q_1 are negative for a few tenths of microseconds, when the primary side switches are turned on and off. The behavior of v_r is also shown in this figure. Then the experimental waveforms of secondary side are illustrated, where two drain-source voltages of SRs with mentioned overlapping periods are highlighted.

TABLE I
PARAMETERS AND COMPONENTS OF THE CIRCUIT

Symbol	Full-Load - Light-load
Vs	150V
Vo	5V
P_{out}	100W
f_s	220kHz
C_r	23nF
L_r	25µH
C_1	1nF
C_2	1nF
R_1	0.5Ω
R_2	0.5Ω
f_r	202kHz

IV. Conclusion

Working under "Zero Voltage Switching (ZVS)" for low-voltage and high-current applications, a new isolated resonant converter with SDSR is presented. The active resonant network is composed of a transformer leakage inductance, a resonant capacitor and a diode which provide ZVS conditions for all switches. A simple SDSR with a center-tapped transformer is employed at the secondary side to promote converter performance and three transformers are merged into one. Hence the output section needs no further inductor, resulting in a major size reduction of the circuit. Experimental results are presented for waveforms to validate the theoretical outcomes.

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