LOW VOLTAGE VERTICAL RECORDING PREAMPLIFIER FOR HARD DISK DRIVES

A Thesis

by

RAMACHANDRA MURTHY MELLACHERVU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Jose Silva-Martinez (Chair of Committee)	
Ugur Cilingiroglu (Member)	Laszlo Kish (Member)
Kumbakonam Rajagopal (Member)	Chanan Singh (Head of Department)

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ABSTRACT

Low Voltage Vertical Recording Preamplifier

for Hard Disk Drives. (August 2004)

Mellachervu Ramachandra Murthy, B.Tech., Indian Institute of Technology, Madras

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Higher data rate hard disk drives(HDD) and improved read channel electronics are demanding preamplifier performance be extended well beyond 1 Gb/s. Historically, preamplifier power requirements were of low priority; however, with increased demand for battery powered devices such as laptops, MP3 players, personal video recorders, and many other wireless hand-held devices, power consumption has become an important design parameter. Furthermore, in order to continue to increase drive capacities, new read-write head technologies(vertical recording and TGMR heads) are demanding innovative preamplifier circuit solutions. Today's production preamplifiers possess a wide band response of 2.5 MHz-600 MHz; however next generation preamplifiers will require response greater than 250 KHz-1 GHz. Low corner frequencies below 250 KHz present read recovery (sleep-to-read, write-to-read, etc) challenges which can limit drive capacity.

This project targets a $>$ 2 Gb/s TGMR (tunneling giant magneto-resistive) read path for vertical recording HDDs. A high performance BiCMOS process(IBM's $0.5\mu m$ 5HP process) is essential due to the large transconductances, low noise and high speed requirements of the read path's first stage.

System frequency limitations at the input are a result of the large TGMR read sensor and preamplifier input capacitance. Due to read head and preamplifier manu-

facturing variations, resistive feedback around the first stage is used to set a controlled input impedance targeted to match the interconnect transmission line. Head resistance variations lead to gain variations; however, the TGMR element becomes more sensitive with larger resistance. This, to a first order approximation, acts like an automatic gain control and reduces variations in gain due to the head.

To Sruti

ACKNOWLEDGMENTS

Over the course of my study at Texas A&M University, I met a lot of wonderful people who have shaped my thinking for the better. AMSC is a huge group and hence provides one with the opportunity to interact with a lot of students of circuit design. My discussions with Praveen Kallam, though limited to a semester, were basic and rigorous, and exposed me to the complexity of circuit design. Huseyin, Xin, Chava and Faramarz used to be always forthcoming for discussions which have proved very fruitful for me.

One of the reasons why I chose Dr. Silva as my advisor is his love for circuit design. He showed me the intuitive and rather more beautiful aspect of working with circuits. My interactions with him have provided me with new ways of looking at circuits. Working under him has been a very illuminating experience.

The most important influence on me, though very indirect, has been Dr. Ugur Cilingiroglu. Attending his courses has given me the confidence of learning things myself. His careful and systematic approach of dealing with things, his patience while dealing with students trying to understand their confusion and providing the correct cure has left me in awe.

I take this opportunity to thank Bryan Bloodworth and Davy Choi for helping me with the development of the project when I was doing my internship at Texas Instruments Incorporation. In spite of busy schedules, Davy always had time to listen to me and clear any problems I had with understanding the working of the preamplifier.

Any work I do would be incomplete without thanking my parents for providing me the background and support to deal with the ups and downs of life. I am very

fortunate to be able to avail their counsel when needed.

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CHAPTER I

INTRODUCTION

Higher data rate disk drive and faster read channel electronics are demanding the preamplifier performance be extended beyond 1-Gb/s. The way information is stored on the magnetic media is also changing to achieve higher data density. Magnetic dipoles are being placed vertically(vertical recording) rather than horizontally to pack more data onto the magnetic media.

Traditionally, the preamplifier has been designed using bipolar technologies because of the low noise, high frequency and high gain requirements. But with CMOS read-channels overtaking the bipolar read-channels the stress has been towards realizing preamplifiers in digital CMOS for future integration possibilities [1]. With a purely CMOS preamplifier integrating the AGC and low pass filter onto the preamplifier is feasible. In such a scenario the read-channel becomes a purely digital system. This can lead to lower prices and higher integration of the read channel with other blocks.

A. CMOS vs SiGe

Keeping up with the rising data rates with digital CMOS is very difficult. The most recent work using a CMOS(Complementary Metal Oxide Semiconductor) process for MR/GMR [1] head preamplifier achieves a data rate of 1-Gb/s [2]. SiGe BiCMOS processess provide very high f_t bipolar transistors that can be used to build high speed preamplifiers at manageable costs.

Style and format follow *IEEE Journal of Solid-State Circuits.*

[1]Giant Magneto Resistance

The current state of the art preamplifier is designed for 2.2 Gb/s data rates using 0.35 μm SiGe 45 GHz BiCMOS process for desk top disk drives. These preamplifiers use $\pm$5V to achieve these rates[2].

B. Goals of the project

This project aims for a 3-Gb/s Vertical Recording Preamplifier with Tunneling Giant Magneto Resistance(TGMR) in a 0.5 μm BiCMOS(Bipolar and CMOS) process with vertical NPN transistors having f_t upto 30 GHz. The supplies used(3.3/-2.1 V) cater to the needs of the mobile applications. The preamplifier comes with a DC offset at its input due to the DC biasing needed by the read head and hence has a high pass corner. Vertical Recording requires this corner to be as low as 250 KHz($\tau = 4\mu s$). Achieving this can be a challenging task especially when the preamplifier needs to switch from the write mode to the read mode very fast($\approx 50ns$).

The preamplifier must also have gain, bandwidth and high pass corner programability for different reasons. Gain programability is required to help the read channel VGA over come the media variations and the read head height fluctuations as it is flying over the magnetic media. The bandwidth programmablity becomes important when the SNR degrades. Reducing the bandwidth improves the Signal to Noise Ratio(SNR) when the signal power during a particular section of the data is not high frequency. The high pass corner needs to be changed to higher frequency values during switching from write to read mode. Higher frequency corners improve the switching times.

Due to the different functionalities, the preamplifier has been divided into three stages realizing the different requirements of the preamplifier. The first stage acts

[2]http://eu.st.com/stonline/prodpres/dedicate/datastor/preamp/preamp.htm

like a low noise amplifier and gives the maximum boost($\approx 36dB$) to the signal. The second stage is used to realize the programmable bandwidth and high pass corners. The last stage is used for programmable gain. The last two stages give a combined gain which varies from $5dB - 10dB$.

C. Thesis Guide

A brief description of what is to follow is given below. The thesis has been divided into 4 different chapters.

Chapter II deals with a system description of the hard disk drive and the preamplifier. The design challenges are presented and a few known ways of solving the problems faced are given.

The core of the thesis is in Chapter III. This chapter defines the specifications of the preamplifier. The architecture used is described and the innovations with respect to stability of the first stage and the problem of signal feedthrough are described.

Chapter IV includes the post layout simulation results for gain, bandwidth and high pass corner. Gain and bandwidth are shown to have single bit programability while the high pass corner has 2-bit programmability. The input resistance plots and linearity are also shown. The conclusions derived during the project have also been presented.

CHAPTER V

HARD DISK DRIVE AND PREAMP

In this chapter we are going to study the basic architecture of the Hard Disk Drive and we will also see the importance of the preamplifier in this system, the challenges faced by it compared to conventional amplifier structures. Some of the architectures for preamplifiers will also be discussed.

A. Hard Disk Drive

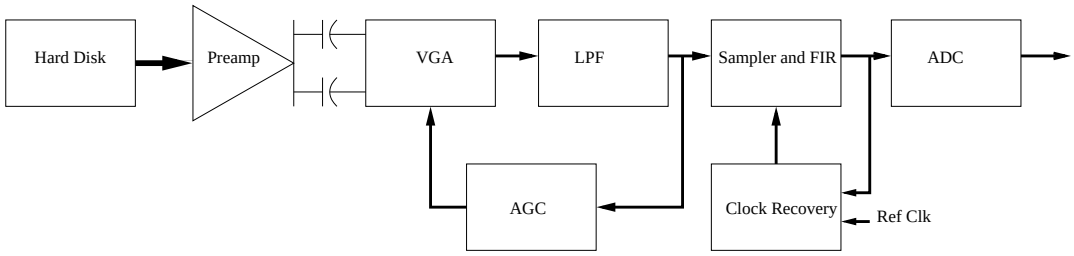

Fig. 1. The analog front of the hard disk drive

Fig.1 represents a block level diagram of the Hard Disk Drive analog front. The read head moves very close to the magnetic media. The signal coming through the read head can vary quite a lot because of height variations. An essential requirement of any communication system is to be able to improve data transfer and error rates which are usually done with the help of signal shaping, bandlimiting and automatic gain control. Such circuits ensure that the signal shaping and amplitude are optimal for data detection.

The data on the disk is stored using NRZI(Non Return to Zero Inverted) [1] coding method. Whenever a logic one is encountered there is a change in the direction

of the magnetic flux on the HDD(hard disk drive) while a zero produces no change. A series of ones hence produces a stream of alternating magnetic flux. The data density increases by *encoding* it. Sometimes zeroes are introduced in between continuous stream of ones for easier recovery of the signal. The data recovery is dependant on successful detection of data peaks. This is achieved by looking at the signal derivative and assigning '1' to time window in which it crosses zero. Errors however occur when zero crossing occurs in the wrong time window due to *intersymbol interference, noise and phase distortions introduced due to the limited bandwidth of the electronics.* To keep this to a minimum, wide-band low-noise amplifiers must be used with an almost constant group delay. Group Delay is the rate of change of the total phase shift with respect to angular frequency, $\mathrm{d}\theta$ /$\mathrm{d}\omega$, through a device or transmission medium, where θ is the total phase shift, and ω is the angular frequency equal to 2πf, where f is the frequency.

B. Preamplifier

The preamplifier is the first stage of the analog front of the hard disk. The module is placed close to the read head to keep interconnections(flex) as small as possible. Usually this is on the rotating arm *inside the Drive Enclosure(DE)* to shield it from external interference. Being the first stage of the system it has to be low noise. The signal comes to the preamplifier from the read head through a flex, an extremely light cable. The critical data information is present over a broad range of frequencies so it is necessary to match the input impedance of the preamplifier to the cable over a broad range of frequencies and is usually done through resistive matching.

Broadly the preamplifier is divided into 2 stages to realize its different requirements. The first stage provides most of the signal boosting and will be called the

input stage of the preamplifier. The second realizes the programmable gain, high pass corner and bandwidth of the preamplifier and is called the *backend* of the preamplifier.

1. Design Challenges

There are a few characteristics that make the preamplifier different from the usual amplifiers. The read head is such that its resistance varies with the magnetic field. Hence when biased with a constant DC current the voltage across it changes and this is sensed by the preamplifier. There is an optimal DC biasing point of the read head for it to be maximally sensitive. This means that there is always a DC offset at the amplifier's input which when coupled with the gain requirement is enough to send the usual amplifiers to rail. Hence it is essential to incorporate DC offset cancellation in these amplifiers for proper functioning.

Given the gain and bandwidth requirements of the modern day preamplifiers it is almost impossible to design them in CMOS(Complementary Metal-Oxide Semiconductor) technologies. The BiCMOS(bipolar and CMOS) on the other hand combines high transconductance of the bipolar as well as the low voltage capabilities of the MOS which can be exploited to design the low-voltage high speed preamplifiers.

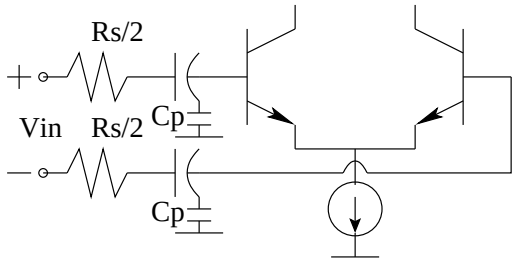

Fig. 2. Input drivers of the preamplifier along with the decoupling caps and parasitics

Traditionally the preamplifiers have been used along with a decoupling capacitor

to take care of the dc offset problem as shown in Fig.2. But these on-chip decoupling capacitors bring additional design issues.

To improve the data density on the disk the magnetic poles are being placed vertically rather than horizontally. This is critical as the servo information which is a part of the overall data information streaming through is usually low frequency and for *Vertical Recording* becomes very low frequency≈100KHz-1MHz. Trying to realize this using the conventional decoupling capacitors means a lot of area. Also these capacitors come along with the parasitics which kill the high frequency performance of the preamplifier by introducing parasitic poles. In Fig.2 it is seen that the pole's frequency due to the parasitics is given by $\omega_p \approx \frac{2G_s+G_\pi}{C_p}$. G_π is the equivalent resistance seen at the base of the common emitter transistor.

Mobile applications present new difficulties to the Hard Disk Drives. One of the more important ones being the realization of the system using lower supplies. Desktop preamplifiers conventionally are designed using 5V dual supplies for the input stage of the preamplifier and just 5V supply for the *backend* of the preamplifier. The dual supply for the input stage is essential for differential input preamplifiers as the read head common mode is biased near the ground [3]. This prevents arcs across the disk and the read head space which can completely damage the read-head and make the whole disk useless. With the common mode of the input source already near the ground there is no head room for circuitry without the dual supplies. "Mobile" preamps will be using much smaller supplies.

2. Architecture Survey

The preamplifier architectures can be divided into four broad categories. They are :-

1. Voltage biased voltage sensing scheme, $\Delta V_s = (\Delta R_h/R_h)V_b$[1].

2. Voltage biased current sensing scheme, $\Delta I_s = -(\Delta R_h/R_h^2)V_b$.

3. Current biased voltage sensing scheme, $\Delta V_s = \Delta R_h I_b$[2].

4. Current biased current sensing scheme, $\Delta I_s = -(\Delta R_h/R_h)I_b$.

Of these the voltage-bias voltage-sense and current-bias current-sense schemes are popular because the final gain is $\propto \frac{\Delta R_h}{R_h}$ which is independant of the variations in the thickness of the read head and hence the system gain is stable [4].

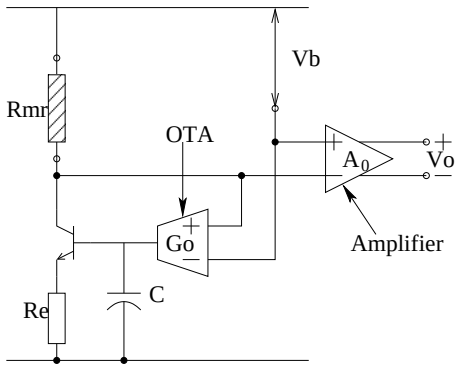

Fig. 3. Voltage bias voltage sensing scheme

Fig.3 gives an understanding of how to voltage-bias and then voltage-sense the signal due to variations in the read head. The feedback OTA(G_o) along with the capacitor(C) decides the high-pass corner. *This can be looked at like an integrator in feedback which ensures that the negative terminal of the amplifier A, is fixed to a DC bias at low frequencies. At higher frequencies the feedback eases and allows the*

[1] R_h is the resistance of the read head which varies with the magnetic field, V_b is the DC voltage bias across the read head.

[2] I_b is the DC current bias through the read head

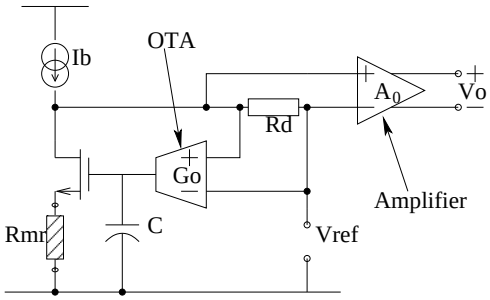

Fig. 4. Current bias current sensing scheme

signals through. The small signal response of this circuit is given by[3],

$$\frac{V_0}{V_{in}} = \frac{A_0}{1 + \frac{G_o R_{mr}}{s(R_e + r_e)C}} \Rightarrow V_0 = \frac{V_b \Delta R_{mr}}{R_{mr}} \frac{A_0}{1 + \frac{G_o R_{mr}}{s(R_e + r_e)C}} \tag{5.1}$$

A_0 is the DC gain of the amplifier shown in Fig.3. While G_0 is the transconductance of the feedback OTA. V_{in} is the signal generated due to the read head and is in series with the read head resistance(R_{mr}).

Fig.4 shows us a way to realize the current-bias current-sensing scheme. The response for this circuit is given by[4],

$$\frac{V_0}{V_{in}} = \frac{A_0 R_d/(R_{mr} + r_s)}{1 + \frac{G_o R_d}{s(R_{mr} + r_s)C}} \Rightarrow V_{sout} = \frac{I_b \Delta R_{mr}}{R_{mr} + r_s} \frac{A_0 R_d}{1 + \frac{G_o R_d}{s(R_{mr} + r_s)C}} \tag{5.2}$$

In the voltage-bias voltage-sense scheme there is a fixed DC voltage across R_{mr}. When this changes the current *through* the read head becomes $\frac{V_b}{R_{mr} + \Delta R_{mr}}$ then $i_{R_{mr}} \approx \frac{V_b \Delta R_{mr}}{R_{mr}}$. $i_{R_{mr}}$ is the signal component of $\frac{V_b}{R_{mr} + \Delta R_{mr}}$. Similarly in the current-bias current-sense scheme we have $i_{R_{mr}} = I_b \Delta R_{mr}$. *This relation is exact while the previous is an approximation for very small* $\frac{\Delta R_{mr}}{R_{mr}}$.

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[3] r_e unless otherwise mentioned is $1/g_m$ of the bipolar transistors and $r_s = 1/g_m$ of the MOS transistors.

[4] V_{sout} is the signal coming out of the preamplifier

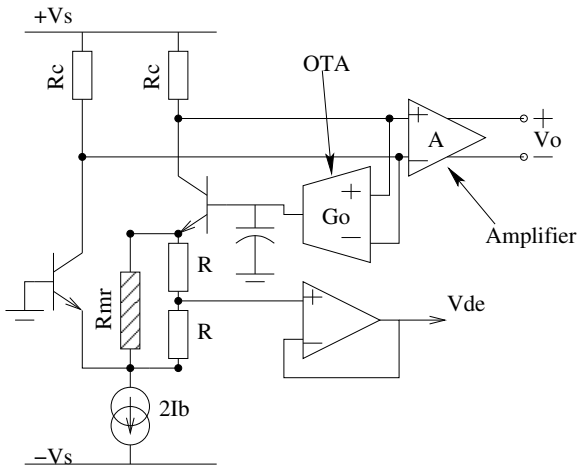

Fig. 5. Current bias scheme which common mode sense voltage to DE

The potential difference existing between the read head and the hard disk is critical and should be under control. One way of doing this would be to sense the common mode voltage of the read head as shown in Fig.5 and make the DE potential also similar. The AC response of this circuit is given by,

$$\frac{V_0}{V_{in}} = \frac{2R_c/(R_{mr}+2r_e)}{1+\frac{G_0 2R_c}{sC(R_{mr}+2r_e)}} \Rightarrow V_{sout} = \Delta R_{mr} I_b A \frac{2R_c/(R_{mr}+2r_e)}{1+\frac{G_0 2R_c}{sC(R_{mr}+2r_e)}} \tag{5.3}$$

It is not possible to use decoupling capacitors directly with bipolar input drivers. The bipolar transistors have a base bias current which will keep charging or discharging the decoupling capacitor and hence the operating point of the bipolars is not fixed. One way to overcome the problem is to use decoupling caps with bipolar transistors as shown in Fig.6. When there is an offset at the input and the decoupled input of the diff-pair driver is different from V_2 then capacitor is going to be charged by the $(i_{b1} - i_{b2})/2$ till $i_{b1} = i_{b2}$. The high pass corner of this circuit is given by the decoupling cap and the r_π of the BJT input drivers. The output frequency response is given by,

$$\frac{V_0}{V_{in}} = \frac{G_m R_C r_\pi}{R_{mr}/2 + r_\pi + 1/sC} \tag{5.4}$$

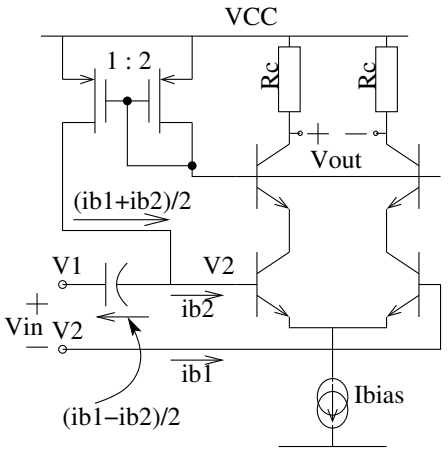

Fig. 6. Decoupling the inputs of the differential pair using feedback

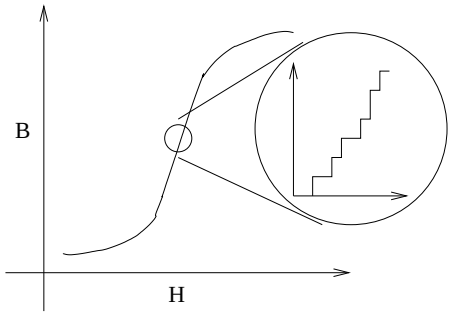

Fig. 7. Barkhausen noise

Another architecture uses magnetic feedback to reduce the *non-linearity, polarity asymmetry and barkhausen noise* of the read head. Barkhausen noise is caused due to the pinning and then releasing of the magnetic dipoles to microstructural obstacles like grain boundaries and non-metallic intrusions. Hence the magnetic induction(B) doesnot vary smoothly with the external magnetizing force(H) as seen in Fig.7.

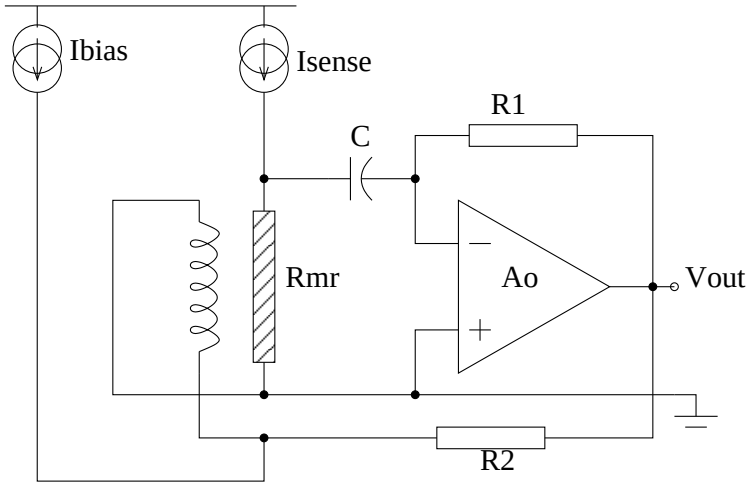

Fig. 8. Architecture to remove read head non-linearity,polar asymmetry and magnetic noise

Fig.8 shows an architecture based on magnetic feedback. The change at the output sends a current in the coil through R_2, sets the feedback and cancels the field due to the data on the read head. Depending on how good this cancellation holds across the active area of the sensor, any change in the magnetization of the sensor is suppressed. Hence the voltage change varies linearly with magnetic field and the nonlinearities, polarity assymmetry and Barkhausen noise are suppressed.

The noise in the preamplifier is characterized by two sources which are usually correlated. It is possible to introduce a transformer [5] before the preamplifier(Fig 9) to improve the noise already present. The total noise after introducing the transformer is given by,

$$\overline{v_{tn}^2} = \overline{v_{hn}^2} + \frac{\overline{v_{an}^2}}{N^2} + 2\gamma(\omega)\overline{v_{an}i_{an}}|Z_h| + N^2\overline{i_{an}^2}|Z_h|^2 \tag{5.5}$$

γ is the correlation coefficient of the voltage and current noise. This equation shows that the noise is dependant on N, the turn ratio in the transformer and hence

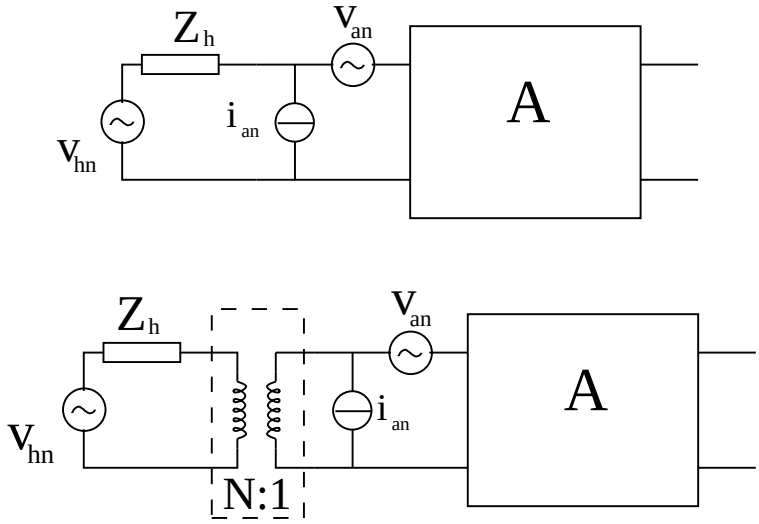

Fig. 9. Using a transformer to improve the noise performance of the preamplifier

can be minimized with respect to N. Hence the turn ratio for minimal noise is,

$$N = \sqrt{\frac{v_{an}/i_{an}}{Z_h}} \tag{5.6}$$

The above techniques show some very basic but useful techniques used to build preamplifiers. Figs. 3-5 especially show us the way to generating offset cancellation using OTA-C structures in feedback. The same technique has been used in the project architecture instead of simple decoupling capacitors to generate very low, high pass corner frequencies.

CHAPTER VI

3 GB/S VERTICAL RECORDING PREAMPLIFIER

A rule of thumb to decide the bandwidth required to transport data at 3Gb/s is $BW = (0.6)\cdot(Data-rate)$. This means the required bandwidth for the preamplifier is at least 1.8 GHz. The preamplifier also has programmable bandwidth, programmable high-pass corner, programmable gain, noise, THD, broadband input matching and write to read time specifications. The details are given in Table. I.

Table I. Specifications for the hard disk drive at 3 Gb/s

S_{no}	**Parameters**	**Values**
1	Gain	$200\frac{V}{V}$
2	Bandwidth	1.8 GHz
3	High Pass Corner	250 KHz
4	Noise	$1.9\frac{nV}{\sqrt{Hz}}$ at 100 MHz
5	THD	0.5%, $V_{outpp} = 300mV$
6	R_{in}	70 Ω
7	T_{W-R}	50 ns
8	PSRR	-50dB
9	CMRR	-50dB
10	VEE	-2.1 V
11	VCC(input)	3.3 V
12	VCC(backend)	1.2 V

A. Basic Architecture

The read path of the preamplifier is split up into 4 stages(Fig.10).

1. Read Input Stage(RIS): This block interfaces with the read-head through the flex. Since this is the first block and has a large gain, noise becomes a critical design parameter [2].

2. Read Middle Amplifier(RMA): The variable bandwidth and boost requirements are met here to overcome process and head variations. This stage usually includes circuitry to compensate for thermal asperity too.

3. Read Secondary Amplifier(RSA): This stage implements the variable gain of the read path to compensate for process and head variations. This also is the final stage of the preamp and needs to match its output to the interconnect between the preamplifier and the read channel.

4. Magneto Resist Biasing Stage(MRBS): This block takes care of the biasing of the read head[1].

B. Important BJT Device Physics

Two important transistor parameters to be considered are β and f_t. Both vary with bias current [6].

1. β dependance on bias

The base current of the transistor consists of two major components. Fig.11 shows a crude profile of a vertical NPN transistor. It highlights one of the reasons for the

[1]The differential biasing of the R_{mr} has not been dealt with in the project.

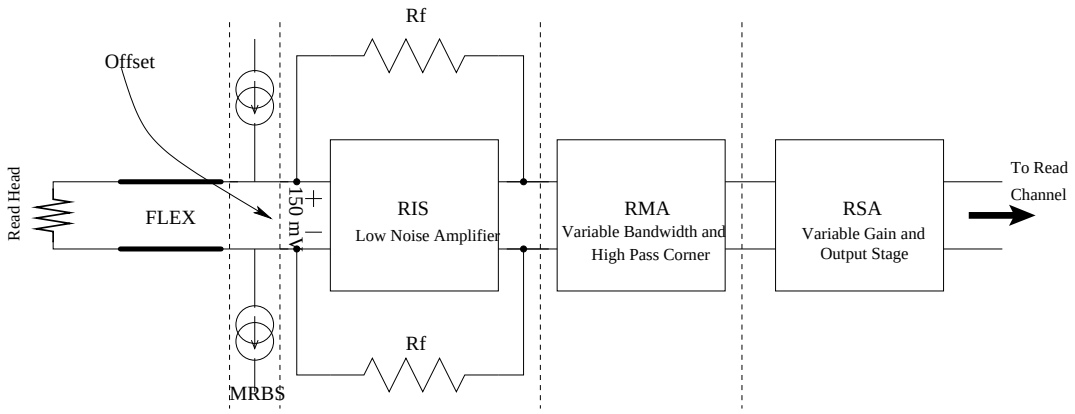

Fig. 10. The read path architecture for the current project

occurrence of the base current i.e. *injection efficiency*. The majority carriers of the base diffuse back into the emitter creating the base current which is given by Eq (6.1).

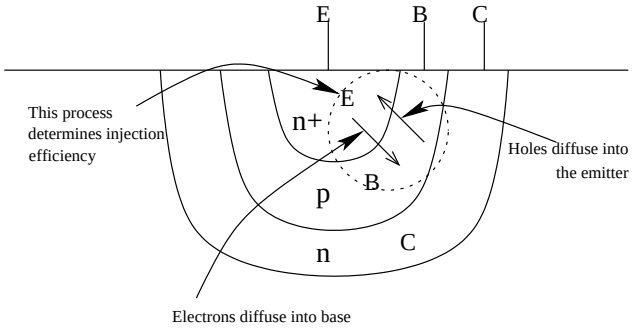

Fig. 11. Cross section of a vertical PNP transistor

$$I_{B1} = \frac{qAD_p}{L_p} p_{nE}(0) \tag{6.1}$$

The second source of base current is recombination of electrons and holes occurring at the base and it is proportional to the minority-carrier charge in the base.

$$Q_e = \frac{1}{2} n_{pB}(0) W_B q A \tag{6.2}$$

$$I_{B2} = \frac{Q_e}{\tau_b} = \frac{1}{2} \frac{n_{pB}(0) W_B q A}{\tau_b} \tag{6.3}$$

τ_b is the minority carrier life time in the base. Fig.12 shows the concentration profile of a bipolar transistor and depicts how the recombination process leads to a base current. Electrons are injected into the base depending on the base-emitter voltage. These recombine with the holes because of the excess number of holes present. But the recombined holes need to be replenished to maintain the concentration profile and are provided by the base current. Effectively the base current is flowing all the way to the emitter.

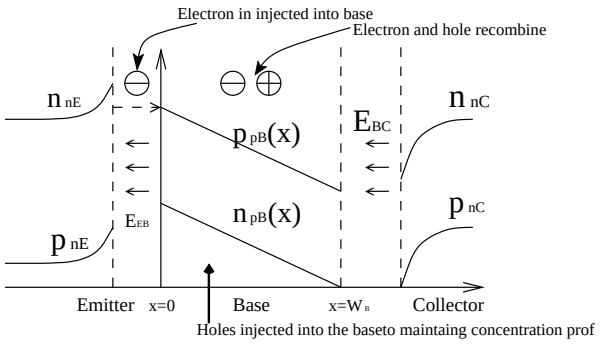

Fig. 12. Concentration profile of an NPN transistor

Hence we can write,

$$I_B = I_{B1} + I_{B2} = \left(\frac{qAD_p}{L_p} \frac{n_i^2}{N_D} + \frac{1}{2} \frac{n_{pBo} W_B q A}{\tau_b} \right) e^{\frac{V_{BE}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} \tag{6.4}$$

Since $\beta_F = I_C / I_B$(forward current gain) we can write[2],

[2] I_C is the collector current in the transistor.

$$\beta_F = \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \tag{6.5}$$

Now as the bias current is reduced the recombination current becomes the dominant base current and is given by[3],

$$I_{BX} \approx I_{SX} e^{\frac{V_{BE}}{mV_T}}; m \approx 2 \tag{6.6}$$

Since $I_C = I_S e^{\frac{V_{BE}}{V_T}}$ we can write the low bias current gain as,

$$\beta_{FL} \approx \frac{I_S}{I_{SX}} \left(\frac{I_C}{I_S} \right)^{[1-(1/m)]} \tag{6.7}$$

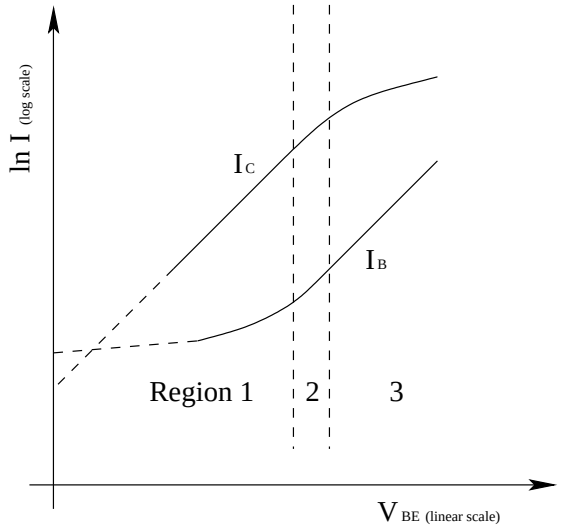

Fig. 13. Variation of I_B and I_C with V_{BE}

Hence we see that β_F is not constant but varies as $\sqrt{I_C}$ at very low currents. When the currents start becoming high, I_C starts decreasing as the bias voltage V_{BE} starts increasing. This is partly due to *high level injection*. In this region,

[3]The subscript 'X' denotes the low current region, 'H' denotes high current.

$$\beta_{FH} \approx \frac{I_{SH}^2}{I_S}\beta_{FM}\frac{1}{I_C} \tag{6.8}$$

Fig.13 shows the base and collector currents as function of the base-emitter voltage and Fig.14 shows variation of β_F directly with I_C.

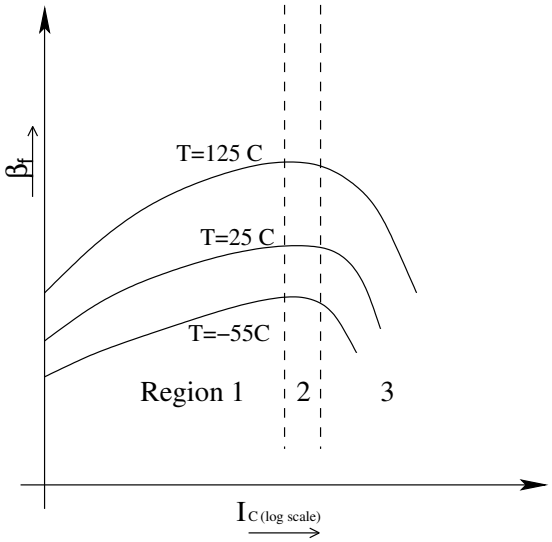

Fig. 14. Variation of β with I_C

2. f_t dependance on bias conditions

Using the small signal equivalent circuit shown in Fig.15, the small signal high frequency current gain can be calculated as,

$$\beta(j\omega) = \frac{\beta_0}{1 + \beta_0 \frac{C_\pi + C_\mu}{g_m} j\omega} \tag{6.9}$$

ω_T is the frequency where the current gain is unity. Hence one can also write,

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} \Rightarrow \tau_T = \frac{1}{\omega_T} = \frac{C_\pi}{g_m} + \frac{C_\mu}{g_m} \tag{6.10}$$

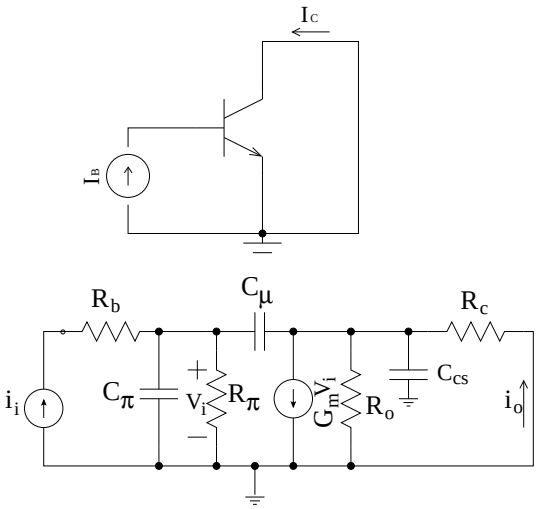

Fig. 15. Small signal equivalent circuit for calculation of f_t

C_π is the sum of base charging capacitance C_b and the emitter-base depletion capacitor C_{je}. Hence Eq(6.10) can also be written as,

$$\tau_T = \frac{C_b}{g_m} + \frac{C_\pi}{g_m} + \frac{C_\mu}{g_m} = \tau_F + \frac{C_\pi}{g_m} + \frac{C_\mu}{g_m} = \frac{W_B^2}{2D_n} + \frac{C_\pi}{g_m} + \frac{C_\mu}{g_m} \tag{6.11}$$

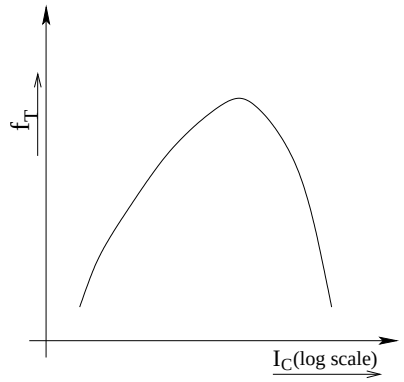

Fig. 16. f_T variation with I_C

τ_T is dependant on I_C through g_m. Decreasing I_C hence increases τ_T hence

decreasing f_T. For higher currents this model is incomplete. τ_F starts increasing for higher current caused by higher injection levels and Kirk effect, the same factors responsible for the decrease in β_F. This effect is shown in Fig.16

C. Proposed Read Input Stage

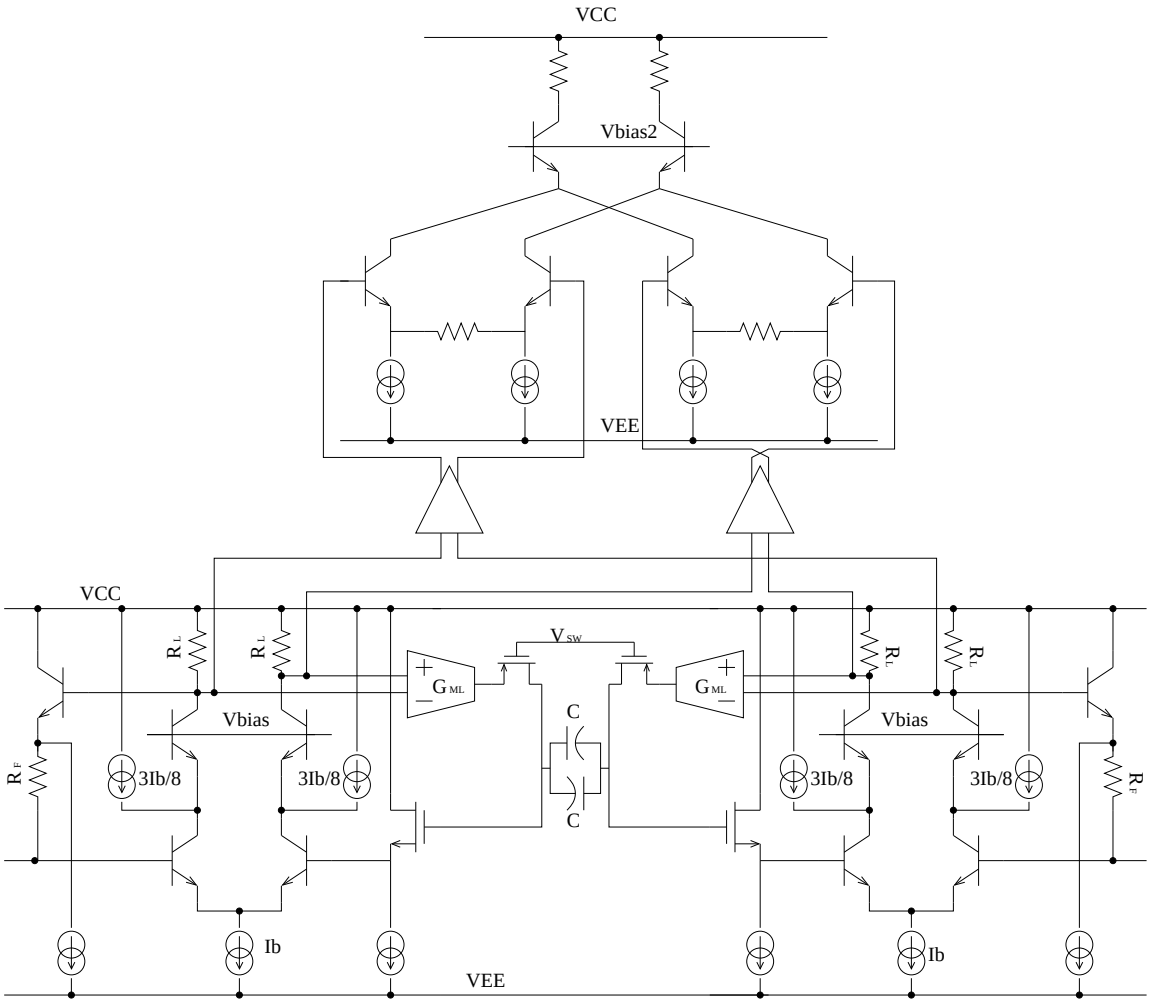

Fig. 17. RIS schematic

The main design consideration of the RIS is to give sufficient boost to the sig-

nal without adding a lot of noise to it while maintaining a matched resistive input impedance to the flex. The schematic diagram of the RIS is shown in Fig.17. This differential circuit can be broken down into its half circuit for simplicity. The half circuit is of the input stage is shown in Fig.18.

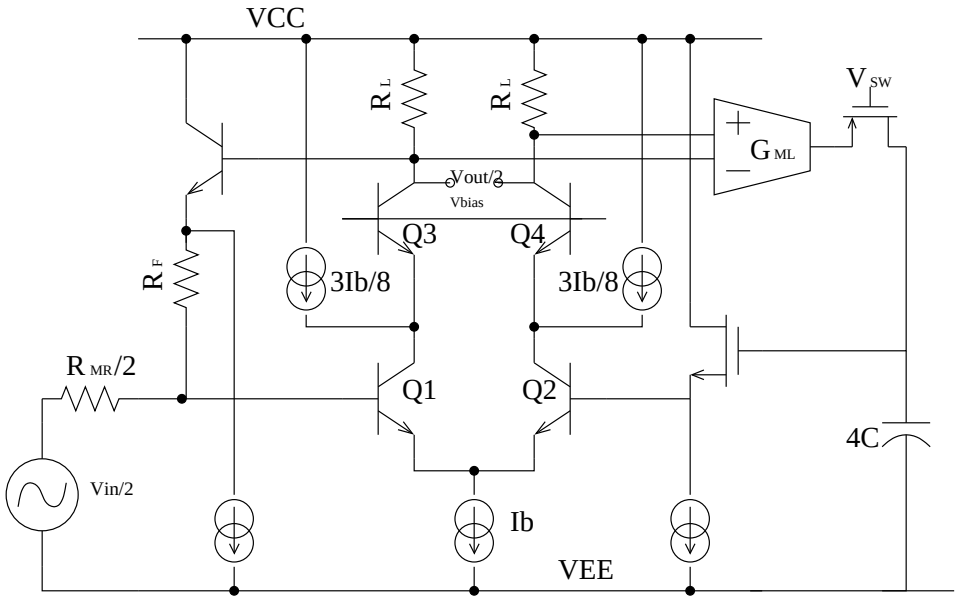

Fig. 18. RIS schematic half circuit

At DC and low frequencies the feedback from the OTA ensures that the base of Q2 follows the base of Q1 and the outputs are held together. Thus at low frequencies there is no signal at the output. At higher frequencies the capacitor gets shorted and the feedback loses steam. High frequency variations donot go through to the base of Q2 allowing the signal to go through. The currents at the cascoded low impedance nodes(emitter of Q3 and Q4) allow large gains with the low supplies.

For the input to be low noise large transistors are used; this reduces thermal noise(4kTR) due to parasitic resistance. Fig.19 shows the cross-section and top view of a bipolar transistor. By increasing the area of the transistors i.e. increasing the

length of the emitter the parasitic resistance shown reduces because of an increase in the number of parallel paths.

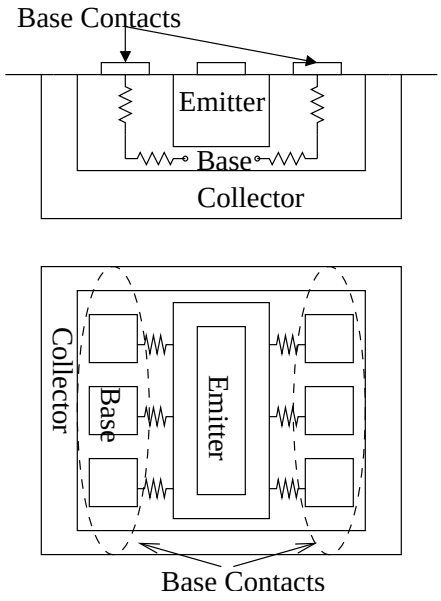

Fig. 19. Reduction of parasitic resistance due to area

To get maximum bandwidth, the input drivers must be biased according to Fig.16 near the peak f_t of the transistors. To get the required gain from this stage with given supplies one doesnot have enough headroom and hence one has to reduce the DC currents in R_L to reduce the headroom requirements. This is done with help of current sources attached to the low impedance cascoded node($3I_b/8$) to reduce current flowing through the load resistances.

1. Realization of Large Time Constants

The RIS is designed for a very low high pass corner. The specified corners are achieved in the RMA using a resistor, capacitor bank which are more reliable than the transconductance of the MOS transistor. To be able to do this it is necessary to generate very

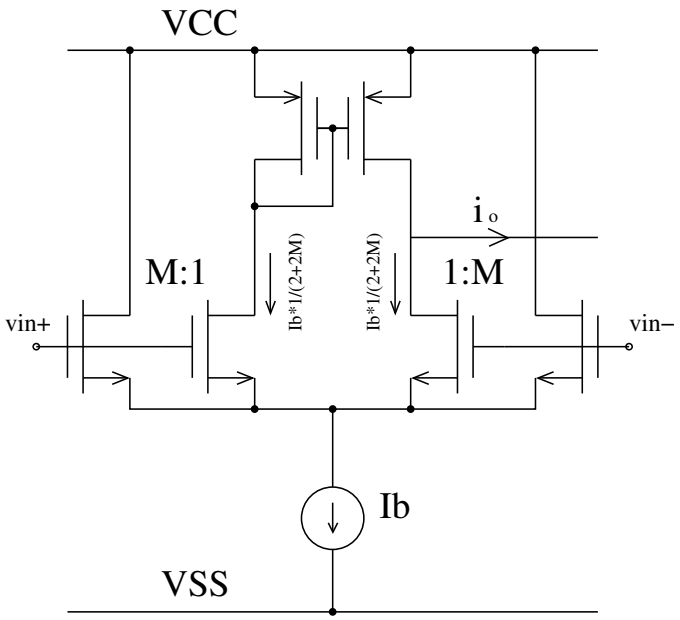

Fig. 20. Generation of low transconductances

low frequency corners(around 10 KHz) in the RIS so that it doesnot interfere with the corner generated in the RMA stage. To be able to do this very large time constants need to be generated. This is being done in the RIS(G_{mL}) using current division techniques as shown in Fig.20 [7].

The transconductance of this circuit can be shown to be,

$$g_m = \sqrt{\frac{I_b \mu_n C_{ox}}{(M+1)} \frac{W}{L}}; \tag{6.12}$$

By increasing M one can get really low values of g_m without having to reduce I_b, which might have to be done using a lot of current mirrors taking up a lot of silicon area.

Other ways can be used to generate large time constants. Impedance scalars are frequently used in biomedical applications where the time constants are very large [7].

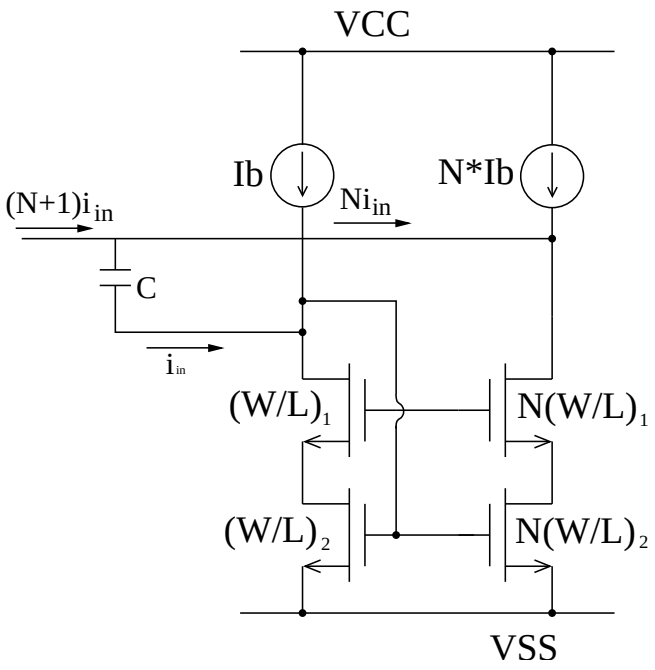

Fig. 21. Impedance scaler

One of the impedance scalers [8] uses current mirrors to amplify the capacitors to get large time constants. The detailed circuit diagram is shown in Fig.21.

A small signal excitation at the input sends a current i_{in} through the capacitor C. This gets amplified by the current mirror and draws a total current of $(N+1)i_{in}$ from the input. This means that the capacitor is scaled by a factor $N+1$. Analyzing this circuit with a very simple model as shown in Fig.22 we arrive at the equivalent capacitance to be,

$$Z_{eq} = \frac{1}{s(N+1)C} + \frac{1}{g_m + sC_p} \tag{6.13}$$

Hence for low frequencies the capacitance seen is $(N+1)C$ and for high frequencies it is $\approx C_p$.

Another very interesting way of generating large time constants is using volt-

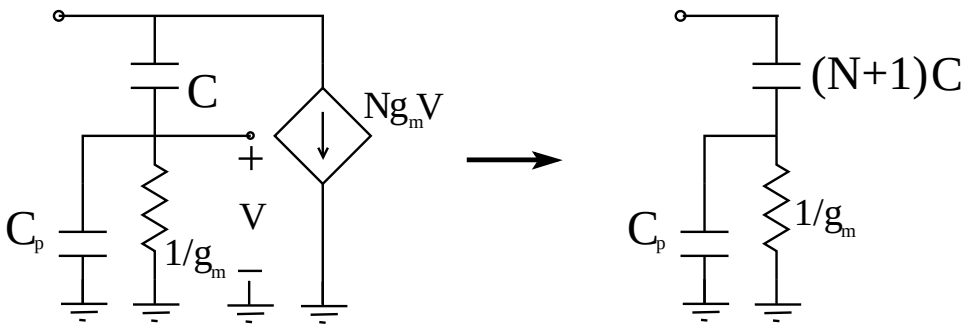

Fig. 22. Analyzing the impedance scalar

age/current dividers as shown in Fig.23. Analyzing the circuit we can write,

$$\tau = (\frac{R_1 R_2}{R_3} + R_1 + R_2)C \tag{6.14}$$

In (6.14) we can have $R_1, R_2 >> R_3$. Hence we can have large time constants. The idea is to reduce the current ultimately going into the feedback capacitor.

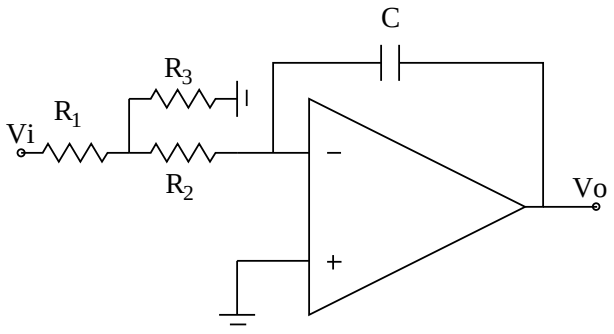

Fig. 23. An interesting way to generate large time constants

This can still be reduced by splitting R_2 again in a nested fashion into a resistance in series with two parallel resistances. This reduces the current again depending of the resistors and hence one can get very large time constants. The problem with this

though would be the noise generated by the resistances used.

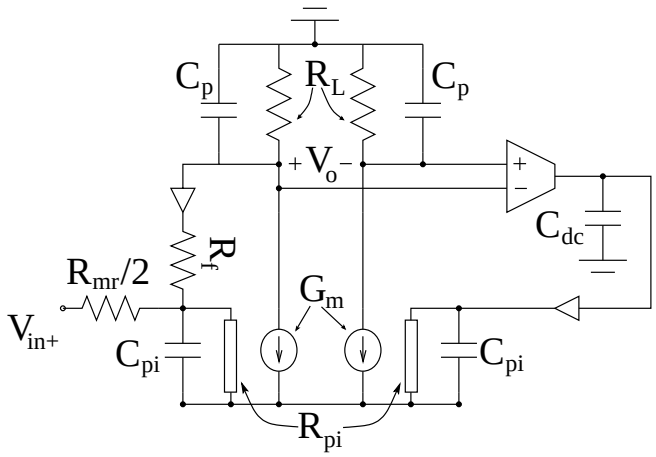

Fig. 24. Half circuit analysis of the RIS input stage

2. Half Circuit Frequency Analysis

Fig.24 is a small signal representation of the RIS half-circuit. Frequency analysis shows that,

$$\frac{V_o}{V_{in}} = -\frac{2G_{mr}}{\frac{(2G_{mr}+G_f)G_{mL}}{sC_{dc}} + \frac{s^2C_pC_{pi}+s(C_p[G_{pi}+2(2G_{mr}+G_f)]+C_{pi}G_L)+G_L[G_{pi}+2(2G_{mr}+G_f)]+G_fG_m}{2G_m}} \tag{6.15}$$

The denominator has been divided into two parts. One of these represents the low frequency high pass behaviour of the circuit and the other reflects the high frequency behaviour of the circuit. For the low frequencies the Eq 6.15 can be written as,

$$\frac{V_o}{V_{in}} = -\frac{2G_{mr}}{\frac{(2G_{mr}+G_f)G_{mL}}{sC_{dc}} + \frac{G_L[G_{pi}+2(2G_{mr}+G_f)]+G_fG_m}{2G_m}} \tag{6.16}$$

The midband gain is hence calculated to be,

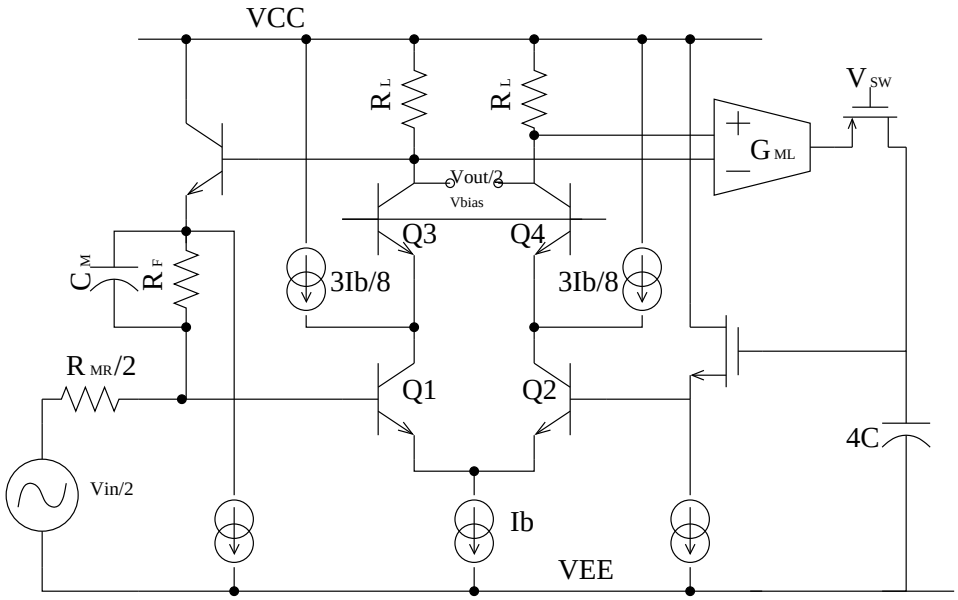

Fig. 25. Miller capacitor to stabilize the circuit

$$A_{dc} = -\frac{4G_{mr}G_m}{G_L[G_{pi} + 2(2G_{mr} + G_f)] + G_f G_m} \approx -\left(\frac{4R_f}{R_{mr}}\right)||\left(G_m R_L\right); \tag{6.17}$$

The high pass corner is given by,

$$\omega_{HP} = \frac{A_{dc}G_{mL}}{C_{dc}} \tag{6.18}$$

The higher frequency response of the circuit can be approximated as,

$$\frac{V_o}{V_{in}} = \frac{-4G_{mr}G_m}{s^2C_pC_{pi} + s(C_p[G_{pi} + 2(2G_{mr} + G_f)] + C_{pi}G_L) + G_L[G_{pi} + 2(2G_{mr} + G_f)] + G_f G_m} \tag{6.19}$$

The R_f feedback in the RIS can sometimes be unstable because there are no dominant poles in the system and the loop gain doesnot have enough phase margin.

One way to compensate this loop would be using a Miller capacitor(Fig.25). But this reduces the bandwidth of the system drastically. So, we compensate the loop with pole-zero pairs(Fig.26).

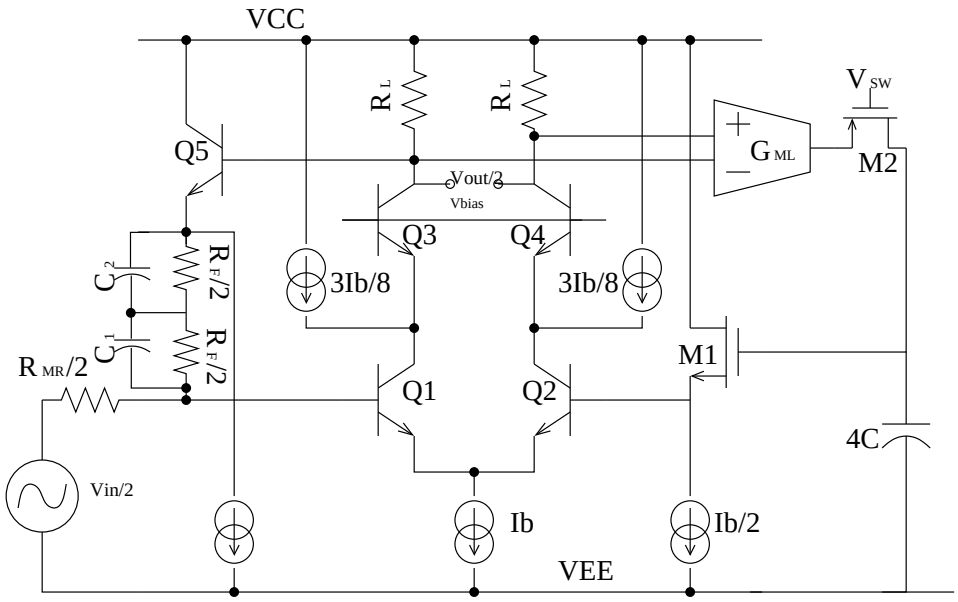

Fig. 26. Introduction of zero in the loop to stabilize it

To understand this in more detail we break the loop at the input driver transistor and analyze the open loop circuit[4]. The open loop circuit approximately looks as shown in Fig.27. Analysing this circuit one can write,

$$A_{open-loop} = \frac{(1+\eta\tau s)(1+\tau s)}{\eta s^2\tau^2 + (\beta+1)(\eta+1)\tau s + 2\beta + 1} \tag{6.20}$$

where $\tau = (R_F C_0)/2$ and $\beta = \frac{2R_F}{R_{mr}}$.

The zeroes are located at $\omega_{z1} = -1/(\eta\tau); \omega_{z2} = -1/\tau$ and the poles are at $\omega_{p1} = \frac{-1}{(\eta+1)\tau}; \omega_{p2} = \frac{-\beta(\eta+1)}{\eta\tau}$. ω_{z1} and ω_{p1} cancel each other as they are very close

[4] $\eta = C_2/C_1$(Fig.26).

together but ω_{p2} is very far away. Hence ω_{z2} acts like the compensating zero. The pole created is far away to be of any consequence.

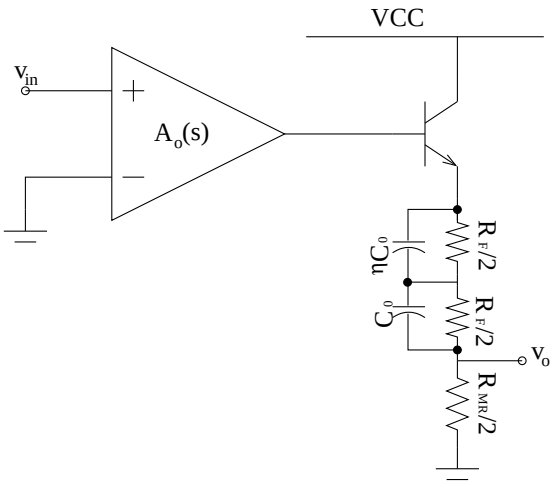

Fig. 27. Open loop diagram for the zero compensation scheme

The capacitor ηC_0(Fig.27) might seem unnecessary but a simple analysis of Fig.28 shows that,

$$A_{open-loop} = \frac{1+\tau s}{\beta + 1 + \tau s} \tag{6.21}$$

The effect of η is that it pushes the high frequency pole still further away and reduces its effect on the bandwidth of the system.

Hence forth high frequency analysis can be done using inspection if we assume that the other end of the input drive transistors is a DC. This is quite a valid assumption because all the high frequency signals are filtered out by the low pass filter.

It is important to see the parasitic capacitors C_{pi} in the light of signal feedthrough. The signal at higher frequencies will couple from one driver to the other and it is im-

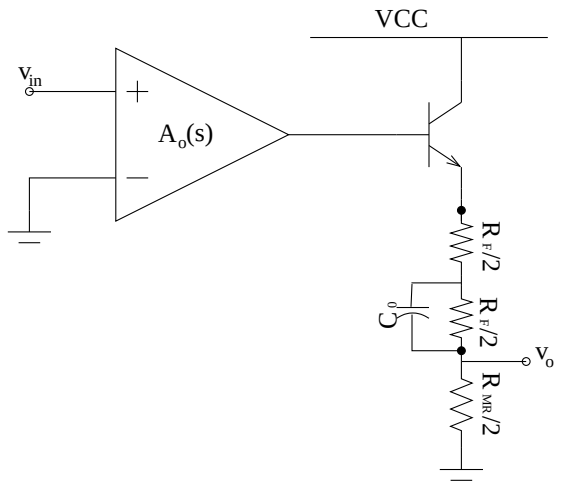

Fig. 28. Open loop diagram for the simple zero compensation scheme

portant to design the buffer[5] such that it doesnot effect us. The signal coupling leads to a formation of an unwanted zero which is dependant on the transconductance(g_m) of the buffer driver MOS. It is necessary to push the zero to higher frequencies so that it doesnot effect us.

Fig.29 depicts the half circuit at high frequencies. As mentioned before the MOS driver gate has been grounded to *represent* that this node is silent to high frequency signals. The output gain at high frequencies taking a simple R_f feedback without capacitors for zero is given by,

$$\frac{V_o}{V_{in}} = \frac{1}{A_1} \frac{1 + \frac{sCA_1}{G_{mL}} + \frac{s^2\left[CC_{gs}+C_{pi}(C+C_{gs})\right]}{g_{mN}G_{mL}}}{1 + s\left[\frac{2C}{G_{mL}A_o} + \frac{C_{gs}}{g_{mN}} + \frac{g_{pi}(C+C_{gs})}{g_{mN}G_{mL}A_o}\right] + s^2\frac{\left[2CC_{gs}+C_{pi}(C+C_{gs})\right]}{A_o g_{mN}G_{mL}}} \tag{6.22}$$

The terms used have been shown in Fig.29. $A_1 = G_{mL}R_{G_{mL}}$ where $R_{G_{mL}}$ is the output resistance of the low transconductance OTA. $A_o = G_m R_L$ when G_m is the

[5]The source follower after the low pass filter in the RIS half circuit is a buffer.

transconductance of the input drive BJT's. g_{mN} is the transconductance of the MOS buffer driver transistor.

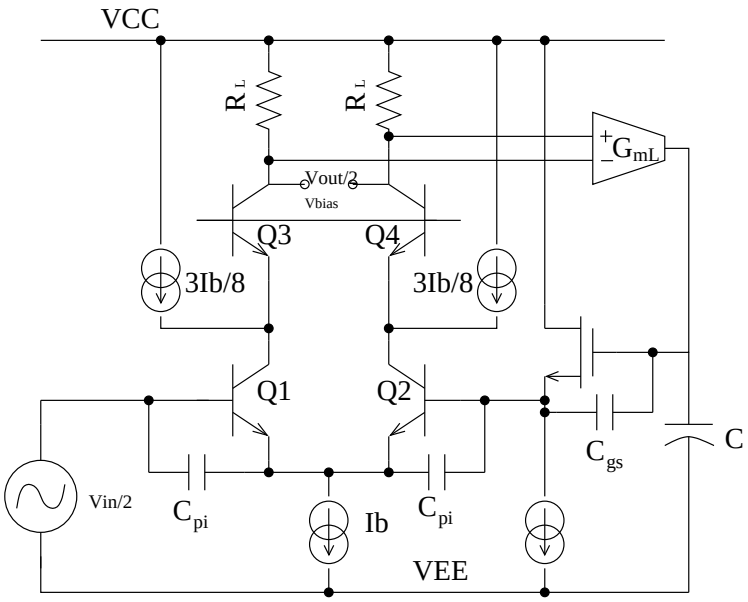

Fig. 29. Schematic to understand signal feedthrough due to parasitic base-emitter capacitor

The equation can be simplified if we assume $g_{mN} >> G_{mL}A_o$[6] and can be written as,

$$\frac{V_o}{V_{in}} = \frac{1}{A_1}\frac{\left(1+\frac{sCA_1}{G_{mL}}\right)\left(1+\frac{s(C_{gs}+C_{pi})}{g_{mN}}\right)}{\left(1+\frac{s2C}{G_{mL}A_o}\right)\left(1+\frac{s(C_{gs}+C_{pi}/2)}{g_{mN}}\right)} \tag{6.23}$$

Careful analysis hence shows that there is an extra pole zero combination formed due to C_{pi} and $\omega_z = g_{mN}/(C_{gs}+C_{pi})$;$\omega_p = g_{mN}/(C_{gs}+C_{pi}/2)$. If g_{mN} is small then the zero falls in band and shows us a response similar to Fig.30. Hence g_{mN} must be made large to ensure that this doesnot happen. It will be seen later that noise

[6]This makes sense because G_{mL} is very very small because of the low frequency corner spec.

becomes more critical than signal feedthrough and g_{mN} is ultimately decided by the noise performance of the system.

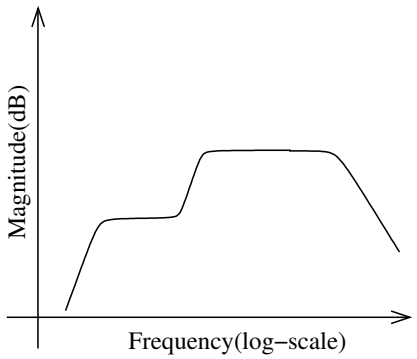

Fig. 30. Effect of feedthrough due to parasitics on AC response

3. Noise Performance

There is a gain of around 36 dB in the RIS. This ensures that the subsequent blocks are not very critical noise wise. The main sources of noise are the input drivers, the feedback resistance R_f, feedback buffer driver and feedback buffer current source. One would expect the buffer noise not to come into picture as input impedance of the driver is much smaller compared to R_{pi} of the bipolar and only a very small fraction of the MOS driver noise leaks through. But the noise of the MOS transistors is so large compared to the bipolar transistors that even after getting attenuated they still contribute to the system noise.

For the bipolars we will be concerned about *shot noise and base parasitic resistance thermal noise*. For the MOS we are only concerned about the thermal noise of the transistors. The $1/f$ noise of the transistors is not important because of the high pass characteristics of the transistor. Fig.31 represents a block level diagram of the RIS in the higher frequency range when the feedback OTA(G_{mL} in Fig.29) ceases to

function[7].The feedback connection of the R_f reduces the thermal noise performance of the matching resistance by the gain of the feedforward amplifier [1], [3].

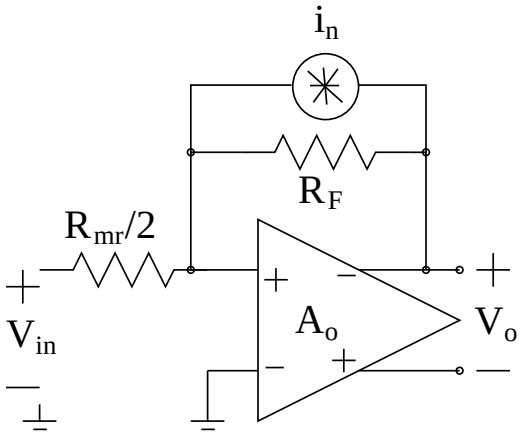

Fig. 31. Block level representation of the RIS at high frequencies

The output voltage in terms of current across the feedback resistance is given by,

$$\overline{V_o^2} = \left(\frac{2A_oR_F}{2A' + A_o}\right)^2 \overline{i_n^2} \tag{6.24}$$

where $A' = 2R_F/R_{mr}$, while the input to output transfer function can be written as,

$$\frac{V_o}{V_{in}} = \frac{2A_oA'}{2A' + A_o} \tag{6.25}$$

The input referred noise of the feedback resistor therefore can be written as,

$$\overline{v_n^2} = \frac{4kTR_F}{(A')^2} = \frac{4kTR_{mr}^2}{4R_F} \tag{6.26}$$

Since $R_{mr} << R_F$ this noise is greatly attenuated. Hence the only dominant

[7]The GBW of the OTA is so small the signal gets attenuated

sources of the noise are the two input bipolar drivers, and the MOS buffer driver and the buffer current source. The input referred noise for each is now calculated.

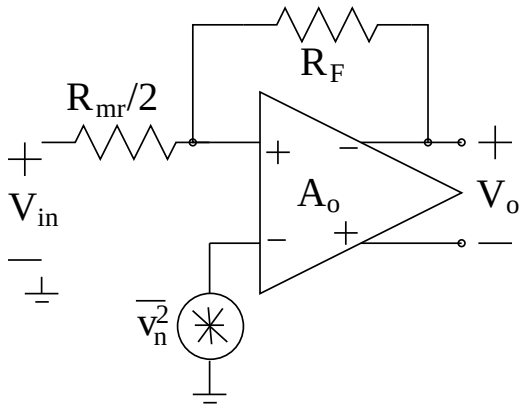

Fig. 32. Block level representation of the RIS at high frequencies for MOS noise

The noise of the MOS driver, its MOS current source and the *current noise* of the Q_2(Fig.29) can be coupled to one noise source[8]. After calculating the equivalent voltage noise source(by also including the voltage noise of Q_1,Q_2) at the input of Q_2 in Fig.17 we can simplify the diagram as in Fig.32. The output noise transfer function is hence calculated as,

$$\overline{V_o^2} = \left(\frac{2A_oA'}{2A' + A_o}\right)^2 \overline{v_n^2} \tag{6.27}$$

The current noise for Q_1 when referred to the input behaves differently. For the current noise(Fig.33) we can calculate the output voltage transfer function to be,

$$\overline{V_o^2} = \left(\frac{2A_oR_F}{2A' + A_o}\right)^2 \overline{i_n^2} \Rightarrow \overline{V_{in}^2} = \left(\frac{R_F}{A'}\right)^2 \overline{i_n^2} = \frac{R_{mr}^2}{4}\overline{i_n^2} \tag{6.28}$$

[8]The total power being the sum of the three individual noise powers.

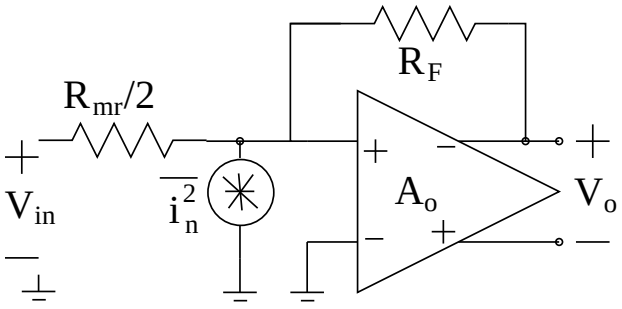

Fig. 33. Block level representation of the RIS at higher frequencies for BJT current noise

Current noise due to MOS sources is $\approx \frac{8}{3}kT(g_{mN} + g_{mNc})$ where g_{mNc} is the transconductance of the MOS current source; and that due to Q_2 is $2qI_B + \frac{2qI_C}{|\beta(j\omega)|^2}$[9]. The input voltage noise hence can be written as,

$$\overline{v_{n1}^2} = \left(\frac{8}{3}kT(g_{mN}+g_{mNc})+\left(2qI_B+\frac{2qI_C}{|\beta(j\omega)|^2}\right)\right)\left|\frac{1}{g_{mN}+G_{pi}+j\omega(C_{pi}+C_{gs})}\right|^2 \quad (6.29)$$

The current noise of Q_1 is modified by $|R_{mr}/2|^2$. Hence assuming matched input transistors the total noise can be written as,

$$\overline{v_n^2} = \left(\frac{8}{3}kT(g_{mN}+g_{mNc})+\left(2qI_B+\frac{2qI_C}{|\beta(j\omega)|^2}\right)\right)\left|\frac{1}{g_{mN}+G_{pi}+j\omega(C_{pi}+C_{gs})}\right|^2 + \left(2qI_B+\frac{2qI_C}{|\beta(j\omega)|^2}\right)\left|\frac{R_{mr}}{2}\right|^2 + 2\cdot(4kTr_b) \quad (6.30)$$

r_b is the parasitic base resitance of the BJTs. The tradeoff here is between the voltage noise($4kTr_b$) and the current noise. Increasing the sizes of the input drivers reduces the effect of the parasitic resistance. At the same time if high frequency per-

[9] β is a function of frequency, see Eq (6.9)

formance is desired, larger transistors require higher currents. High currents increase the shot noise in the transistors, increasing the current noise. Hence the sizes of the transistors must be optimally chosen for low noise.

One important effect in the bipolars [6] on input referred noise is due to the degradation of the current gain(β) of the transistors with frequency. The current gain bandwidth is less than the voltage bandwidth and this shows on the input referred noise which starts increasing after a certain point of time. This is clearly seen in Eq. (6.30).

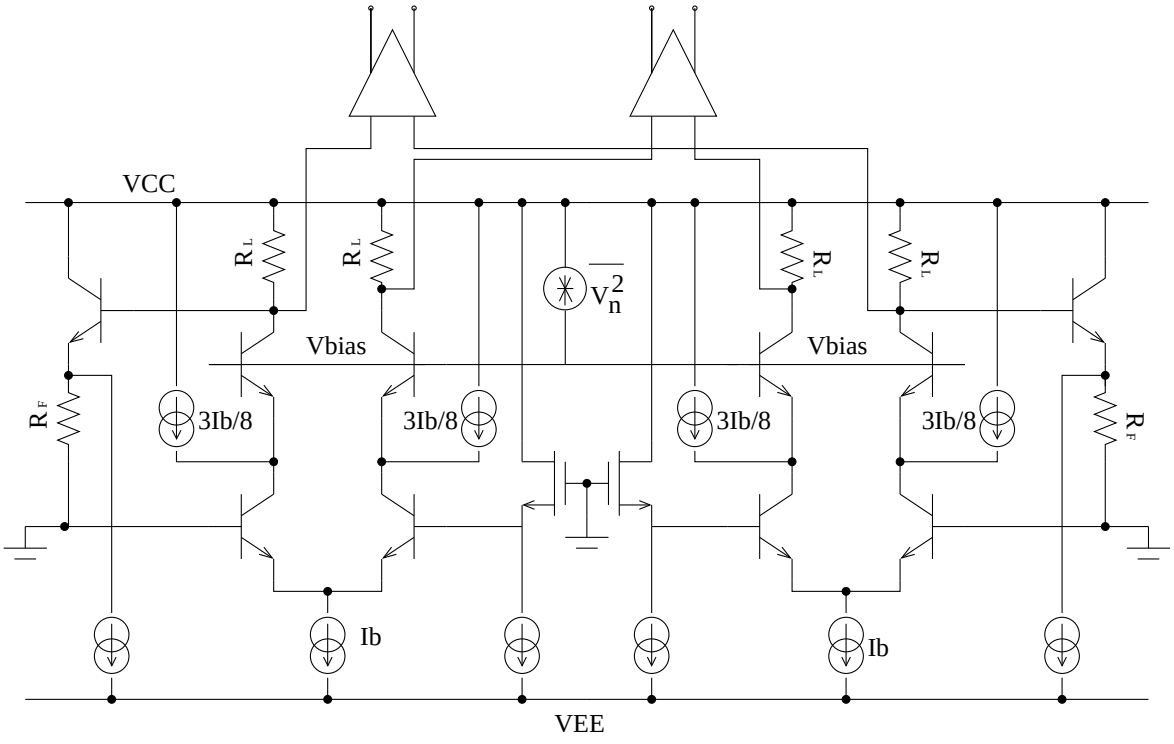

Fig. 34. Cascode bias circuit noise

It is also important to carefully bias the transistors because unnecessary bias circuitry can add to noise. Fig.34 shows the simplified diagram of the RIS. When the cascode transistors are biased with the same circuit then all its noise becomes common

mode. A noise perturbation in one cascode transistors also means a correlated noise disturbance at the corresponding cascode transistor in the other half.

D. Proposed Backend of the Preamplifier

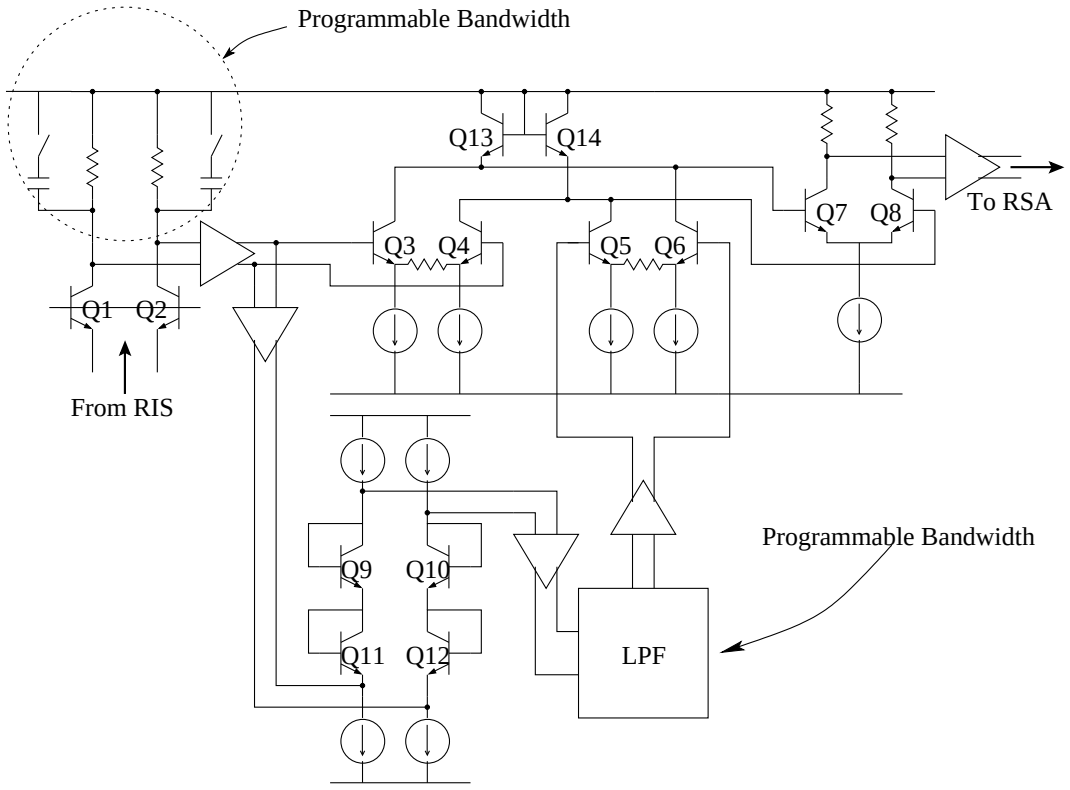

Fig. 35. Read middle amplifier schematic

The *Backend* of the preamplifier is divided into two subblocks, RMA and RSA. The RMA is that part of the preamp which has programmable bandwidth and high pass corners incorporated in it. The RSA has programmable gain and is the output stage of the preamplifier that needs to drive the signal to the read channel. Fig.35 represents the schematic diagram of the RMA. The details of the low pass filter are shown in Fig. 36.

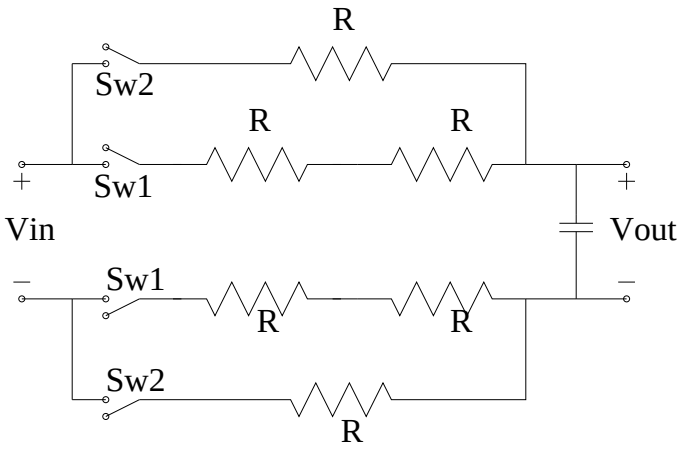

Fig. 36. Low pass filter used in the RMA

The core of the both these blocks is the multiplexer/summer block. The conventional implementation is using cascode blocks(Fig.37). The low impedance node of the cascoded transistors is used for the multiplexing/summing.

But cascodes need high voltage head room to operate. For low voltage applications the translinear amplifier can be used. The translinear amplifier is commonly used in VGA's as multipliers [9]. The low impedance node in the translinear amplifier can be used with the same functionality as that of the cascode. Fig.38 shows a translinear circuit with the small signal current distribution.

Assuming that the emitter degeneration is large enough, we can assume that the voltage to current conversion is linear. So large signal voltage V1 can be written as,

$$V1 = V_T \ln\left(\frac{I_b + i}{I_b - i}\right) \tag{6.31}$$

Also the output currents in the differential pair(Q5-Q6) can be written as,

$$V1 = V_T \ln\left(\frac{I_b - i1}{I_b + i1}\right) \tag{6.32}$$

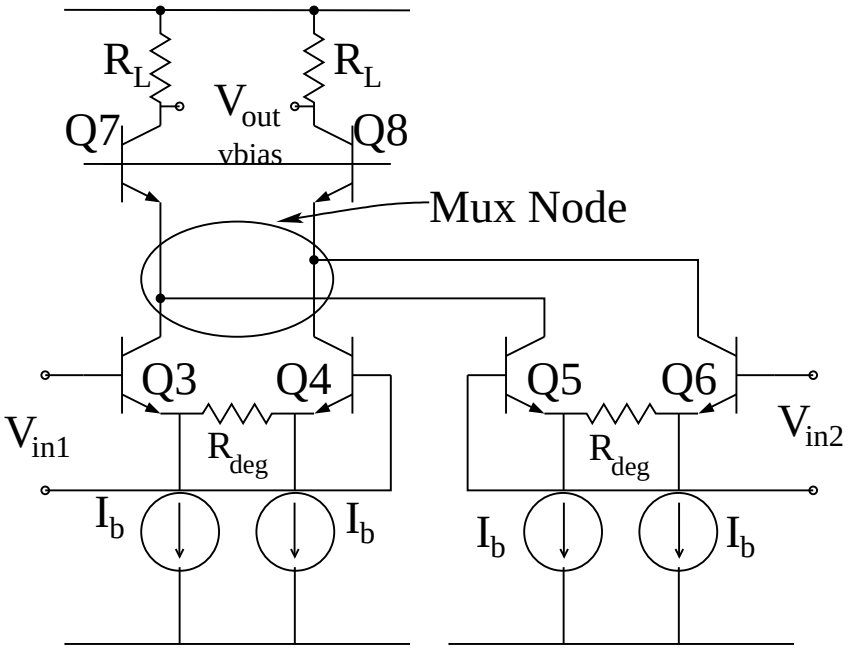

Fig. 37. Cascode structure used for multiplexing/summing

$$V_{out} = 2i1R_L; V_{in} = iR_{deg} \tag{6.33}$$

Hence we can write,

$$\frac{V_{out}}{V_{in}} = -\frac{2R_L}{R_{deg}} \tag{6.34}$$

Since this is a large signal analysis, linearity is dependant only on the input degeneration. Output voltage range is higher for the translinear circuit by at lease V_{be}. When the output voltage comes down in the translinear circuit it needs to be above the collector voltages of Q3-Q4. For the cascode they need to be above the base bias of the cascoded transistors which at least V_{be} above the collector voltages of Q3-Q4.

The signal in the RMA is sent through a low pass filter and then subtracted

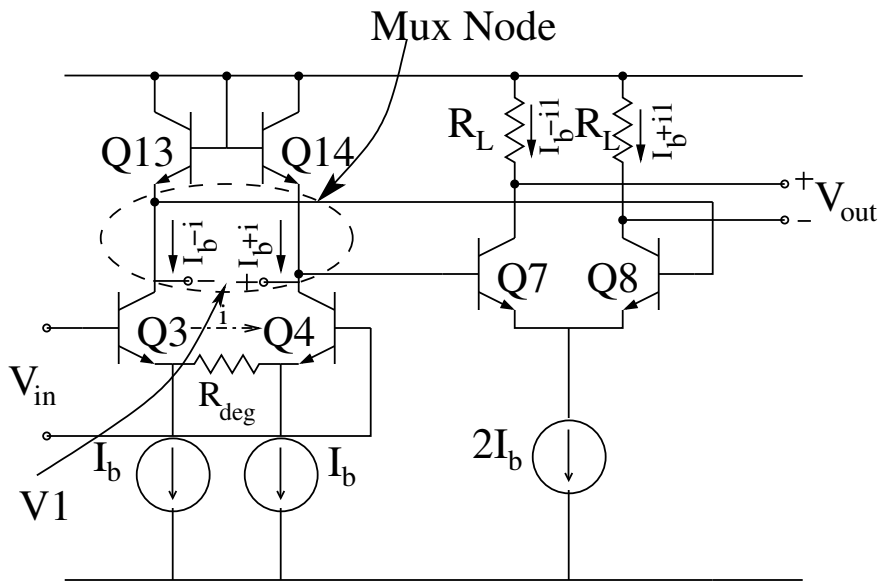

Fig. 38. Translinear circuit

from itself to generate the high-pass corner. The low pass filter has programmable bandwidth and hence we have the programmable high-pass corners. Programmable bandwidth of the preamplifier is obtained by connecting a bank of capacitors across the resistance receiving the signal from the RIS as shown in Fig.35.

The RSA(Fig. 39) has a translinear circuit at its core. The different branches are switched for gain programmability. The output stage(Fig.40) is an emitter follower followed by a resistive termination to the output flex connecting the preamplifier to the read channel. R_{ch} is the matched impedance seen by the flex connecting the preamplifier to the read channel.

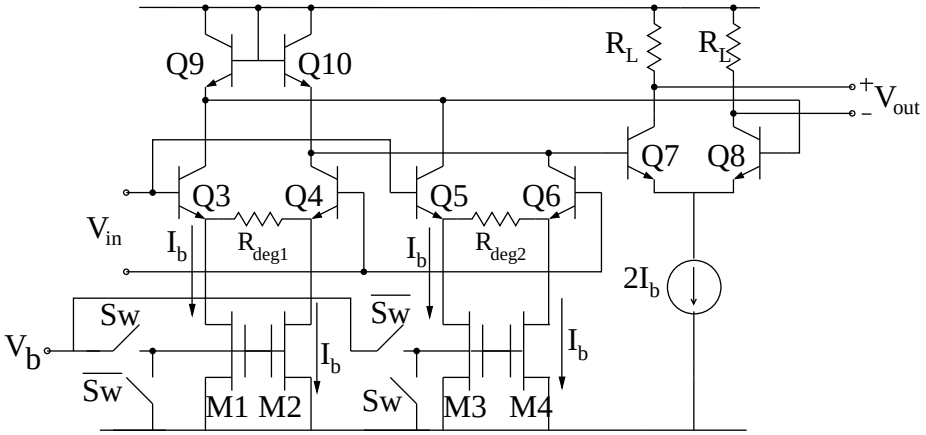

Fig. 39. RSA schematic

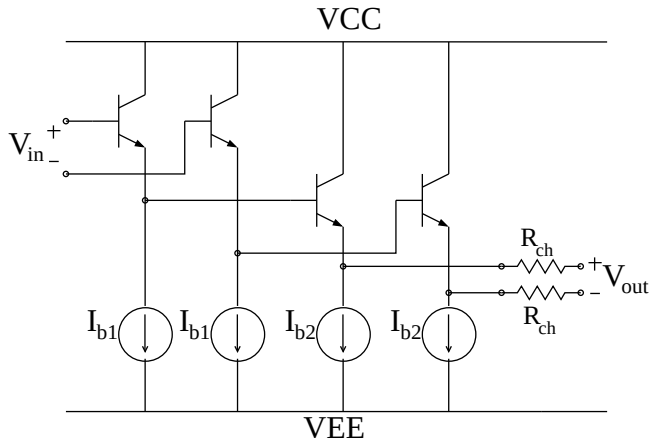

Fig. 40. Output stage

CHAPTER VII

POST LAYOUT SIMULATION RESULTS

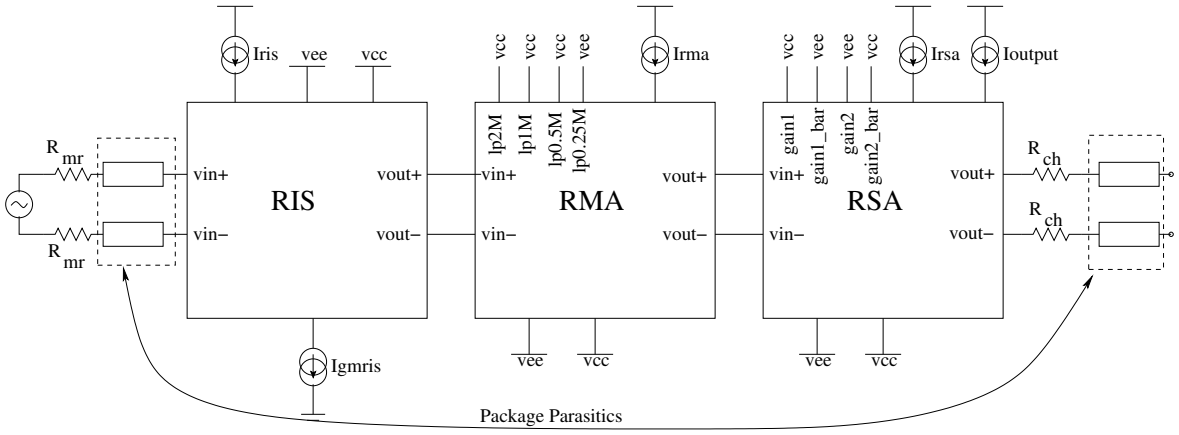

Fig. 41. Block level representation of the final circuit

The post layout simulations of the preamplifier are summarized here. Of the many parasitics the capacitance of the interconnect to other interconnects and the substrate are crucial for the high frequency performance of the circuit. These are modeled in the *IBM5HP* toolkit as *Raphael capacitors* and can be utilized by including them during the extraction of the layout for high frequency simulations. The package parasitics of the LQFP48A have also been added in the final simulations(Fig.41). The chip has reverse biased diodes connected to the supplies for bias pins protection against ESD(Electro Static Discharge). For floating nodes additional protection has been provided by connecting the gates to series resistance and protecting them from voltage spikes due to charge dumping on the gates.

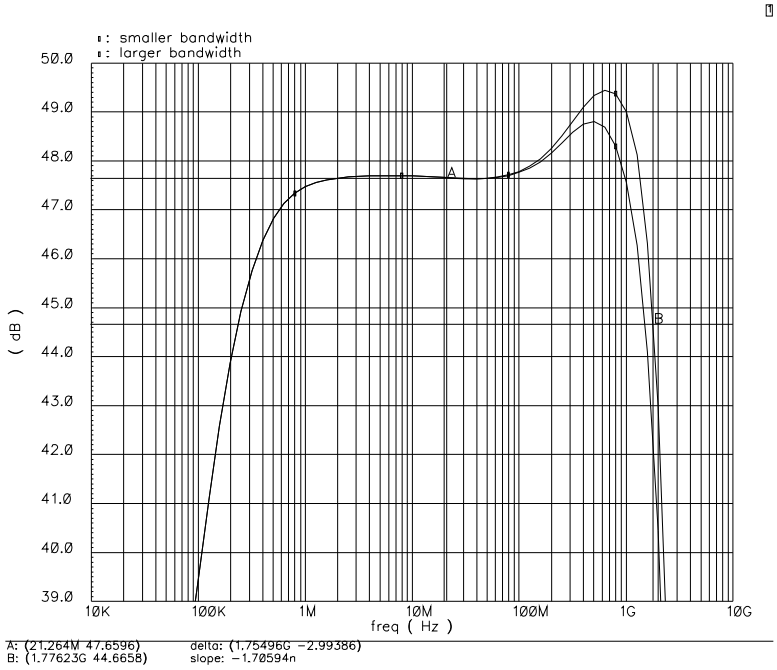

Fig. 42. Higher bandwidth of the preamplifier

A. Results

Tables III,IV,V give the important circuit parameters of the 3 blocks of the preamplifier. The frequency response of the preamplifier is shown in Fig.42 for different bandwidths. Single bit programmability has been incorporated for the gain and bandwidth while its 2-bit for the high pass corners. Fig.43 shows the gain of the preamplifier. The response of the preamplifier is broadband with a high pass corner. The different gains of the preamp are 42 dB and 47.6 dB. The DC rejection is $<$ -40 dB. A 150 mV offset at the input appears as 1.5 mV offset at the output which is not a problem.

Fig.42 and Fig.44 show the different bandwidths of the preamplifier. The higher

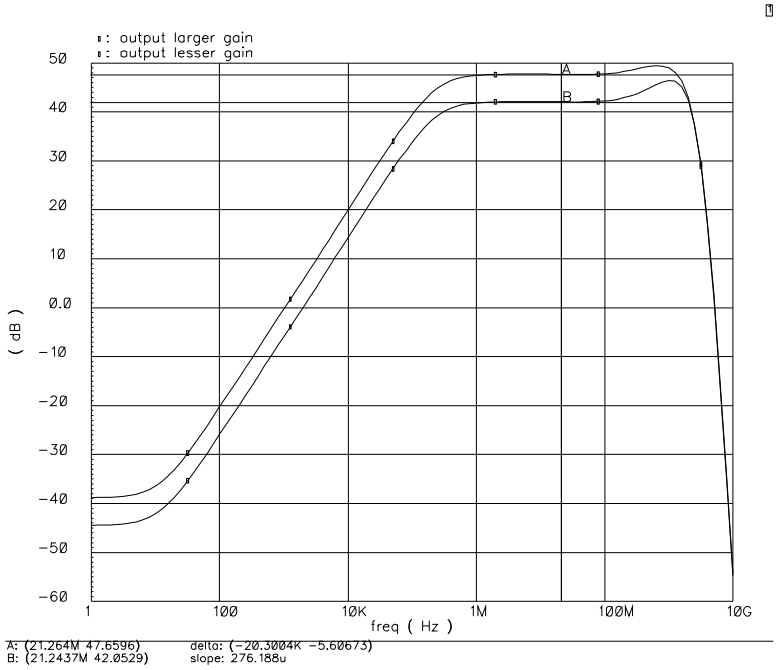

Fig. 43. Variable gain of the preamplifier

bandwidth is 1.76 GHz while the lower bandwidth is 1.47 GHz. This programmability is included in case noise becomes more critical than the bandwidth while reading a particular section of the data. Though the change in SNR might seem very small, Hard Disk Drives require very small Bit Error Rates(BER) to function and even small changes in the SNR can affect the BER.

Variable high pass corners are needed in the preamplifier to help it recover faster while moving from write mode to read mode. Lower corners are needed only while reading the servo information which is low frequency. Fig.45 shows the different programmed corners of the preamplifier. The corners are supposed to be at 250KHz, 500KHz, 1MHz and 2MHz with a allowed variation of $\pm 10\%$.

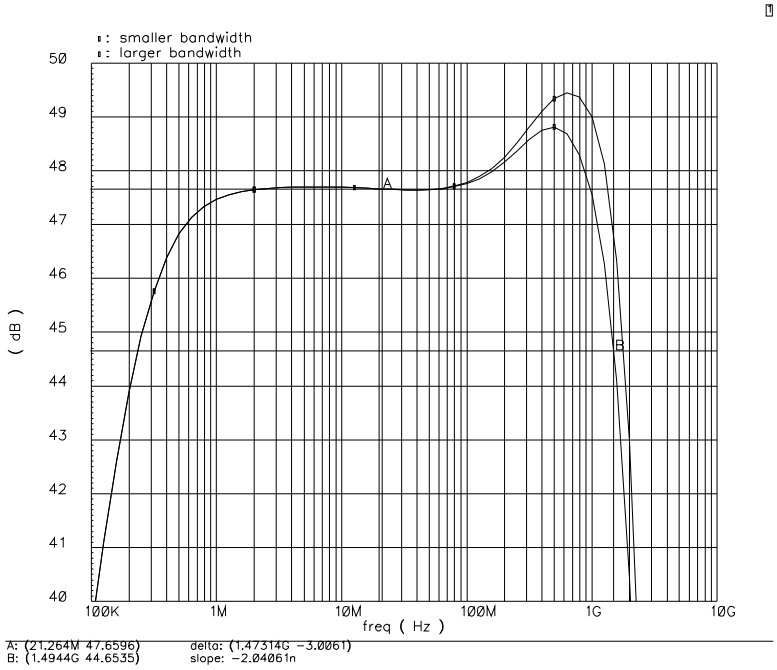

Fig. 44. Lower bandwidth of the preamplifier

The input resistance of the preamplifier needs to match 70Ω characteristic impedance of the flex. The matching needs to be resistive because it is over a broad band of frequency. Fig.46 shows the overall response of the input resistance. The high input resistance at lower frequencies shows the effect of feedback at low frequencies that holds the base of one of the input drivers and prevents the diff-pair from drawing any signal current.

At higher frequencies, the feedback dies down and lets R_f feedback take over. Zooming into Fig.46 the input resistance over a broad range of frequencies looks like Fig.47. The input resistance starts increasing at high frequencies. This is because of the *inductive effect of the feedback bipolar transistor*. At low frequencies the output

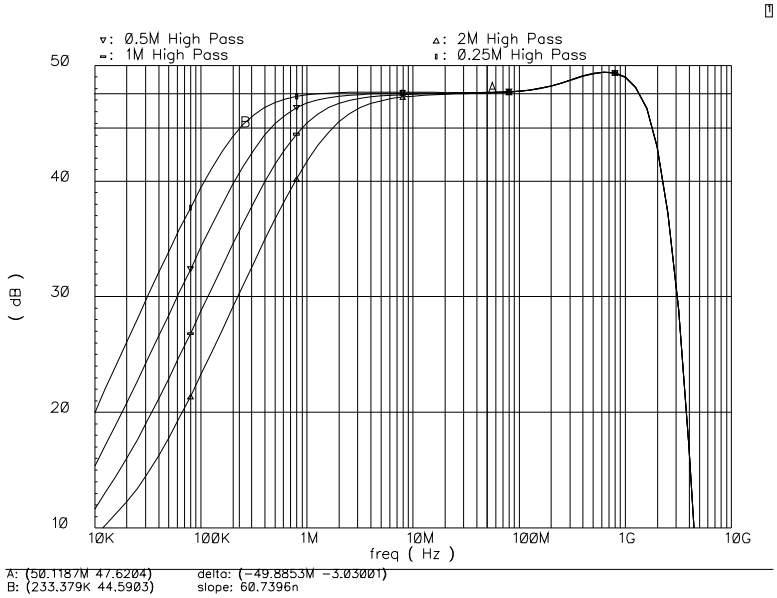

Fig. 45. High pass corners of the preamplifier

impedance of this bipolar is close to r_e but at high frequencies it rises due to the coupling of the load resistance through the C_{be} capacitor.

The preamplifier output needs to be around 300 V_{pp}. This is shown in Fig.48. Fig.49 shows a HD3= $60dB$.

Table II summarizes the final results of the preamplifier. The preamplifier has not been tested for process, supply and temperature variations. Even though the empirical rule for the bandwidth requirement for 3 Gb/s data rates is 0.6∗Data-rate, preamplifiers with bandwidths equal to 0.5∗Data-rate also work well. The optimization for process, supply and temperature variations should ensure a bandwidth of at least 1.5 GHz. The final layout is shown in Fig. 53.

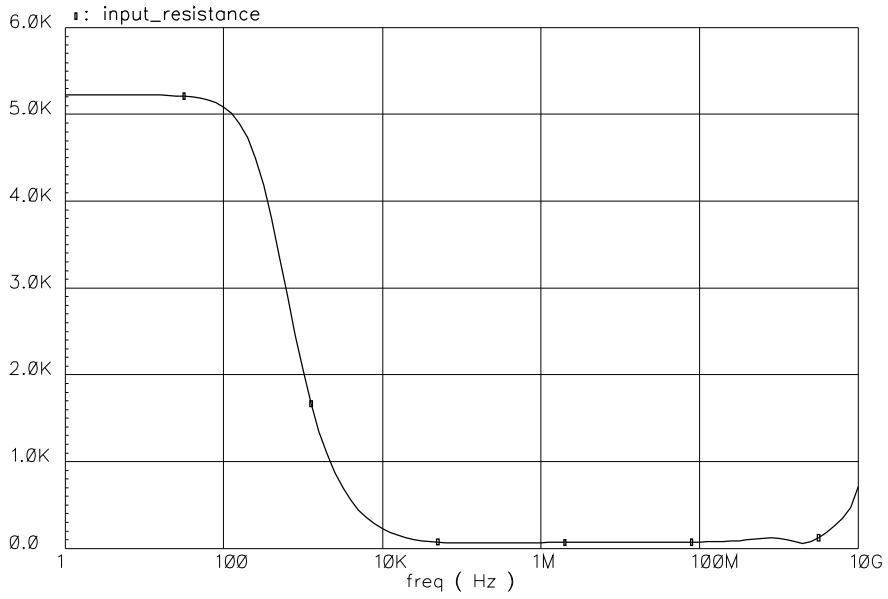

Fig. 46. Overall input resistance

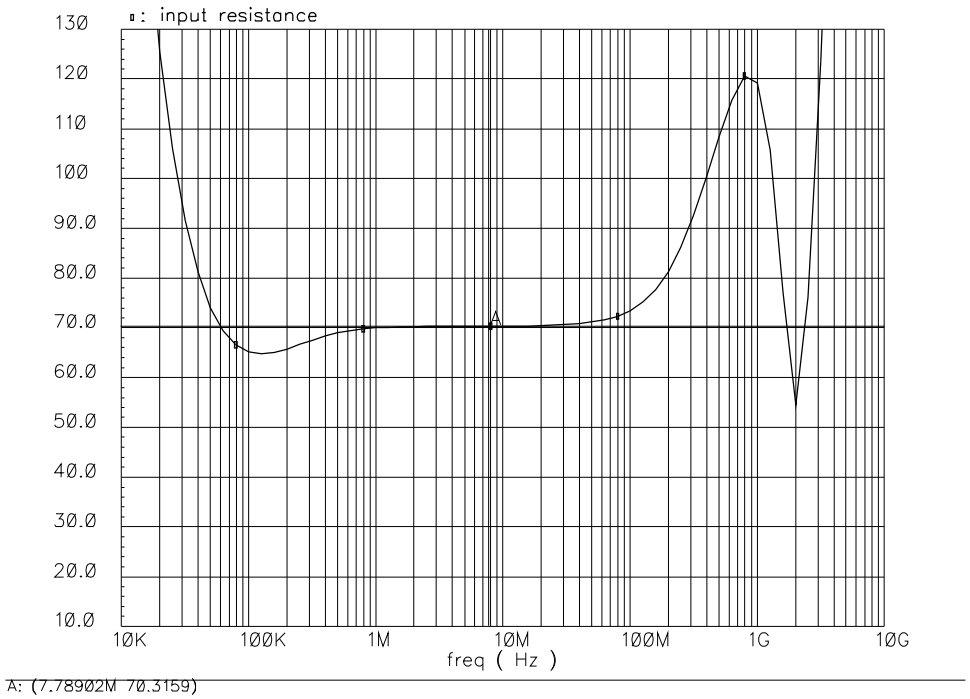

Fig. 47. Input resistance of the preamplifier

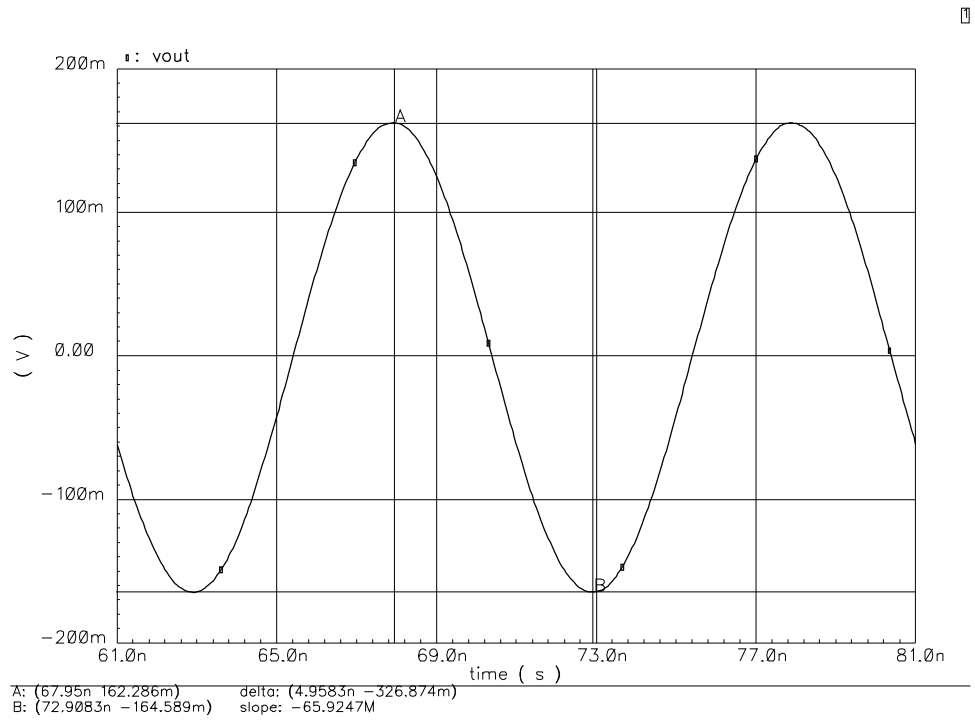

Fig. 48. Output transient response of the preamplifier

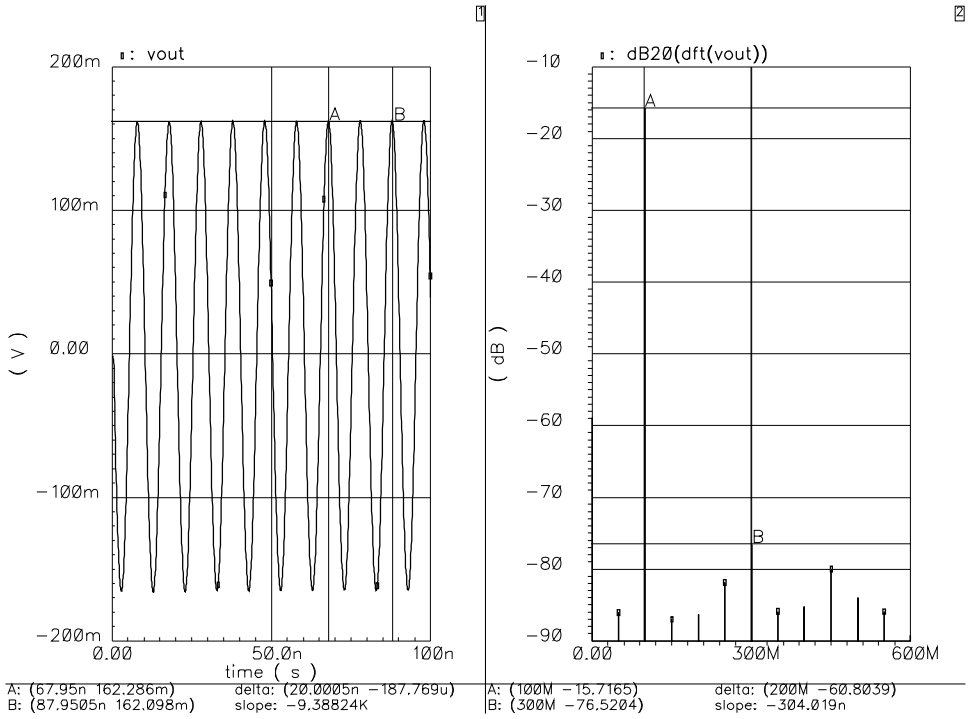

Fig. 49. Output THD of the preamplifier

Table II. Final results of the preamplifier.

$\mathbf{S_{no}}$	**Parameters**	**Values**
1	Gain	42/47dB
2	Bandwidth	1.47/1.75 GHz
3	High Pass Corner	0.25/0.5/1/2 KHz
4	Noise	$1.94\frac{nV}{\sqrt{Hz}}$ at 100 MHz
5	THD	0.13%, $V_{outpp} = 300mV$
6	R_{in}	70 Ω
7	PSRR	$< -50dB$
8	CMRR	$< -50dB$

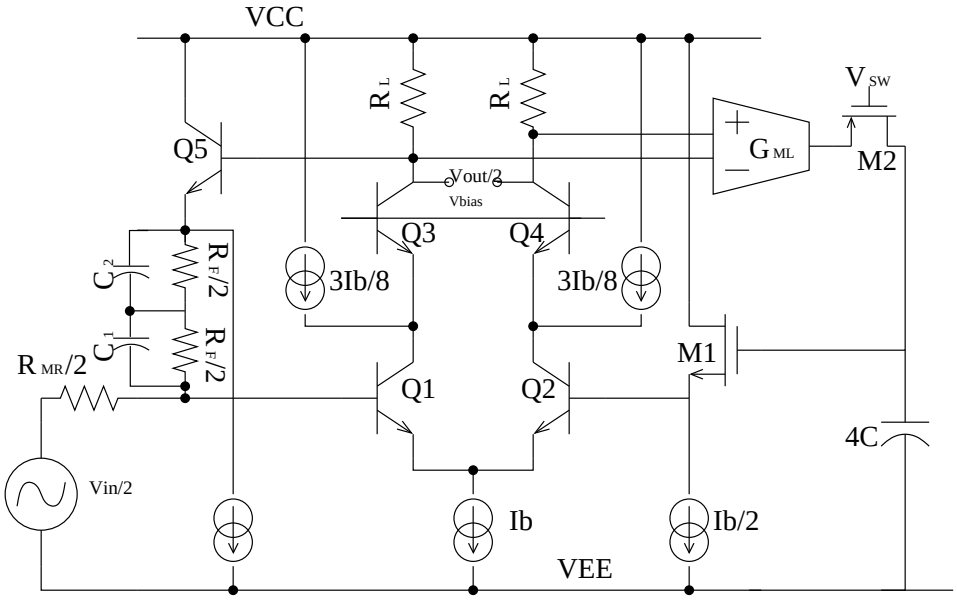

Fig. 50. RIS half circuit

Table III. Important circuit parameters and bias currents of RIS(Fig.50).

S_{no}	**Parameters**	**Values**
1	Q1,Q2(emitter area)	$3 \times 20\mu m \times 0.5\mu m$
2	Q3,Q4(emitter area)	$5\mu m \times 0.5\mu m$
3	Q5	$2.5\mu m \times 0.5\mu m$
4	M1	$\frac{W}{L} = 30 \times \frac{40\mu m}{1\mu m}$
5	M2	$\frac{W}{L} = \frac{40\mu m}{1\mu m}$
6	R_F,R_L	2.85KΩ,800Ω
7	C_2,C_1	$200fF$,$45fF$
8	I_b	$12mA$

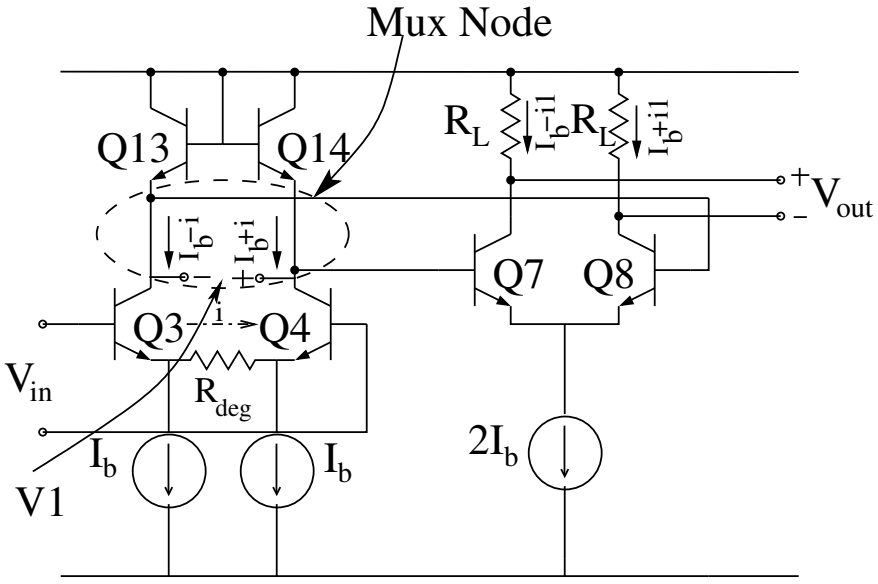

Fig. 51. Translinear core of the RMA

Table IV. Important circuit parameters and bias currents of RMA(Fig.51).

S_{no}	**Parameters**	**Values**
1	Qk(k=3-4)	$5\mu m \times 0.5\mu m$
2	Qk(k=7-8)	$5\mu m \times 0.5\mu m$
3	Qk(k=13-14)	$5\mu m \times 0.5\mu m$
4	R_{deg},R_L	800Ω
5	I_b	$750\mu A$

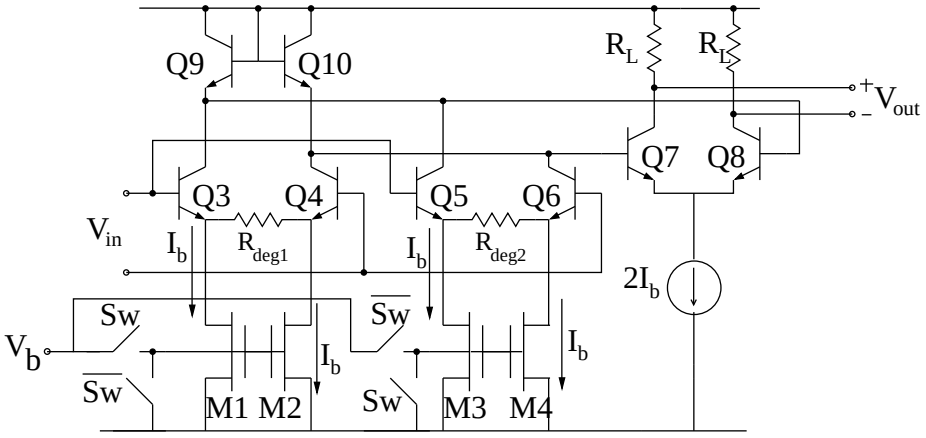

Fig. 52. RSA schematic

Table V. Important circuit parameters and bias currents of RSA(Fig.52).

S_{no}	**Parameters**	**Values**
1	Qk(k=3-10)	$5\mu m \times 0.5\mu m$
2	Mk(k=1-4)	$\frac{W}{L} = 6 \times \frac{20\mu m}{2\mu m}$
3	R_{deg1},R_{deg2},R_L	1KΩ,2KΩ,1.6KΩ
4	I_b	$750\mu A$

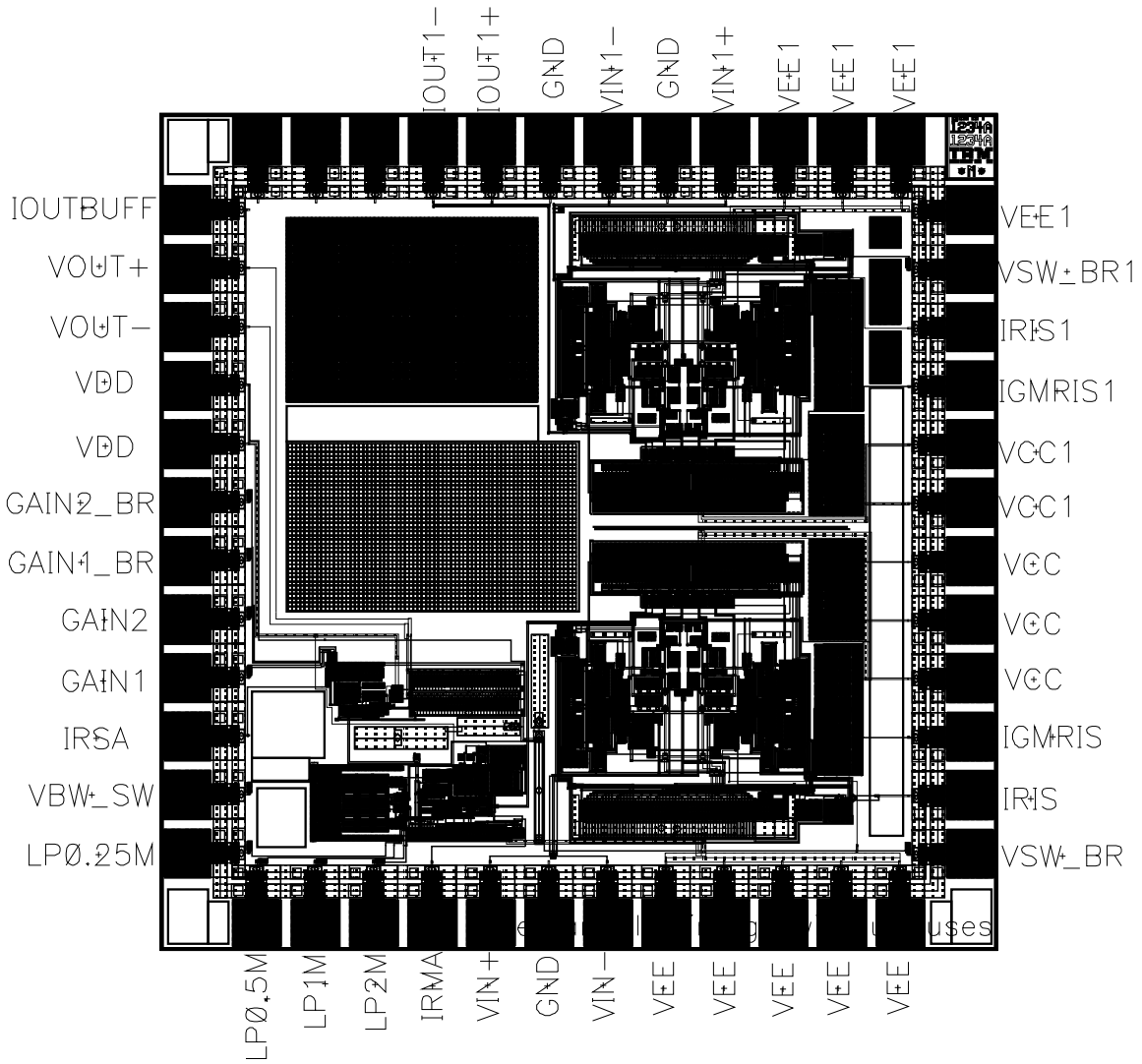

Fig. 53. Final layout of the preamplifier

CHAPTER VIII

CONCLUSIONS

The preamplifier has been designed for a TGMR read head whose resistance hovers around 240Ω. With the gain and noise specifications to be met the input transistors are large enough to present parasitic capacitances $> 0.5pF$. This puts the input pole at $\approx 2.6GHz$. The large input resistance of the read head hence limits the speed of the preamplifier for the used process. The input capacitance can be reduced at the cost of noise performance by reducing the transistor areas.

Low noise requirements require the matching resistance to be placed in feedback. Any high frequency loop will have a tendency to be unstable because of the absence of a dominant pole. Introduction of a zero in the loop stabilizes it without effecting the high frequency response of the circuit. The need to stabilize the loop creates more limitations on the bandwidth of the preamplifier.

There is a tradeoff between voltage noise and current noise. The voltage noise is determined predominantly by the parasitic base resistance of the drivers. To reduce this noise large area transistors are used which have lesser base parasitic resistance. For high frequency operations therefore large currents must be pumped[1]. This increases the shot noise of the drivers which leads to an increase in current noise. For low noise this tradeoff must be optimized.

Signal feed-through due to parasitic capacitors creates unwanted zeroes in the current architecture. For proper functioning of the system these must be pushed out of the band of interest.

As the signal becomes larger in the later stages, linearity becomes important.

[1]The f_t of bipolars is dependant on biasing.

Translinear circuits provide us with a way of realizing the preamplifier functions using low supplies without compromising on linearity.

A. Future Work

The preamplifier is the interface between the read channel and the magnetic media. It is therefore required to read the data from the media to the read channel as well as write the data sent by the read channel onto the magnetic media.

This project deals only with the read path of the preamplifier. The writing of data onto the magnetic data, at the rates which the read path has been designed and for limited supplies, can be quite challenging.

When writing and reading data at such high speeds it is necessary to switch fast from write mode to read mode otherwise lot of time is spent in the transitions and the advantage of reading and writing at high speeds is lost. The preamplifier needs to be modified for fast switching between the two modes. The transition from write to read mode is especially important.

The project could finally be extended to include the AGC and the loop filter also in the preamplifier. High speed SiGe processes should make these designs easy and compact. This makes the read channel an essentially digital block making it easier to design and cheaper to fabricate.

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VITA

Ramachandra Murthy Mellachervu was born in Machlipatnam, India. He received his B.Tech. degree from the Indian Institute of Technology, Chennai, India in 2001. He is presently working toward his M.S. degree under the supervision of Dr. Jose Silva-Martinez in the Analog and Mixed Signal Center, Texas A&M University. From August 2002 to May 2003 he had an internship with Texas Instruments in Dallas, TX. His research interests are focused on integrated radio frequency circuit designs for wireless receivers. He held a Texas Instruments research assistantship in 2001. He has been an IEEE student member since 2001. He can be reached through the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843.

The typist for this thesis was Murthy Mellachervu.