DESIGN OF A 3.3 V ANALOG VIDEO LINE DRIVER WITH CONTROLLED OUTPUT IMPEDANCE

A Thesis

by

NARAYAN PRASAD RAMACHANDRAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2003

Major Subject: Electrical Engineering

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ABSTRACT

Design of a 3.3 V Analog Video Line Driver with

Controlled Output Impedance. (May 2003)

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The internet revolution has led to the demand for high speed, low cost solutions for providing high bandwidth to the consumers. Cable and DSL systems address these requirements through sophisticated analog and digital signal processing schemes. A key element of the analog front end of such systems is the line driver which interfaces with the transmission medium such as co-axial cable or twisted pair.

The line driver is an amplifier that provides the necessary output current to drive the low impedance of the line. The main requirements for design are high output swing, high linearity, matched impedance to the line and power efficiency. These requirements are addressed by a class AB amplifier whose output impedance can be controlled through feedback. The property of this topology is that when the gain is unity, the output resistance of the driver is matched to the line resistance.

Unity gain is achieved for varying line conditions through a tuning loop consisting of peak-to-peak detectors and differential difference amplifier. The design is fabricated in 0.5 μ AMI CMOS process technology. For line variations from 65 Ω to 170 Ω, the gain is unity with an error of 3 % and the impedance matching error is 20 % at the worst-case. The linearity is better than 50 dB for a 1.2 V peak-to-peak signal over the signal bandwidth from 10 kHz to 5 MHz and the line resitance range from 65 to 160 Ω.

To my first teacher, Ms. Kausalya

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I am indebted to my colleagues in the AMSC group with whom the long hours of interaction and discussion have resolved several doubts and provided insights into aspects that I would otherwise have ignored. Finally, I am grateful to my parents and sister who inspired me to pursue my dreams.

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CHAPTER I

INTRODUCTION

The 1990s saw the creation of the “information superhighway”, an infrastructure that can provide high-speed data communications for business, entertainment and interactive services. The need to provide low-cost affordable service without compromising quality has led to the reuse of existing telephone and cable networks. This has led to expanding their capabilities for high volume data through sophisticated analog front-end solutions. The demand for information has led to the mushrooming of several competing technologies such as wireless LAN, Bluetooth, DSL and cable broadband services. DSL (Digital Subscriber Lines) and cable modem technology provide voice, data and real-time images over the existing twisted-pair or co-axial cables by using additional hardware at the transmission and reception end. Thus, low cost and high bandwidth services are made possible to home offices and business.

A typical system architecture of a wireline communication system as in DSL and cable services is shown in Fig. 1. The digital data from the DSP is interpolated and

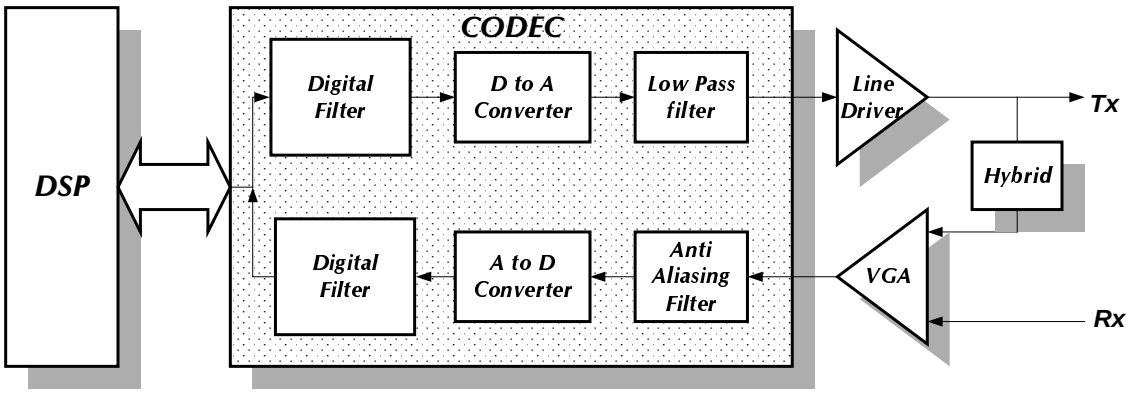


Fig. 1. Block diagram of wireline communication system.

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits*.

modulated by the digital filters. The DAC converts these signals into analog waveforms, which are then filtered using an analog low-pass filter to attenuate the images. The analog signals are then fed to the line driver, which acts as a high-speed buffer. The hybrid isolates the incoming signal and reduces interference from the transmission side, known as near end cross talk (NEXT). The incoming signals are boosted by the VGA (variable gain amplifier) and high-pass filtered to remove the low frequency transmission components. The ADC converts the analog data into digital bits, which are decimated and pre-processed in the digital filter blocks. The digital bit stream is then extracted and sent to the DSP.

The important link between the sophisticated DSP algorithms and the analog signals riding the cable are hybrid circuits, of which the line driver is a key element. Line drivers find application in ISDN transceivers, DSL and cable modems to drive the analog signals onto the communication channel or medium. The line driver is part of the analog front-end transmitter for wired communication systems, analogous to the power amplifiers in wireless transmission. Line drivers are voltage amplifiers or buffer that provide the necessary output current to drive the low load impedance (nominally matched to the line impedance), which is nominally between 50-150 ohms, but varies upon the cable length, quality and other line impairments. The main requirements of a line driver are high output swing, high linearity, impedance matching and good power efficiency as summarized in the following sections.

A. LINE DRIVER SPECIFICATIONS

1. Output Voltage Swing

The attenuation along the cable is exponentially proportional to the cable length and radius. As a result, high output swing is required so that the signal can be differentiated from the noise at the receiver end or the repeater. Furthermore, modulation techniques such as discrete multi-tone (DMT) distribute information in discrete tones that can be treated as pseudo-random noise in time domain [1]. These tones add up to create

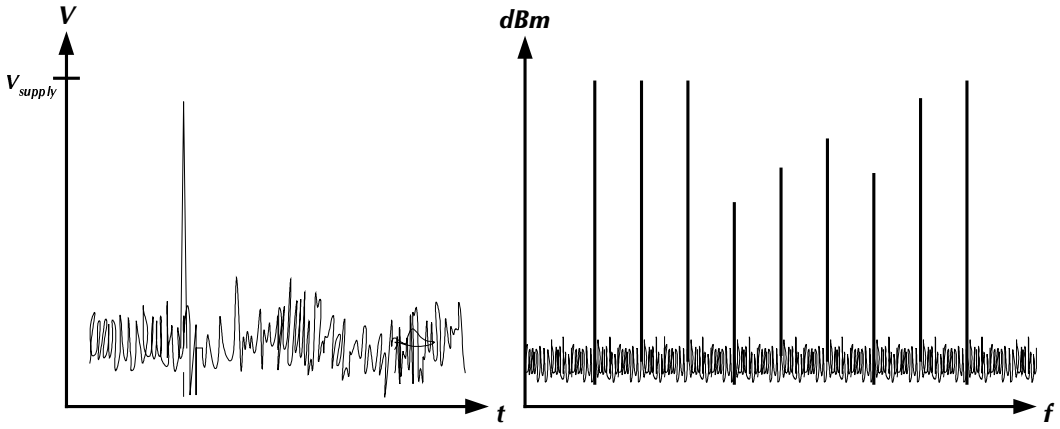


Fig. 2. DMT signals in time and frequency domain.

high crest factor (peak-to-average voltage ratio), which can exceed the linear range of the amplifier or hit the supply rails.

Fig. 2 shows the time domain response and the frequency spectrum of a transmitted DMT signal. Multiple tones add up in amplitude to create peaks that reach close to the supply voltage (V_{supply}). Although this occurs quite infrequently, the necessity to handle such worst-case conditions force a higher power consumption and lower efficiency for the line driver. Additionally, back termination requirements are required for impedance matching. This causes half the voltage to drop across the series resistor even before actual transmission.

2. Linearity

One of the important parameters of a communication system is the bit error rate (BER) at the receiver, which is correlated with the distortion in the analog blocks. Excessive distortion requires more effort on the DSP for sophisticated algorithms to implement error correction [1]. Thus, high dynamic range of the line driver ensures lower BER of the overall system. The system performance in multi-carrier data transmission systems is also judged by the 2-tone and multi-tone tests, wherein the power in the inter-modulation components is compared to the actual signal power. In Fig. 3, transmission

components (f_1 and f_2) create tones at $2f_2$-f_1 and $2f_1$-f_2. IM3 measures difference in the power of transmitted signal and tones. Similarly MTPR (multi-tone power ratio) compares the power in the transmitted bands to the distortion in a band that has been transmitted empty (f_3). These components need to be as small as possible (lower than 60 dB usually) in-order not to corrupt the data.

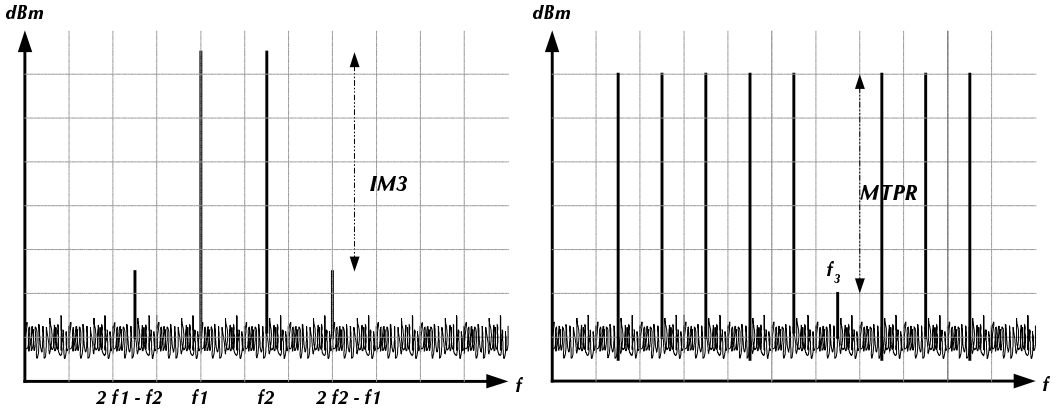


Fig. 3. Two-tone and Multi-tone Test.

3. Impedance Matching

The line impedance is subject to variations due to loading effects, the line length variation and line quality [2]. Without matching, the reflections are not canceled at the transmitter end, which may degrade the driver performance. Thus line terminations at the receiver and transmitter end are required to eliminate signal reflections. A series termination is the most common solution at the driver end. This series resistance is matched to the nominal line resistance. However, as mentioned before, this causes a reduction in voltage swing due to the resistor drop. Further, the resistors need to be trimmed to adjust for process variations on chip.

4. Power Efficiency

Power efficiency is traded-off with distortion performance in line driver designs. Large output voltage swing and high linearity require higher supply voltages, thereby increasing power consumption and reducing efficiency. Usually class AB output stages provide best results in terms of efficiency and swing. However several other solutions have been attempted to address the efficiency problem, including the system on peak approach [3]. Power dissipation is of greater concern at the central office end, since it handles multi-channels on the same card. Power regulation, battery back up and cooling add up to system costs.

5. Frequency Response

DSL systems utilize the telephone network for full-duplex data transmission. The upstream and downstream bandwidth range from 100 kHz to 10 MHz. The bandwidth is divided into multiple channels, with each channel modulated by QAM or QPSK. The attenuation of a signal is also proportional to the frequency as shown in Fig. 4. Hence data transmission is limited to lower frequencies.

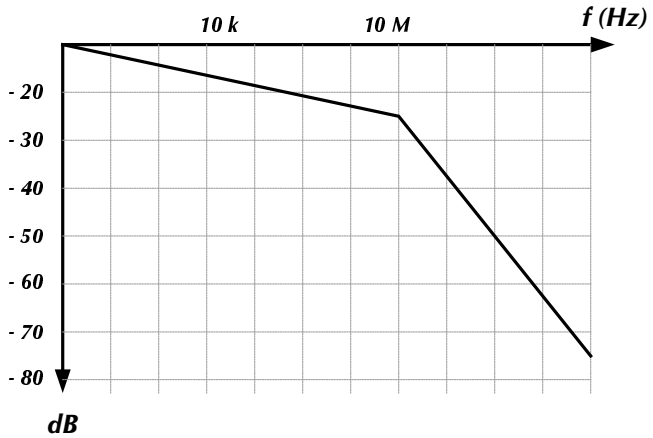


Fig. 4. Line attenuation vs. frequency.

6. Echo Cancellation

The signal at the driver end needs to be sufficiently powerful so that it can be differentiated at the receiver from noise. However this can interfere strongly with its own incoming signal. This requires an attenuation of transmit data before the incoming signal can be boosted by the VGA, as to not overload the ADC following it. The analog echo cancellation is implemented using the hybrid, which mimics the characteristics of the transmission channel.

B. PREVIOUS WORK

Several line driver architectures for different applications (Serial Bus, Video, xDSL and ISDN) are extensively available in open literature, with emphasis on linearity, output swing, power efficiency, bandwidth and matching**.** An ISDN line driver [4] has been designed with 80 dB linearity and 5 V_{P-P} differential swing by careful control of the quiescent current in the output stages. This current is a trade-off between crossover distortion and power consumption. An HDSL line driver with three stages (dual-differential preamp stage, class AB midamp stage and output stage), resistive feedback and nested miller compensation [5] achieved better than 70 dB linearity and 2.4 V_{P-P} swing with 30 Ω load resistance across the signal bandwidth upto 100 kHz. A wide-band line driver [6] has been designed using a pseudo differential architecture and a transconductor with active termination. This design can provide automatically tuned termination accounting for process and load variations. It achieved 2 V_{P-P} swing with better than 47 dB linearity at 75 Ω load. The power efficiency is however poor. In [7] a line driver with accurate current control to reduce crossover distortion is proposed. A tuning circuit compares the quiescent currents in the output stages with a reference and adjusts the gate voltages appropriately. Also [8] describes a video line driver with synthesized output impedance for matching to line variations. Table I summarizes the important design results of the various line driver architectures discussed.

In [6], [7] and [8], tuning schemes are utilized for gain, impedance or quiescent current adjustment to achieve improved performance. The concept of

impedance matching however is not addressed in most cases other than [6], [8] and [9]. Again Ref [6] and [9] utilize class A topology which results in poor efficiency. The aim of this thesis is to design an improved line driver with class AB topology that provides consistent performance in gain and linearity across line variations. This thesis describes a CMOS line driver capable of delivering 1.2 V_{P-P} signal up to 5 MHz with a linearity of better than 45 dB across load variations from 70 to 180 ohms. The emphasis of the design is on impedance matching, thereby maximizing power efficiency. Using an on-chip, offline-tuning scheme with continuous calibration, the output impedance of the line driver is matched with the line impedance. This minimizes return loss thereby providing uniform line driver performance across a range of line impedance variation.

TABLE I

COMPARISON OF LINE DRIVER ARCHITECTURES IN LITERATURE

Application	Output Swing	Linearity	Band-width	Power Efficiency	Output load	Tunability
ISDN [3]	5 V_{pp}	82 dB @ 40 kHz	10 MHz	Class AB push-pull	40-60 Ω	-
HDSL [4]	2.4 V_{pp} (3 V supply)	70dB @ 200 kHz	30 MHz	Push-pull fully differential	30 Ω	-
ADSL [5]	2 V_{pp} (3.3 V supply)	47.5dB @ 10 MHz	160 MHz	Class A Pseudo differential	75 Ω	Adaptive gain and impedance tuning
ISDN [6]	2.5 V_{pp} (3.3 V supply)	68dB @ 10 kHz	60 kHz	Class A/B push-pull	67 Ω	Quiescent current control
Video [8]	1.2 V_{pp} (2.4 V supply)	50dB @ 10 MHz	130 MHz	Class A operation	75 Ω	38-85 Ω impedance matching

The thesis is organized into six chapters including the introduction. Chapter II discusses the need for impedance matching. Further, several output stages that can be used to implement active termination are investigated and the proposed topology is introduced. There from, the design methodology and the mathematical rigor behind the design are investigated.

Chapter III provides detailed description on the specifications, design tradeoffs and design procedure for the line driver. Chapter IV introduces the need for tuning and the mechanism thereby implemented in the design. The circuit blocks forming the tuning scheme are investigated with the circuit schematic and simulation results. The overall transient response and tuning loop characteristics are also provided.

Chapter V deals with the implementation issues in layout and chip packaging. The prototype chip results from the PCB are presented and summarized. Chapter VI summarizes the thesis with the conclusions drawn and relevant improvements to the circuit for future revisions.

CHAPTER II

LINE TERMINATIONS AND OUTPUT STAGES

Several key design parameters for line drivers such as voltage swing, linearity, power efficiency and impedance matching have been discussed in the previous chapter. However the requirement of impedance matching at the driver and receiver end is usually not addressed. The advantage of proper termination lies in its ability to attenuate signal reflections as explained in the following sections. However this technique also results in reduced signal swing thereby affecting the maximum reach. So this loss in voltage should be compensated while designing the line driver. Consequently higher supply voltages and power consumption are required.

Alternatively, using active termination techniques, proper termination can be achieved without affecting output swing. This technique eliminates the series resistor required for termination by directly matching the output resistance of the driver to the line. In this chapter, several termination techniques and their advantages and disadvantages are mentioned. Active termination is shown as the ideal way to terminate signals at the driver end. Later, output stages are explored wherein the output resistance can be controlled and finally the class AB amplifier with controlled impedance is discussed.

A. LINE TERMINATIONS

1. Unterminated

Fig. 5 shows the macromodel of a line driver, modeled as a voltage controlled voltage source with output resistance r_o and gain A_v. The cable is treated as a resistor with its characteristic impedance R_L. According to the principles of transmission theory, when a signal is transmitted from point A to B, the outbound signals are reflected back to the source when a mismatch in the impedance at the far end is encountered [10]. In the case of an unterminated line, the signal encounters another mismatch at the driver end,

generating further reflections towards the receiver. Finally a steady state is achieved, as seen in Fig. 6, for an unterminated driver and receiver.

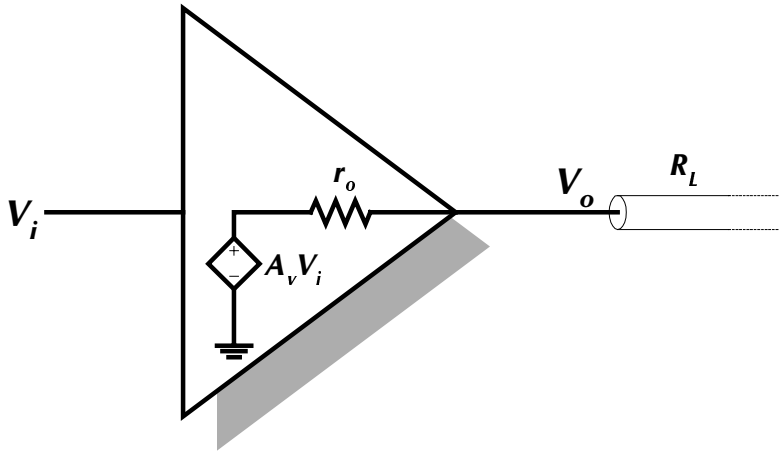


Fig. 5. Line Driver with interface to the cable.

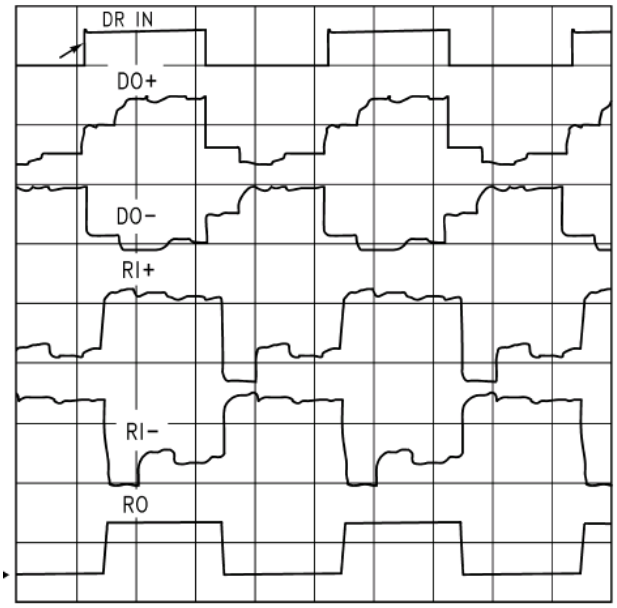


Fig. 6. Reflections superimposed on signals for unterminated line. [10]

The reflections can be seen superimposed on the driver and receiver end signals. Unterminated lines are an option only for short-length, low-data rate systems. However, the demand is for high speed and fast access to information over relatively long distances. This precludes that some form of termination is required.

2. Series termination

Series or backmatch termination, as shown in Fig. 7, involves adding a series resistor (R_s) between the output of the line driver and the input to the cable. The value of this termination resistor is such that the sum of the output resistance (r_o) and series resistance (R_s) equals the line resistance (R_L). In such a case, signal reflections back to the driver are properly terminated. When the receiver end is also matched, all signal reflections are cancelled out as seen in Fig. 8.

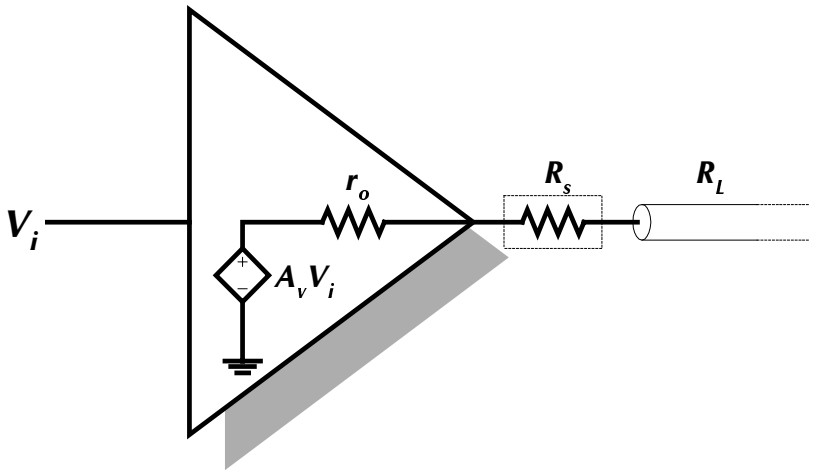


Fig. 7. Line driver with series termination.

However there are three main disadvantages with this scheme of series termination

- Process variations cause the output resistance of the line driver to vary. This requires a rework in choosing the series resistance (R_s) accordingly. It is very difficult to attempt to match the impedances for all the process corners.

- The line resistance (R_L) in itself is subject to variations depending on length, cable diameter and other impairments. This makes the selection of R_s only suitable for a particular R_L. In the case of variations in R_L, signal reflections would still occur.

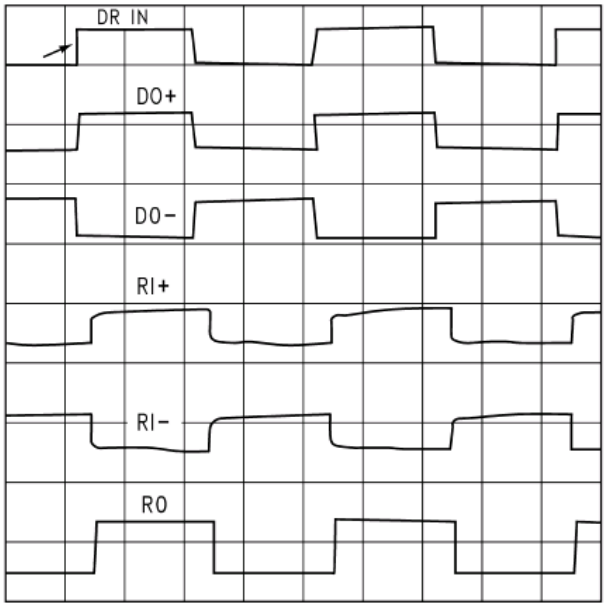


Fig. 8. Signal Reflections attenuated at receiver and driver. [10]

3. Active termination

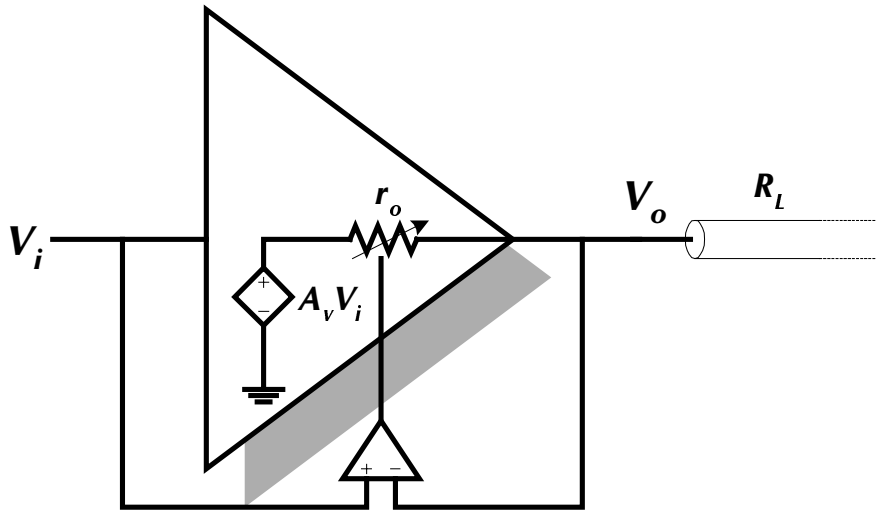


Fig. 9. Active termination of driver using feedback.

Active termination or synthesized impedance is a technique that uses feedback to match the output resistance of the driver to the line, as shown in Fig. 9. This eliminates the requirement for the series termination resistor, thereby easing the requirements for the driver voltage swing. Further the supply voltages can be reduced saving power.

The line impedance (R_L) affects the signal level at the output (V_o). The input and output voltages (V_i and V_o) are compared with the amplifier and the difference is used to control the output resistance. This scheme solves the problem of termination without the use of series resistor for matching. Further process variations on chip or external line variations can be compensated for by the feedback loop, thereby providing a proper termination across a wide range of impedance. Thus, active termination technique provides best results in terms of proper termination, output voltage swing, reduced voltage supply and hence lower power consumption. Table II shows a comparison of the techniques with their merits and demerits.

TABLE II

SUMMARY OF LINE TERMINATION TECHNIQUES

Termination	Data Rate	Reach	Tunability
Unterminated	Low	Short	-
Series Terminated	High	Medium	Line matching for one particular value of R_L
Active Terminated	High	Long	Matching across line variations (R_L) and process variations (r_o)

In order to implement the active termination scheme, an output stage with controlled impedance is required such that when the output voltage is forced equal to the input, the output resistance is matched to the line. Such a scheme would provide uniform performance (gain and linearity) and proper matching for various line resistance values.

B. OUTPUT STAGES

Output stages serve the purpose of interfacing the gain stages of a multi-stage amplifier to the external load. Their main purpose is to deliver maximum signal power to the load with minimum distortion. Furthermore, they require small output resistance compared to the load in order not reduce the gain from the previous stages. Finally they need to have good efficiency in terms of low power consumption. The requirements for the output stage are thus the same as the line driver. The design of the output stage forms the key element in line driver design. Although bipolar and BiCMOS stages provide good current control capabilities, the circuits discussed in this thesis are limited to CMOS only. This is due to economic reasons and greater availability of CMOS for fabrication.

For linear output stages, design choices are limited to class A,B or AB topologies. Class A stages provide high swing and linearity but require DC bias current flowing through the output devices even in the absence of AC input. Hence their power efficiency

is poor. Class B stages on the other hand have zero current flowing in the absence of an input due to the use of two active devices in a push-pull manner. However crossover distortion occurs while switching from one device to another, thereby affecting linearity. A compromise is sought in class AB stages by achieving a balance between linearity and power efficiency. Several topologies are explored which serve as output stages wherein the output impedance can be controlled though circuit parameters, thereby providing active termination.

1. Common Drain Class AB Stage

The classical common drain class AB output stage is shown in Fig. 10. By matching the dimensions of transistors M_1-M_4 and M_2-M_5, accurate current control in the output stages, a crucial requirement for offset cancellation, can be achieved.

The following conditions (2.1) and (2.2), however, limit the output swing.

$$v_{o,\max} = V_{DD} - V_{gs1} - V_{ds3} \qquad (2.1)$$

$$v_{o,\min} = -V_{SS} + V_{ds6} + V_{gs2} \qquad (2.2)$$

Furthermore, the threshold voltage of M_1 has a bulk dependency as v_o increases. This further limits the upward swing and causes asymmetric distortion to the signal. Large transistor sizes are required to improve the voltage swing, but the parasitics associated with the output devices dominate the distortion performance. The output resistance of the push-pull stage is given in (2.3).

$$r_o = \frac{1}{g_{m1} + g_{m2} + g_{d1} + g_{d2}} \approx \frac{1}{g_{m1} + g_{m2}} \qquad (2.3)$$

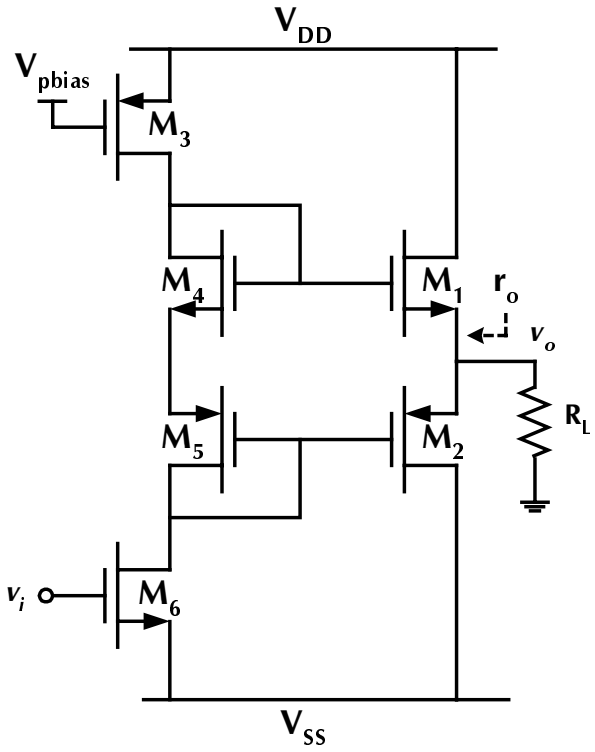


Fig. 10. Class AB push-pull output stage.

To achieve low output resistance of around 50 Ω, the g_m requirements are about 10 mA/V each. This requires large bias current and transistor sizes to achieve such low resistance. The means to control the output resistance is by the DC bias current flowing through M_1 and M_2, which is too cumbersome. Thus the topology is unsuited for the high swing, high linearity and controlled output impedance requirements of the line driver.

2. Pseudo Source Follower

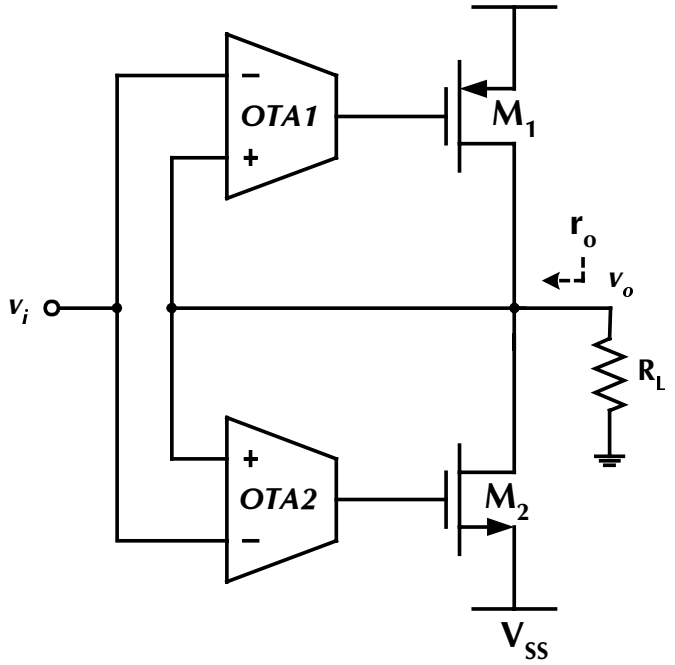


Fig. 11. Pseudo source follower.

The pseudo source follower output stage, shown in Fig. 11 consisting of the error amplifiers and common source output devices is identical to a source follower with high output conductance. This scheme has the advantages of better swing and higher linearity compared to the class AB push-pull stage since the bulk effects of M_1 and M_2 are eliminated. The negative feedback due to the error amplifiers serves to reduce the output resistance as given by the (2.4).

$$r_o = \frac{1}{A(g_{m1} + g_{m2})} || \, r_{o1} \, || \, r_{o2} \approx \frac{1}{A(g_{m1} + g_{m2})} \qquad (2.4)$$

With a gain of 100 (40 dB) and transconductance of 200 μA/V each, the output resistance achieved is 50 ohm. However control of the output resistance is still difficult due to the signal dependencies of g_{m1} and g_{m2}. Another problem is the lack of quiescent current control in the output devices. This can affect the offset and crossover distortion performance of the output stage. One way to mitigate this effect is to reduce the gain of the amplifiers. The reduction in amplifier gain causes smaller variations in the gate-to-source voltages (V_{gs1} and V_{gs2}) that control the quiescent current. However too small a gain results in error between the input and output signals.

3. Class A Controlled Impedance Output Stage

In the topology shown in Fig. 12, the input signal (v_i) is copied to the node (v_x) by OTA1 in negative feedback. The resulting current (v_x / nR_{nom}) flows through M_1 and is mirrored to M_2 (1:n mirroring ratio). Finally a current to voltage conversion is achieved at the load R_L, signifying the resistance of the line.

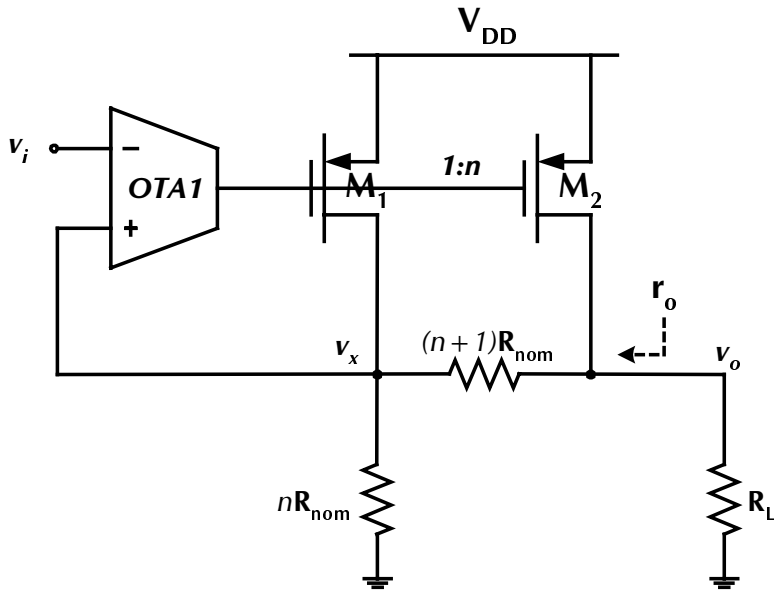


Fig. 12. Class A controlled impedance stage.

When the transistors M_1-M_2 are properly matched and the input offset is eliminated, the DC node voltages and v_i and v_x are the same and no DC current flowing across the bridge resistance. This resistor sees only the signal reflections on the line and provides proper termination through the choice of n and R_{nom}. Equations (2.5) and (2.6) provide the gain and output resistance expressions for the output stage.

$$\frac{v_o}{v_i} = \frac{R_L}{R_{nom}} \qquad (2.5)$$

$$r_o = R_{nom} \qquad (2.6)$$

$$n = \frac{W_2}{L_2} . \frac{L_1}{W_1} \qquad (2.7)$$

By choosing R_{nom} to be equal to R_L, the gain of the output stage is exactly one, and the output resistance is R_L, the same as the output load. Thus ideal buffer stage is realized with proper termination. The output can swing from ground to V_{DD}- V_{dsat2}. The cause of distortion is the output resistance of the current mirrors and output offset. By using high compliance or cascode current mirrors and careful layout techniques these problems can be addressed.

This circuit is however not completely tunable. Once the choice of R_{nom} (equal to R_L) has been made, the design cannot be altered. Process variations tend to change the output resistance and the line resistance varies depending on external conditions. This results in incomplete or imperfect matching.

4. Class A Output stage with Variable Impedance

A natural extension of the buffer in Fig. 12 is the topology in Fig. 13 with a variable current mirror (M_1-M_2, R_{s1}, R_{s2}) configuration. The mirroring ratio (m) adds a

degree of freedom in the design, compensating for process and line variations. (2.8) and (2.9) give the gain and output resistance of the topology in Fig. 12.

$$\frac{v_o}{v_i} = \frac{m}{n}\frac{R_L}{R_{nom}} \qquad (2.8)$$

$$r_o = \frac{n+1}{m+1}R_{nom} \qquad (2.9)$$

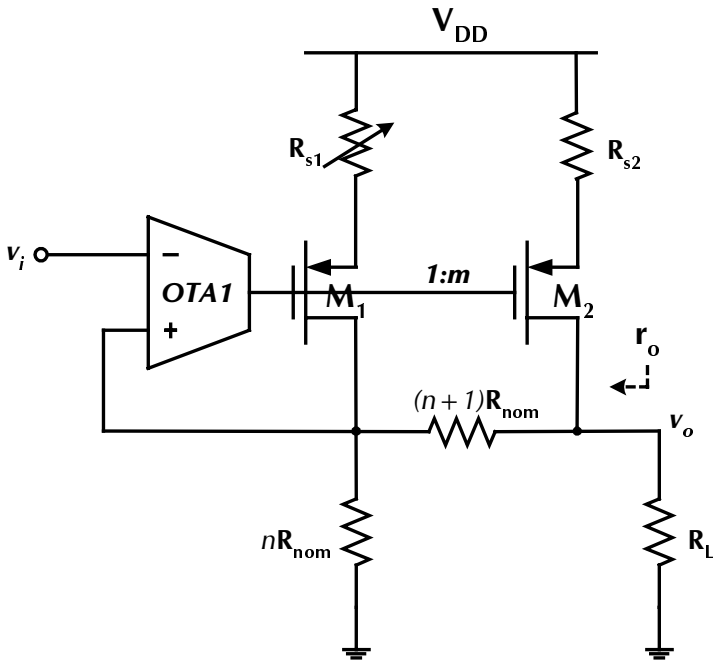


Fig. 13. Controlled output impedance stage with variable current mirror.

The linearity and output swing are reduced due to the addition of resistor R_{s2} but the performance improvement is achieved over a wide range of resistance values. A tuning scheme compares the input and output voltage and controls the variable resistor R_{s1} through negative feedback. When the output is forced to be the same as the input, the condition in (2.12) results, and the output resistance is equal to R_L, as in (2.13).

$$m = n\frac{(V_{gs2} - V_{Tp})^2}{(V_{gs1} - V_{Tp})^2} \qquad (2.10)$$

$$\frac{v_o}{v_i} = \frac{m}{n}\frac{R_L}{R_{nom}} = 1 \qquad (2.11)$$

$$\Rightarrow R_{nom} = \frac{m}{n}R_L \qquad (2.12)$$

$$r_o = \frac{n+1}{m+1}R_{nom} = \frac{n+1}{m+1}\frac{m}{n}R_L = R_L \qquad (2.13)$$

The gain is forced to one through the tuning loop, and due to the topology, the output resistance is equal to R_L, thus matching it to the line. The condition for tuning loop convergence is given in (2.14).

$$m.R_L = n.R_{nom} \qquad (2.14)$$

When line variation cause R_L to change and process variations on chip affect R_{nom}, the mirroring ratio (m) can be changed through the tuning loop to maintain the condition in (13). This results in a gain of one and an output resistance matched to the line across line resistance variations. The dynamic performance of the output stage is thus improved. However power efficiency remains poor due to class A nature of design.

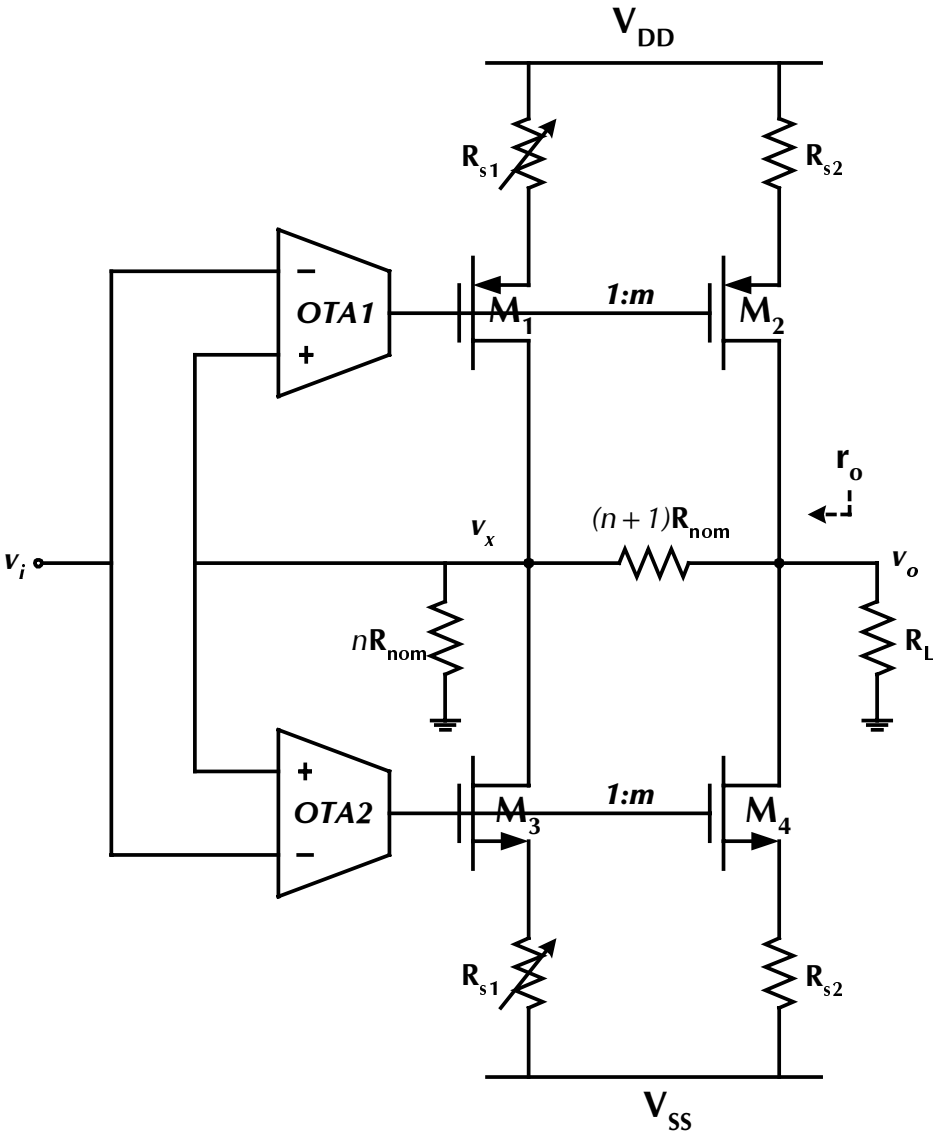


Fig. 14. Class AB push-pull stage with controlled output impedance.

5. Class AB Output Stage with Variable Impedance

The topology in Fig. 14 is the proposed line driver to be discussed in detail in this thesis. This line driver architecture is ideal in terms of output swing, linearity and impedance matching. The output resistance is a ratio of resistor values, transistor dimensions and mirroring ratios, each of which can be controlled through layout and circuit techniques. The power efficiency of the output stage in Fig. 13 is very low. In order to maximize the swing, the output node (v_o) is biased at $V_{DD}/2$. In a 3 V design, with a 75 Ω line impedance, the DC biasing current is about 20 mA. An improvement to the efficiency can thus be achieved through a class AB topology shown in Fig. 14.

By using complimentary nMOS and pMOS half circuits in a push-pull manner, the DC current drawn by the output stage can be reduced by 60 % with similar results in output swing as compared to the class A stage. These savings in terms of bias current results in better efficiency. The equations (2.5)-(2.14) continue to be valid for this structure. The input voltage (v_i) is made available at the node (v_x) through the high gain of OTA1 and OTA2. The resulting current (v_x / nR_{nom}) splits into the two half-circuits, each mirrored through M_1-M_2 and M_3-M_4 and summed at the output (v_o). Each half-circuit provides the drive current during one-half cycle with a small overlap period between the two. Table III summarizes the output stages investigated for the design of the line driver.

TABLE III

COMPARISON OF OUTPUT STAGES

Output Stage	Output Swing	Linearity	Output Resistance(r_o)	Tunability (impedance matching)
Common drain Class AB	Low	Low	$1/g_{m1}+g_{m2}$	• Difficult to achieve low r_o • Difficult to tune g_{m1} and g_{m2}
Pseudo Source follower	High	High	$1/A(g_{m1}+g_{m2})$	• Difficult to tune g_{m1} and g_{m2}
Class A Controlled Impedance	High	High	R_{nom}	• R_{nom} made equal to R_L by design • R_{nom} cannot be adjusted after design
Class A Variable Controlled Impedance	Medium	High	$R_{nom}.(n+1)/(m+1)$	• R_{nom} made equal to R_L by design • r_o adjusted by controlling m
Class AB Variable Controlled Impedance	Medium	Medium	$R_{nom}.(n+1)/(m+1)$	• r_o adjusted by controlling m

The class AB structure (Fig. 14) with a controlled impedance which can be adjusted through the mirroring ratio (m) provides an ideal output stage in terms of balancing all the requirements of a line driver. A trade-off is achieved in terms of lower voltage swing and linearity but proper termination and uniform performance (gain and linearity) across various line resistance variations. The structure is further investigated in the following chapters for use as a line driver for video applications.

CHAPTER III

LINE DRIVER DESIGN

A. DESIGN OF OUTPUT STAGE

The class AB structure with controlled impedance shown in Fig. 14 is the topology for the adaptive video line driver. This structure provides optimum performance in terms of signal swing, linearity and output impedance matching. Equations (2.8) and (2.9) relate the gain and output resistance of the output stage to the circuit parameters (R_{nom}, R_L, n and m). Gain and consequently output resistance is controlled through the variable mirroring ratio (m).

The nominal line resistance (R_L) is usually 75 Ω for video line drivers. By design, R_{nom} is chosen the same value as R_L. Further by choosing the value of n (device ratios of M_1-M_2 and M_3-M_4), the only parameter that can be used to adjust gain and output resistance is m (the mirroring ratio of M_1-M_2 and M_3-M_4). The choice of n is a tradeoff between output swing and linearity on one hand and power consumption on the other. The design values for deciding the value of n is shown in Table IV.

TABLE IV

SIMULATION VALUES FOR LINE DRIVER OUTPUT STAGE

M_1	144 μm/0.6 μm
M_3	48 μm/0.6 μm
R_{s2}	15 Ω
R_{nom}	75 Ω
R_L	75 Ω
R_{s1}:R_{s2}	n:1

Fig. 15 shows the linearity and output swing of the line driver for different values of n ranging from 5 to 20. The OTAs (OTA1/OTA2) are modeled as ideal voltage controlled voltage sources with large gain, infinite bandwidth, infinite input and zero output resistance. The current in the input stage (M_1-M_3) is fixed and by changing n, the output stage current is varied. For small values of n, the transistors are in saturation but weak inversion. The linear range of swing is not sufficient and hence the linearity is poor. As the ratio n increases, the transistors enter into strong inversion and the linearity improves. Also the output swing increases due to the lower V_{DSAT} caused by larger currents, thereby providing more headroom for swing. For values of n above 15, the higher distortion observed is attributed to the mismatch (due to mobility and threshold voltage) in the P-type and N-type half-circuits. Thus, the quiescent current control is an important design constraint to improving the linearity of the output stage.

The ideal choice for n is around 10-13, with a maximum output swing of 2.2 V, linearity of 50 dB and power consumption of 25 mW. For a variation of 25 Ω around the nominal line resistance (75 Ω), the mirroring ratio varies from 9 to 18, in order to maintain unity gain of the line driver, as seen from equation (1). The design results for the driver are summarized in Table V.

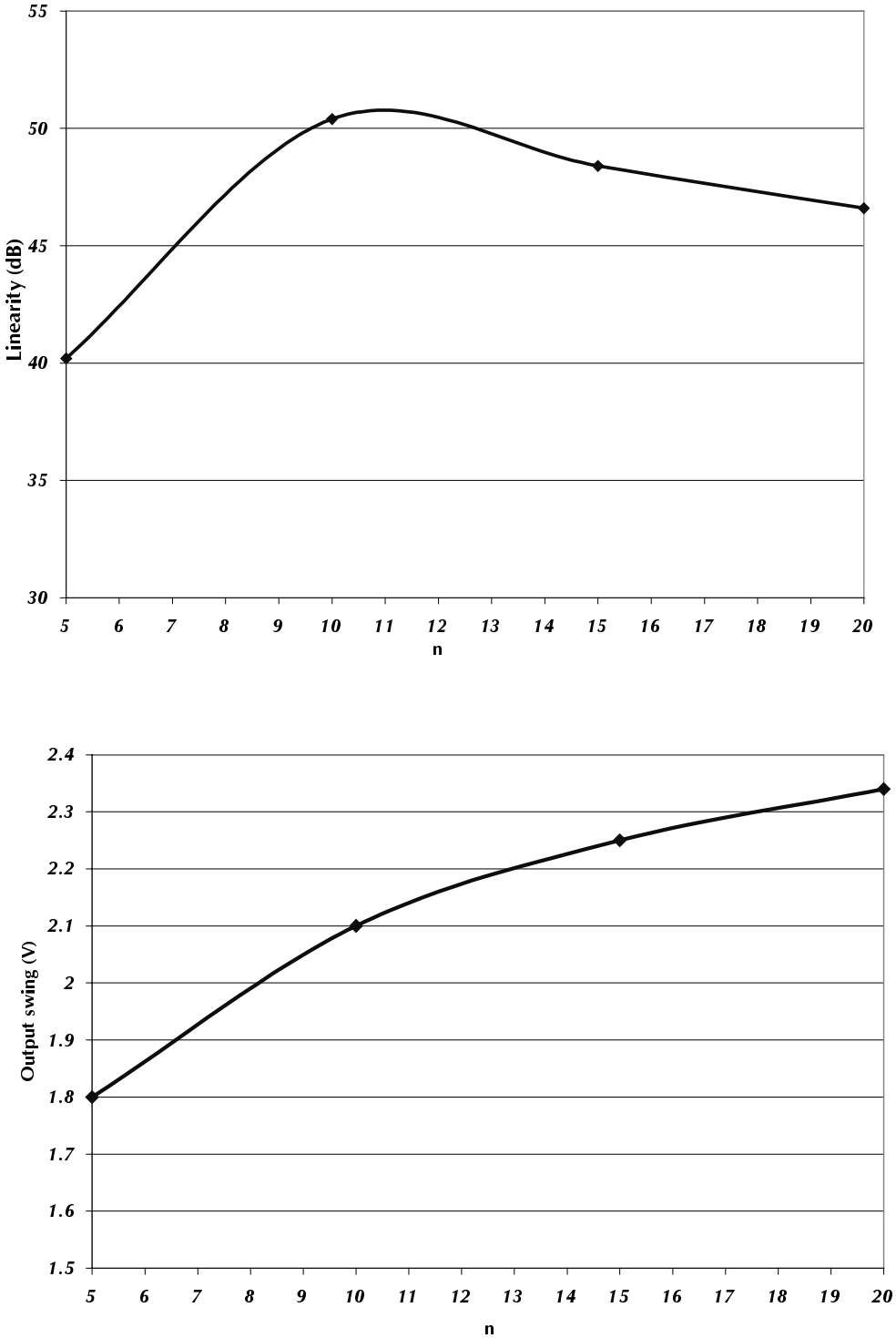


Fig. 15. Linearity and output swing versus mirroring ratio (n).

TABLE V

RESULTS OF LINE DRIVER OUTPUT STAGE DESIGN

n	12
R_{nom}	75 Ω
Variation in R_L	50-100 Ω
Variation in m	9-18
Linearity (0.8 V, 100 kHz)	50 dB
Maximum output swing	2.2 V
Power Consumption	25.6 mW

B. DESIGN OF TRANSCONDUCTOR

The output stage in the previous section has been designed using ideal transconductors having infinite gain, infinite input resistance and zero output resistance. By adding the transconductors (OTA1 and OTA2 in Fig. 14), non-linear behavior in the output stage is introduced, which is investigated in terms of distortion performance (total harmonic distortion). Each OTA is modeled as in Fig. 16, by a voltage controlled current source (G_m), output resistance (R_{out}) and output capacitance (C_p). The gain and the gain-bandwidth product (GBW) of the OTA are given in (3.1) and (3.2), respectively.

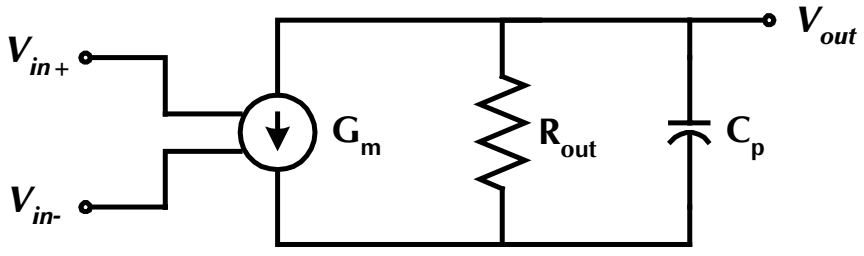


Fig. 16. OTA macromodel.

$$\frac{v_{out}}{v_{i+} - v_{i-}} = G_m R_{out} \qquad (3.1)$$

$$GBW = \frac{G_m}{C_p} \qquad (3.2)$$

OTA specifications such as gain, gain bandwidth, output resistance, offset and common mode range are estimated by measuring the effect of various parameters (G_m, R_{out}, C_p, offset) on the linearity. Varying OTA parameters (G_m, C_p, R_{out}) affects the OTA specifications (Gain, GBW) as shown in Table VI. The effect of varying each parameter on the linearity is shown in Fig. 17.

TABLE VI

OTA PARAMETERS AND SPECIFICATIONS

	Gain	GBW	Output resistance	Offset
C_P =0.2 to 1.2 pF G_m =1.5 mA/V	44 dB	200 MHz – 1.3 GHz	100 kΩ	0
G_m =1.5 mA/V, Cp =0.5 pF	20 – 60 dB	500 MHz	10 k – 500 kΩ	0
G_m =0.5 to 1.5 mA/V	34 – 60 dB	160 MHz – 500 MHz	100 kΩ	0
Offset –100 to +100 mV	60 dB	500 MHz	100 kΩ	-100 mV to 100 mV

As the transconductance (G_m) increases, the bandwidth of the OTA increases, which improves the linearity (THD). This is because the gain control around the feedback loop is sustained for higher frequencies. It should also be noted that when the bandwidth is increased more than the requirement, the total integrated noise of the system also increases. This affects the signal-to-noise performance of the circuit.

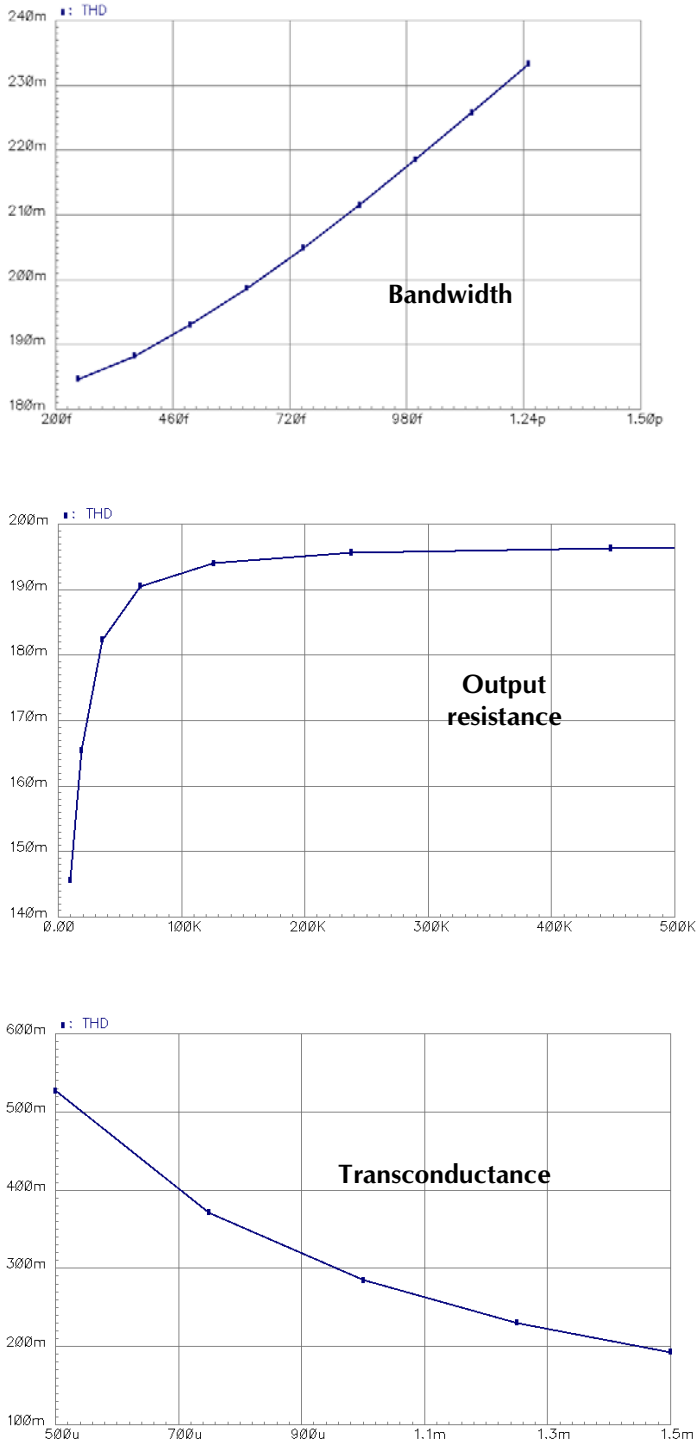


Fig. 17. Variation of THD versus bandwidth, output resistance (Rout), transconductance and offset.

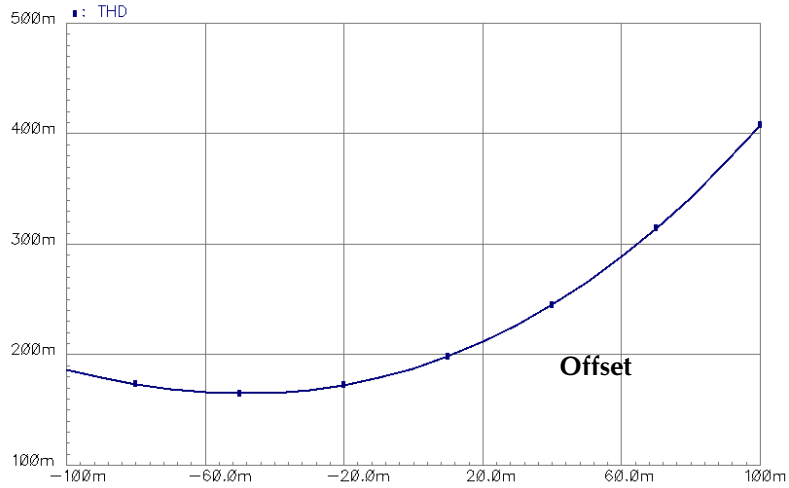


Fig. 17. continued

The next issue to discuss is the gain of the OTA. Gain is essential for linearity but it cannot be increased freely because as the gain increases, the output transistors are forced to conduct more current with fixed aspect ratio. At first glance, larger drain current seems to result in more linearity, but this is true for class A operation. Larger current implies larger overdrive voltage and it is known that THD is inversely proportional to over drive voltage. For class A/B operation the quiescent current should be very well adjusted so as to minimize cross over distortion [11], [12]. Thus, gain of the OTAs is varied and the effect of gain variation on THD is investigated. The result is given in THD versus gain plot in Fig. 17(c). It is seen that the gain should be around 35 dB for the designed W/L ratios.

Another disadvantage of having high gain is higher sensitivity to input referred offset. The variation of THD with input referred offset is also provided in Fig. 17(d). Identical offsets are applied to each OTA input. In fact different offset values can result in higher distortion. Based upon the above discussion, the OTA specifications are summarized in Table VII.

TABLE VII

ESTIMATED OTA PARAMETERS

Parameter	Value	Unit
DC Gain	35-40	dB
Gain bandwidth	150-200	MHz
Transconductance	1.2	mA/V
Input Referred Offset	< 20	mV
Slew rate	≈ 30	V/μs
Input referred Noise (10Hz-5MHz)	< 40	μV
Output Swing	+/- 1	V
THD (closed loop 1.2 Vpp @ 10MHz)	< 0.1	%

As far as the noise budget is concerned, the total estimate is 67 μV to provide an SNR of 70-80 dB. From this, the noise contribution of the output stage is deducted. This is the available budget for the OTA and tuning loop. OTA1 and OTA2 are realized as simple differential pairs as shown in Fig. 18.

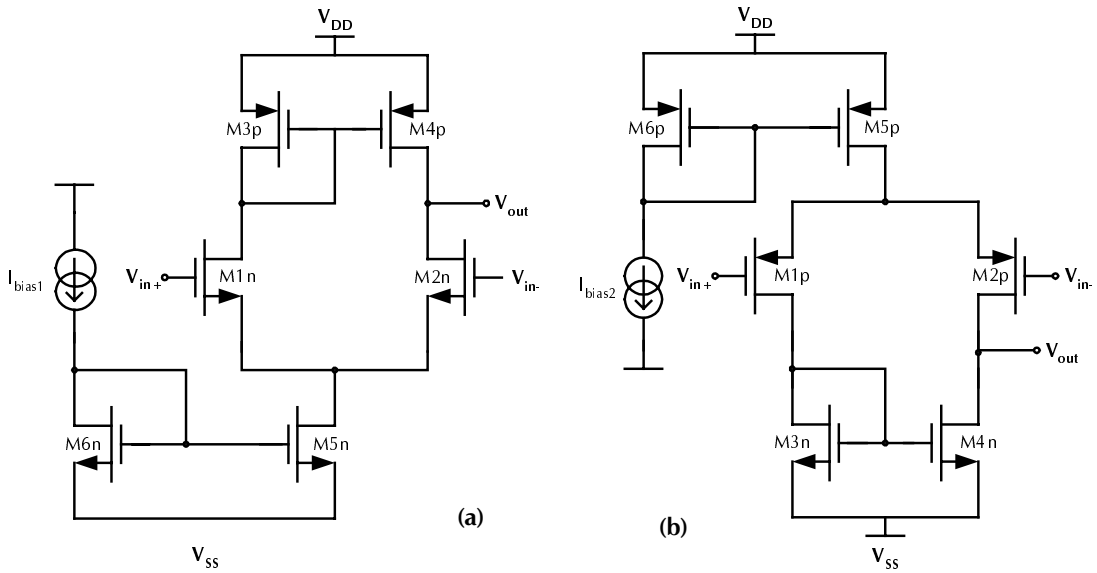


Fig. 18. (a) N-type (OTA1) and (b) P-type (OTA2) differential amplifiers.

The positive-half (OTA1) and negative-half (OTA2) error amplifiers are basic differential amplifiers with P-type and N-type drivers, respectively. Using such complementary structure is crucial in handling large signal swings for both the negative and positive cycle. The differential amplifier with NMOS drivers can handle input common mode signals as high as (V_{DD}- $V_{GS,M3p}$+ $V_{T,M1n}$) which makes it a good positive half error amplifier. On the other hand the amplifier with PMOS drivers can handle input common mode signals as low as (V_{SS}- $V_{GS,M3n}$+ $V_{T,M1p}$), which makes it appropriate for a negative half error amplifier.

The DC gain of the error amplifiers is about 30-35 dB. Lower gain causes gain error in signal voltage when copied from V_i to V_1 and then to V_o. On the other hand, large gain causes higher variations in gate-to-source voltages and hence the DC operating point and offset [13]. The gain-bandwidth product of the transconductors is greater than 200 MHz which ensures negligible phase shift from input to output, in the frequency band of interest (100 kHz to 5 MHz). This condition ensures a robust tuning scheme through the comparison of the input and output envelopes, even with a simple peak detector. Salient results of the two OTAs are presented in Table VIII.

TABLE VIII

OTA SPECIFICATIONS AND RESULTS

Parameter	Specs	OTA1	OTA2	Unit
DC Gain	35-40	31.3	31.1	dB
Gain bandwidth (0.5 pF load)	150-200	270	245	MHz
Transconductance (G_m)	1.2	1.21	0.98	mA/V
Input Referred Offset	< 20	13	-16	mV
Slew rate 1.5 V, 1 MHz (2 pF load)	≈ 30	110	85	V/μs
Input referred Noise (10 Hz – 5 MHz)	< 40	13.3	15.3	μV
Output Swing	+/- 1	1.9	2.2	V
THD (closed loop) 1.2 V_{pp} @ 10 MHz)	< 0.1	0.15	0.25	%

Fig. 19 shows the frequency response of the OTA. The DC gain is 32 dB for both OTAs and the gain-bandwidth product is 250 MHz for a 0.5 pF load. By matching the device dimensions in both the cases, identical performance is achieved. Further by using complimentary transistors, the common mode signal and output swing capabilities for each half-circuit is better managed. The DC response of the line driver is shown in Fig. 20. The swing varies from –1.2 V to 1 V for ± 1.65 V power supplies. The swing is not symmetric due to the higher threshold voltages associated with the P-type devices and mobility effects. The same plot shows the derivative of the output voltage against the input. This is an indication of the linearity of the driver. The maximally flat portion of the curve from –0.7 to 0.6 V represents a gain of accurately one. With an input sinusoid of 1 V_{p-p} at 100 kHz, the distortion is lower than 0.04 %.

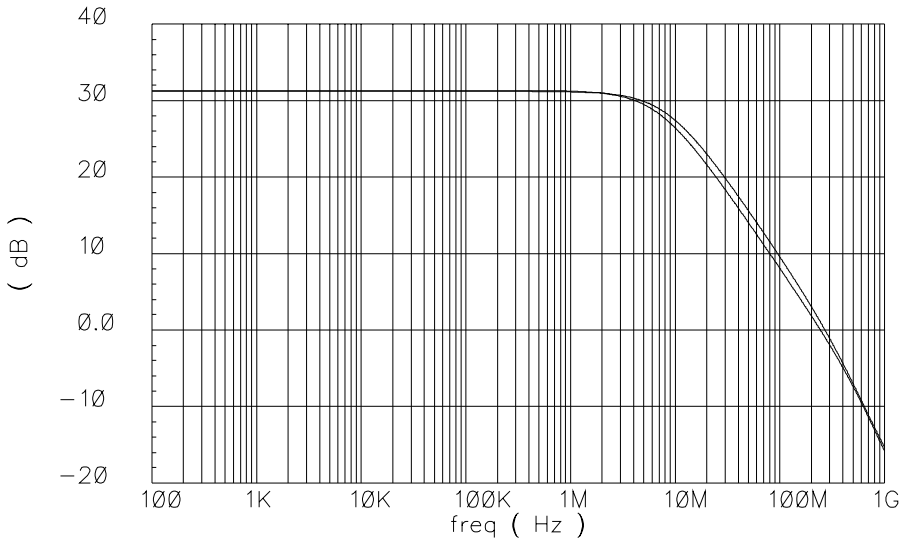


Fig. 19. Frequency response of transconductors (OTA1 and OTA2).

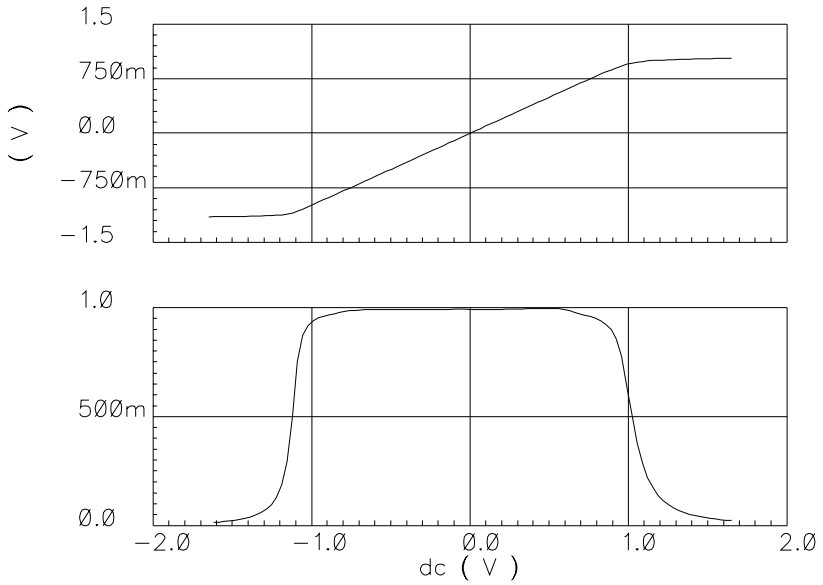


Fig. 20. Input-output characteristics of line driver.

C. DESIGN OF VARIABLE RESISTOR (R_{s1})

The design of the line driver stage and the error amplifiers (OTA1 and OTA2) has been done with the line resistance to be fixed at 75 Ω. In order to adjust the line driver for impedance variations, the resistor R_{s1} needs to be variable so that the mirroring ratio can be altered to satisfy the condition in (3.3).

$$m.R_L = n.R_{nom} \tag{3.3}$$

$$m = n\frac{(V_{g2} + I_{d2}R_{s2} - V_{DD} - V_{Tp})^2}{(V_{g1} + I_{d1}R_{s1} - V_{DD} - V_{Tp})^2} = n\frac{(V_{g4} - I_{d2}R_{s2} + V_{SS} - V_{Tn})^2}{(V_{g3} - I_{d1}R_{s1} + V_{SS} - V_{Tn})^2} \tag{3.4}$$

The mirroring factor (m) is a ratio of device dimensions and gate-to-source voltages as given in (3.4). The impedance matching range required is between 50 and 100 Ω, a 30 % variation around the nominal value of 75 Ω. This requires a range of resistance values for R_{s1} to adjust the output impedance accordingly. The output resistance plotted against resistance R_{s1} is shown in Fig. 21.

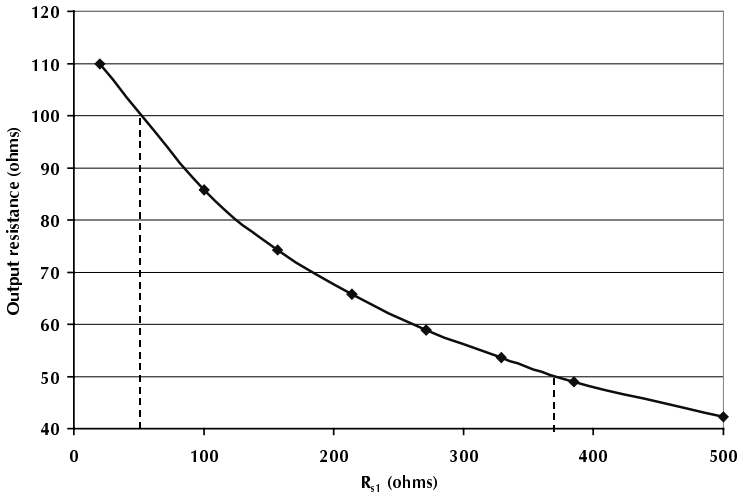


Fig. 21. Output resistance as a function of variable resistor (R_{s1}).

For the matching range of 50 to 100 Ω, the variation of R_{s1} required is between 50 and 360 Ω. Resistor R_{S1} is implemented as a poly-resistor (R_{s1a}) in parallel with an NMOS/PMOS device as shown in Fig. 22. Resistance R_{s2} is split into two equal parts (R_{s2a}, R_{s2b}), and along with the transistors M_{tp} and M_{tn} provide the necessary gate bias to transistors M_{Nres} and M_{Pres}. The current I_{tune} that controls the gate bias of M_{Nres}/M_{Pres} and hence its effective resistance (R_{s1}) is generated from V_{cntrl} as shown in Fig. 23. Control voltage V_{cntrl} is generated from a tuning loop that compares the input and output voltage and computes the error. The tuning scheme is discussed in detail in the next chapter.

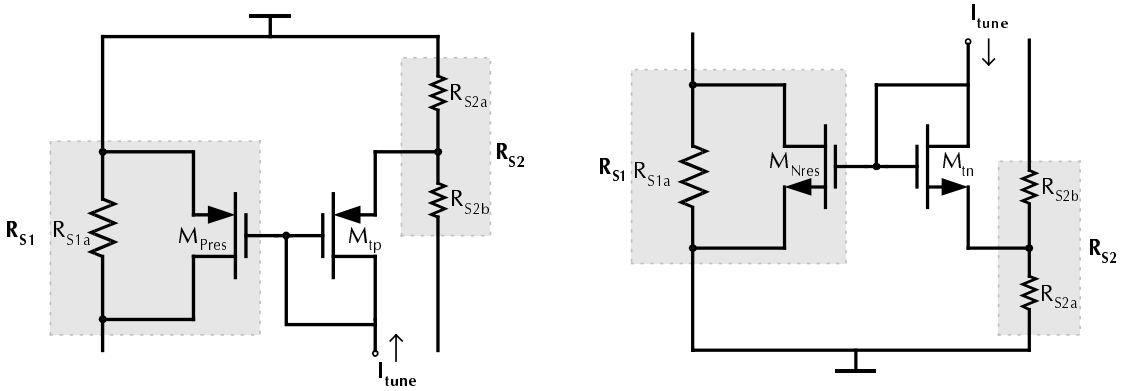


Fig. 22. Implementation of variable resistor (R_{s1}) with linearization.

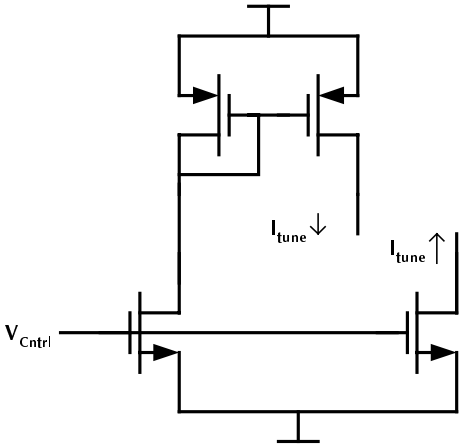


Fig. 23. Biasing for controlling gate voltage of variable resistor (R_{s1}).

$$I_d = K(V_{gs,Mnres} - V_{Tn})V_{ds} - \frac{{V_{ds}}^2}{2} \quad (3.5)$$

$$V_{gs,Mnres} = V_{gs,Mtn} + \frac{V_{ds}}{2} \quad (3.6)$$

$$\therefore I_d = K(V_{gs,Mtn} - V_{Tn})V_{ds} \quad (3.7)$$

The current through the transistor (M_{Nres}) in the linear region is given in (3.5). The voltage applied to M_{Nres} is the sum of the gate-to-source voltage of M_{tn} (controlled through I_{tune}) and one-half the drain-to-source voltage of M_{Nres} as in (3.6). This gives a current (I_d) that is linearly dependent on the drain (V_{ds}) as shown in (3.7). A similar analysis holds true for the transistors M_{Pres} and M_{tp}. By eliminating the second order effects, a linearized resistor with variable resistance is designed. The main design parameters for the variable resistor with the biasing scheme is given in Table IX.

TABLE IX

CIRCUIT PARAMETERS FOR LINEARIZED VARIABLE RESISTOR (R_{S1})

R_{s1a}	500 Ω
R_{s2a}, R_{s2b}	7.5 Ω
M_{Nres}	60 μm/1.2 μm
M_{Pres}	180 μm/1.2 μm
M_{Tn}	18 μm/1.8 μm
M_{Tp}	54 μm/1.8 μm

The combination of fixed poly-resistor (500 Ω) and NMOS variable resistor (60 u/1.2 u) can achieve the required range of resistance R_{s1} from 50 to 360 Ω, as specified for impedance matching from Fig. 21. An important design issue is the matching of

mirroring ratio (m) for the P and N-type half-circuits. The mirroring ratios need to be identical for symmetric swing and high linearity. Matched resistor ratios can be accurate to 0.1 %. However, integrated resistors using poly or diffusion layers have more than ± 10 % spread in their absolute values. The effect of resistance spread on the mirroring ratio are simulated for the three combinations (500/500, 450/450 and 550/550 Ω) and the results shown in Table X. The results are for a control voltage (V_{cntrl}) of –350 mV, mirroring ratio of 12 and line resistance of 75 Ω.

TABLE X

RESISTOR (R_{S1A}) MISMATCH AND MIRRORING RATIO (M) ERRORS

Resistor (R_{s1a})	P-type mirroring ratio	N-type mirroring ratio
450 Ω, 450 Ω	12.2	12
500 Ω, 500 Ω	12.4	12.2
550 Ω, 550 Ω	12.6	12.4
Nominal m		12
Line resistance		75 Ω

The mismatch between the P-type and N-type mirroring ratio is 0.2 in each case, with the worst-case mismatch of 5% occurring for the 550/550 Ω combination. This can however be tolerated in design since the gain is affected by less than 1 % in each case. The control voltage (V_{cntrl}) is converted to a tuning current (I_{tune}), as shown in Fig. 23. This provides the flexibility of controlling the gate voltage of M_{Nres} and M_{Pres} almost independently. The control voltage connected directly to the gates of M_{Nres} and M_{Pres} (Fig. 22) would limit the range of voltage that can be applied since the devices cannot be cutoff. This chapter thus concludes here with the design of the output stage, transconductors and the variable resistor. In chapter IV, the tuning scheme is discussed which completes the overall design. The feedback loop for tuning compares the input and output voltage through a peak detector and differential amplifier, and generates the control voltage (V_{cntrl}) thus closing the loop.

CHAPTER IV

AUTOMATIC TUNING CIRCUIT

Design parameters in integrated circuits including gain, bandwidth and quality factor (in filters) are set by absolute values of resistors, capacitors and transconductance. Process variations during fabrication cause wide spread in their nominal values, thereby affecting the design parameters. A commonly adopted solution is to design automatic electronic tuning along the functional circuit. A tuning circuit measures the circuit response, compares it with the external reference, calculates the error and applies the correction to the design. The external reference is a clock or a sinusoid of well defined frequency and amplitude. The reference and the circuit output are usually compared in terms of their peak, rms or rms-squared voltage. Alternatively the phase difference can also be compared and the error is estimated.

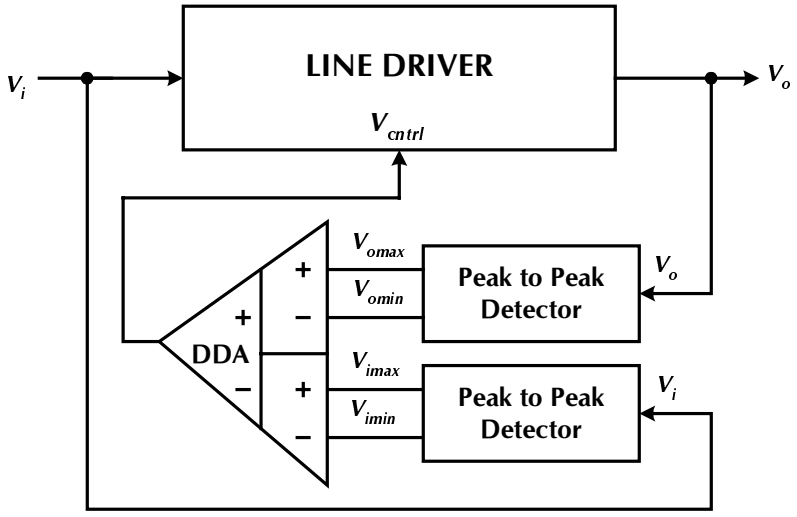


Fig. 24. Block diagram of line driver with tuning scheme.

A circuit is tunable if the observed error in design parameters can be corrected by varying component values electronically [14]. Typically variable resistors (MOS transistor in linear region), variable capacitors (reverse-biased p-n junction) and transconductors (g_m stage with variable bias current) are utilized for tuning purpose. The error computed in terms of voltage is used to control the component values.

In the line driver design, a tuning scheme has been adopted to provide unity gain across process and line variations. This also achieves proper line termination by matching the output resistance to the line resistance thereby eliminating signal reflections. The conceptual block diagram of the tuning loop is shown in Fig. 24, consisting of the line driver designed previously and the peak-to-peak detectors and differential difference amplifier (DDA). The reference signal is a sinusoid of fixed amplitude, and the line driver output and reference are compared in terms of their peak-to-peak amplitude. The error computed by the DDA in terms of voltage (V_{cntrl}) is applied to the variable resistors (R_{s1} in Fig. 14). The variable resistors control the gain and output resistance of the line driver through the mirroring ratio (m). The tuning circuit should be simple and robust, consuming a small portion of area and power. A scheme that is more complicated than the actual circuit serves no purpose. Since the reference is well controlled, proper design of a high gain, low bandwidth negative feedback loop forces the circuit to have the output to be equal to the reference.

A. DESIGN OF PEAK-TO-PEAK DETECTORS

The peak-to-peak detector consists of two circuits, one each for the positive and negative peak values, as shown in Fig. 25. The first stage consisting of M_{1n} and M_{2n} acts as a source follower, charging capacitor C_1 to the positive peak value of V_i. Once the peak value is reached, M_{2n} is turned off ($V_{gs} < 0$) and the voltage on C_1 is discharged at a slow rate. The discharge rate is controlled by the current through M_{1n}, which is determined by the device aspect ratio (W/L) and the biasing voltage V_n.

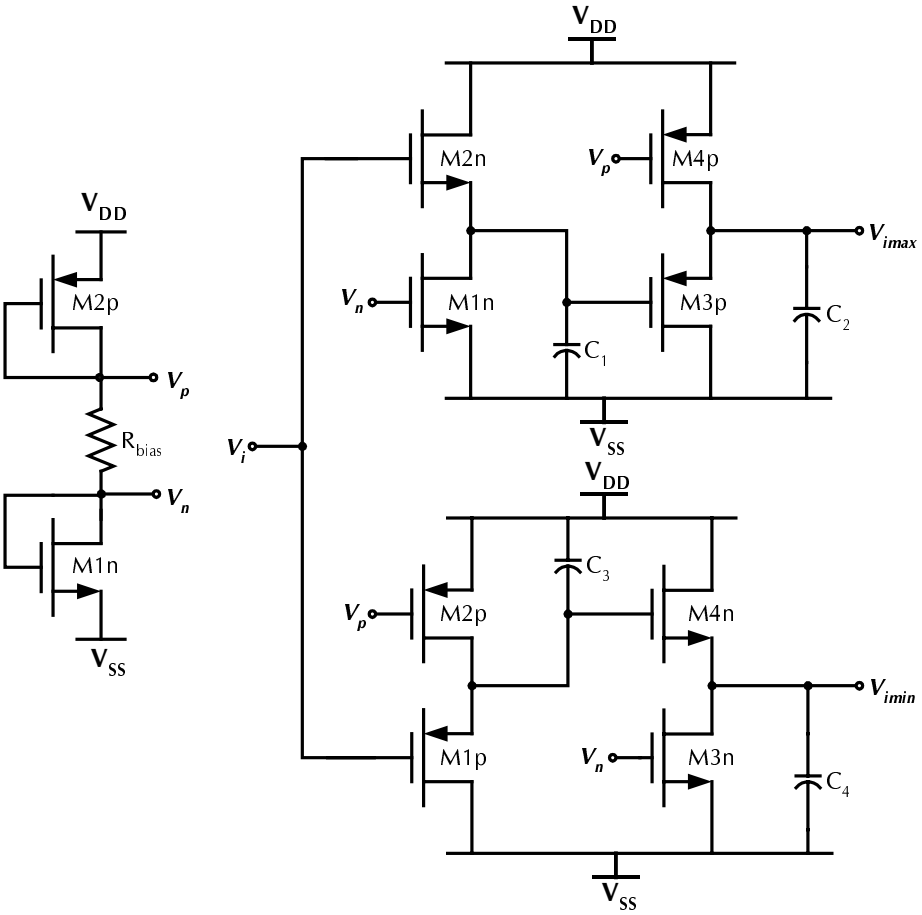


Fig. 25. Peak detector schematic with biasing circuit.

The second stage (M_{3p} and M_{4p}) acts as negative peak detector to the signal on C_1 and reduces the DC shift between V_i and V_{imax}. This stage helps further reduce the ripple, thus giving an almost constant peak voltage available at V_{imax}. The operation of the negative peak detector is similar, with C_3 charged to the negative peak through M_{1p} and M_{2p}. Transistors M_{3n} and M_{4n} along with C_4 reduces the ripples in the peak voltage. The negative peak value is available at V_{imin}. Table XI summarizes the aspect ratios for the peak detectors and the capacitor values.

TABLE XI

PEAK DETECTOR COMPONENT VALUES

M_{1n}, M_{3n}	12 μm/0.6 μm
M_{2n}, M_{4n}	6 μm/0.6 μm
M_{1p}, M_{3p}	12 μm/0.6 μm
M_{2p}, M_{4p}	24 μm/0.6 μm
C_1, C_2, C_3, C_4	1.5 pF
R_{bias}	50 kΩ

The transient response of the peak-to-peak detector for a 1 V_{P-P} input signal at 2.5 MHz is shown in Fig. 26 with the positive and the negative peak signals. The ripple in the peak values is about 30 mV, caused due to a faster discharge rate of the capacitor. By using smaller currents, the ripple can be further filtered out. Simulation results show that the positive and negative peak values are not exactly 500 mV and –500 mV, respectively. The error is due to the finite output resistance and bulk transconductance of the input devices. The gain from the input (V_i) to the nodes C_1 and C_3 are summed up in expression (4.1) and (4.2), where g_o and g_{mb} represent the output and bulk conductance, respectively.

$$\frac{v_{c1}}{v_i} = \frac{g_{m,M2n}}{g_{m,M2n} + g_{o,M2n} + g_{o,M1n} + g_{mb,M2n}} \qquad (4.1)$$

$$\frac{v_{c3}}{v_i} = \frac{g_{m,M1p}}{g_{m,M1p} + g_{o,M1p} + g_{o,M2p}} \qquad (4.2)$$

The output and bulk conductance account for 25 % of the g_m, thus causing around 20% decrease in the peak value, of voltage stored on capacitance C_1 and C_3. Since identical peak detectors are used for the input and the output, an approximate value of the peak voltage is sufficient for tuning purposes. However an important concern is the input offset to the peak detectors. Figure 27 shows the input-output characteristics of the peak-

to-peak detector for varying input offset voltages. It can be seen that offset has minimal impact on the transfer characteristics. Any output offset difference between the two peak-to-peak detectors is cancelled, since it is common mode signal to the following stage, the DDA.

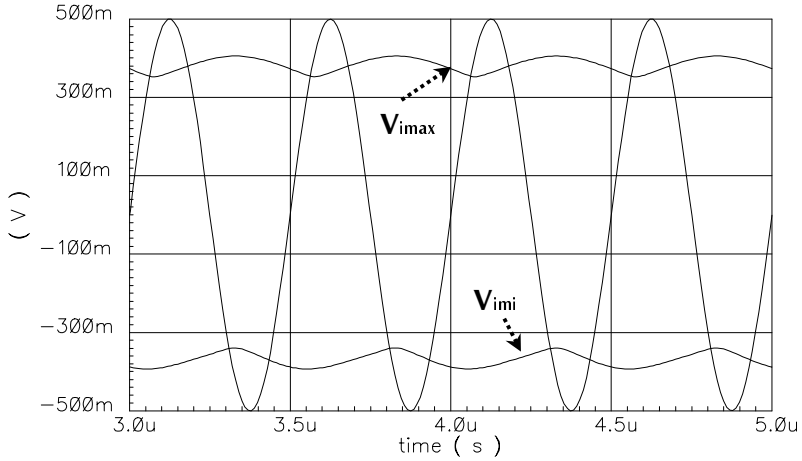


Fig. 26. Input sinusoid and output peak voltages of the peak detector.

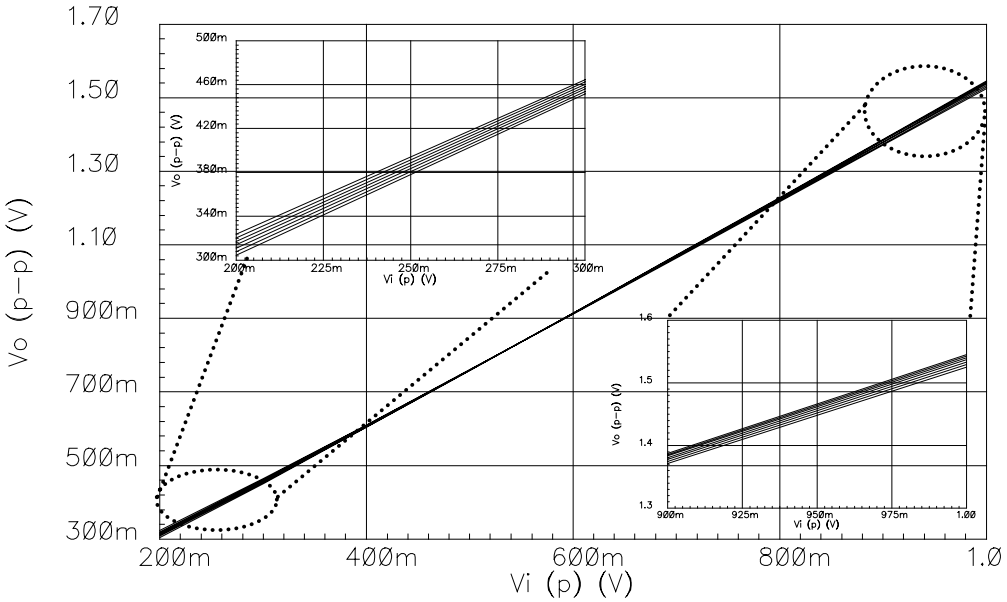


Fig. 27. Peak-to-peak detector input-output characteristics.

Two identical peak-to-peak detectors are used for the inputs and the outputs. Systematic mismatch between the positive or negative peak circuits for the inputs and outputs is not of much concern since they are cancelled at the inputs of the differential difference amplifier. However random mismatches including wafer gradients can offset the tuning process, causing improper matching. The positive and negative peak values of the input (V_i) are available at V_{imax} and V_{imin}, respectively. Two such peak detector circuits are used to obtain the four peak voltages of the line driver input and output (V_{imax}, V_{imin}, V_{omax} and V_{omin}) as in Fig. 24.

B. DESIGN OF DIFFERENTIAL DIFFFERENCE AMPLIFIER

The differential difference amplifier (DDA) is a four input, single output topology with P-type input transistors as shown in Fig. 28. The overall transfer function can be written as in (4.3), where A is the overall gain.

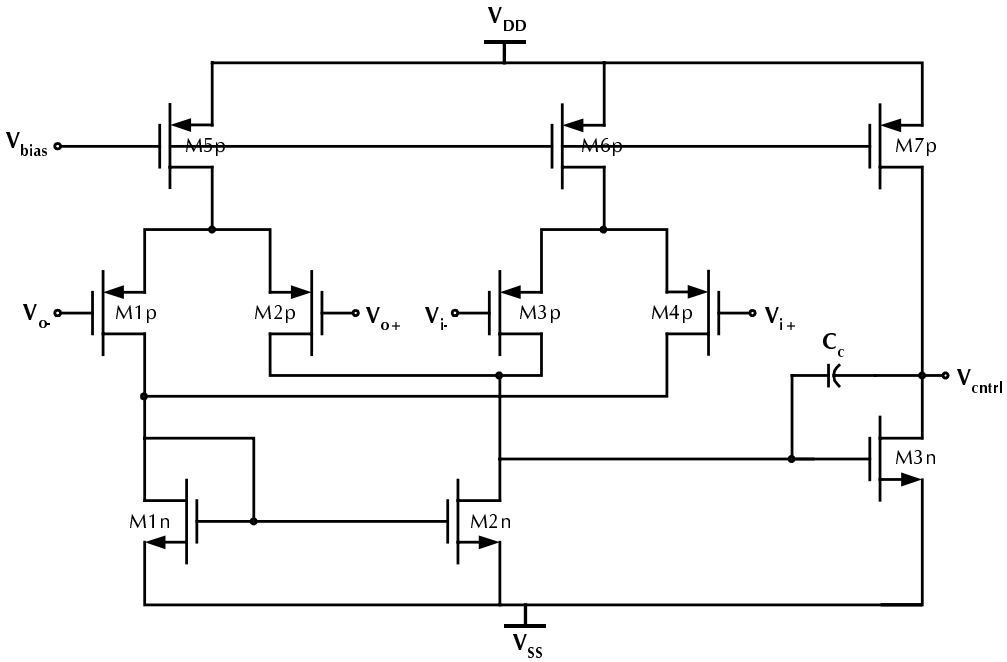


Fig. 28. Single output differential difference amplifier (DDA) topology.

$$V_{cntrl} = A((V_{o+} - V_{o-}) - (V_{i+} - V_{i-})) \quad (4.3)$$

$$V_{cntrl} = g_m((V_{o+} + V_{i-}) - (V_{o-} + V_{i+}))R_{out} \quad (4.4)$$

The circuit is realized according to equation (4.4), where the input voltages are converted to current by the input transistors (M_{1p}-M_{4p}) since it is easier to process currents than voltages. The sum of the currents due to V_{o-} and V_{i+} is mirrored by M_{1n} onto M_{2n}. This is subtracted from the current due to V_{o+} and V_{i-} and flows through the capacitor C_c, generating the output voltage V_{cntrl}. The aspect ratios for the transistors used in the design of the DDA is summarized in Table XII.

TABLE XII

DDA COMPONENT VALUES

M_{1p}, M_{2p}, M_{3p}, M_{4p}	18 μm/1.2 μm
M_{5p}, M_{6p}	12 μm/1.2 μm
M_{7p}	24 μm/1.2 μm
M_{1n}, M_{2n}	12 μm/1.2 μm
M_{3n}	18 μm/1.2 μm
C_c	2 pF

The DDA is simple by construction, yet provides 45 dB gain with a gain-bandwidth product of 20 MHz, while consuming less than 0.7 mW of power. The frequency response of the DDA is shown in Fig. 29. Since the inputs to the DDA are almost DC voltages from the peak-to-peak detector, these values are sufficient for design in tuning loop. The gain-bandwidth product often determines the overall response time of the tuning loop.

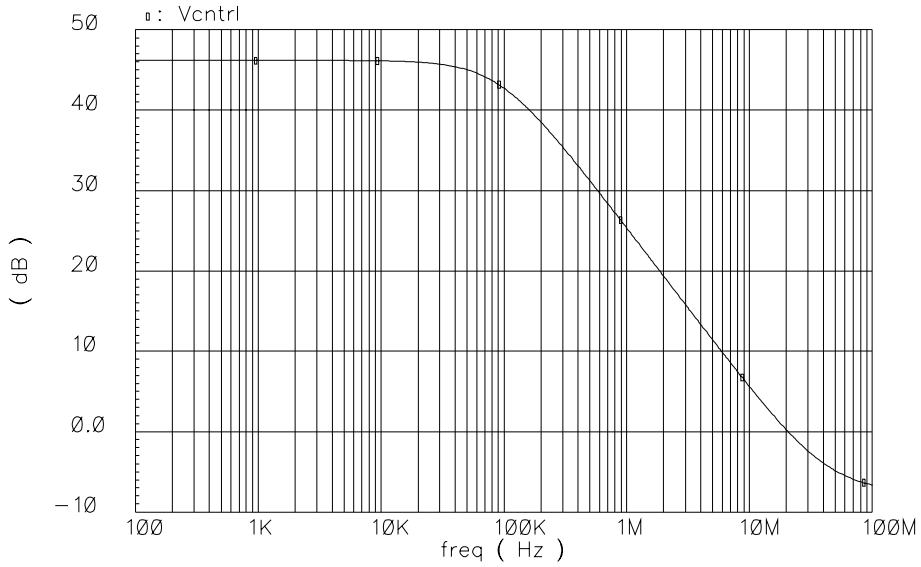


Fig. 29. DDA frequency response.

C. TUNING LOOP RESPONSE

With all components (line driver, peak-to-peak detectors, DDA) designed, the overall circuit behavior is analyzed by the transient response. For this purpose, an input reference signal of $1V_{P\text{-}P}$ at 5 MHz is chosen for tuning. The choice of the test signal is determined by the tuning loop. The input amplitude is chosen as high as possible, without saturating the line driver (typically 1-1.4 $V_{P\text{-}P}$). This is because the peak detector has a limited input range between 0.4 and 1.2 $V_{P\text{-}P}$. As a result, for small input voltages (around 200 mV), the tuning loop error cannot be tolerated. The frequency of the test signal should be close to the maximum operating frequency of line driver so as to filter out the high frequency signal components and obtain a steady state control voltage (V_{cntrl}). Simulation results indicate the overall settling time response of the tuning loop to be about 10 μs.

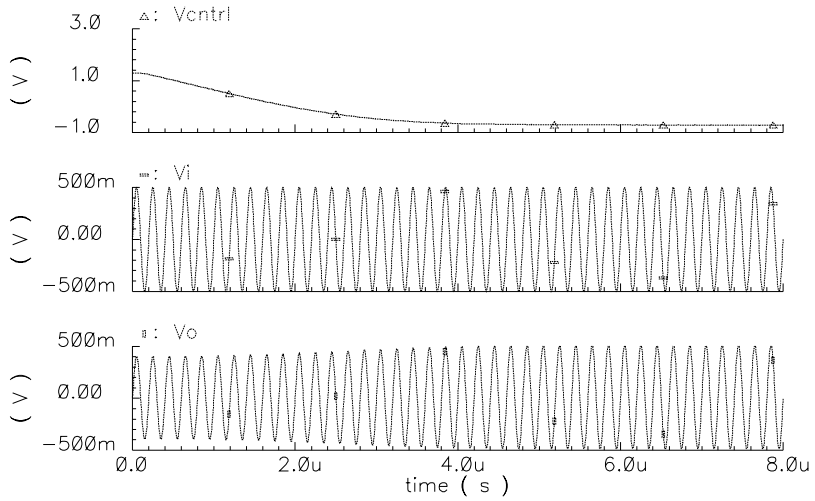


Fig. 30. Transient response of line driver with tuning circuit (R_L=65 Ω, pre-layout).

The variable resistance R_{S1} that is controlled through the feedback loop largely determines the mirroring ratio (m). If the gate-to-source (V_{GS}) voltage of the transistors M_1-M_2 and M_3-M_4 are the same, the mirroring ratio (m) is determined by the transistor dimensions (M_1-M_2 and M_3-M_4) and is equal to n. This occurs when the load resistance R_L is the same as R_{nom}. When the load resistance R_L decreases, the signal current is increased in order to maintain the same output swing as the input. This is achieved by increasing the resistance $R_{S1,}$ which consequently increases V_{G3} and decreases V_{G1}. However gate to source voltages of M_1 and M_3 do not change. On the other hand $|V_{GS2}|$ and $|V_{GS4}|$ increase, which results in an increase in the mirroring ratio (m).

When the reference signal is applied to the input, the instantaneous output voltage is in most cases (except for the nominal load of 75 Ω) different from the input amplitude. The peak voltages of both the input and output signals are extracted with the peak-to-peak detector and the error voltage (V_{cntrl}) computed by the DDA. The tuning current (I_{tune}) further generated from the control voltage adjusts the variable resistor R_{s1} suitably to increase or decrease the mirroring ratio, thereby completing the tuning loop. When the output voltage is less than the input, the mirroring ratios are increased and vice versa.

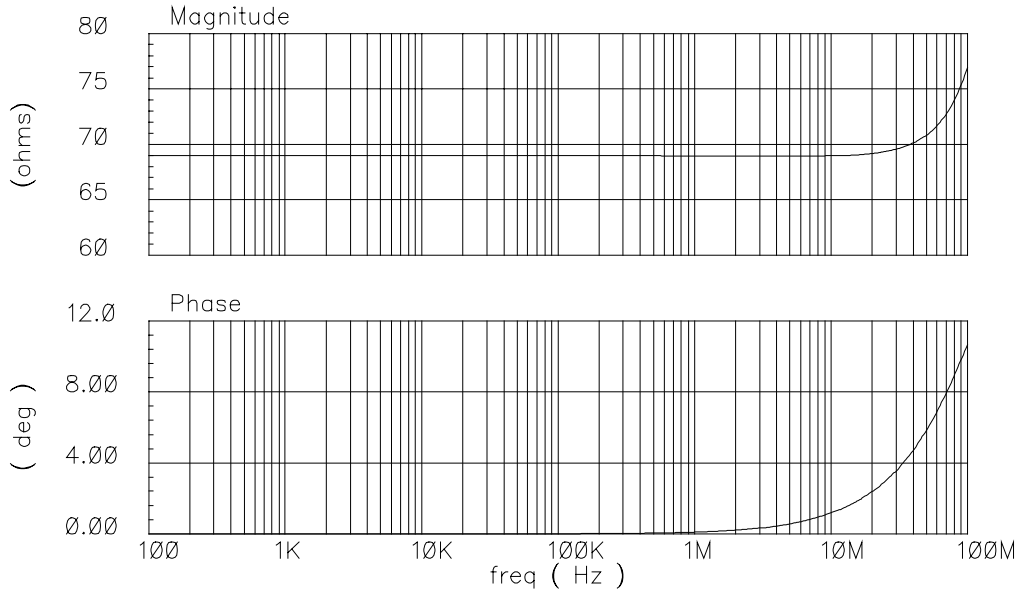


Fig. 31. Magnitude and phase of output resistance (R_L=75 Ω).

The transient response of the tuning process with the control voltage (V_{cntrl}), input (V_i) and output (V_o) is shown in Fig. 30, for a line resistance of 65 Ω. The output voltage can be seen increasing with time until its peak-to-peak amplitude is the same as the input reference voltage of 1 $V_{P\text{-}P}$. At this instance, the tuning voltage achieves a steady state condition. The error in output voltage is 1 % and the linearity is 54 dB for a 1 V signal at 100 kHz.

The tuning range for gain and output resistance varies from 60 to 130 Ω. Magnitude and phase information of the output resistance (r_o) of the line driver as a function of frequency for 75 Ω termination is shown in Fig. 31. The output resistance is 69 Ω, resulting in a mismatch of about 8 %. However the output resistance is purely resistive up to a frequency of 9 MHz, where the phase changes by 1°. The output resistance variation is less than 10 % over the tuning range.

CHAPTER V

LAYOUT AND MEASUREMENT RESULTS

In chapters III and IV, the design of the line driver with the tuning scheme were discussed, concluding with the simulation results and key design parameters. This chapter deals with the relevant layout issues and means to address them. Furthermore, the experimental set-up for testing the chip and the important characterization results are shown.

A. LAYOUT ISSUES

The material properties of semiconductor doped layers are subject to variations since it is impractical to manufacture 100 % pure silicon. These variations affect the design values of integrated resistors, capacitors and transistors, the building blocks of the chip. This makes each chip manufactured different from the other. In order to control the spread of design parameters several techniques such as matching, inter-digitization and common-centroid layout are employed for proper circuit design and performance.

Resistors are fabricated using n- or p-diffusion, poly or metal layers depending upon the value of resistance (low, medium or high). Poly-resistors are ideal for integration due to their medium value of sheet resistance. These poly-resistors are encased in field oxide layers and thus have lower parasitic capacitance and better noise performance [15]. All the resistors in the line driver design are constructed using poly1 layers with a sheet resistance of 20 Ω/square. The resistors are laid-out in an n-well with guard rings to prevent spurious signal injection. Furthermore, dummy strips are added to provide uniform etch rates. Fig. 32 shows the resistor bridge in the output stage of the line driver, whose layout is shown in Fig. 33. The resistors are in a serpentine fashion with a common-centroid arrangement. This helps to even out the gradients caused due to material imperfections or fabrication process.

Resistors that cannot be matched (R_{s1a} in Fig.22) are also laid out in serpentine fashion in an n-well to provide noise immunity. Since the effective resistance is controlled through a MOS transistor in linear region, variations in the absolute value of the resistor can be tolerated. In designing very small resistances (R_{s2a}, R_{s2b}), large widths are utilized. This reduces the effect of etching uncertainties on the resistor values. A large array of contacts are utilized in each resistor for interconnects so that the contact resistance does not affect the poly-resistor value.

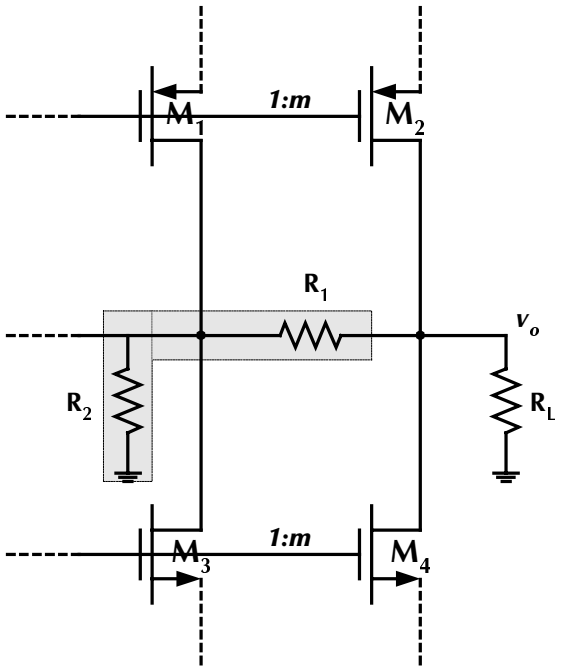


Fig. 32. Line driver output stage with bridge resistance (R_1, R_2).

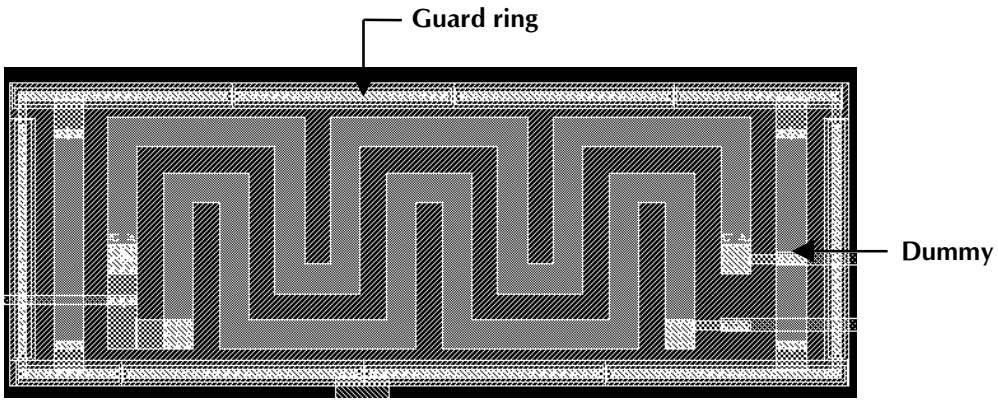


Fig. 33. Layout of matched resistors R_1 and R_2.

Capacitors in integrated circuits have similar issues as resistors in terms of tolerances. Standard processes offer junction capacitors, MOS capacitors and poly or thin-film capacitors. Poly-poly capacitors are ideal for integration in terms of noise performance, reduced parasitic capacitance and smaller area. The non-linearities associated with MOS capacitances can also be avoided. Fig. 34 shows the layout of the capacitors (C_1-C_4 in Fig. 25) in the peak-to-peak detectors. The bottom layer is poly1 that is common to all the capacitors. The top layer is poly2 and it defines the area and hence the effective capacitance. Dummy poly2 strips around the capacitors ensure uniform etching. Guard rings around the poly1 layer provide noise immunity. The capacitors are rounded off at the edges to prevent the fringing effects of the electric field.

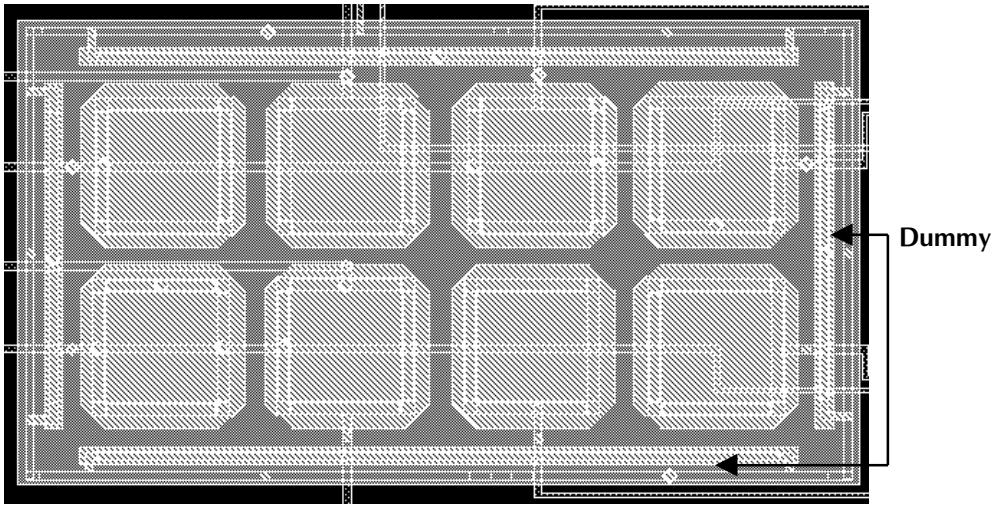


Fig. 34. Layout of capacitors in peak-to-peak detector.

Transistors are laid out in common centroid and inter-digitized wherever possible to reduce mismatch and cancel out gradients. Transistor pairs having identical gate lengths and sharing a common source or drain node can be properly matched. This includes the differential pair and current mirrors in the error amplifiers (OTA1 and OTA2) and the differential difference amplifier (DDA). The overall layout of the entire chip with the line driver and tuning circuit is shown in Fig. 35. The chip occupying 270 x 290 μm is placed in a 40-pin DIP package, with a total of 13 pins required by design and the rest unconnected. The pins for the signal input and output are chosen to have the least pad capacitance from the package information provided by MOSIS. Most of the other pins are static in nature, required for biasing the error amplifiers (OTA1, OTA2), differential difference amplifier and the peak-to-peak detectors.

The final layout is verified with the schematic for structural equivalence and the component values are extracted along with the associated parasitic. The extracted cell view is simulated to cross check with pre-layout simulation results. Fig. 36 shows the tuning response for the line driver in conditions similar to the pre-layout version (Fig. 30).

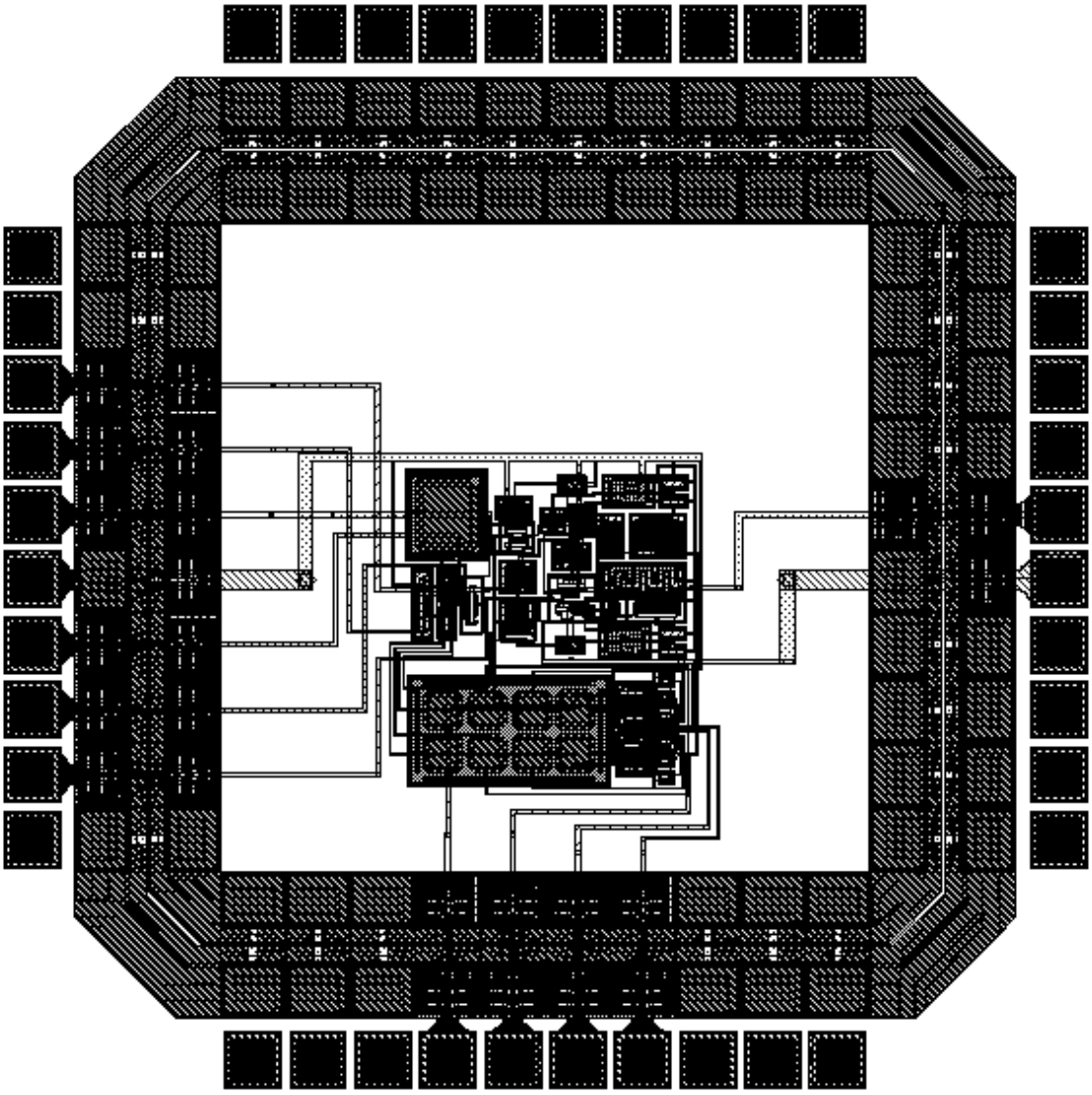


Fig. 35. Full chip layout with bond pads.

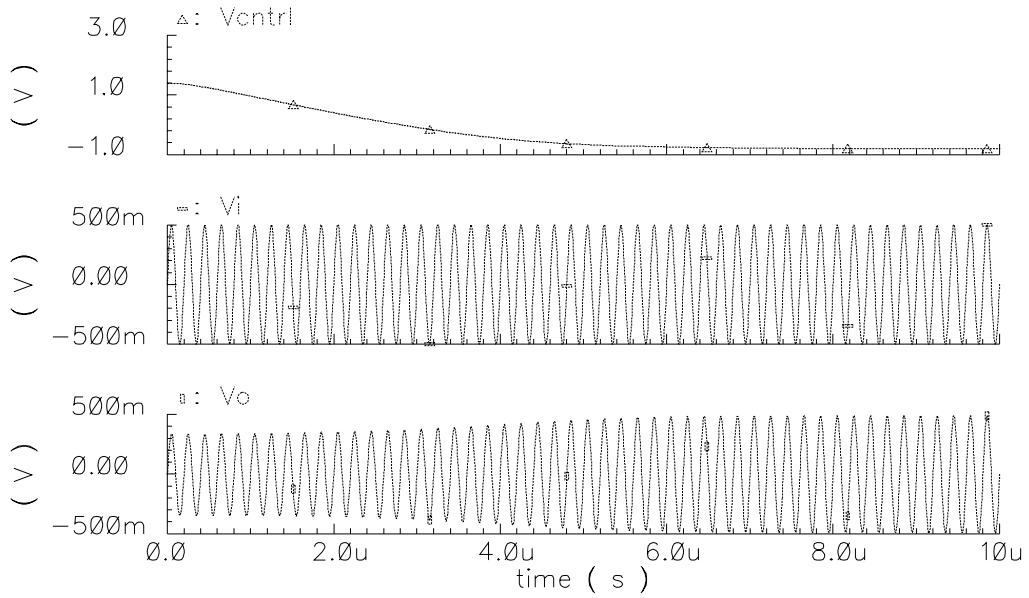


Fig. 36. Transient response of line driver with tuning circuit (R_L=65 Ω, post-layout).

Simulations show identical results for circuit response between the pre-layout and post-layout designs. The post-layout simulations are more accurate in terms of parasitic and component values. A complete characterization of the layout requires the design to be stable and functional across process, temperature and supply voltage corners. Process variations tend to make the transistors fast or slow. Temperature affects the mobility of the carriers and integrated resistors have temperature co-efficient that change their values. Supply voltage variations can cause gain reduction or push transistors out of the saturation region, wherein the design fails to function.

In order to characterize the design, the tuning response of the line driver is tested for a combination of process (min, nom and max), temperature (-40, 27 and 80 ° C) and voltage (3, 3.3 and 3.6 V). Further the line resistance is also varied from 65 to 135 Ω. Though not all combinations of PTV (process, temperature, voltage) and line variations

are tested, key design corners are simulated with a 1 V_{P-P} input. The measured output voltages are given in Table XIII. The maximum error in the output voltage is 3 % caused mainly due to the reduced supply voltage and consequently lower output swing.

TABLE XIII

LINE DRIVER PERFORMANCE CHARACTERIZATION

Process	Temperature (° C)	Voltage (V)	Line Resistance (Ω)	Output voltage (mV)
T17z	27	3.3	75	987
T17z	27	3	75	970
T17z	27	3.6	75	987
T17z	85	3.3	75	980
T17z	-40	3.3	75	992
T17z	27	3.3	65	982
T17z	27	3.3	135	1005
T21s	27	3.3	75	986
T24o	27	3.3	75	987

Fig. 37 shows the AC response of the line driver for 3 different line conditions-65, 75 and 135 ohms. The gain is one for each case, with the 3 dB bandwidth of 225 MHz with 5 pF load capacitance. The gain variation from 100 kHz to 5 MHz (signal bandwidth) is less than 2 %. The linearity is better than 50 dB across the tuning range between 65 and 135 Ω. Power consumption is 22.7 mW with the tuning circuit consuming 10 % of it.

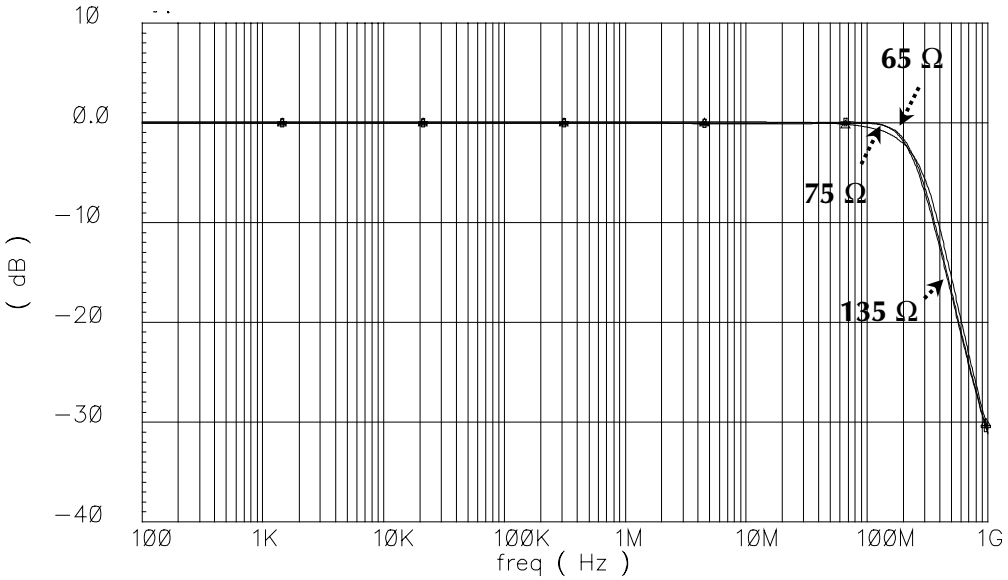


Fig. 37. Frequency response of line driver (R_L=65, 75 and 135 Ω).

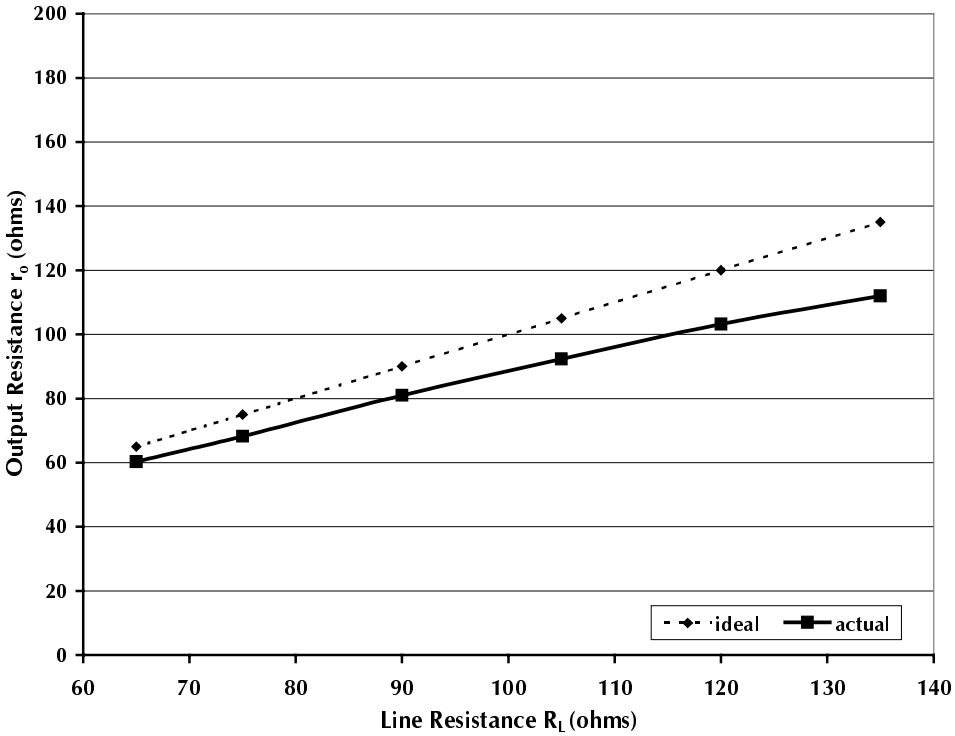


Fig. 38. Output resistance as function of line resistance (R_L).

The central idea of the line driver design relies on impedance matching between the output stage and the line. In Fig. 38, the relation between output resistance (r_o) of the driver and the line resistance (R_L) is shown. The dotted line represents the ideal impedance matching condition of R_L equal to r_o. The maximum error between the ideal and actual output resistance is 20 %. Table XIV summarizes the key results from layout.

TABLE XIV

LINE DRIVER PERFORMANCE METRICS (LAYOUT)

Technology	0.5 μm CMOS 3 metal 2 poly
-3 dB bandwidth	220 MHz
Gain Flatness	2 % upto 5 MHz
Output Voltage Range	± 0.9 V
Tuning range	65 to 135 Ω
Linearity	> 50 dB (1.2 V_{p-p})
Power Consumption	22.7 mW
Power Efficiency (@ 1.2 V_{P-P})	11 %
Voltage Supply	± 1.65 V

B. PCB MEASUREMENT SETUP

The chip is packaged in a 40 pin DIP with 13 functional pins. Fig. 39 shows the experimental setup required to characterize the chip. Two pins are required for the input and output, two for the supplies and one for the ground connection. Five pins (IBIAS1, IBIAS2, IBIAS3, VTP and VTN) provide the bias for the error amplifiers, DDA and peak-to-peak detectors through external resistors. The tuning loop is completed externally by short-circuiting VTUNEOUT2 and VTUNEIN. This is useful for observing the tuning voltage (V_{cntrl}). Further it also helps to evaluate the line driver performance in the absence of tuning by opening the loop and feeding a constant DC voltage (tuning voltage at 75 Ω) to VTUNEIN. The pin VOUT is connected to the load (R_L) and a buffer to prevent loading of the output by the measurement probe. The setup requires no transformers or baluns since all the signals are single-ended. The PCB is designed using PROTEL software. Due to the simple design, all tracks are routed in the bottom layer interconnecting the components on top as seen in Fig. 40. Chip sockets (DIP40 and DIP8) are used for mounting the line driver and output buffer. The buffer used is a Burr-brown BUF601 amplifier with a bandwidth of 200 MHz at 5 pF load. Potentiometers (100 kΩ) are used to control bias currents for peak detector and DDA. The tuning loop is completed through a jump switch as shown in Fig. 41.

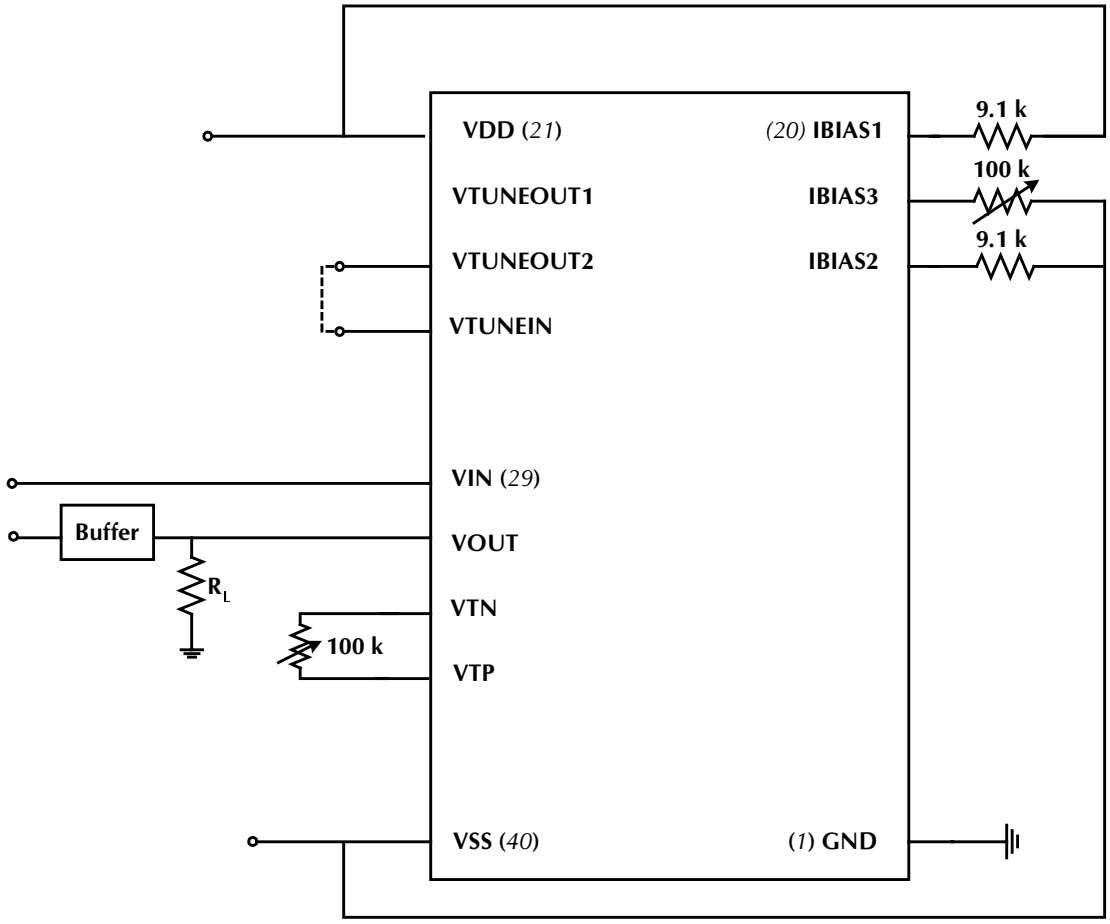


Fig. 39. Experimental setup for line driver characterization.

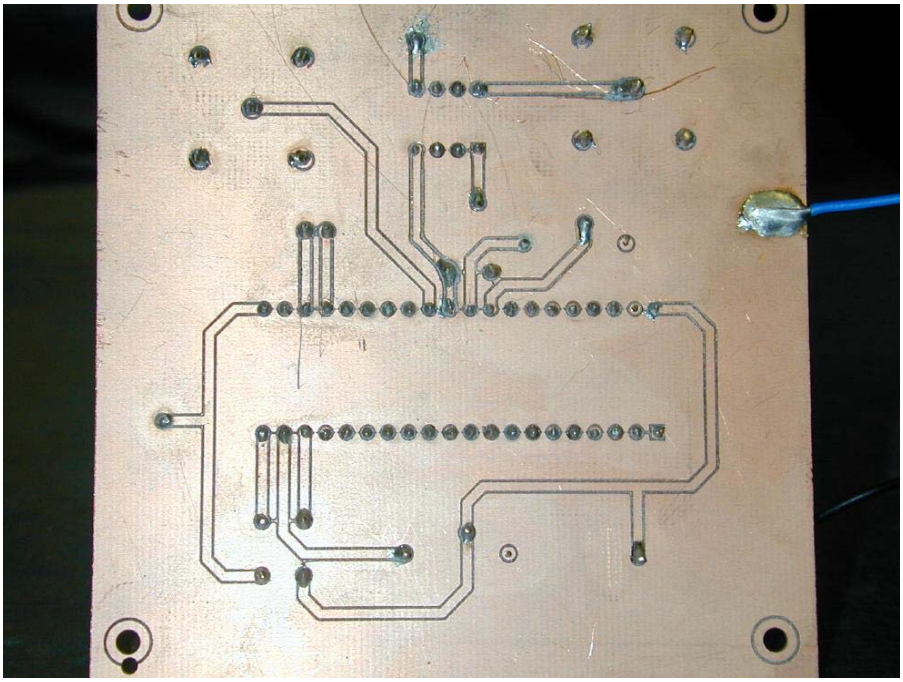


Fig. 40. PCB bottom layer with routing tracks.

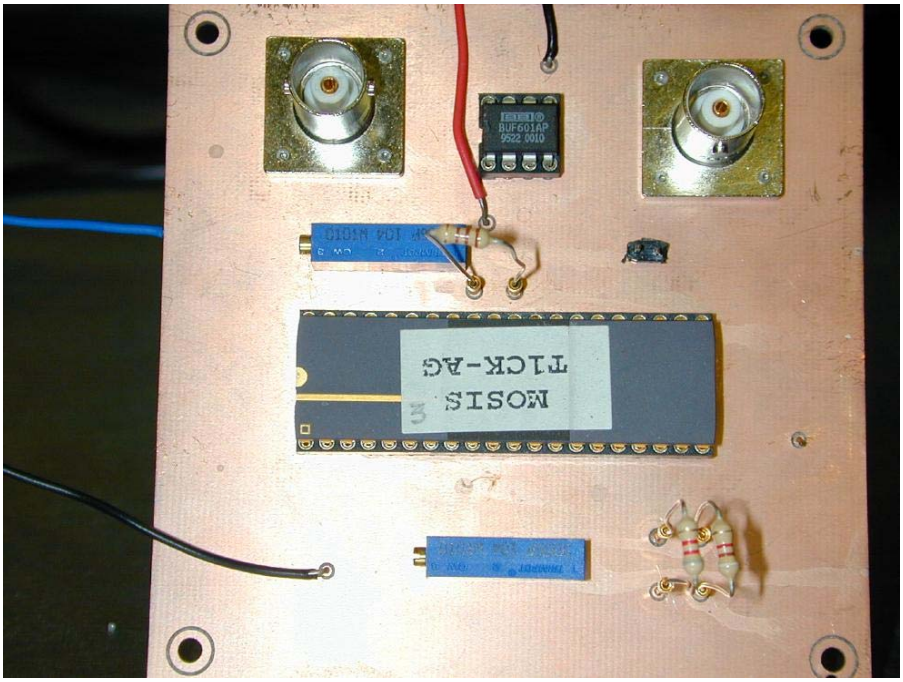


Fig. 41. PCB top layer with components.

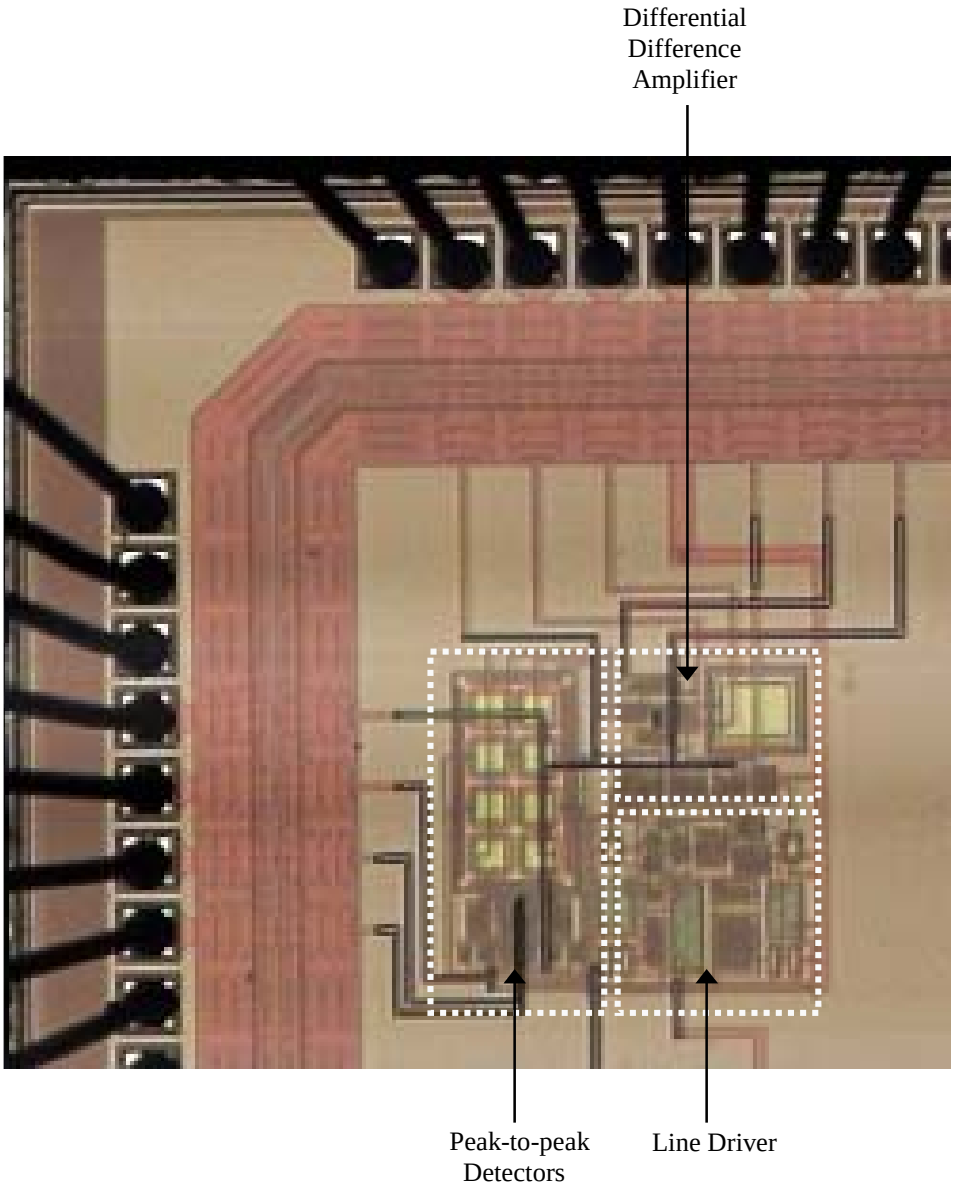


Fig. 42. Chip microphotograph.

C. MEASUREMENT RESULTS

The line driver with the tuning loop is integrated in a standard 0.5μ CMOS process. The microphotograph of the fabricated chip is shown in Fig. 42. The active area is about 0.22 mm^2. The input of 1 V sinewave at 5 MHz is generated from Agilent 33250A function generator while tuning response of the line driver is observed with Agilent Digital Oscilloscope. The tuning voltage at 75 Ω is used to characterize the line driver in the absence of tuning by feeding a constant DC voltage to VTUNEIN pin and opening the feedback loop.

1. Gain Response

The line driver AC response with and without impedance matching is shown in Fig. 43. In the absence of tuning, the output voltage exceeds or is less than the input. This is because a fixed current is supplied to the load, irrespective of the line impedance. However for the case of tuning, variable current is provided to the load by adjusting the mirroring ratio (m), thereby forcing the output to follow the input. Thus as load resistance increases, current is decreased and vice versa to achieve constant output. The tuning range is this case varies from 65 to 160 Ω with less than 3 % error between input and output voltage.

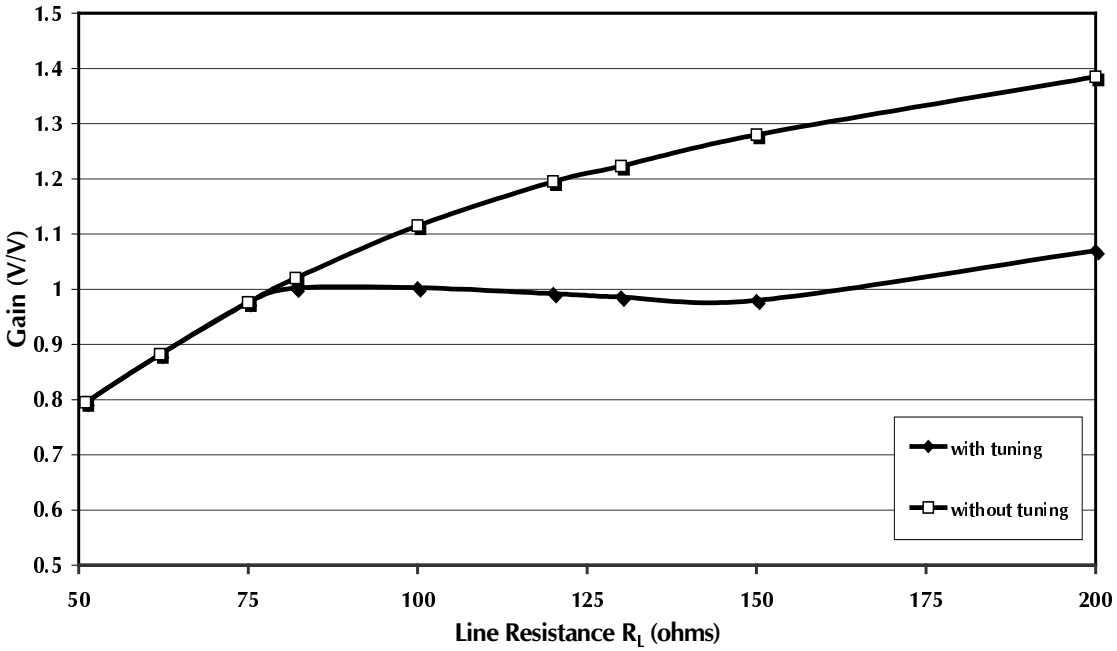
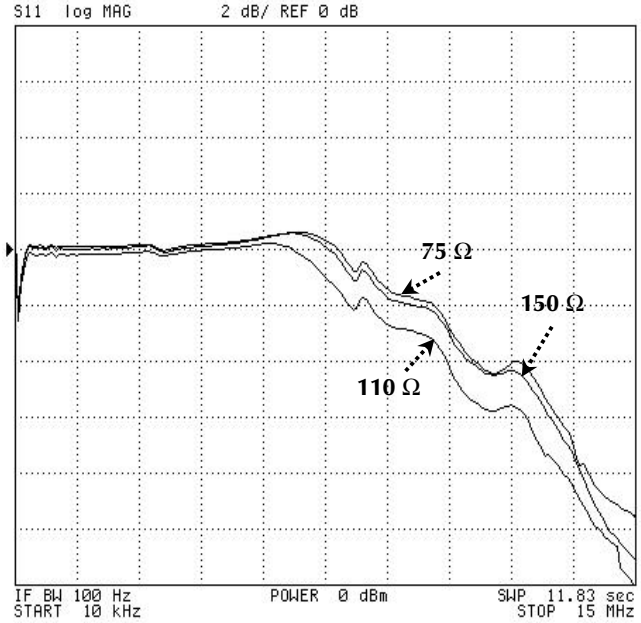
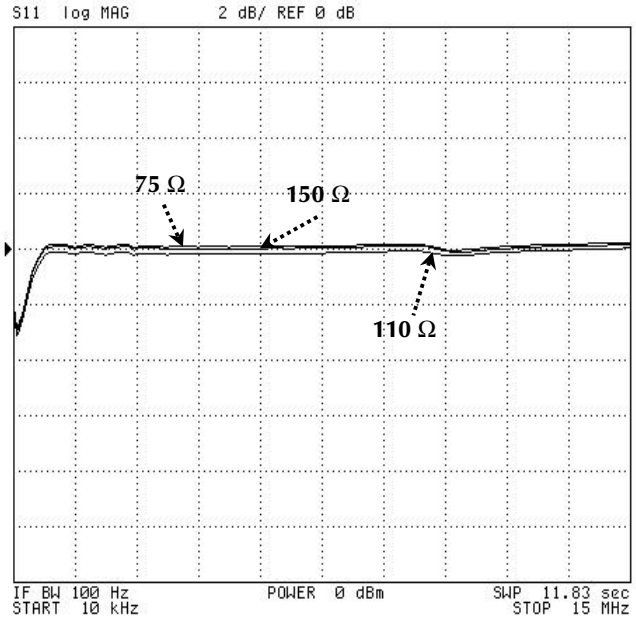


Fig. 43. Gain of line driver versus line resistance (R_L).

The gain versus frequency response is measured using HP 4395 network analyzer and the AC response is shown in Fig. 44(a) for the line driver at 75, 110 and 150 Ω line impedance. The bandwidth in all three cases is around 15 MHz due to the loading of the output stage. The gain is equal to 1 in the case of 75 and 150 Ω load, while it is 0.98 at 110 Ω, an error of 2 %. The gain flatness is accurate to 0.1 % variation upto 5 MHz as seen in Fig. 44(b).



(a) 10 kHz - 20 MHz



(b) 10 kHz – 5 MHz

Fig. 44. Frequency response for R_L of 75, 110 and 150 Ω.

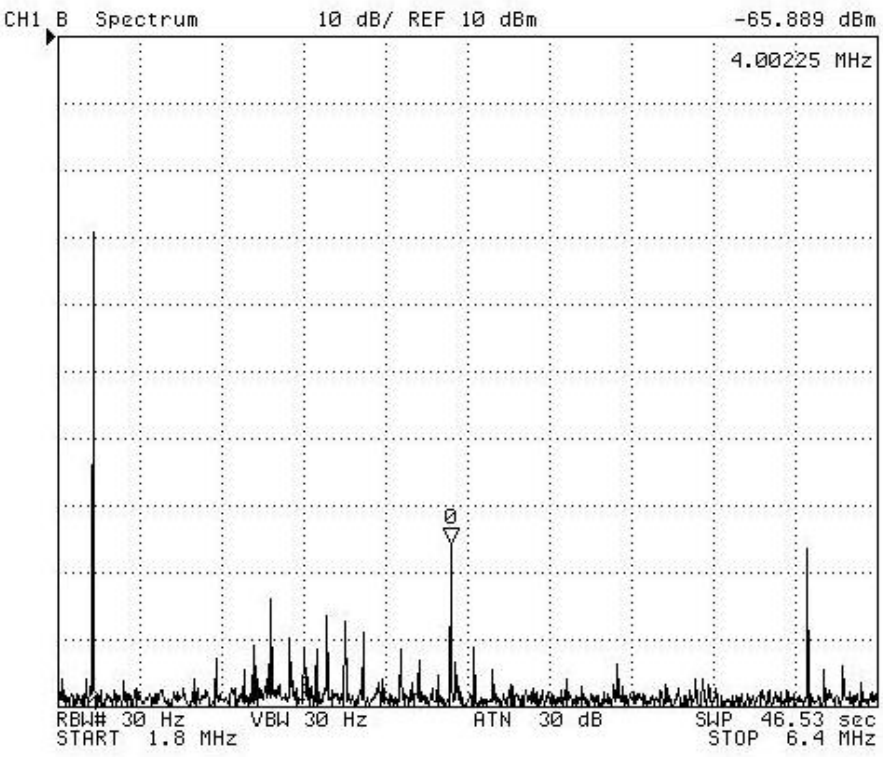


Fig. 45. Frequency Spectrum at 75 Ω load, 1 V_{p-p}, 2 MHz input.

2. Linearity

While impedance matching to provide uniform performance is essential, the linearity of the line driver cannot be sacrificed. This imposes additional constraints to the design in terms of distortion specifications. Fig. 45 shows the distortion performance for 75 Ω line impedance and 1 V_{P-P} output at 2 MHz measured using HP4395 spectrum analyzer. The 2nd harmonic is lower than 45 dB compared to the input and improves with lower frequency. Due to the single ended nature of the design, even harmonics dominate. Fig. 46 shows the linearity measurement as a function of frequency for three different line impedance at 1 V_{P-P} while Fig. 47 shows linearity against input voltage for 500 kHz input frequency. The overall line driver performance is better than 42 dB over the frequency range from 100 kHz to 5 MHz, with 1 V_{P-P} output.

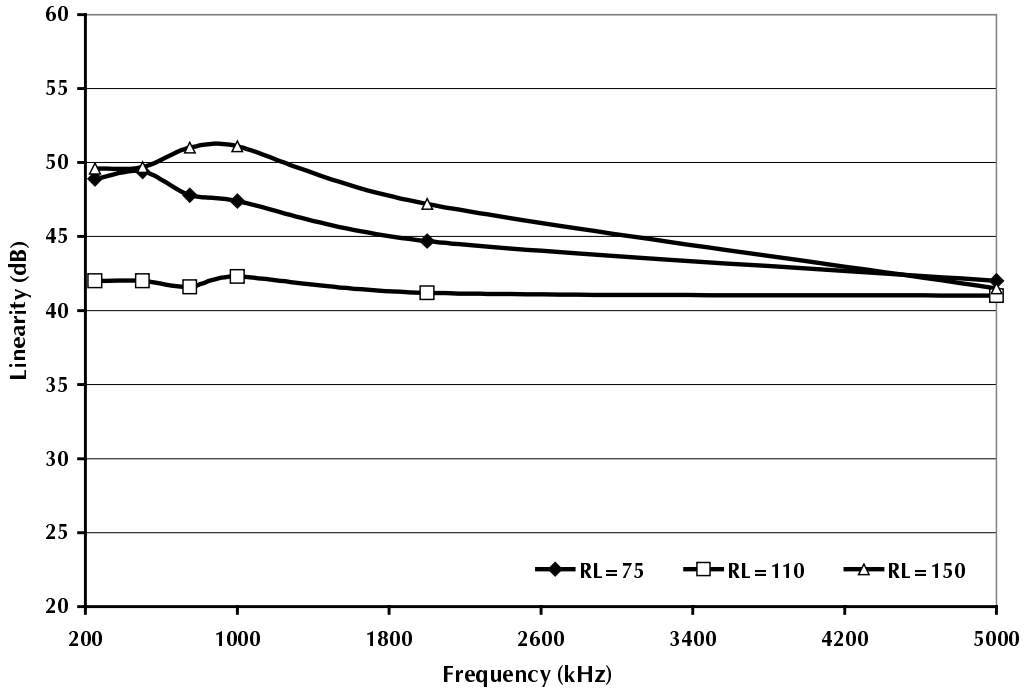


Fig. 46. Linearity as a function of frequency for different line resistance (R_L).

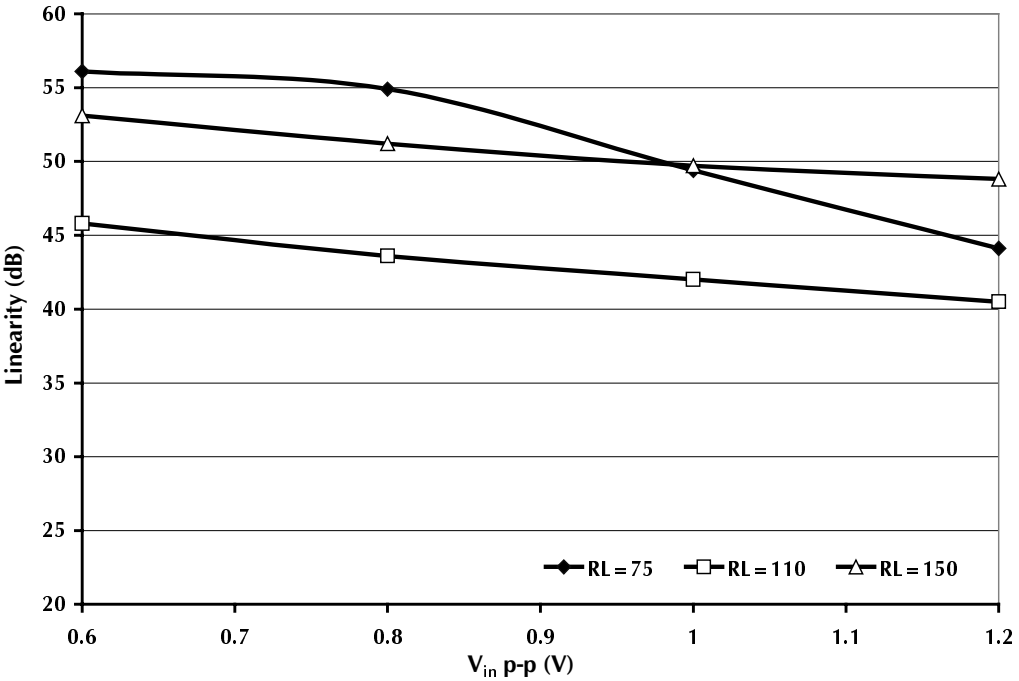


Fig. 47. Linearity as a function of input voltage for different line resistance (R_L).

TABLE XV

LINE DRIVER CHIP MEASUREMENT RESULTS

Technology	0.5 μm CMOS 3 metal 2 poly
-3 dB bandwidth	15 MHz
Gain Flatness	0.5% to 5 MHz
Output Voltage Range	± 0.75 V
Tuning range	65 to 160 Ω
Linearity	> 50 dB (1.2 V_{p-p})
Power Consumption	27 mW
Voltage Supply	± 1.65 V

Table XV summarizes the experimental results of the line driver. Across a wide range of line impedance, the linearity has been shown to be consistently better than 42 dB for 1 V swing and gain response is unity with an error of less than 3 %. The power consumption is 27 mW with the tuning loop consuming about 15 % of it. The line driver can be easily scaled for different supply voltages from 3 to 6 V. The input test signal amplitude has to be correspondingly scaled to achieve best results.

CHAPTER VI

CONCLUSION

Several line driver topologies are presented in this thesis and the design of video line drivers is explored. The importance of impedance matching in eliminating signal reflections is emphasized and a new class AB topology with controlled impedance is presented. This topology has the property that when the gain is unity, the output resistance is the same as the line resistance. In this manner, impedance matching is achieved.

The tuning scheme is simple yet robust. Peak-to-peak voltage matching is utilized to make the gain of the line driver unity. The line driver can be calibrated offline during power up or before actual transmission. This would require additional hardware such as a sampling switch that can hold the tuning voltage after calibration and during the data transmission period.

The tuning range from 65 to 160 Ω is sufficient for the application. The linearity however suffers due to the single ended nature of the design. Further the supply voltage is also reduced for power efficiency and the threshold voltage of the MOS device are high for 0.5 μ CMOS process. A redesign with a faster process technology (0.35 / 0.25 μ) and a fully differential line driver can achieve better linearity results.

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