AUTOMATIC TUNING FOR LINEARLY TUNABLE FILTERS

A Thesis

by

SUNG-LING HUANG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Aydin Karsilayan (Chair of Committee)	
Edgar Sanchez-Sinencio (Member)	Kai Chang (Member)
Chii-Der Suh (Member)	Chanan K. Singh (Head of Department)

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ABSTRACT

Automatic Tuning for Linearly Tunable Filters.

(May 2004)

Sung-Ling Huang, B.S., Tatung Institute of Technology, Taiwan;

M.S., Tatung Institute of Technology, Taiwan

Chair of Advisory Committee: Dr. Aydin I. Karsilayan

A new tuning scheme for linearly tunable high-Q filters is proposed. The tuning method is based on using the phase information for both frequency and Q factor tuning. There is no need to find out the relationship between a filter's passband magnitude and Q. A g_m-C biquadratic filter is designed to demonstrate the proposed tuning circuitry. The project includes a phase locked loop (PLL) based frequency tuning loop, reference clock generator, and differential difference amplifier (DDA) for dealing with frequency and Q factor tuning loop and linearly tunable second order g_m-C bandpass filter. Simulation results for a 10 MHz prototype filter using AMI 0.5μm process is presented. The chip testing results show that the automatic frequency tuning error is 2.5% for the 10 MHz case.

DEDICATION

To my wife, my son, my mother, and the memory of my father

ACKNOWLEDGEMENTS

It has been an honor to be a M.S. student of the Analog and Mixed-Signal Center, Texas A&M University, and to work with Dr. Aydin I. Karsilayan. His keen insight into analog circuit design and analysis is the key factor in my successful research. He has provided guidance and encouragement to my study and research over the past few years.

I am so thankful for Dr. Sanchez of our AMSC group. I took his course and got resourceful knowledge from him. He is kind and willing to answer questions. His suggestion about my research was very helpful in making my research more complete. I would also like to thank Dr. Kai Chang. He has served as a committee member and I also learned a lot from his microwave integrated circuit course.

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CHAPTER I

INTRODUCTION

Filters are designed to pass a specific frequency band in the frequency domain while rejecting other frequencies [1]. Based on the passband and stopband frequency specifications, filters can be classified as lowpass, highpass, bandpass, and bandstop. Integrated continuous time filters have many applications in many areas such as video range systems and RF communications. High frequency and high quality factor (Q) filters [2-5] are widespread throughout the design of RF communication circuits [6]. In integrated circuit filter design, manufacturing process variation and parasitics limit the filter's accuracy. For obtaining the desired center frequency and Q of an integrated filter, automatic tuning system is needed.

Continuous time filters can be implemented using several techniques. The basic fundamental structure is based on passive elements where resistors, inductors, and capacitors are designed to realize a specific transfer function. Although integrated inductors can be used to design in high frequency applications, the parasitic series resistor can decrease the Q of the filter. Another implementing method is using gyrators [7] to emulate the inductor. Active RC filters are built using resistors, capacitors, and operational amplifier. The operating frequency of such filters is low and the RC variation causes the filter's parameters to drift. MOSFET-C filters are specific types of active RC filters where resistors are replaced by MOSFETs working in the triode region.

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Switched-Capacitor filters have accurate response at relatively low frequency. Operational transconductance amplifier-capacior (OTA-C) filters are other choices to implement continuous time filters [8].

OTA-C filters are good candidates for high frequency (from a few MHz to several hundreds of MHz) operation. OTA-C filters are constructed by OTAs and capacitors. They are very suitable for a high frequency signal processing application, but due to the process variation and parasitic effects, that can cause the filter's parameters to be incorrect.

In general second order OTA-C filter design, gyrator in designing biquad can implement integrated inductors. The biquad is the second order filter structure and higher order filters can be built by cascading it. The biquad's center frequency and Q are two important characteristics. The two parameter errors are caused by process variation and parasitics. To compensate the biquad's parameter errors generated by such factors, automatic tuning circuits are needed. The tuning system adjusts the biquad's parameters to the desired value.

In this research, we propose a new tuning scheme for second order high Q filters. The scheme uses the phase information for both center frequency and Q tuning. This tuning method does not need to find out the relationship between the filter's passband magnitude and its Q value. Most Q tuning schemes assume a certain relationship between the filter's quality factor and its passband gain. This assumption relies on matching of the filter's transconductances and capacitors, including the additional parasitic. This may limit the accuracy of tuning in the presence of dominant or large

parasitics. But it needs linearly tunable OTAs and filters. To get the wide tuning range, we designed a linearly tunable filter and proposed a new tuning method to tune the filter.

1.1 Organization of Thesis

In the following part of this thesis, many topics will be discussed. In Chapter II, the existing linear OTAs will be covered for giving basic knowledge to understand linear OTAs and their tuning ideas. The circuit structure of linearly tunable OTA will be investigated and explored. The second order biquad linearly tunable filter will be addressed. Through Chapter III, most existing filter tuning methods will be addressed. The master-slave tuning scheme for both frequency and Q tuning will be investigated. The proposed new tuning method will be explained and its implementing circuit structures will be provided. Simulation and experiment results of the tested chip will be covered in Chapter IV. Chapter V summarizes this research work and gives some future directions of this research.

CHAPTER II

LINEARLY TUNABLE OTA AND FILTER DESIGN

2.1 OTA's Application and Circuit Implementation

Operational transconductor amplifier (OTA) is the basic element used in building OTA-C filters. OTAs are especially used in filters and instrumentation amplifiers with high cut-off or corner frequencies. Furthermore, they can be used in switching current mode analog-to-digital converters (ADCs) and hard-disk drive circuits.

2.1.1 Single Ended OTA

The OTA has attracted a great deal of attention as a fundamental building block in analog continuous time circuits. In Figure 2.1, a simple CMOS OTA is composed of a self-biasing MOSFET differential stage with active load. Transistor M_1 and M_2 form a matched transistor pair with equal W/L ratios. Transistor M_3 and M_4 also have equal W/L ratios as well. All current levels are determined by current source I_B, half of which flows through M_1 and M_3, the other half flowing through M_2 and M_4. In low frequency operating range, the transconductance of the OTA is given by $G_m=g_{m1}=g_{m2}$, which is given by

$$G_m = \sqrt{2k_n I_B (\frac{W}{L})_1} \qquad (2\text{-}1)$$

$(W/L)_1$ is the aspect ratio of input transistors; k_n is the transconductor parameter for an NMOS. Current I_B in equation (2-1) is the total supply current, which is twice the current through one transistor M_1 or M_2.

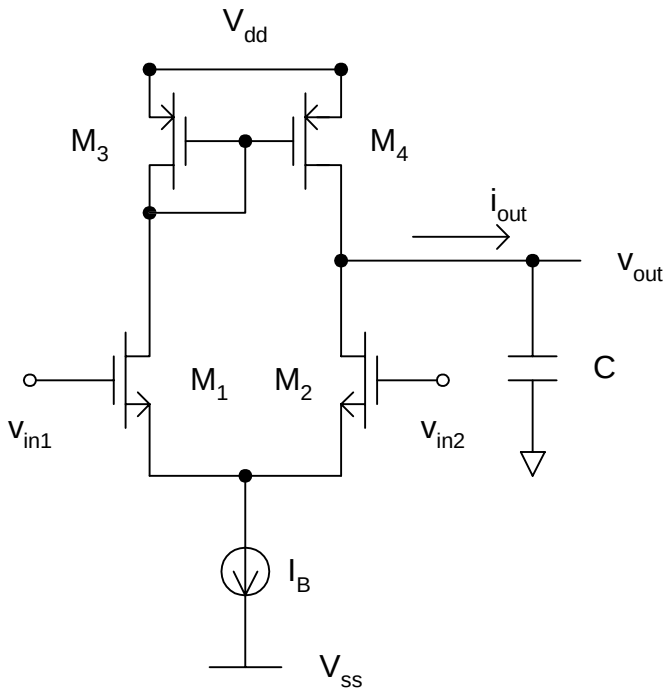

Figure 2.1.Configuration of Simple CMOS OTA

2.2 Linear OTAs and Circuit Structures

If the input transistors are working in the saturation region [9], MOS transistor's square law is usually exploited in such a way that linearization is achieved [10, 11]. If the transistors are working in the triode region, it is to obtail linear voltage-current (V-I) relationship [12, 13].which leads to transconductors with high linearity and a wide

tuning range. In this thesis, a special type of filter is designed where the center frequency is a linear function of its control voltage. This design requires a linearly tunable transconductor. Many linear OTAs have been reported in the past [14-18]. According to the general classification of OTAs by these references, linear OTAs can be approximately classified in four categories: Tunable Biased Source-Coupled Input Pair, Cross-Coupled Differential Pair, Differential Pair with Input Common Mode Signal and Regulated Cascode Input Differential Pair.

2.2.1 Tunable Biased Source-Coupled Input Pair

The tunable biased source-coupled input pairs' circuit structure can be shown in Figure 2.2. When I_s is fixed, the transconductance has no linear relation between the input voltage and output current. The output differential current can be shown as

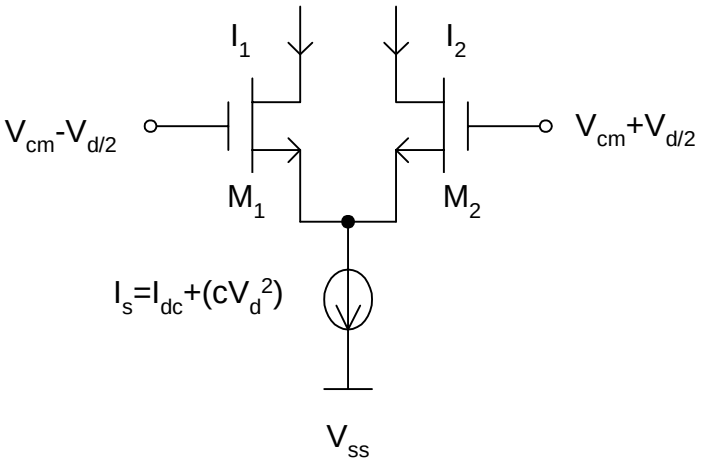

Figure 2.2 Principle of Tunable Biased Source-Couple Input Pair

$$\Delta I = I_1 - I_2 = \sqrt{2I_s K}V_d \sqrt{1 - \frac{K}{2I_s}V_d^{\,2}} \tag{2-2}$$

$$\Delta I = \sqrt{2I_{dc} K V_d} \sqrt{1 - \frac{K - 2C}{2I_{dc}}V_d} \tag{2-3}$$

The output differential signal can be linearized if the current source satisfies

$$I_s = I_{dc} + CV_d^{\,2} \tag{2-4}$$

The input transistor pair M_1, M_2 are adaptively biased by setting C=K/2. The detailed circuit structure is shown in Figure 2.3. The circuit consists of two unbalanced differential pairs (M_3 to M_6). The output is taken as the sum of the drain currents in the two smaller transistors M_3 and M_6. The percentage error of the output differential current [15] is expressed by

$$\varepsilon = \frac{\Delta I - g_m V_d}{g_m V_d} \tag{2-5}$$

In this circuit structure, input common mode voltage V_{cm} does not change the linearity error significantly.

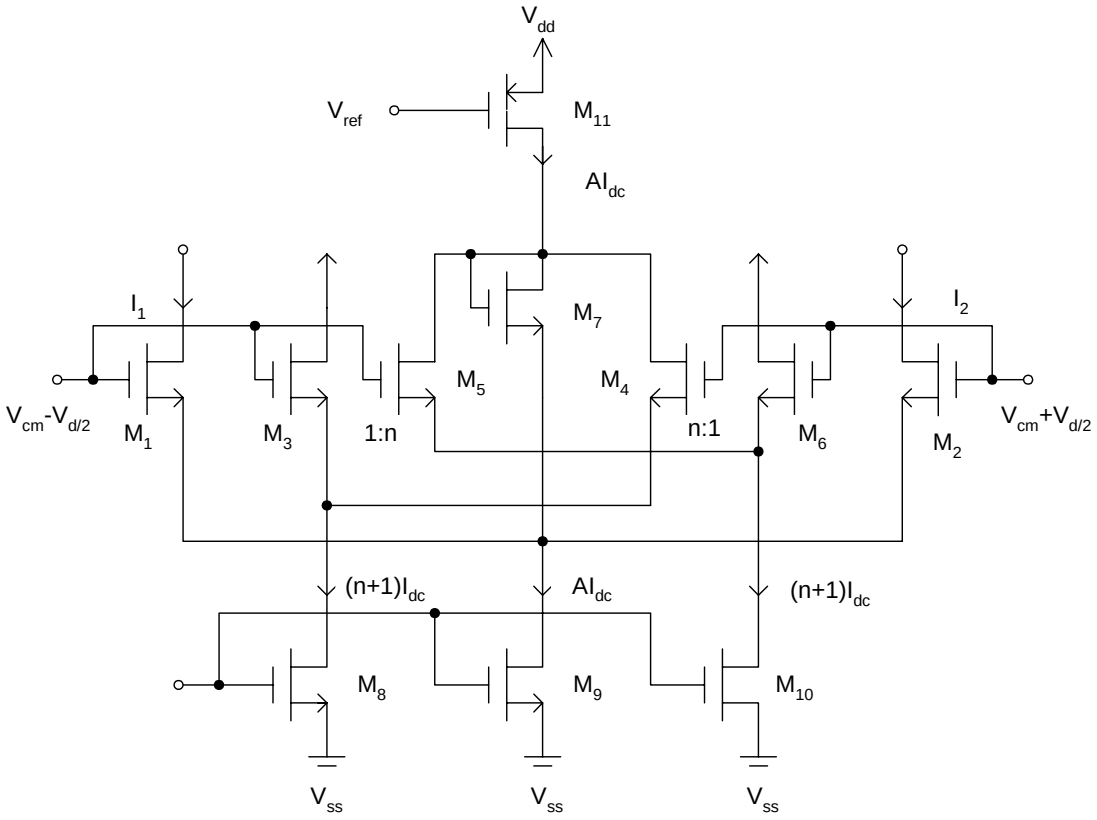

Figure 2.3. Implementation of an Adaptively Biased Source-Couple Pair

2.2.2 Cross-Coupled Differential Pair

Many circuit designers use the cross-coupled differential pair [14,15] shown in Figure 2.4. All transistors have the same dimensions and operate in saturation region. The output transistor's differential current is proportional to the input differential voltage V_d and its tail current control voltage V_s. The transconductance can be affected by the changed threshold voltage ΔV_t. The output differential current can be written as

$$\Delta I = I_1 - I_2 = \frac{W}{L}\beta(V_s + \Delta V_t)V_d \tag{2-6}$$

when the differential voltage satisfies

$$|V_d| \le 2|V_{CM} - V_s - V_t - \Delta V_t| \tag{2-7}$$

In Figure 2.4, a stable current source which is controlled by V_s will get a good common mode rejection ratio (CMRR) [14].

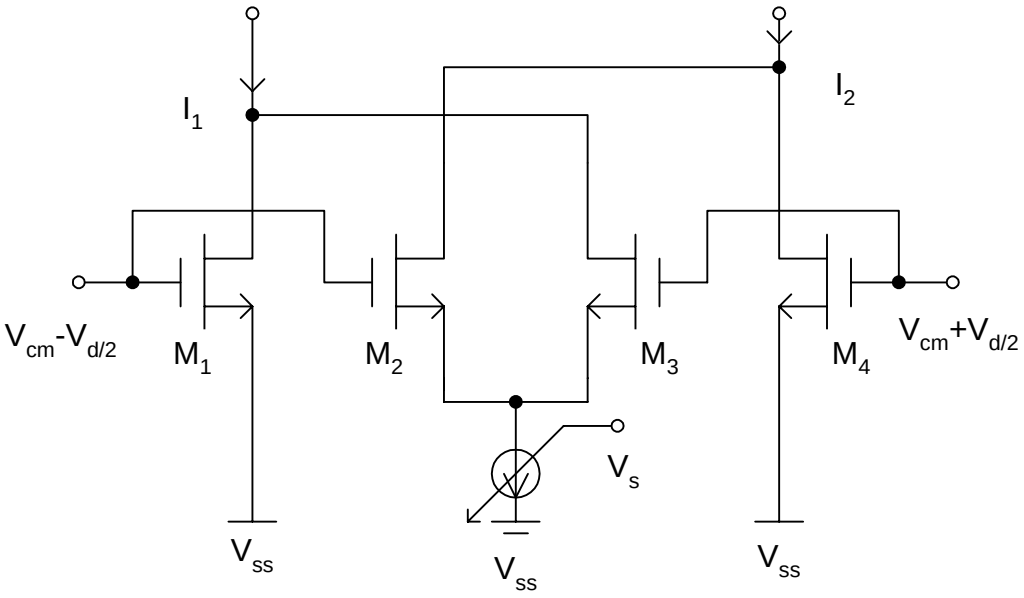

Figure 2.4 Principle of a Cross-Coupled Differential Pair OTA

2.2.3 Differential Pair with Stable Common Mode Signal

In this circuit structure [17] as shown in Figure 2.5, the input voltage V_d with a variable common mode range is to the input of two identical transistors M_1 and M_2 as a fixed common mode voltage.

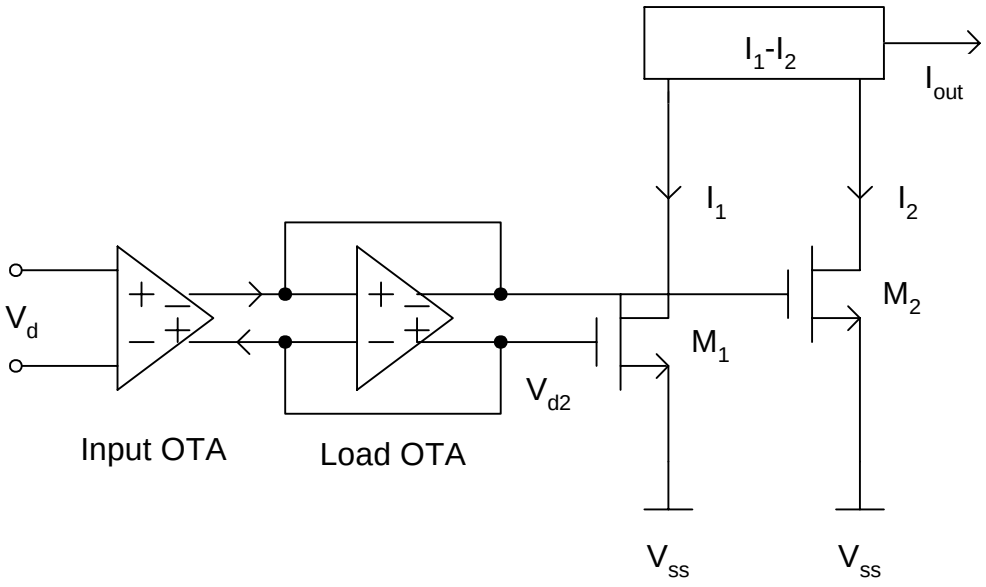

Figure 2.5 Differential Pair with Stabilized Input Common Mode Signal

The output current can be shown as

$$I_{out} = 2\beta(V_{GS} - V_t)V_d \tag{2-8}$$

In this structure, the first order input-output characteristic is linear; however, mobility reduction and channel length modulation decrease the linearity.

2.2.4 Regulated Cascode Differential Pair

Contrary to the circuits mentioned above, the input transistors M_1, M_2 in Figure 2.6 are working in the triode region [16,18]. The control voltage V_s can be adjusted to make the input transistors work in the triode region. The drain voltage is constant due to amplifiers A_1, A_2 and the cascode transistors M_3, M_4. The input-output characteristics are linear and can be expressed by

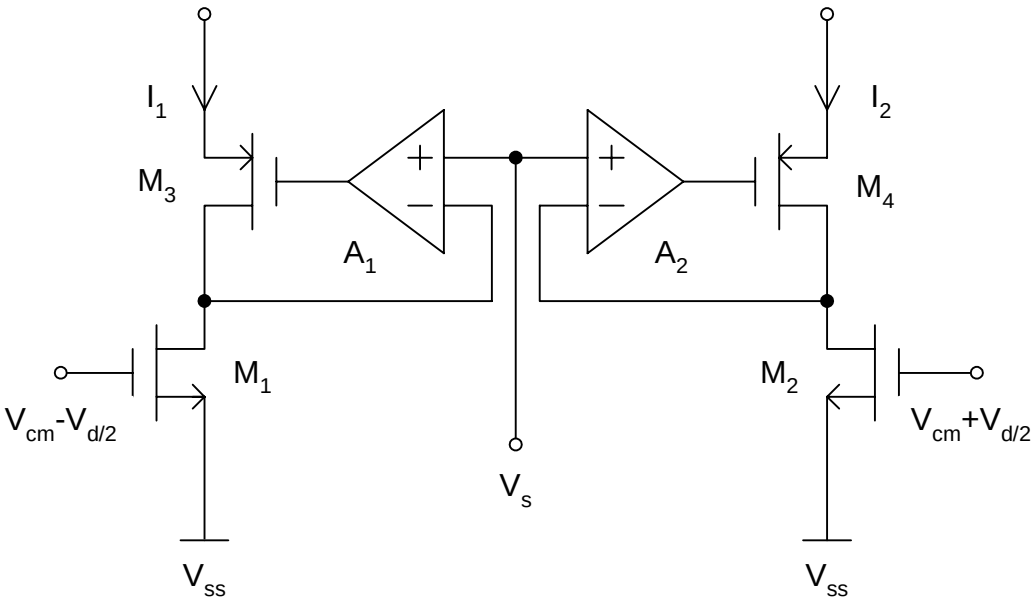

Figure 2.6 Regulated Cascode Differential Pair

$$\Delta I = \frac{W}{L}\beta V_s V_d \tag{2-9}$$

The input common-mode range is limited by the fact the input transistors should stay in the triode region. The linearity is influenced by the mobility reduction, which

also changes the transconductance stability. If the gain of the cascode stage is high enough, the mismatch between the drain-source voltage and V_s can be neglected.

2.2.5 Linear OTAs' Structure Comparison

Table 2-1 Comparison of Four Different Linear OTA Structures

Linear OTA Structure	Linearity	Sensitivity to V_{cm} variation
Tunable Biased Source-Coupled Input Pair	Medium	Low
Cross-Coupled Differential Pair	High	High
Stabilized Input Common Mode Signal	Medium	Very Low
Regulated Cascode Differential Pair	Very High	High

From the four studied linear transconductor structures shown in Table 2-1, we choose the regulated cascade differential pair structure to design the linearly tunable OTA.

2.3. Linearly Tunable OTA

OTA can be carried out with a double or a single ended output. We design fully differential OTA according to be having symmetric internal signal paths. Fully differential OTA will reduce second order harmonic distortion.

2.3.1 Input Transistors with Constant V_{ds}

Drain current of a transistor biased in the triode region can be expressed by

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{tn})V_{ds} - \frac{V_{ds}^{\ 2}}{2}\right] \tag{2-10}$$

Fully differential circuit structures can be used to cancel even-order harmonics. The OTA schematic is shown in Figure 2.7. M_1 and M_2 are working in the triode region and their drain-source voltages are set equal to V_c through the use of M_3, M_4, and the two extra amplifiers A_1 and A_2. The differential input signal V_i is applied to the gate of M_1, and M_2, and is superimposed on a constant common-mode voltage V_{cm}. The drain current of Q_1 can be shown as

$$i_{D1} = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[\left(\frac{V_i}{2} + V_{cm} - V_{tn}\right)V_{ds} - \frac{V_{ds}^{\ 2}}{2}\right] \tag{2-11}$$

Current i_{o1} is the difference between i_{D1} and I_1, which is expressed as

$$I_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[(V_{cm} - V_{tn})V_{ds} - \frac{V_{ds}^{\ 2}}{2}\right] \tag{2-12}$$

$$i_{o1} = i_{D1} - I_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(\frac{V_i}{2}\right)V_{ds} \tag{2-13}$$

This results in

$$G_m = \mu_n C_{ox} \left(\frac{W}{L} \right)_1 V_{ds} \tag{2-14}$$

This formula shows that the transconductance is linearly proportional to M_1 drain-source voltage.

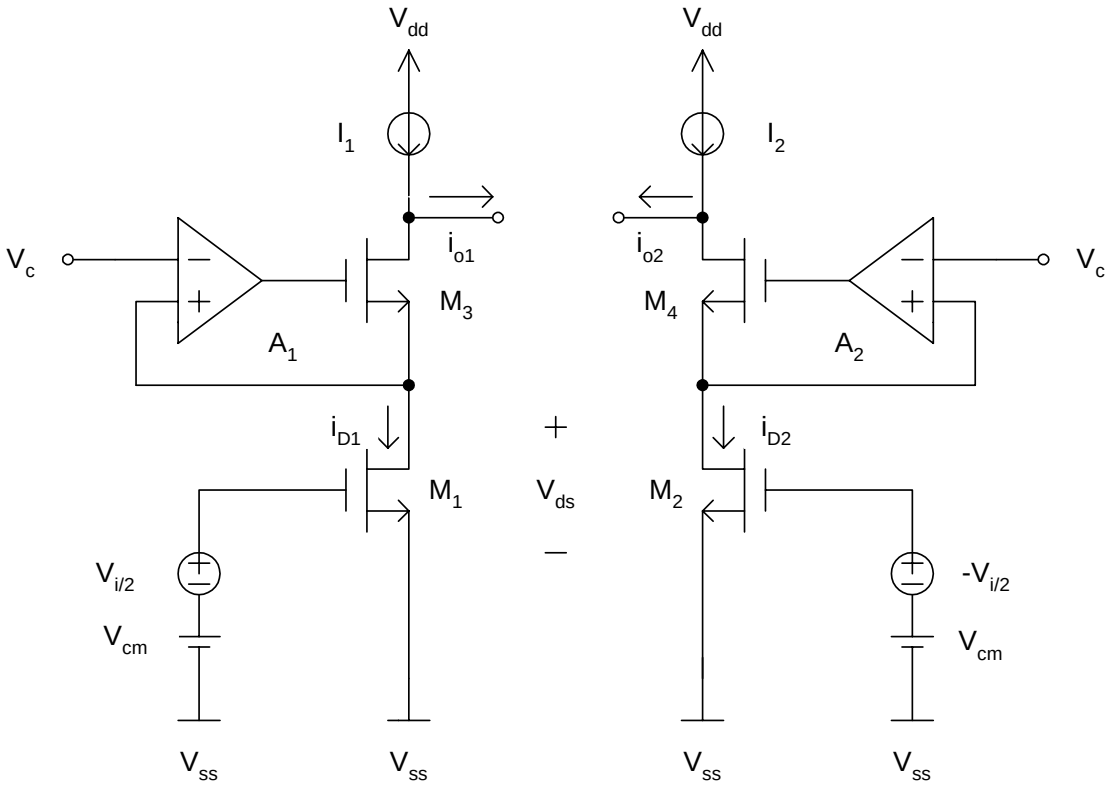

Figure 2.7 Regulated Cascode OTA Schematic

2.3.2 Transconductor Design

The schematic of the transconductor is shown in Figure 2.8. Differential input signal is applied to M_{1A} and M_{1B}, which work in the triode region, whereas remaining transistors work in the saturation region.

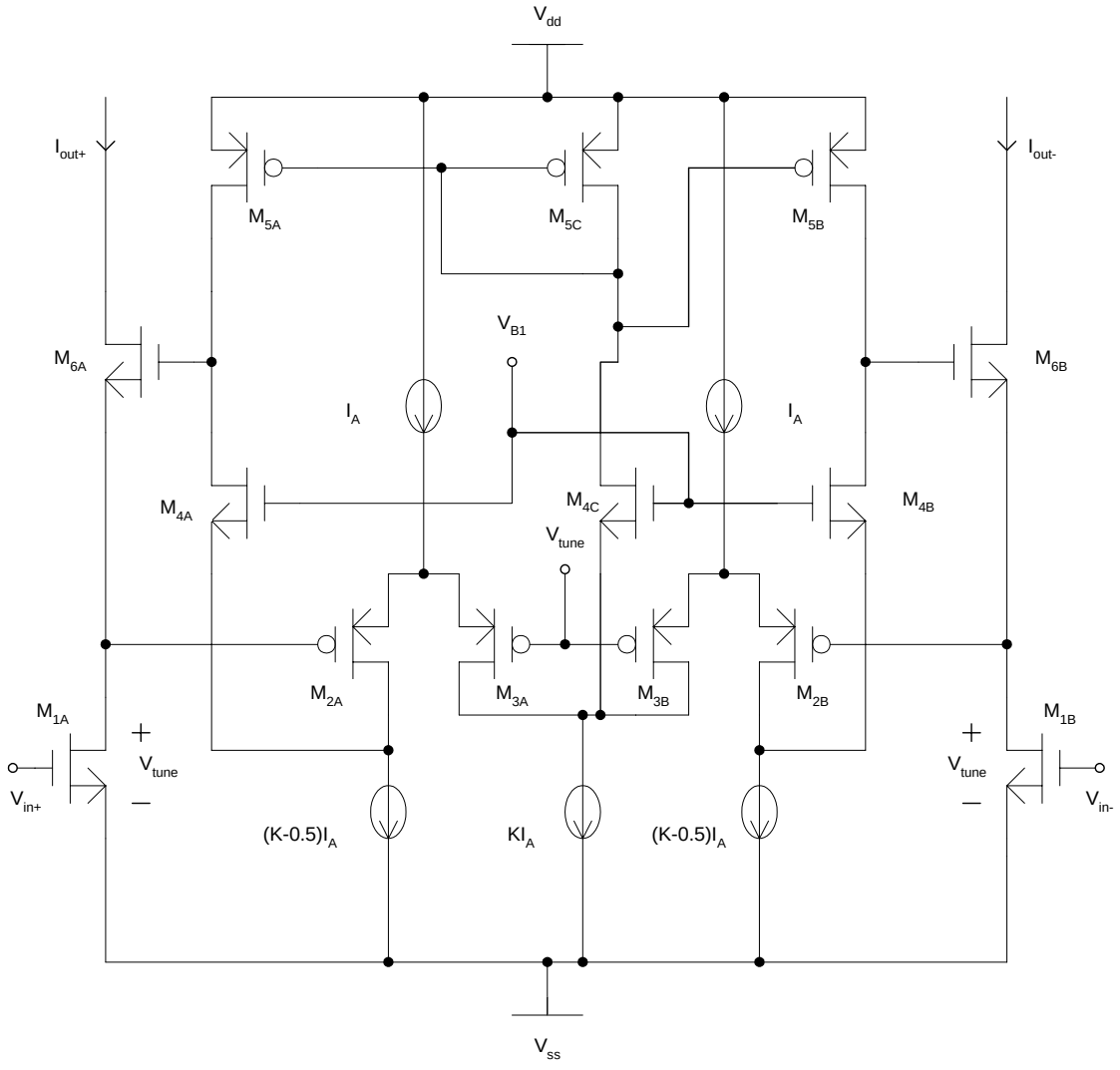

Figure 2.8 Transconductor Schematic

The input transistors M_{1A}, and M_{1B} are working in the triode region. The amplifier feedback loops are composed of M_{2A}, M_{4A}, M_{6A}, M_{2B}, M_{4B} ,and M_{6B}. Transistors M_{2A}, M_{3A}, M_{3B} and M_{2B} are biased with wide-swing current sources, which are I_A, KI_A, and (K-0.5) I_A, where K>1. Assuming these transistors are matched, tail current I_A can be equally separated between M_{2A} and M_{3A} (M_{2B} and M_{3B}). Under this condition, these transistors have identical V_{GS} voltage. As a result, tuning voltage V_{tune} is copied to the drain of M_{1A} (M_{1B}) and the current flowing in M_{4A} (M_{4B}) is (K-1) I_A. Feedback loop amplifiers also enlarge the output impedance and isolate the output nodes from the input transistors' low impedance drain nodes. Owing to V_{GS} drop voltage is not stacked between the power sources; this structure is also suited for low voltage design. The relationship between drain current and input voltage [19] can be expressed as

$$I_{ds} = \frac{W_1}{L_1}\mu_n C_{ox} V_{tune}[(V_{in} - V_{th}) - \frac{p}{2}V_{tune}] \qquad (2\text{-}15)$$

where $P= 1+\left(\frac{\partial V_{th}}{\partial V_{BS}}\right) = 1+\left(\frac{\gamma}{2(2\phi_F + V_{BS})^{\frac{1}{2}}}\right)$ and $\gamma = \sqrt{2q\varepsilon_{si}N_{sub}}/C_{ox}$ is called body effect coefficient, V_{BS} is the source-bulk potential difference [20], and ϕ_F is the work function. Input voltage V_{in} is the applied ac signal v_{in} added to a common-mode voltage V_{cm}. The differential mode transconductance can be expressed by

$$g_m = g_{m1A} = g_{m1B} = \frac{\partial I_{out}}{\partial V_{in}} = \frac{W_1}{L_1}\mu_n C_{ox} V_{tune} \tag{2-16}$$

In this circuit structure, the output resistance seen from the drain of M_{6A} (M_{6B}) can be expressed by

$$r_{out} \cong \frac{g_{m2}}{g_{ds5}} \frac{g_{m6}}{g_{ds6}} \frac{1}{g_{ds1}} \tag{2-17}$$

where g_{dsi} is the conductance of the transistor i. If we keep M_{2A} in saturation, the voltage V_{B1} should satisfy the following requirement

$$V_{th4} + V_{dsat4A} + V_{compI_A} \le V_{B1} \le V_{tune} + |V_{th2}| + V_{th4} + V_{dsat4A} \tag{2-18}$$

V_{compI_A} is the compliance voltage of current source I_A and V_{dsat4A} is the drain source saturation voltage of M_{4A}.

2.3.3 Transconductor Frequency Response

The feedback loop built in the transconductor should be checked its stability. The frequency response can be analyzed by using the half circuit of this transconductor. Figure 2.9 shows half circuit of the transconductor.

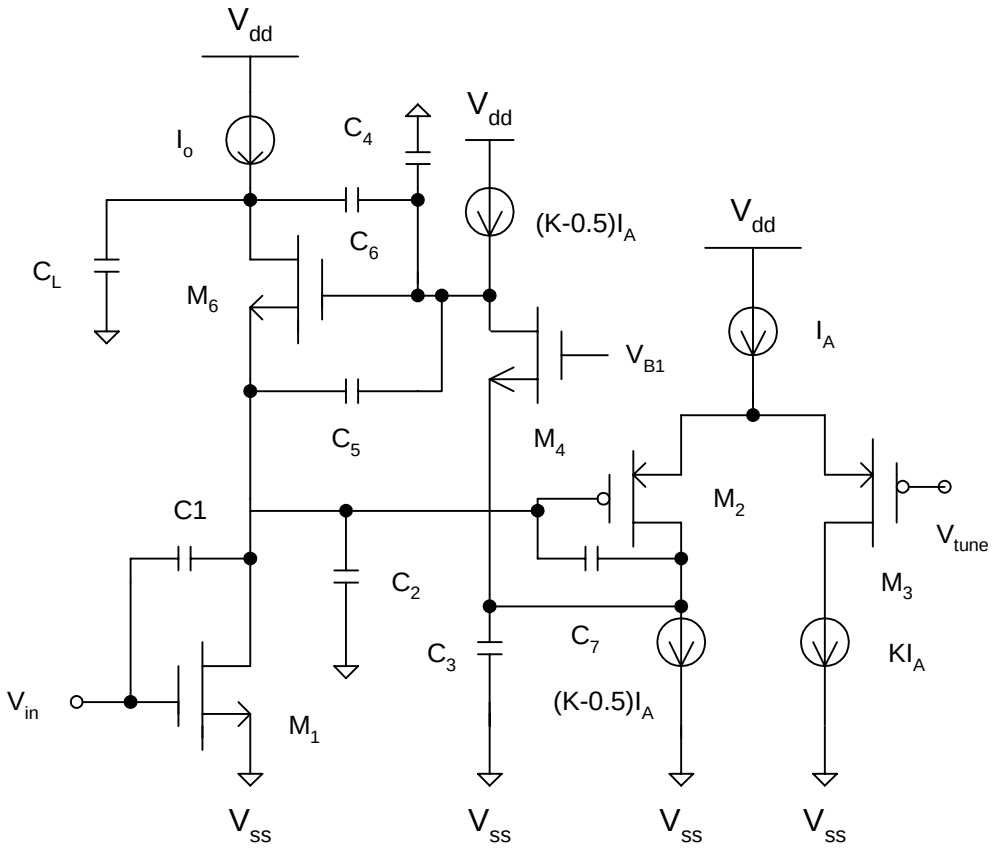

Figure 2.9 Transconductor Half Circuit

The analysis is based on the small signal first order behavior where the feedback loop gain can be expressed as $A_v \cong g_{m2} / g_{ds6}$. The transition frequency is $\omega_t = g_{m2} /(C_4 + C_5 + C_6)$. The non-dominant pole is g_{m4} / C_3. The non-dominant pole can be pushed far away from the transition frequency by reducing C_3 or increasing the current factor *K*. Assuming the non-dominant pole is pushed far away from the transition frequency, a simple analysis shows that the dominant pole is

$$p_1 = \frac{-1}{\frac{1}{g_{ds1}}\frac{g_{m2}}{g_{ds5}}\frac{g_{m6}}{g_{ds6}}C_L} = -\frac{1}{r_{out}C_L} \tag{2-19}$$

The dominant pole and non-dominant pole are all in the left hand plane (LHP) so that the transconductor can be guaranteed stable. The large gate to drain capacitance C_1 in the input transistor causes the zero in lower frequency range. Reducing input transistor length will push the zero into higher frequency and increasing I_A will reduce the integrator phase error.

2.3.4 Adaptive-Bias Common Mode Feedback Loop

There are two general methods to design CMFB circuits: the continuous time approach and the switched-capacitor approach. In switched-capacitor CMFB design, this kind of structure can introduce some glitches. Therefore, we design CMFB circuit using continuous time approach. When designing CMFB circuits, consideration should be given to stability. If CMFB is not well designed, its common mode signal can cause circuits to become unstable. Although many transconductors designed with CMFB circuit claimed to meet the stability and high linearity requirements [21], the dependence of the processed signal common mode voltage on their tuning mechanism may severely degrade the filter performance. Several published circuit structures basically intended to reduce common mode voltage fluctuation in balanced amplifiers [22-24]. These amplifiers are chosen to stabilize common mode voltage when the transconductor is in the tuning process. We use an adaptive-biased CMFB circuit [25] to cancel the

deviations of the common mode voltage during transconductor tuning through sending adaptive current to the transconductor load. Common mode voltage should be fixed when the circuit is in the tuning process. The signal swing will be limited when the common mode voltage is changing. Using the adaptive bias CMFB circuit can keep the common mode voltage stable. The block diagram of the adaptive-biasd CMFB is shown in Figure 2.10.

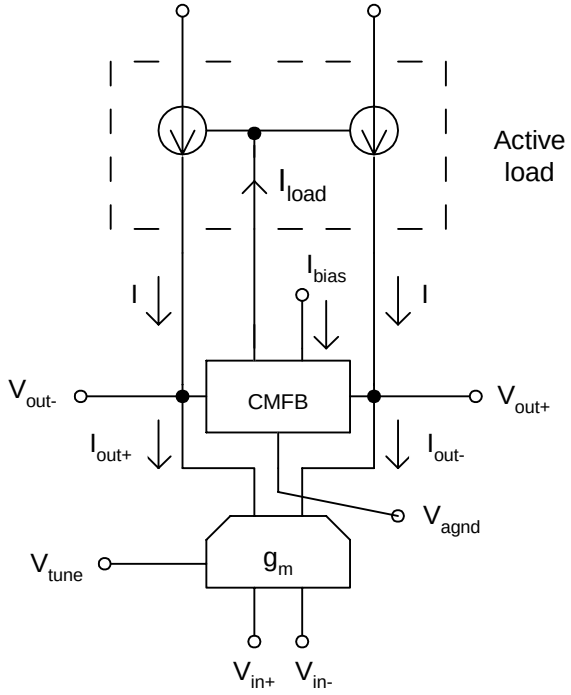

Figure 2.10. The Block Diagram of Adaptive-Biased CMFB

As shown in Figure 2.10, the OTA consists of a transconductor, active load and CMFB. Detailed circuit implementation is shown in Figure 2.11. The CMFB loop

amplifies the voltage difference between $\frac{1}{2}(V^{+}_{out} + V^{-}_{out})$ and V_{agnd} and delivers the adaptive current

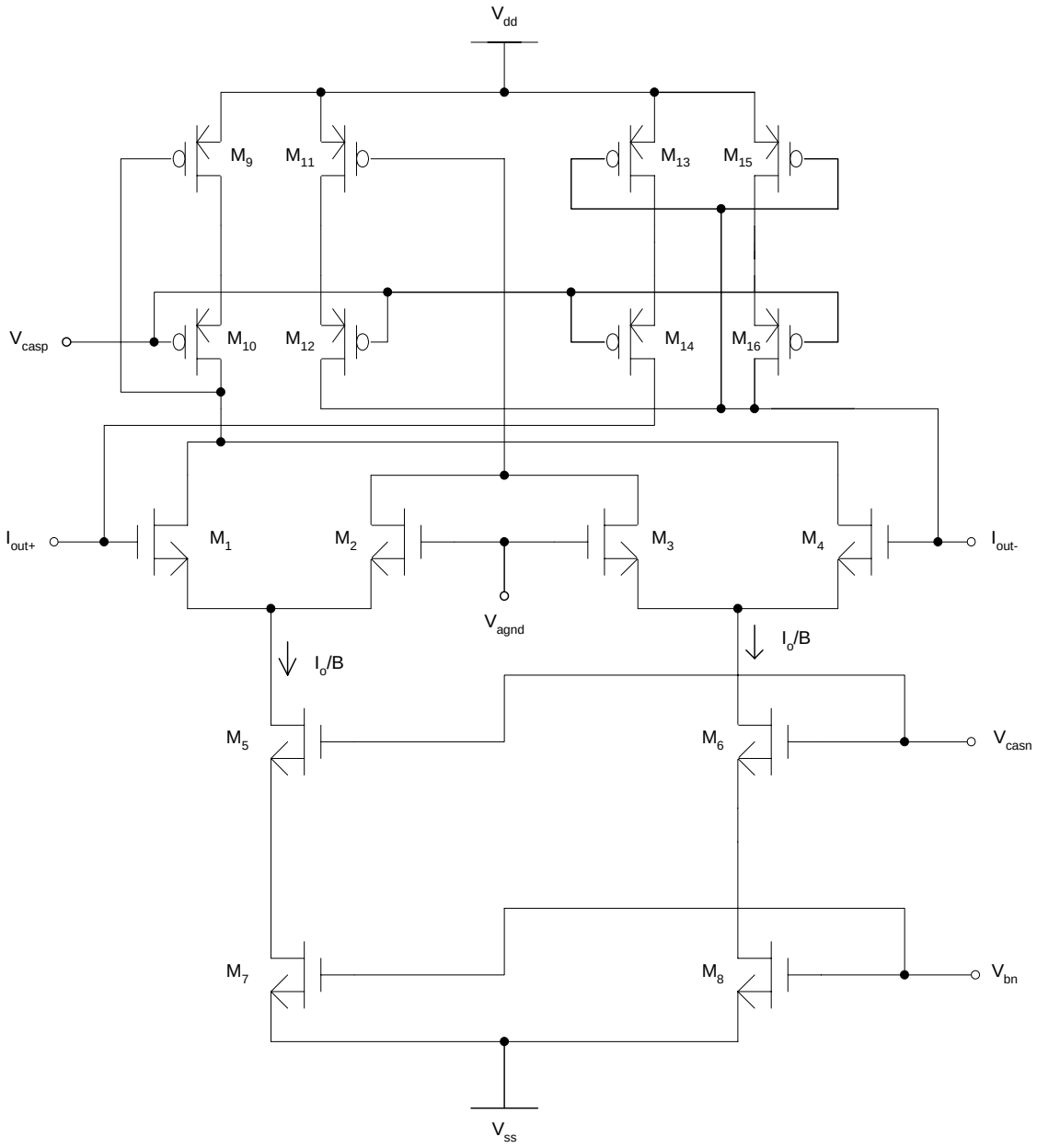

Figure 2.11 Common Mode Feedback Circuit of the OTA

I_o to keep $V_{cm} = V_{agnd}$ where V_{cm} is the common mode voltage of the OTA shown in Figure 2.7. The CMFB circuit is composed of an error amplifier (M_1-M_4) with tail current $I_{Bias} = I_o / B$, where B is the current division ratio. Transistors (M_5-M_8) provide the bias current. P-type current sources (M_9-M_{16}) are the load of the error amplifier (M_1-M_4). V_{casn} and V_{casp} are adjusted to minimize the voltage compliance to $2V_{dsat}$. The objective of reducing tail current ratio from I_o to I_o / B is to decrease power consumption of the current-mirror devices. The ratio B is limited by the minimum required unit-gain frequency of the CMFB circuit. If we define A_{CM} and A_{CMF} as the transconductor open loop and close loop (connected with CMFB) gain and CML_{gain} as the CMFB loop gain, we can get

$$A_{CMF} = \frac{V_{out^+}}{V_{in^+}} = \frac{V_{out^-}}{V_{in^-}} = \frac{A_{CM}}{1 + CML_{gain}} \tag{2-20}$$

In general, differential mode gain is expressed by A_{DM} and we get common mode rejection ratio (CMRR) equals to

$$CMRR = \frac{A_{DM}}{A_{CMF}} \cong CML_{gain} \tag{2-21}$$

Common mode loop gain can be increased to improve the common mode rejection ratio. However, if the common mode loop gain is less than expected, it will introduce higher distortion [26].

2.3.5 Large-Signal Distortion

The input transistor pairs working in the triode region shows improvement of linear range compared to the circuit structures mentioned in Table 2-1. However, second order effects still need to be investigated in order to improve linearity. For instance, mobility-dependence on channel vertical-field is

$$\mu_n = \mu_{no} / \left[1 + \theta (V_{GS} - V_{th})\right] \tag{2-22}$$

where μ_{no} is the low-field mobility and θ is a process parameter. If we only take the first term in Taylor's expression, the transconductor large-signal output current can be expressed by

$$I_{out} = I^{+}{}_{out} - I^{-}{}_{out} = \frac{W_1}{L_1} \mu_{no} C_{ox} V_{tune} \left[1 - 2\theta \left(V_{AGND} - V_{th} - \frac{nV_{tune}}{4} \right)\right] v_{in} \tag{2-23}$$

where g_m is reduced by the factor $\left[1 - 2\theta \left(V_{AGND} - V_{TH1} - \frac{nV_{TUNE}}{4} \right)\right]$. Nonlinearity is influenced by mobility, active load, and nonlinear parasitic capacitances [27]. In

adaptive bias CMFB design, common mode output voltage V_o with a differential input V_s can be shown as [26]

$$V_o = \alpha_1 V_{SCM} + \alpha_2 V_{SDM} + \alpha_3 V^2{}_{SDM} \tag{2-24}$$

where $\alpha_3 V^2{}_{SDM}$ is caused by the MOSFET nonlinear characteristic, $\alpha_2 V_{SDM}$ is the mismatch term caused by common mode sensing circuit and $\alpha_1 V_{SCM}$ is the output common mode voltage. Increasing common mode loop gain will reduce α_3 and increase linearity. In Figure 2.11, common loop gain can be expressed by

$$CML_{gain} = I_o \left(\frac{g_m}{I_{DS4}} \right)_{M4} R_{OUT} \tag{2-25}$$

where R_{OUT} is the transconductator output resistance, which is proportional to transistors' channel length modulation. The high value of CML_{gain} can be attained by increasing $\left(\frac{g_m}{I_D} \right)$ of input transistors M_1 to M_4 of Figure 2.11. Second and third harmonic distortions induced by nonlinear device in the CMFB loop are shown as

$$HD_2 = \frac{1}{2} K_r \frac{\alpha_3}{CML_{gain}} v_i \tag{2-26}$$

$$HD_3 = \frac{1}{2}\left(K_r \frac{\alpha_3}{CML_{gain}} v_i \right)^2 = 2HD_2{}^2 \qquad (2\text{-}27)$$

If V_i=1, K_r is a constant and can usually be considered as unity. If CML_{gain} is large enough, the total harmonic distortion (THD) can be reduced.

2.3.6 Adaptive Bias Current Generator

The adaptive bias circuit structure is shown in Figure 2.12. This circuit stabilizes the common mode voltage while g_m is being changed. Adaptive bias generator also increases the common mode loop gain and CMRR.

2.3.7 Noise Analysis

From Table 2-1, we can see that the regulated cascode transconductor has better linearity in deep triode region. But its low drain voltage will degrade the noise characteristics. Half circuit of the transconductor is being analyzed.

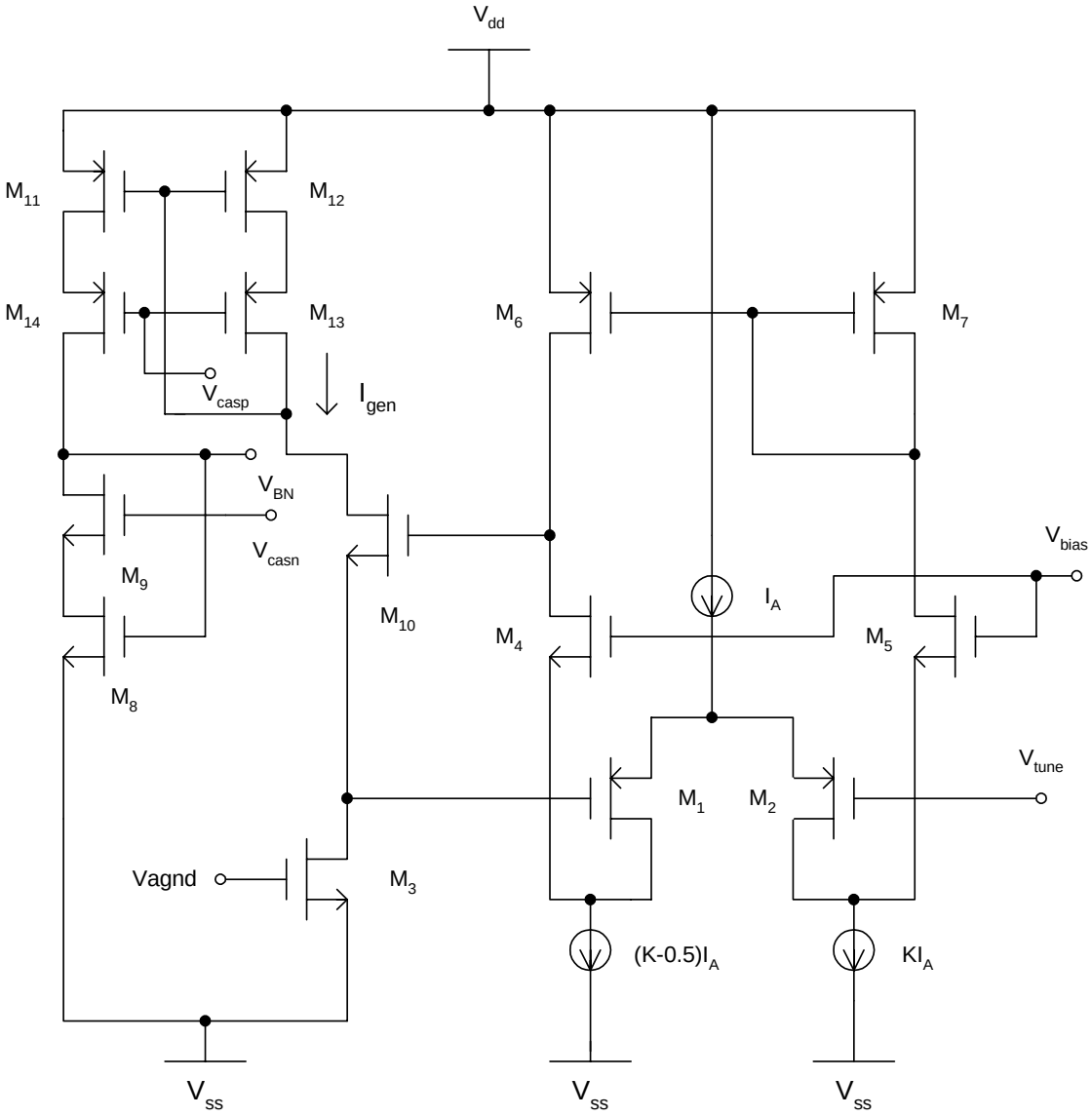

Figure 2.12 Adaptive Bias Current Generator

The half circuit of this transconductor is shown in Figure 2.13. The overall transconductance is shown as

$$G_m = g_{m1}\frac{g_{m5}}{g_{o5}} \tag{2-28}$$

where g_{o5} is the overall conductance at the output node. The thermal noise power spectral density (PSD) S_N of a single transistor referred to the drain can be defined by

$$S_N = 4KTG_N \tag{2-29}$$

where G_N is the thermal noise conductance, which is proportional to the source transconductance

$$G_N = \eta g_{ms} \tag{2-30}$$

The device noise parameter η depends on bias condition [28]. The thermal noise conductance G_N evaluated at the output of transconductor in Figure 2.13 is derived by

$$G_N = \left(\frac{g_{m5}}{g_{o5}}\right)^2\left[\eta_1 g_{ms1} + \eta_2\left(\frac{g_{md1}}{g_{ms2}}\right)^2 g_{ms2} + \eta_3 g_{ms3} + \eta_5\left(1+\frac{g_{md1}}{g_{ms5}}\right)^2 g_{ms5}\right] \tag{2-31}$$

The excess noise factor (Γ) of the overall transconductor can be obtained by dividing (2-31) with $\eta_1 g_{ms1}$

$$\Gamma \cong \frac{\eta_1 n_1}{1-\frac{g_{md1}}{g_{ms1}}}\left[1+\frac{\eta_2}{\eta_1}\frac{g_{ms1}}{g_{ms2}}\left(\frac{g_{md1}}{g_{ms1}}\right)^2+\frac{\eta_3}{\eta_1}\frac{g_{ms3}}{g_{ms1}}+\frac{\eta_5}{\eta_1}\frac{g_{ms5}}{g_{ms1}}\left(1+\frac{g_{md1}}{g_{ms5}}\right)^2\right] \qquad (2\text{-}32)$$

where n_1 is the sloping factor of the transistor M_1 which is biased in triode region. η_1 is approximately equal to 1. Other transistors except M_1 are biased in strong inversion. Equation (2-32) is further becomed to

$$\Gamma \cong \frac{\eta_1 n_1}{1-\frac{g_{md1}}{g_{ms1}}}\left[1+\frac{2}{3}\frac{g_{ms1}}{g_{ms2}}\left(\frac{g_{md1}}{g_{ms1}}\right)^2+\frac{2}{3}\frac{g_{ms3}}{g_{ms1}}+\frac{2}{3}\frac{g_{ms5}}{g_{ms1}}\left(1+\frac{g_{md1}}{g_{ms5}}\right)^2\right] \qquad (2\text{-}33)$$

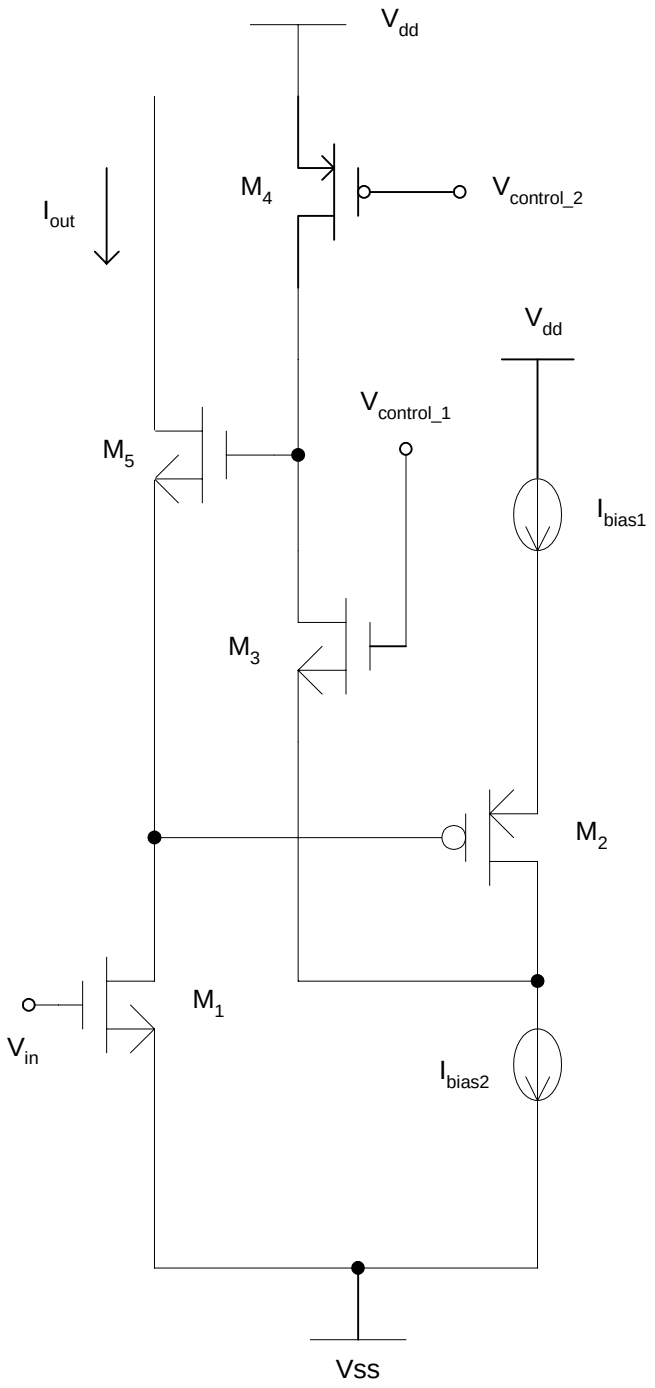

Figure 2.13 Regulated Cascode Half Circuit

2.4 Linearly Tunable Filter Design

Based on the OTA described in the previous section, a second order g_m-C filter is built as shown in Figure 2.14. Positive and negative conductance cells (g_{m2} and g_{m5}, respectively) are added to control the Q factor of the filter. Because the g_m cells are linearly controllable, the filter's center frequency and Q factor will also be linearly tunable.

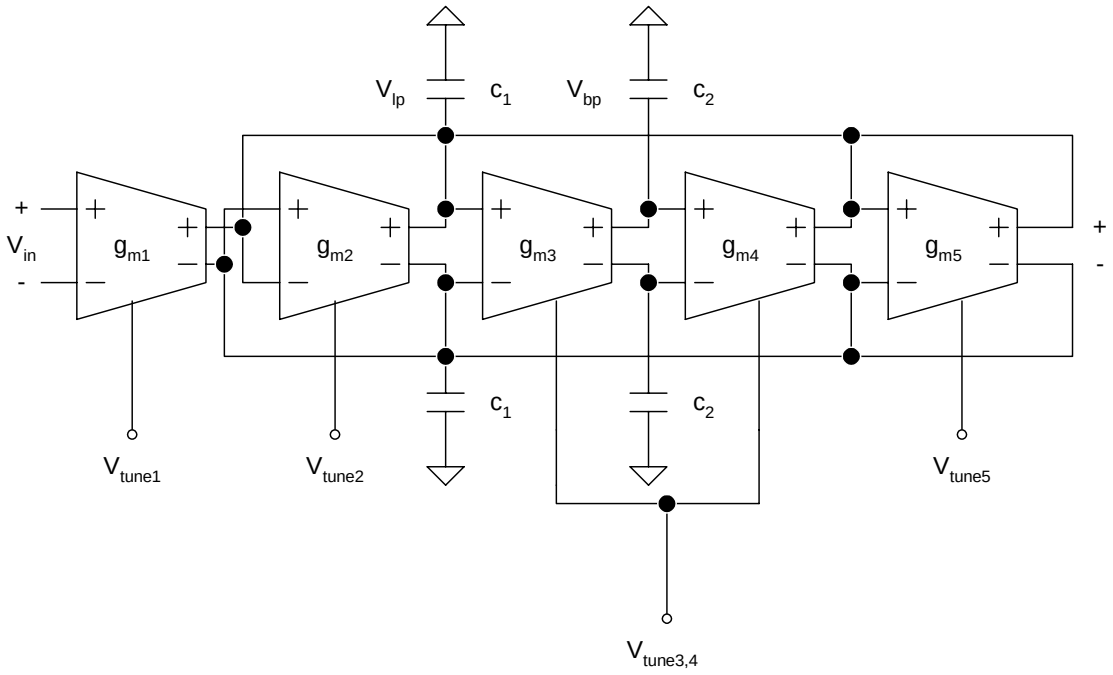

Figure 2.14 g_m-C Filter Structure Composed of Linearly Controllable g_m Cells

Transfer function of the bandpass filter in Figure 2.14 can be found as

$$H(s) = \frac{Ks}{s^2 + \frac{\omega_o}{Q} s + \omega_o{}^2} \tag{2-34}$$

where

$$K = \frac{g_{m_1}}{C_1} \tag{2-35}$$

$$\omega_0 = \sqrt{\frac{g_{m_3} g_{m_4}}{C_1 C_2}} \tag{2-36}$$

$$Q = \sqrt{\frac{g_{m_3} g_{m_4} C_1}{C_2}} \frac{1}{(g_{m_2} - g_{m_5})} \tag{2-37}$$

$$g_{m_1} = K_1 V_{tune1} \tag{2-38}$$

$$g_{m_2} = K_2 V_{tune2} \tag{2-39}$$

$$g_{m_3} = g_{m_4} = K_{3,4} V_{tune_{3,4}} \tag{2-40}$$

$$g_{m_5} = K_5 V_{tune_5} \tag{2-41}$$

$$K_i = \mu_n C_{ox} \frac{W_i}{L_i} \tag{2-42}$$

The center frequency (ω_0) and Q can be found

$$\omega_0 = \sqrt{\frac{g_{m3} g_{m4}}{C_1 C_2}} = \frac{K_{3,4} V_{tune_{3,4}}}{\sqrt{C_1 C_2}} \tag{2-43}$$

$$Q = K_{3.4} V_{tune_{3,4}} \sqrt{\frac{C_1}{C_2}} \frac{1}{(K_2 V_{tune_2} - K_5 V_{tune_5})} \tag{2-44}$$

The filter gain at ω_0 is equal to

$$H(s)\Big|_{s=j\omega_0} = \frac{\frac{g_{m_1}}{C_1}\omega_0}{{\omega_0}^2 + \frac{(g_{m_2} - g_{m_5})\omega_0}{C_1} + \frac{g_{m_3} g_{m_4}}{C_1 C_2}} \tag{2-45}$$

From equations (2-43) and (2-44), the filter gain and Q factor can be tuned linearly and independently. The filter gain at center frequency (ω_0) can be varied while keeping Q constant. The center frequency can be adjusted by changing $g_{m3,\,4}$ and $C_{1,\,2}$ in Figure 2.14. If all the g_m cells and capacitances are equal, then the gain of this biquad is equal to its Q value. This assumption will no longer hold when the parasitic capacitances and

mismatch exist. In order to get the accurate frequency response, automatic frequency and Q factor tuning circuits are required.

CHAPTER III

PROPOSED TUNING METHOD FOR LINEARLY TUNABLE FILTER

3.1 Existing Tuning Methods

3.1.1 Pre-Tuning Method

Pre-tuning technique [29, 30] tunes the filter before processing the main signal. During the specific tuning time, control signals are stored in an EPROM and tuning circuits are removed. The filter itself acts as a tuned circuit, which has the advantage of not using extra circuits to match the filter. The shortcoming is the necessity of the on-chip EPROM with some analog-to-digital and digital-to-analog converter circuits occupying large chip areas. If the environment conditions change during the signal processing period, the filter cannot be tuned again.

3.1.2 Burst Tuning Method

This tuning method [31] is similar to pre-tuning scheme and is composed of two time periods: one is the tuning time period and the other is the processing time period. The circuit itself is switched between two periods. The advantage is that there is no need to have another filter so matching problems are avoided. The disadvantage is faced when the signal is being processed; the circuit performance will be affected by tuning. The burst tuning technique provides periodic tuning.

3.2. Master-Slave Scheme

In this method [32, 33], the master filter is tuned using an external reference source and the generated tuning signal is applied to both the master and the slave filters. The master filter is matched to the slave filter such that the master filter models the slave filter's circuit characteristics [19]. The drawback of this circuit structure is that any mismatch between master and slave filters results in tuning errors. However, the advantage of this structure is that it allows continuous signal processing and tuning. Figure 3.1 shows the block diagram of the master-slave technique.

The master filter and an exact copy of it (slave filter) occupy double chip areas. Tuning of cascaded biquad filters use only one master block to adjust all the biquads.

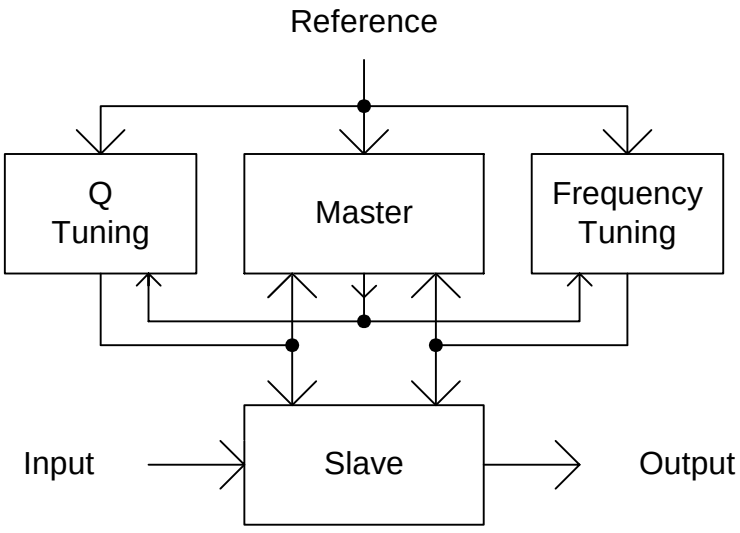

Figure 3.1. Master-Slave Tuning Scheme

3.2.1 Frequency Tuning

There are several different tuning schemes to tune the center frequency and quality factor. Several center frequency-tuning methods are used such as Phase Locked Loop using Voltage Control Filter [34], Phase Locked Loop using Voltage Controlled Oscillator [35], Direct Sample Tuning [14] ,and Charge Detection [15].

1. PLL Tuning Methods with Voltage Controlled Filter

The basic idea of this frequency tuning method [34] is using Phased Locked Loop (PLL) with a second-order voltage-controlled filter (VCF) to tune the center frequency. The general block diagram is shown in Figure 3.2.

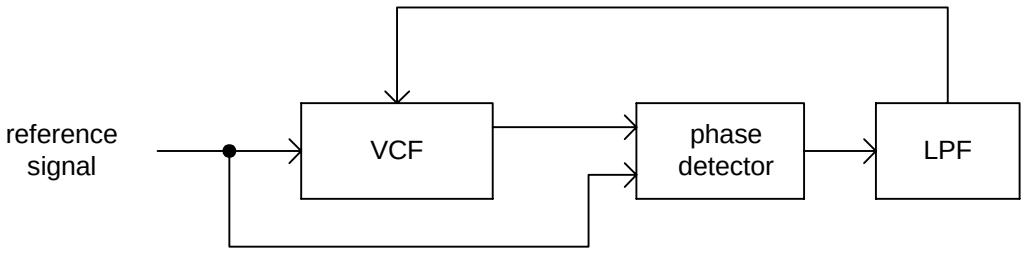

Figure 3.2 Phase Locked Loop with Voltage-Controlled Filter (VCF)

In Figure 3.2, the reference signal with a specific frequency is applied to the voltage controlled filter (VCF), if the lowpass output is used, then the reference signal and the output has 90^0 phase difference. The PLL loop can track the two signals' phase difference until a 90^0 phase difference is attained. The phase detector can be either an

analog multiplier or an XOR gate. When the two signals have 90^0 phase difference, the output of the phase detector will have zero time average. However, if an XOR gate is used as a phase detector, both the reference signal and the filter output should pass through comparator in order to get digital waveform. Under this condition, the offset of the comparator will cause frequency-tuning error. Approximate calculation results [22] show that when the offset error is 2^0 in the phase detector, the tuning error will be around 1%.

2. Tuning Methods with Voltage Controlled Oscillator

PLL frequency tuning with voltage controlled oscillator (VCO) can be shown in Figure 3.3. The phase detector compares the reference frequency with output signal frequency of the VCO. This method [35] is not affected by phase offset of the detector. However, implementation of VCO [36] causes matching problems to the filter to be tuned. VCO is designed by the same biquadratic filter in positive feedback configuration.

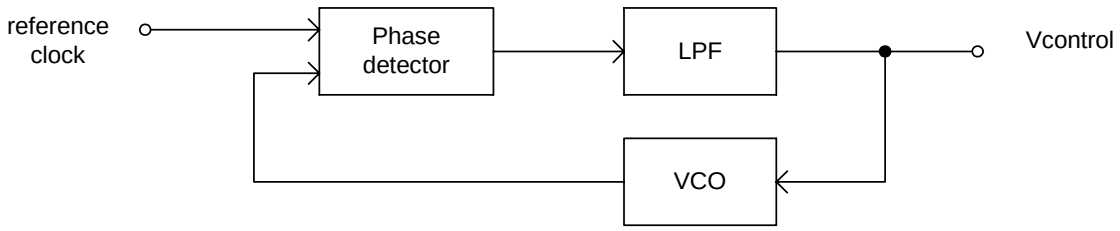

Figure 3.3 Phase Locked Loop with Voltage-Controlled Oscillator

3. Direct Sample Tuning

This method uses the master-slave tuning technique. The MOSFET-C filter acts as the slave filter and the tuning scheme adjusts the time constant of one integrator rather than the entire filter, which reduces the chip area [14]. The tuning circuit can be shown in Figure 3.4

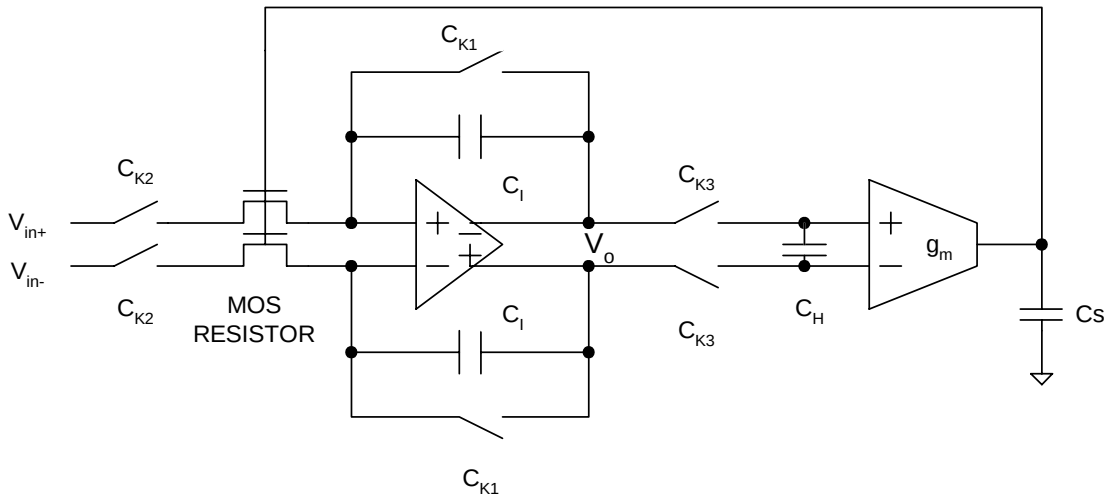

Figure 3.4 Direct Sample Tuning Technique

The whole tuning process can be divided into three stages: C_{K1}, C_{K2}, and C_{K3} time periods. In the C_{K1} period, the charge on the integration capacitor C_I is cleared and V_o is zero. In the C_{K2} timing phase, differential voltage charges the integration capacitor and causes the ramp voltage shown on V_o. In the last period of C_{K3}, the charge stored on C_I is transferred to C_H and the error charges are stored on C_s. When steady state is reached, the error between the differential voltage V_o and the voltage stored on C_H is zero. The major tuning error is caused by the operational amplifier (opamp) in the integrator [37].

4. Charge Detection

This tuning scheme [15] uses two nonlinked control loops.These loops are operated at a lower frequency than the filter's center frequency.The basic idea of this tuning scheme is shown below.

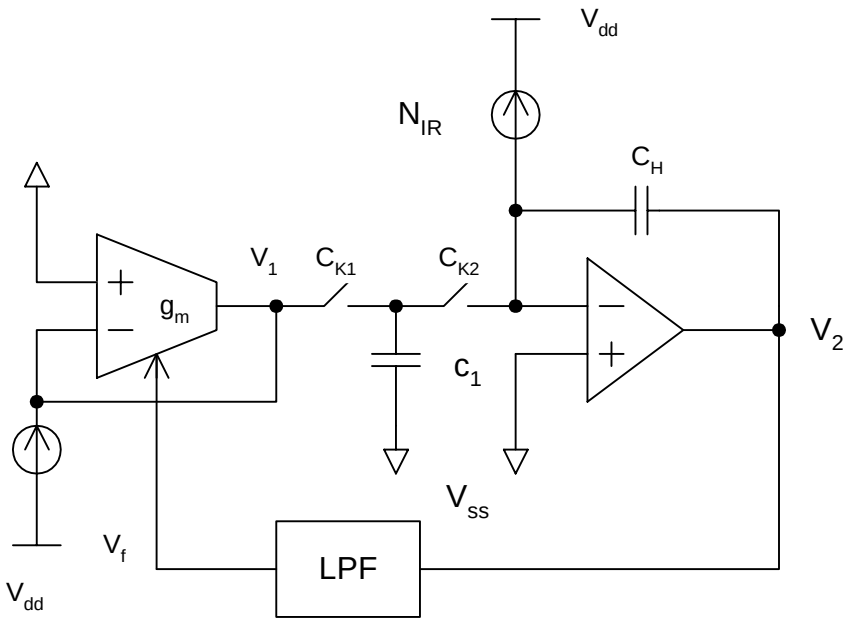

Figure 3.5 Charge Detection Tuning Diagram

In Figure 3.5, C_{k1} and C_{k2} are two non-overlapping clocks with period T and the charge transferring equation can be shown as [15]

$$C_H V_2(t) = (t - t_o) N I_R - (C_1 V_{C1}(t_0))_{Ck2} + C_H V_2(t_0) \tag{3-1}$$

The tuning loop will reach steady state and the steady-state equation is shown as

$$\frac{g_m}{C_1} = \frac{1}{NT} = \frac{f_{clock}}{N} \tag{3-2}$$

The time constant $\frac{C_1}{g_m}$ can be expressed by current mirror ratio N and the period of the clock signal. If the current mirror ratio is accurate, accurate tuning can be achieved.

3.2.2 Q factor Tuning

There are many techniques to tune the quality factor of the filter such as Magnitude Locked loop [16], Impulse response [15], and Adaptive tuning [17].

1. Magnitude Locked Loop

This Q tuning method assumes that the filter's gain is equal to its Q value [16]. The transfer function of a second order bandpass filter can be shown as

$$H(s) = \frac{\omega_0 s}{s^2 + \frac{\omega_o}{Q} s + \omega_0{}^2} \tag{3-3}$$

When s= $j\omega_0$, the magnitude of the transfer function is equal to Q. In this tuning scheme, the assumption is that filter passband gain equals to its Q value. This assumption will not be exactly true because of parasitics.

2. Impulse Response

In the impulse response method [15] the reference signal is applied to the filter and the output waveform's envelop is for tuning. Another first order reference filter is needed as the reference, which is a switched capacitor circuit and provides very accurate response. The block diagram is shown in Figure 3.6. The first order filter is implemented using switched capacitor topology and the step response is shown as

$$H_{step1}(t) = Ke^{-\omega_1 t} \tag{3-4}$$

$$H_{step2}(t) = \frac{K}{\sqrt{1-\frac{1}{4Q^2}}} e^{-\frac{\omega_2}{2Q}t} \sin\left(\sqrt{1-\frac{1}{4Q^2}}\omega_2 t + \theta\right) \tag{3-5}$$

The first order filter's center frequency is lower than the biquad's center frequency. The tuning loop matches $\frac{\omega_2}{2Q}$ to ω_1, where ω_1 is the first order filter's center frequency and ω_2 is the biquad's center frequency. Shortcoming is that the envelop detector is hard to implement and will give large Q tuning errors.

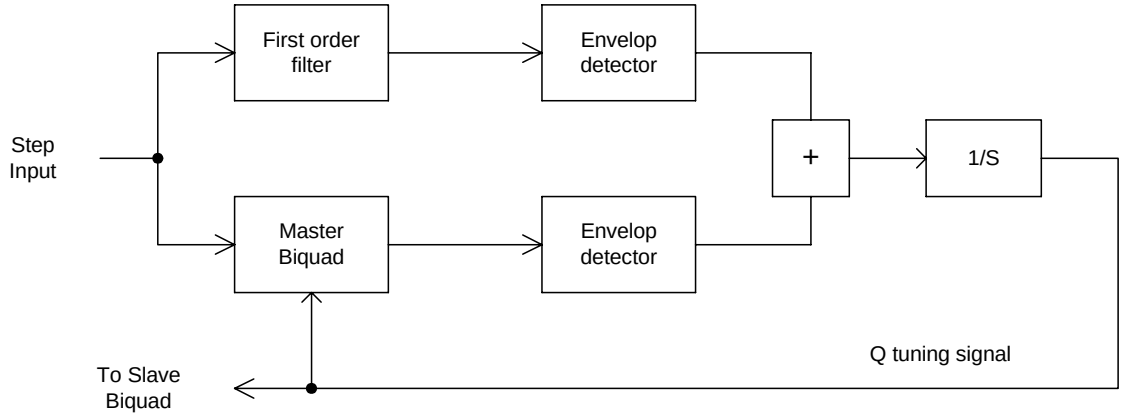

Figure 3.6 Impulse Response Q-Tuning Block Diagram

3. Adaptive Tuning

This method is based on LMS (least mean square) algorithm [38] where the tuning circuit adjusts the output of the master filter to desired value by minimizing mean-square error. The tuning block diagram is shown in Figure 3.7

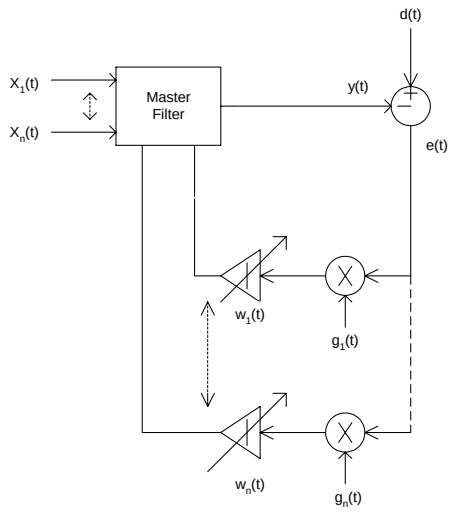

Figure 3.7 Adaptive Tuning Scheme

From Figure 3.7, the tuning equation can be shown as

$$\dot{W}_i(t) = \mu[d(t) - y(t)]g_i(t) \tag{3-6}$$

where $\dot{W}(t) = \frac{dW_i(t)}{dt}$ is the gradient of tuning signal, d (t) is the desired output and y(t) is filter output, and $g_i(t)$ is the gradient of tuning direction. e(t) in Figure 3.7 is the error signal. When the gradient of the tuning signal becomes zero, the tuning process reaches steady state.

3.3 Proposed Tuning Method

In a typical frequency-locked-loop (FLL) tuning system, a reference signal at the desired center frequency (ω_o) is applied to the filter input, and the phase difference between the input and the bandpass output is detected using a phase detector. The phase difference is equal to zero when the frequency control loop becomes stable. The proposed tuning method is based on this fact.

The general second order bandpass filter transfer function can be expressed as

$$H(s) = \frac{Gs\omega_0 / Q}{s^2 + s\omega_0 / Q + \omega_0{}^2} \tag{3-7}$$

The phase response can be found as

$$\angle H(j\omega) = \varphi(\omega) = 90^0 - \tan^{-1}\frac{\omega_0 \omega / Q}{{\omega_0}^2 - \omega^2} \tag{3-8}$$

The input frequency is set to $\omega = \omega_R$. When the output phase is locked to $\phi(\omega_R) = -45^0$, the center frequency is tuned to $\omega_0 = \omega_L$, given by

$$\frac{\omega_L \omega_R / Q}{{\omega_L}^2 - {\omega_R}^2} = -1 \tag{3-9}$$

which yields

$$\omega_L = \omega_R\left(\sqrt{\frac{1}{4Q^2}+1} - \frac{1}{2Q}\right) \tag{3-10}$$

Similarly, when the phase difference is locked to 45^0, the center frequency ω_o will be tuned to ω_H given by

$$\omega_H = \omega_R\left(\sqrt{\frac{1}{4Q^2}+1} + \frac{1}{2Q}\right) \tag{3-11}$$

If the filter has its center frequency (ω_0) as a linear function of its control voltage, i.e., $\omega_0 = G_0 V_C$, then the control voltage corresponding to the tuned center frequency ω_L

will be $V_L = \omega_L / G_0$. Similarly, $V_H = \omega_H / G_0$ will be the control voltage for the tuned center frequency ω_H. The average voltage of V_L and V_H can be calculated as

$$V_F = \frac{V_L + V_H}{2} = \frac{\omega_R}{G_0}\sqrt{\frac{1}{4Q^2} + 1} \tag{3-12}$$

The difference between V_L and V_H can be found as

$$V_H - V_L = \frac{\omega_R}{G_0 Q} \tag{3-13}$$

If Q >>1, the equations 3-12 and 3-13 can be simplified to

$$V_F \approx \frac{\omega_R}{G_0} \tag{3-14}$$

$$Q = \frac{V_F}{V_H - V_L} \tag{3-15}$$

Once V_L and V_H are detected, the average value V_F gives the tuning voltage to set the center frequency to ω_R. When the tuning loop is stable, $(V_H - V_L)$ is equal to V_F / Q_d where Q_d is the desired quality factor.

3.4 Implementation of the proposed tuning scheme

In order to detect the control voltages V_L and V_H, phase difference of the filter should be tuned to -45^0 and 45^0, respectively. We choose the charge pump phase locked loop (PLL) structure to implement this phase difference detection, where the delay of the reference input of the phase detector shown in Figure 3.8 should be set either to -45^0 and 45^0 in alternative cycles. Figure 3.9 shows the entire tuning system.

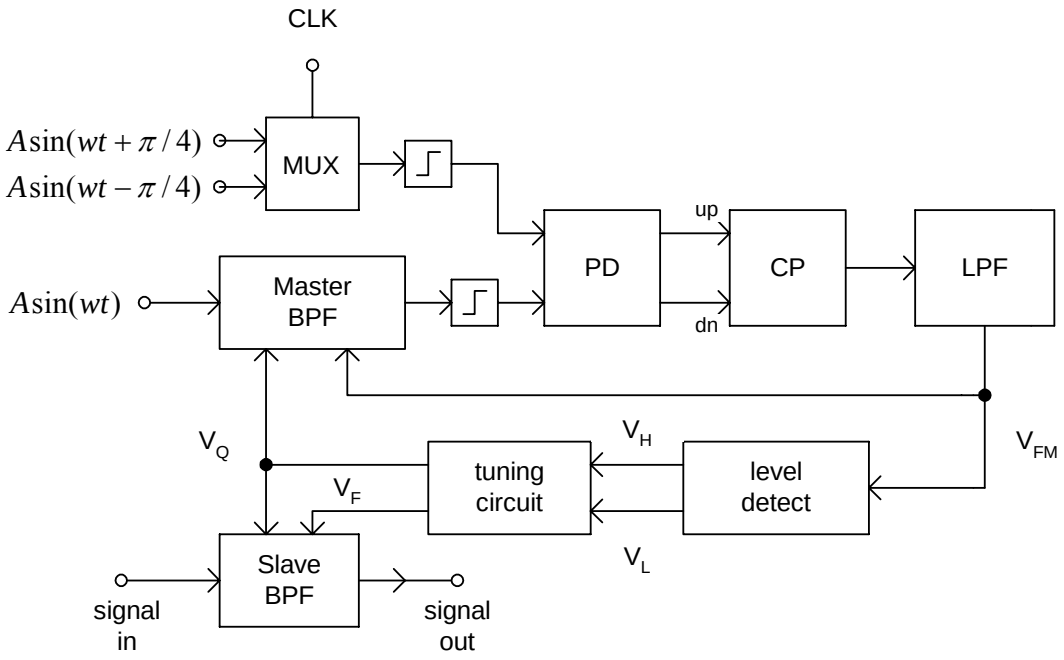

Figure 3.8 Block Diagram of The Complete Tuning System

The reference signal at ω_R with zero phase is applied to the master bandpass filter. Using the multiplexer (MUX), one of the inputs of the phase detector becomes either 45^0 or -45^0 delayed reference clock, which changes the steady-state phase difference between the filter input and the output. The period is set by the CLK signal. The phase

detector, as shown in Figure 3.9, generates UP and DN signals to be used by the charge pump circuit, which is shown in Figure 3.10. After filtering out the high-frequency component, the control voltage V_{FM} is fed back to the frequency control voltage of the master filter. During alternate cycles, set by CLK in the MUX, V_{FM} converges to V_L and V_H. These two voltages are separated into two DC signals by using the level detection circuit as shown in Figure 3.11. The tuning circuit generates the appropriate tuning voltage V_F and V_Q for the slave filter in which the actual signal is processed. The circuit block diagram is shown in Figure 3.12. The averaging operation is performed using a single differential difference amplifier (DDA) [39] [40].

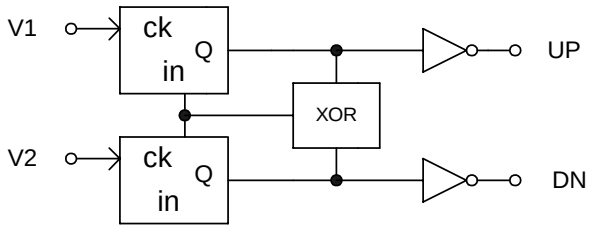

Figure 3.9 Phase Detector Circuit

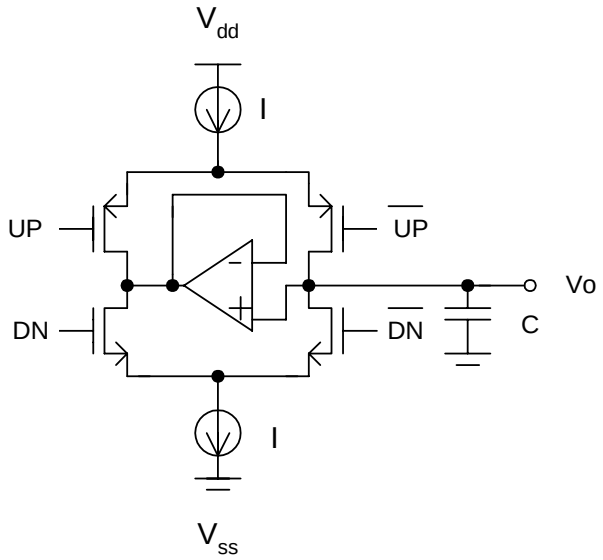

Figure 3.10 Charge – Pump Circuit

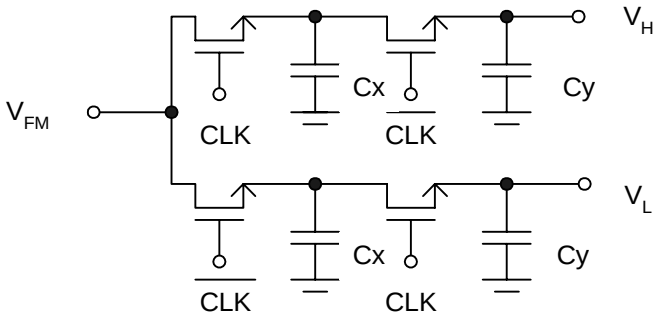

Figure 3.11 Level Detection Circuit

Applying V_L and V_H to two non-inverting terminals of the DDA1 and forming a negative feedback from both inverting terminals to the output, the output voltage V_F can be obtained as $V_F = (V_H + V_L)/2$, which is the desired frequency tuning voltage, as in equation (2-6), so V_F can be directly applied to the slave filter in order to tune its pole

frequency to ω_R. To tune the Q factor, the difference $V_H - V_L$ is compared with V_F / Q_d by means of DDA2 in Figure 3.12.

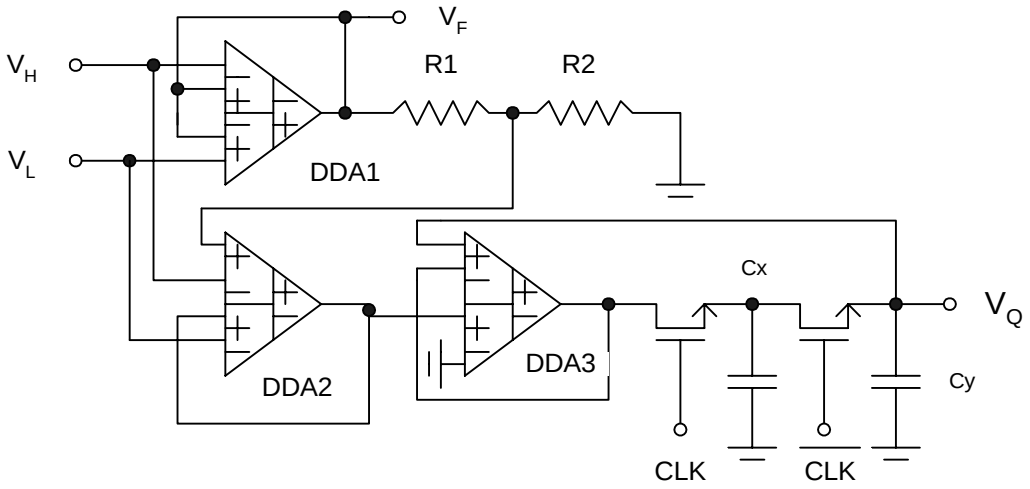

Figure 3.12 Tuning circuit

The desired Q value is set by

$$Q_d = \frac{R1 + R2}{R2} \tag{3-16}$$

At the end of each cycle set by CLK, Q tuning voltage is updated by

$$(V_Q)_{n+1} = (V_Q)_n + \frac{C_x}{C_x + C_y}\left(\frac{V_F}{Q_d} - (V_H - V_L)\right) \tag{3-17}$$

At steady state, $Q_d = V_F /(V_H - V_L)$ is achieved.

3.5 Detailed Circuit Implementation

3.5.1 Phase Difference Generation Circuit

In this tuning system, two reference signals at the center frequency of the filter are used [41]. One references 45^0 phase difference with respect to the filter input and the other one has -45^0 phase difference. In Figure 3.13, the clock generation circuit provides eight output signals: Q_1, Q_2, Q_3, Q_4 with 45^0 , -45^0 , 135^0 , and -135^0 phase differences ,respectively, and corresponding waveform Q_{1B}, Q_{2B}, $Q_{3B,}$ and Q_{4B}. In Figure 3.14, a high-speed inverter is used to generate for creating C_k. The reason for using a high-speed inverter is to reduce the signal propagation delay between C_k and C_{kb}.

3.5.2 Differential Difference Amplifier (DDA)

Differential difference amplifier (DDA) is an important circuit block [40] that has many applications such as switched capacitor circuits, common mode detection and continuous time filters. In the Q tuning circuit, the loop needs to calculate reference control voltage of the filter's center frequency and its bandwidth. A detailed DDA circuit diagram is shown in Figure 3.14. The input output relation of the DDA is shown as

$$Vo = A\left(\left(V_{pp} - V_{pn}\right) - \left(V_{np} - V_{nn}\right)\right) \tag{3-18}$$

where *A* is the gain of the DDA.

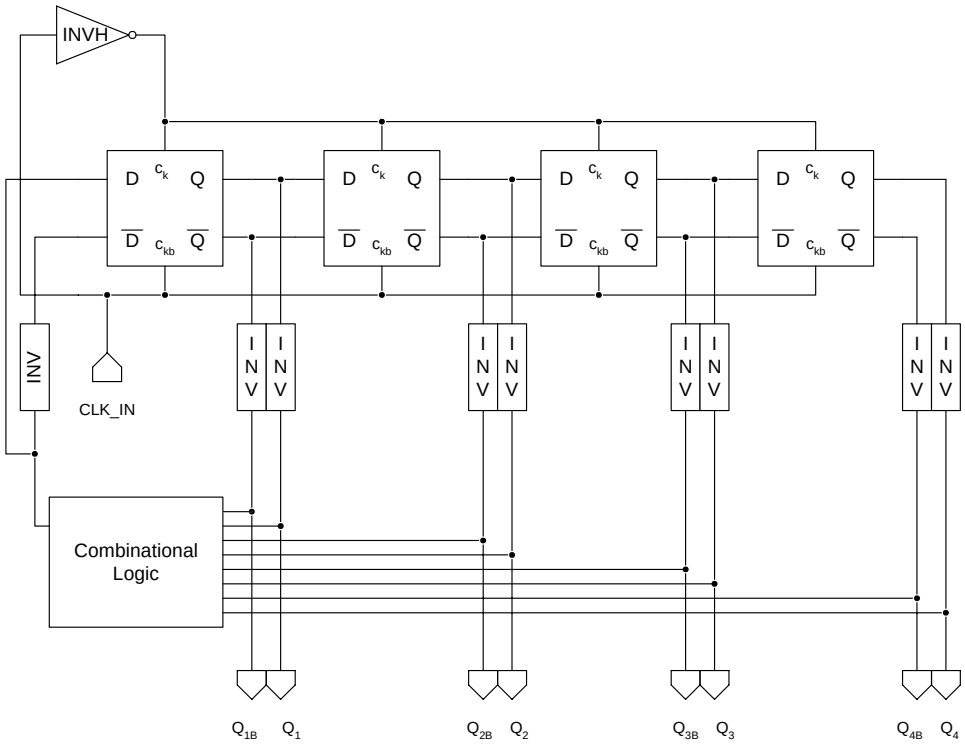

Figure 3.13 Reference Clock Generation Circuit

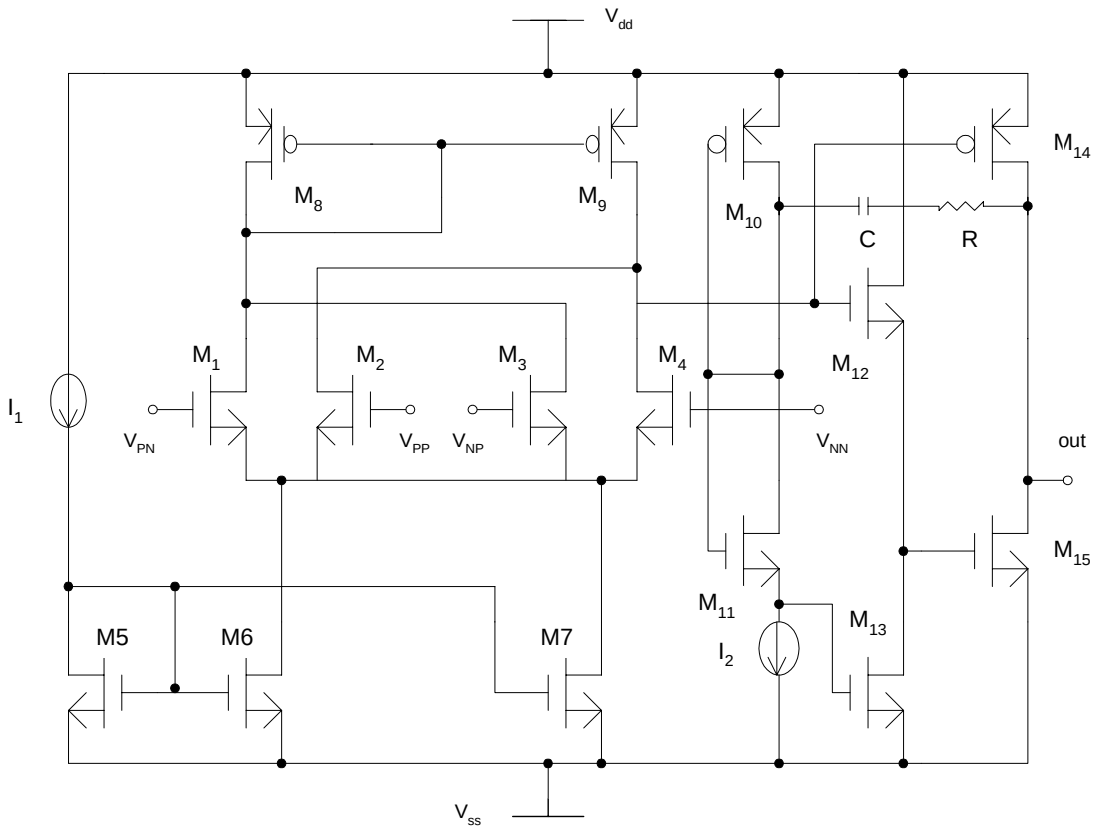

Figure 3.14 Differential Difference Circuit

CHAPTER IV

SIMULATION AND MEASUREMENT RESULTS

4.1 Simulation Results for Open Loop Tuning

Figure 4.1 shows the transconductance of the OTA as a function of control voltage V_{tune}, where the linear dependence is verified.

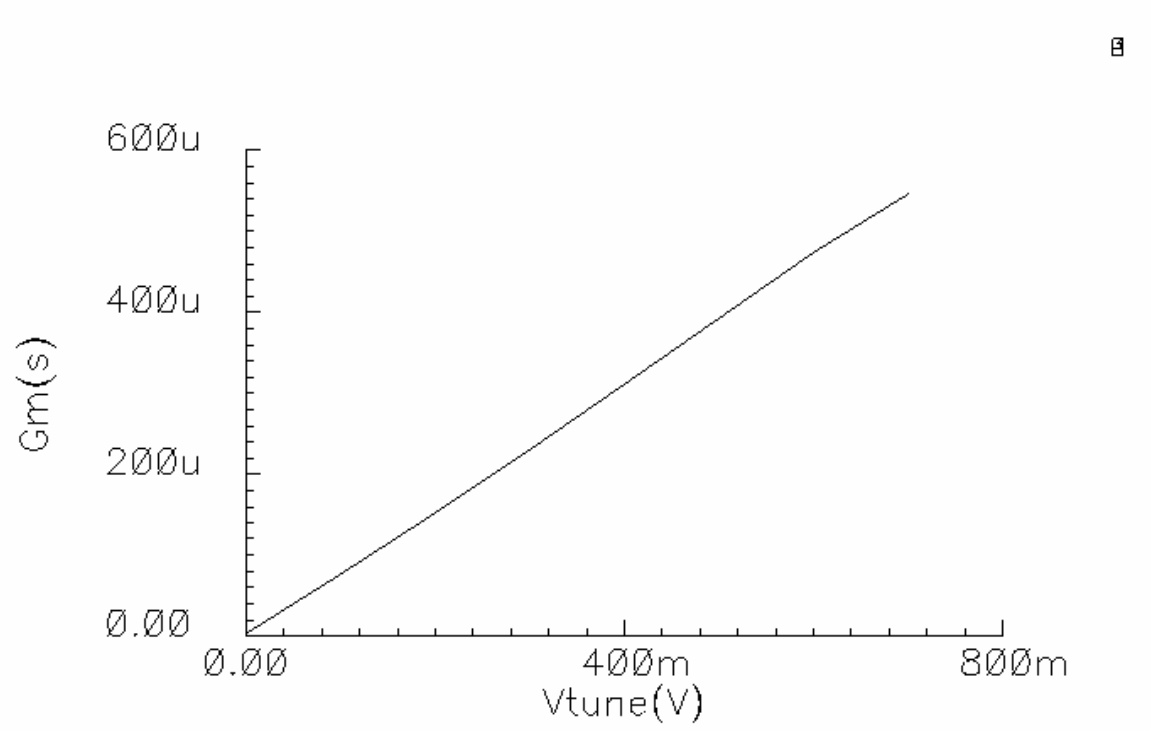

Figure 4.1. Transconductance Linearly Tunable by Control Voltage

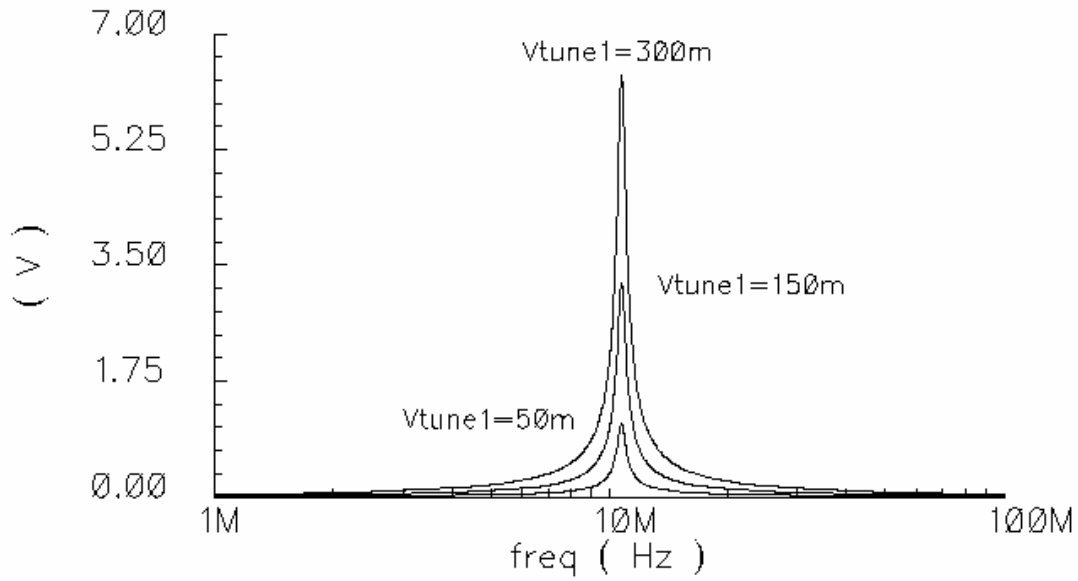

Figure 4.2 Filter Magnitude for Several Gain and Constant Q=20

Figure 4.2 shows that the filter gain can be varied linearly with constant Q=20.

4.2 Simulation Results for Close Loop Tuning

Figure 4.3 shows that V_F is equal to $Q_d(V_H - V_L)$ at steady state, which sets the quality factor, given in equation 3-15, to the desired value, Q_d. Figure 4.4 shows the waveforms of V_{FM}, V_L, and V_H.

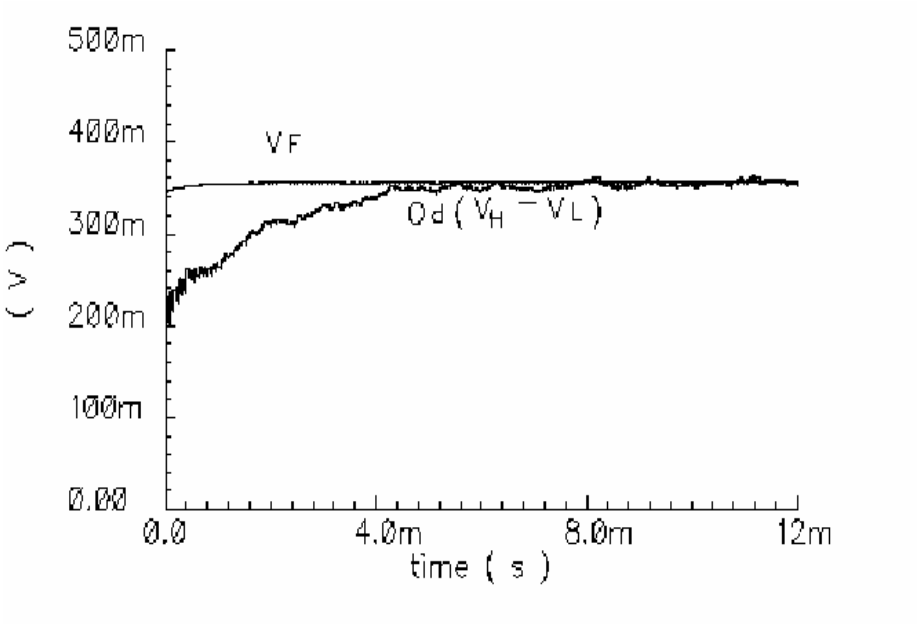

Figure 4.3 Tuning voltages of the center frequency and bandwidth

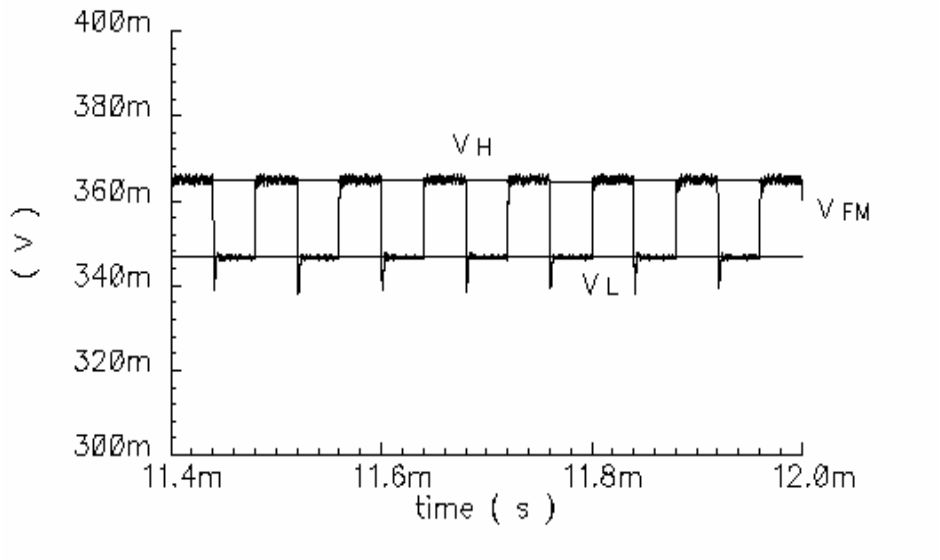

Figure 4.4 Master BPF Frequency Control Voltage V_{FM} with the DC Levels V_L and V_H

4.3 Layout and Related Photograph

The layout of the circuit is designed using AMI 0.5µm technology provided by MOSIS. Chip layout is shown in Figure 4.5.

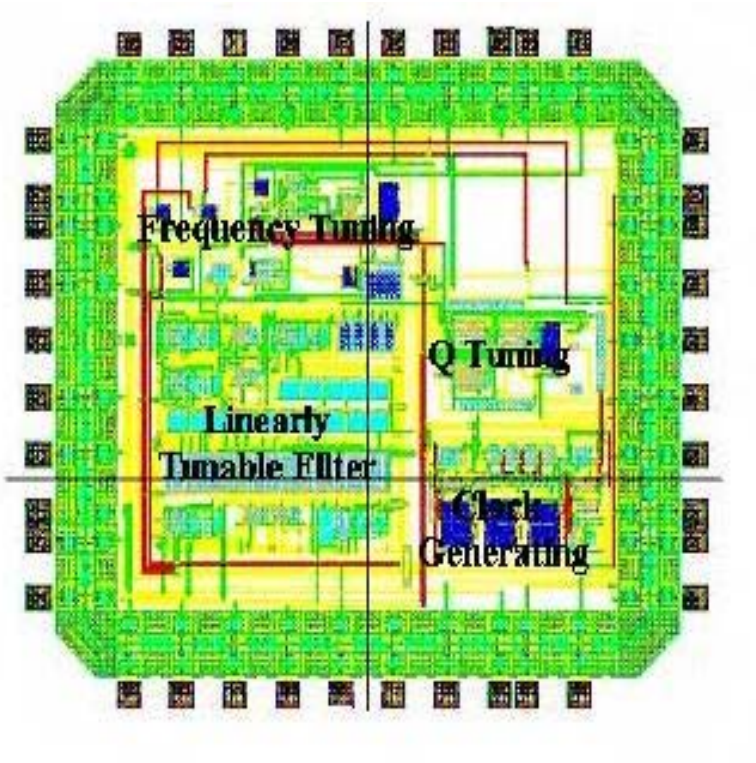

Figure 4.5 The Layout of the Chip with AMI 0.5µm Technology

Including the padframe, layout size is 2.3mm by 2.3mm. The number of pins is 40 and the package is DIP40. The clock generating circuit is laid out with symmetry to improve matching. The filter's differential pairs are designed using 'interdigitation' and 'common centroid' layout techniques and some dummy transistors are added to improve

accuracy. Large current biasing transistor width is used to reduce the mismatch effect. The output signal is connected to buffers to reduce loading effects.

4.4 Experimental Results

4.4.1. Experimental Setup

A printed circuit board is designed for testing the filter and the tuning system. The whole test board is shown in Figure 4.6. Transformers are used to convert differential ended signals into single-ended signals and vice verse. Transformer impedance ratio is 1:4 and its 3dB bandwidth range is from 1 to 600 MHz. DC blocking is implemented by 47nF capacitors. Resistors and variable resistors are used for controlling DC bias voltage and currents. In Figure 4.6, there are two input ports for the filter. These two ports are connected to the transformer. There are also two input ports for 80 MHz and 100 KHz reference clocks. These references are used for tuning purposes. The two inputs switch_freq_control and switch_Q_control are used to switch between manual or automatic tuning modes. The whole PCB picture is shown in Figure 4.7. The chip photograph is shown in Figure 4.8.

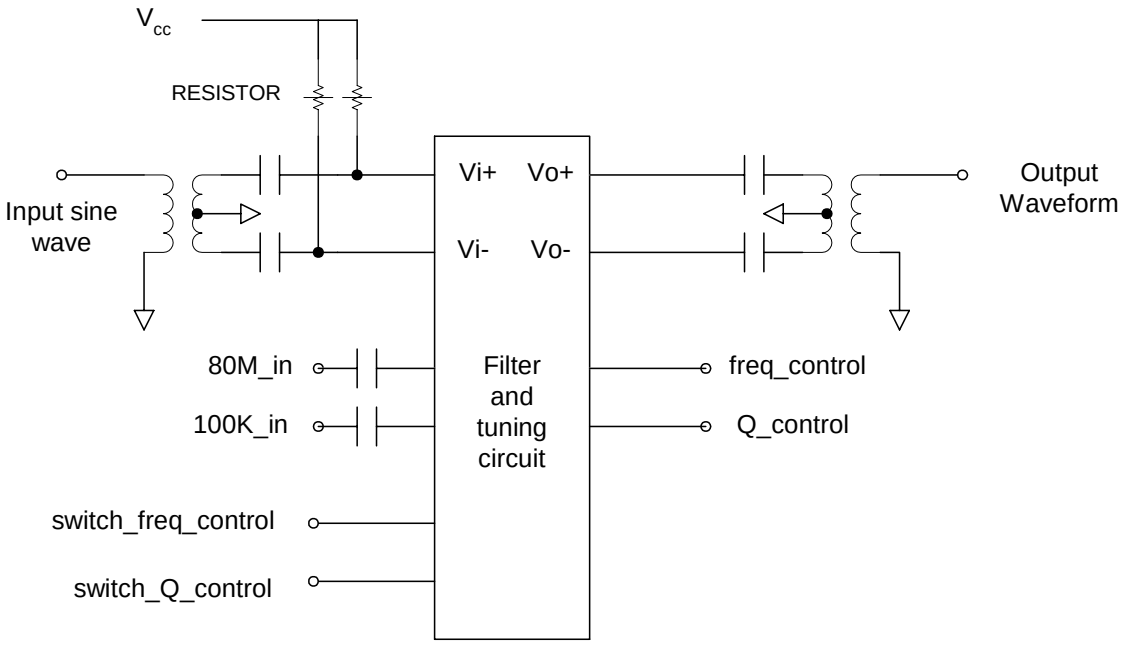

Figure 4.6 Testing Setup for the Filter and Tuning Scheme

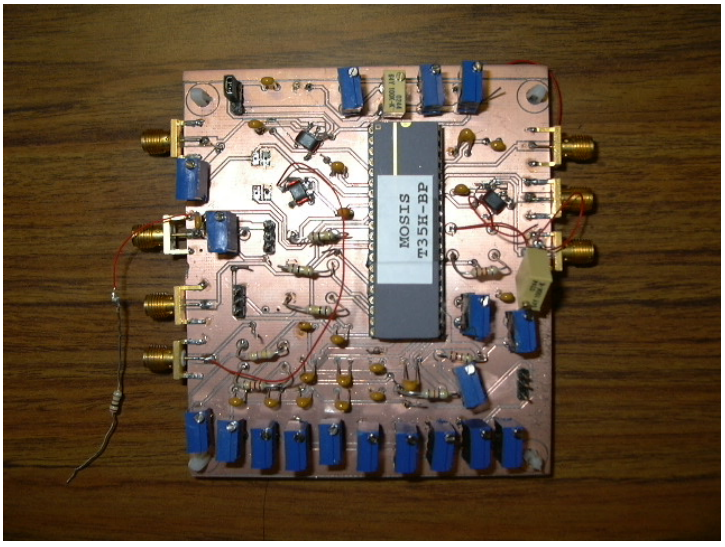

Figure 4.7 Picture of PCB

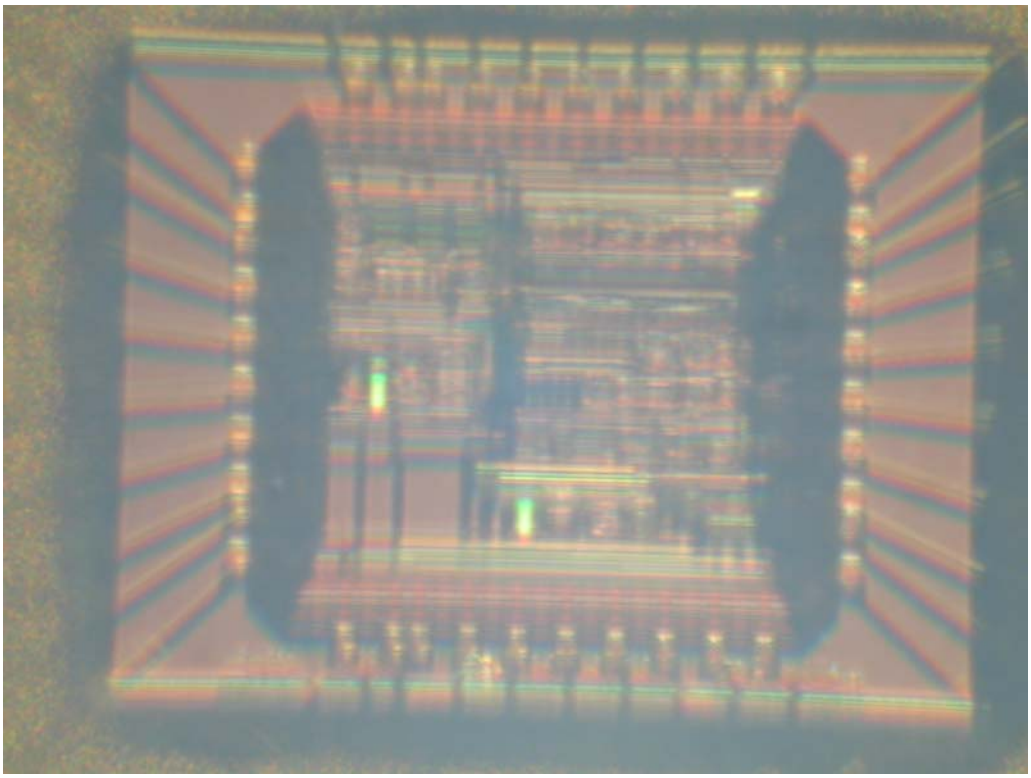

Figure 4.8 Photograph of Chip

4.4.2 Experimental Results

Figure 4.9 shows the spectrum of the filter output, the center frequency is 10 MHz and Q is 140.

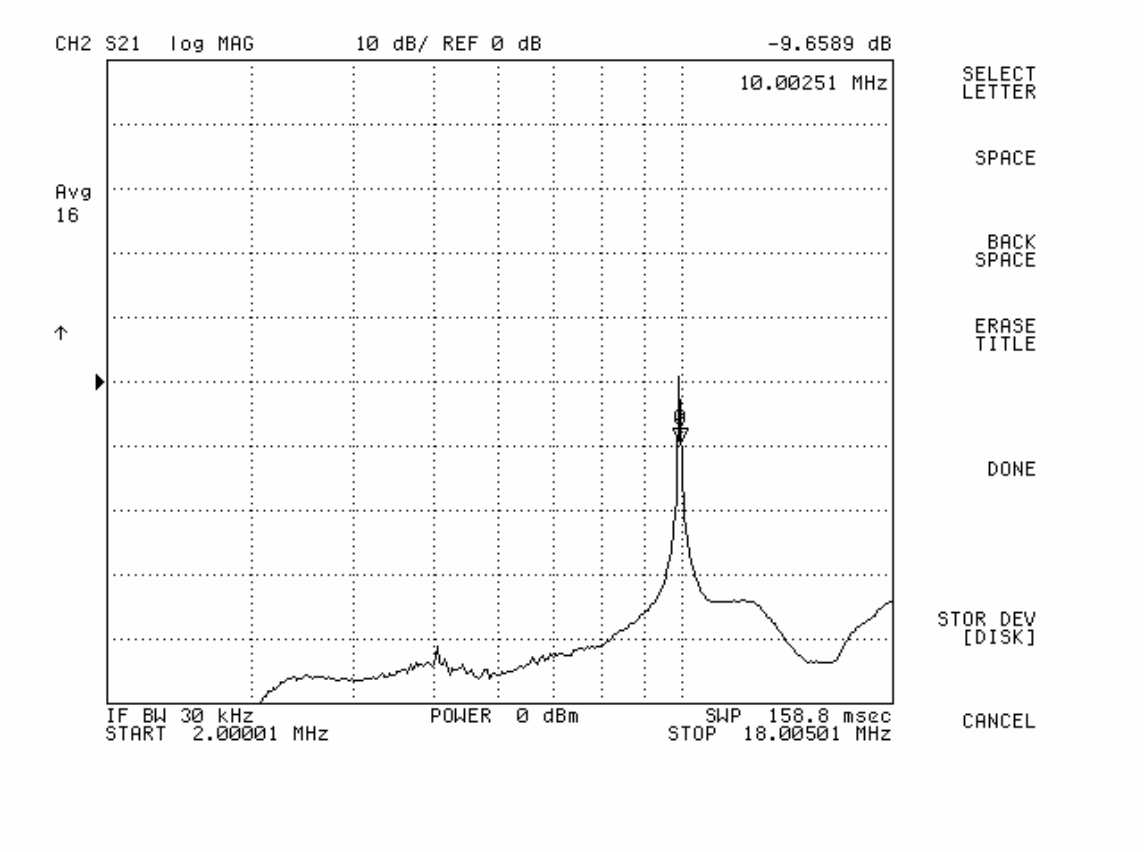

Figure 4.9 Filter Spectrum Analysis with Center Frequency 10 MHz and Q is 140

Figure 4.10 shows manual tuning of the frequency range from 9 MHz to 11 MHz and Q is kept around 40. Figure 4.11 shows different Q values from 18 to 140 and the center frequency varies from 9.63 MHz to 10.12 MHz.

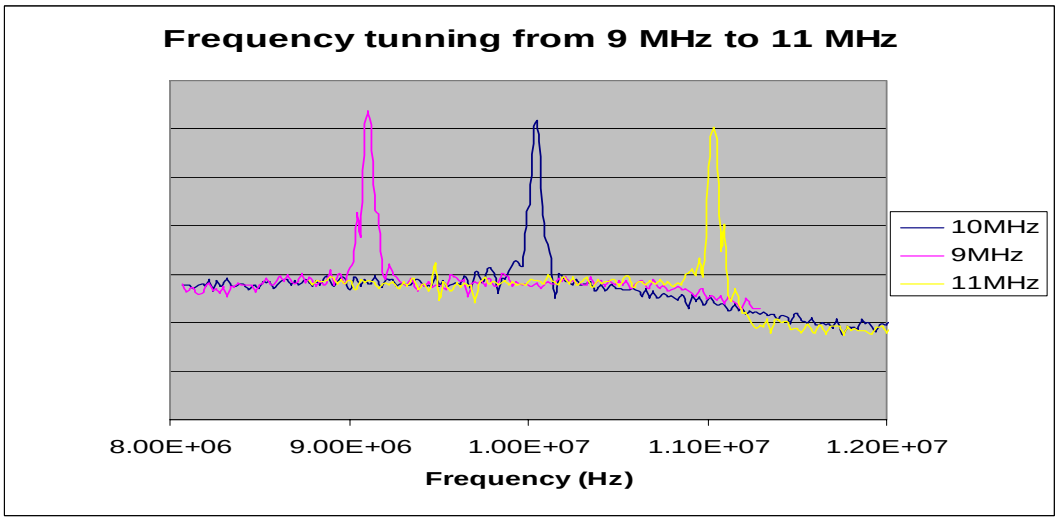

Figure 4.10 Frequency Tuning from 9 MHz to 11 MHz

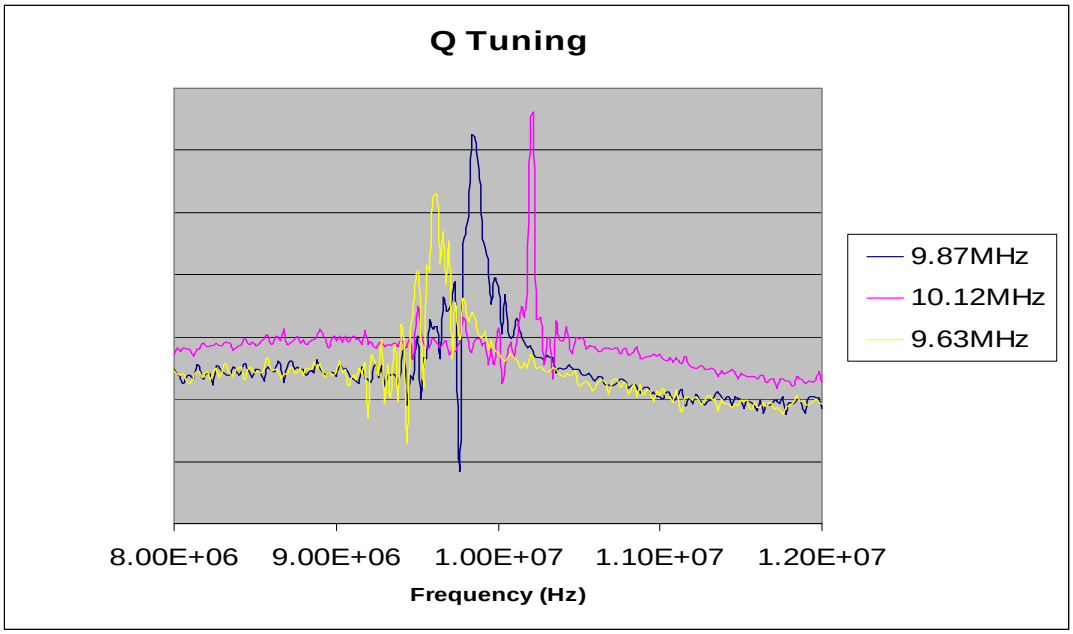

Figure 4.11 Q Tuning from 18 to 140

Frequency control voltage waveforms are recorded in the oscilloscope and use this voltage to show the referenced center frequency. Figures 4.12 and 4.13 show the tuning voltages of center frequency and Q. The automatic frequency tuning errors are shown in Table 4.1.

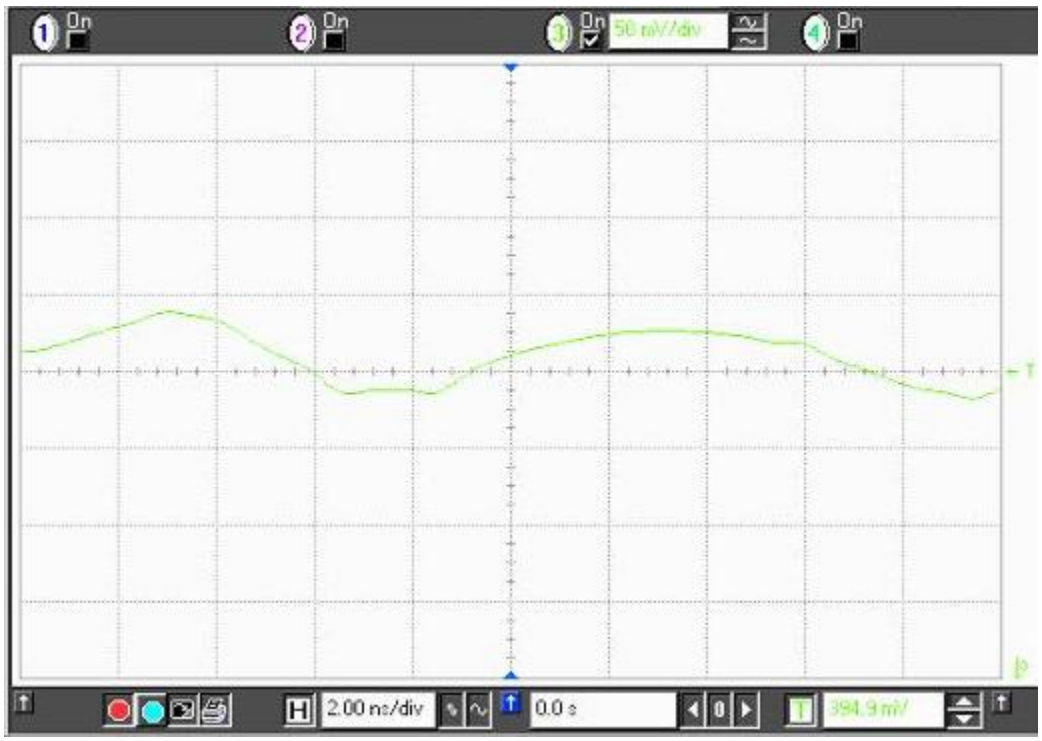

Figure 4.12 Frequency Tuning Voltage

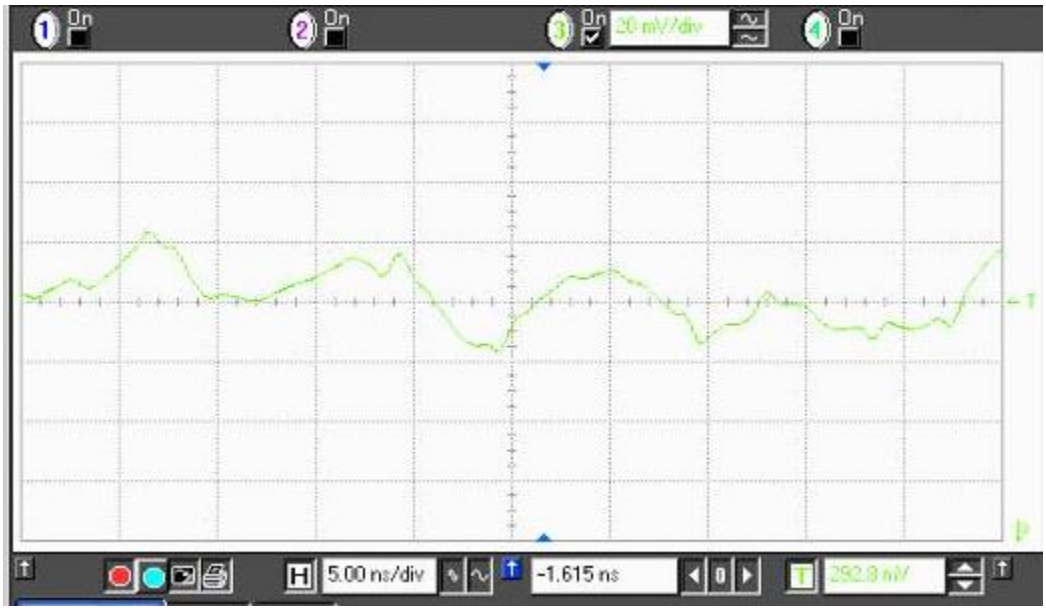

Figure 4.13 Q Tuning Voltage

Table 4.1 Frequency Tuning Errors with Automatic Tuning

Clock input frequency	Tuning voltage (detected)	Center frequency (MHz)	Frequency tuning error
80(MHz)	0.4403(V)	9.72	2.50%
96(MHz)	0.513(V)	11.34	2.67%
72(MHz)	0.421(V)	9.26	2.54%
64(MHz)	0.378(V)	8.16	2.38%

CHAPTER V

CONCLUSION

Most Q factor tuning schemes assume a certain relationship between the quality factor and the filter's passband gain. This assumption relies on matching of transconductances and capacitors, including the additional parasitics. This may limit the accuracy of tuning in the presence of dominant or large parasitics.

A new tuning scheme is proposed. The method uses the phase information and a reference signal at a single frequency. The filter does not need to have the relationship between the filter's gain and its Q, but it needs the linearly tunable filter [42]. The proposed new tuning method has the advantage of just using single frequency to tune both center frequency and Q of the filter. The tested results show that the automatic frequency tuning errors are 2.5% for a 10 MHz references.

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VITA

Sung-Ling Huang was born in Taipei, Taiwan. He received his B.S. and M.S. degrees in electrical engineering from Tatung Institute of Technology, Taipei, Taiwan, in 1988 and 1990, respectively. He worked towards his M.S. degree in electrical engineering under the supervision of Dr. Aydin I. Karsilayan in the Analog & Mixed-Signal Center at Texas A&M University, College Station, TX. From January to August 2001, he worked in the mixed signal and wireless baseband division at Texas Instruments in Dallas as a co-op student. His activities are focused on analog and filter circuit design. His permanent address is 5F, no1, nang-ging erd sec2 Taipei, Taiwan.