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An Integrated Analog Readout for Multi-Frequency Bioimpedance Measurements

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Abstract—Bioimpedance spectroscopy is used in a wide range of biomedical applications. This paper presents an integrated analog readout, which employs synchronous detection to perform galvanostatic multi-channel, multi-frequency bioim-pedance measurements. The circuit was fabricated in a 0.35-μηι CMOS technology, occupying an area of 1.52 mm^2. The effect of random dc offsets is investigated, along with the use of chopping to minimize them. Impedance measurements of a known RC load and skin (using commercially available electrodes) demonstrate the operation of the system over a frequency range up to 1 MHz. The circuit operates from a ±2.5 V power supply and has a power consumption of 3.4-mW per channel.

Index Terms—Analog circuit design, bioimpedance, impedance spectroscopy, multi-frequency, readout, synchronous detection.

I. Introduction

BIOIMPEDANCE measurement is an established technique with a wide range of medical applications. These include cancerous tissue characterization and detection [1], electrical impedance tomography (EIT) [2], total body analysis systems [3], gas sensors [4], impedimetric biosensors [5] and various lab-on-a-chip applications [6]. In human tissue measurements [1]-[3] typically a galvanostatic approach (inject current, measure voltage) is used in order to limit the current injected to the tissue and thus, adhere to medical safety regulations with the maximum allowable current being a function of frequency [7]. The current driver input signal can either be a single frequency sinusoid or a multi-frequency signal [8].

Impedance can be described by its magnitude and phase or, alternatively, by its real and imaginary parts. Magnitude/phase measurement is the simplest and most straightforward tech-nique. The magnitude can be calculated using a peak detector [9] or by full-wave rectification and subsequent low-pass filtering [10] of the measured sinusoidal voltage across the load. Calculation of the phase requires a reference signal in-phase (0°) to the one applied to the impedance under test. Comparison of square wave versions of this reference signal with the measured one across the impedance at each frequency with a phase detector provides a measure of the impedance phase. The phase output can then be processed further as discussed in [10]. Hence, a magnitude/phase measurement requires two different measurement channels, each with poten-tially different sources of error, requiring different techniques to address them. Synchronization is only important for the phase channel. Multi-frequency measurements require the use of bandpass filters in this topology, with a dedicated channel for each frequency.

Real/imaginary part measurement is more complicated. A methodology to obtain the real and imaginary components is the sampling technique [11], [12]. Since the excitation signal frequency, phase and amplitude are typically known, there is no need to perform a fast Fourier transform (FFT). By sampling at the exact instances where the input frequency components reach their peak value and cross zero, the real and imaginary components are obtained. This technique is known as synchronous sampling (SS). Obtaining these samples in both half cycles of the period eliminates offsets by averaging the measurements [12]. Averaging the measurements within the full period of a multi-frequency signal allows the calcula-tion of the real and imaginary components at each frequency using a single channel [12], which is an advantage over other techniques. However, accurate synchronization for obtaining the samples is essential, which can be challenging, particularly at high frequencies [11].

Synchronous detection (SD, also known as lock-in, phase sensitive and quadrature demodulation) is a popular technique for this type of measurement and is well established [4], [13]-[15]. Multiplication of the measured sinusoidal voltage signal by an in-phase (0°) and a quadrature (90°) signal is required to calculate the real and imaginary component values, respectively, at the frequency of the applied signal (in a single frequency measurement) or with a frequency of interest which is present in the applied signal (in a multi-frequency measurement). In this way the readout locks to a specific frequency component, demodulating it to dc with all other frequency components being modulated to higher frequencies (including electrode dc voltages). The multiplier output needs to be lowpass filtered in order to reject all frequency components generated by the multiplication and

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any other frequencies present, and keep the dc component proportional to the real or imaginary part of the impedance. The combination of the multiplication and the lowpass filter effectively imposes a frequency selective property to the system. Hence, no additional bandpass filters are required as in the magnitude/phase system. Once again, two channels are required, which need to be accurately matched. In this case, however, the channels are identical and thus, sources of error are common. In applications where the impedance does not change rapidly, a single channel can be used, by switching the demodulation signal between 0° and 90°. The cutoff frequency and order of the filter for the abovementioned systems can be selected by considering the lowest frequency of interest and the settling-time required, defined by the biological system being investigated [8].

One of the challenges in such a system is the design of the current driver [16], [17]. The amplitude of the drive current should remain constant irrespective of the impedance mag-nitude of the load and the frequency (in order to eliminate the need to constantly measure it). Another performance characteristic of the current driver is the phase difference between the output current signals relative to the input applied signals. Depending on the impedance measurement (readout) topology, the current driver phase error may need to be kept to a minimum, as it can introduce errors in the calculation of the measured impedance.

EIT for neonatal lung function monitoring, which is one of the target applications, requires a large number of measure-ments from 32 or more electrodes. To avoid issues associated with physiological drift, the measurements should be per-formed rapidly. This dictates a system capable of simultaneous measurements of the real and imaginary components of the load impedance (typically <100 Ω to > 5 k Q) at multiple frequencies, with a frequency range up to 1 MHz [18]. A minimum of two frequencies are required to perform frequency differencing measurements for imaging [19]. The minimization of parasitics (e.g. due to cabling), and the need for a multi-channel readout (for multi-frequency opera-tion), portability and miniaturization, necessitate the develop-ment of custom designed integrated circuits for bioimpedance applications, which can also offer the option to embed the instrumentation on the electrodes. This paper presents an integrated multi-channel analog readout employing SD for multi-frequency bioimpedance measurements, which to the authors' knowledge is the first of its kind. The performance of the fabricated chip (in a 0.35-^m CMOS technology) is demonstrated with both single- and multi-frequency signals. Chopping is used to minimize the dc offset voltages of the on-chip instrumentation amplifiers (IAs). The effect of the offsets on the measurement is assessed.

The paper is a development of [14] and presents details of the circuit and measurements from a second version of the chip design. The rest of the paper is organized as follows. Section II presents the system architecture and the theory of operation. Section III presents simulated and measured results showing the electrical performance of the fabricated samples for single-and dual-frequency excitation. The chip was combined with a current driver to form a tetrapolar impedance measurement system. Measurements show impedance responses of an RC circuit and skin impedance (obtained with commercial skin electrodes). The discussion and the conclusion in Sections IV and V, respectively, complete the paper.

II. Architecture and Operation

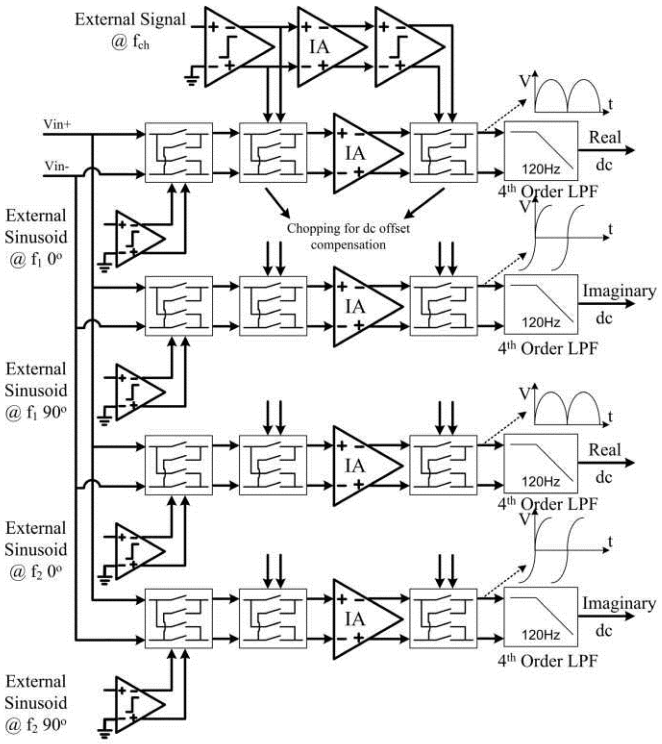

Fig. 1. System block diagram of the multi-frequency analog readout. The voltage versus time curves are examples of the outputs of the amplifiers when the offset is zero, the chopping is disabled and input signal has no phase shift.

Fig. 1 shows the block diagram of the analog readout. In a single frequency scenario the SD modulator output for the real (VsD_{Re}) and the imaginary (VsDJm) channels are [15]

$$V_{\mathrm{SD\_Re}} = \frac{A}{2}\left[\cos\left(\phi_1\right) - \cos\left(2\omega_1 t - \phi_1\right)\right] + C\sin\left(\omega_1 t\right)$$
$$V_{\mathrm{SD\_Im}} = \frac{A}{2}\left[\cos\left(\phi_1 + \frac{\pi}{2}\right) - \cos\left(2\omega_1 t - \phi_1 + \frac{\pi}{2}\right)\right] + C\sin\left(\omega_1 t + \frac{\pi}{2}\right), \quad (1)$$

where A is the amplitude of the voltage across the electrodes, ^1 is the phase delay due to the impedance at angular frequency ω_1 and C is the dc voltage of the electrode. For brevity, only the real part is considered in the following equations. In a dual-frequency scenario where there are two frequency components present [$f_1 = (\omega_1/2\pi)$ with amplitude A and $f_2 = (\omega_2/2\pi)$ with amplitude B] and the signal is demodu-lated with a frequency f_1, then the real part becomes

$$V_{\mathrm{SD\_Re}} = \frac{A}{2}\left[\cos\left(\phi_1\right) - \cos\left(2\omega_1 t - \phi_1\right)\right] + \frac{B}{2}\left[\cos\left(\left(\omega_1 - \omega_2\right)t + \phi_2\right) - \cos\left(\left(\omega_1 + \omega_2\right)t - \phi_2\right)\right] + C\sin\left(\omega_1 t\right). \quad (2)$$

The signal component of interest is the dc value equal to $\frac{A}{2}\cos(\phi_1)$ for the real part (and $\frac{A}{2}\cos\left(\phi_1+\frac{\pi}{2}\right)$ for the imaginary part).

Amplification and lowpass filtering can be combined as in [20]. However, a high common-mode rejection ratio (CMRR) is required in order to reject inevitable common-mode signals generated at the recording electrodes. To satisfy this, a current-feedback IA is used as in [10], [13], and [14] with digitally programmable gains of 10, 75, 140 and 200 V/V. The IA circuit topology used in this design is presented and characterized in [21]. In order to eliminate the effect of the IA phase delay, demodulation is performed before amplification. A multistage clockless comparator [10] provides a square-wave drive to the mixer switch (modulator). The comparator is driven by a sinusoidal signal.

The dc offset of the IA should be minimized to obtain an accurate measurement. The dc offset is random and varies from channel-to-channel and from chip-to-chip. Furthermore, temperature variations, aging and power supply instability could cause the dc offset to fluctuate. To minimize the effect of the dc offset, chopping is employed [22]. The signal of interest is modulated by a carrier signal and this is subsequently amplified by the IA. The signal at the output of the IA contains the amplified signal plus any dc offset of the IA. This is then modulated again with the same carrier (same frequency and phase). In this way, the dc offset is modulated to the frequency of the carrier, while the signal of interest is demodulated back to its original frequency. In practice, the limited bandwidth of the amplifier contributes to high frequency glitches. Thus, the phase delay of the amplifier should be considered. To limit the glitches, the chopping frequency should be within the zero phase delay band of the amplifier. Alternatively, the chopping signal needs to be phase shifted by a phase equal to the ampli-fier phase at that frequency through a delay line or a phase shifter [22]. In the present implementation a path consisting of two comparators and an identical IA in between them is used to drive the choppers and thus, reduce the effect of the amplifier phase delay to the chopping. This structure is shown at the top of Fig. 1. A square wave signal from an external signal generator is used for chopping. All other frequencies resulting from the modulation and demodulation processes are suppressed by the following lowpass filter. The filter uses a chain of two biquadratic filters as in [10]. When (1) is multiplied by a sinusoidal signal of frequency f_{ch} ($= \omega_{(\pm/2\pi)}$) and unity amplitude the output of the first chopper is

$$\begin{aligned} V_{\text{Ch1\_Re}} &= \frac{A}{2}\cos(\phi_1)\sin(\omega_{\text{ch}}t) \\ &\quad - \frac{A}{4}\left[\sin\left((2\omega_1+\omega_{\text{ch}})t-\phi_1\right)-\sin\left((2\omega_1-\omega_{\text{ch}})t-\phi_1\right)\right] \\ &\quad + \frac{C}{2}\left[\cos\left((\omega_1-\omega_{\text{ch}})t\right)-\cos\left((\omega_1+\omega_{\text{ch}})t\right)\right]. \end{aligned} \tag{3}$$

If two frequencies are present, using (2), the output of the first chopper is

$$\begin{aligned} V_{\text{Ch1\_Re}} &= \frac{A}{2}\cos(\phi_1)\sin(\omega_{\text{ch}}t) \\ &\quad - \frac{A}{4}\left[\sin\left((2\omega_1+\omega_{\text{ch}})t-\phi_1\right)\right. \\ &\qquad \left.-\sin\left((2\omega_1-\omega_{\text{ch}})t-\phi_1\right)\right] \\ &\quad + \frac{B}{4}\left[\sin\left((\omega_2-\omega_1+\omega_{\text{ch}})t-\phi_2\right)\right. \\ &\qquad -\sin\left((\omega_2-\omega_1-\omega_{\text{ch}})t-\phi_2\right) \\ &\qquad -\sin\left((\omega_2+\omega_1+\omega_{\text{ch}})t-\phi_2\right) \\ &\qquad \left.+\sin\left((\omega_2+\omega_1-\omega_{\text{ch}})t-\phi_2\right)\right] \\ &\quad + \frac{C}{2}\left[\cos\left((\omega_1-\omega_{\text{ch}})t\right)-\cos\left((\omega_1+\omega_{\text{ch}})t\right)\right]. \end{aligned} \tag{4}$$

The $V_{\text{Ch1\_Re}}$ signals in (3) and (4) are then amplified with a gain G and the dc offset voltage of the IA, D, is added to the signal. Subsequently, the signal is multiplied again by the same chopping signal. The signal before the lowpass filter is

$$\begin{aligned} V_{\text{Ch2\_Re}} &= \frac{G\cdot A}{4}\left[\cos(\phi_1)-\cos(2\omega_{\text{ch}}t-\phi_1)\right] \\ &\quad + \frac{G\cdot A}{8}\left[\cos\left((2\omega_1-2\omega_{\text{ch}})t-\phi_1\right)\right. \\ &\qquad +\cos\left((2\omega_1+2\omega_{\text{ch}})t-\phi_1\right) \\ &\qquad \left.-\cos(2\omega_{\text{ch}}t-\phi_1)-\cos(2\omega_{\text{ch}}t+\phi_1)\right] \\ &\quad + \frac{G\cdot C}{4}\left[2\sin(\omega_1 t)-\sin\left((\omega_1-2\omega_{\text{ch}})t\right)\right. \\ &\qquad \left.-\sin\left((\omega_1+2\omega_{\text{ch}})t\right)\right] \\ &\quad + D\sin(\omega_{\text{ch}}t). \end{aligned} \tag{5}$$

If two frequencies are present, using (4), the output of the second chopper is

$$\begin{aligned} &V_{\text{Ch2\_Re}} \\ &\quad = \frac{G\cdot A}{4}\left[\cos(\phi_1)-\cos(2\omega_{\text{ch}}t-\phi_1)\right] \\ &\quad + \frac{G\cdot A}{8}\left[\cos\left((2\omega_1-2\omega_{\text{ch}})t-\phi_1\right)\right. \\ &\qquad +\cos\left((2\omega_1+2\omega_{\text{ch}})t-\phi_1\right) \\ &\qquad \left.-\cos(2\omega_{\text{ch}}t-\phi_1)-\cos(2\omega_{\text{ch}}t+\phi_1)\right] \\ &\quad + \frac{G\cdot B}{8}\left[2\cos\left((\omega_2-\omega_1)t-\phi_2\right)\right. \\ &\qquad -\cos\left((\omega_2-\omega_1+2\omega_{\text{ch}})t-\phi_2\right) \\ &\qquad -\cos\left((\omega_2-\omega_1-2\omega_{\text{ch}})t-\phi_2\right) \\ &\qquad -2\cos\left((\omega_2+\omega_1)t-\phi_2\right) \\ &\qquad +\cos\left((\omega_2+\omega_1+2\omega_{\text{ch}})t-\phi_2\right) \\ &\qquad \left.+\cos\left((\omega_2+\omega_1-2\omega_{\text{ch}})t-\phi_2\right)\right] \\ &\quad + \frac{G\cdot C}{4}\left[2\sin(\omega_1 t)\right. \\ &\qquad \left.-\sin\left((\omega_1-2\omega_{\text{ch}})t\right)-\sin\left((\omega_1+2\omega_{\text{ch}})t\right)\right] \\ &\quad + D\sin(\omega_{\text{ch}}t). \end{aligned} \tag{6}$$

In (1) to (6), the chopping and SD multiplication signals are considered as pure sinusoids for simplicity. In reality these are square wave signals, which contain many harmonic com-ponents. More detailed expressions for these multiplications are presented in [13]. At the filter output, there will be a small ripple with the same frequency as the carrier signal. Its amplitude depends on the offset value, the cutoff frequency of the lowpass filter and the frequency of the carrier signal used to perform the chopping function [23]. The lowpass filtered output dc signal (Vdcout) of the chopped lock-in amplifier

needs to be divided by G and a 2/π factor resulting from the series of modulation and demodulation stages, to obtain the actual dc component (V_o). This is equal to

$$V_o = \frac{\pi}{2G} V_{dc\_out}. \quad (7)$$

Charge injection mismatch due to mismatch between the chop-ping clock lines, and thus the parasitic capacitances associated with these, leads to residual offset. This can be reduced by minimizing the parasitic capacitances and with a symmetric layout of the chopping clock wires [23]. This source of residual offset is also a function of the chopping frequency and the on-resistance (R_{on}) of the input chopper switches, being directly proportional to both. Another source of charge injec-tion is parasitic channel charge redistribution and capacitive feedthrough in the switches in the choppers [22], [23]. The former is directly proportional to the width and length product of the transistors and the latter is directly proportional to their gate-to-source capacitance (and thus also the area of the tran-sistor). Although these errors could be reduced by using min-imum size transistors, this solution leads to a high R_{on}.Other techniques to minimize charge injection errors include the use of dummy switches, transmission gates (leading to a lower R_{on}) , differential topologies, the use of a delayed demod-ulation signal or a guard band in the demodulation signal and spike filtering [22], [23]. In this implementation a fully-differential architecture and transmission gate switches are used. To improve matching, common-centroid layout is used. In total there are four channels, two for measuring the real and imaginary parts at frequency f_1 and the other two at f_2.

III. Results

To examine the performance of the circuit under process variations and device mismatch, a single channel (see Fig. 1) was simulated with an input sinusoidal signal of 1 kHz frequency and 50 mV amplitude. The signal was demodu-lated with an in-phase square wave (0°) of 1 kHz frequency generated by the comparator. The mixer switches performing the chopping were driven by a square wave of 10 kHz frequency, as shown in Fig. 1. The nominal output (i.e., with no mismatch) of the channel, using (7), should have a dc value of approximately 50 mV. The result of the Monte Carlo simulation for 500 runs with both process variations and mismatch is shown in the histogram in Fig. 2. The channel output has a mean value of 49.7 mV and a standard deviation (std) of 1.2 mV. 97 % of the runs are within a 5% deviation from the mean value. This result demonstrates the robustness of the design under process variations and device mismatch.

The analog readout was fabricated in a 0.35-μ mCMOS technology. Fig. 3 shows the chip microphotograph with the various parts identified. A series of electrical tests were first performed to characterize the performance of the circuit (single- and multi-frequency scenarios). Following this, the chip was used with a current driver to perform tetrapolar impedance measurements, as described below. The required input and clock signals were provided from two synchronized TTi TGA12101 signal generators. All output dc voltage measurements were performed with a Keithley 2182 Nanovoltmeter. An Agilent Infinii Vision oscilloscope was used to monitor the various voltage signals. External noise or interference sources were not an issue and thus the use of a Faraday cage was not necessary.

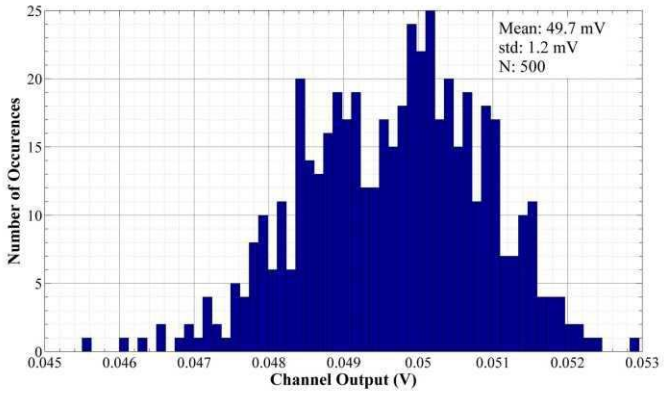

Fig. 2. Monte Carlo simulation, including device mismatch and process variations, of a of single channel output. Number of Monte Carlo iterations (N): 500.

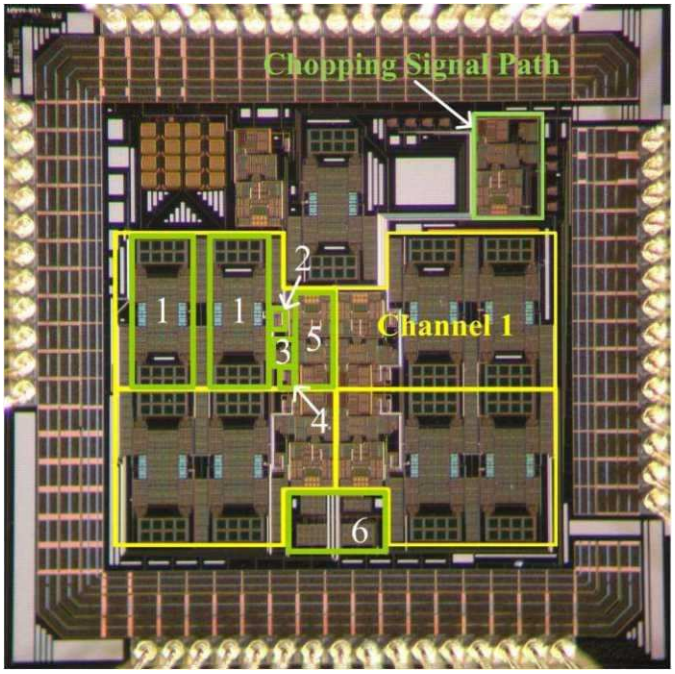

Fig. 3. Chip microphotograph indicating each channel in yellow and the chopping signal generation path. 1: filter, 2: demodulation and chopping switches, 3: comparator, 4: gain control switches, 5: variable gain instru-mentation amplifier, 6: current biasing circuitry.

A. Single-Frequency Measurement

Sinusoidal test signals at various frequencies from 50 Hz to 1 MHz with a peak amplitude of 50 mV, were applied to the chip. The gain of the IA was set to its lowest value of 10 V/V, the output was lowpass filtered, and the phase relationship between input and demodulation signals was varied between 0° and 180°. Channels 1 and 2 (which provided probing points along the channel to assess their performance) of 5 chips in total were tested and the average results are shown in Fig. 4.

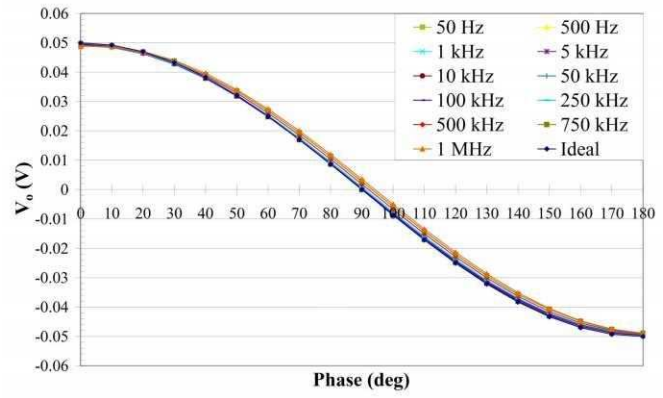

Fig. 4. Measured average dc output following synchronous detection and amplification when varying the phase relationship between input and demodulation signals between 0° and 180°.

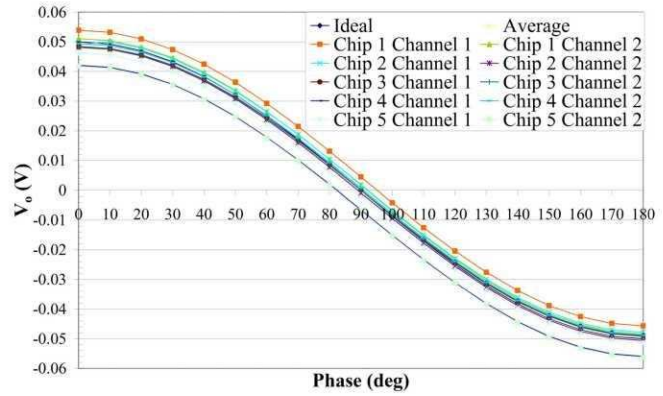

Fig. 5. No chopping: The effect of the random dc offset on the IA on the synchronous detector output from chip-to-chip and channel-to-channel with a 100 kHz 50 mV input signal.

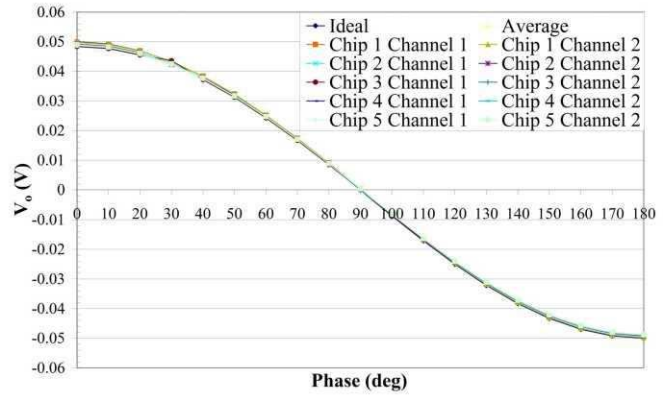

Fig. 6. Same as Fig. 5, with chopping at 10 kHz.

Since the signal of interest is at dc, the dc offsets of the IA are important. Fig. 5 shows the effect of the random dc offsets to the system output when the input to the system is a signal of 50 mV amplitude at 100 kHz. Fig. 6 shows how the results are improved giving the correct dc value, when chopping at 10 kHz is performed.

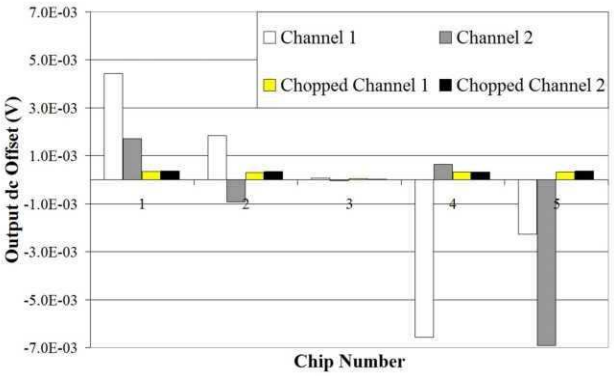

Fig. 7. Measured random dc offset at the outputs of the IA (with gain of 10 V/V, before and after the application of chopping. The data were extracted from Fig. 5 and Fig. 6 for Φ = 90°.

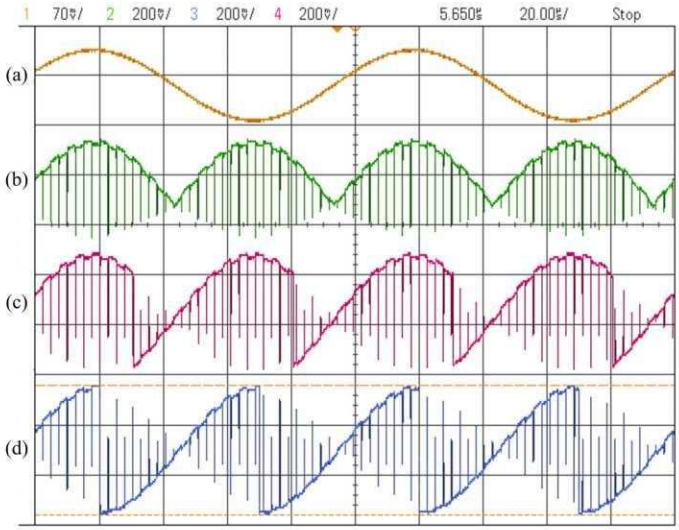

Fig. 7 shows the value of the IA output dc offset measured before and after the offset

Fig. 8. Waveforms obtained when (a) a sinusoidal input signal with a 50 mV amplitude at 1 kHz is recorded and demodulated by a signal of the same frequency phase shifted by (b) 0°,(c)45° and (d) 90°. (b), (c) and (d) are chopped at 10 kHz.

compensation modality used is activated. For example, for channel 2 (no chopping) of chip 5 with an output dc offset of about 7 mV and for a 20 μ A drive current, using Ohm's law, this corresponds to a 350 Ω error in the calculation of the real or imaginary parts of the impedance. Fig. 8 presents oscillo-scope waveforms using an input sinusoidal signal of 50 mV at 1 kHz [Fig. 8(a)], a sinusoidal demodulation signal of the same frequency, phase shifted by 0° [Fig. 8(b)], 45° [Fig. 8(c)] and 90° [Fig. 8(d)] and chopped at a frequency of 10 kHz. The effect of chopping can be seen on the signals of Fig. 8(b)-(d). The offset voltage has been modulated to the chopping fre-quency, resulting to the high frequency switching present in these signals [13].

B. Multi-Frequency Measurement

For the multi-frequency tests, frequencies from 76 Hz to 1 MHz were used. These frequencies are suitable for neonatal lung function monitoring [18] and cervical cancer

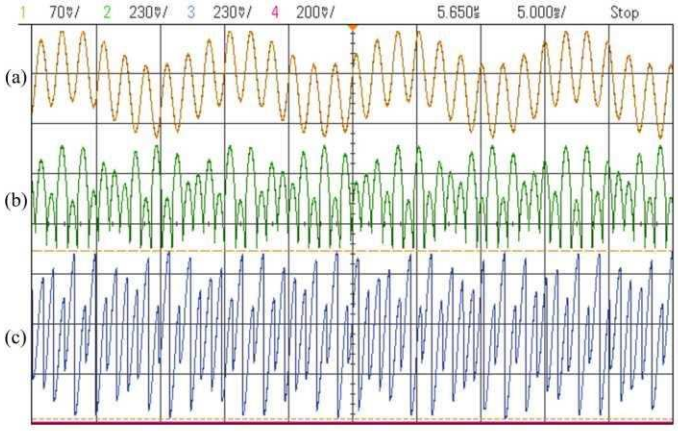

Fig. 9. Multi-frequency measurements. (a) A composite signal comprised of a sinusoid at 76 Hz and 25 mV and a second one at 610 Hz and 53 mV. The recorded signal is demodulated with a 610 Hz square wave at (b) 0° and (c) 90°. (b) and (c) are chopped at 10 kHz.

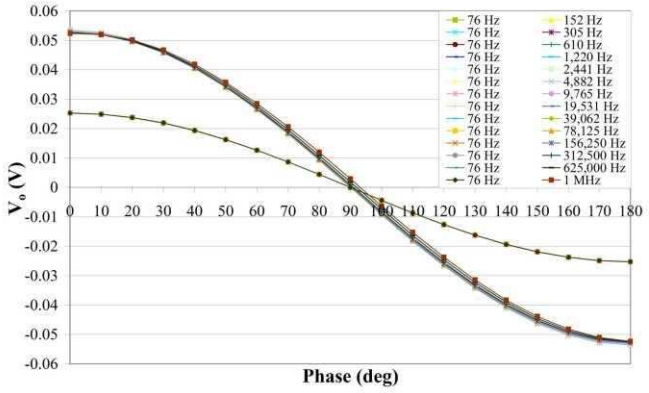

Fig. 10. Multi-frequency measurements. Two frequency signals were inputted to the system. The first frequency component was kept at 76 Hz and 25 mV. The second frequency component had constant amplitude of 53 mV and its frequency was varied from 152 Hz to 1 MHz.

detection [24]. Fig. 9 shows waveforms experimentally obtained from the fabricated chip when a multi-sine excitation is introduced to its inputs [Fig. 9(a)]. This is comprised of two frequency components: one at 25 mV, 76 Hz and one at 53 mV, 610 Hz. To illustrate the performance, this is demodulated by a 610 Hz signal 0° [Fig. 9(b)] and 90° [Fig. 9(c)] out of phase and chopped at 10 kHz. Fig. 10 shows the results obtained, as the phase relationship between input and demodulation signals of each frequency component is altered between 0° and 180°. The first frequency component was kept constant at 25 mV, 76 Hz signal, while the second one had a constant 53 mV amplitude but a varying frequency (from 152 Hz to 1 MHz).

C. RC Circuit Measurement

The chip was used with a custom current driver chip (a low current version of [16]) to perform tetrapolar impedance mea-surements. The Bode plots of the magnitude and phase of the output current of the current driver (set to deliver 20 μ A) are shown in Fig. 11(a) and (b), respectively. An RC circuit [10] comprised of a 200 Ω resistor in series with the parallel combination of a 45 nF capacitor and a 5 kΩ resistor, was

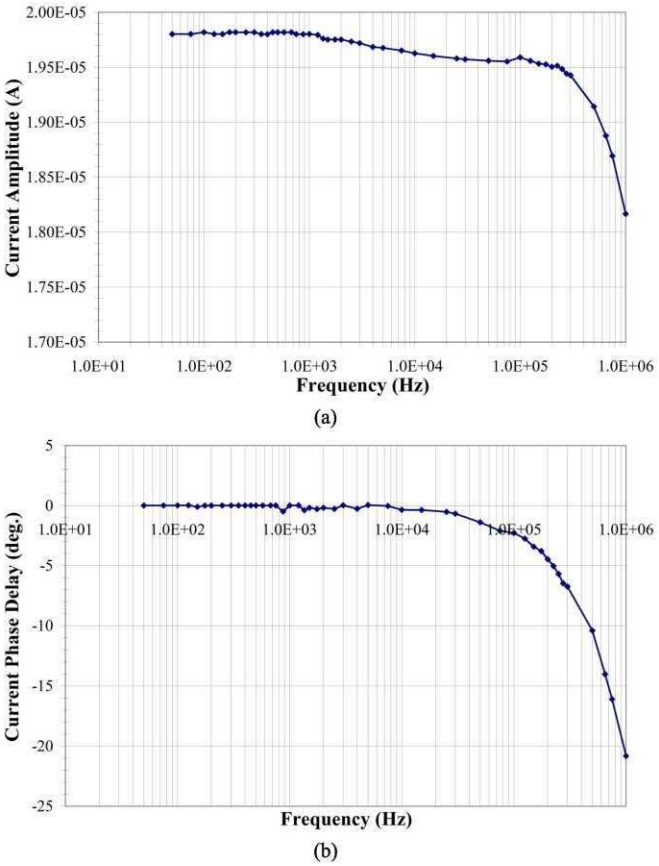

Fig. 11. (a) Magnitude and (b) phase of the output current of the current driver versus frequency.

used as the test impedance. A 3 kΩ sense resistor was placed on each side of this load in order to continuously monitor the current, through an AD8253 IA as in [16]. Synchronization between the injecting and measuring sides is essential in SD and any delays should be minimized or compensated for by adjusting the 0° and 90° demodulation to accommodate the delay. The results of Fig. 11(b) were used in order to adjust the demodulation signal phase, while the results of Fig. 11(a) were subsequently used in order to divide the resulting dc voltage value and obtain the value of the impedance. The real and imaginary parts of the impedance measured using the fabricated chips as a function of frequency, are shown in Figs. 12 and 13, respectively. These are compared with the real and imaginary parts of the same load impedance measured using a Wayne Kerr 6500B impedance analyzer.

D. Skin Impedance Measurement

The system was used to measure the impedance of the back of the forearm of a healthy adult volunteer with hairy skin using a tetrapolar arrangement as in [25]. The electrodes used were the Ambu Blue Sensor BRS self-adhesive Ag/AgCl electrodes [26]. The electrode and skin contact size was L χ W =16 mm χ 19 mm, with an adhesive area of 269 mm^2. The adhesive, which comes into contact with the skin, is a solid gel, while the electrode carrier material is carbon-filled polyvinyl chloride. The core of the lead wire is made of carbon which, through a brass/polypropelene connector, is interfaced

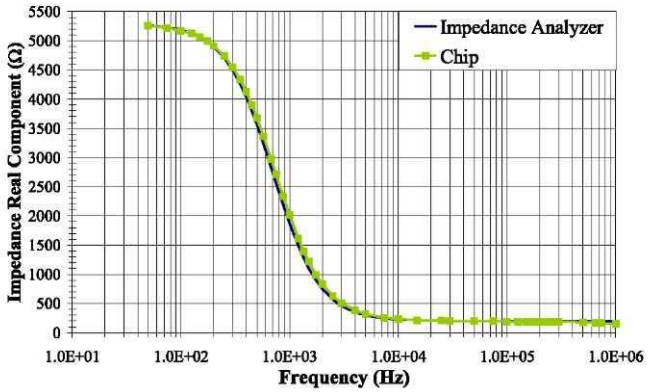

Fig. 12. Measured impedance real component versus frequency of the RC circuit characterized.

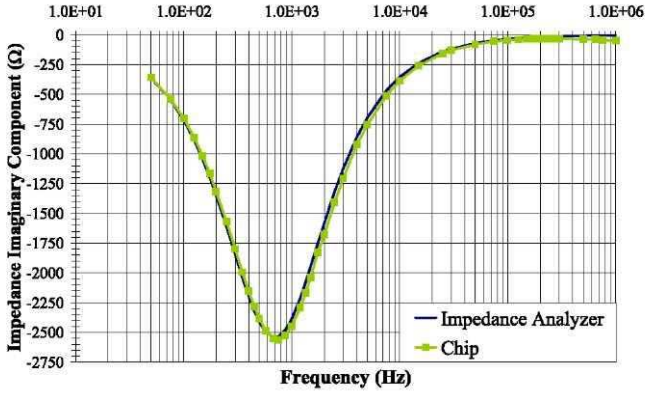

Fig. 13. Measured impedance imaginary component versus frequency of the RC circuit characterized.

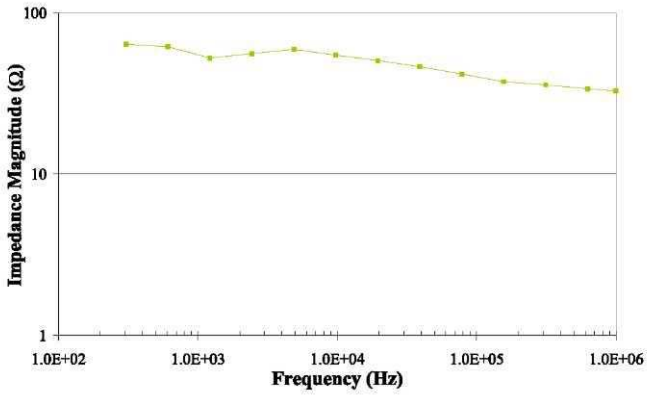

Fig. 14. Skin impedance measurement using the current driver and readout chip with commercially available skin electrodes from Ambu.

with the instrumentation. Fig. 14 shows the magnitude of the impedance as a function of frequency, obtained with the real and imaginary impedance components using the system designed. The results are plotted in a log-log scale to allow a visual comparison with the data presented in [25].

IV. Discussion

The measured results obtained from the fabricated analog readout chips show the performance of the system, indicating a good correlation with the theoretical (ideal) performance. Before performing tetrapolar measurements, the circuit was characterized with electrical test signals. The ideal response gives a result equal to 50 mV when the phase difference is 0° and 0 V when the phase difference is 90°. The measurement accuracy reduces as the frequency is increased and over the frequency of operation the mean measurement accuracy is about 95% (Table I). This is attributed to comparator non-idealities (such as delay and offset) and residual charge in the choppers (due to charge injection and clock feedthrough).

TABLE I

Summary of Measured Performance

Parameter	Value
Technology	0.35^mCMOS
Active area	1.525 mm^2
Supply voltage	±2.5 V
Power consumption per channel	3.4 mW
Max operational frequency	1 MHz
IA output dc offset	255μv±127μv
Measured impedance range	32 Ω < |Z| > 5.3 kQ
Mean measurement accuracy	

Fig. 5 clearly indicates the effect of the dc offset on the lock-in amplifier response. In this example a sinusoidal input signal of 50 mV at 100 kHz is applied to the system. After the chopping function is activated and performed with a signal of 10 kHz, the offset is removed and the results are corrected as is evident from Fig. 6. The IA output dc offset voltage is more clearly seen in Fig. 7 where the values obtained from all chips and channels examined are compared with and without chopping. The offset varies from 6.92 mV for the second channel of chip 5, down to 45.3 μV for the second channel of chip 3 without chopping. With chopping it varies from 3.67 mV down to 26.1 μV for the same chips and channels, giving an average value of 255 μY In all cases the offset is reduced. These are not input-referred values. The ability of the system to differentiate between the two frequency components is evident from the results in Fig. 10. The 76 Hz measurement through remains unaffected as the second frequency compo-nents is varied. The standard deviation of the 76 Hz data varies between 8.6 μV and 28 μY

According to Fig. 11(a), the output current varies by 1% up to 750 kHz and increases to 2.8% at 1 MHz. Knowledge of the current amplitude is required for calculating the impedance. The response of Fig. 11(b) indicates a phase delay of about 10° at 500 kHz increasing to 21° at 1 MHz. Knowledge of the phase is critical for applying the appropriate demodulation signals in the SD readout.

Having characterized the readout in detail and obtained the current driver characteristics, which are vital for the measurement, the two are combined in order to measure the RC circuit. It is evident from Figs 12 and 13 that theoretical and experimental data are in agreement. The measurement error is less than 1% for frequencies below 350 Hz and less than 4% at 100 kHz. For comparison, the integrated impedance measurement chips in [27] and [28] have an error of 10% at 250 Hz and at 1 kHz, respectively. In addition, both these designs are single-frequency systems. The nonlinearity of the measured impedance over the range of values in Figs 12 and 13 is below 2%.

Finally, the experimental results of Fig. 14 obtained using the fabricated chips and the skin electrodes, are in agreement with the results presented in [25]. Table I summarizes the key features of the chip.

V. Conclusion

This paper presented an integrated analog readout for multi-frequency bioimpedance measurements. The chip has been assessed in detail with the experimental results demonstrating its single- and multi-frequency performance to a level that, to the authors' knowledge, has not been presented before. The dc offsets of the IA have been minimized through the use of chopping. The paper has identified and compensated for phase errors between the two chopping stages and, more importantly, it has addressed phase issues between the demod-ulation signals and the current driver output, an error that is inherent in common SD topologies but rarely mentioned in the literature. Measurements of the impedance of an RC circuit and tissue have demonstrated good agreement with theoretical and published results. Future work involves the integration of the whole system on a single chip (current driver and readout) with additional features incorporated, such as signal generators and analog-to-digital conversion.

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