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Sulfuric acid and hydrogen peroxide surface passivation effects on AlGaN/GaN high electron mobility transistors

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In this work, we have compared SiN_x passivation, hydrogen peroxide, and sulfuric acid treatment on AlGaN/GaN HEMTs surface after full device fabrication on Si substrate. Both the chemical treatments resulted in the suppression of device pinch-off gate leakage current below 1 μA/mm, which is much lower than that for SiN_x passivation. The greatest suppression over the range of devices is observed with the sulfuric acid treatment. The device on/off current ratio is improved (from 10^4–10^5 to 10^7) and a reduction in the device sub-threshold (S.S.) slope (from ~215 to 90 mV/decade) is achieved. The sulfuric acid is believed to work by oxidizing the surface which has a strong passivating effect on the gate leakage current. The interface trap charge density (D_{it}) is reduced (from 4.86 to $0.90 \times 10^{12}\,cm^{-2}\,eV^{-1}$), calculated from the change in the device S.S. The gate surface leakage current mechanism is explained by combined Mott hopping conduction and Poole Frenkel models for both untreated and sulfuric acid treated devices. Combining the sulfuric acid treatment underneath the gate with the SiN_x passivation after full device fabrication results in the reduction of D_{it} and improves the surface related current collapse. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4904923]

I. INTRODUCTION

In recent years, GaN based AlGaN/GaN HEMTs have demonstrated excellent potential for power electronics owing to very favorable material properties such as high electron mobility, high 2DEG concentration, and a wide band gap for a large blocking voltage capability. However, due to the presence of surface states, devices generally suffer from DC to RF dispersion, otherwise known as current collapse.[1–3] This effect can severely limit the HEMT switching performance in power electronics applications. Additionally, for practical power applications at high operating voltages, it is very important to reduce the gate leakage current in the blocking state.

There have been several successful demonstrations of the suppression of surface related current collapse by depositing different dielectric layers such as SiN_x, SiO_2, AlN, HfO_2, and Al_2O_3.[4–8] SiN_x deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) is generally effective and widely used as a passivation technique and also serves to support field plates for high voltage operation,[9] but the surface leakage can be dependent on the prior chemical state of the surface and the details of the deposition conditions. In the past, hydrogen peroxide (H_2O_2) treatment on the AlGaN surface was shown[10] to reduce the gate leakage current, but no detailed studies on surface leakage mechanisms were conducted.

In this work, we have compared SiN_x passivation, hydrogen peroxide (H_2O_2), and sulfuric acid (H_2SO_4) treatment on GaN/AlGaN/GaN surfaces after full device fabrication (post-gate metal deposition). We have identified the surface conduction mechanisms and suggest an optimum combination of surface treatment and SiN_x to achieve a good combination of reduced current collapse and low gate leakage.

II. RESULTS AND DISCUSSION

The wafers were grown by metal organic chemical vapor deposition on 6-in. Si substrates. To facilitate the growth on the Si substrate, a nucleation layer of AlN (250 nm) was used together with a series of compositionally graded Fe-doped AlGaN layers and GaN layers. A 12 nm thick AlN layer was inserted between the Fe-doped region and the unintentionally doped GaN channel region (1.9 μm). A 1 nm mobility enhancement AlN layer was grown on the channel layer and an $Al_{0.28}Ga_{0.78}N$ barrier layer of thickness 27 nm grown on top of that. Finally, the wafer was capped with a 2 nm undoped GaN layer. A standard device fabrication procedure was followed with mesa isolation achieved by inductively coupled plasma etching. The ohmic contacts used Ti/Al/Ti/Au (20 nm/100 nm/45 nm/55 nm) metal stacks which were annealed at 850 °C for 30 s. The 1 μm long Ni/Au (20 nm/140 nm) gate was deposited symmetrically between the source-drain contacts (7 μm separation). Finally, Ti/Au (20 nm/200 nm) bond pads were deposited to allow electrical probing of the devices. The contact resistance and sheet resistance extracted from the transmission line measurement are 0.8 Ω mm and 400 Ω/sq, respectively. Hall measurements

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yielded a mobility of 2036 $cm^2\ V^{-1}\ s^{-1}$ and 2DEG density of $6.9 \times 10^{12}\ cm^{-2}$. Chemical treatments of post-processed devices were carried out by exposure to H_2O_2 (30% concentrated) or H_2SO_4 (98% concentrated) solutions for ~48 h at room temperature (we did not do a systematic study of the effect of treatment time and temperature but the large treatment time compared to that used in Ref. 10 was thought to be due to the relative stability of the oxides of the GaN cap used in this work). The H_2SO_4 treatment was also performed pre-gate metal deposition. PECVD was used to deposit the 100 nm SiN_x passivation layers. (The PECVD SiN_x deposition conditions were: pressure 900 mTorr, temperature 300 °C, RF power 25 W, RF 13.56 MHz, and DC bias 7 V). Devices were measured before and after the treatment.

The gate transfer characteristics of AlGaN/GaN HEMT devices before and after 100 nm PECVD SiN_x post-gate metal passivation, H_2O_2 and H_2SO_4 post-gate metal treatment, and H_2SO_4 pre-gate metal treatment are shown in Figure 1. Compared with SiN_x passivation, both chemical treatments resulted in much greater suppression of gate leakage current (<1 μA/mm), an improved sub-threshold slope (S.S.) and higher on/off current ratios (~10^7). Although the untreated devices showed a range of gate leakage currents, over the devices studied in this work, H_2SO_4 treatment was found to be the most effective in suppressing the gate leakage current and improving the S.S. Compared to other treatments, a noticeable reduction in peak drain current (from 647 to 427 mA/mm at $V_{GS} = +2$ V) is observed in the H_2SO_4 treated device together with a larger positive shift in threshold voltage. These results suggest that H_2SO_4 treatment oxidizes the surface and, in the process, consumes some of the barrier layer (AlGaN) which in turn reduces the 2DEG charge. Formation of an oxide layer on the surface has a strong passivating effect and reduces the overall gate leakage current.

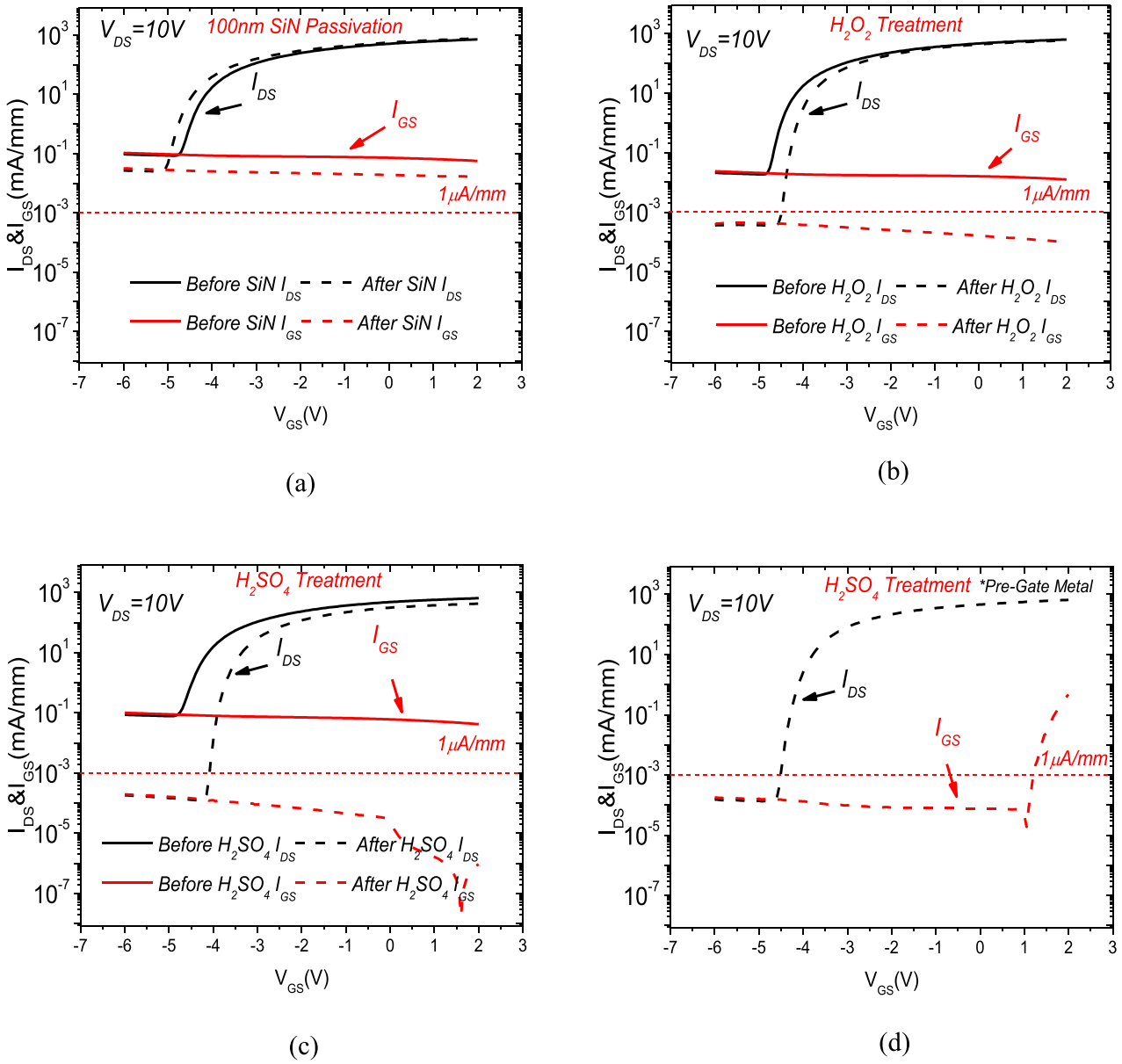


FIG. 1. Gate transfer characteristics of AlGaN/GaN HEMTs before and after (a) 100 nm SiN post-gate metal passivation, (b) H_2O_2 post-gate metal treatment, (c) H_2SO_4 post-gate metal treatment, and (d) H_2SO_4 pre-gate metal treatment.

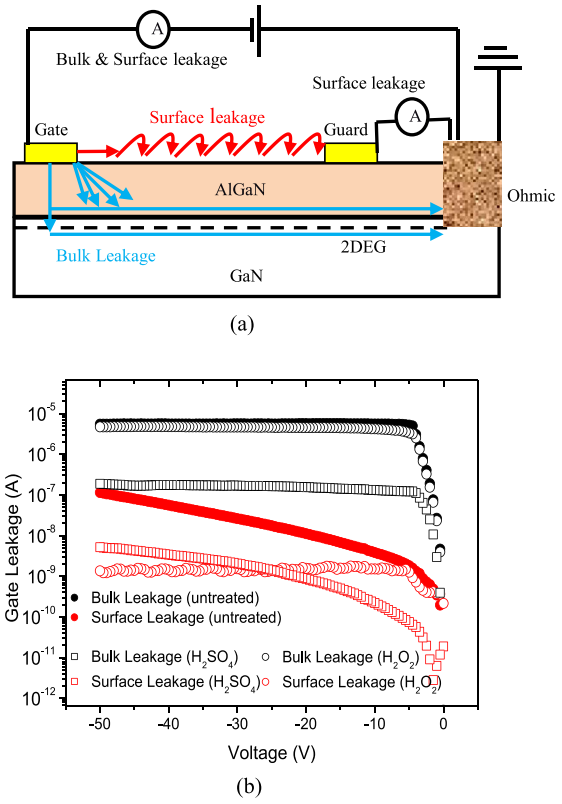


FIG. 2. (a) Surface leakage test structure circuit configuration showing gate bulk and surface leakage components. (b) Leakage currents measured from test structure after both H_2O_2 and H_2SO_4 chemical treatments.

In order to extract the interface trap charge density (D_{it}) from the S.S., we performed H_2SO_4 pre-gate metal treatment as shown in Figure 1(d) and an almost identical suppression in gate leakage is observed compared to treatment after the gate deposition. It is not possible to compare the same device in this case since H_2SO_4 treatment is performed pre-gate metal and variations in the electrical characteristics from device to device made it difficult to directly compare with and without treatment. However, the S.S. is reduced for a typical untreated device from 215 mV/decade to 90 mV/decade after the H_2SO_4 treatment. Using the expression for D_{it}[11]

$$D_{it} = \left(\frac{S.S.}{\ln(10)} \times \frac{q}{kT} - 1\right)\frac{C}{q^2}, \tag{1}$$

where q is electron charge, k is the Boltzmann constant, T is temperature in Kelvin, and C is the gate capacitance per unit area, we measure an equivalent reduction in D_{it} from 4.9 to $0.9 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ after H_2SO_4 treatment.

In order to measure the gate surface and bulk leakage (through the channel) components independently, a custom test structure incorporating a guard ring is used[12] as shown in Figure 2(a) and the results before and after the chemical treatments are shown in Figure 2(b). It can be seen that compared to untreated devices, both H_2SO_4 and H_2O_2 treatments are effective in suppressing the gate surface leakage component as expected. However, H_2SO_4 treatment also suppressed the gate bulk leakage component by a few orders of magnitude as shown in Figure 2(b). These results suggest that surface oxidization by H_2SO_4 treatment influences the overall gate bulk leakage through modification of the gate edge electron injection where the electric field is highest. The reduction in 2DEG charge will also reduce the peak electric field near the gate edge.

We have selected the H_2SO_4 treated devices for further detailed study of the gate surface leakage mechanism and compared it with the untreated device. The Arrhenius plots are shown in Figures 3(a) and 3(b) with activation energies extracted from the gate surface leakage at different voltage biases for untreated and H_2SO_4 treated devices, respectively. For identification purposes, we have split the inverse temperature axis into two regions in the H_2SO_4 treated device (low and high temperatures).

For the untreated device, a straight line fit can be extended over most of the temperature regime and activation energies are measured in the range of ~0.26–0.31 eV, which agrees well with that reported in the literature.[12–14] Note that there is a departure from the straight line at low

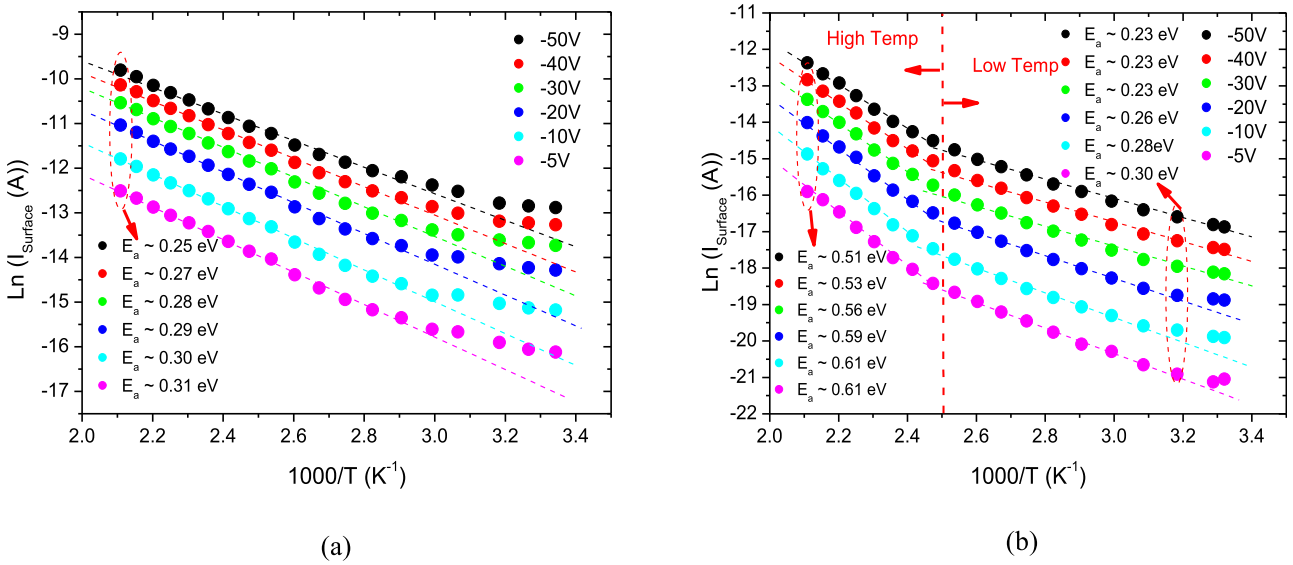


FIG. 3. Arrhenius plot with activation energies extracted from gate surface leakage component (a) for untreated device and (b) for H_2SO_4 treated device.

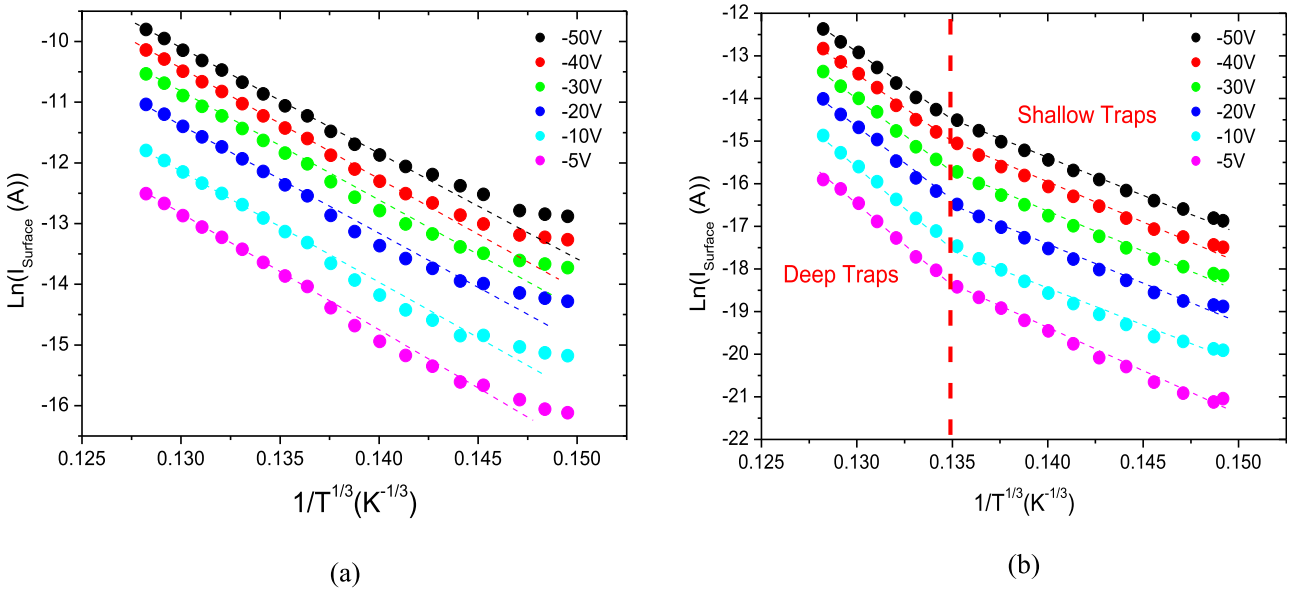


FIG. 4. Mott's hopping conduction model plot of surface leakage with 1/T1/3 temperature dependence (a) for untreated device and (b) for H_2SO_4 treated device.

temperatures. The reason for this is unclear but it may indicate the onset of the domination of states with much smaller activation energies. However, for the H_2SO_4 treated device, two distinct slope regions can be seen. In the lower temperature region (<130 °C), the activation energy is similar to the untreated device, but at higher temperature (>130 °C) it has increased to around ~0.5–0.6 eV. For both cases, the activation energy reduces with an increase in applied voltage. The clear dependence of surface leakage current on temperature rules out a tunneling mechanism. A two-dimensional variable range Mott hopping conduction model (2D-VRH) was used to analyze the data. The temperature dependent conductivity, σ, is given by the Mott expression[15,16]

$$\sigma(T)\alpha \exp\ [-(1/T)^{1/3}], \tag{2}$$

where T is the temperature in Kelvin.

Plots of surface leakage current versus $1/T^{1/3}$ are shown for both the untreated and H_2SO_4 treated devices in Figures 4(a) and 4(b), respectively. A good fit of the surface leakage current with the 2D-VRH model is obtained. In contrast to the untreated device, two distinct fits in the H_2SO_4 treated device suggest that at the lower temperature range (<130 °C) electron hopping along the surface states is via shallow states and in the higher temperature (>130 °C) range effects from electrons trapped in the deeper states are also introduced. These results indicate that even though H_2SO_4 treatment has reduced the interface trap charge density (D_{it}), in turn reducing gate leakage current, it has introduced some deeper level electron traps on the surface.

To understand the dependence of activation energy on applied voltage, Poole-Frenkel behavior[17] was considered. The observed exponential dependence of surface leakage

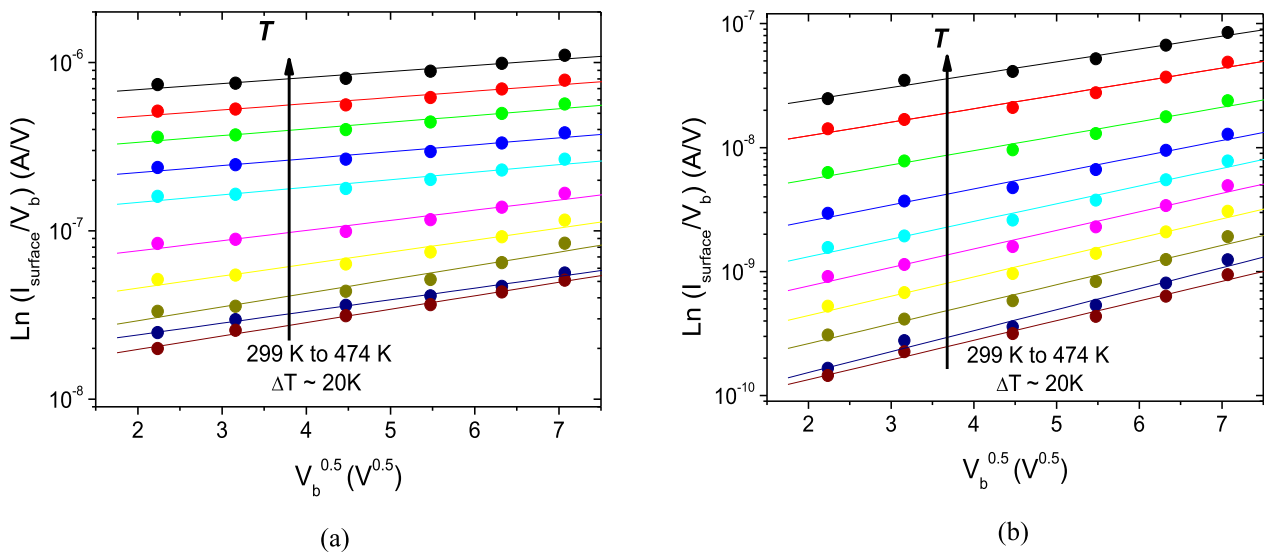


FIG. 5. Plot of log (Isurface/Vb) versus square root of applied voltage (Vb) at different temperatures (a) for an untreated device and (b) for an H_2SO_4 treated device.

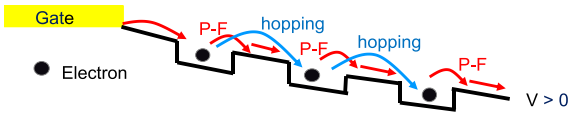


FIG. 6. Gate surface leakage mechanism along the surface states explained by combined effect of hopping conduction (blue) and Poole-Frenkel (red) behavior.

current with the square root of applied voltage (V_b), a characteristic of Poole-Frenkel emission, was plotted with different temperatures for both the untreated and H_2SO_4 treated devices as shown in Figures 5(a) and 5(b), respectively. These excellent straight line fits suggest that a hopping conduction model combined with Poole-Frenkel emission is responsible for the surface leakage mechanism. The proposed model is shown in Figure 6.

Extrapolated values of activation energy to zero bias from the plots of Figure 3 are shown in Figure 7. The zero bias activation energy values are a measure of the trap depth in the absence of any applied electric field. For the untreated device, the activation energy is 0.33 eV, which is in good agreement with the low-bias Arrhenius plots of Figure 3 and the trap depths reported previously.[12–14] However, for the H_2SO_4 treated device, the activation energy is very similar at low temperatures (0.3 eV) but increases significantly to 0.68 eV at high temperatures. This again highlights the fact that the H_2SO_4 treatment has introduced some deep level traps in the surface states.

The presence of deep level surface states can be catastrophic as electrons get trapped in the surface states under normal switching conditions causing a reduction in the total available drain current (current collapse) due to their sluggish response to changing bias. Therefore, to reduce the charge trapping effects and gate leakage and to improve the S.S., H_2SO_4 pre-gate metal treatment is combined with 100 nm PECVD SiN_x surface passivation and the results are shown in Figure 8. This optimum configuration sustains a

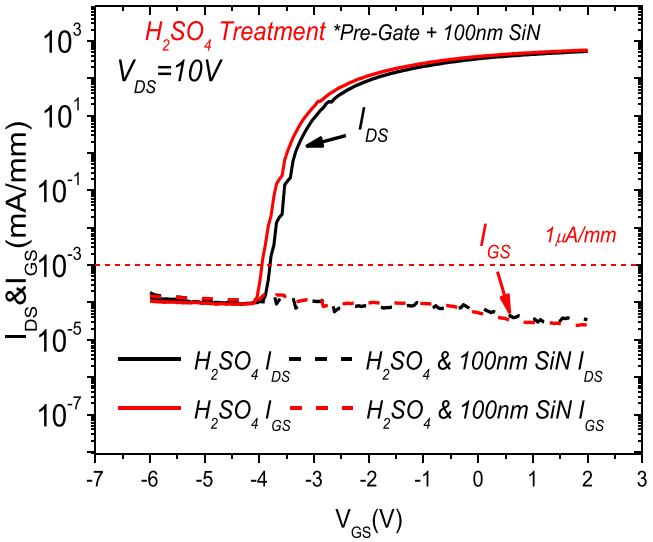
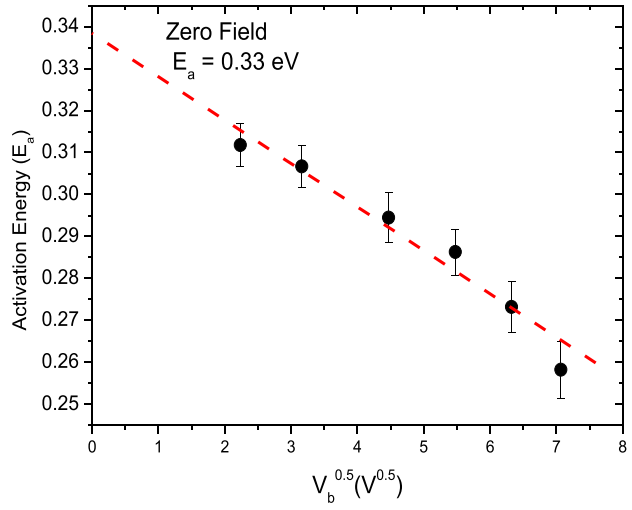


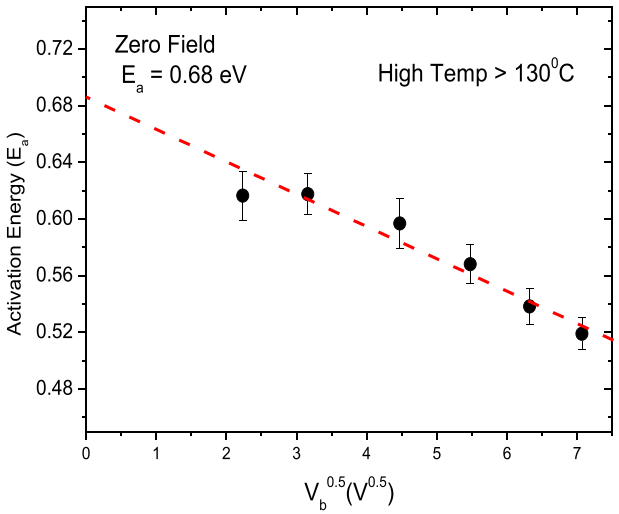
FIG. 8. Gate transfer characteristics of AlGaN/GaN HEMTs with H_2SO_4 treatment combined with 100 nm SiN passivation. The black curves are for pre-gate metal treatment and the red curves are for treatment after gate metal deposition. In both cases the SiN was deposited after the gate metal.

low gate leakage (<1 μA/mm) with reduced sub-threshold slope (100 ± 10 mV/dec).

To characterize the charge trapping along the surface, single pulse gate lag measurements were performed. In the pulse measurements, the device was biased by a dc voltage source in the off-state below the gate pinch-off voltage (−6 V), and then the gate is turned on by a short duration pulse (~400 ns) during which the drain current flows and its magnitude is measured. The gate lag is the ratio of pulse to dc drain current at fixed drain-source bias (V_{DS} = 10 V) and the results are shown in Figure 9. A low gate lag ratio of 0.4 ± 0.2 is measured in the H_2SO_4 treated devices, showing that the treatment is not effective in mitigating the current collapse. This may be due to the presence of the 0.3 eV and 0.68 eV states



(a)



(b)

FIG. 7. Extrapolated values of activation energy to zero bias plotted against the square root of voltage for (a) untreated device and (b) H_2SO_4 treated device at high temperatures (>130 °C).

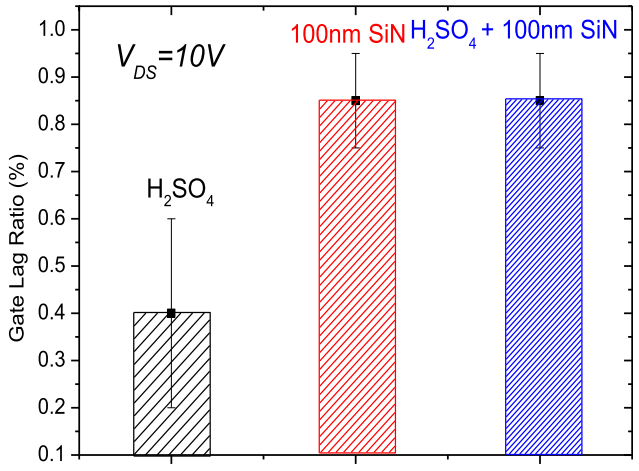


FIG. 9. Gate lag ratio (%) of AlGaN/GaN HEMTs with H_2SO_4 treatment, 100 nm SiN passivation and combined H_2SO_4 treatment with SiN passivation.

which act as electron traps and hence lead to the formation of virtual gate. However, with the addition of the 100 nm SiN_x passivation, the gate lag ratio is drastically improved to 0.85 ± 0.1.

III. CONCLUSION

We have demonstrated that the H_2SO_4 treatment is more effective in reducing the gate leakage compared to H_2O_2 when using a GaN cap layer. The surface oxidization by the H_2SO_4 treatment has a strong passivating effect and reduces the overall gate leakage current. The chemical treatment can form a very effective and easy method to reduce high gate leakage currents in GaN/AlGaN/GaN HEMTs. After the treatment, the device sub-threshold slope is significantly reduced due to a reduction in the interface trap charge density. The surface leakage mechanism is explained by a combined Mott hopping conduction and Poole-Frenkel model. After the H_2SO_4 treatment, some deep level traps are introduced along the surface states resulting in current collapse. Therefore, an optimized H_2SO_4 treatment plus a SiN_x passivation is required to reduce the surface trap charge density and current collapse whilst maintaining low gate leakage with improved sub-threshold slope.

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[1]R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," IEEE Trans. Electron Devices **48**(3), 560–566 (2001).
[2]S. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," IEEE Trans. Electron Devices **48**(3), 465–471 (2001).
[3]T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," IEEE Trans. Electron Devices **50**(10), 2015–2020 (2003).
[4]B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, and L. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," IEEE Electron Device Lett. **21**(6), 268–270 (2000).
[5]M. Ha, S. Lee, J. Park, J. Her, K. Seo, and M. Han, "Silicon dioxide passivation of AlGaN/GaN HEMTs for high breakdown voltage," in *Proceedings of the 18th International Symposium on Power Semiconductor Device and ICs* (2006), pp. 1–4.
[6]S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. Chen, "Effective passivation of AlGaN/GaN HEMTs by ALD-grown AlN thin film," IEEE Electron Device Lett. **33**(4), 516–518 (2012).
[7]C. Liu, E. F. Chor, and L. S. Tan, "Investigations of HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors," Appl. Phys. Lett. **88**(9), 173504 (2006).
[8]D. S. Lee, O. Laboutin, Y. Cao, W. Johnson, E. Beam, A. Ketterson, M. Shuette, P. Saunier, and T. Palacios, "Impact of Al_2O_3 passivation thickness in highly-scaled GaN HEMTs," IEEE Electron Devices Lett. **33**(7), 976–978 (2012).
[9]N. Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. Denbaars, and U. K. Mishra, "High breakdown in GaN HEMT with overlapping gate structure," IEEE Electron Device Lett. **21**(9), 421–423 (2000).
[10]H. Y. Liu, B. Y. Chou, W. C. Hsu, C. S. Lee, and C. S. Ho, "Novel oxide-passivated AlGaN/GaN HEMT by using hydrogen peroxide treatment," IEEE Trans. Electron Devices **58**(12), 4430–4433 (2011).
[11]S. M. Sze, *Physics of Semiconductor Devices*, 3rd ed. (John Wiley and Sons, 2006).
[12]W. S. Tan, M. J. Uren, P. A. Houston, R. T. Green, R. S. Balmer, and T. Martin, "Surface leakage currents in SiN_x passivated AlGaN/GaN HFETs," IEEE Electron Device Lett. **27**(1), 1–3 (2006).
[13]R. Dietrich *et al.*, "Effect of illumination on the electrical characteristics of AlGaN/GaN FETs," Phys. Status Solidi A **176**(1), 209–212 (1999).
[14]G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of SiN passivation and UV illumination," IEEE Trans. Electron Devices **50**(4), 886–893 (2003).
[15]N. F. Mott and E. A. Davis, *Electronic Process in Non-Crystalline Materials*, 2nd ed. (Oxford University Press, 1979).
[16]J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, "Mechanism of surface conduction in the vicinity of Schottky gates on AlGaN GaN heterostructures," Appl. Phys. Lett. **91**(9), 093501 (2007).
[17]O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," J. Appl. Phys. **95**(11), 6414–6419 (2004).