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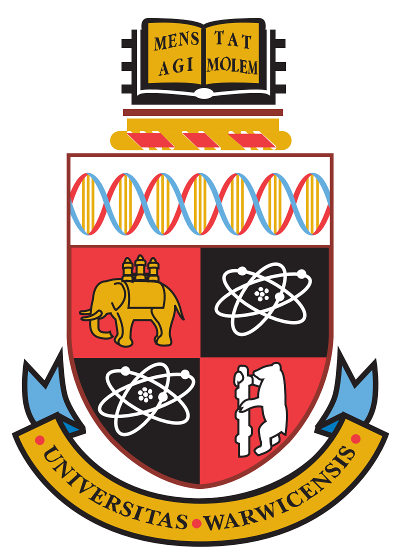
Development of 4H-SiC Power MOSFETs for High Voltage Applications



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Dissertation submitted for the degree of

Doctor of Philosophy

September 2015

Contents

Nomenclature **xviii**

1 Introduction **1**
1.1 Background 5
1.2 Silicon Carbide for Power Electronics 7
1.2.1 Polytypes of Silicon Carbide 8
1.2.2 Electrical and Physical Properties of Silicon Carbide 11
1.2.3 Material Defects and SiO_2/SiC Interface Problems 14
1.3 Current Status of Silicon Carbide Power Devices 18
1.4 Thesis Outline 20

2 High Voltage 4H-SiC Power MOSFETs **24**
2.1 The VD-MOSFET Cell Structure and Operation 24
2.2 Forward Conduction Characteristics 27
2.2.1 MOS Interface 32
2.2.2 Threshold Voltage 37
2.2.3 Work Function Difference 40
2.2.4 Oxide Charge 41
2.3 Off-state Breakdown Voltage 45
2.3.1 Edge Terminations 46
2.3.2 Junction Termination Extension 47
2.4 Power Vertical MOSFET On-Resistance 54
2.4.1 Channel Resistance 56
2.4.2 Accumulation Resistance 57
2.4.3 JFET Resistance 58
2.4.4 Drift Region Resistance 59
2.4.5 Total On-Resistance 61
2.5 SiC Oxidation Techniques 61
2.5.1 Thermal Oxidation Process 62
2.5.2 Novel High Temperature Oxidation 64
2.5.3 Post Oxidation Annealing 65

2.5.4 N_2O Grown Oxide . . . 66
2.6 Device Fabrication Technology . . . 66
2.6.1 SiC Etching . . . 67
2.6.2 Ion Implantation and Activation Annealing . . . 68
2.6.3 Ohmic Contacts to 4H-SiC . . . 69
2.7 Summary . . . 71

3 Design and Simulation of High Voltage 4H-SiC MOSFETs 72
3.1 4H-SiC Planar Power MOSFET Design . . . 73
3.1.1 Drift Layer Design . . . 79
3.1.2 Shielded Planar Inversion-Mode Structure . . . 81
3.1.3 Power VD-MOSFET Cell Optimisation . . . 84
3.1.3.1 Optimisation of JFET width . . . 84
3.2 Novel Junction Termination Extension (JTE) Design . . . 92
3.2.1 Space Modulated JTE . . . 96
3.2.2 Space Modulated Two Zones JTE . . . 101
3.2.3 Two-Steps MESA JTE . . . 103
3.3 Numerical Simulation of Shielded Planar VD-MOSFETs . . . 108
3.3.1 1 kV Inversion-Mode MOSFET . . . 108
3.3.1.1 On-State Characteristics . . . 109
3.3.1.2 Blocking Characteristics . . . 112
3.3.1.3 Shielded Planar VD-MOSFET with SMJTE structure . . . 117
3.3.2 3.3 kV Inversion-Mode MOSFET . . . 117
3.3.2.1 On-State Characteristics . . . 119
3.3.2.2 Blocking Characteristics . . . 122
3.3.2.3 Shielded Planar VD-MOSFET with SMJTE structure . . . 122
3.4 Summary . . . 125

4 Characterisation Techniques for High Voltage 4H-SiC Devices 128
4.1 Physical Characterisation . . . 128
4.1.1 Atomic Force Microscopy (AFM) . . . 129
4.1.2 Secondary Ion Mass Spectrometry (SIMS) . . . 131
4.2 Electrical Characterisation . . . 133
4.2.1 Capacitance-Voltage (C-V) Measurements . . . 134
4.2.1.1 Oxide Thickness . . . 134
4.2.1.2 Doping Concentration . . . 135
4.2.1.3 Flat-band Voltage . . . 136
4.2.1.4 Interface Trap Density . . . 137
4.2.2 Field-Effect Mobility . . . 141
4.2.3 Current-Voltage (I-V) Measurements . . . 142
4.2.4 Contact Resistance Measurements . . . 143

4.3 Summary 148

5 Fabrication Process Development for 4H-SiC Devices 150

5.1 Carbon Capping Layer 150

5.1.1 Fabrication Process 152

5.1.2 Effects on 4H-SiC Surface Roughness 153

5.1.3 Effects on 4H-SiC MOSFET Channel Mobility 159

5.2 Ion Implantation and Activation 162

5.3 Ohmic contact Study for 4H-SiC 165

5.3.1 Fabrication Process for TLM Structures 166

5.3.2 Electrical Characterisation Results 172

5.4 Summary 176

6 Fabrication and Characterisation of 4H-SiC MOS capacitors and Schottky diodes 179

6.1 4H-SiC MOS Capacitors Fabrication 179

6.1.1 N_2O Passivation and N_2O grown oxide 184

6.1.2 Phosphorous Passivation 186

6.1.3 Combined N_2O and Phosphorous Passivation 188

6.2 Interface Trap Density and Breakdown Characteristics 189

6.2.1 High Frequency Capacitance Method 189

6.2.2 Combined High-Low Frequency Capacitance Method 195

6.2.3 Breakdown Characteristics of N_2O and Phosphorous Annealed Oxides 202

6.3 4H-SiC Schottky Diodes with JTEs Fabrication 204

6.3.1 Photomask Design 204

6.3.2 Fabrication Process 205

6.3.3 Reverse I-V Characterisation Results 208

6.4 Summary 213

7 Fabrication and Characterisation of 4H-SiC Lateral MOSFETs 215

7.1 Photomask Design 216

7.2 Fabrication Process 218

7.3 First Generation 4H-SiC Lateral MOSFETs 226

7.3.1 Effect of High Temperature Oxidation 227

7.3.2 N_2O Post Oxidation Annealing and N_2O grown oxide 230

7.4 Second Generation 4H-SiC Lateral MOSFETs 236

7.4.1 Impact of Sacrificial Oxide Thickness on Channel Mobility 236

7.4.2 N_2O and The Novel Phosphorous Passivation 239

7.4.3 Oxide Breakdown Electric Field 244

7.5 Temperature Dependence of the Field Effect Mobility 245

7.6 Summary 250

8 Fabrication and Characterisation of 4H-SiC Vertical MOSFETs 253
8.1 Photomask Design . . . 254
8.2 Fabrication Process . . . 258
8.2.1 Challenges in the Fabrication Process . . . 261
8.3 First Generation of 4H-SiC Vertical MOSFETs . . . 268
8.3.1 SIMS Analysis . . . 269
8.3.2 Forward I-V Characterisation Results . . . 270
8.4 Second Generation of 4H-SiC Vertical MOSFETs . . . 274
8.4.1 Forward I-V Characterisation Results . . . 275
8.5 Summary . . . 279

9 Conclusions and Future Work 283
9.1 Conclusions . . . 283
9.2 Future Work . . . 292

A Vertical MOSFET Process Flow 296

B Silicon Carbide Device Cleaning Process 305
B.1 Organic Cleaning . . . 305
B.2 Piranha Cleaning . . . 306
B.3 RCA Cleaning . . . 306

C Standard Photolithography Processes 308
C.1 Positive Photoresist Process . . . 308
C.2 Negative Photoresist Process . . . 309
C.3 Thick Photoresist (AZ9260) Photolithography Process . . . 310

References 312

List of Figures

1.1 Sources of CO_2 emissions by sector (worldwide, 2009) [2]. 2
1.2 Application of discrete power semiconductors [3]. 3
1.3 Two types of tetrahedrons forming the building blocks of all SiC crystals. One type is obtained by rotating another type around its c-axis (vertical line here) by 180° [20]. 9
1.4 Three types (A, B and C) of SiC double-atomic layers arrangement along the c-axis (stacking direction) through close-packed spheres. [20]. 9
1.5 Polytypes of SiC [13]. 10
1.6 Theoretical limit of specific on-resistance against breakdown voltage for Si, 4H-SiC and GaN [25]. 13
1.7 Cross sectional view of a micropipe originating from the substrate and propagating into the epitaxial layer as shown in [27]. 15
1.8 Formation of dangling bonds at the interface between SiO_2 and semiconductor (SiC or Si) after thermal oxidation. 16

2.1 VD-MOSFET structure. 25
2.2 Lateral MOSFET showing the channel region with drain bias voltage less than the gate bias voltage (linear region) [44]. 28
2.3 Lateral MOSFET showing the channel region with drain bias voltage greater than the gate bias voltage (saturation region) [44]. 30
2.4 Typical output characteristics of a power VD-MOSFET [44]. 31
2.5 Metal oxide semiconductor capacitor. 32
2.6 Energy band diagram of a p-type MOS capacitor at the flat band condition [44]. 33
2.7 Energy band diagram of a p-type MOS capacitor under accumulation condition [44]. 35
2.8 Energy band diagram of a p-type MOS capacitor under depletion condition [44]. 36
2.9 Energy band diagram of a p-type MOS capacitor under inversion condition [44]. 37

2.10 Energy band diagram of a p-type MOS capacitor with negative work function difference [44]. 41
2.11 MOS structure showing various charges in the oxide and in the SiC interface 42
2.12 Band diagram of a p-type MOS capacitor with positive charge in the oxide. 44
2.13 Representation of vertical device showing active area, drift layer and the periphery without JTE termination. 47
2.14 Schematic view of vertical device with JTE termination. 49
2.15 Junction termination extension. 49
2.16 Junction termination extension with variable spacing between them. 52
2.17 Simulated electric field distribution for a 4H-SiC PiN diode with (a) single zone JTE structure and (b) SMJTE structure for JTE dose of 1×10^{13} cm^{-2} [59]. 53
2.18 Breakdown voltage versus JTE dose for 4H-SiC PiN diode with various JTE structures from the literature [59]. 53
2.19 Resistance and current path in the shield planar SiC power vertical MOSFET structure. 55
2.20 Power vertical MOSFET full-cell structure showing current paths in the drift region. 57

3.1 Electric field profile at breakdown for non-punch-through P-i-N diode structure. [44] 73
3.2 Breakdown voltage as a function of N- region doping concentration in both Si and 4H-SiC [44]. 76
3.3 Maximum depletion width versus of N- region doping concentration in both Si and 4H-SiC. [44]. 77
3.4 Critical electric field as a function of N- region doping concentration in both Si and 4H-SiC [44]. 77
3.5 Electric field profile at breakdown for punch-through P-i-N diode structure [44]. 78
3.6 Breakdown voltage as a function of doping concentration of 4H-SiC with different estimation methods. 80
3.7 Shielded planar inversion-mode power VD-MOSFET structure. 82
3.8 Simulation result of specific on-state resistance for 1 kV shielded planar VD-MOSFET with different width of JFET region. 85
3.9 Specific on-state resistance for the 1 kV shielded 4H-SiC shielded planar MOSFET structures from the analytical model calculations. 86
3.10 Simulation result of specific on-state resistance for 3.3 kV shielded planar VD-MOSFET with different width of JFET region from the analytical model calculations. 87

3.11 Simulation result of specific on-state resistance for 10 kV shielded planar VD-MOSFET with different width of JFET region from the analytical model calculations. 88
3.12 Simulated breakdown voltage of the 1 kV shielded planar VD-MOSFET structure with different JFET region width. 89
3.13 Potential contours for the shielded planar VD-MOSFET structure with JFET region width of 10 μm. 89
3.14 Potential contours for the shielded planar VD-MOSFET structure with JFET region width of 1 μm. 90
3.15 Breakdown voltage versus JFET doping concentration of 1 kV 4H-SiC shielded planar MOSFET. 91
3.16 Structure of 1 kV Schottky diode used in reverse breakdown simulations. . 93
3.17 Electric field distribution at breakdown of unterminated 1 kV mesa-isolated Schottky diode. 94
3.18 Schematic of Schottky diodes with single zone JTE structures. 94
3.19 Breakdown voltage versus range of JTE doping concentration for 4H-SiC Schottky diode with single zone JTE structure. 95
3.20 Schematic of Schottky diodes with SMJTE structures. 97
3.21 Comparison of breakdown voltage with various JTE doping concentration between SMJTE and Single zone JTE structures for 4H-SiC Schottky diode. 98
3.22 Effect of oxide charge on the breakdown voltage versus JTE doping concentrating of SMJTE structure for 4H-SiC Schottky diode. 99
3.23 Schematic of JTE structure with positive (left) and negative (right) oxide charge under reverse bias conditions. 100
3.24 Schematic of Schottky diodes with SM two zones JTE structures. 102
3.25 Breakdown voltage versus JTE doping concentration for 4H-SiC Schottky diode with single zone JTE, SMJTE and SM two zone JTE structures. . . 103
3.26 Schematic of (a) two-step mesa JTE and (b) two-step mesa with single implant JTE. 104
3.27 Simulated breakdown voltages as a function of etching depth D1 with various of D2 for two-step mesa JTE. 105
3.28 Schematic of (a) two-step mesa JTE and (b) two-step mesa with single implant JTE. 106
3.29 Breakdown voltage versus JTE doping concentration of Schottky diode with various of JTE structures. 107
3.30 1 kV shielded planar inversion-mode power MOSFET structure. 109
3.31 Transfer characteristic of 1 kV shielded planar VD-MOSFET. 110
3.32 Output characteristic of 1 kV shielded 4H-SiC planar VD-MOSFET. . . . 111
3.33 Lateral doping profile for the 1 kV shielded planar VD-MOSFET. 113
3.34 Potential contours profile for the 1 kV shielded planar VD-MOSFET. . . . 114

3.35 Breakdown electric field distribution for the 1 kV shielded planar VD-MOSFET. . . . 115
3.36 Electric field distribution for the 1 kV shielded planar VD-MOSFET through the JFET region. . . . 116
3.37 Breakdown characteristic of 1 kV shielded planar VD-MOSFET. . . . 116
3.38 Schematic of 1 kV shielded VD-MOSFET with SMJTE structure. . . . 118
3.39 The simulated breakdown voltage versus SMJTE doping concentration for the 1kV shielded VD-MOSFET. . . . 118
3.40 Schematic of 3.3 kV shielded planar inversion-mode power MOSFET. . . . 119
3.41 Transfer characteristic of 3.3 kV shielded planar VD-MOSFET. . . . 120
3.42 Output characteristic of 3.3 kV shielded planar VD-MOSFET. . . . 121
3.43 Breakdown electric field distribution of the 3.3 kV shielded planar VD-MOSFET. . . . 123
3.44 Breakdown characteristic of 3.3 kV shielded planar VD-MOSFET. . . . 123
3.45 The simulated breakdown voltage versus SMJTE doping concentration for the 3.3 kV shielded VD-MOSFET. . . . 125

4.1 Block diagram of atomic force microscope using beam deflection detection. 130
4.2 Secondary ion sputtering process of SIMS [110]. . . . 132
4.3 Schematic of a typical dynamic SIMS instrument [110]. . . . 133
4.4 $1/\mathrm{C}^2$ versus V_{G} plot used to determine the background concentration and built-in potential of a semiconductor junction. . . . 136
4.5 High frequency of $1/\left(C_{\mathrm{hf}}/C_{\mathrm{OX}}\right)^2$ versus gate voltage plot, and the differentiation of the curve showing the flat-band voltage V_{FB} [111]. . . . 137
4.6 Theoretical C-V curve (shown in black) compared with the C-V curve with interface trap (shown in red) [46]. . . . 139
4.7 High and low frequency C-V curves showing the offset of capacitance values due to interface traps. . . . 140
4.8 Cross-sectional schematic of semiconductor showing metallic contact on an implanted layer with associated resistances: metal resistance R_{m}, contact resistance R_{c} and semiconductor resistance R_{s}. . . . 144
4.9 Transfer length method test structures. . . . 144
4.10 Transfer length method plot of total resistance as a function of contact spacing. . . . 146
4.11 Transfer length method contact end resistance test structure. . . . 147

5.1 Carbolite CTF 18/300 high temperature advanced tube furnace. . . . 153
5.2 Graphite box and cap used for post-implantation annealing. . . . 154
5.3 Inductively Couple Plasma (ICP) etcher in the clean room. . . . 154
5.4 AFM scan on the original sample before annealing. . . . 155

5.5 AFM scan on the sample after annealing at 1650°C for 1 hour without carbon capping layer. 156
5.6 AFM scan on the sample after annealing at 1650°C for 1 hour with carbon capping layer. 156
5.7 The surface of 4H-SiC wafer after post-implantation annealing at 1600°C for 45 minutes. 157
5.8 AFM scan on the sample after annealing at 1700°C for 30 minutes with carbon capping layer. 158
5.9 Field effect mobility versus gate bias for lateral 4H-SiC MOSFETs with and without carbon capping layer [130]. 160
5.10 Field effect mobility versus gate bias for the fabricated 4H-SiC lateral MOSFETs with and without carbon capping layer. 161
5.11 Field effect mobility as a function of the gate bias for the fabricated 4H-SiC lateral MOSFETs at different post-implantation annealing temperature of 1650°C for 1 hour and 1600°C for 45 minutes. 165
5.12 Fabricated 4H-SiC TLM structures (all dimensions are in μm). 166
5.13 LPCVD system (Thermco Systems^{TM}) used to deposit SiO_2 on SiC. 167
5.14 Karl Suss MJB3 photo-mask aligner. 167
5.15 Electron Beam Evaporator Deposition system. 169
5.16 Rapid Thermal Annealing (RTA) furnace in the clean room. 169
5.17 Rectifying I-V characteristics of unannealed Ti/Ni ohmic contact scheme on n-type 4H-SiC (d1 to d6 refer to contact spacings as shown in Figure 5.12). 174
5.18 I-V characteristics of annealed Ti/Ni ohmic contact scheme (1000°C for 2 minutes) on n-type 4H-SiC (d1 to d6 refer to contact spacings as shown in Figure 5.12). 174
5.19 Surface morphology of TLM structures on n-type 4H-SiC with Ti/Ni metal scheme. 175

6.1 Photomask design for MOS capacitor fabrication with diameters of 1000, 600 and 400 μm. 180
6.2 High temperature oxidation furnace in the clean room. 181
6.3 Standard thermal oxidation at 1400°C to grow $\sim$ 50nm of SiO_2 on 4H-SiC. 182
6.4 Example of N_2O post oxidation annealing process at 1400°C for 1 hour. . . 185
6.5 Annealing furnace use for phosphorous passivation. 187
6.6 Schematic of process inside the PDS furnace. 188
6.7 Theoretical and ideal C-V curves for the MOS capacitor fabricated at 1400°C for 1 hour (taken at 1 MHz). 190
6.8 Theoretical and ideal C-V curves for the MOS capacitor fabricated with N_2O POA at 1300°C for 4 hours (taken at 1MHz). 191

6.9 Interface trap densities extracted using Terman method for MOS capacitors fabricated with different nitridation conditions. 192
6.10 Theoretical and ideal C-V curves for the MOS capacitor fabricated with phosphorous POA at 1000°C for 2 hours. 194
6.11 Interface trap density extracted using Terman method for MOS capacitors fabricated with N_2O POA, phosphorous POA and combined N_2O and phosphorous POA. 195
6.12 High-low frequencies capacitance measurement for MOS capacitor fabricated at 1400°C oxidation for 1 hour without POA. 196
6.13 High-low frequencies capacitance measurement for MOS capacitor fabricated with N_2O POA at 1300°C for 4 hours. 197
6.14 Interface trap densities extracted using high-low frequency capacitance method for MOS capacitors fabricated at various N_2O POA temperatures and time. 198
6.15 High-low frequencies capacitance measurement for MOS capacitor fabricated with phosphorous POA at 1000°C for 2 hours. 199
6.16 Interface trap density extracted using high-low frequency capacitance method for MOS capacitors fabricated with N_2O POA, phosphorous POA and combined N_2O and phosphorous POA. 200
6.17 I-V characteristics of MOS capacitors fabricated without POA, N_2O POA at 1300C 4 hours, phosphorous POA and combined N_2O and phosphorous POA. 203
6.18 Die design for Schottky diode fabrication. 205
6.19 High voltage breakdown test rig with power supply goes up to 20 kV. . . . 208
6.20 Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 3×10^{17} cm^{-3} (medium-dose JTE1). 210
6.21 Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 2×10^{17} cm^{-3} (low-dose JTE2). 211
6.22 Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 4×10^{17} cm^{-3} (high-dose JTE3). 212
6.23 Forward I-V characteristics of the 4H-SiC Schottky diodes. 212

7.1 Die design for lateral MOSFET fabrication. 217
7.2 Dimensions of lateral MOSFET structure (in μm). 217
7.3 Simulated implanted box-like profile for p-body region of lateral MOSFETs. 219
7.4 Simulated implanted retrograde profile in p-body region of lateral MOSFETs used in the second generation devices. 220
7.5 Simulated implanted box-like profile for source and drain regions of lateral MOSFETs. 221
7.6 Top view of the fabricated 4H-SiC lateral MOSFET from the microscope. . 226
7.7 Standard thermal oxidation at 1400°C to grow ~50 nm of SiO_2 on 4H-SiC. 228

7.8 Field effect mobility as a function of gate bias for the 4H-SiC lateral MOSFETs with thermal oxidation at 1500°C for 30 minutes and at 1400°C for 1 hour. 229
7.9 Transfer characteristic of lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions. 232
7.10 Field effect mobility versus gate voltage of lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions. 233
7.11 Field effect mobility versus gate bias for the lateral MOSFETs with different sacrificial oxide thickness. 237
7.12 Peak field effect mobility versus oxidation time of sacrificial oxide. 238
7.13 Field effect mobility against the gate bias for the 4H-SiC lateral MOSFETs after N_2O POA at 1300°C for 4 hours for different sacrificial oxide thickness. 240
7.14 Field effect mobility and the drain current against the gate bias for the first batch of lateral MOSFETs. 241
7.15 Field effect mobility and the drain current against the gate bias for the second batch of lateral MOSFETs. 242
7.16 Gate current density versus oxide electric field for the lateral MOSFETs with different POA conditions. 245
7.17 Variable temperature probe station set up in the clean room. 246
7.18 Field effect mobility versus the gate bias for the lateral MOSFETs with phosphorous POA at 1000°C for 2 hours under different temperatures. . . . 247
7.19 Field effect mobility versus the gate bias for the lateral MOSFETs with N_2O POA at 1300°C for 4 hours under different temperatures. 247
7.20 Temperature dependence of the field effect mobility for the 4H-SiC MOSFETs with no POA, N_2O POA and phosphorous POA treatments. 248

8.1 Mask plate design overview of the vertical MOSFETs. 256
8.2 Die design for the vertical MOSFETs with 2 μm channel length 256
8.3 Die design for the vertical MOSFETs with 5 μm channel length 257
8.4 Fabricated SiC single finger vertical MOSFETs. 260
8.5 Fabricated SiC multi-fingers vertical MOSFETs. 260
8.6 Suss MicroTec MA/BA8 mask aligner. 261
8.7 Alignment mark with gap of 2 μm before the P-well implantation. 262
8.8 Alignment mark after the P+ implantation with TEOS oxide on top. . . . 263
8.9 Small misalignment of multi fingers vertical MOSFETs after the lift-off process, which shows the source metal (grey colour) in contact with the gate metal (white colour). 264
8.10 Multi fingers vertical MOSFETs without misalignment between the source (grey colour) and the gate (white colour) metals. 264
8.11 Schematic view of photoresist patterns in the deep trench with (a) thin liquid resist (b) thick liquid resist. 266

8.12 Multi fingers vertical MOSFET source metal regions patterned using the standard photolithography process with S1818 photoresist. 266
8.13 Multi fingers vertical MOSFET source metals after lift-off process, which shows the peel off of metals in the trench regions. 267
8.14 Typical defect seen on the 4H-SiC material used in this work. 268
8.15 Experimental and simulated implanted aluminium retrograde doping profile for P-body region in 4H-SiC. 270
8.16 Experimental and simulated implanted nitrogen box-like doping profile for N+ source region in 4H-SiC. 271
8.17 Experimental and simulated implanted aluminium box-like doping profile for P+ region in 4H-SiC. 271
8.18 Output characteristics of small single cell vertical MOSFETs with 2 μm channel length. 272
8.19 Output characteristics of longer single cell vertical MOSFETs with 2 μm channel length. 273
8.20 Transfer characteristics of single cell vertical MOSFETs with 2 μm channel length. 274
8.21 Output characteristics of small single cell vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours. 275
8.22 Output characteristics of longer single cell vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours. 276
8.23 Transfer characteristics of single cell vertical MOSFETs with 2 μm channel length after N_2O POA at 1300°C for 4 hours. 277
8.24 Output characteristics of 0.1 A multi-fingers vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours. 279

List of Tables

1.1 Electrical properties of selected semiconductors at 300 K [21, 23, 24]. 12
1.2 Comparison of commercially available SiC MOSFETs from different manufacturers [8, 34–36]. 19
1.3 Comparison of commercially available full-SiC power module from different manufacturers [37–41]. 20

2.1 Typical High Voltage Junction Terminations used on Silicon devices. . . . 48

3.1 Dimensions of SMJTE design. Design parameters refer to those in Figure 3.20 (all dimensions in μm). The total JTE width is 600 μm, with the largest JTE region being 500 μm wide. 97
3.2 Dimensions of SM two zone JTE design. Design parameters refer to those in Figure 3.24, where dimensions of S4 to S7 and D5 to D7 are equal to S1 to S3 and D2 to D4 (all dimensions in μm). 102

5.1 Surface roughness values of a 4H-SiC sample at different annealing temperature and time both with and without carbon capping layer. 158
5.2 4H-SiC TLM fabrication process flow. 170

6.1 : 4H-SiC MOS capacitor fabrication process flow. 183
6.2 Ion implantation profiles for the JTE regions of 4H-SiC Schottky diodes, for low-dose (LD JTE2), medium-dose (MD JTE1) and high-dose (HD JTE3) 207

7.1 Ion implantations with the box-like doping profile and the retrograde doping profile. 219
7.2 4H-SiC lateral MOSFET fabrication process flow (not to scale). 222
7.3 Summary of first generation of 4H-SiC lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions. 231

A.1 Vertical MOSFET Process Flow. 297

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has not been submitted for a degree at any other University. The author wishes to declare that apart from commonly understood and accepted ideas, or where reference is made to the work of others, all of the work described in this thesis was carried out in the School of Engineering, University of Warwick from October 2011 until August 2015.

H. Rong
September 2015

Acknowledgements

Firstly, I would like to thank my PhD supervisor, Professor Philip Mawby, who has shown enormous support, guidance and faith in me throughout my PhD studies. I particularly appreciate the opportunity you gave me to work in this most high-tech electronics engineering environment at the University of Warwick, and to attend international conferences to present our work.

I would also like to thank my colleagues within the PEATER group, especially Dr. Yogesh Sharma, Dr. Craig Fisher and Dr. Mike Jennings for their useful advices and overall help. Their expertise in silicon carbide and devices fabrication were invaluable for this project. Thanks also go to Dr. Benedict Donnellan, for his kindly help with the finite element modelling problems I encountered in my first year of PhD studies, Dr. Dean Hamilton and Frank Courtney for their help on soldering and wire bonding of my devices, Dr. Stephen Thomas for his semiconductor knowledge and expertise in the cleanroom and Dr. Vishal Shah for his support in using the parameter analyser and the LCR meter.

Special thanks to Fan Li for his suggestions and many insightful conversations about my research, and his cooperation on building the high voltage test rig. I must also thank Dr. Mark Crouch for his expertise and support in the cleanroom, without whom the device fabrication work would not have been possible. Similarly, I must also thank Corinne Maltby and Dr Richard Jefferies for their cleanroom support.

Last but not least, I would like to thank my parents, for their unconditional love, encouragement and support in all that I have done. And I thank God for giving me joy, peace and guidance throughout my life.

Publications

1. H.Rong, Y.K.Sharma, T.Dai, F.Li, M.R.Jennings and P.A.Mawby "High Temperature Nitridation of 4H-SiC MOSFETs", Manuscript accepted for publication, *Materials Science Forum*, 2015.

2. H.Rong, Y.K.Sharma, F.Li, M.R.Jennings and P.A.Mawby "4H-SiC Diode Avalanche Breakdown Voltage Estimation by Simulation and Junction Termination Extension Analysis", *Materials Science Forum*, Vols. 778-780, pp. 824-827 (2014).

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Abstract

Silicon carbide is a promising wide bandgap semiconductor for high-power, high-temperature and high frequency devices, owing to its high breakdown electric field strength, high thermal conductivity and ability to grow high quality SiO_2 layers by thermal oxidation. Although the SiC power MOSFET (metal-oxide-semiconductor field effect transistor) is preferred as a power switch, it has suffered from low channel mobility with only single digit field effect mobility achieved using standard oxidation process (1200°C thermal oxidation). As such, this thesis is focussed on the development of 4H-SiC MOSFETs (both lateral and vertical MOSFETs) to improve the channel mobility and breakdown characteristics of these devices.

In this work, high temperature nitridation using N_2O has been investigated on MOS capacitors and MOSFETs, both with gate oxides grown directly in N_2O environment or in a O_2 ambient followed by a N_2O post-oxidation annealing process. Results have demonstrated that at high temperature (>1200°C) there is a significant improvement in the interface trap density to as low as (1.5×10^{11}cm^{-2}eV^{-1}) and field effect channel mobility (19 cm^2/V.s) of 4H-SiC MOSFET compare with a lower temperature (between 800 and 1200°C) oxidation (1×10^{12}cm^{-2}eV^{-1} and 4 cm^2/V.s). Nitridation temperatures of 1300°C was found to be the most effective method for increasing the field effect channel mobility and reducing threshold voltage. The number of working devices per sample also increased after N_2O nitridation at 1300°C as observed for both lateral and vertical MOSFETs. Other post oxidation techniques have also been investigated such as phosphorous passivation using solid SiP_2O_7 planar diffusion source (PDS). The peak value of the field effect mobility for 4H-SiC MOSFET after phosphorus passivation is approximately 80 cm^2/V.s, which is four times more than the valued obtained using high temperature N_2O annealing.

Different JTE structures have been designed and simulated including single-zone JTE, space modulated JTE (SMJTE) and the novel two-step mesa JTE structures. It was found that for the same doping concentration the SM two-zone JTE and SMJTE have higher breakdown voltage than the single zone JTE. With SMJTE, the device could achieve more than 90% of the ideal parallel plane voltage from simulations and 86% from the breakdown test of the fabricated devices.

Nomenclature

AFM	Atomic Force Microscopy
DAQ	Data Acquisition
FRD	Fast recovery diode
GaN	Gallium nitride
GTO	Gate turn-off thyristor
ICP	Inductively Coupled Plasma
IGBT	Insulated gate bipolar transistor
JFET	Junction Field Effect Transistor
JTE	Junction Termination Extension
LAGBs	Low-angle grain boundaries
LPCVD	Low pressure chemical vapour deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MZ-JTE	multiple zones Junction Termination Extension
PDS	Planar diffusion source
PDS	Planar diffusion source
POA	Post oxidation anneal
ppb	Parts-per-billion
ppm	Parts-per-million
PSG	Phosphosilicate glass
RCA	Radio Corporation of America
RIE	Reactive-Ion Etching
rpm	Revolutions per minute
RTA	Rapid thermal anneal
SCCM	Standard Cubic Centimeters per Minute
SCR	Silicon controlled rectifier
SEM	Scanning Electron Microscope
Si	Silicon
SiC	Silicon carbide

SIMS	Secondary Ion Mass Spectrometry
SMJTE	Space Modulated Junction Termination Extension
SMJTE	Space-modulated junction termination
SMU	Source Measuring Unit
TEOS	Tetraethyl Orthosilicate
TLM	Transmission line method
VD-MOSFET	Vertical Diffused Metal Oxide Semiconductor Field Effect Transistor

χ_{o}	Electron affinity of oxide (kJ/mol)
χ_{s}	Electron affinity of semiconductor (kJ/mol)
λ	Reduction of channel length with increasing drain bias (cm)
μ_{FE}	Field-effect mobility (cm^2/V.s)
μ_b	Bulk mobility (cm^2/V.s)
μ_{ni}	inversion layer mobility (cm^2/V.s)
μ_n	Charge carrier effective mobility (cm^2/V.s)
ϕ_{MS}	Metal-semiconductor work function difference (eV)
ϕ_{M}	Work function of metal (eV)
ϕ_{S}	Work function of semiconductor (eV)
ψ_{B}	Potential difference between intrinsic and Fermi level (V)
ψ_{S}	Surface potential (V)
ρ_{C}	Specific contact resistance (Ω/cm^2)
ρ_{D}	Resistivity of the drift region (Ω.m)
ρ_{JFET}	Resistivity of the JFET region (Ω.m)
A	MOS capacitor gate area (cm^2)
CF_4	Tetrafluoromethane
D_{it}	Interface Trap Density ($\mathrm{cm}^{-2}\mathrm{eV}^{-1}$)
NO	Nitric oxide
N_2O	Nitrous oxide
O_2	Oxygen
$\varepsilon_{\mathrm{OX}}$	Permittivity of the oxide (F/m)
ε_{S}	Permittivity of the semiconductor (F/m)
a	With of the drift region of power MOSFET (cm)
BV_{PP}	Breakdown voltage of P-i-N diode (V)
C_{hf}	High frequency capacitance (F)
C_{lf}	Low frequency capacitance (F)
C_{OX}	Oxide capacitance per unit area ($\mathrm{F/cm}^2$)
C_{S}	Semiconductor capacitance (F)
E_{cr}	Critical electric field of 4H-SiC (V/cm)
E_{C}	Energy of conduction band in the semiconductor (eV)
E_{FM}	Fermi energy position in metal (eV)

E_{FS}	Fermi energy position in semiconductor (eV)
E_{F}	Fermi energy position (eV)
E_{G}	Energy bandgap of semiconductor (eV)
E_{i}	Intrinsic energy position (eV)
E_{i}	Position of the intrinsic level (eV)
E_{m}	Maximum electric field (V/cm)
E_{S}	Semiconductor surface electric field (V/cm)
E_{T}	Energy of trap level in the semiconductor (eV)
E_{V}	Valence band in the semiconductor (eV)
I_{D}	Drain current of MOSFET (A)
k	The Boltzmann constant
L	Gate length (cm)
L_{D}	Extrinsic Debye length for holes (cm)
L_{JTE}	Length of JTE region (cm)
L_{T}	Transfer length of TLM (cm)
N_{DJ}	JFET region doping concentation (cm^{-3})
N_{D}	Drift layer doping concentration (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
P_{o}	Hole concentration (cm^{-3})
q	Charge of electron (C)
Q_{F}	Fixed oxide charge on MOS interface (F)
Q_{I}	Interface state charge on MOS interface (F)
Q_{Na}	Mobile ion charge on MOS interface (F)
Q_{OPT}	Optimum charge in the implanted JTE (F)
Q_{OX}	Total positive charge in the oxide (F)
Q_{S}	Total charge per unit area under strong inversion ($\mathrm{F/cm}^2$)
Q_{T}	Trapped charge on MOS interface (F)
Q_n	Local inversion layer charge density ($\mathrm{F/cm}^2$)
R_{A}	Accumulation region resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{CD}	Drain contact resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{ce}	End resistance of TLM (Ω)
R_{CH}	Channel region resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{CS}	Source contact resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{c}	Contact resistance (Ω)
R_{D}	Drift region resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{JFET}	JFET region resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{m}	Metal resistance (Ω)
$R_{\mathrm{N+}}$	Source region resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{ON}	Total on-resistance of power MOSFET ($\mathrm{m\Omega.cm}^2$)
R_{sh}	Sheet resistance (Ω)
R_{sk}	Sheet resistance under the contact and the transfer length of TLM (Ω)

R_{SUB}	Substrate resistance of power MOSFET (mΩ.cm^2)
R_{s}	Semiconductor resistance (Ω)
R_{T}	Total resistance (Ω)
T	Temperature in Kelvin (K)
t_{OX}	Oxide thickness (cm^2)
U_{F}	Normalised Fermi potential (V)
U_{S}	Normalised surface potential (V)
V_{D}	Drain to source voltage (V)
V_{FB}	Flat band voltage (V)
V_{G}	Gate to source voltage (V)
V_{TH}	Threshold voltage (V)
V_{bi}	Build-in potential of MOSFET (V)
W	Gate width (cm)
W_0	Zero-bias depletion width for the JFET region (cm)
W_{D}	Depletion width of the main juction of device (cm)
W_{J}	Width of JFET of VDMOSFET (cm)
W_{PP}	Maximum depletion width of P-i-N diode (V)
Z	MOSFET cell length in the orthogonal direction to the cross section (cm)

Chapter 1 Introduction

Top climate researchers have warned that global greenhouse gas emissions need to be reduced by at least sixty percent below the present levels by 2050 to avoid catastrophic climate change [1]. But such a radical reduction looks very challenging as the worlds energy needs are increasing day by day. One of the potential ways of mitigating CO_2 emissions is to upgrade our power distribution system, because the electricity sector produces about 40% of total global CO_2 emissions, followed by transportation at about 31% of the total as shown in Figure 1.1 [2]. Applying smart grid technologies can potentially reduce CO_2 emissions. The smart grid technologies include optimising the existing assets of overhead transmission lines, underground cables, transformers and substations, so as to minimise generation requirements in the future [2].

In this new technology, high-voltage semiconductor devices will play a crucial role in power electronic systems. Most of these applications today are built around silicon device

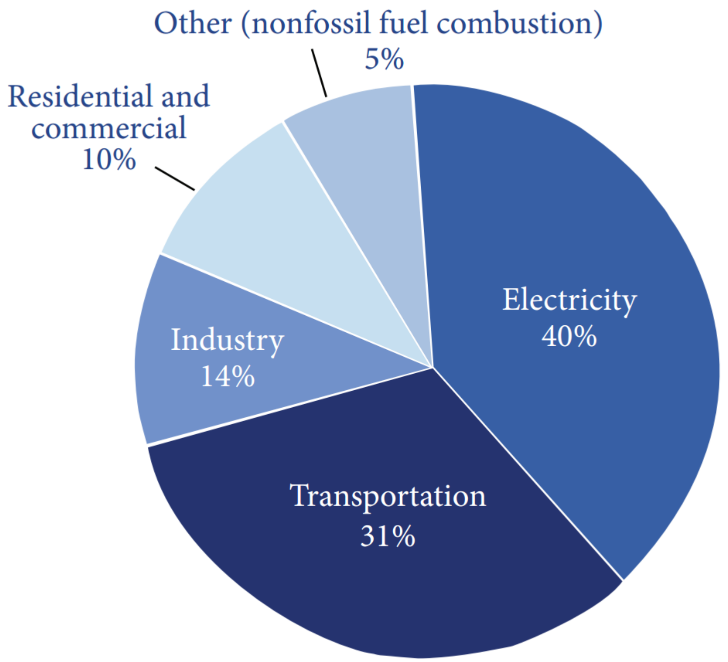


Figure 1.1: Sources of CO_2 emissions by sector (worldwide, 2009) [2].

technology. The superior properties of SiC power devices compared with Si are expected to have a significant impact on next-generation power systems. SiC power devices offer the potential for higher switching speeds, higher breakdown voltage, lower switching losses and a high junction temperature than traditional silicon-based switches. Figure 1.2 shows the application areas of discrete power semiconductors. It is seen that thyristors (SCR) are used for high-power applications (>1 MW). MOSFETs and IGBTs are mainly used for high frequency applications (>10 kHz).

There are two particular places in energy networks that existing technology and infrastructure needs radical change to move us to a low carbon economy and to meet the UK greenhouse emission reduction targets by 2050 [4]. The very "top" of the energy network is

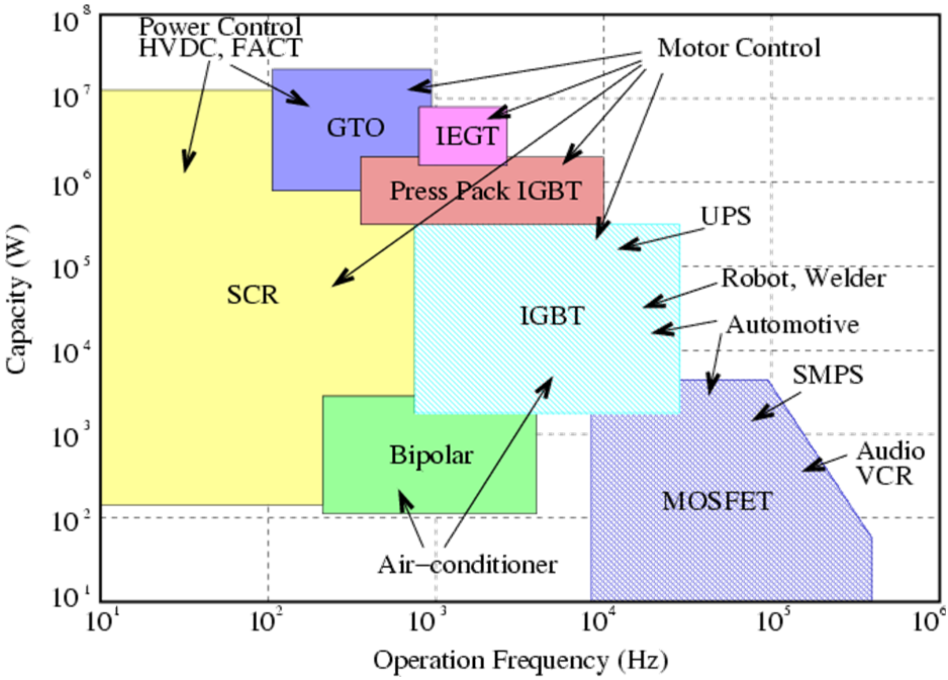


Figure 1.2: Application of discrete power semiconductors [3].

formed by the expected emergence of a transcontinental energy exchange in Europe (and elsewhere) that is driven by exploitation of diversity in renewable sources and diversity in load. The "tail" of the network is the so-called "last mile" and "behind the meter" wiring into customer premises. The work described here is focussed on the "top" of the network which investigates new approaches for super-scale capacity converters (GW levels) using novel semi-conductors materials, silicon carbide in particular.

The semiconductor switch is the fundamental building block of all power electronic converters. Current silicon switching devices such as IGBTs and integrated gate commutated thyristors (IGCT) are reaching their physical limits of power handling and switching frequency capabilities, and so a step change in technology is needed to move beyond this lim-

itation. Wide bandgap silicon carbide (SiC) is the most promising material alternative to silicon because of its superior properties including about ten times higher breakdown electric field, higher thermal conductivity and much lower intrinsic-carrier concentration [5]. These properties allow devices to have higher voltage ratings and higher operating temperatures compared to traditional silicon, which translates into smaller and less expensive components. 4H-SiC is particularly suited for vertical power devices compared with other polytypes of SiC because it has a higher mobility along the c-axis (direction normal to the Si-C double-atomic layers), higher critical electric field, and a mature growth technology.

Diamond is the ultimate candidate as a semiconductor theoretically, but its chemical strength and density make it very difficult to process compared to SiC. Gallium Nitride (GaN) is also a contender. However, it has a much lower thermal conductivity than Si. Silicon carbide semiconductor device technology has matured greatly over the past few years and has gone from research to commercial production. In particular, 4H-SiC Schottky barrier diodes, JFETs, and MOSFETs are commercially available, mainly for 600- to 1700- V applications [6–8]. However, for the advanced electric power network such as HVDC transmission, ultra-high-voltage (UHV) power devices with blocking voltage of 10 kV or more are required. These high voltage power devices based on silicon carbide will be a critical component in building a smart grid with distributed and fluctuating sources of power generation, which would result in a reduction in greenhouse gas emissions and imported energy. 4H-SiC bipolar devices, such as PiN diodes, BJTs and thyristors, can achieve lower static power loss than the unipolar devices in UHV (>10 kV) area due to

their large concentration of holes and electrons (conductivity modulation) [9–12]. The conductivity modulation reduces the on-state resistance of the drift region as long as the carrier lifetime in the material are sufficiently long; therefore reducing on-state power loss. However, the low carrier lifetime in 4H-SiC which is due to the lifetime-killing defects, such as $Z_{1/2}$ and $EH_{6/7}$ defects can be a problem for UHV bipolar devices [13]. Low carrier lifetime will result in a high on-state voltage drop due to insufficient conductivity modulation. The switching speeds of bipolar devices are also significantly slower than for unipolar devices because of the relatively slow process of electron-hole recombination. As a result, unipolar devices such as MOSFETs and Schottky barrier diodes (SBDs) usually use in low to medium blocking voltage applications, up to around 900 V for commercial Si MOSFETs and around 200 V for Si SBDs. However, if SiC devices is used, the voltage range of commercial MOSFETs and SBDs extends to 1700 V, with the potential for even greater voltage ratings in the future.

1.1 Background

The aim of this thesis is to design, fabricate and characterise 4H-SiC MOSFETs and MOS capacitors for high voltage (>10 kV) applications, with focus on optimising device performance, particularly on MOSFETs. This work studied the channel mobility and the oxide quality of 4H-SiC MOSFETs using novel high temperature nitridation and phosphorous passivation techniques. Also, of key interest is the reverse breakdown performance of

4H-SiC devices with different junction termination structures.

The design and fabrication of 4H-SiC power MOSFETs and MOS capacitors in this work was built on previous work carried out at the University of Warwick on the development of 4H-SiC PiN diodes for high voltage applications [13, 14]. One of the key issues in 4H-SiC device processing is the formation of ohmic contacts to both n-type and p-type 4H-SiC. The ohmic contacts to n-type and p-type 4H-SiC were achieved by using Ti(30 nm)/Ni(100 nm) and Ti(30 nm)/Al(90 nm) metallisation schemes and annealed at 1000°C for 2 minutes, which results in a specific contact resistance in the order of 10^{-6} $\Omega \cdot cm^2$ as shown by Fisher [13]. Therefore, it was logical to incorporate these findings into the fabrication of 4H-SiC power MOSFETs, especially the n-type ohmic contact which is more important for MOSFETs fabrication.

In addition, the introduction of a unique high temperature thermal oxidation furnace in the Science City cleanroom facility at Warwick, intended specifically for SiC device processing, has provided motivation for further research into high temperature fabrication processes for SiC devices. In terms of 4H-SiC MOSFET fabrication, the ability to perform high temperature oxidation and post oxidation annealing is of great interest as it can increase the channel mobility and oxide reliability by passivating the interface traps/defects at the SiC/SiO_2 interface, which are formed during the oxidation process. A standard passivation process at present is based on post-oxidation annealing in nitric oxide (NO) or nitrous oxide (N_2O) [15, 16]. These passivation anneals increase the channel mobility of a SiC MOSFETs from single digits ($\sim$1 cm^2/V.s) to around 20 to 30 cm^2/V.s depending on

whether the MOSFET was an ion-implanted or epitaxial P-body region. Direct growth of gate oxide by NO or N_2O nitridation has also been reported by some researchers [16, 17], but available data on high temperature (>1200°C) oxidation and nitridation on 4H-SiC (0001) MOSFETs and MOS capacitor is very limited. Most literature on SiC device fabrication only investigates thermal oxidation up to 1300°C, due to equipment limitations. The capabilities at Warwick allow investigation of thermal oxides grown at temperature up to 1600°C, with the aim of further improving the channel mobility as well as the oxide quality. In this work, a number of different oxidation and anneal processes (up to 1500°C), including the novel phosphorous passivation using the solid SiP_2O_7 planar diffusion source (PDS), have been investigated.

1.2 Silicon Carbide for Power Electronics

Silicon (Si) is currently the dominant base material for the fabrication of power semiconductor devices. High-quality monocrystalline Si is widely available at low cost, and its fabrication processes have been developed over many years which resulted in the successful development of both unipolar and bipolar devices. However, its physical property limits its operation for most modern applications which demand increasingly high power density and temperature. For such applications, the use of wide band gap semiconductor material is important and necessary. Among these materials, SiC is the only wide band gap material that can be thermally oxidised to form chemically and thermally stable silicon dioxide

(SiO_2), which is crucial for all MOS based power devices such as MOSFET. And its relative maturity compared to GaN and diamond makes it the prime candidate for replacing Si for high voltage power electronics applications. SiC devices provide several advantages over Si, such as higher breakdown voltage, higher operating temperature, higher switching frequency and lower losses. Although the price of SiC devices is still higher than Si, SiC devices are finding more applications where SiC technology can offer system advantages, which can offset the increased device cost. The cost of SiC substrates is also dropping while their qualities are improving as more companies and research institutions are becoming involved in SiC technology.

1.2.1 Polytypes of Silicon Carbide

Silicon carbide occurs in many different crystal structures, known as polytypes. A comprehensive introduction to SiC crystallography and polytypism can be found in [18,19]. In the crystalline form, each silicon atom is covalently bonded to four neighbouring carbon atoms to form a tetrahedron and vice versa as shown in Figure 1.3. There are two types of tetrahedrons in the SiC crystal, with one type is obtained by rotating another type around its c-axis by 180°.

Despite the fact that all SiC polytypes consist of an equal number of covalently bonded Si and C atoms, each polytype has its own distinct set of electrical properties. There are over 200 polytypes for SiC, but only a few are commonly grown in a reproducible form

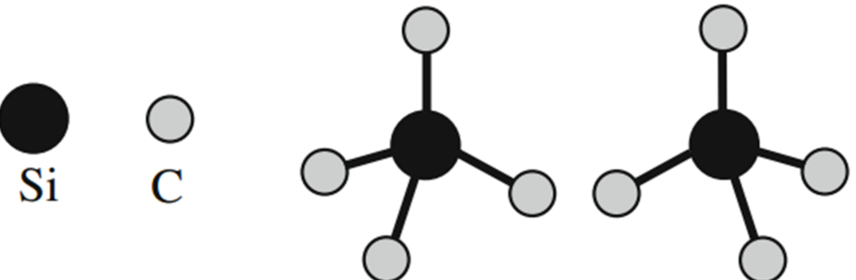


Figure 1.3: Two types of tetrahedrons forming the building blocks of all SiC crystals. One type is obtained by rotating another type around its c-axis (vertical line here) by 180° [20].

suitable for use as an electronic semiconductor. The most common polytypes of SiC presently being developed for electronics are the cubic 3C-SiC and the hexagonal 4H-SiC. These polytypes are characterised by the different stacking sequence of the double-atomic layers of SiC. In each layer, the silicon (or carbon) atoms have a close-packed hexagonal arrangement. There are three types of sites (named A, B and C) in arranging the SiC double-atomic layers as illustrated in Figure 1.4.

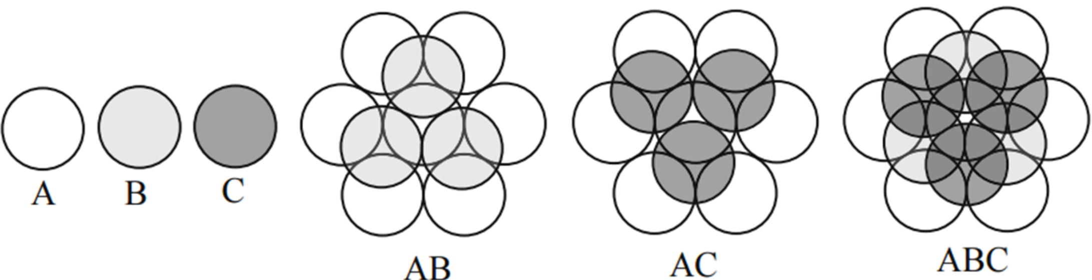


Figure 1.4: Three types (A, B and C) of SiC double-atomic layers arrangement along the c-axis (stacking direction) through close-packed spheres. [20].

The different stacking sequence of these double-atomic layers arrangements defines different polytypes of SiC. For example, in 3C-SiC, the stacking sequence of the double-

atomic layer is ABCABC. The letter C in 3C-SiC denotes the cubic crystal structure and 3 refers to the number of double-atomic layers in one repeating unit (ABC). For the 4H-SiC which is used in this work, the stacking sequence is ABCBABCB Similarly, the letter H in 4H-SiC refers to the hexagonal crystal structure and there are 4 double-atomic layers in one repeating unit (ABCB). The stacking sequences of the common SiC polytypes are illustrated in Figure 1.5.

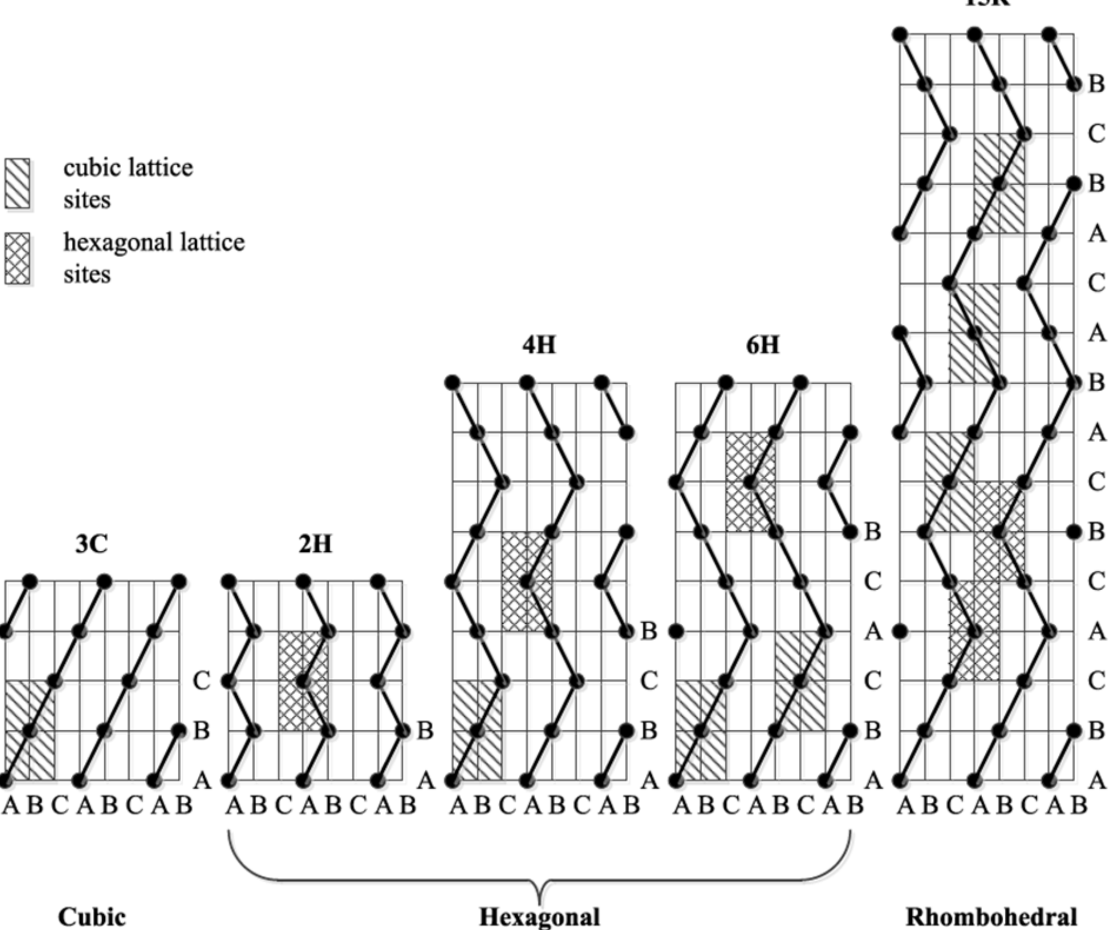


Figure 1.5: Polytypes of SiC [13].

It is seen that the stacking sequence of 4H-SiC consists of 1/2 hexagonal and 1/2 cubic sites. This is in contrast to the 6H-SiC polytype, which consists of 1/3 hexagonal and 2/3 cubic sites, more anisotropy in its material characteristics. It is this anisotropy in material characteristics, particularly the carrier mobility, that have led to 4H-SiC being preferred over 6H-SiC for power semiconductor devices in recent years [13]. The cubic nature of 3C-SiC has also gained great interest in recent years, as it can be grown on a substrate such as Si which offers a lower cost compare to 4H-SiC. However, its progress has been hampered by its low quality material.

1.2.2 Electrical and Physical Properties of Silicon Carbide

Silicon carbide (SiC) exhibits higher values of thermal conductivity (∼3 times), critical electric field (∼7 times) and saturated carrier velocity (∼2 times) compared to the conventional semiconductor material such as silicon and gallium arsenide [21]. Table 1.1 compares some of the key electrical properties of SiC and other semiconductor materials. It is seen that Si has significant larger intrinsic carrier concentration compared to the wide band gap semiconductors. It is this property that limits Si device operation temperature to around 150° [22]. The number of electron-hole pairs thermally generated at this temperature exceed the number of free carriers due to the intentional doping of the material, and at this point the material becomes intrinsic and the device fails. In contrast, the wide band gap and much lower intrinsic carrier concentration of SiC allows

Table 1.1: Electrical properties of selected semiconductors at 300 K [21, 23, 24].

Property	Units	**Si**	**3C-SiC**	**4H-SiC**	**GaN**	**C**
Bandgap Energy, E_G	eV	1.1	2.2	3.26	3.4	5.5
Critical Field, E_C	MV/cm	0.3	1.2	2.2	3.3	5.6
Int. Carrier Conc., n_i	cm^{-3}	$\sim10^{10}$	$\sim10^{0}$	$\sim10^{-8}$	$\sim10^{-10}$	$\sim10^{-27}$
Dielectric Constant, ε_r		11.8	9.6	9.7	9.9	5.5
Thermal Conductivity, λ	W/cm.K	1.5	4.5	4.5	1.3	20
Elec. Sat. Velocity, V_{sat}	10^7cm/s	1	2	2	2.5	2.7
Electron Mobility, μ_n	cm^{-3}	1350	900	720	1000	1900
Hole Mobility, μ_p	cm^{-3}	480	40	120	30	1200

it to reach temperature of around 700° before operating in the intrinsic region.

From the above comparison is also seen that the critical electric field for 4H-SiC is approximately ten times larger than that for Si. The value of critical electric field is related to the band gap energy of a semiconductor material; a wider band gap means it can support larger electric fields to be applied before avalanche breakdown occurs. The larger critical electric field strength of 4H-SiC compared to Si means that for the same drift region thickness, 4H-SiC can withstand about ten times the voltage before it breaks down. Figure 1.6 shows the theoretical limit of specific on-resistance against breakdown voltage for Si, 4H-SiC and GaN. It can be seen from this Figure that for the same breakdown voltage level, 4H-SiC devices offer much lower specific on-resistance (about 350 times) than their Si counterparts. Furthermore, the thinner drift regions of 4H-SiC means they can be operate at higher frequencies and lower switching losses. The thermal conductivity of 4H-SiC is also about three times higher than Si, which is another important advantage for power electronics applications since this can reduce the requirement for large, bulky

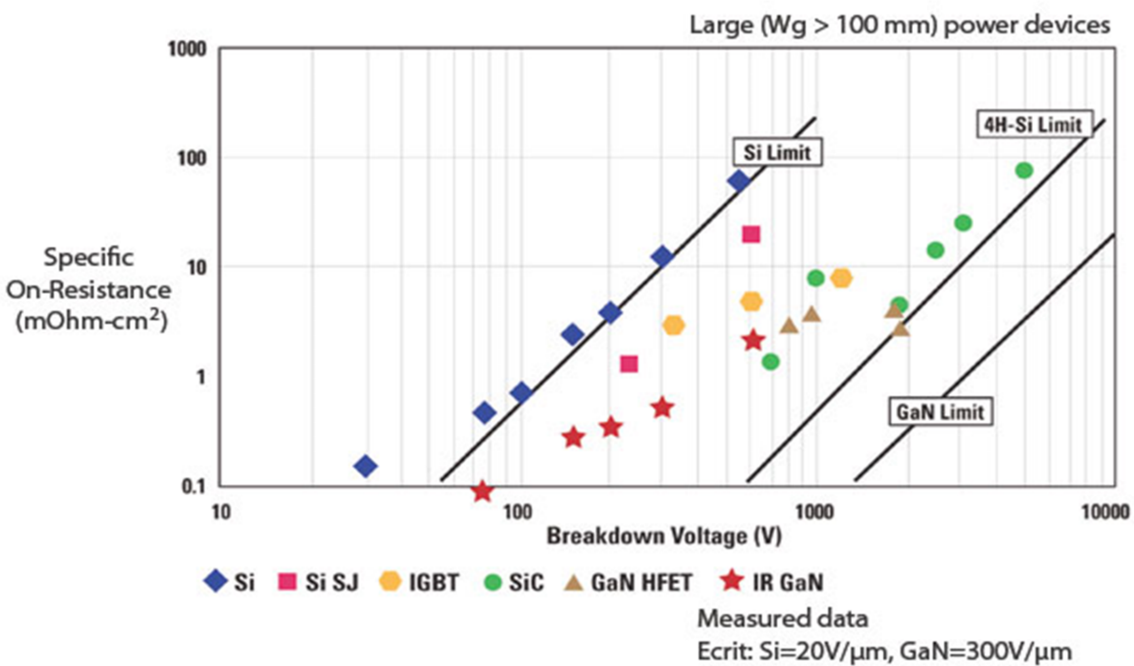


Figure 1.6: Theoretical limit of specific on-resistance against breakdown voltage for Si, 4H-SiC and GaN [25].

heat sinks and cooling apparatus.

One disadvantage of 4H-SiC when compared to Si as seen from Table 1.1 is the lower carrier mobility (both electrons and holes) in the material. A lower mobility corresponds to higher on-resistance and thus higher on-state losses. However, as mentioned previously, the 4H-SiC can have thinner, more highly doped drift region compared to Si, which can mitigate this disadvantage. It is important to note that the values for mobility outlined in Table 1.1 are for the bulk material, however for 4H-SiC MOS devices the surface mobility is significantly lower than in the bulk of the material due to the poor quality interface between 4H-SiC and SiO_2, which is discussed in more details in following Section. This low channel interface mobility leads to a high channel resistance and thus high on-state

losses.

1.2.3 Material Defects and SiO_2/SiC Interface Problems

Although significant progress has been made in the past two decades to reduce the defect density of SiC substrates, this is still the most critical challenge faced by SiC wafer technology, and is continuing to hinder the development of large area high current and high voltage devices. Defects in SiC include open-core dislocations (also called micropipes), low-angle grain boundaries and conventional dislocations. Micropipe defects were considered as preventing the commercialisation of many types of SiC devices, especially high current power devices [26]. Figure 1.7 illustrates a typical micropipe defect within SiC material used in this work. The micropipe is the hollow core of a large screw dislocation, they follow the growth direction in SiC (c-axis) and propagating into the epitaxial layer(s) of the device. This defect will prevent a SiC device from blocking a reverse voltage, making it potentially useless. The large density of micropipes within a wafer will result a loss of yield in the device fabrication process.

The low-angle grain boundaries (LAGBs) near the crystal periphery tend to form with the growth of large-diameter crystals grown under non optimised process conditions. These LAGBs are defined as the boundaries between misaligned regions of SiC material. This may be either a relative tilt of the (0001) planes or a rotation of the planes with respect to each other, and generally consist of threading edge and screw dislocations.

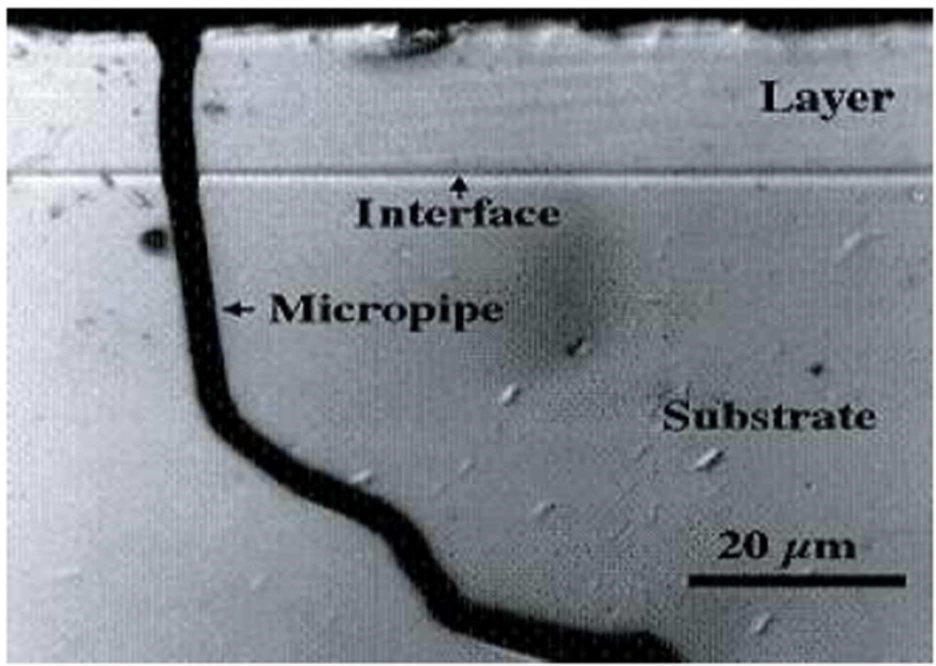


Figure 1.7: Cross sectional view of a micropipe originating from the substrate and propagating into the epitaxial layer as shown in [27].

These LAGBs can act as stress concentrators and increase the chance of wafer cracking at defect locations during the epitaxial growth process. It is therefore important to reduce the density of low angle grain boundaries in the crystals. The LAGBs around the periphery of the wafer have been predominantly removed in the current commercial SiC material [28].

As mentioned previously, SiC is the only compound semiconductor that can be thermally oxidised to form chemically and thermally stable silicon dioxide (SiO_2) layers. These insulating layers are crucial for nearly all electronics applications. However, the high density of interface trap at the SiC/SiO_2 interface is the major obstacle in the development of SiC devices, mainly for MOS based devices. A large trap density will affect device

performance as they will capture the carriers from the channel thus lowering the conduction current. Moreover, the charge traps also act as Columbic scattering centres, which decrease the effective channel mobility in a MOSFET. Although it is still unclear what factors make the interface between thermal oxides and SiC so dramatically different from the classic and highly successfully SiO_2/Si interface, it is believed mainly related to silicon and carbon dangling bonds, carbon clusters, carbon dimmers in the SiC and oxygen vacancies in the oxide near the interface [29]. Depending upon the surface potential, these traps can be charged positively or negatively. Figure 1.8 illustrates an example of the dangling bonds at the interface between SiO_2 and semiconductor (SiC or Si) after thermal oxidation.

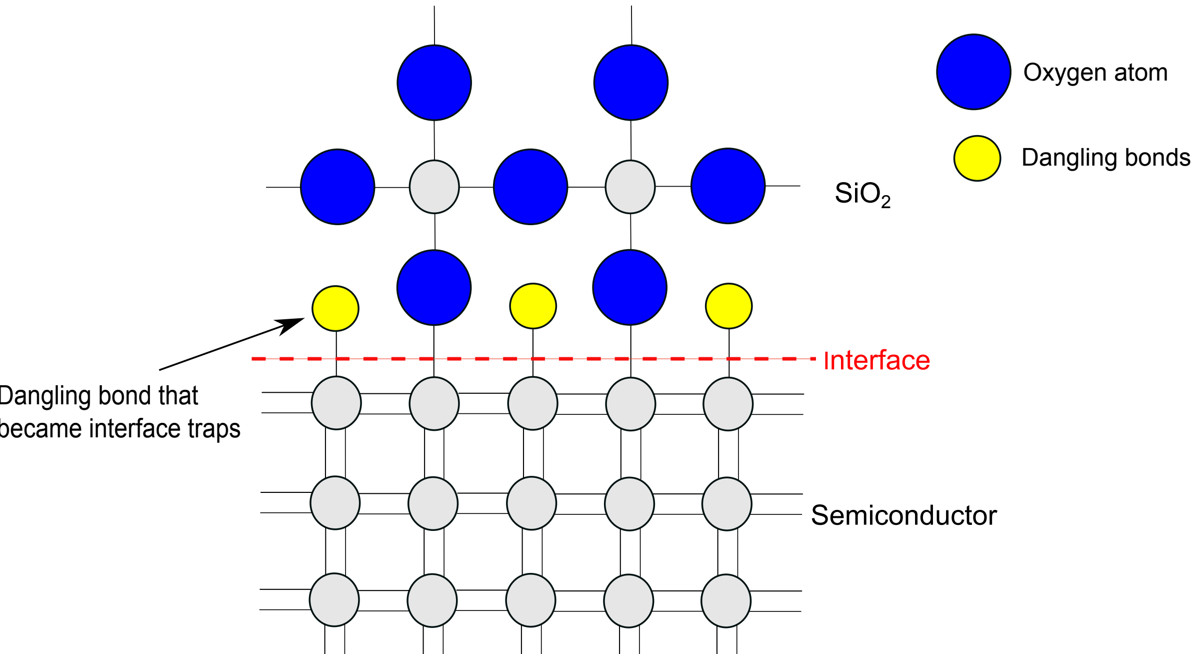


Figure 1.8: Formation of dangling bonds at the interface between SiO_2 and semiconductor (SiC or Si) after thermal oxidation.

To fully utilise SiC's potential, the quality of the SiO_2/SiC interface will need to be improved by developing more efficient processes to passivate defects which were formed during the oxidation process. As discussed in Chapter 6 and 7 of this thesis, the standard passivation process was based on post-oxidation annealing in nitric oxide (NO) or nitric oxide followed by hydrogen annealing (NO+H_2) [29]. However, NO is very toxic and for safety reasons nitrous oxide (N_2O) is becoming more popular in terms of nitridation of thermally grown oxide. These passivations increase the channel mobility of a SiC MOSFET from single digit ($\sim$1 cm^2/V.s) to around 30 cm^2/V.s, which have made the commercialisation of SiC MOSFETs possible. However, this channel mobility value is only about 4% of bulk mobility value of SiC, whereas in the case of Si, the inversion channel mobility can be as much as 50% of bulk mobility. There are other methods reported in the literature that can further improve the channel mobility, such as oxide growth in the presence of sodium, which has mobility value as high as 150 cm^2/V.s, but devices are highly unstable and no practical use because sodium is mobile under stress [30]. Phosphorous passivation is another passivation technique which has been shown to be more effective in reducing the interface trap density compared to NO passivation, with peak field effect mobility of about 80 cm^2/V.s [31]. However, the phosphorous passivation will convert SiO_2 to phosphsilicate glass (PSG), which is a polar material and cause threshold voltage instability. In this work, both N_2O and phosphorous passivation have been investigated and compared for both 4H-SiC MOS capacitor and MOSFETs as discussed in more details in Chapter 6 and 7.

Recently, Sharma et al. [31] reported a phosphorous passivation process which uses a thin PSG layer capped with deposited oxide. This process improves the threshold voltage stability compared to the thick PSG passivation method with the peak field effect mobility of around 70 $cm^2/V.s$. High temperature oxidation (>1500°C) with a low oxygen flow rate has also been reported to reduce the interface trap density to around 2×10^{11} $cm^{-2}eV^{-1}$ with field effect mobility of approximately 40 $cm^2/V.s$ [32, 33]. High temperature nitridation, both annealing of thermally grown oxides and direct growth in N_2O on 4H-SiC(0001) MOSFETs with implanted p-body region have been investigated and published recently as discussed in more details in Chapter 7. Results have demonstrated that at high temperature nitridation (>1200°C) there is a significant improvement in the interface trap density ($\sim1.5\times10^{11}$ $cm^{-2}eV^{-1}$) and field effect channel mobility ($\sim$20 $cm^2V.s$) compared with those at lower temperature (1×10^{12} $cm^{-2}eV^{-1}$ and 4 $cm^2/V.s$). Among those nitridation temperatures, 1300°C has found to be the most effective in increasing the field effect channel mobility and reducing threshold voltage.

1.3 Current Status of Silicon Carbide Power Devices

In recent years, commercial-grade silicon carbide (SiC) power semiconductor devices have shown the promise to deliver the next generation of SiC-based power electronic converters. The only types of SiC devices that are commercially available at the moment are MOSFETs and Schottky diodes, with maximum voltage ratings of 1200 V and 1700 V re-

spectively. There are only few companies in the world that manufacture SiC MOSFETs at the moment. Table 1.2 summarise the electrical performance of some of the commercially available SiC MOSFETs.

Table 1.2: Comparison of commercially available SiC MOSFETs from different manufacturers [8, 34–36].

	Drain source voltage [V]	Drain current [A]	On-state resistance [mΩ]	Maximum junction temperature [°C]
Cree Inc.	1200	60	25	150
Cree Inc.	1700	2.6	1000	150
Rohm Semiconductor	1200	40	80	175
Microsemi Corporation	1200	40	80	175
ST Microelectronics	1200	40	100	200

It is seen that for the 1200 V rating, SiC MOSFET available from Cree provides the highest drain current of 60 A and lowest on-state resistance of 25 mΩ . However, devices available from other manufacturers allow maximum operating temperature of 175°C and 200°C, which is higher than the value of 150°C specified by Cree, Inc. The highest voltage rating of SiC MOSFET in the market today is 1700 V provided by Cree Inc.

A full-SiC power module, integrating SiC MOSFETs and SiC SBDs, is also commercially available today from few manufacturers such as Cree Inc., Rohm Semiconductor, Semikron and Microsemi Corporation. Table 1.3 summarise the electrical performance of some of SiC power modules in the market.

Table 1.3: Comparison of commercially available full-SiC power module from different manufacturers [37–41].

	Drain source voltage [V]	Drain current [A]	Total power dissipation [W]	Junction temperature (Max.) [°C]
Cree Inc.	1200	300	1660	150
Cree Inc.	1700	225	1760	150
Rohm Semiconductor	1200	300	1875	175
Semikron	1200	541	n/a	175
Microsemi Corporation	1200	293	2300	175
Microsemi Corporation	1700	200	1250	150
Mitsubishi Electric	1200	800	n/a	n/a

SiC module has the advantage of substantial reduction in switching losses compared to the conventional IGBT module which combine Si IGBTs and Si fast recovery diodes (FRDs). Other benefits of SiC power module over Si module are: 1. Improvement of conversion efficiency due the lower switching losses, 2. Simplification of thermal management (smaller and less expensive heat sink or cooling system), and 3. Downsizing of passive components due to increasing switching frequency.

1.4 Thesis Outline

The theoretical concepts that apply to the design of high voltage 4H-SiC power MOSFETs are presented in the following Chapter. The basic operating principles of vertical power MOSFET, and the shielded planar inversion-mode power MOSFET structures that used

in this work are outlined. Introduction to different edge terminations design including the junction termination extension which were used in this work were presented next. The on-resistance of a power VD-MOSFET and its internal resistance components are then discussed. This is followed by discussion of different oxidation techniques and fabrication issues that are encountered in the development of 4H-SiC power devices. Chapter 3 presents the design and simulation of high voltage 4H-SiC power MOSFET and junction termination extension (JTE). The device designs which include the drift layer design to support the high voltage (1kV, 3kV and 10kV) are presented. Both conventional planar power MOSFET and shielded planar VD-MOSFET structures design are illustrated. On-state I-V and reverse breakdown simulations with different JTE structures are also carried out.

Chapter 4 outlines the characterisation techniques both physical and electrical for the SiC devices fabricated in this work. The electrical characterisation includes capacitance-voltage (C-V), current-voltage (I-V) and contact resistance measurements. The physical characterisation of semiconductor yields an assessment of the physical and morphological aspects of a device structure. Technologies for analysis include Atomic Force Microscopy (AFM), which was used to measure the surface roughness of a sample before and after the annealing process. Scanning Electron Microscope (SEM), which is a type of electron microscope that can produce a much greater magnification than optical microscope. It was used to evaluate the morphology of etched features in the 4H-SiC and SiO_2. Secondary Ion Mass Spectrometry (SIMS) was used to determine the distribution and concentration

of implanted dopant species in the 4H-SiC material.

Chapter 5 presents the fabrication processes optimisation which are required for 4H-SiC MOSFETs fabrication. Firstly, the fabrication and characterisation of a carbon capping layer on 4H-SiC to suppress step bunching on 4H-SiC was carried out. Next, a study into the ion implantation and activation of 4H-SiC was presented. Following this, TLM structures were fabricated and characterised to determine the contact resistance of the ohmic contacts to both P-type and N-type 4H-SiC.

The fabrication processes developed in Chapter 5 are then applied in Chapter 6, which the fabrication and characterisation of 4H-SiC MOS capacitor and Schottky diodes are presented. The details of fabrication process for 4H-SiC MOS capacitors using N_2O and phosphorous passivation are presented. The interface traps density (D_{it}) were then extracted and compared using both Terman and High-Low C-V methods. Following this, the design, fabrication and characterisation of the Schottky diodes with various JTE structures are discussed.

Chapter 7 presents the fabrication and characterisation of 4H-SiC n-channel lateral MOSFETs. The fabrication process and the electrical characterisation results for the 4H-SiC MOSFETs with different oxidation and passivation conditions is described, which follows the chronological evolution of these devices. The effect of high temperature oxidation (1500°C), N_2O nitridation and phosphorous passivation techniques have been investigated. Similarly, Chapter 8 presents the fabrication and characterisation of 4H-SiC vertical power MOSFETs, which also follows the chronological evolution of these devices.

First generation devices have been fabricated on a 10 μm thick n-type epitaxial layer with doping concentration of 2×10^{16}cm^{-3}, and the gate oxide was grown using standard thermal oxidation at 1400°C for 1 hour. The second generation device have been fabricated on a 30 μm thick n-type epitaxial layer with doping concentration of 4×10^{15}cm^{-3}, and the gate oxide was grown using standard thermal oxidation followed by a N_2O post oxidation anneal at 1300°C. Finally, Chapter 9 presents the conclusions of this thesis, as well as outlining suggestion for further work.

Chapter 2 High Voltage 4H-SiC Power MOSFETs

This chapter presents the technical background information require to develop and evaluate the high voltage 4H-SiC power MOSFET detailed in this thesis. The basic operating principles of vertical power MOSFET and the shielded planar inversion-mode power MOSFET structure that used in this work are outlined. Next, the impact of edge termination on breakdown voltage and design of high voltage junction termination extension are discussed. The on-resistance of a power VD-MOSFET and its internal resistance components are then discussed. This is followed by a discussion of different oxidation techniques and fabrication issues that are encountered in the development of 4H-SiC power devices.

2.1 The VD-MOSFET Cell Structure and Operation

The vertical power MOSFET or vertical diffused MOSFET (VD-MOSFET) was developed in mid 1970s to improve the performance over the existing power bipolar transistors [42].

It has the advantages of high input impedance, fast switching speed and support high voltage. A cross section of the VD-MOSFET structure is shown in Figure 2.1.

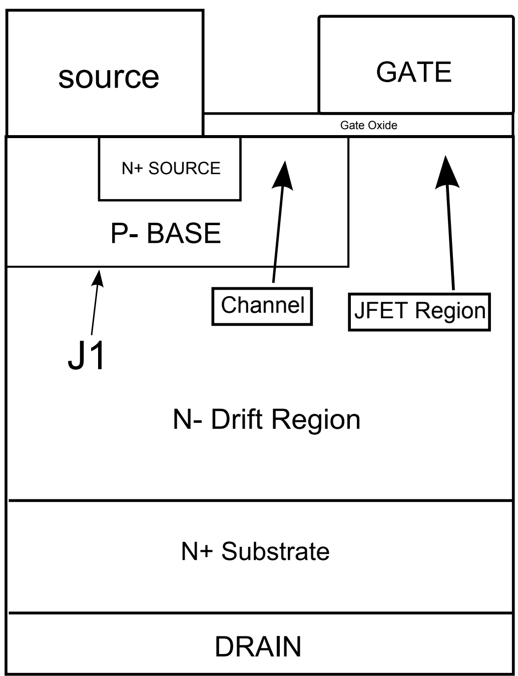


Figure 2.1: VD-MOSFET structure.

From Figure 2.1 it is seen that the device is fabricated on an N- epitaxial layer, which is grown on a heavily doped N+ substrate. The device can support high voltages by utilising a lightly doped N- drift region. For the n-channel VD-MOSFET as shown in Figure 2.1, the current path is generated between the source and the drain when a positive bias is applied to the gate electrode. An inversion layer is formed at the surface of the P-base region by pushing away holes and attracting electrons when positive gate bias is larger than the threshold voltage and the drain-source voltage ($V_G > V_{TH}$ and $V_D < V_G - V_{TH}$).

After electrons go through the channel region, they then enter a JFET region which

is located between the P-base regions as shown in Figure 2.1. Because the JFET region is relatively narrow, current flow is restricted in this region which causes an increase of resistance of the VD-MOSFET. The JFET region resistance can be reduced by optimising the JFET width or enhancing its doping concentration by ion implantation. Detailed optimisation of the JFET width and its doping concentration for the VD-MOSFET are outlined in Chapter 4.

After through the JFET region, the electrons then enter the N- drift region. The non-uniform current distribution within the drift region makes the internal resistance of the VD-MOSFET structure larger than the ideal specific on-resistance of the drift region. For high voltage devices (>10 kV), the drift region resistance will be the dominant contributor to the overall on-state resistance. As the electrons leave the JFET region and enter the drift region, they spread out (see Figure 2.19), this spreading needs to be taken into account in determining the resistance. Details of each resistance component within VD-MOSFET are discussed in Section 2.4.

The VD-MOSFET structure was developed and widely utilised for silicon, but is not suitable for silicon carbide devices due to the much greater bandgap of silicon carbide material. As discussed in [43] the low doping concentration require in the P-base region to achieve low threshold voltage cannot sustain a high blocking voltage anymore. And the electric field under the gate oxide in silicon carbide is much larger than those in silicon devices, which will cause the breakdown of gate oxide at large blocking voltage. Therefore, a modified VD-MOSFET structure which called the shielded planar MOSFET structure

was developed and also used in this work for SiC power MOSFET design. Details of its structure and design are discussed in Chapter 4.

2.2 Forward Conduction Characteristics

MOSFETs have different operating regions, which depend on the voltages at the terminals. There are three regions of operation, which are the cut-off region, linear region and saturation region.

In the cut-off region, where the gate bias voltage is less than the threshold voltage of the device ($V_{\mathrm{G}} < V_{\mathrm{TH}}$), the MOSFET is turned off and there is no conduction between the drain and the source. Ideally the current between the drain and the source should be zero when the MOSFET is turned off, but in reality there is a weak-inversion current which is also called subthreshold leakage.

In linear region, where the gate bias voltage is greater than the threshold voltage and the drain bias voltage ($V_{\mathrm{G}} > V_{\mathrm{TH}}$ and $V_{\mathrm{D}} < (V_{\mathrm{G}} - V_{\mathrm{TH}})$), the MOSFET is turned on and an inversion channel is formed which allows current to flow between the drain and the source. In this region, the MOSFET acts like a resistor, in which the drain current is linearly proportional to the drain bias voltage, controlled by the gate voltage.

When the drain current is increased to be greater than the gate bias voltage ($V_{\mathrm{G}} > V_{\mathrm{TH}}$ and $V_{\mathrm{D}} \geq (V_{\mathrm{G}} - V_{\mathrm{TH}})$), the resistance to current flow increases. The drain current will saturate at larger drain bias voltages. This is called the saturation region.

The drain current in these operating regions for the MOSFET structure can be derived from the resistance of the inversion layer which forms the channel. Figure 2.2 shows the MOSFET channel structure with the drain bias voltage smaller than the gate bias voltage (linear region). To calculate the channel resistance it is assumed that (a) the gate dielectric is a perfect insulator, (b) channel mobility is independent of the electric field in both longitudinal and transverse directions, and current transport in the channel is by drift current transport theory only (c) the p-base region is uniformly doped, (d) there is no leakage current in the substrate and (e) electric field in the longitudinal direction along the surface caused by the drain-source bias is much smaller than the electric field in the transverse direction caused by the gate bias (gradual channel approximation).

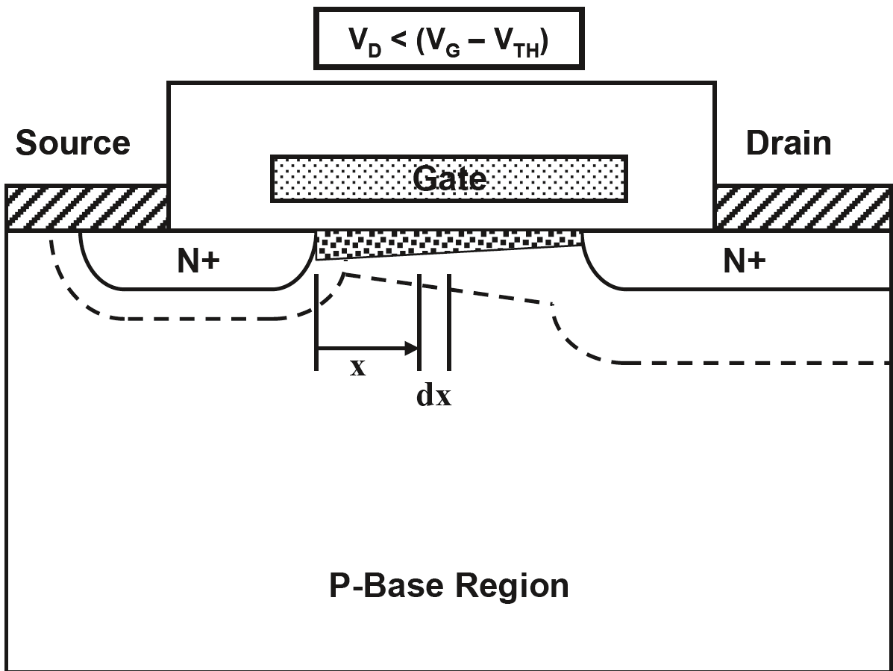


Figure 2.2: Lateral MOSFET showing the channel region with drain bias voltage less than the gate bias voltage (linear region) [44].

Figure 2.2 shows the channel region of lateral MOSFET structure when $V_G > V_{TH}$ and $V_D \leq (V_G - V_{TH})$. The resistance of the small segment dx is determined by

$$\mathrm{d}R = \frac{dx}{W\mu_{ni}Q_n(x)} \tag{2.1}$$

where $Q_n(x)$ is the charge density, W is the channel width perpendicular to the cross section in the Figure 2.2. μ_{ni} is channel mobility. The charge in the channel region is determined by the gate bias voltage, oxide capacitance and the local potential $V(x)$:

$$Q_n(x) = C_{\mathrm{OX}}\left[V_{\mathrm{G}} - V_{\mathrm{TH}} - V(x)\right] \tag{2.2}$$

The voltage drop across each small segment dx is given by

$$\mathrm{d}V = I_{\mathrm{D}}\mathrm{d}R \tag{2.3}$$

Integrating along the channel

$$\int_0^L I_{\mathrm{D}}\mathrm{d}x = W\mu_{ni}C_{\mathrm{OX}}\int_0^{V_{\mathrm{D}}}\left(V_{\mathrm{G}} - V_{\mathrm{TH}} - V\right)\mathrm{d}V \tag{2.4}$$

Leading to

$$I_{\mathrm{D}} = \mu_{ni}C_{\mathrm{OX}}\frac{W}{L}\left[\left(V_G - V_{\mathrm{TH}}\right)V_{\mathrm{D}} - \frac{V_{\mathrm{D}}^2}{2}\right] \tag{2.5}$$

where L is the channel length and C_{OX} is the gate oxide capacitance per unit area.

Figure 2.3 shows the channel region of lateral MOSFET structure when it is in the saturation region (pinch off, $V_{\mathrm{G}} > V_{\mathrm{TH}}$ and $V_{\mathrm{D}} \geq (V_{\mathrm{G}} - V_{\mathrm{TH}})$). The drain current is now weakly dependent upon the drain voltage but primarily controlled by the gate bias voltage, and can be modelled as

$$I_{\mathrm{D}} = \mu_{ni} C_{\mathrm{OX}} \frac{W}{L} \frac{(V_{\mathrm{G}} - V_{\mathrm{TH}})^2}{2} \tag{2.6}$$

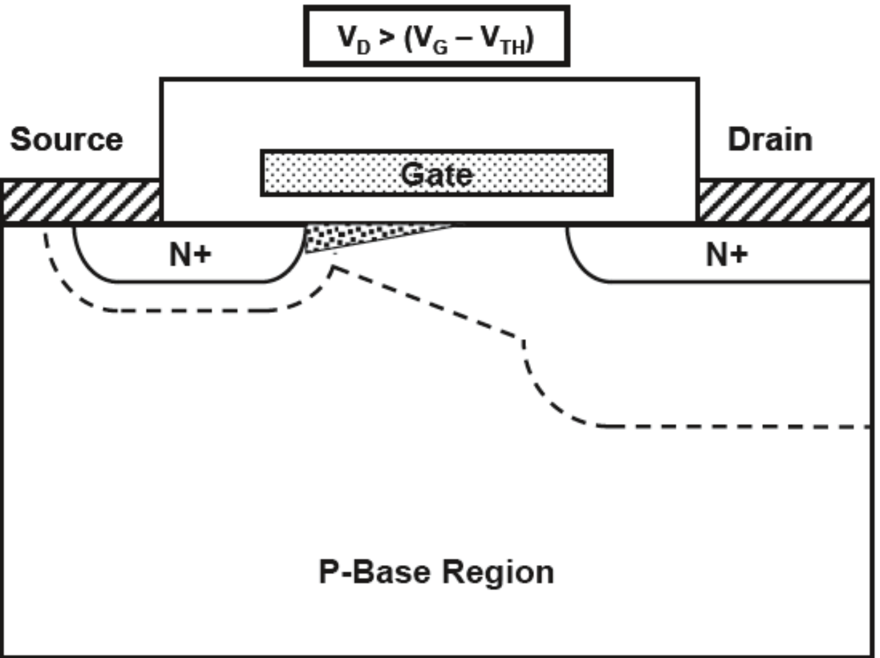


Figure 2.3: Lateral MOSFET showing the channel region with drain bias voltage greater than the gate bias voltage (saturation region) [44].

The typical output characteristics of power VD-MOSFET is shown in Figure 2.4.

The characteristics of power MOSFET are slightly different from the lateral n-channel

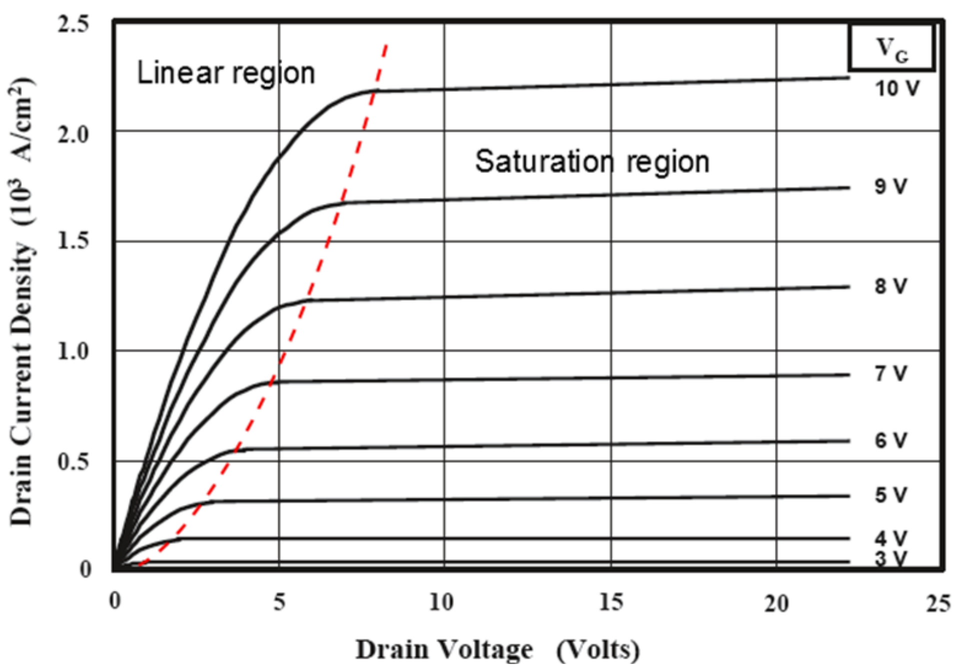


Figure 2.4: Typical output characteristics of a power VD-MOSFET [44].

MOSFET. The drain current will increase slightly when increasing the drain bias voltage even in the saturation region after the channel is pinch-off. This is because of a reduction in channel length when the drain bias voltage is increased. By considering the reduction of channel length , the saturated drain current of power VD-MOSFET becomes

$$I_{D,sat} = \frac{W\mu_{ni}C_{\mathrm{OX}}}{L-\lambda}\left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)^2 \tag{2.7}$$

where λ is the reduction of the channel length when the drain bias voltage is increased. Details of λ model can also be found in [44].

2.2.1 MOS Interface

The behaviour and the quality of the channel region of the power VD-MOSFET is important as it governs the performance of the device. The properties of the channel region are determined by the Metal-Oxide-Semiconductor (MOS) structure. Using this structure, we can study the characteristics of an oxide-semiconductor interface as well as the breakdown characteristics of the oxide [29].

A MOS structure is shown in Figure 2.5 in which a silicon dioxide is sandwiched

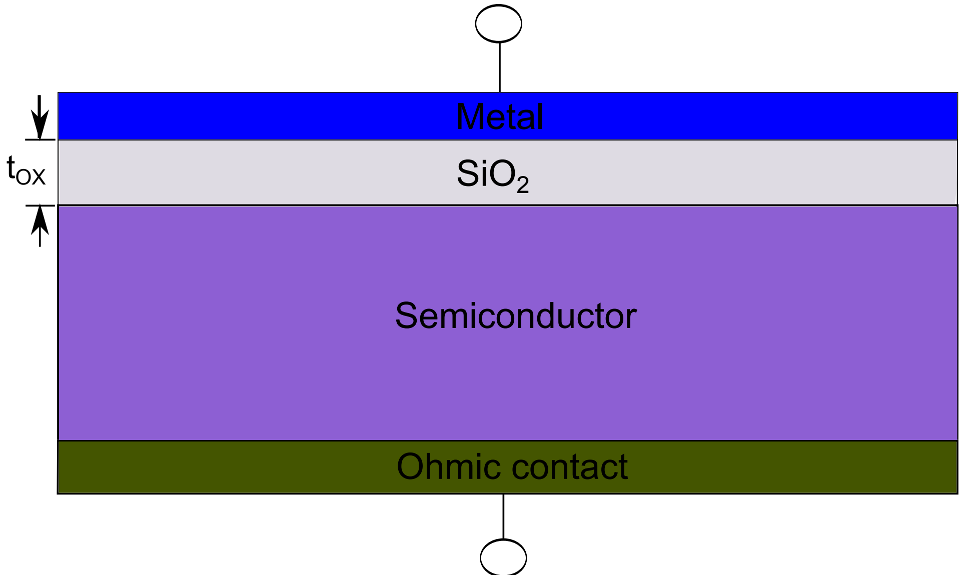


Figure 2.5: Metal oxide semiconductor capacitor.

between a metal layer and a semiconductor. The discussion in this section is based on an ideal MOS structure. An ideal MOS structure is assumed that (a) the oxide is a perfect insulator and no current is flowing under static bias (b) charges are only in the metal and the semiconductor, the oxide is free of mobile charges and traps and (c) Work function

of the metal is equal to the work function of the semiconductor, $\phi_m = \phi_s$ (flat-band condition).

MOS capacitor can have different operation conditions depending on the voltage applied on the gate electrode. Figure 2.6 shows the energy band diagram for the p-type MOS capacitor at the flat band condition.

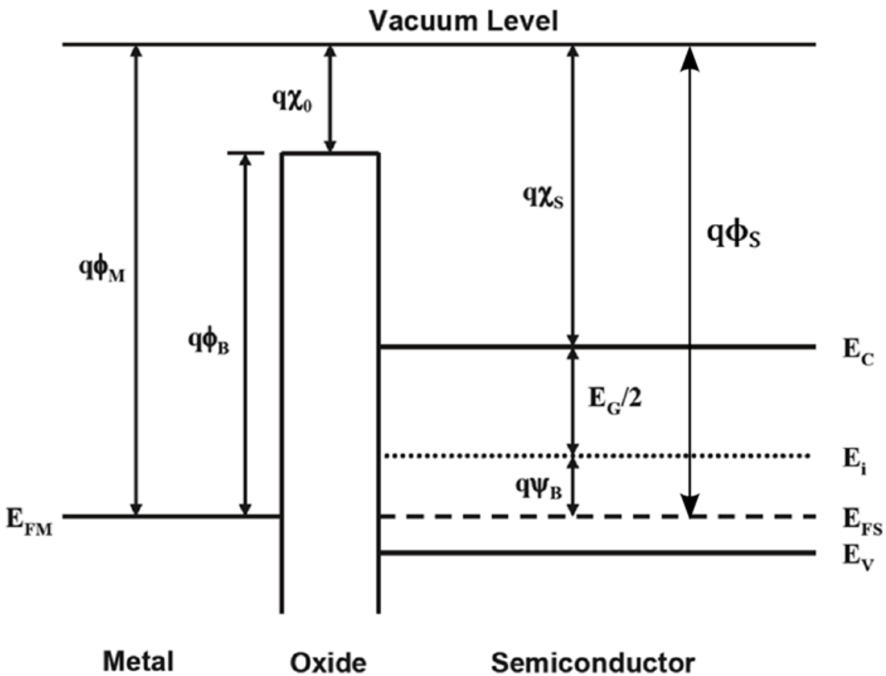


Figure 2.6: Energy band diagram of a p-type MOS capacitor at the flat band condition [44].

Under the assumption that work function of the metal is equal the work function of the semiconductor ($\phi_m = \phi_s$), the Fermi level of the metal (E_{FM}) has the same energy as the Fermi level of the semiconductor (E_{FS}). Therefore, there is no charge transfer between the metal and the semiconductor when no gate bias voltage is applied, leading

to flat band condition as illustrated in the Figure 2.6. From the Figure 2.6, it can be seen that

$$q\phi_{\mathrm{M}} = q\chi_S + \frac{E_{\mathrm{G}}}{2} + q\psi_{\mathrm{B}} = q\phi_B + q\chi_0 \tag{2.8}$$

where χ_S is the electron affinity, E_{G} is the energy bandgap of the semiconductor, ψ_{B} is the bulk potential of the semiconductor, and χ_0 is the electron affinity for the oxide. ψ_{B} can also be obtained by using following equation [44]

$$\psi_{\mathrm{B}} = \left(\frac{E_{\mathrm{i}} - E_{\mathrm{FS}}}{q}\right) = \frac{kT}{q} ln\left(\frac{N_{\mathrm{A}}}{n_i}\right) \tag{2.9}$$

where E_{i} is the intrinsic energy level of the semiconductor, n_i is the intrinsic carrier concentration of the semiconductor and N_{A} is the hole concentration.

When the metal contact of the p-type MOS capacitor is applied with negative bias voltage, the metal becomes negatively charged and attracts the holes (positively charged) in the semiconductor towards the oxide and semiconductor interface. This condition of MOS capacitor is referred to as accumulation. Figure 2.7 shows the energy band diagram of a p-type MOS capacitor under accumulation condition. The increased concentration of holes at the interface between the semiconductor and the oxide reduces the energy difference between the Fermi level and the valence band edge as illustrated in Figure 2.7.

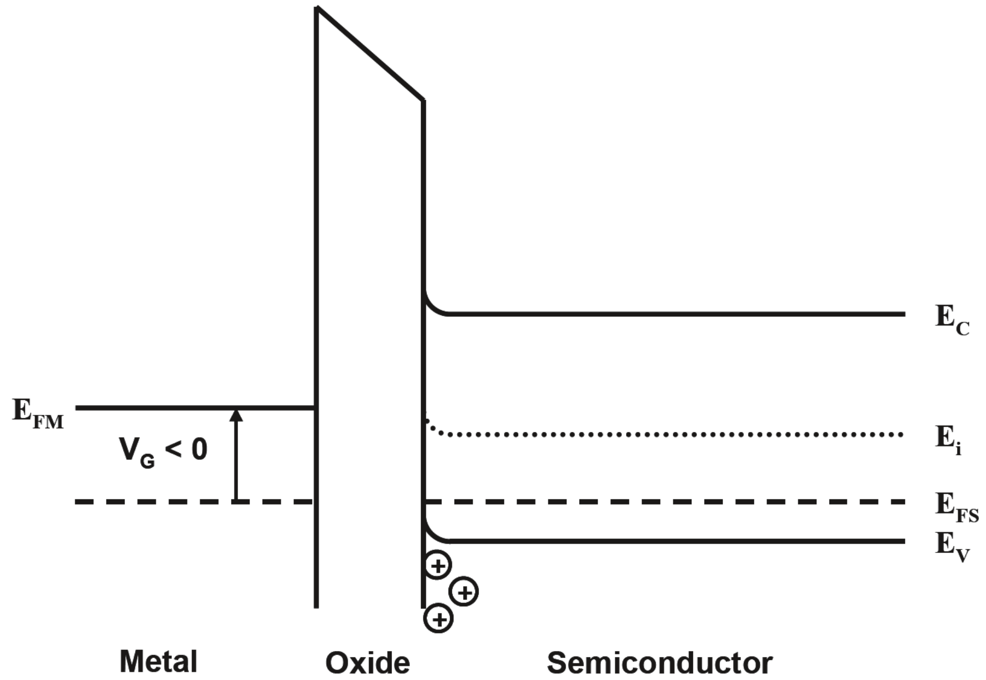


Figure 2.7: Energy band diagram of a p-type MOS capacitor under accumulation condition [44].

When a small positive bias is applied to the metal contact of the p-type MOS capacitor, the metal becomes positively charged and repels the positively charged holes in the semiconductor away from the interface. The semiconductor at the interface between the oxide and semiconductor becomes depleted of holes (majority carriers), which leads to the energy band bending as illustrated in Figure 2.8. This condition of MOS capacitor is referred to as depletion. Again net charge is equal to zero, as no current is flowing.

When a larger positive bias is applied to the metal contact of the p-type MOS capacitor, the positively charged holes are pushed further away from the interface and the negatively charged minority carriers (electrons) are attracted to the oxide semiconductor interface, creating a so called inversion layer. This condition of MOS capacitor is referred

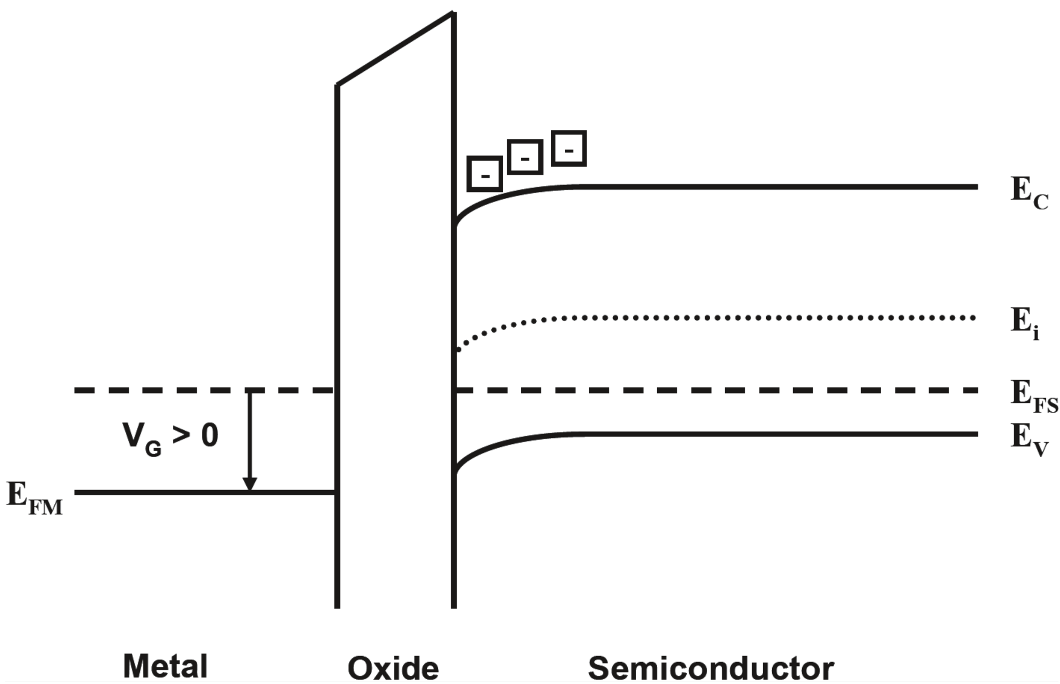


Figure 2.8: Energy band diagram of a p-type MOS capacitor under depletion condition [44].

to as inversion. Figure 2.9 shows the energy band diagram for the p-type MOS capacitor under inversion condition. It is seen that the band bending increases and the intrinsic level crosses the Fermi level. The semiconductor surface now has the properties of an n-type semiconductor. This inversion layer can be utilised to form the channel in the MOSFET. When the intrinsic level is close to the Fermi level, the concentration of minority carriers (electrons) is small, this condition is referred to as weak inversion. When there is sufficiently large positive bias apply to the metal contact of p-type MOS capacitor, the concentration of minority carriers will exceed the concentration of the majority carriers, and this condition is referred to as strong inversion. The depletion region width for the p-type MOS structure will reach its maximum value.

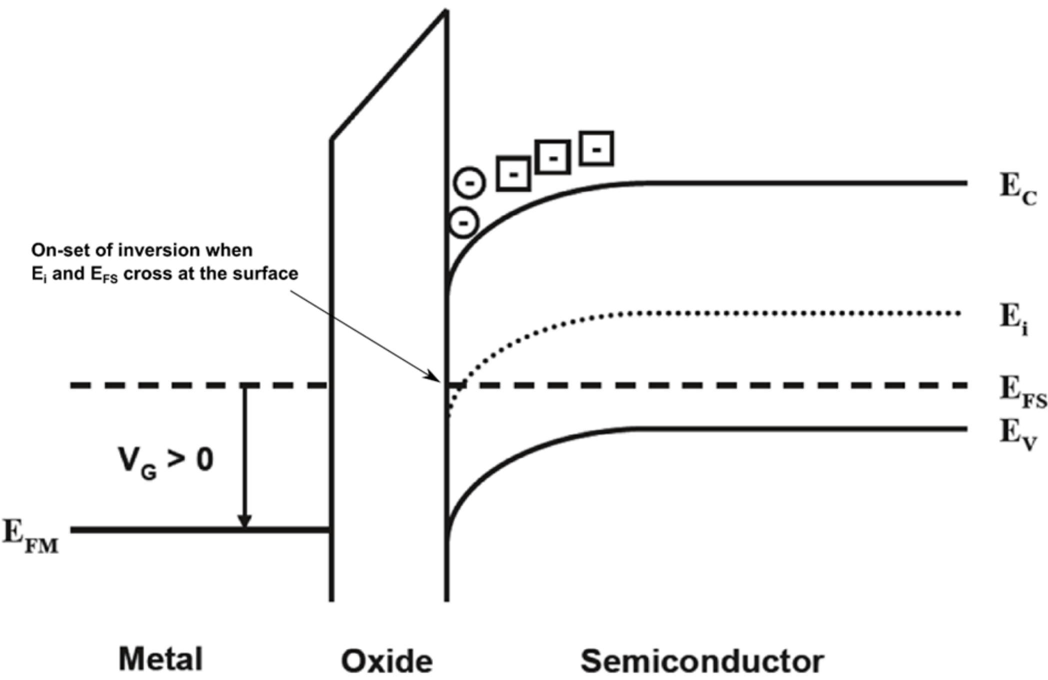


Figure 2.9: Energy band diagram of a p-type MOS capacitor under inversion condition [44].

2.2.2 Threshold Voltage

The threshold voltage (V_{TH}) is defined as the voltage that apply to the metal contact of the MOS capacitor to enter the strong inversion condition. In terms of a MOSFET, it is the minimum gate to source voltage that is needed to create a conducting channel between the source and the drain terminals. This implies that the surface electron concentration equals the surface doping concentration and thus we must have a surface potential (ψ_S) of twice the bulk potential (ψ_B) as defined in Figure 2.6. Since the voltage applied to the metal contact of the MOS capacitor is shared between the oxide and the semiconductor,

the threshold voltage is equal to

$$V_{\mathrm{TH}} = V_{OX} + \psi_S \tag{2.10}$$

where V_{OX} is the voltage across the oxide and ψ_S is the surface potential of the semiconductor which equal to twice the bulk potential, so

$$V_{\mathrm{TH}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{OX}}} + 2\psi_{\mathrm{B}} \tag{2.11}$$

Since the total charge per unit area $Q_{\mathrm{S}} = -\varepsilon_{\mathrm{S}} E_{\mathrm{S}}$ from Gauss's law, where the semiconductor surface electric field E_{S} can be derived from the integration of the potential distribution equation from Poisson's equation

$$E(x) = -\frac{\mathrm{d}\psi}{\mathrm{d}x} = \frac{\sqrt{2}kT}{qL_{\mathrm{D}}} F\left(\frac{q\psi}{kT}, \frac{N_D}{N_{\mathrm{A}}}\right) \tag{2.12}$$

where

$$F\left(\frac{q\psi}{kT}, \frac{N_D}{N_{\mathrm{A}}}\right) = \left\{\left[e^{-q\psi/kT} + \left(\frac{q\psi}{kT} - 1\right)\right] + \frac{N_D}{N_{\mathrm{A}}}\left[e^{q\psi/kt} - \left(\frac{q\psi}{kT} - 1\right)\right]\right\}^{1/2} \tag{2.13}$$

and

$$L_{\mathrm{D}} = \sqrt{\frac{kT\varepsilon_{\mathrm{S}}}{q^2 N_{\mathrm{A}}}} \tag{2.14}$$

which is the extrinsic Debye length as discussed in [44]

Under strong inversion conditions, the second term of equation 2.13 becomes dominant, so

$$Q_{\mathrm{S}}(\text{strong inversion}) = \sqrt{2\varepsilon_{\mathrm{S}} kTN_{\mathrm{A}}} \times e^{q\psi_S/2kT} \tag{2.15}$$

Substitute equation 2.15 into 2.11, the threshold voltage becomes

$$V_{\mathrm{TH}} = \frac{\sqrt{4\varepsilon_{\mathrm{S}} kTN_{\mathrm{A}} ln(N_{\mathrm{A}}/n_i)}}{C_{\mathrm{OX}}} + \frac{2kT}{q} ln\left(\frac{N_{\mathrm{A}}}{n_i}\right) \tag{2.16}$$

The first part for the equation 2.16 is the dominant term for the threshold voltage. Therefore, after substituting the specific oxide capacitance (C_{OX}) with the oxide thickness (t_{OX}) and the permittivity of the oxide ($\varepsilon_{\mathrm{OX}}$), the threshold voltage becomes

$$V_{\mathrm{TH}} = \frac{t_{\mathrm{OX}}}{\varepsilon_{\mathrm{OX}}} \sqrt{4\varepsilon_{\mathrm{S}} kTN_{\mathrm{A}} ln\left(\frac{N_{\mathrm{A}}}{n_i}\right)} \tag{2.17}$$

where ε_{S} is the permittivity of the semiconductor, N_{A} and n_i are the doping concentration and the intrinsic carrier concentration of the semiconductor.

From equation 2.17 it is seen that the threshold voltage is proportional to the oxide thickness (t_{OX}) and the square root of the doping concentration of the semiconductor (N_{A}). This relationship is useful when comes to the design of the power MOSFETs as discussed in Chapter 4 of this thesis.

In a real MOSFETs, the threshold voltage will be slightly different, due to the work function difference the metal contact and the semiconductor and the presence of oxide charge, which is discussed in the following section.

2.2.3 Work Function Difference

Since the metal and the semiconductor have different work function, this difference in the work function for a MOS structure will cause the transfer of charge between the metal and semiconductor at equilibrium conditions. Figure 2.10 shows the energy band diagram of a p-type MOS capacitors band bending due to the work function difference between the metal and the semiconductor, with the work function of the metal smaller than that of the semiconductor.

From Figure 3.6 it is seen that the work function difference between the metal and the semiconductor is given by (see Figure 2.6)

$$q\phi_{MS} = q\phi_B + q\chi_0 - (q\chi_S + E_{\mathrm{i}} + q\psi_{\mathrm{B}}) \tag{2.18}$$

A negative work function results in the charge transfer from the semiconductor to the metal, which forms a depletion region at the interface between the semiconductor and the oxide. This corresponds to the reduction of threshold voltage for the n-channel MOSFET as more charges at the channel region for the same positive gate bias voltage. However, this can be compensated by increasing the doping concentration in the P-base region and

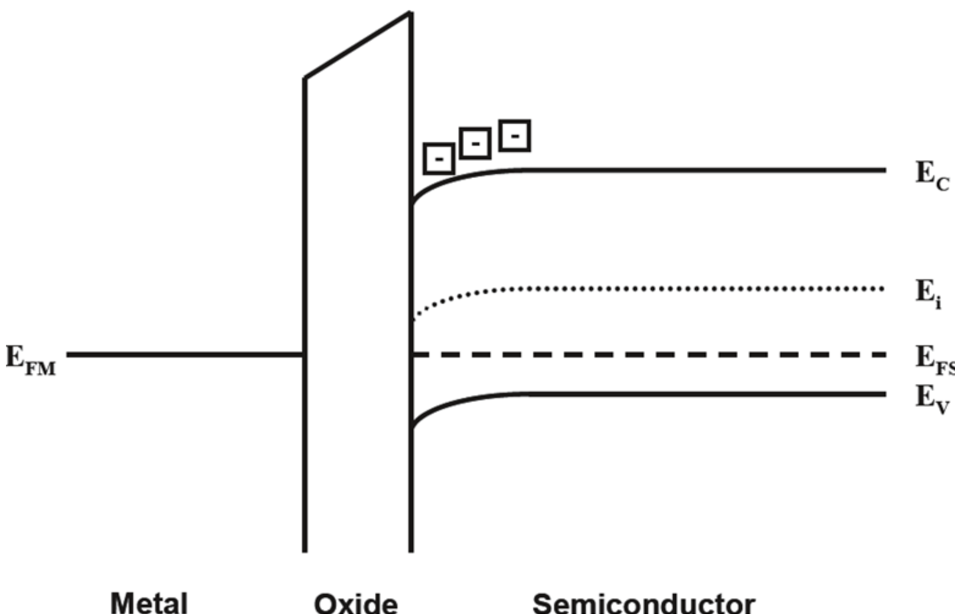


Figure 2.10: Energy band diagram of a p-type MOS capacitor with negative work function difference [44].

reducing the channel length by using the lateral non-uniform doping effect as discussed in [45].

2.2.4 Oxide Charge

Gate oxide for silicon or silicon carbide power devices is usually grown by thermal oxidation. It is observed and reported in the literature that the thermally grown oxide contains different types of charges. There are four types of charges which are commonly known - mobile ion charge, fixed oxide charge, oxide trapped charge and interface trapped charge. Figure 2.11 illustrates various charges within the oxide and the oxide semiconductor interface.

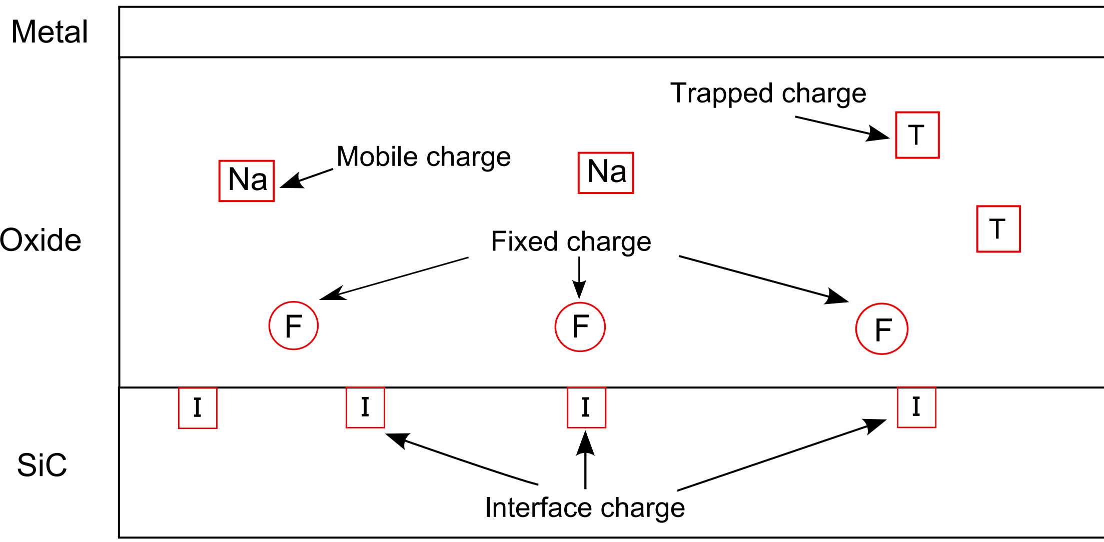


Figure 2.11: MOS structure showing various charges in the oxide and in the SiC interface

The mobile oxide charge exists due to the presence of mobile ions in the oxide such as Na+ and K+. These charges are mobile under voltage bias and presence of electric field, depending upon the polarity of dc bias, these mobile charges can be moved to and from the interface causing a shift in the threshold voltage. These mobile charges can be suppressed or eliminated by performing rigorous cleaning processing (see Appendix B) for SiC samples in the clean room prior to the thermal oxidation in an uncontaminated oxidation furnace.

The oxide trapped charge and the fixed oxide charge exist due to the imperfection and incomplete oxidation of the silicon carbide surface, and are immobile. The fixed oxide charges are normally located close to the surface, and cannot be charged or discharged. The oxide trapped charge however can be negatively or positively charged depending upon the nature of trapping. Both fixed oxide charge and oxide trapped charge are related

to the SiC crystal orientation and the thermal oxidation conditions such as oxidation temperature, time and gas ambient. These charges can cause the degradation of the oxide quality and shift in the threshold voltage.

The interface trapped charge is currently the major obstacle for the silicon carbide MOS research and development [29, 46]. These interface traps form potential wells that capture electrons and holes, and charge traps will also act as Columbic scattering centres which would decrease the channel mobility of MOSFET. These interface traps can be charged positively or negatively depending on the surface potential as discussed in Section 1.2.3 in Chapter 1. Their density also depends upon the crystal orientation of SiC and the thermal oxidation conditions. Smaller density of interface state and therefore higher mobility can be obtained by using the $(1\bar{1}00)$ or $(11\bar{2}0)$ face of 4H-SiC as reported in the literature [47–50].

These interface traps typically lie in the upper half of the 4H-SiC bandgap, the interface traps density (D_{it}) at 0.2 eV from the conduction band edge is usually around $2-4\times10^{12}$ $cm^{-2}eV^{-1}$ without any passivation or post-oxidation techniques [51, 52]. These high D_{it} values will severely degrade the channel mobility of MOSFETs to less than 10 $cm^2/V.S$ [51], which results in having a high on resistance, negating the advantageous the SiC material as discussed in Chapter 1. Reducing the D_{it} is vital for realising the advantageous of 4H-SiC devices and it is the focus of this work to reduce the Dit by using different post oxidation techniques, such as nitrogen or phosphorous to passivate the interface traps [53–55]. Dry oxidation of SiC at high temperature (1500°C) with low oxygen flow

rate was also reported that can reduce the (D_{it}) to about 5×10^{11} $cm^{-2}eV^{-1}$ and field effect mobility can increase to 40 cm^2/V.S [32, 33].

Figure 2.12 illustrates the band bending of p-type MOS capacitor when there is positive charge (Q_{OX}) in the oxide. It is seen that band bending occurs even though there is no voltage bias to the metal contact. The band bending will form a depletion region and reduces the threshold voltage.

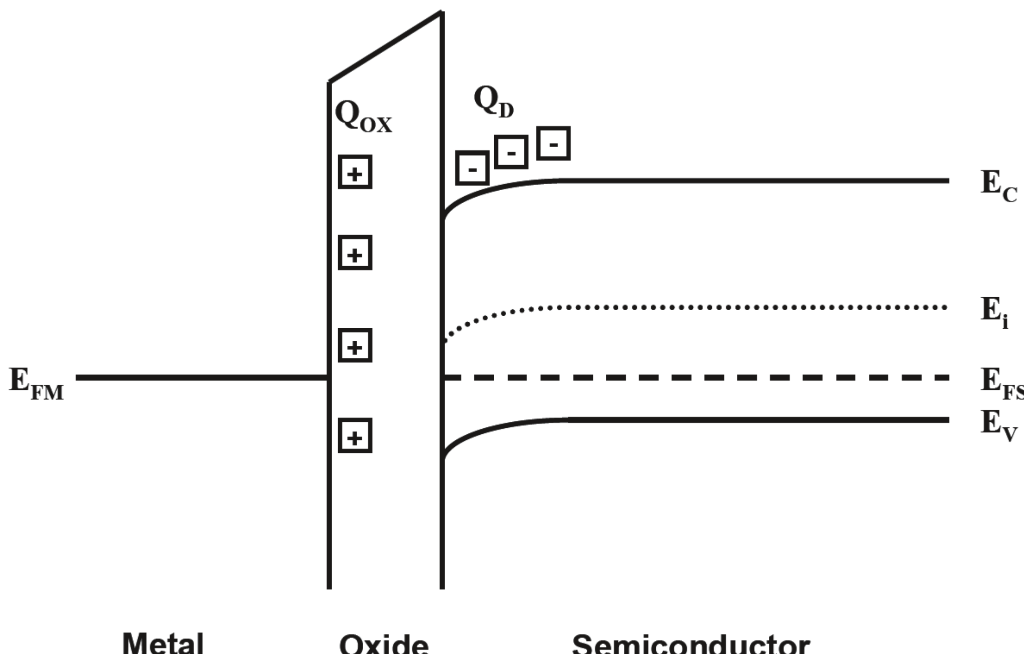


Figure 2.12: Band diagram of a p-type MOS capacitor with positive charge in the oxide.

Assuming all the charges are at the interface between the metal and the oxide, the threshold voltage can be written as

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A ln(N_A/n_i)}}{C_{OX}} + \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \tag{2.19}$$

where Q_{OX} is the total effective oxide charge, which include the mobile oxide charge, the oxide trapped charge, the fixed oxide charge and the interface state charge.

2.3 Off-state Breakdown Voltage

The power MOSFET structure must be designed to support high blocking voltage. The blocking voltage capability for the ideal SiC power MOSFET structure is mainly determined by the drain regions doping concentration and its thickness provided that the JFET region is sufficiently small and there is no early breakdown of the gate oxide. Detail design of the SiC power MOSFET is discussed in Chapter 3.

In the off-state blocking mode, the gate of the MOSFET is shorted to the source to make sure that the device is in off-state. When MOSFET is in the off-state, a reverse bias across the junction between the P-base and the N- drift region. To achieve a high blocking voltage for SiC power MOSFET, the P-base region doping concentration need to be high. However, this will lead to an increase of the threshold voltage, which is not good from the application point of view. This problem can be solved by using the shielded planar structure, which discussed in more details in Chapter 4. The additional P+ shielding region in the shield planar structure creates a potential barrier under the P-base region, which can support high blocking voltage while keeping threshold voltage the same. This shielded planar structure can also reduce the electric field in the gate oxide to prevent the early breakdown of the gate oxide under reverse bias [43].

2.3.1 Edge Terminations

For the ideal one-dimensional structure, the blocking voltage performance of MOSFET structure is determined by the drain regions doping concentration and thickness. However, in the practice, two- and three-dimensional effects mean that the electric field will build up in the edges and limit the breakdown voltage. A specially designed edge termination structures and proper layout design rules are therefore required to minimise the electric field build up and achieve high blocking voltages in practice.

There are many types of terminations for SiC device which have been published in literature and most of them are based on floating field rings and field plates [56–60]. High voltage device composes of three parts: the drift layer, the active area and the periphery. When reverse biased, the electric field is distributed horizontally and vertically around the active area, and it will build up at the edges of the active area if no termination was used. Figure 2.13 shows a vertical device structure with active area, drift layer and the periphery, where the periphery normally composed of two parts: termination and the channel stopper. The role of termination is to control the potentials distribution around the device in order to reduce electric field crowding in the periphery. The channel stopper is made of a highly doped area of the same doping type of the drift layer. Its role is to ensure that the potential in this area is the same as the potential of the bulk, so that other devices on the same wafer do not turn on at the same time, since the surface charge can create a conduction channel between devices. Various termination designs

already exist for silicon device as shown in Table 2.1 [61, 62]. This thesis will be focused on the Junction Termination Extension (JTE) structure as it is very easy to fabricate and effective in reducing the electric field crowding compare with other edge termination designs.

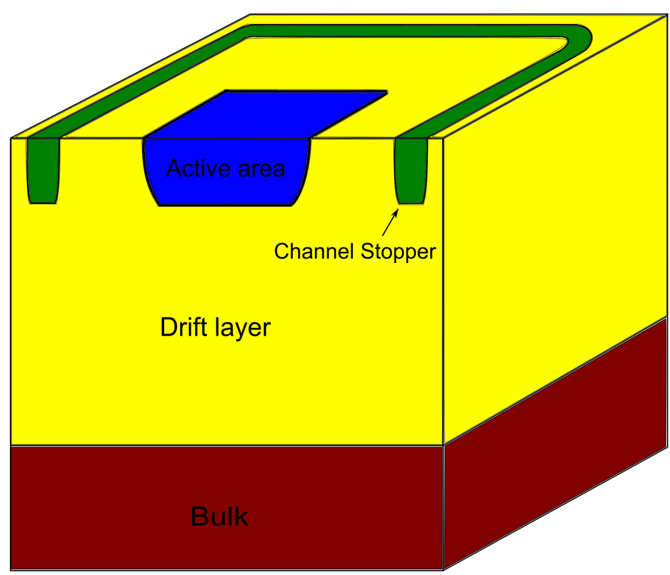


Figure 2.13: Representation of vertical device showing active area, drift layer and the periphery without JTE termination.

2.3.2 Junction Termination Extension

The junction termination extension (JTE) is the one of the most commonly used edge termination techniques in SiC power devices because of its easy to fabricate and effective in improving breakdown voltage. It is usually consist of large p-type ring surrounding the active area, as shown in Figure 2.14.

Table 2.1: Typical High Voltage Junction Terminations used on Silicon devices.

Floating Field Ring	floating field ring, Oxide, main junction, P+, P+, N
Floating Field Plate	floating field plate, Oxide, contact, P+, N
Etched Mesa Termination	P+, Moat, N, N+
Junction Termination Extension	Oxide, Main Junction, P, P+, N

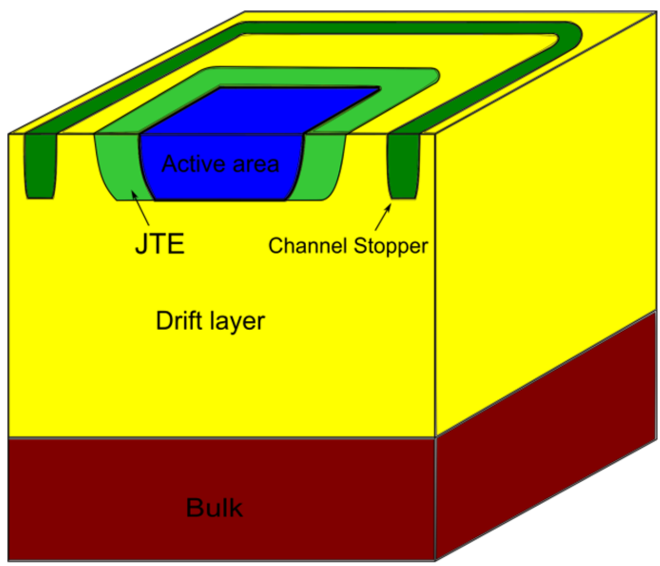


Figure 2.14: Schematic view of vertical device with JTE termination.

The charge within the p-type region can be precisely adjusted with an ion implantation dose. A p-type implantation is used to provide ionised acceptors extending away from the main junction, as illustrated in Figure 2.15.

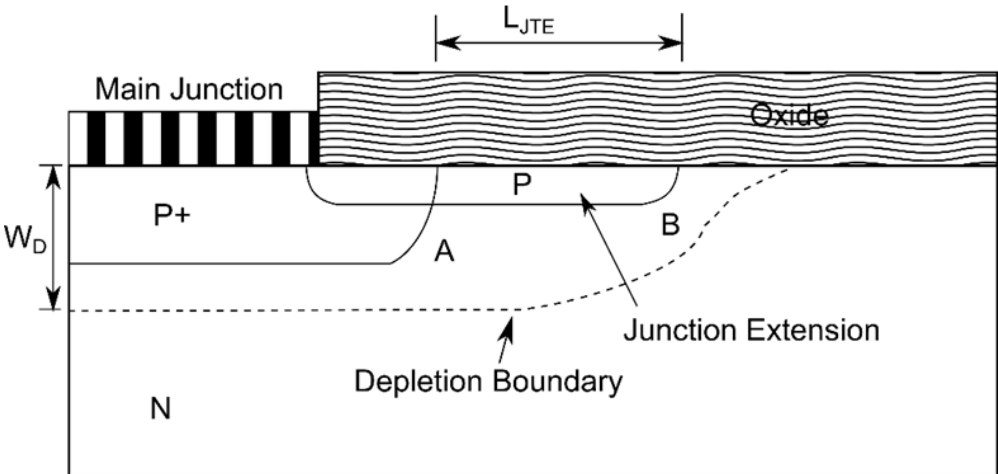


Figure 2.15: Junction termination extension.

When the device is under reverse bias, the depletion region will spread laterally into the JTE as shown in Figure 2.15. In order to achieve the highest breakdown voltage, the dose of the JTE needs to be chosen carefully so that it can be fully depleted along the JTE region. If the dose of the JTE is too low, the JTE will be depleted at lower voltage and breakdown early at corner close to the main junction (point A in Figure 2.15). However, if dose of the JTE is too high, it cannot be fully depleted and the early breakdown will occur at the outmost edge of the JTE (point B in Figure 2.15). To reduce the electric field crowding at both point A and point B under reverse bias, the charge in the JTE needs to be fully depleted.

The charge in the depletion region is given by

$$Q = \int_0^W qN_\mathrm{A} dx = qN_\mathrm{A} W_\mathrm{D} = \varepsilon_\mathrm{S} E_\mathrm{m} \tag{2.20}$$

where W is the depletion width, N_A is the JTE's doping concentration. When the device reaches its breakdown voltage, the electric field at the junction equal to the critical electric field. The charge in the depletion region becomes

$$Q_\mathrm{OPT} = \varepsilon_\mathrm{S} E_\mathrm{cr} \approx 1.71 \times 10^{-6} \mathrm{C/cm^{-2}} \tag{2.21}$$

where the Q_OPT is the optimum charge within the JTE region, ε_S is the dielectric constant of 4H-SiC and E_cr is the critical electric field of 4H-SiC which is assumed to be 2 MV/cm.

The corresponding ion implantation dose can be determined

$$\text{Dose} = \frac{Q_{\text{OPT}}}{q} = 1.07 \times 10^{13}\text{cm}^{-2} \tag{2.22}$$

Equation 2.22 shows the dose require for the JTE region to become completely depleted when it is at breakdown. The electric field distribution is also related to the length of the JTE region (L_{JTE}). If length of the JTE (L_{JTE}) is much longer than the depletion width (W_{D}), the electric field at the surface can be reduced to less than that of in the parallel plane structure and the breakdown voltage can therefore approach to the ideal parallel plane breakdown voltage.

In practise, the breakdown voltage is found to be strongly dependent on the charge of the implanted JTE region. The charge of the JTE can vary significantly depending upon the implant activation temperature and the oxide passivation layer. Mobile ions from packaging of the die and the surface charge may also affect the breakdown voltage. Mobile ions from packaging of the die and the surface charge may also affect the breakdown voltage. A good JTE design is achieve the highest breakdown voltage with a wider optimum JTE dose window (less sensitivity toward the surface charge). One way to achieve this is by using the multiple zones JTE (MZ-JTE) [44, 63]. The idea of multiple zones JTE (MZ-JTE) is to introduce a decreasing doping concentration laterally away from the main junction or mesa edge, the intention being to gradually spread the electric field away from the main junction. This can be achieved by using a series of masking,

etching and implantation steps to create the required charge concentration in each of the JTE zones, as outlined in [24]. However, this approach is expensive and time-consuming. Another less expensive and popular way is to use a single ion-implantation but with variable window size as illustrated in Figure 2.16.

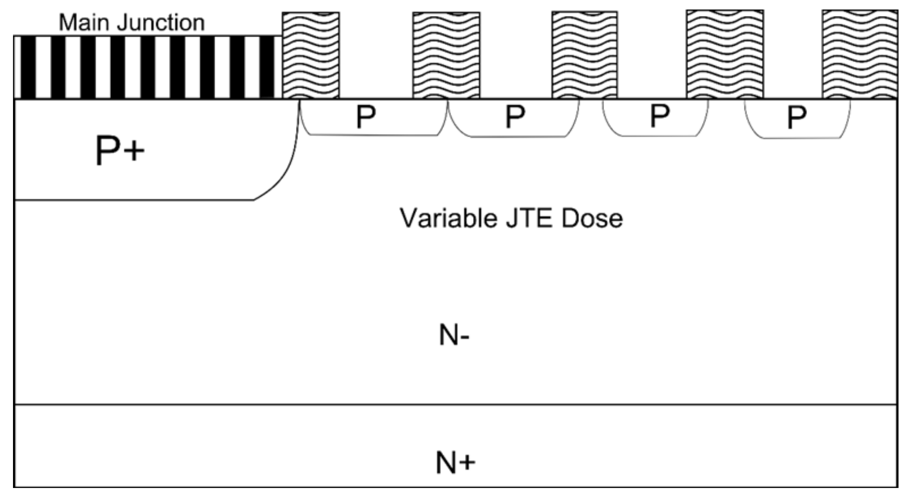
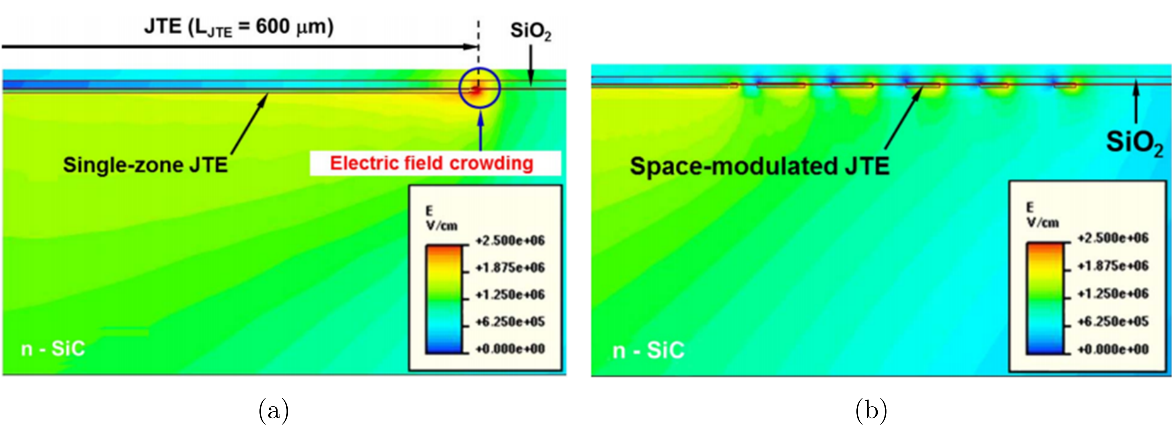


Figure 2.16: Junction termination extension with variable spacing between them.

This method is called the space-modulated junction termination extension (SMJTE), which has been reported in the literature [59,64–66] to be an effective termination in high voltage 4H-SiC power devices. By using the SMJTE the breakdown voltage of over 96% of the parallel-plane value have been reported [67]. Figure 2.17 and Figure 2.18 show an example of the electric field distribution and breakdown voltage of the single zone JTE and the SMJTE structures from the literature [59]. It can be seen that the SMJTE can suppress the electric field crowding at the outmost corner of the single zone JTE by spreading them evenly along each small JTEs. The SMJTE structure also increases the



(a) (b)

Figure 2.17: Simulated electric field distribution for a 4H-SiC PiN diode with (a) single zone JTE structure and (b) SMJTE structure for JTE dose of 1×10^{13} cm^{-2} [59].

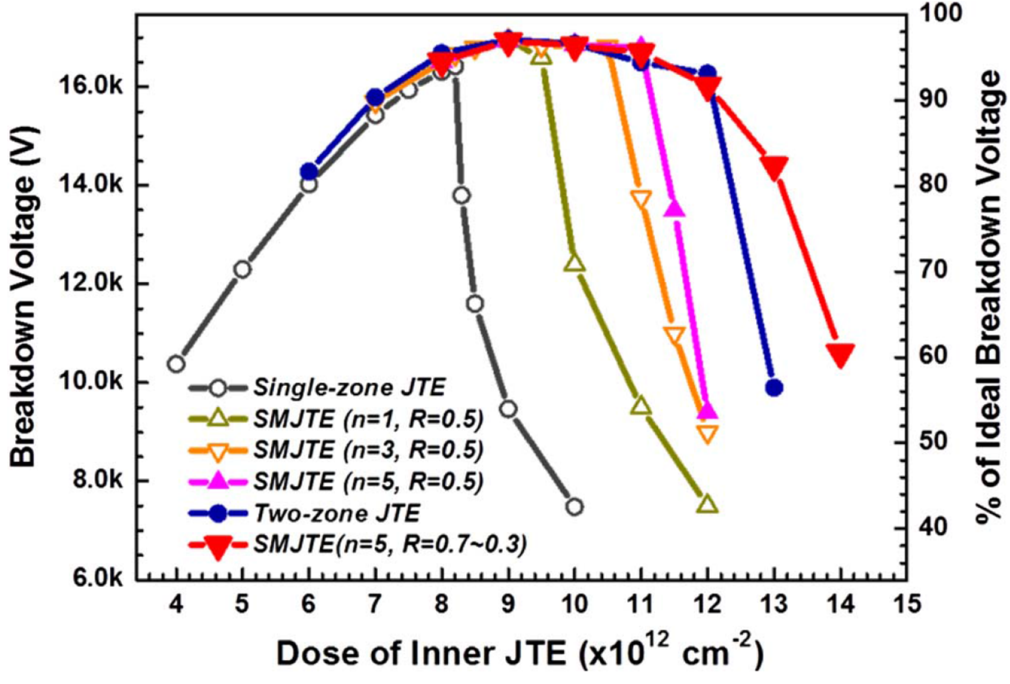


Figure 2.18: Breakdown voltage versus JTE dose for 4H-SiC PiN diode with various JTE structures from the literature [59].

breakdown voltage close to that of the ideal parallel plane breakdown voltage and with wider optimum JTE dose window than those of single zone JTE structure.

In this work, the author investigated the design of the SMJTE structure on 4H-SiC Schottky diode and power MOSFETs and compared it with other popular high voltage JTE published in literature. Details of the SMJTE design and simulation are discussed in Chapter 3 and in recent published papers [66, 67] by the author.

2.4 Power Vertical MOSFET On-Resistance

The power vertical MOSFET on-resistance is the total resistance of the device when a gate bias is applied to turn on the device. The total on-resistance for the vertical MOSFET can be calculated by adding each resistance components between the source and the drain electrodes:

$$R_{\mathrm{ON}} = R_{\mathrm{CS}} + R_{\mathrm{N+}} + R_{\mathrm{CH}} + R_{\mathrm{A}} + R_{\mathrm{JFET}} + R_{\mathrm{D}} + R_{\mathrm{SUB}} + R_{\mathrm{CD}} \tag{2.23}$$

where R_{CS} is the source contact resistance, $R_{\mathrm{N+}}$ is the N+ source region resistance, R_{CH} is the channel resistance, R_{A} is the accumulation region resistance, R_{JFET} is the JFET region resistance, R_{D} is the drift region resistance, R_{SUB} is the substrate resistance and R_{CD} is the drain contact resistance. Since the resistance contribution from the source contact (R_{CS}), the N+ source region ($R_{\mathrm{N+}}$), and the drain contact (R_{CD}) are very small compare to other components in SiC power MOSFET [44], they were neglected when calculating the total on-resistance in this chapter. The substrate resistance (R_{SUB}) has

also been neglected in the analysis. For the silicon carbide shielded inversion-mode planar MOSFET structure which used in this study, the total on-resistance is approximated by

$$R_{\mathrm{ON,sp}} = R_{\mathrm{CH}} + R_{\mathrm{A}} + R_{\mathrm{JFET}} + R_{\mathrm{D}} \tag{2.24}$$

Figure 2.19 shows the resistance components and the current flow pattern for the shield planar MOSFET structure as indicated by the shaded region.

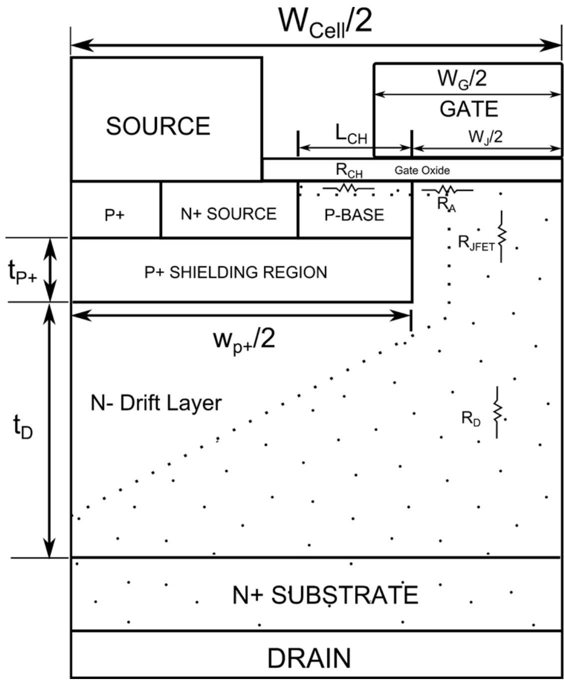


Figure 2.19: Resistance and current path in the shield planar SiC power vertical MOSFET structure.

2.4.1 Channel Resistance

The channel resistance for a lateral MOSFET structure can be expressed as:

$$R_{\mathrm{CH}} = \frac{L_{\mathrm{CH}}}{Z\mu_{ni}C_{\mathrm{OX}}\left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)} \tag{2.25}$$

where L_{CH} is the channel length, Z is the cell length perpendicular to the cross section. μ_{ni} is the inversion layer (channel) mobility and C_{OX} is the specific oxide capacitance. In the power vertical MOSFET structure, the total specific on-resistance is calculated by multiplying the cell resistance by the cell area, taking into account that there are two half-cells within a single cell MOSFET structure (see Figure 2.20):

$$R_{\mathrm{CH,sp}} = \frac{L_{\mathrm{CH}}W_{\mathrm{Cell}}}{2\mu_{ni}C_{\mathrm{OX}}\left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)} \tag{2.26}$$

A channel mobility of up to 165 $\mathrm{cm^2/V.s}$ has been observed in lateral 4H-SiC MOSFET structure [68]. However, the channel mobility reported in the literature for 4H-SiC power MOSFET structure is between 5 to 20 $\mathrm{cm^2/V.s}$ without any post oxidation annealing treatments [69, 70]. These values are less than 4% of the bulk mobility of 4H-SiC ($\sim 800 - 1000$ $\mathrm{cm^2/V.s}$). With N_2O or phosphorus passivation the mobility for 4H-SiC MOSFET is typically between 25 $\mathrm{cm^2/V.s}$ and 80 $\mathrm{cm^2/V.s}$ [31, 71]. This relatively low channel mobility makes the channel resistance the dominant resistance component in SiC MOSFET structure. The channel resistance can also be reduced by reducing the channel

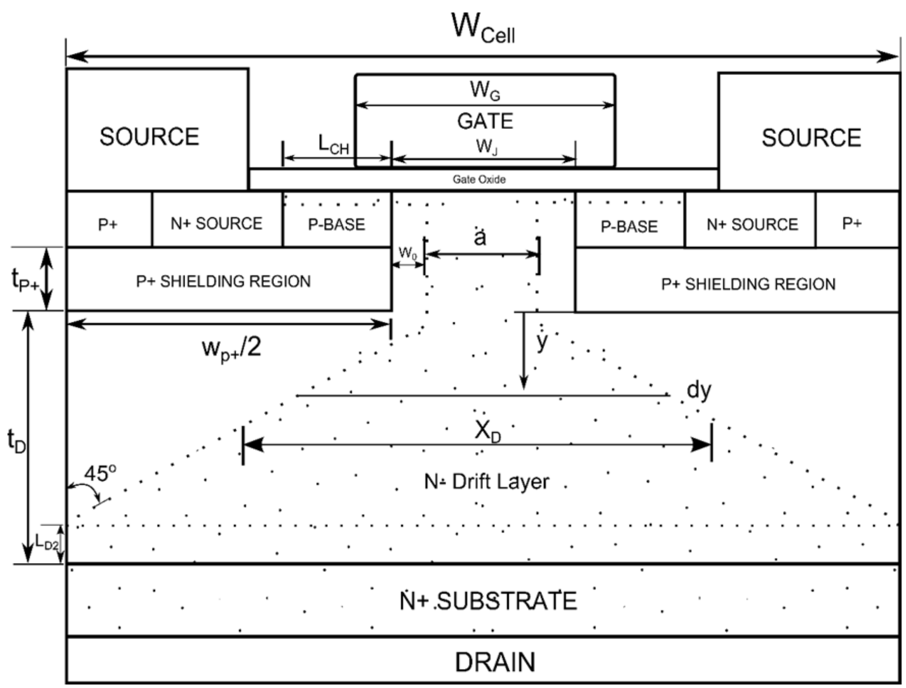


Figure 2.20: Power vertical MOSFET full-cell structure showing current paths in the drift region.

length to sub-micron using self-aligned process [72].

2.4.2 Accumulation Resistance

After the current flow through the channel of the MOSFET, it enters the JFET region at the edge of the p-base region. The resistance of the accumulation region for the half-cell lateral SiC MOSFET structure is given by

$$R_{\mathrm{A}} = \frac{W_{\mathrm{J}}/2}{Z\mu_{\mathrm{nA}}C_{\mathrm{OX}}\left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)} \tag{2.27}$$

where $W_{\mathrm{J}}/2$ is the distance between the edge of the p-base region and the centre of the accumulation region as shown in Figure 2.19 and μ_{nA} is the accumulation layer mobility. In the power vertical MOSFET structure the specific accumulation region resistance is obtained by multiplying the above resistance by the cell area, taking into account that there are two half-cells within a single cell MOSFET structure:

$$R_{\mathrm{A,sp}} = K_A \frac{W_{\mathrm{J}} W_{\mathrm{Cell}}}{4\mu_{\mathrm{nA}} C_{\mathrm{OX}} \left(V_{\mathrm{G}} - V_{\mathrm{TH}}\right)} \tag{2.28}$$

where K_{A} is the coefficient that introduced to account for the current spreading from the accumulation layer into the JFET region with a typical value of 0.6 for SiC power vertical MOSFET as discussed in [73].

2.4.3 JFET Resistance

In the vertical MOSFET structure the JFET region is the region right underneath the accumulation region and above the drift region as shown in Figure 2.19. The current flow in the JFET region is considered to be a uniform, the specific JFET resistance for SiC power vertical MOSFET is given by

$$R_{\mathrm{JFET,sp}} = \frac{\rho_{\mathrm{JFET}} t_{\mathrm{p+}} \times W_{\mathrm{Cell}}}{\left(W_{\mathrm{J}} - 2W_0\right)} \tag{2.29}$$

where ρ_{JFET} is the JFET regions resistivity which can be written as:

$$\rho_{\text{JFET}} = \frac{1}{q\mu_b N_{\text{DJ}}} \tag{2.30}$$

where μ_b is the SiC bulk mobility which related to the doping concentration of the JFET region, and N_{DJ} is the doping concentration in the JFET region. W_0 is the depletion width of the JFET region at zero bias as shown in Figure 2.20, which is given by

$$W_0 = \sqrt{\frac{2\varepsilon_{\text{S}} V_{bi}}{qN_{\text{DJ}}}} \tag{2.31}$$

where V_{bi} is the built-in potential which is related to the doping concentrations of JFET region and the P+ shielding region (N_{A}). The built-in potential for 4H-SiC device is about three times larger than the silicon devices.

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_{\text{A}} N_{\text{DJ}}}{n_i^2}\right) \tag{2.32}$$

2.4.4 Drift Region Resistance

The drift region resistance in the power vertical MOSFET structure is larger than that of the ideal drift region resistance, this is due to the non-uniform current spreading in the drift region. In this thesis, it is assumed that a 45° angle of current spreading from the JFET region as illustrated in Figure 2.20. The specific drift region resistance can be

determined separately from two parts, this first part is the triangular current spreading region and the second part is the uniform current spreading region.

In the first part, the width of the triangular region (X_{D}) at a depth of (y) from the JFET region can be related as

$$X_{\mathrm{D}} = a + 2y \tag{2.33}$$

The resistance of each small segment below the JFET region is therefore

$$\mathrm{d}R_{\mathrm{D}} = \frac{\rho_{\mathrm{D}}\mathrm{d}y}{ZX_{\mathrm{D}}} = \frac{\rho_{\mathrm{D}}\mathrm{d}y}{Z\left(a+2y\right)} \tag{2.34}$$

where Z is the MOSFET cell length in the orthogonal direction to the cross sectional plane. The resistance of the first part of the drift region in the range between $y = 0$ and $y = \mathrm{W}_{\mathrm{P+}}/2$ is therefore given by

$$R_{\mathrm{D1}} = \frac{\rho_{\mathrm{D}}}{2Z} ln\left[\frac{a + \mathrm{W}_{\mathrm{P+}}}{a}\right] \tag{2.35}$$

In the second part of the drift region, the resistance with the uniform cross section width $\mathrm{W}_{\mathrm{Cell}}$ is given by

$$R_{\mathrm{D2}} = \frac{\rho_{\mathrm{D}}}{ZW_{Cell}}\left(t_D + \frac{a}{2} - \frac{W_{Cell}}{2}\right) \tag{2.36}$$

The total specific resistance of the drift region is obtained by adding both parts of resistances and then multiply by the cell area:

$$R_{\mathrm{D,sp}} = \frac{\rho_{\mathrm{D}} W_{\mathrm{Cell}}}{2} ln \left[\frac{a + W_{\mathrm{P+}}}{a} \right] + \rho_{\mathrm{D}} \left[t_{\mathrm{D}} - (W_{\mathrm{P+}}/2) \right] \tag{2.37}$$

where $a = (W_{\mathrm{J}} - 2W_0)$ and ρ_{D} is the resistivity of the drift region.

2.4.5 Total On-Resistance

The total specific resistance for the power vertical MOSFET can be obtained by adding all the resistance components discussed above. The specific resistance of the accumulation, JFET and the channel resistances can be reduced by optimising the width of the JFET region. Increase the width of the JFET region increases the channel resistance and the accumulation resistance. However, the JFET and the drift region resistances will decrease as the width of JFET region increases as discussed in more details in Chapter 3. Simulation results for the specific on-resistance of the shielded planar MOSFET structure with different JFET width are also shown in Chapter 3.

2.5 SiC Oxidation Techniques

Silicon carbide (SiC) is the only wide band-gap semiconductor that can be thermally oxidised to form a native oxide insulator, which has the same properties as the SiO_2 on

Si. This oxide can form a chemically and thermally stable insulation layer as part of the SiC MOSFET structure. It can also be used as a passive oxide film for passivation and edge termination. The thermal oxidation kinetics and the SiO_2/SiC interface is inferior to that of SiO_2/Si interface, which the interface traps density for SiC is at least an order of magnitude higher than the Si [74]. This Section discussed different oxidation techniques that used in this work for fabricating reliable power devices such as diodes and MOSFETs.

2.5.1 Thermal Oxidation Process

The growth process of SiO_2 layer on silicon carbide is similar to the growth on silicon, except that the growth rate of silicon carbide is much slower and requires higher temperatures. Thermal oxidation of silicon is usually performed at a temperature below 1200°C, and dry oxidation temperature for silicon carbide is typically between 1000 and 1300°C [75]. The oxidation process can be carried out in a dry or wet atmosphere. The difference between these two processes are the oxide growth rate and the oxide dielectric breakdown strength. Dry oxidation has higher quality and hence the dielectric breakdown strength is also high, but growth rate is slower. In contrast, the wet oxidation provide a bad interface and oxide quality but faster growth rate [75]. Since the interface and oxide quality is crucial for the performance of SiC power MOSFET, dry oxidation is preferred oxidation process for our work.

Dry oxidation (sometimes called pyrogenic oxidation for temperatures greater than

1200°C) is achieved by supplying an oxygen gas to the high temperature dry environment (>1000°C). Dry oxidation results in a very good interface quality ($10^{11} - 10^{12}$ cm^{-2}eV^{-1} for 4H-SiC) and high dielectric breakdown (11-12 MV/cm) [75]. Depending upon the oxygen concentration, high temperature oxidation of silicon carbide may be either active or passive. When the oxygen pressure is less than one bar, it is regarded as active oxidation according to the following equation:

$$\mathrm{SiC(s) + O_2(g) \rightarrow SiO(g) + CO(g)} \tag{2.38}$$

SiO formed gets vaporised after its formation leading to loss of mass according to the oxidation model [76]. There are three chemical reactions in the case of active SiC oxidation, which are SiC with SiO_2, SiC with O_2 and SiC with H_2O for the case of wet oxidation. All of them result in the formation of SiO and CO gases. These gases react with oxygen to produce CO_2 (gas) and SiO_2 (solid) which is deposited on the oxide interface.

In the case of passive oxidation, SiO_2 is directly produced from the first chemical reaction with O_2 in the oxidation environment. There are no intermediate reactions or product such as SiO. Passive oxidation occur by the following reaction

$$\mathrm{2SiC(s) + 3O_2(g) \rightarrow 2SiO_2(s) + 2CO(g)} \tag{2.39}$$

Different dry oxidation temperatures have been employed during this thesis: 1200°C,

1300°C, 1400°C and 1500°C. The details of oxidation procedure is discussed in Chapter 6.

2.5.2 Novel High Temperature Oxidation

A typical oxidation furnace which designed for silicon has maximum temperature of about 1200°C. However, a higher oxidation temperature is usually required for SiC because the oxidation rate is much slower for SiC compare with for Si [51, 52, 77, 78]. It has been reported in some literature that oxidation at 1200°C results in the formation of high defect density near the SiO_2/SiC interface. Although the origin of these interface trap charges which lead to high interface trap density and degrade the channel mobility is not well understood, it is believed that the carbon dimer [79] in the SiC and intrinsic oxide defects [80, 81] are responsible. Many researchers have mainly focused on passivating the traps after oxide growth with nitrogen or phosphorus to reduce the D_{it} and also increase the field effect mobility [16,31,51,52]. Dry oxidation of SiC at high temperature (≥1200°C) was also reported in the literature to reduce the D_{it} [82, 83], although [83] indicates that the corresponding MOSFETs have a mobility of about 2 cm^2/V.s. Recent work by our research group in the University of Warwick has shown that D_{it} can be reduced to about 2 cm^2/V.s by oxidation at higher temperature (1500°C) under a low oxygen flow rate [32]. MOSFET fabricated under 1500°C in an ambient of 7% oxygen and 93% argon results the peak field effect mobility of approximately 40 cm^2/V.s [33].

2.5.3 Post Oxidation Annealing

Post oxidation annealing after the oxide grown can effectively passivate the interface traps between the SiC/SiO_2 interface. Post oxidation annealing in many different ambients have been reported in literature such as argon (Ar), hydrogen (H), helium (He), nitric oxide (NO), nitrous oxide (N_2O) and phosphorous [16, 46, 53]. Nitrous oxide and phosphorous passivation on 4H-SiC MOS capacitor and MOSFET are the main focus of this work.

The theory of N_2O passivation is that the Si $\equiv$ N bonds that are created at the SiO_2/SiC interface can (a) passivate the interface traps due to dangling and strained bonds and (b) act as a barrier for removal of carbon-oxides and other complex silicon oxides compounds. The incorporation of nitrogen during post oxidation annealing can also reduce stress between SiC and oxide because of the large mismatch between 4H-SiC and SiO_2 as discussed in as discussed in [84].

Phosphorous passivation in a P_2O_5 ambient which converts the SiO_2 layer to PSG (phosphosilicate glass) [53] has shown to have best result so far in this work with peak mobility up to approximately 80 cm^2/V.s on 4H-SiC MOSFET(0001) face with Al+ implanted P-body. Details of fabrication and characterisation results on 4H-SiC MOS capacitors and MOSFETs are shown in Chapter 6 and Chapter 7.

2.5.4 N_2O Grown Oxide

Direct growth oxide under N_2O environment has also been investigated and compared with other post oxidation annealing techniques. Some authors [85] have reported that oxides grown in N_2O have better reliability under high-field stress compared to those annealed in N_2O on 6H-SiC. And [16] also support this finding that the direct grown oxides in a nitrogen rich ambient exhibit better electrical properties compared to those annealed in N_2O. However, [46] indicates that results on oxide grown on 4H-SiC in 100% pure N_2O on SiC were not encouraging, as D_{it} and the near-interface trap density were increased, whereas the oxide grown in diluted N_2O results in improvements. This suggests that the rates of carbon accumulation and carbon removal are closer in diluted N_2O. Diluted N_2O (20% N_2O and 80% Ar) was used in this work because of the flow rate limitation of N_2O gas (maximum 1 L/min) in our clean room. To prevent O_2 in the air entering into the furnace, the N_2O oxidation process is mixed with Ar gas. Oxide grown under diluted N_2O environment in Ar for 4H-SiC MOS capacitors and MOSFETs have been fabricated and electrically characterised. Results are shown in Chapter 6 and Chapter 7.

2.6 Device Fabrication Technology

This section aims to introduce the technology difference in fabricating SiC compare to Si. Etching of SiC, ion implantation and activation and formation of ohmic contact will be discussed. Processing equipment utilised in the fabrication of SiC devices are discussed in

relevant Chapters in this thesis, and the details of cleaning and photolithography process are outlined in the Appendix B and Appendix C of this thesis.

2.6.1 SiC Etching

The etching process is a fundamental in the fabrication of the most semiconductor devices. There are two type of etching: dry etching and wet etching. Wet etching of SiC requires the use of molton salts, such as potassium hydroxide (KOH) or sodium hydroxide (NaOH) at temperature of around $600 - 800°C$. Dry etching is anisotropic etch and avoids undercutting of material which typically happened to wet etching techniques. Due to the chemical inertness of 4H-SiC, it is difficult to etch 4H-SiC in conventional acid or base solutions, as can be used in Si. It is favourable to employ dry, plasma-based etching techniques for 4H-SiC. Typical SiC dry etch chemistries are based on fluorinated plasmas such as fluoroform (CHF_3) or sulfur hexafluoride (SF_6).

The most commonly reported dry etching method for SiC is reactive-ion etching (RIE). RIE etching is done by immersing the material to be etched into a gas discharge that initiates ion bombardment and contact with a chemical reactive species. The RIE recipe (50 sccm SF_6 + 3 sccm O_2) was used in this work. However, the ion bombardment on the SiC would result in relatively high surface damage, which decreases the overall carrier lifetime in the device. As such, high-density plasma source etching methods, such as inductively coupled plasma (ICP) etching is favoured over RIE if the etching depth is less

than 2μm. The ICP etching recipe (100 sccm CHF_3 + 5 sccm O_2) was used in this work. ICP etching provides better results in terms of etching rate and surface roughness as reported in [86]. Therefore, for devices fabricated in this research, ICP etching of 4H-SiC has been employed.

2.6.2 Ion Implantation and Activation Annealing

Unlike for Si semiconductor, where selectively doped region can be realised by using thermal dopant diffusion. The dopant diffusion process cannot be simply applied to the fabrication of 4H-SiC device due to the low diffusion coefficients of the main dopant species. As such, ion implantation is the most widely used technology for realising doping regions in 4H-SC devices.

Ion implantation in 4H-SiC require higher implant energies than in Si, in the range of keV to MeV depending on the depth of the implants. These junction depths are typically limited to below 1 μm. The common P-type dopants for 4H-SiC are aluminium (Al) and boron (B), and boron is preferred if deeper junction is needed as it has smaller atomic size. However, the aluminium has the advantage of having a shallower ionisation energy, meaning that larger P-type carrier concentrations in the freeze-out temperature region are realised. And lower sheet resistances are achievable with aluminium doped 4H-SiC when compared to boron-doped 4H-SiC. For the n-type dopant for 4H-SiC, nitrogen and phosphorous are the most commonly used implanted species. Nitrogen is more suitable

when deep implants are required as it has deeper projected range than phosphorous for the same energy. However, as reported in [87], the phosphorous implants achieve sheet resistance of approximately an order of magnitude lower than that which is achieved for nitrogen implants. This is due to the higher activation ratio of implanted phosphorous compared to nitrogen.

The advantage of ion implantation is that it allows accurate control of the charge introduced into the semiconductor material. However, the implantation process also causes damage to the crystal structure of the semiconductor, and may also create defects in the implanted regions of the semiconductor material [88]. To activate these dopant atoms and reducing the damage in the semiconductor crystal, a high temperature thermal annealing is required. A temperature of ~1300°C is required to activate n-type dopants and temperature of ~1600°C or higher is generally required for aluminium and boron. In this work, activation temperature of 1600°C for 45 minutes have been employed for 4H-SiC devices and has found to be sufficient in activate both n-type and p-type dopants.

2.6.3 Ohmic Contacts to 4H-SiC

Creating a reliable, low resistance ohmic contacts to 4H-SiC is difficult, particularly for p-type 4H-SiC. This is because of the poor dopant activation and ionisation for the p-type dopant species. This means that at room temperature there are very few carriers available for current transport. A good ohmic good contact to 4H-SiC is important

if low on-state power losses are to be minimised, and if high switching speeds are to be realised. The typical process that is applied to form ohmic contacts on 4H-SiC is to deposit suitable metals on heavily doped n- or p-type regions, then perform a post-deposition anneal. A short high temperature anneal usually allows ohmic contact to be formed. The contact resistance is dependent on several factors, including metals used, doping concentration of the semiconductor, surface treatment prior to metal deposition and the annealing conditions.

The formation of ohmic contact to n-type SiC has been widely studied [89–91]. Most of the work involved the use of nickel (Ni) and Ni-based alloys for the contact metal, such as titanium (Ti), tantalum (Ta), niobium (Nb) and molybdenum (Mo) [92]. The typical specific contact resistances to n-type 4H-SiC is in the order of 10^{-6} $\Omega.cm^2$. For p-type 4H-SiC it is more difficult to form the ohmic contact because of the wide bandgap of 4H-SiC as discussed before. Therefore, in order to achieve ohmic behaviour, the semiconductor underneath the contact is heavily doped so as to facilitate field emission current transport through potential barrier [93]. However, in practice the heavily doped p-type region in 4H-SiC is difficult to achieve due to the poor dopant ionisation of acceptors at the room temperature. As discussed in [94] and [95], metallisation schemes based on Ti/Al alloys have yielded the best results in terms of specific contract resistance, both for epitaxial and implanted p-type 4H-SiC. With Al/Ti/Al metallisation scheme reported in [95], the lowest specific contact resistance of 5×10^{-6} $\Omega.cm^2$ is achieved. However, the resistance values that are reported by different research groups vary significantly even for the similar

metallisation scheme and annealing conditions. This suggest that the semiconductor material quality and pre-deposition surface treatment both play important role in achieving low contact resistance.

2.7 Summary

In this chapter, the technical aspects of high voltage 4H-SiC power MOSFET have been presented. This includes a detailed analysis of the forward and reverse breakdown characteristics of vertical power MOSFET, the effect of different junction termination extension (JTE) designs on the breakdown voltage and the on-resistance of vertical MOSFET. Different oxidation techniques on 4H-SiC to improve the interface quality as well as the oxide reliability were discussed next, with the most promising results of N_2O and Phosphorous passivation being identified for incorporation into the device fabrication. Finally, 4H-SiC device fabrication technology and some issues have been presented, such as implant activation and ohmic contact on 4H-SiC.

Chapter 3 Design and Simulation of High Voltage 4H-SiC MOSFETs

The design and optimization of 4H-SiC power MOSFET and junction termination extension (JTE) is presented in this chapter. The numerical simulations were carried out using the finite element simulation software SILVACO. Designs are evaluated using simulated electrical characteristics including on-state I-V and breakdown performance. The device designs which include the drift layer design to support the high voltage (1 kV, 3 kV and 10 kV) are presented. Both conventional planar power MOSFET and shielded planar VD-MOSFET structures design are illustrated. On-state I-V simulations are presented in order to optimise the on-state performance of the MOSFET. Reverse breakdown simulations are carried out for different junction termination extension (JTE) structures, and a novel junction termination scheme has been developed and simulated, in order to achieve a blocking voltage that is closer to the ideal parallel plane breakdown voltage and has wider optimum doping window.

3.1 4H-SiC Planar Power MOSFET Design

In the design of power MOSFET, one of the first thing to consider is the specification of the drift region, which determines the breakdown voltage. This drift region is typically formed by growing a lightly doped epitaxial layer on a highly doped substrate. There are two key parameters need to be considered for drift layer design, the doping concentration, N_{D}, and the drift region thickness, W_{D}. The goal of the drift region design is to minimise the power dissipation while maintaining the desired blocking voltage rating in the off-state.

The drift region design of power MOSFET can be done by the analysis of a one-dimensional abrupt junction structure. Figure 3.1 illustrates an non punch-through P-i-N structure and its corresponding electric field profile at breakdown, where P+ side is very highly doped region. When a positive bias is applied to the P+/N− junction, a depletion

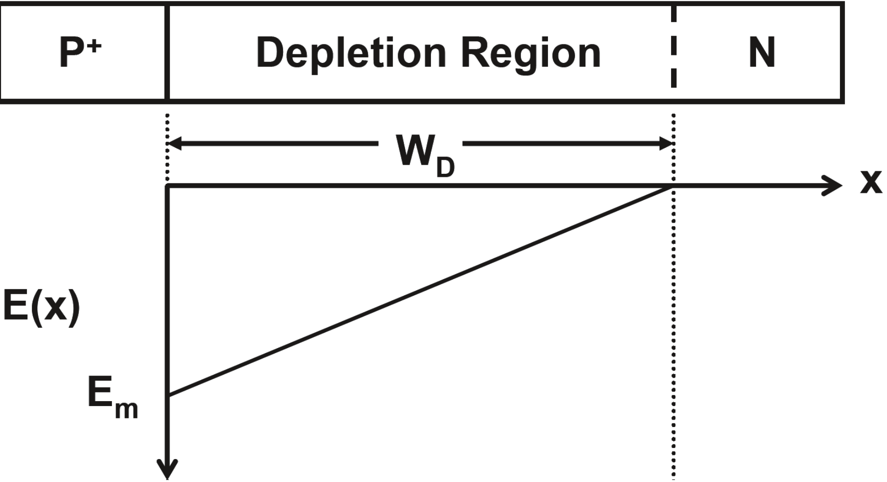


Figure 3.1: Electric field profile at breakdown for non-punch-through P-i-N diode structure. [44]

region is formed within the N- region and it can support voltage. From the Poisson's equitation, it is known that

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = -\frac{\mathrm{d}E}{\mathrm{d}x} = -\frac{Q\left(\mathrm{x}\right)}{\varepsilon_{\mathrm{S}}} = -\frac{qN_{\mathrm{D}}}{\varepsilon_{\mathrm{S}}} \tag{3.1}$$

where N_{D} is the doping concentration of the drift region, ε_{S} is the semiconductors dielectric constant.

By integrating the equation 3.1 with the boundary condition (from x to the depletion wdith W_{D}:

$$E\left(\mathrm{x}\right) = -\frac{qN_{\mathrm{D}}}{\varepsilon_{\mathrm{S}}}\left(W_{\mathrm{D}} - \mathrm{x}\right) \tag{3.2}$$

Integrate the electric field gives the potential distribution in the depletion region:

$$V(\mathrm{x}) = \frac{qN_{\mathrm{D}}}{\varepsilon_{S}}\left(W_{\mathrm{D}}\mathrm{x} - \frac{\mathrm{x}^2}{2}\right) \tag{3.3}$$

The depletion region thickness can also be related to the applied voltage (Va):

$$V\left(W_{\mathrm{D}}\right) = V_{\mathrm{a}} \tag{3.4}$$

$$W_{\mathrm{D}} = \sqrt{\frac{2\varepsilon_{\mathrm{S}} V_{\mathrm{a}}}{qN_{\mathrm{D}}}} \tag{3.5}$$

Substitute equation into equation , the maximum electric field is:

$$E_{\mathrm{m}} = \sqrt{\frac{2qN_{\mathrm{D}}V_{\mathrm{a}}}{\varepsilon_{\mathrm{S}}}} \tag{3.6}$$

The breakdown voltage can be determined by:

$$\int_{0}^{W} a \,\mathrm{d}x = 1 \tag{3.7}$$

where a is the impact ionization coefficient, which is material dependent and can be obtained by different power law as discussed in [44]. Using Baliga's power law for 4H-SiC as discussed in [96] and equations 3.7 and 3.1, the breakdown voltage and the depletion width can be related to the doping concentration of the drift region, which are:

$$BV_{\mathrm{PP}}(\text{4H-SiC}) = 3.0 \times 10^{15} N_{\mathrm{D}}^{-3/4} \tag{3.8}$$

and

$$W_{\mathrm{PP}}(\text{4H-SiC}) = 1.82 \times 10^{11} N_{\mathrm{D}}^{-7/8} \tag{3.9}$$

The critical electric field can be also given by combining equations 3.6 and 3.8:

$$E_{\mathrm{C}}(\text{4H-SiC}) = 3.3 \times 10^{4} N_{\mathrm{D}}^{1/8} \tag{3.10}$$

The breakdown voltage, maximum depletion width and critical electric field as a function of doping concentration on the N- drift region are shown in Figure 3.2 to Figure 3.4. For the same doping concentration, 4H-SiC has higher breakdown voltage and larger

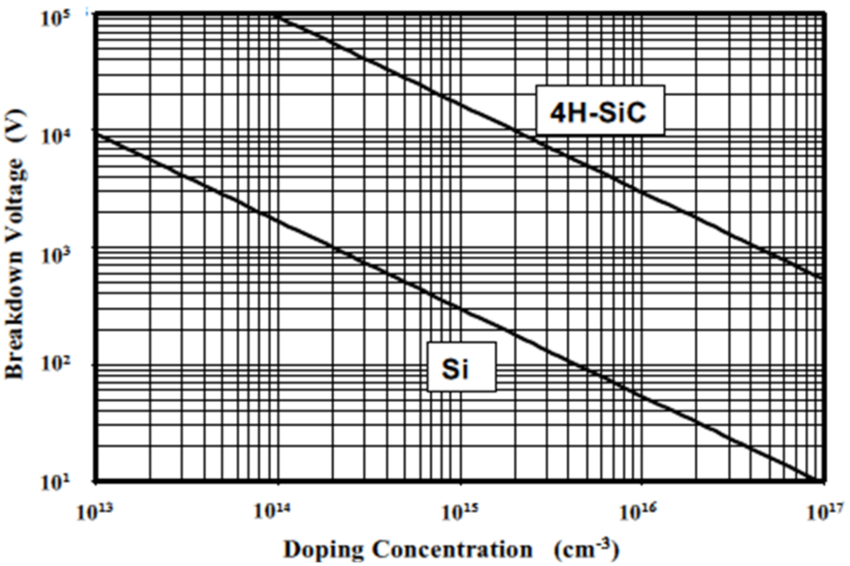


Figure 3.2: Breakdown voltage as a function of N- region doping concentration in both Si and 4H-SiC [44].

maximum depletion width than in silicon. It is about 56.2 times higher in breakdown voltage, 6.8 times larger in maximum depletion width and 8.2 times larger in critical electric field in 4H-SiC than in silicon [44]. However, for the same breakdown voltage, 4H-SiC has smaller depletion width and larger doping concentration in the drift region than Si. This will result significant reduction in the specific on-resistance of the drift region in SiC compared with Si.

In the bipolar power devices, such as P-i-N diode, because of the conductivity modulation effect, the on-state resistance of the device does not depend upon the drift region

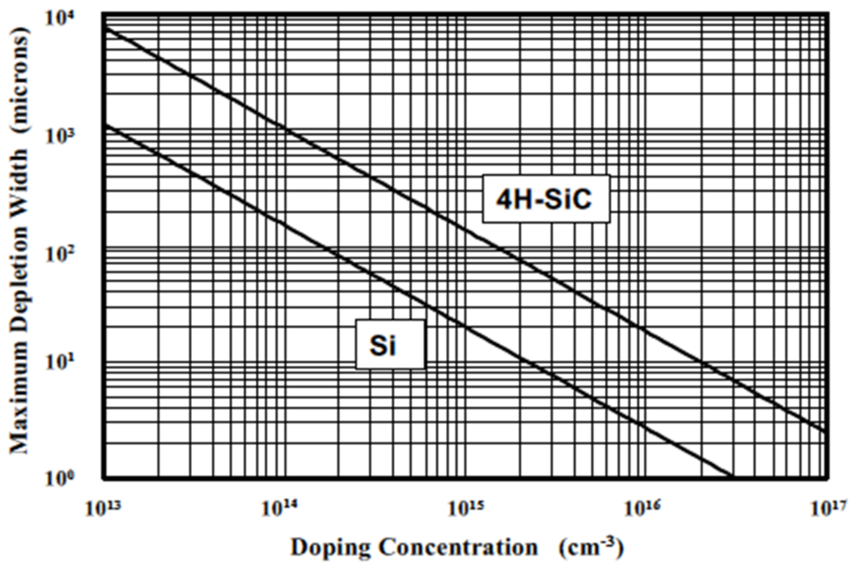


Figure 3.3: Maximum depletion width versus of N- region doping concentration in both Si and 4H-SiC. [44].

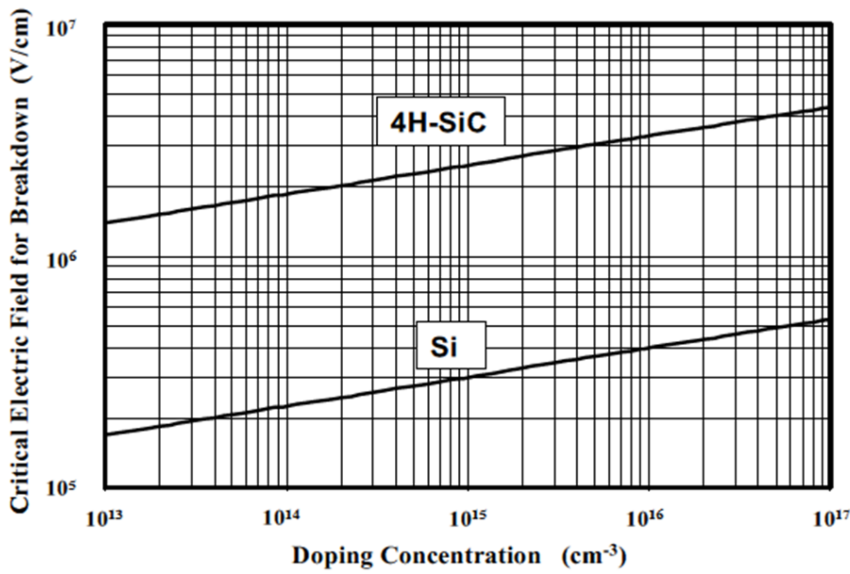


Figure 3.4: Critical electric field as a function of N- region doping concentration in both Si and 4H-SiC [44].

doping concentration alone. A punch-through structure is usually used for P-i-N diode because it can provide the same breakdown voltage with thinner epitaxial layer. Figure 3.5 shows a punch-through P-i-N structure and its corresponding electric field profile at breakdown.

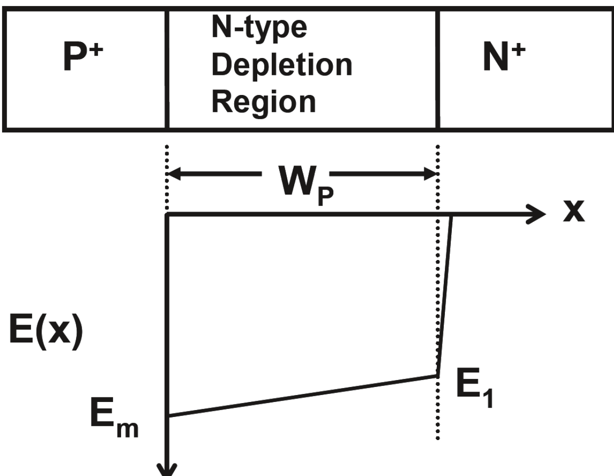


Figure 3.5: Electric field profile at breakdown for punch-through P-i-N diode structure [44].

Compare to the triangular electric field distribution as shown in Figure 3.5, the electric field for the punch-through structure has a trapezoidal shape. By integrating the area of the electric field profile, the punch-through drift region can be designed using the following equation:

$$BV_{\mathrm{PT}} = E_{\mathrm{C}} W_{\mathrm{D}} - \frac{q N_{\mathrm{D}} W_{\mathrm{D}}^2}{2\varepsilon_{\mathrm{S}}} \tag{3.11}$$

The breakdown voltage is directly proportional to the drift regions thickness. As the

drift regions thickness is reduced the breakdown voltage will be reduced. From the design point of view, it is possible to obtain a breakdown voltage with half of the drift region thickness that used in the non-punch through design. This reduced drift region thickness with the punch-through design has advantage for reducing the on-state voltage drop as well as reducing the stored charge and therefore reduce the reverse recovery power loss.

3.1.1 Drift Layer Design

Based on the one-dimensional parallel-plane junction as illustrated in Figure 3.1, the equations for the breakdown voltage, the corresponding maximum depletion width and the critical electric field can be derived for 4H-SiC. However, recent publications [67,97,98] and our simulation results have shown that the previous equations (3.8 to 3.10) published by Baliga [44] for breakdown voltage of 4H-SiC are overestimated by up to 80%. Figure 3.6 shows the breakdown voltage as a function of drift region doping concentration for different estimation methods [44, 97, 98] for a 100 μm epi-layer 4H-SiC.

The equation for impact ionisation rate as function of electric field used in this work is from literature [97], which is shown in equation 3.12. Equations 3.13 to 3.15 show the breakdown voltage, depletion width and the critical electric field as function of drift region doping concentration for 4H-SiC.

$$a = 1.746 \times 10^{-35} \times E^{6} \tag{3.12}$$

$$BV_{\mathrm{PP}} = 4.766 \times 10^{14} \times N_{\mathrm{D}}^{-5/7} \tag{3.13}$$

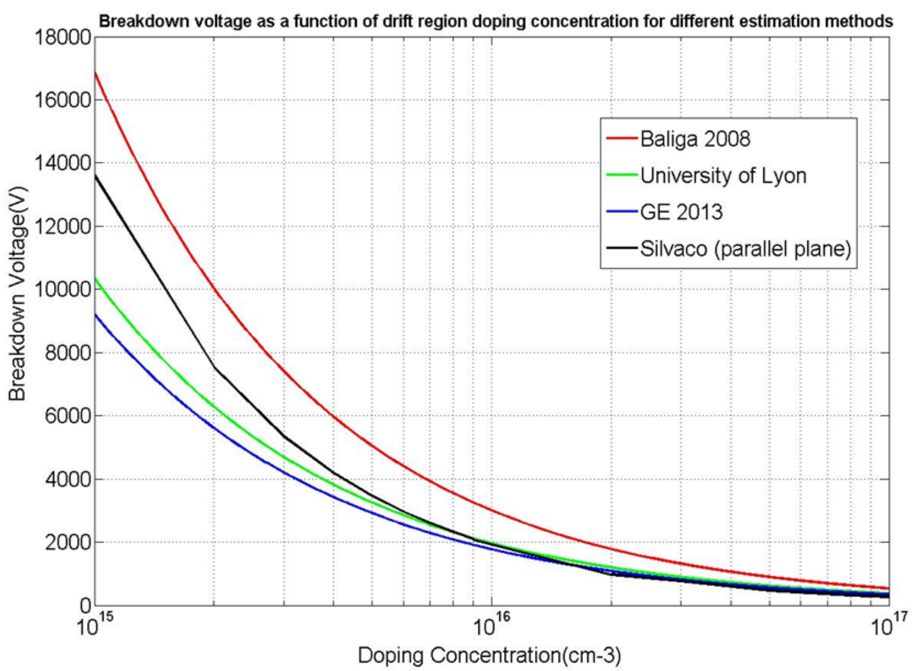


Figure 3.6: Breakdown voltage as a function of doping concentration of 4H-SiC with different estimation methods.

$$W_{\mathrm{PP}} = 7.151 \times 10^{10} \times N_{\mathrm{D}}^{-6/7} \tag{3.14}$$

$$E_{\mathrm{C}} = 1.333 \times 10^{4} \times N_{\mathrm{D}}^{1/7} \tag{3.15}$$

where a is the impact ionization coefficient, N_{D} is the doping concentration of drift region in cm^{-3}, W_{PP} is the maximum depletion layer width in cm, BV_{PP} is the breakdown voltage in V and E_{C} is the critical electric field in V/cm.

From equations 3.13 and 3.14 one can estimate the drift region doping concentration and drift region thickness for a required breakdown voltage. A breakdown voltage of 1 kV can be obtained in 4H-SiC by using a doping concentration of $N_{\mathrm{D}} = 2.23 \times 10^{16}$ cm^{-3} with drift region thickness of approximately W_{D}=7 μm. For a 3.3 kV-rated device, the drift

region thickness needs to be approximately $W_{\mathrm{D}} = 30\ \mu$m and the doping concentration of N_{D}=4×10^{15} cm^{-3}. Similarly for a 10 kV rated-device, the drift region thickness needs to be 110 μm and doping concentration of 8×10^{14} cm^{-3}.

3.1.2 Shielded Planar Inversion-Mode Structure

The conventional planar power VD-MOSFET design that is often used in silicon is not suitable for the development of silicon carbide devices as discussed in [96]. Although most of the commercial 1.2 kV SiC MOSFET still using the conventional VD-MOSFET design, for high voltage SiC MOSFET ($>$ 10 kV) a shielded planar structure which is achieved by using retrograde P-body doping profile is usually required [99, 100]

Because of the much larger bandgap of silicon carbide and the fact that the intrinsic carrier concentration is far smaller than that for silicon. At room temperature (300 K), the intrinsic carrier concentration (n_i) for silicon is 1.4×10^{10} cm^{-3} while that for 4H-SiC is only 6.7×10^{-11} cm^{-3} [44]. As discussed in Chapter 2 of this thesis, the threshold voltage is proportional to the square root of $\ln\left(\frac{N_{\mathrm{A}}}{n_i}\right)$, which means that a larger threshold voltage is required to create an inversion layer. For 4H-SiC inversion-mode MOSFET structures as shown in Figure 3.7, with a gate oxide thickness of 50 nm and P-base doping concentration of 2×10^{16} cm^{-3}, the analytical model predicts a threshold voltage of about 5 V. Such a low P-base doping concentration cannot sustain a high blocking voltage with the conventional planar power VD-MOSFET structure, due to reach-through of the depletion layer in the

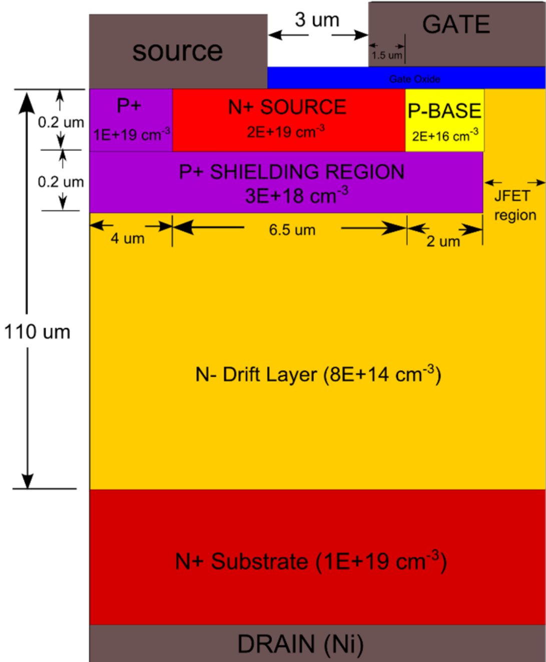


Figure 3.7: Shielded planar inversion-mode power VD-MOSFET structure.

P-base region. On the other hand, if the doping concentration of the P-base is increased to sustain high blocking voltage, the threshold voltage would be too high. The much larger electric field in the silicon carbide drift region under the gate oxide will also cause the early breakdown of the gate oxide.

These issues can be addressed by using a shielded region (highly dose P+ region) to suppress the high electric field developed in the drift region to reach to the gate oxide. The concept of the shielded planar structure was first proposed by Baliga [101] in 1990s. The P+ shielded region can be formed by separate P+ doping or by retrograde doping profile which was used in this work. The detailed structure and doping concentration for the 10 kV shielded planar power VD-MOSFET is shown in Figure 3.7.

The shielded planar structure contains an extra P+ shielding layer under the P-base region as shown in Figure 3.7. The P-base and the P+ shielding region can be achieved at the same time by using a single implantation with a retrograde doping profile (Details of implantation profiles are shown in Chapter 7). When the MOSFET is turned on, an inversion layer is formed at the surface of the P-base region enabling a conduction between the source and the drain. For the low breakdown voltage devices (up to 1 kV) the specific on-resistance is limited by the channel resistance due to the low channel mobility. For the high breakdown voltage device (>10 kV) the specific on-resistance is limited by the drift resistance as the channel resistance is not dominant resistance in the 10 kV 4H-SiC MOSFET. However, the channel resistance is still important for the higher voltage 4H-SiC power MOSFETs as it affects the on-state performance and the output current of the device. Field effect mobility of high voltage 4H-SiC power MOSFET is typically in the range of $1-40$ cm^2/V.s [55, 102] although larger values (up to 165 cm^2/V.s) have been reported in lateral MOSFETs [68].

In the conventional planar silicon carbide power VD-MOSFET structure, the thickness and the doping concentration of the P-base region are constrained by the reach-through limitation as discussed before. However, in the shielded planar power VD-MOSFET structure this is not a problem since the P+ shielding region shields the P-base region from the drain potential. Therefore the P-base regions doping concentration can be reduced to achieve a desired threshold voltage without the reach-through problem which causes the early breakdown of the device.

3.1.3 Power VD-MOSFET Cell Optimisation

As discussed in Chapter 2 that the total on-resistance of power VD-MSOFET can be minimised by adjusting the width of the JFET region. The channel resistance and the accumulation resistance will increase when the width of JFET region is increased, however, the JFET and drift region resistances will reduce if the width of JFET region is increased. Therefore, it is necessary to optimise the width of JFET (W_{J}) to obtain the lowest possible specific on-resistance.

3.1.3.1 Optimisation of JFET width

The optimisation process for the power VD-MOSFET was carried out using the finite element simulation software SILVACO. To find out the optimum JFET width for the power VD-MOSFET structure, the JFET width was varied from 1 μm to 10 μm in the simulation. Since the lateral dimensions (i.e. widths of the channel, JFET and cell pitch regions) are the same for all 1 kV, 3.3 kV and 10 kV VD-MOSFETs design, the simulation was performed on a 1 kV rating VD-MOSFET structure and the results were apply to the 3.3 kV and 10 kV VD-MOSFETs design. The computation time for simulation 1 kV device was greatly reduced compare to 10 kV device because of the much thinner drift region and much lower number of mesh points required for reliable results.

Figure 3.8 shows the numerical simulation for 1 kV VD-MOSFET structure when the JFET region width is increased from 1 to 10 μm while keeping the window size from P+

region to the edge of P-body the same. A gate bias of 20 V and drain source voltage of

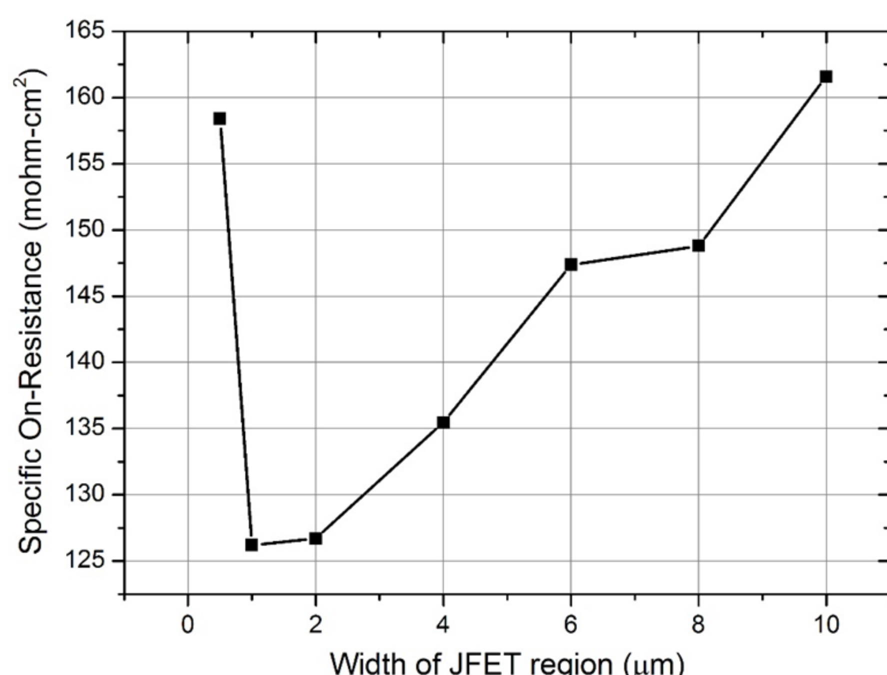


Figure 3.8: Simulation result of specific on-state resistance for 1 kV shielded planar VD-MOSFET with different width of JFET region.

1.5 V was used in this plot. Figure 3.9 to 3.11 show the impact of different width of the JFET region on the specific on-resistance for the 1 kV, 3.3 kV and 10 kV shielded planar VD-MOSFET. An inversion layer mobility of 20 $cm^2/V.s$ was used for this analysis.

From Figure 3.8 it is seen that there is a low total specific on-resistance for structures with JFET region width in a range of 1 to 2 μm. However, the specific on-resistance increases sharply if the JFET region width is less than 1 μm and beyond 5 μm. The resistance of the JFET region and drift region will increase significantly when the JFET region width is less than 1 μm, which leads to increase of total specific on-resistance. From

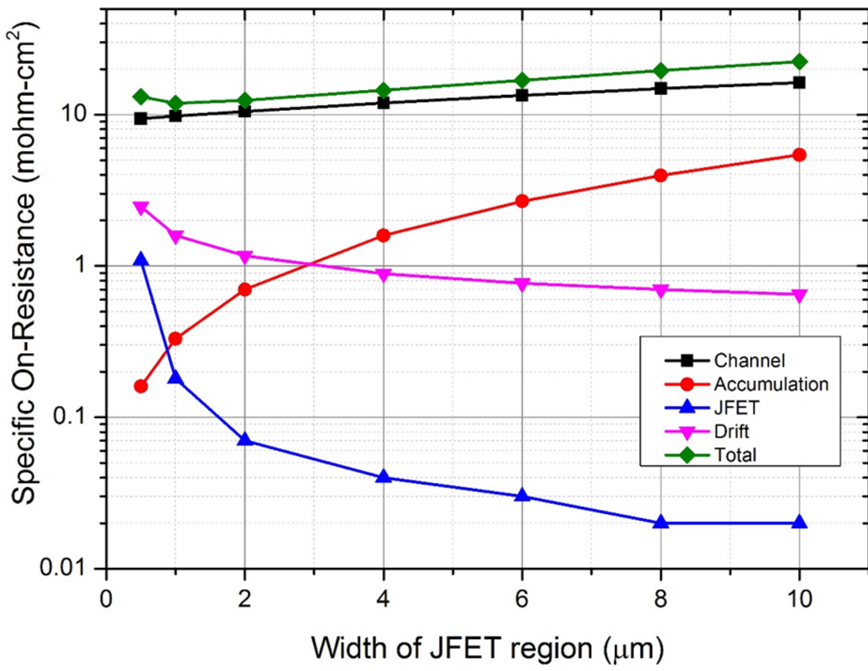


Figure 3.9: Specific on-state resistance for the 1 kV shielded 4H-SiC shielded planar MOSFET structures from the analytical model calculations.

the analytical model calculations as shown in Figure 3.9 to Figure 3.11, it is seen that the resistance contribution from the channel and accumulation region become dominant when the JFET region width exceeds 10 μm. For 1 kV shielded planar VD-MOSFET, the total specific on-resistance is dominated by the channel resistance which contribute to about 90% of the total on-resistance of the VD-MOSFET as shown Figure 3.9. For the 3.3 kV shielded planar VD-MOSFET, the contribution of the drift region to the total on-resistance has increased close to that of the channel resistance, and the drift resistance will be higher than the channel resistance if the width of JFET region is less than 2 μm as shown in Figure 3.10. However, for the 10 kV shielded planar VD-MOSFET the largest contribution to the total on-resistance is the drift region resistance as shown in Figure

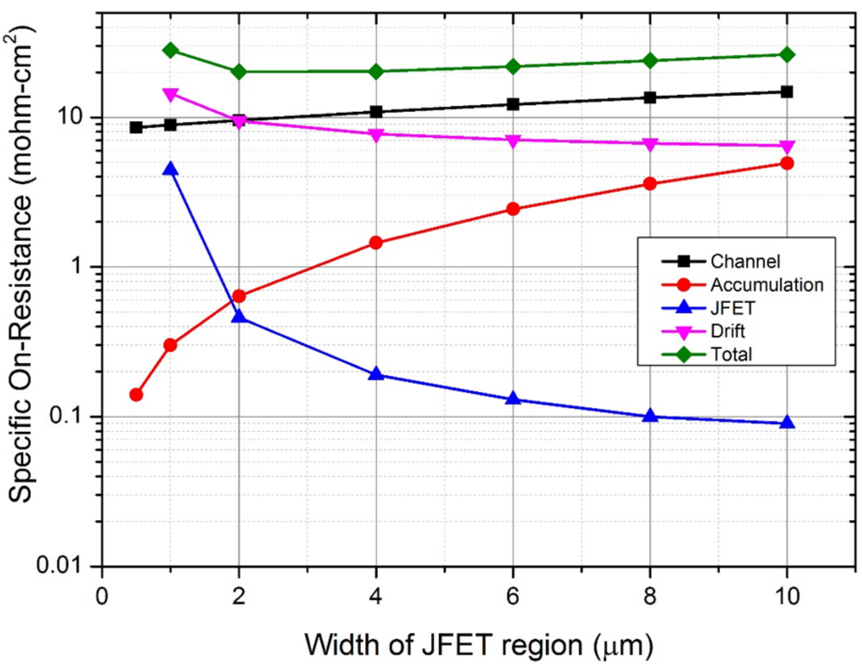


Figure 3.10: Simulation result of specific on-state resistance for 3.3 kV shielded planar VD-MOSFET with different width of JFET region from the analytical model calculations.

3.11.

The two-dimensional numerical simulations of breakdown voltage for the 1 kV shielded planar VD-MOSFET structure is shown in Figure 3.12. It is seen that the breakdown voltage increases when the width of the JFET region is decreased. With JFET region width larger than 8 μm, the breakdown voltage reaches a plateau at 850 V. The improvement of breakdown voltage with smaller JFET region can be explained by examination of the potential distribution in the shielded planar VD-MOSFET structure. Figure 3.13 shows the potential distribution for the shielded planar VD-MOSFET with JFET cell pitch width of 10 μm. It can be observed that a depletion region is formed below the P-body region and under the gate oxide region. A crowding of the potential contours

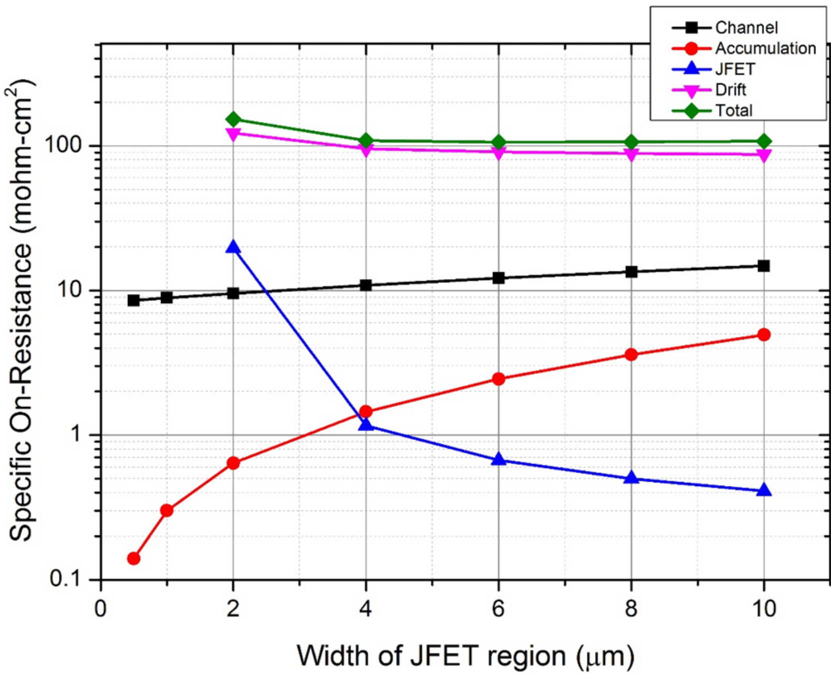


Figure 3.11: Simulation result of specific on-state resistance for 10 kV shielded planar VD-MOSFET with different width of JFET region from the analytical model calculations.

is observed at location "A" in Figure 3.13, which reduces the breakdown voltage of the device. When the JFET region width is reduced the crowding of the potential contour is also reduced as shown in Figure 3.14 with the JFET region width of 1 μm. From Figure 3.14 it is seen that the reduction of the JFET width in the VD-MOSFET structure can reduce the electric field at the junction, and therefore can support a larger voltage. Therefore in order to have a low on-resistance and acceptable breakdown voltage of the shielded planar VD-MSOFET structure, the JFET region width of 2 μm was chosen for the design for shielded planar VD-MOSFETs (1 kV and 3.3 kV) in this work.

A JFET region doping enhancement is usually required to reduce the on-state resistance for high voltage 4H-SiC devices (>5 kV) due to the low doping concentration in the

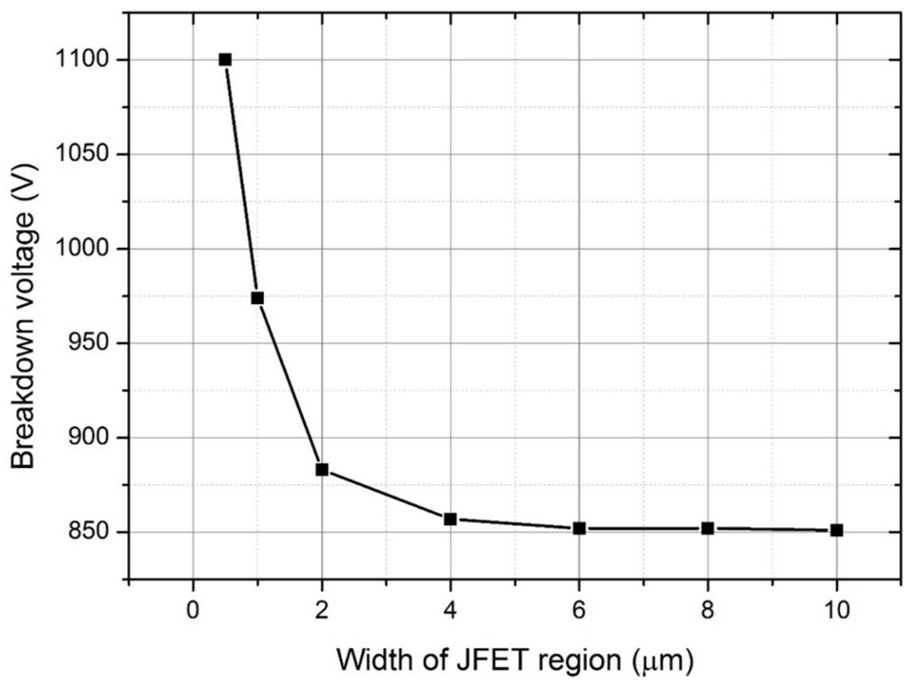


Figure 3.12: Simulated breakdown voltage of the 1 kV shielded planar VD-MOSFET structure with different JFET region width.

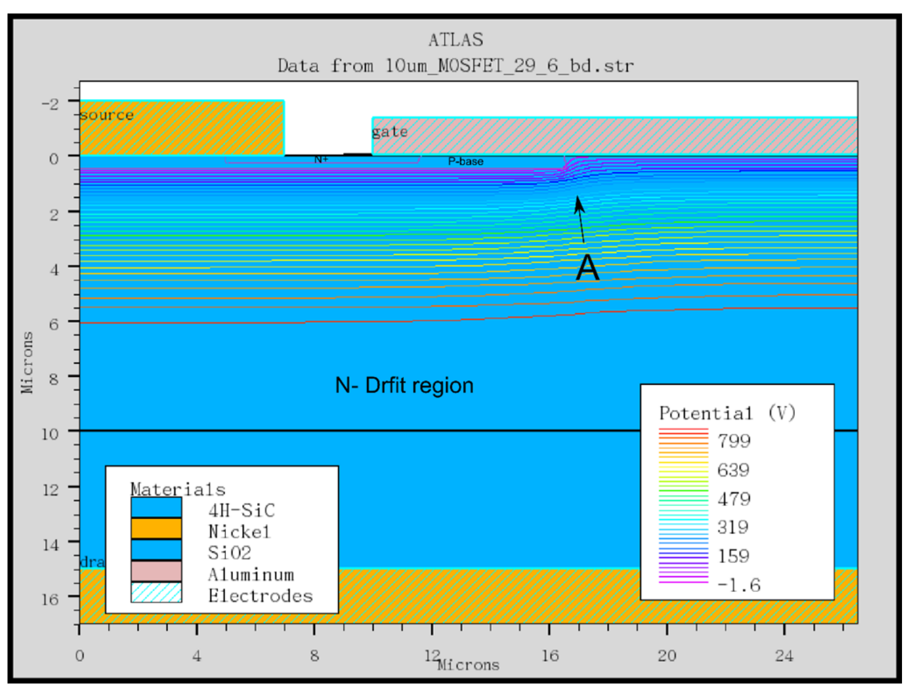


Figure 3.13: Potential contours for the shielded planar VD-MOSFET structure with JFET region width of 10 μm.

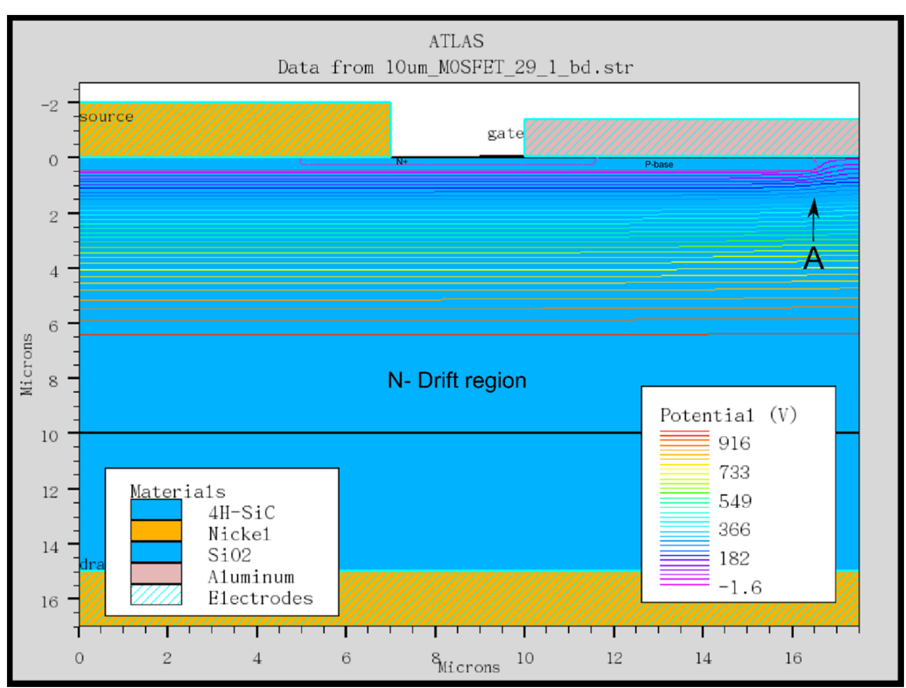


Figure 3.14: Potential contours for the shielded planar VD-MOSFET structure with JFET region width of 1 μm.

drift region as discussed in [44]. Although this was not implemented in the fabrication work, numerical simulation have been performed to verify the effect JFET region doping concentration on the breakdown voltage of the VD-MOSFET structure. The enhanced doping concentration was extended to 0.5 μm below the P+ shielding region. The JFET region resistance is related to JFET region doping concentration (N_{DJ}) as discussed in Chapter 2:

$$R_{\mathrm{JFET,sp}} = \frac{\rho_{JFET} t_{\mathrm{P+}} W_{cell}}{(W_J - 2W_0)} \tag{3.16}$$

where the resistivity of the JFET region ρ_{JFET} is given by

$$\rho_{\mathrm{JFET}} = \frac{1}{q\mu_n N_{\mathrm{DJ}}} \tag{3.17}$$

Increase the JFET region doping concentration (N_{DJ}) will reduce the resistance of the JFET region but the increase of charge in this region will degrade the breakdown voltage. Figure 3.15 shows the numerical simulation results on the breakdown voltage of shielded planar VD-MOSFET structure with different JFET region doping concentration. It is seen

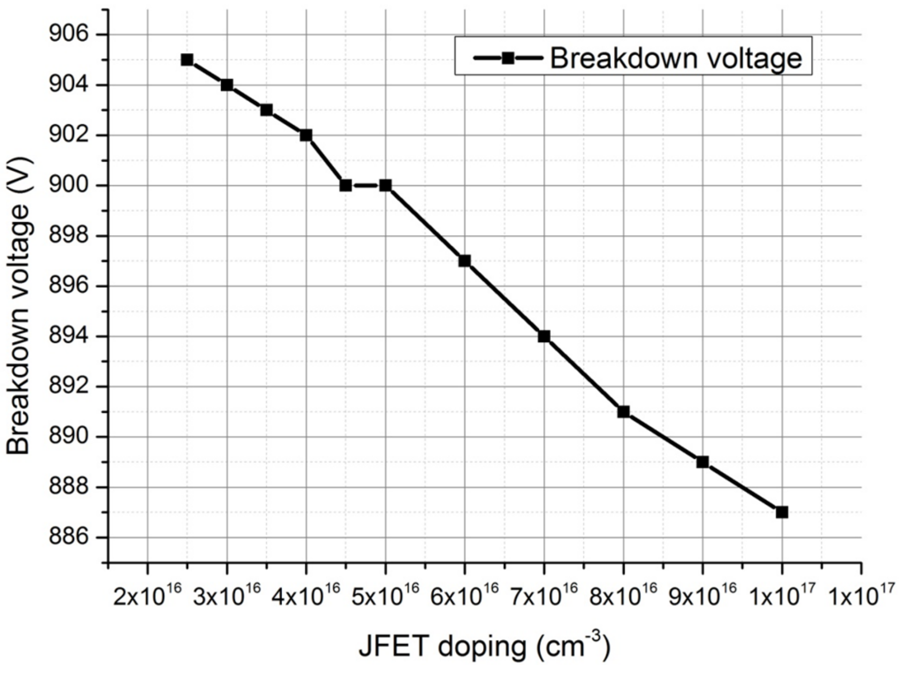


Figure 3.15: Breakdown voltage versus JFET doping concentration of 1 kV 4H-SiC shielded planar MOSFET.

that the breakdown voltage decreases linearly as the JFET region doping concentration increases. The breakdown voltage drop is about 20 V as the JFET doping concentration

increase from $2{\times}10^{16}$ cm^{-3} to $1{\times}10^{17}$ cm^{-3}. The JFET doping concentration in this case should be close to $2{\times}10^{16}$ cm^{-3} in order to achieve high breakdown voltage.

3.2 Novel Junction Termination Extension (JTE) Design

As discussed in Chapter 2, edge termination is an important aspect in the design of high voltage power semiconductor devices. As was shown in previous chapter, the Junction Termination Extension (JTE) is the most popular edge termination technique for high voltage 4H-SiC devices, because of its relatively low process complexity and high breakdown voltage that approaches the ideal parallel-plane value. In this section, the design and numerical simulation results of these termination structures are presented, including unterminated, single-zone, space modulated JTE (SMJTE) and the novel 2-step mesa JTE structures. It is important to note that unless stated otherwise, simulation were performed assuming zero surface charge.

For the ease of simulation and fabrication, the JTE design was initially carried out for a Schottky diode. The basic structure of an unterminated Schottky diode is illustrated in Figure 3.16. The doping concentration of the N- drift region is $2{\times}10^{16}$ cm^{-3} and thickness of 10 μm, with 500 nm thick of field oxide on the SiC next to the Schottky contact. The overall width of the structure is dependent on the width of the JTE region used. The one dimensional parallel plane breakdown voltage for the device is 1110 V, this value is

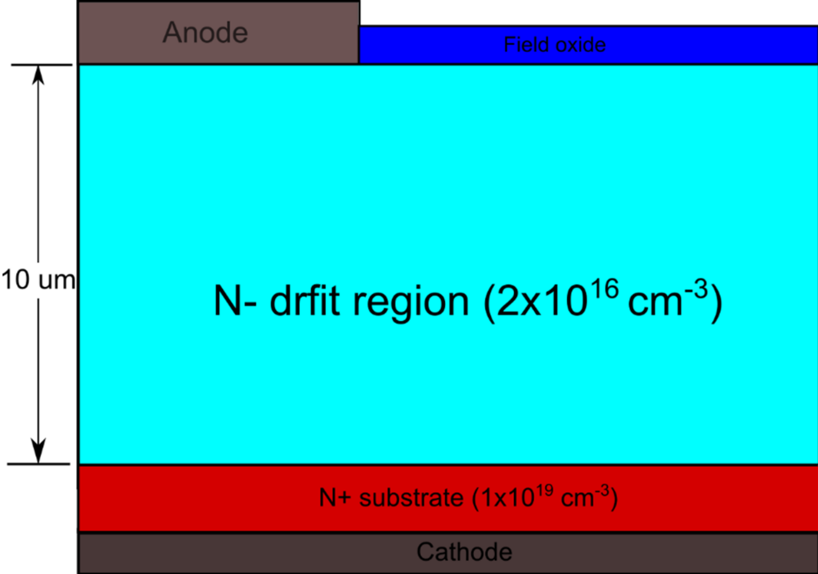


Figure 3.16: Structure of 1 kV Schottky diode used in reverse breakdown simulations.

subsequently used as a benchmark for the JTE designs that have been simulated.

The reverse breakdown voltage simulation was performed for the above unterminated Schottky diode structure. Figure 3.17 illustrates the electric field distribution for this device at avalanche breakdown. This breakdown occurred at a reverse bias of 456 V which is only about 41% of the ideal parallel plane breakdown voltage, and as expected, the breakdown occurs at the outer edge between the metal contact and silicon carbide epitaxial layer.

In order to improve the reverse breakdown voltage performance of the unterminated device structure, different junction termination extension (JTE) designs were simulated and compared. The most common termination is the single zone JTE structure [103,104], which is illustrated in Figure 3.18. A 0.8 μm deep box profile with a Gaussian tail has

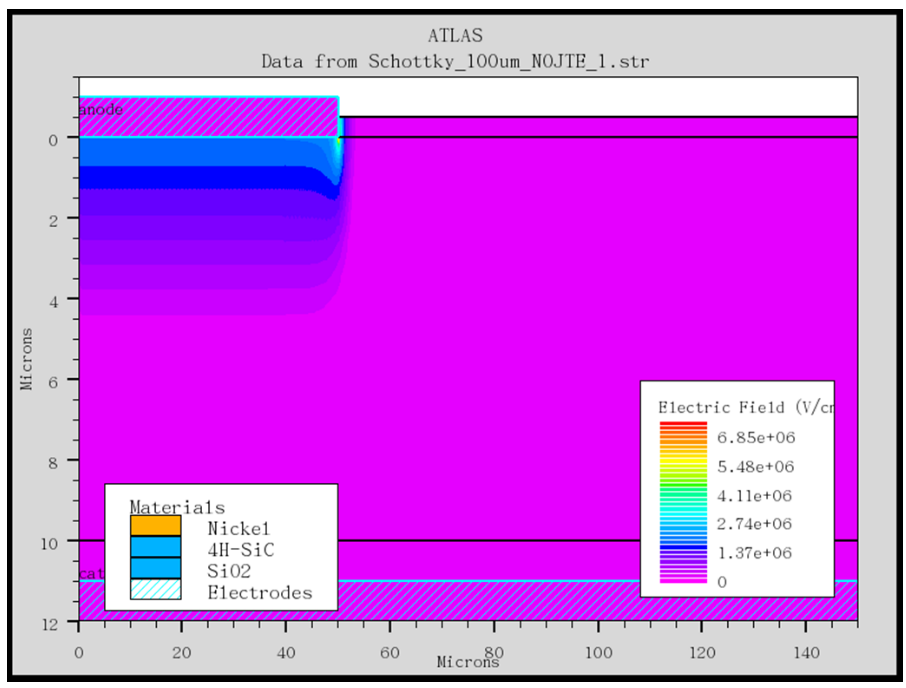


Figure 3.17: Electric field distribution at breakdown of unterminated 1 kV mesa-isolated Schottky diode.

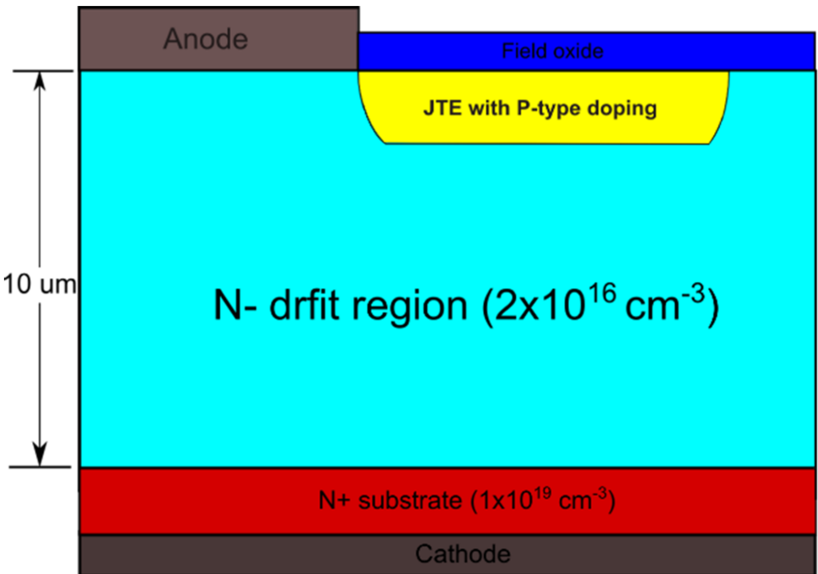


Figure 3.18: Schematic of Schottky diodes with single zone JTE structures.

been used to represent the implanted JTE region. The width of JTE region was fixed to 600 μm for all of the JTE structures in the simulation as those reported in literature [59], because the blocking capability of the conventional single zone JTE becomes saturated at a width of 500 μm. In the simulation, the JTE doping concentration $N_{\mathrm{A,JTE}}$ was varied to determine the optimum value for the device to achieve its peak breakdown voltage. The simulation result of the single zone JTE Schottky diode is shown in Figure 3.19. It

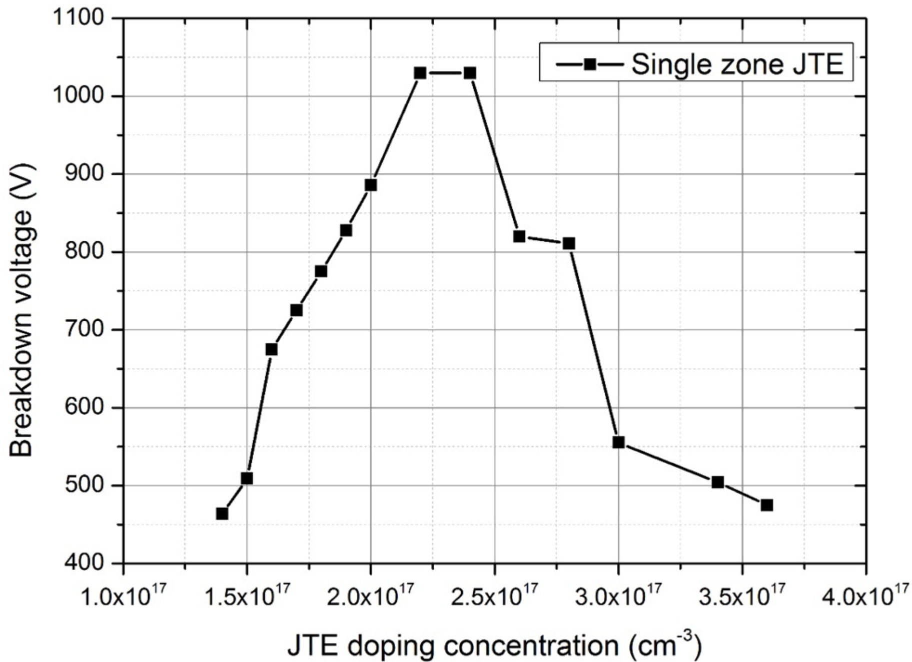


Figure 3.19: Breakdown voltage versus range of JTE doping concentration for 4H-SiC Schottky diode with single zone JTE structure.

is seen from the Figure 3.19 that the sensitivity of the peak breakdown voltage to the doping concentration of the JTE region is very high. The breakdown voltage decrease from its peak value of 1030 V at $N_{\mathrm{A,JTE}} = 2.2 \times 10^{17}$ cm^{-3} to 820 V at $N_{\mathrm{A,JTE}} = 2.6 \times 10^{17}$

cm^{-3}. This corresponds to a drop of about 20% in the peak breakdown voltage for an increase in JTE doping concentration of about 15%. And the peak breakdown voltage of 1030 V is about 92.7% of the ideal parallel plane breakdown voltage. From a practical fabrication point of view, this high sensitivity of the breakdown voltage to the JTE doping concentration is undesirable; therefore, different JTE structures that aim to reduce this sensitivity have been investigated.

3.2.1 Space Modulated JTE

The space-modulated junction termination extension (SMJTE) has been reported in many literatures [59,64–66] to be an effective termination in high voltage 4H-SiC power devices. Compare to other JTE methods for high voltage devices, the SMJTE has the advantage of being simple to fabricate, requiring only single mask patterning and single ion implantation. Therefore, the SMJTE is good for minimising the overall device processing complexity and cost.

The schematic of the SMJTE structure for Schottky diode is illustrated in Figure 3.20, and the dimensions of each JTE ring and spacing between them are outlined in Table 3.1. It is seen that the outer edge of the conventional JTE region is fragmented by employing spaces. The minimum spacing and the width of the ring are chosen to be 6 μm which is within the capability of the photolithography equipment in the cleanroom facility used to fabricate the devices. The width of one period (S_n + D_n) is kept at a constant of 20

Table 3.1: Dimensions of SMJTE design. Design parameters refer to those in Figure 3.20 (all dimensions in μm). The total JTE width is 600 μm, with the largest JTE region being 500 μm wide.

Design ref. of SMJTE	S1	S2	S3	S4	S5	D1	D2	D3	D4	D5
Width in μm	6	8	10	12	14	14	12	10	8	6

μm [59], and the total width of the termination was fixed at 600 μm with the largest JTE region being 500 μm wide.

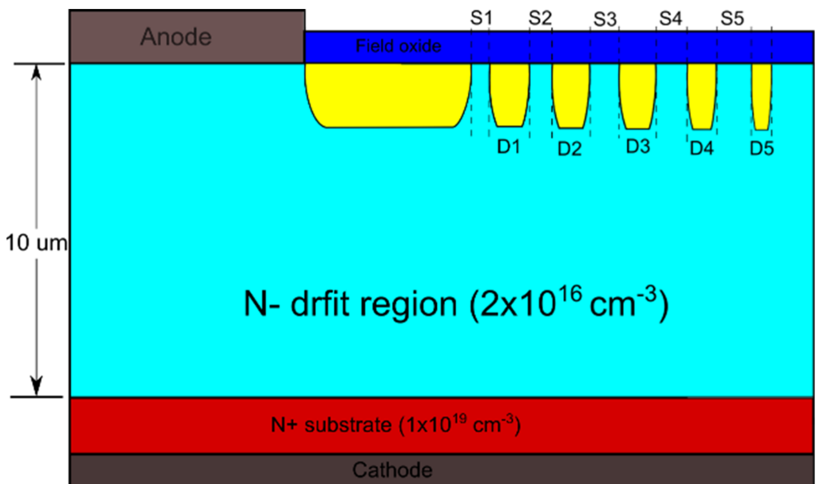


Figure 3.20: Schematic of Schottky diodes with SMJTE structures.

Figure 3.21 shows the simulated breakdown voltage characteristics as a function of doping concentration of the implanted JTE region. It can be seen that by using the SMJTE structure, the sensitivity of breakdown voltage to the doping concentration is reduced and the maximum breakdown voltage is increased, when compared to the simulated characteristic of the single zone JTE structure. For this SMJTE structure, the maximum breakdown voltage is 1100 V, which is about 99% of one-dimensional parallel-plane value. The breakdown voltage decrease from 1030 V at $N_{\mathrm{A,JTE}} = 2.2 \times 10^{17}\mathrm{cm}^{-3}$ to

965 V at $N_{\mathrm{A,JTE}} = 3 \times 10^{17}\mathrm{cm}^{-3}$. This corresponds to a drop of about 6.3% in the peak breakdown voltage for an increase in JTE doping concentration of about 26.7%, which gives significantly broader window for the optimum JTE doping concentration than single zone JTE. This low sensitivity of breakdown voltage to the JTE doping concentration is crucial for high voltage 4H-SiC devices, since in practice the implanted 4H-SiC requires high temperature annealing (>1600°C) to activate the dopants, and the activation rate is dependent on annealing temperature and time. The breakdown voltage will also be affected by the presence of charge near the SiO_2/4H-SiC interface.

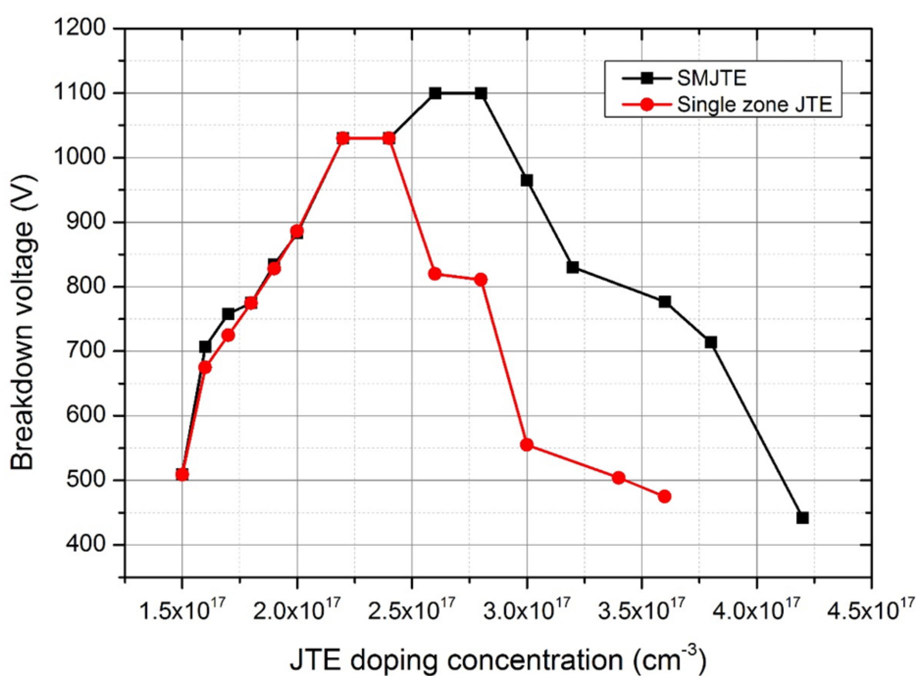


Figure 3.21: Comparison of breakdown voltage with various JTE doping concentration between SMJTE and Single zone JTE structures for 4H-SiC Schottky diode.

The measured fixed oxide charge of 4H-SiC MOS-based devices is much higher com-

pared to Si semiconductor technology, being of the order 10^{12} cm^{-2} [105]. Moreover, this surface charge will change depending on the passivation conditions, cleaning process and may also vary across the same wafer. The effect of surface charge (Q_S) on the breakdown voltage of the 4H-SiC Schottky diode with SMJTE structure has been investigated using numerical simulation. The breakdown voltage as a function of surface charge Q_S is plotted in Figure 3.22. It is seen that the presence of oxide charge causes a shift in the reverse

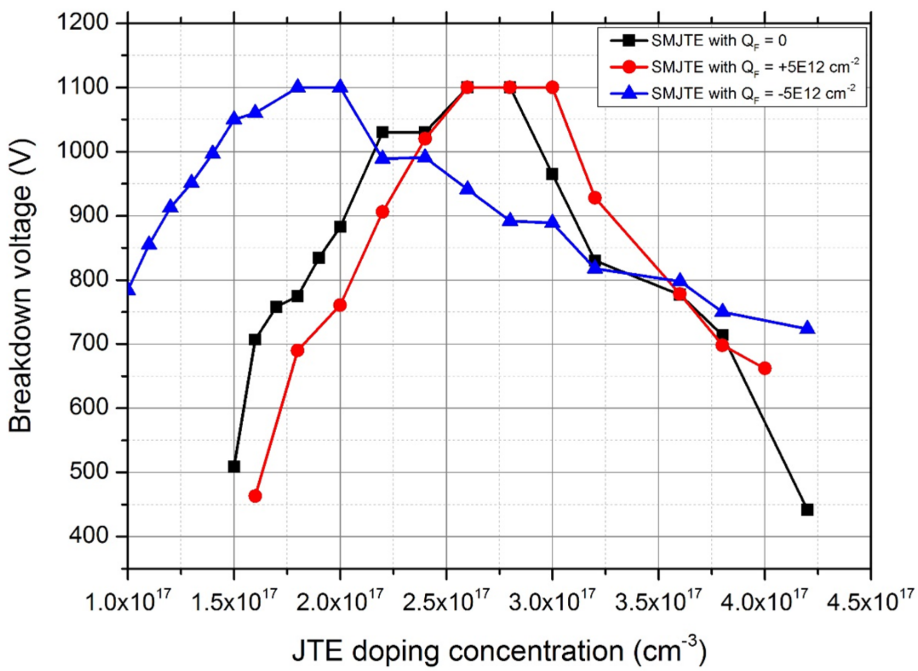


Figure 3.22: Effect of oxide charge on the breakdown voltage versus JTE doping concentrating of SMJTE structure for 4H-SiC Schottky diode.

breakdown voltage against JTE doping concentration profile; a positive charge will shift the breakdown voltage towards the heavier JTE dose and a negative charge will shift the peak breakdown voltage towards lighter JTE doping. In actual device fabrication,

the oxide layer grown on SiC have high interface traps density and a large number of fixed oxide charge. Depending on the oxidation and passivation conditions, these fixed oxide charge could be either positive or negative. From the experimental results as discussed in Chapter 7 and Chapter 8, it is seen that that the oxide grown on SiC without post-oxidation annealing has a large number negative oxide charge because of the positive shifting in the threshold voltage of VD- MOSFET. After the post-oxidation annealing in N_2O or phosphorus, the threshold voltage has reduced which means the negative fixed oxide charge/trapped charge have reduced.

The cause of this shift in the reverse breakdown voltage against JTE doping concentration in the Schottky diode due to the oxide charge can be explained using Figure 3.23. When a positive oxide charge exist, the negative charge of the ionised acceptors in the

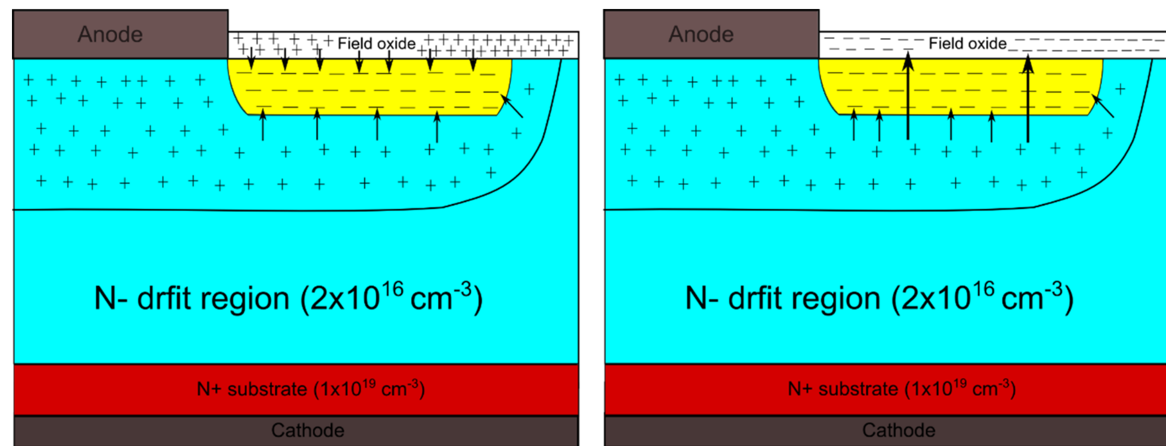


Figure 3.23: Schematic of JTE structure with positive (left) and negative (right) oxide charge under reverse bias conditions.

JTE region will be partially compensated, thus reducing the total concentration of nega-

tive charges in the JTE region for depletion which reducing the spreading of the electric field. As such, higher JTE doping concentration is required to achieve the maximum breakdown voltage. When a negative oxide charge exist, additional negative charge will be added to the negative charge of the ionised acceptor in the JTE region, increasing the total concentration which use for spreading of the electric field. Therefore, a low JTE doping concentration is required to achieve the maximum breakdown voltage.

3.2.2 Space Modulated Two Zones JTE

An improved version of the SMJTE structure for the high voltage 4H-SiC has also been investigated, which is called the space modulated two zones JTE (SM two zones JTE). The design of the SM two zones JTE was first reported in literature [64], which is for the 12-20 kV class 4H-SiC PiN diode. This SM two zone JTE structure was also proven to be effective on high voltage 4H-SiC Schottky diode and MOSFET [66, 67], which will be illustrated in this chapter. Figure 3.24 shows the schematic of the SM two zone JTE structure for Schottky diode, and the dimensions of each JTE and spacing between them are outlined in Table 3.2. It is seen that an extra fragmented JTE region with different doping concentration is added to the outer edge of the SMJTE structure. The width of over 10 μm was used for the spaces between JTE rings while keeping the period (e.g. S1+D2) 35 μm. The total width of the termination was fixed at 600 μm, and the ratio of the JTE doping concentration in JTE1 and JTE2 for SM two zone JTE was fixed to 3:2.

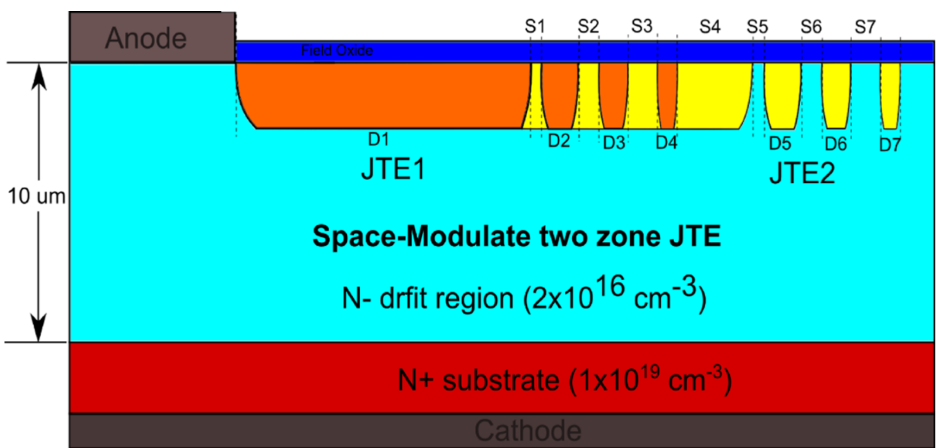


Figure 3.24: Schematic of Schottky diodes with SM two zones JTE structures.

Table 3.2: Dimensions of SM two zone JTE design. Design parameters refer to those in Figure 3.24, where dimensions of S4 to S7 and D5 to D7 are equal to S1 to S3 and D2 to D4 (all dimensions in μm).

Design ref. of JTEs	S1	S2	S3	S4	D1	D2	D3	D4
Width in μm	10.5	17.5	24.5	78	312	24.5	17.5	10.5

The optimum JTEs doping concentrations in this case are $2.5 \times 10^{17}\text{cm}^{-3}$ for the JTE1 region (orange colour shown in Figure 3.24) and $1.67 \times 10^{17}\text{cm}^{-3}$ for the JTE2 (yellow colour shown in Figure 3.24).

Figure 3.25 shows the simulated breakdown voltage characteristics as a function of doping concentration of the implanted JTE region, for different JTE structures. It can be seen that the SM two-zone JTE structure provides the widest optimum JTE doping window. Maximum breakdown voltage of 1070 V was obtained in the SM two-zone JTE, which is about 97% of the ideal one dimensional parallel plane breakdown voltage (1110 V). At the JTE doping concentration of 1.5×10^{17} cm^{-3}, both single zone JTE and SMJTE have breakdown voltage of only about 500 V, however, for the SM two-zone JTE

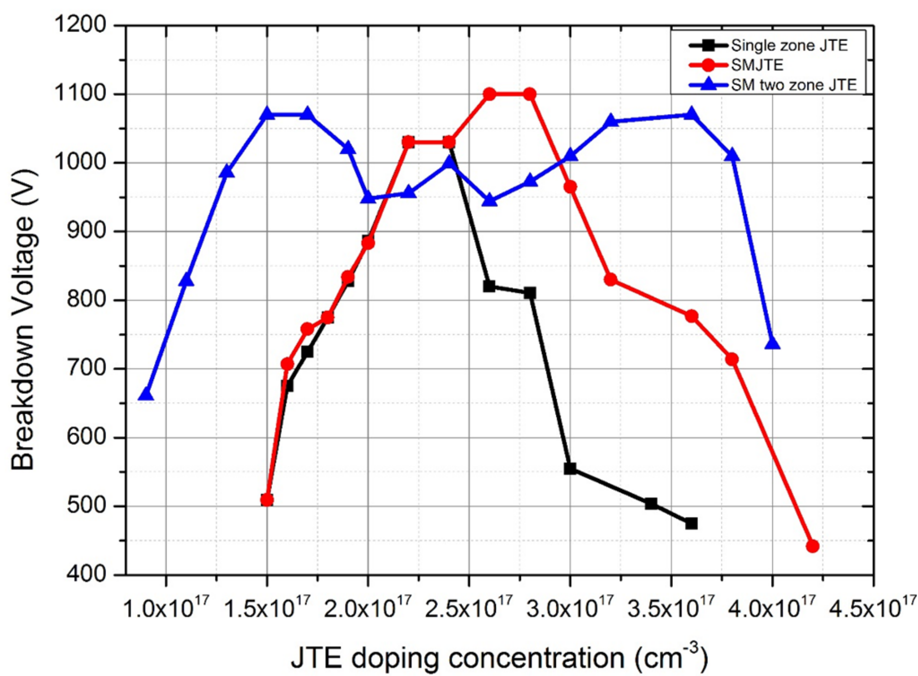


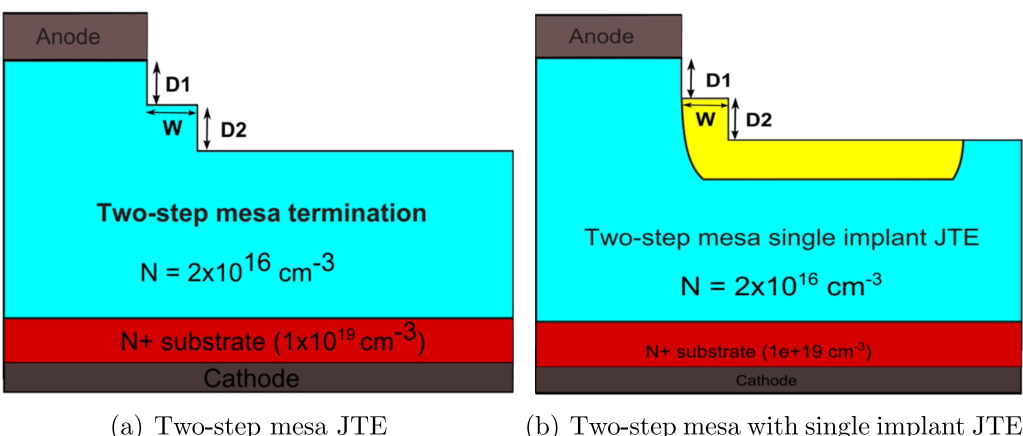
Figure 3.25: Breakdown voltage versus JTE doping concentration for 4H-SiC Schottky diode with single zone JTE, SMJTE and SM two zone JTE structures.

structure breakdown voltage of 1070 V is achieved for the same doping concentration. High breakdown voltage (±11% of peak breakdown voltage) is maintained from the JTE doping concentration of 1×10^{17} cm^{-3} to 3.6×10^{17} cm^{-3}, which is about three time wider than the SMJTEs optimum doping window. The drawback of the SM two-zone JTE is that it requires two separate implantations and thus increases the overall processing cost of the device.

3.2.3 Two-Steps MESA JTE

A novel two-step mesa JTE structure which recently published in [66] by the author shows that with an additional P-type guard ring and a mesa step, the breakdown voltage could

achieve same as the one dimensional parallel plane breakdown voltage. The single-step JTE is a common termination which has been studied in SiC bipolar junction transistors [106] and SiC PiN diodes [107]. However, the single-step mesa JTE suffers from high sensitivity to etching depth and normally requires ion implantation to alleviate electric field crowding at the corners. Using multistep JTE reduces this sensitivity, as demonstrated in many reports [11, 58, 108]. The ability of the mesa termination in reducing electric field crowding are thought to have strong dependence on etching depths. The effect of different etching depths of the two-step mesa JTE on the breakdown voltage will be discussed in this section. Figure 3.26 shows the schematic of the two-step mesa JTE and the two-step mesa JTE with P-ring implantation structures for Schottky diode. The width and depth of ion implanted JTE is 600 μm and 0.8 μm which is the same as the other JTE design discussed previously.



(a) Two-step mesa JTE (b) Two-step mesa with single implant JTE

Figure 3.26: Schematic of (a) two-step mesa JTE and (b) two-step mesa with single implant JTE.

Figure 3.27 shows the simulated breakdown voltage of the Schottky diode with two-step mesa JTE as a function of the etching depth D1 for different etching depth of D2; It can be seen from Figure 3.27 that the depth of D1 has more influence on breakdown voltage than the depth of D2 for the 2-step mesa JTE. Also the deeper D1 is etched, the higher the breakdown voltage. The maximum breakdown voltage it could achieve is almost the same as the parallel plane breakdown voltage when D1 is equal to and more than 6 μm. Figure 3.28 shows their breakdown voltage of the two-step mesa JTE structure with difference in D1 depth while keeping D2 and W the same.

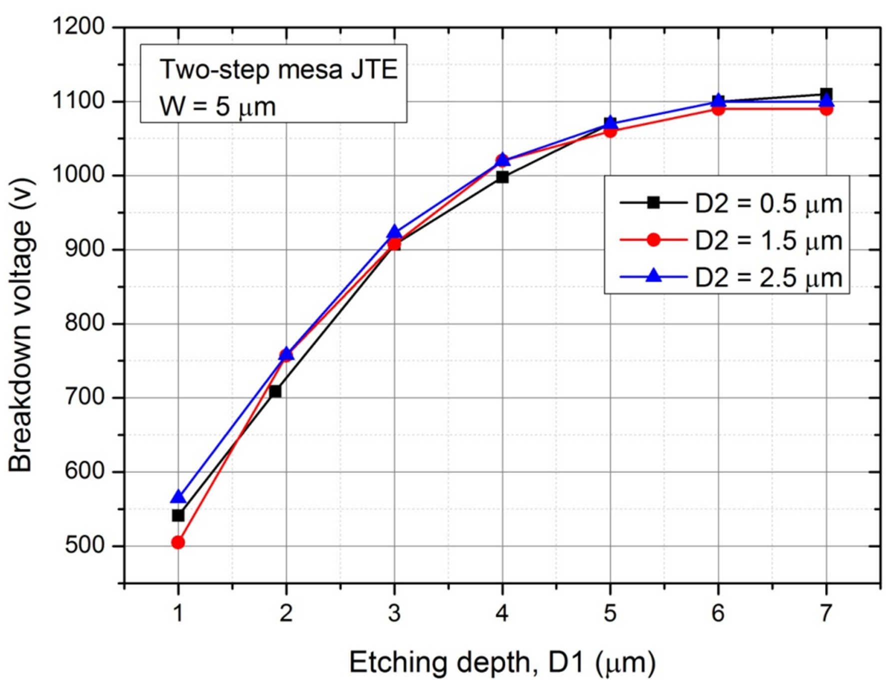
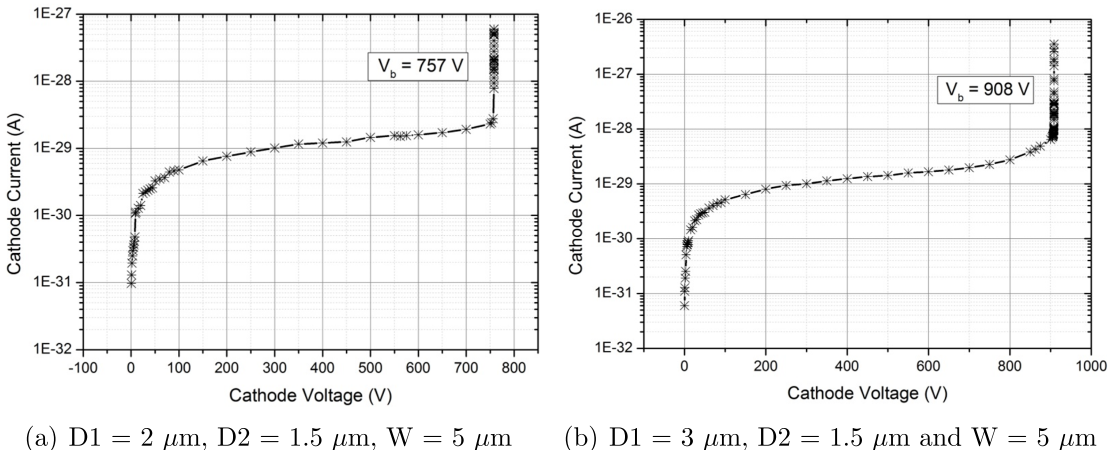


Figure 3.27: Simulated breakdown voltages as a function of etching depth D1 with various of D2 for two-step mesa JTE.

From Figure 3.27 it is seen that the breakdown voltage increases as etching depth



(a) D1 = 2 μm, D2 = 1.5 μm, W = 5 μm (b) D1 = 3 μm, D2 = 1.5 μm and W = 5 μm

Figure 3.28: Schematic of (a) two-step mesa JTE and (b) two-step mesa with single implant JTE.

D1 increases, it will reach its maximum value and saturate at around 1100 V when D1 = 6 μm. The impact of etching depth of D2 on breakdown voltage is almost negligible compare with D1.

The two-step mesa JTE with an additional P-ring implantation was also investigated as shown in Figure 3.26(b). The peak breakdown voltage obtained was 1110 V at JTE doping of around 2×10^{17} cm^{-3}, which is the same as the ideal parallel plane breakdown voltage. Breakdown voltage versus JTE doping concentration for various of JTE structures is shown in Figure 3.29. It is seen that the maximum breakdown voltage of 1100 V was obtained in the two-step mesa JTE with P-ring single zone implantation, which is about 99% of the ideal one dimensional parallel plane breakdown voltage. It also provides the widest optimum doping window compare with other JTE structures. This reduces the sensitivity of the breakdown voltage with respect to the doping concentration of the P-

implant, making this an attractive solution for SiC Schottky diode design. However, because of the more complicated fabrication process and higher cost involved, this two-step mesa design did not implement in our high voltage devices, instead the much simpler SMJTE structure was used.

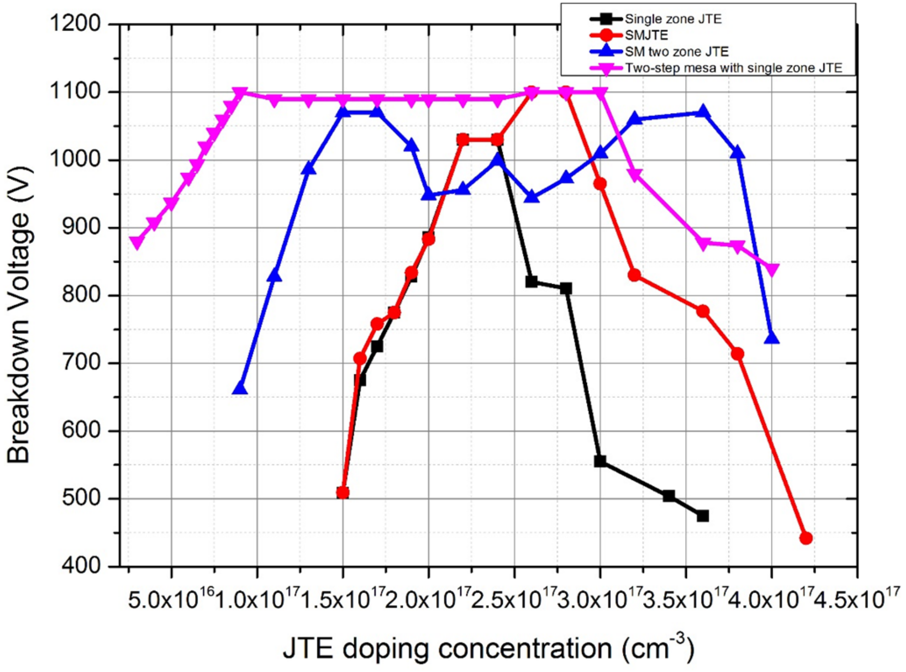


Figure 3.29: Breakdown voltage versus JTE doping concentration of Schottky diode with various of JTE structures.

3.3 Numerical Simulation of Shielded Planar VD-MOSFETs

In this Section, the numerical simulation on shielded planar VD-MOSFET structures are carried out to look at the on-state and reverse breakdown characteristics. The on-state characteristics was used as a benchmark to compare with the results of fabricated shielded planar VD-MOSFET using retrograde P-body doping profile as discussed in Chapter 8. The analytical model is also used to predict the specific on-resistance for the structure. Although the space-modulated junction termination (SMJTE) structure did not include in the final VD-MOSFET fabrication due to the implantation cost and time, the simulation and mask design of the SMJTE for the VD-MOSFETs structure were carried out.

3.3.1 1 kV Inversion-Mode MOSFET

The two-dimensional numerical simulations on the 1 kV shielded 4H-SiC inversion-mode power MOSFET structure is described here. The numerical simulation is done on the half-cell structure as illustrated in Figure 3.30. The P+ shielding region extended from a depth of 0.2 to 0.4 μm with a doping concentration of 3×10^{18} cm^{-3}. The P-base and N+ source regions were formed within the 0.2 μm of the N-drift region located above the P+ shielding region. The doping concentrations of P-base, N+ source and P+ regions are illustrated in Figure 3.30. The JFET region dimension is chosen to be 2 μm in order to have a low on-resistance and acceptable breakdown voltage of the shielded planar

VD-MSOFET structure as discussed in Section 3.1.

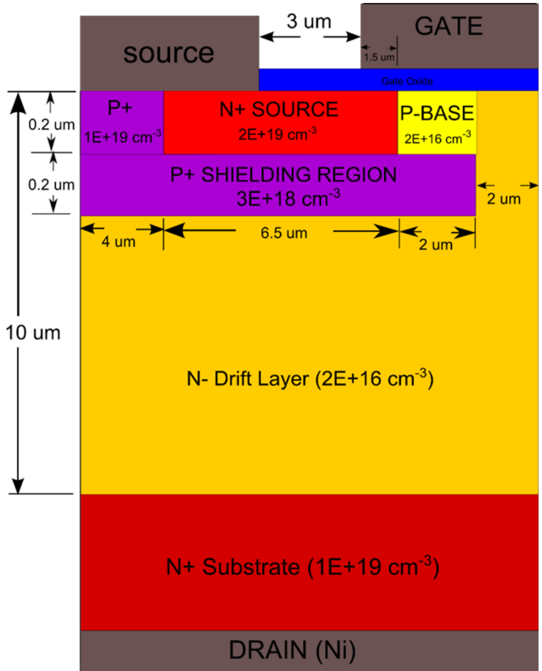


Figure 3.30: 1 kV shielded planar inversion-mode power MOSFET structure.

3.3.1.1 On-State Characteristics

The transfer characteristics for the 1 kV shielded planar VD-MOSFET structure with a drain bias of 0.1 V were obtained using numerical simulations. The resulting transfer characteristics is shown in Figure 3.31. It is seen that a threshold voltage of about 9.5 V is extracted at 300 K. This value is very close to actual result of fabricated MOSFETs without doing any gate oxide passivation treatment as discussed in Chapter 8. Depending on the passivation conditions, the threshold voltage could be varied between -5 to 10 V.

The output characteristics for the 1 kV shielded 4H-SiC planar inversion-mode power

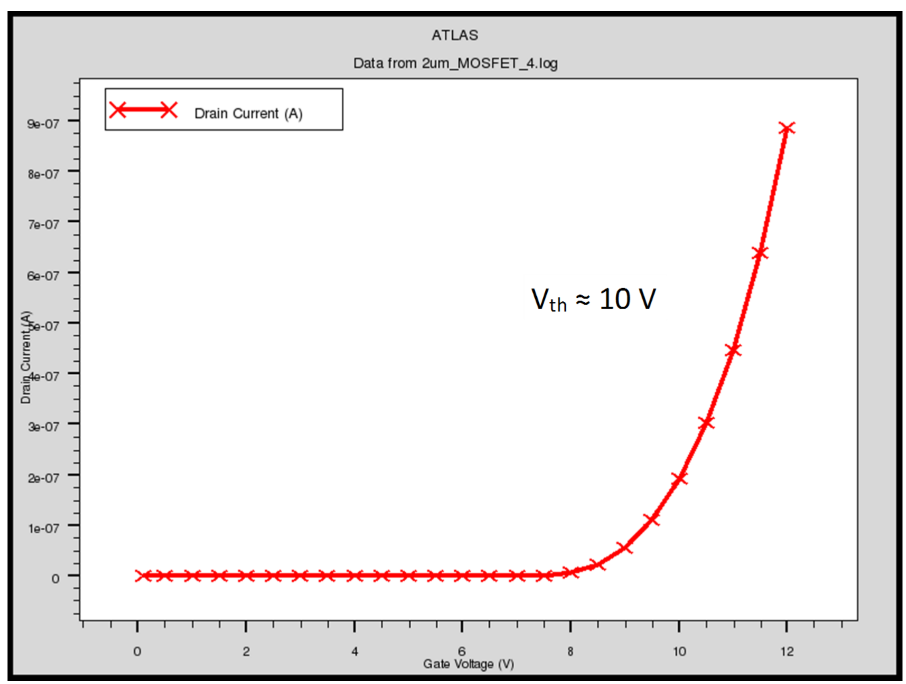


Figure 3.31: Transfer characteristic of 1 kV shielded planar VD-MOSFET.

MOSFET structure at different gate voltage (0, 5, 10, 15 and 20 V) are shown in Figure 3.32. It is seen that there is no current flow between the source and the drain of the MOSFET unless the gate bias is 15 V or above because of the near 10 V threshold voltage. Typically the threshold voltage is between 2 to 5 V for gate drive circuit of 10 to 15 V. Threshold voltage could be reduced by either reducing the oxide thickness or the doping concentration of the channel region as discussed previously in Chapter 2. Gate oxide passivation using N_2O or phosphorus will also have effect on shifting the threshold voltage as observed by the author and in literature [31]. The total specific on-resistance obtained from the numerical simulations for the 1 kV shielded planar VD-MOSFET structure is 23 $m\Omega \cdot cm^2$ at a gate bias of 20 V. This value is comparable to the

ideal specific on-resistance of 12 $m\Omega \cdot cm^2$ for the same VD-MOSFET structure by adding up the channel, accumulation, JFET and drift region resistances. The drain current increases as the gate voltage increases indicate that the channel resistance is dominant in the 1 kV shielded planar inversion-mode MOSFET structure. The theoretical calculation of the specific on-state resistance of the shield planar VD-MOSFET structures indicates that the channel resistance is about 83% of the total on-resistance of the structure as shown in Figure 3.9.

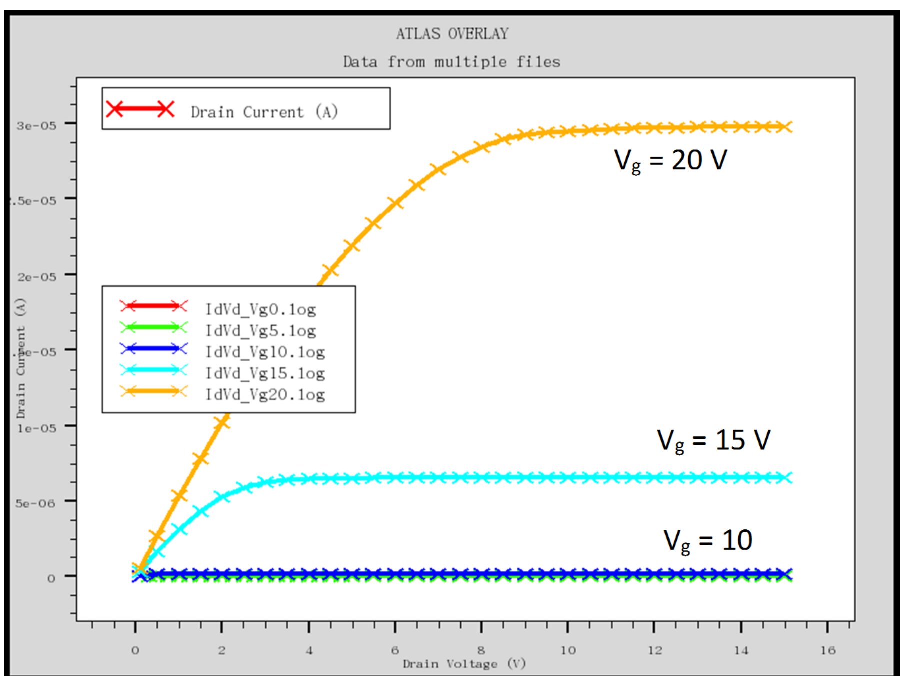


Figure 3.32: Output characteristic of 1 kV shielded 4H-SiC planar VD-MOSFET.

3.3.1.2 Blocking Characteristics

The blocking voltage capability for the shielded planar VD-MOSFET structure is determined by the doping concentration and thickness of the drift region as showed in equation 3.13, given that the JFET region is sufficiently small to prevent the rupture of the gate oxide. As discussed before in Section 3.1.1, a breakdown voltage of 1 kV can be obtained by using a doping concentration of 2×10^{16} cm^{-3} with drift region thickness of 10 μm. This combination of drift region doping concentration and thickness will be used in the simulation modelling of the 1 kV shielded inversion-mode power MOSFET structure.

The doping profile taken along the surface of the 1 kV shielded planar VD-MOSFET structure is shown in Figure 3.33. It is seen that the channel extends from 10.5 μm to 12.5 μm creating a channel length of 2 μm in the P-base region. The doping concentration of the JFET region is 2×10^{16} cm^{-3} and the P-base region is 3×10^{16} cm^{-3}. The N+ source region and P+ contact region are heavily doped with doping concentrations of 1×10^{20} cm^{-3} and 1×10^{19} cm^{-3} in order to form a good ohmic contact. The blocking characteristics for the 1 kV shielded planar 4H-SiC VD-MOSFET were obtained by increasing the drain voltage while keeping the gate bias zero. No substantial leakage current was observed in the device due the very small intrinsic concentration in 4H-SiC. This also confirmed that the reach through of the P-base region has been suppressed by the P+ shielding region. The potential contours in the 1 kV shielded planar VD-MOSFET structure at its breakdown is shown in Figure 3.34 for the upper part of the device structure. It

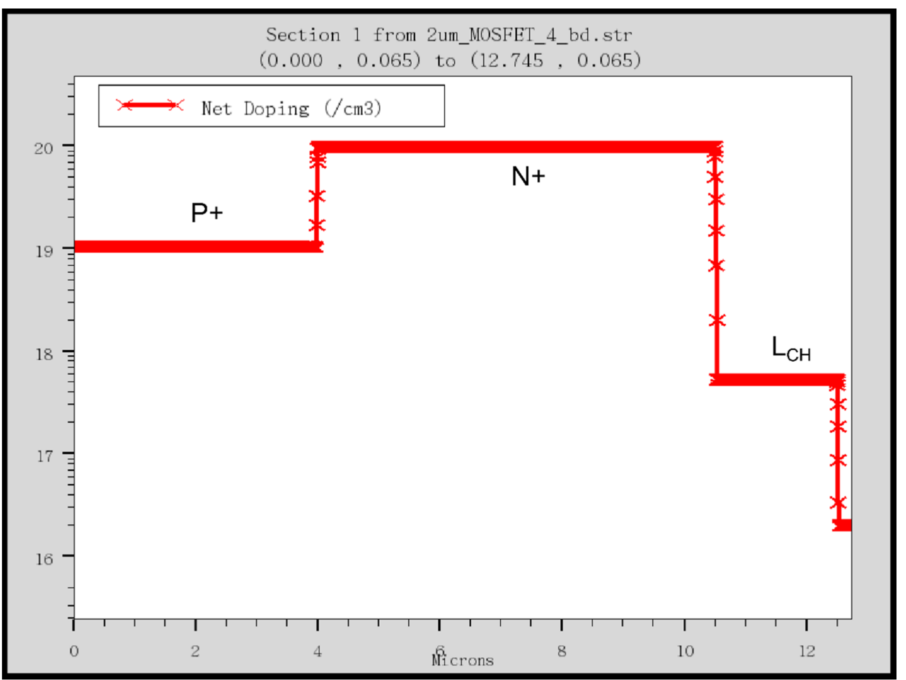


Figure 3.33: Lateral doping profile for the 1 kV shielded planar VD-MOSFET.

can be observed that the drain voltage is supported below the P+ shielding region as the potential contours do not extend into the P-base region but shielded by the P+ shielding region. The potential contours extend into the JFET region just under the gate oxide, this means that under high drain voltage the electric field will be higher in this region. This JFET region and especially its nearby gate oxide are the regions where most likely to breakdown first under high drain voltage. This problem could be improved by increasing the depth of the P+ shielding region under the P-base region, so that the potential contours could be further pushed down towards the drain region and away from the gate oxide region. However, this means higher implant energies are required to reach deeper from the surface and increase the surface roughness of the wafer.

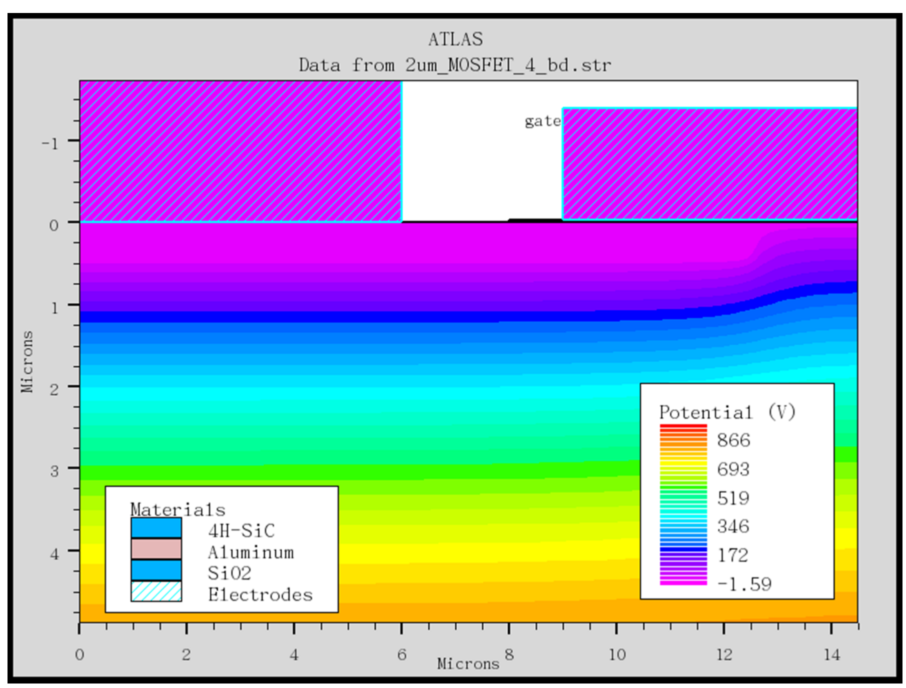


Figure 3.34: Potential contours profile for the 1 kV shielded planar VD-MOSFET.

The electric field distribution in the 1 kV shielded planar VD-MOSFET structure is also shown in Figure 3.35. It can be seen that the electric field in the JFET region, and most importantly at the surface under the gate oxide has been greatly reduced by the presence of the P+ shielding region. These results clearly demonstrate the importance of the using the shielded region concept to achieve practical device structure in silicon carbide.

The electric field distribution through the middle of the JFET region of the 1 kV shielded planar VD-MOSFET structure is shown in Figure 3.36 at its breakdown. It can be observed that the maximum electric field occurs at the depth of about 1 μm from the surface. The P+ shielding region reduces the electric field at the surface under the gate

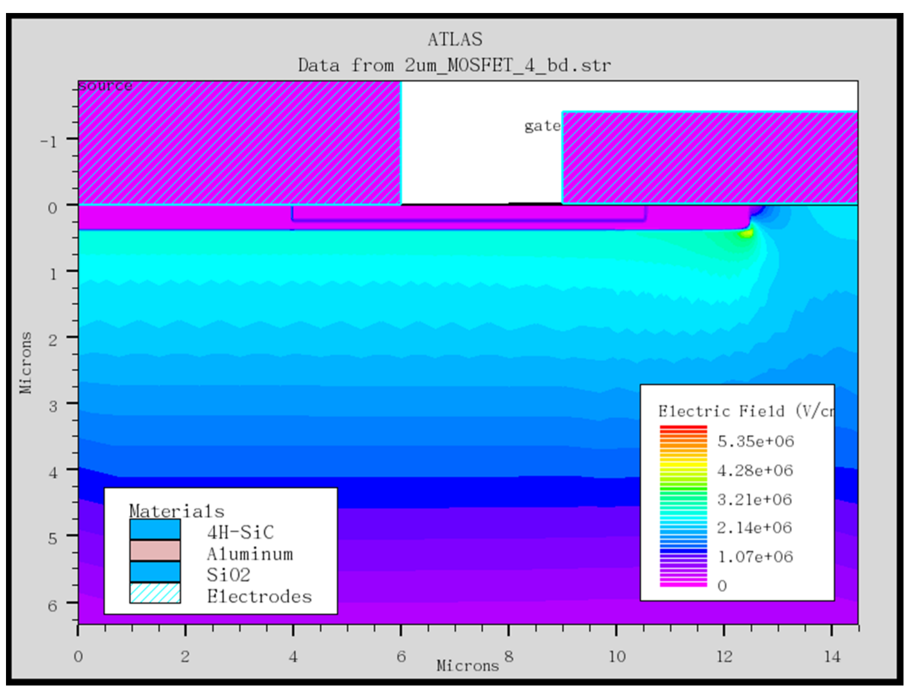


Figure 3.35: Breakdown electric field distribution for the 1 kV shielded planar VD-MOSFET.

oxide to 1.6×10^6 V/cm which is about 1.8 times smaller than the electric field in the drift region blow the P+ shielding region. Therefore, the electric field in the gate oxide is reduced to about 4×10^6 V/cm when the device is breakdown at a drain bias of 921 V as shown in Figure 3.37. The reduced electric field in the gate oxide prevents it from early breakdown and allows stable device performance over long periods of time. Further reduction of electric field in the gate oxide and the JFET region under the gate oxide can be achieved by reducing the width of the JFET region and increase the depth of the P+ shielding region.

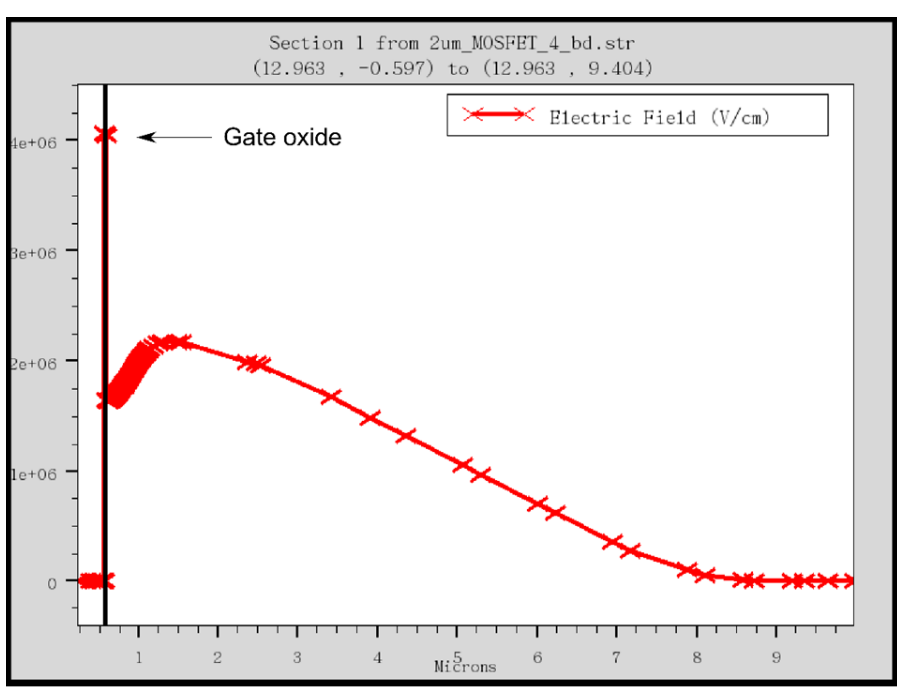


Figure 3.36: Electric field distribution for the 1 kV shielded planar VD-MOSFET through the JFET region.

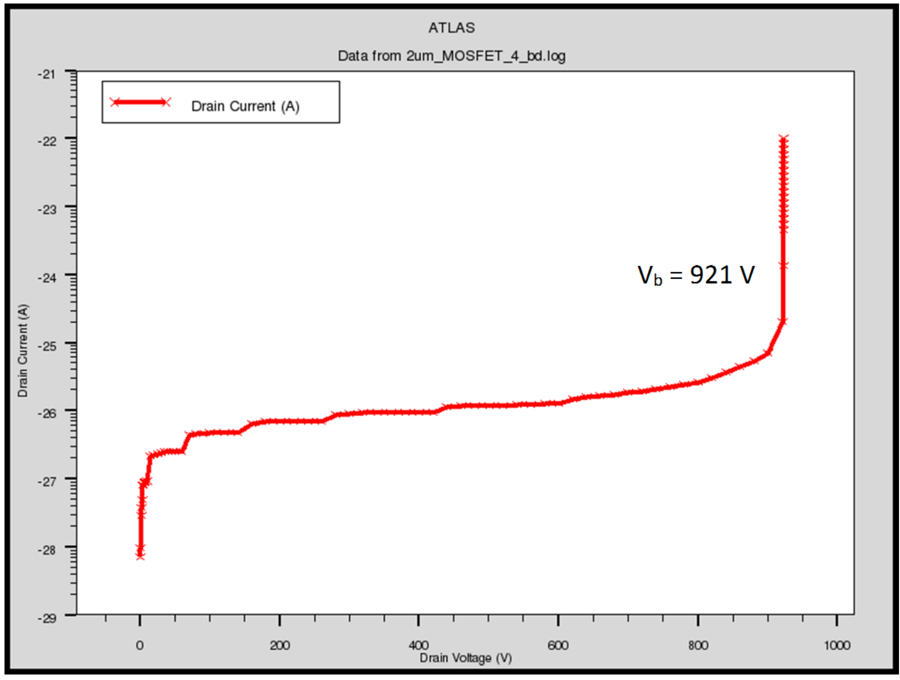


Figure 3.37: Breakdown characteristic of 1 kV shielded planar VD-MOSFET.

3.3.1.3 Shielded Planar VD-MOSFET with SMJTE structure

The space-modulated junction termination extension (SMJTE) structure were used on the design of the shielded planar VD-MOSFET due to its ease of design and fabricate and provide much wider optimum doping widow than the conventional single zone JTE structure. The dimensions of the basic SMJTE structure for simulation are outlined in Section 3.2.2 which was designed for high voltage devices (>10kV). The one-dimensional parallel plane breakdown voltage of the 1 kV shielded planar VD-MOSFET structure is 921 V as illustrated in Figure 3.37, and the simulated breakdown voltage of the two-dimensional shielded planar VD-MOSFET structure without edge termination was found to be 220 V.

Figure 3.38 shows the 1 kV shielded planar VD-MOSFET structure with the SMJTE structure at the last cell. The simulation results of the breakdown voltage versus JTE doping concentrations is shown in Figure 3.39. It is seen that with the SMJTE structure the shielded planar VD-MOSFET increases the breakdown voltage to 920 V with the JTE doping concentration of 3.2×10^{17} cm^{-3} which is the optimum doping concentration for the SMJTE structure.

3.3.2 3.3 kV Inversion-Mode MOSFET

As with the 1 kV shielded planar VD-MOSFET, the two-dimensional numerical simulations on the 3.3 kV shielded 4H-SiC inversion-mode power MOSFET structure is described

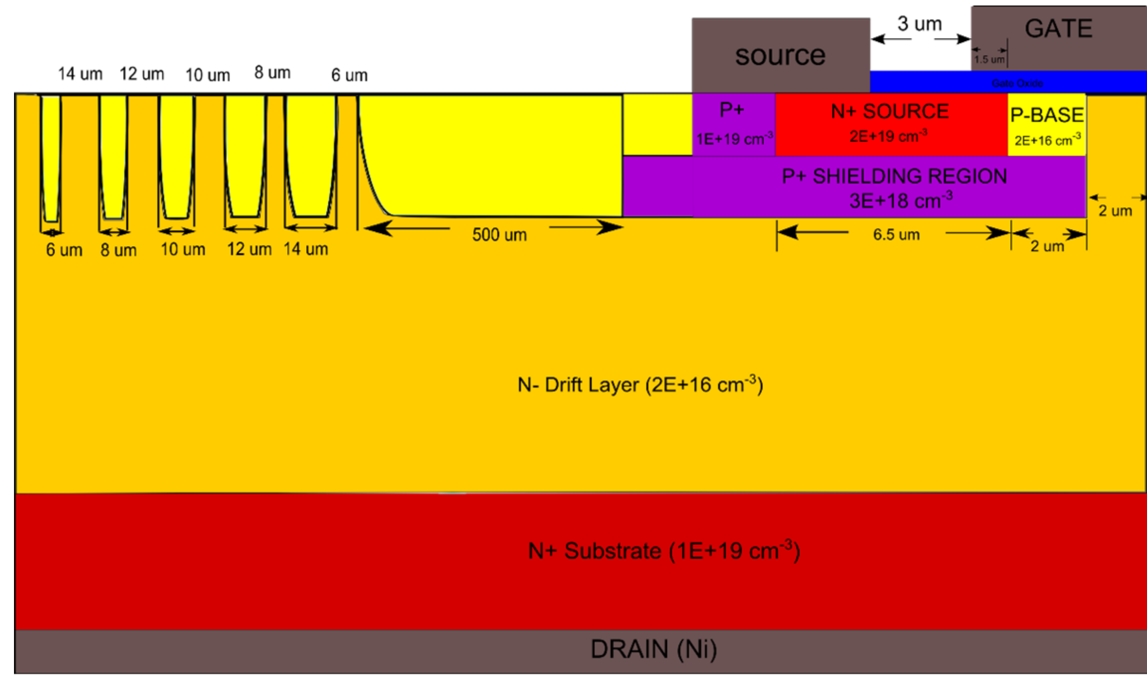


Figure 3.38: Schematic of 1 kV shielded VD-MOSFET with SMJTE structure.

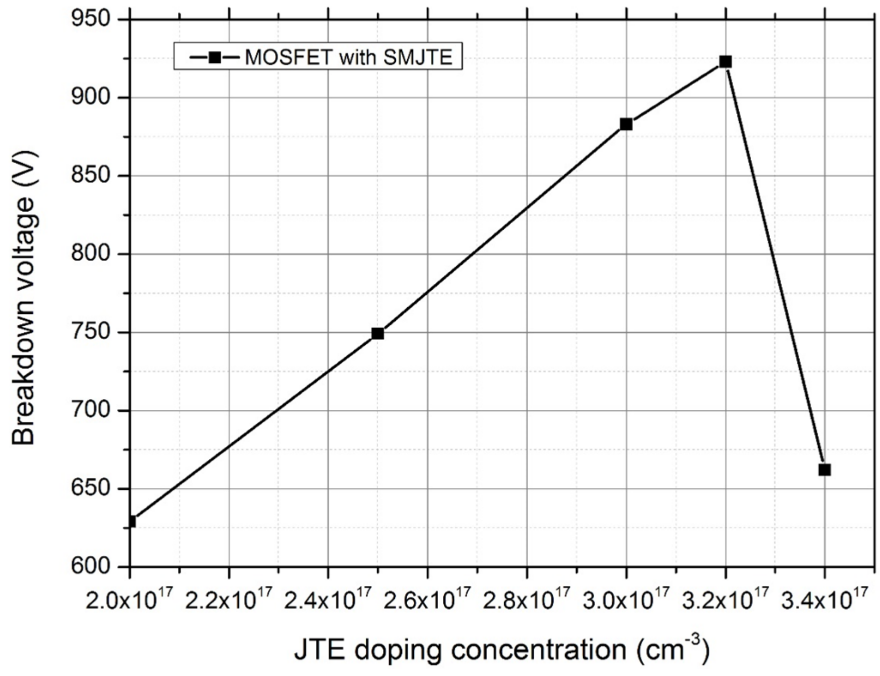


Figure 3.39: The simulated breakdown voltage versus SMJTE doping concentration for the 1kV shielded VD-MOSFET.

here. The numerical simulation is done on the half-cell structure as illustrated in Figure 3.40. The 3.3 kV shielded planar VD-MOSFET design is similar to the 1 kV VD-MOSFET design except that the drift region thickness and doping concentration are different. Based on the drift layer design equations as discussed in Section 3.1.1, to achieve a 3.3 kV device the drift region thickness needs to be approximately 30 μm and the doping concentration of $4{\times}10^{15}$ cm^{-3}.

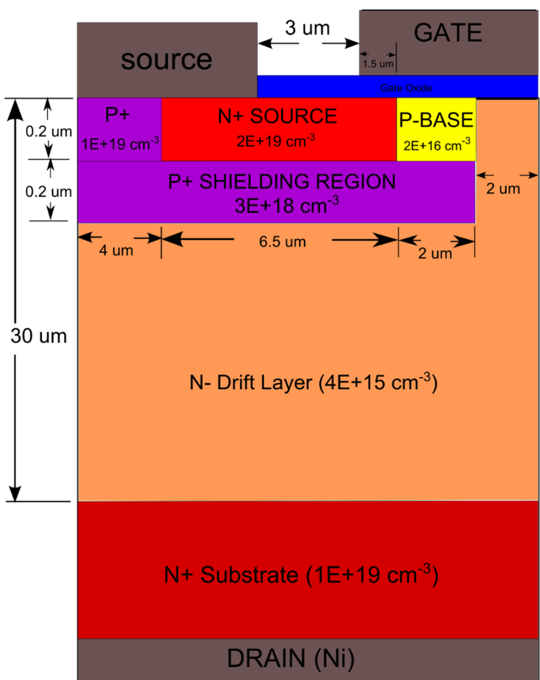


Figure 3.40: Schematic of 3.3 kV shielded planar inversion-mode power MOSFET.

3.3.2.1 On-State Characteristics

The transfer characteristics for the 3.3 kV shielded planar VD-MOSFET structure were again obtained using numerical simulations with a drain bias of 0.1 V. The resulting

transfer characteristics is shown in Figure 3.41. It is seen seem that a threshold voltage of about 9.5 V is extracted at 300 K. This value is similar to the actual result of fabricated MOSFETs without passivation on the gate oxide.

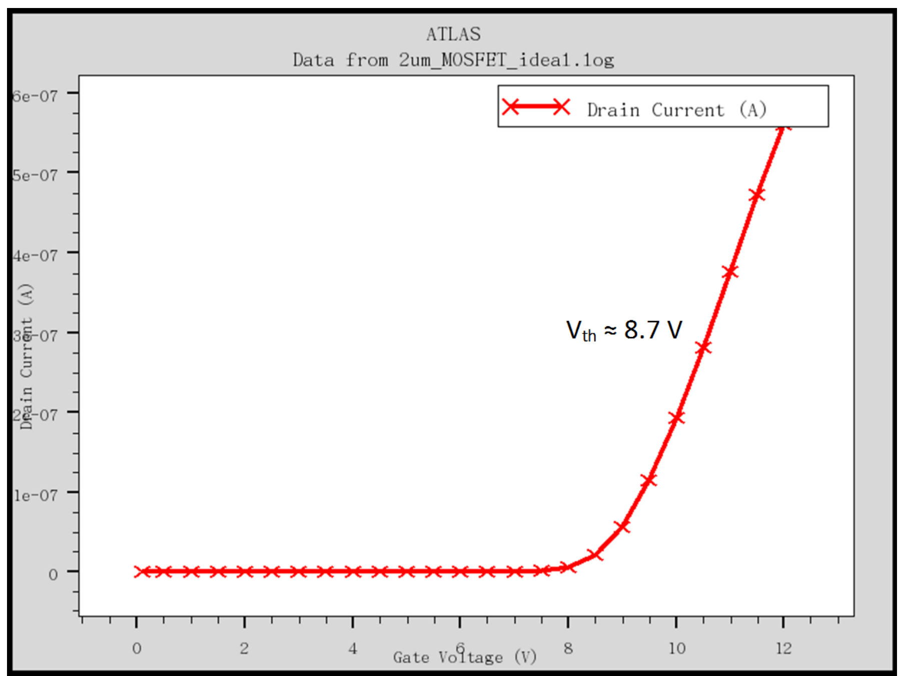


Figure 3.41: Transfer characteristic of 3.3 kV shielded planar VD-MOSFET.

The output characteristics for the 3.3 kV shielded planar VD-MOSFET structure at different gate voltage (0, 5, 10, 15 and 20 V) are shown in Figure 3.42. It is seen that there is no current flow between the source and the drain of the MOSFET unless the gate bias is 15 V or above because of the near 9 V threshold voltage. The total specific on-resistance obtained from the numerical simulations for the 3.3 kV shielded planar VD-MOSFET structure is 158 $m\Omega \cdot cm^2$ at a gate bias of 20 V and drain voltage of 1 V, which is greater than the ideal specific on-resistance of 20 $m\Omega \cdot cm^2$ for the same VD-MOSFET

structure by adding up the channel, accumulation, JFET and drift region resistances. This difference in total specific on-resistance is due to the low channel mobility of the 4H-SiC MOSFETs which is directly related to the high interface trap density between the SiO_2 and 4H-SiC layer. As discussed in Chapter 7, the field effect mobility of 4H-SiC lateral MOSFET without any post oxidation annealing treatment is about 1.2 cm2/V.s, which is only about 1% of the bulk mobility. The low channel mobility results in much higher channel resistance, which lead to increase of total on-resistance.

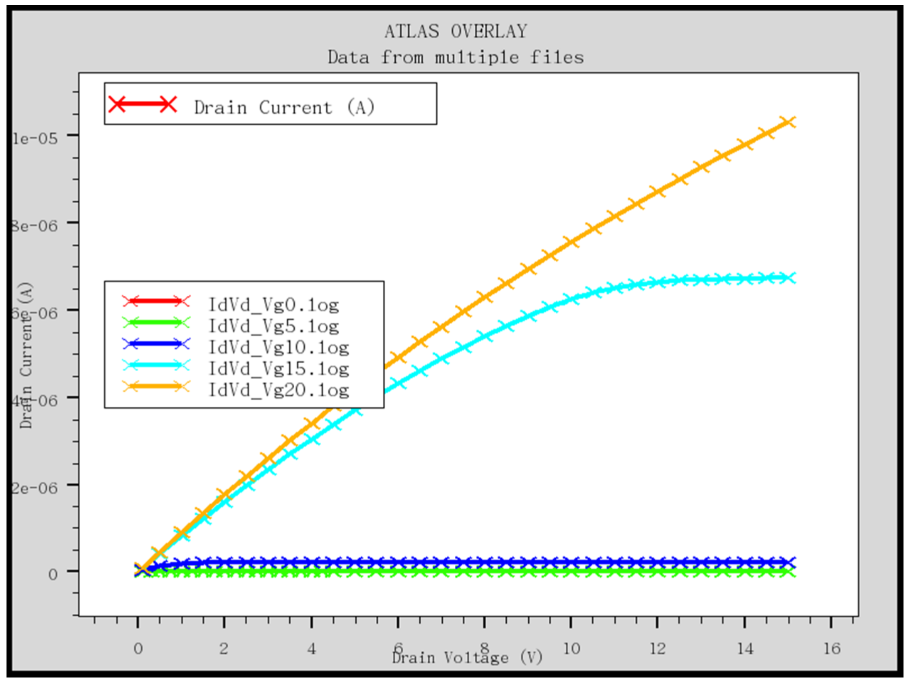


Figure 3.42: Output characteristic of 3.3 kV shielded planar VD-MOSFET.

The theoretical calculation of the specific on-state resistance of the shield planar VD-MOSFET structures indicates that the channel resistance is about 47.4% of the total on-resistance of the structure, and drift region resistance start playing important role in the

overall on-resistance of the device which contribute about 47% of the total on-resistance.

3.3.2.2 Blocking Characteristics

As discussed before in Section 3.1.1, a breakdown voltage of 3.3 kV can be obtained by using a doping concentration of 4×10^{15} cm^{-3} with drift region thickness of 30 μm. This combination of drift region doping concentration and thickness will be used in the simulation modelling of the 3.3 kV shielded inversion-mode power MOSFET structure.

The blocking characteristics for the 3.3 kV shielded planar VD-MOSFET were obtained by increasing the drain voltage while keeping the gate bias zero. The breakdown electric field distribution of the 3.3 kV shielded planar VD-MOSFET structure is shown in Figure 3.43. It can be seen that the electric field at the surface under the gate oxide has been greatly reduced by the presence of the P+ shielding region which is the same as in the 1 kV shielded planar VD-MOSFET structure case. The breakdown voltage of the 3.3 shielded planar VD-MOSFET structure is about 4130 V as shown in Figure 3.44, which is about 18% higher than the value estimated using the equations 3.13 and 3.14 as shown in Section 3.1.1.

3.3.2.3 Shielded Planar VD-MOSFET with SMJTE structure

The space-modulated junction termination extension (SMJTE) structure were used on the design of the 3.3 kV shielded planar VD-MOSFET. The dimensions of the basic SMJTE structure for simulation are outlined in Section 4.2.2 which was designed for high

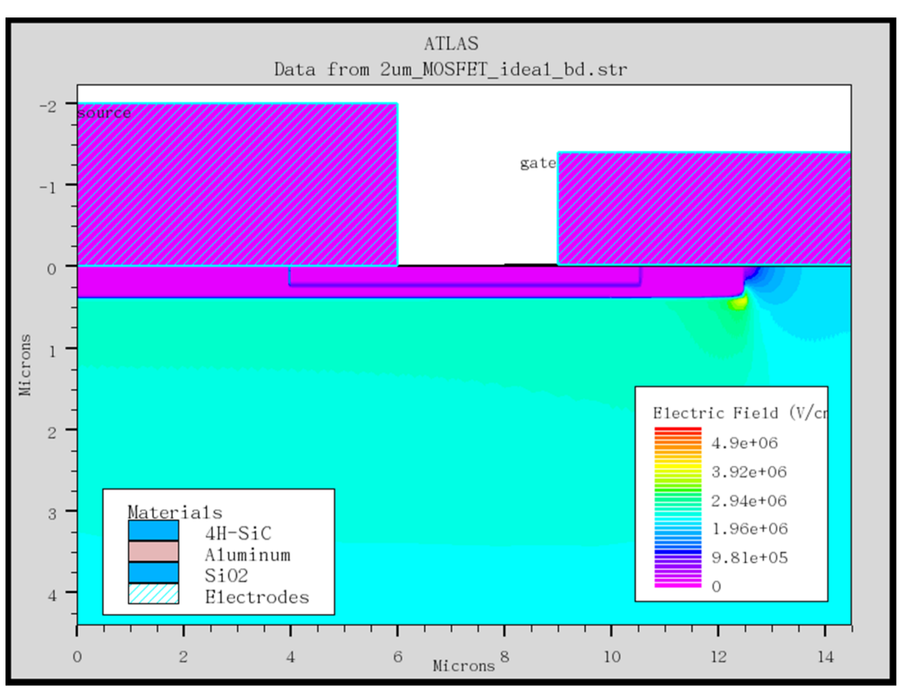


Figure 3.43: Breakdown electric field distribution of the 3.3 kV shielded planar VD-MOSFET.

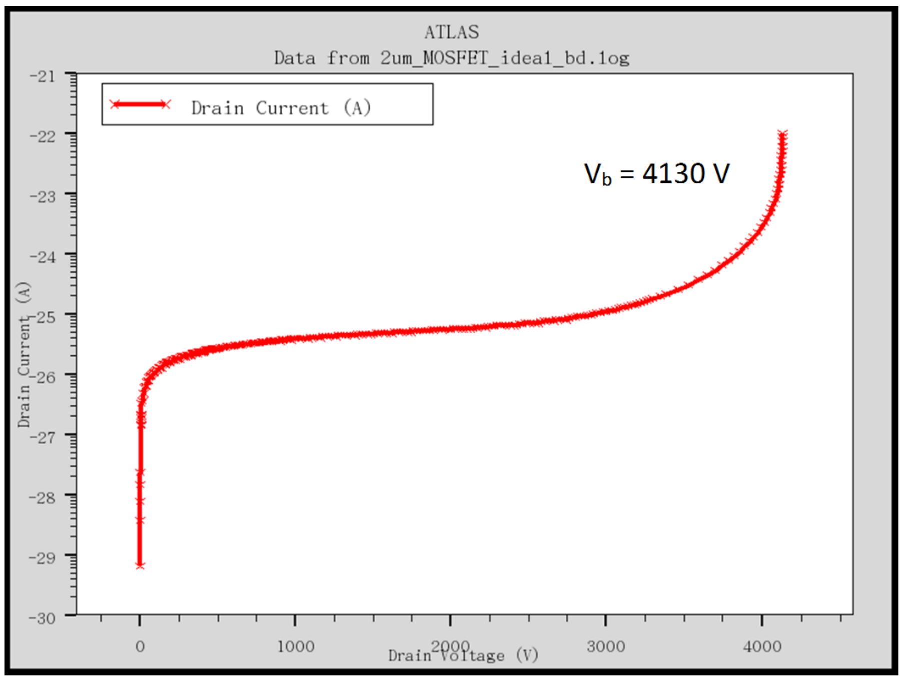


Figure 3.44: Breakdown characteristic of 3.3 kV shielded planar VD-MOSFET.

voltage devices (10 kV). The one-dimensional parallel plane breakdown voltage of the 3.3 kV shielded planar VD-MOSFET structure is 4130 V as illustrated in Figure 3.44, and the simulated breakdown voltage of the two-dimensional shielded planar VD-MOSFET structure without edge termination was found to be 587 V.

The 3.3 kV shielded planar VD-MOSFET structure with the SMJTE structure is similar to those shown in Figure 3.38 for the 1 kV shielded planar VD-MOSFET structure, except the difference in the drift region thickness and doping concentration. The simulation results of the breakdown performance with different JFET doping concentration is shown in Figure 3.45. It is seen that with the SMJTE structure the shielded planar VD-MOSFET increases the breakdown voltage to 2600 V with the JTE doping concentration of 2.2×10^{17} cm^{-3}, which is the optimum doping concentration for the SMJTE structure.

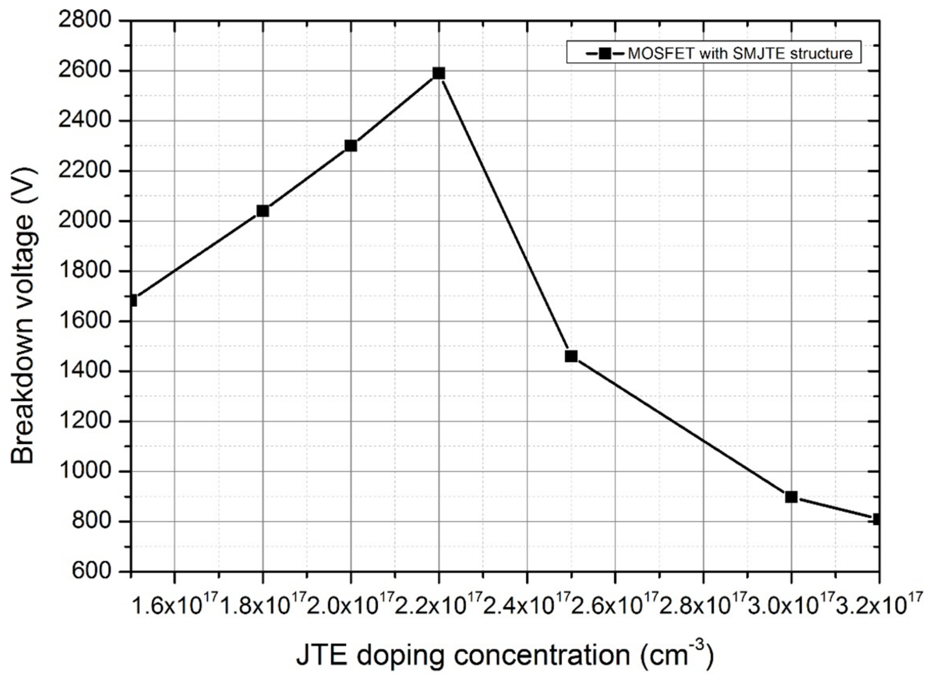


Figure 3.45: The simulated breakdown voltage versus SMJTE doping concentration for the 3.3 kV shielded VD-MOSFET.

3.4 Summary

In this Chapter, the design of high voltage 4H-SiC shielded inversion-mode power MOSFET and different JTE have been presented. The device design including the drift region design for both 1 kV, 3.3 kV and 10 kV devices were first outlined. Recent publications [67, 97, 98] have shown that the equations published by Baliga [44] for breakdown voltage of 4H-SiC are overestimated by up to 80%. A different impact ionisation equation for 4H-SiC used as published in literature [97] was used in this work. The effects of JFET region doping concentration and its width on breakdown voltage and on-state resistance of shielded planar VD-MOSFET were investigated. Simulation results show that the optimum width of JFET region is around 2 μm, which gives the lowest on-state resistance

and high breakdown voltage. Next, the design and numerical simulation of different JTE structures have been performed for the 1 kV 4H-SiC Schottky diode, including single-zone JTE, space modulated JTE (SMJTE) and the novel two-step mesa JTE structures. It was found that for the same doping concentration the SM two-zone JTE and SMJTE have higher breakdown voltage than the single zone JTE. With SM two zones JTE, the device could achieve up to 97% of the ideal parallel plane voltage and gives a wider optimum JTE dose window than single zone JTE and SMJTE structures. However, it has a disadvantage of having more implantation steps which result in higher cost. Therefore, for the cost saving and ease of fabrication, the SMJTE structure was used in the fabrication in this work as it provides good breakdown voltage and wider JTE dose window than the conventional single zone JTE. Two-step mesa JTE structure was also investigated. Results show that with the additional P-ring implants to the two-step mesa JTE structure, it could get up to 99% of the ideal parallel plane breakdown voltage and provides the widest optimum doping window. However, this structure is more complicated in design and fabrication than other JTEs structures. The effects of surface charge on breakdown voltage have been investigated. Simulation results shown that the presence of oxide charge will cause a shift in the reverse breakdown voltage against the JTE doping concentration profile. A positive charge will result in a shift of the peak breakdown voltage towards the heavier JTE dose and a negative charge will shift the peak breakdown voltage towards lighter JTE doping.

Finally, the numerical simulations of 1 kV and 3.3 kV shielded inversion-mode power

MOSFETs were performed, highlighting the high breakdown voltage while keeping the threshold voltage low by the use of P+ shielding region. Simulation results show that the total on-resistance of the devices are comparable to the ideal specific on-resistance for the same VD-MOSFET structure by adding up the channel, accumulation, JFET and drift region resistances. For 1 kV and 3.3 kV shielded planar VD-MOSFETs, the channel resistances are the major contributor on the total on-resistance, which takes up about 83% and 48.9% of the total on-resistance respectively. However, for 10 kV shielded planar VD-MOSFETs the channel resistance is negligible ($< 10\%$) compare to the large drift region resistance, which takes up about 90% of the total on-resistance.

Chapter 4 Characterisation Techniques for High Voltage 4H-SiC Devices

This chapter is aimed at introducing the characterisation techniques employed within this work. The methods presented can extract useful information with respect to the semiconductor contact properties. The characterisation is divided into two categories: electrical and physical. Electrical characterisation can yield information of the contact resistivity, on-state characteristics, reverse breakdown behaviour and capacitance-voltage characteristics. Physical characterisation of semiconductors yields an assessment of the physical and morphological aspects of a device structure. The physical metal-semiconductor interface properties were also examined and correlated to the electrical performance.

4.1 Physical Characterisation

In this Section, the physical characterisation methods that have been employed in the analysis of the 4H-SiC MOSFET fabricated in this work are discussed. A brief overview

of each of the microscopy and spectroscopy techniques is given.

4.1.1 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) or scanning force microscopy (SFM) is a very high-resolution type of scanning probe microscopy, with demonstrated resolution of the order of fractions of a nanometer. It was used to measure the surface morphology of samples, such as the surface roughness and the step height measurement. The system consists of a small probe that is passed across the surface of a sample to obtain information regarding the physical properties of that surface, as illustrated in Figure 4.1. For the work in this thesis, the Asylum research MFP-3D AFM, located in the Physics Department at the University of Warwick has been used. The AFM system was used in this work to obtain surface roughness measurements on 4H-SiC samples after implant activation with and without the carbon cap.

An AFM image is obtained by scanning the cantilever tip over the sample surface. When the tip is brought into close proximity of the surface of the sample, forces between the tip and the sample lead to a deflection of the cantilever according to Hookes law. The deflection is measured using a laser spot, which is reflected from the top of the cantilever into an array of photodiodes. Any change in displacement of the cantilever would result in a change of output signal from the photodiode array. The signal is received by the feedback electronics which controls the cantilever.

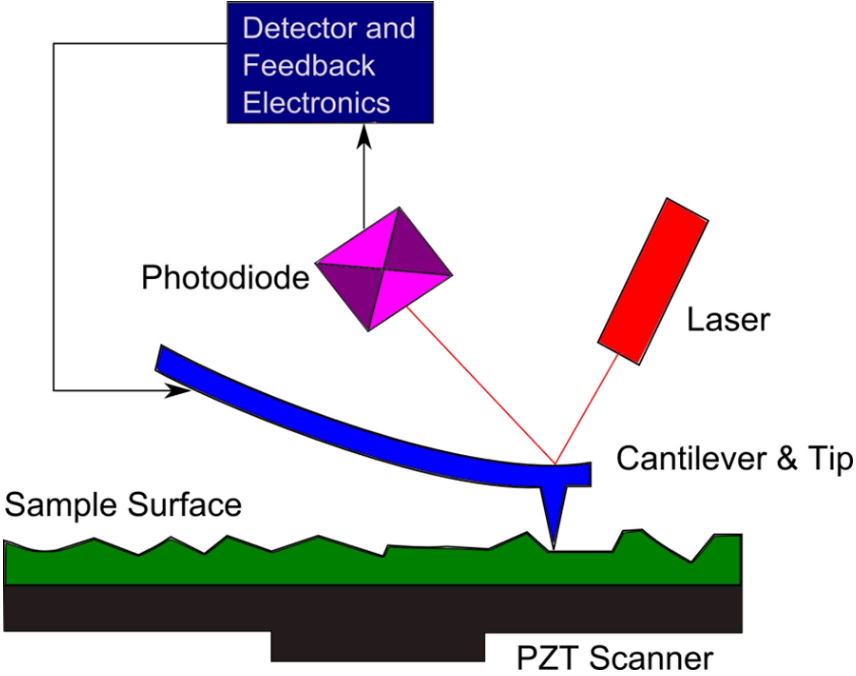


Figure 4.1: Block diagram of atomic force microscope using beam deflection detection.

There are numbers of modes that the AFM can operate, according to the nature of the tip motion. In general, imaging modes are divided into static (also called contact) modes and a variety of dynamic (non-contact or tapping) modes where the cantilever is vibrated. In contact mode, the tip is in contact and move across the surface of the sample. The contours of the surface are measured either using the deflection of the cantilever directly or using the feedback signal required to keep the cantilever at a constant position. In tapping mode (also called AC mode), the cantilever is driven to oscillate up and down at near its resonance frequency by a small piezoelectric element mounted in the AFM tip holder. The height of the cantilever above the sample is controlled using a piezoelectric actuator, with the feedback electronics adjusting the height to maintain a set oscillation

amplitude as the cantilever is scanned over the sample. Similar to the tapping mode, the tip of the cantilever does not contact the sample surface in the non-contact mode. The cantilever is oscillated at either its resonant frequency or just above. Non-contact mode AFM does not suffer from tip or sample degradation effects which may observe with contact AFM after many scans. In this work, contact mode was used for all AFM imaging on 4H-SiC samples.

4.1.2 Secondary Ion Mass Spectrometry (SIMS)

Secondary ion mass spectrometry (SIMS) is a technique used to analyse the composition of solid surface and thin films by sputtering with a focused primary ion beam and collecting and analysing ejected secondary ions. In this work, SIMS has been applied to determine the distribution of implanted dopant species in 4H-SiC material. All SIMS analysis presented in this thesis has been carried out at Loughborough Surface Analysis, Ltd [109].

There are two main variants of SIMS techniques, static SIMS and dynamic SIMS. All of these techniques are based on the same basic physical process which is discussed here. High energy ions were sent by the ion gun to bombard the surface of the sample, resulting the ejection of both neutral and charge species from the surface. Figure 4.2 illustrates this secondary ion sputtering process.

The dynamic SIMS technique, which is the technique relevant to the work in this

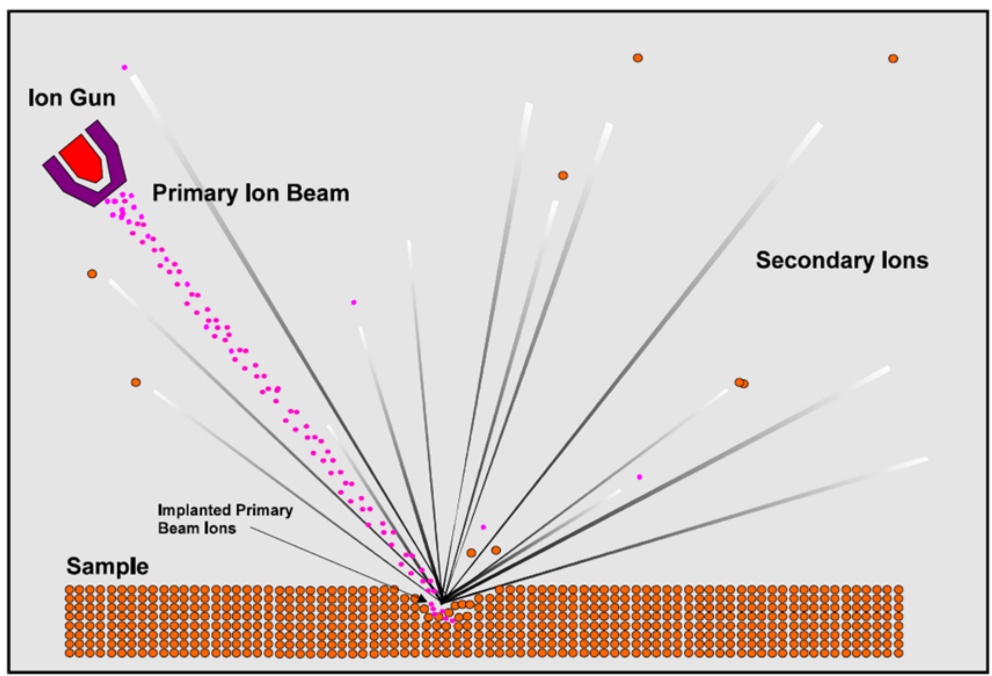


Figure 4.2: Secondary ion sputtering process of SIMS [110].

thesis, involves using an ion beam with much higher current density. The aim is to obtain information on the variation of composition with depth below the initial surface, which is particularly useful for the analysis of layered structures such as those produced in the semiconductor industry. This technique is a destructive process as it need to remove atoms from the surface, but it is ideally suited for obtaining depth profile of a sample. The depth profile of a sample is obtained by recording sequential SIMS spectra as the surface is etched away by ion bombardment.

Once the primary ion beam ionises and sputters some of the atoms off the surface of the sample, the secondary ions are collected and filtered according to their atomic mass in the mass analyser. The secondary ions are then detected by means of Faraday cup, which

measures the ion current and outputs it to the imaging system. A schematic of a typical dynamic SIMS instrument is shown in Figure 4.3. One of the main advantages that SIMS

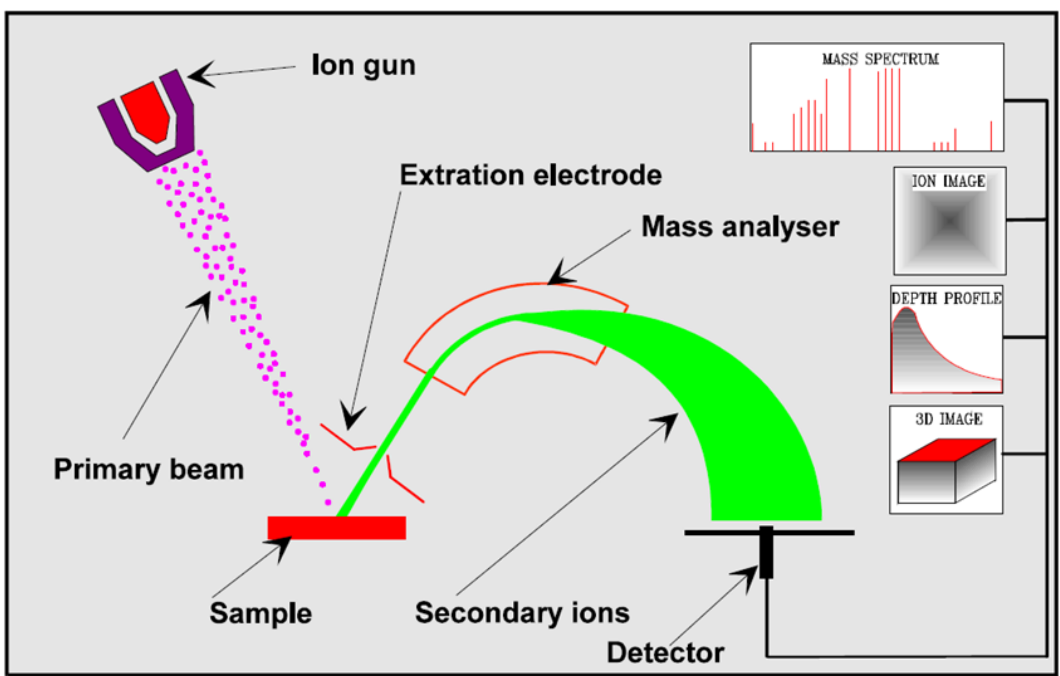


Figure 4.3: Schematic of a typical dynamic SIMS instrument [110].

offers over other depth profiling techniques, such as Auger depth profiling is its capability of measuring very low concentration of dopants (sub-ppm or ppb), this is important in the semiconductor industry where dopants are usually at very low concentrations.

4.2 Electrical Characterisation

In this section, the electrical characterisation techniques undertaken within this work are discussed. These are I-V and C-V measurements. All of the techniques covered in this

work are discussed by Schroder [111].

4.2.1 Capacitance-Voltage (C-V) Measurements

The capacitance-voltage (C-V) measurement is of great importance when considering the metal oxide semiconductor (MOS) devices characterisation. C-V measurement can extract many important parameters such as semiconductor doping concentration, oxide thickness, flat-band voltage and interface trap density between oxide and semiconductor. There are also different C-V techniques to extract the interface trap density of the MOS devices, namely High-Low frequency C-V, High frequency C-V (i.e. Terman method) and Conductance techniques. This work is mainly focused on using High-Low frequency C-V and High frequency techniques for MOS devices analysis, which will be discussed in more details under the Interface Traps section. C-V characterisation technique is carried out using the Agilent E4980A Precision LCR meter, located in Physics department at the University of Warwick.

4.2.1.1 Oxide Thickness

For an oxide thickness larger than 50 Å, extracting the oxide thickness is fairly simple. The oxide capacitance (C_{OX}) is the high frequency capacitance when the device is biased for strong accumulation. The oxide thickness (T_{OX}) can be calculated from C_{OX} and the

gate area using the following equation:

$$T_{OX} = A \times \frac{\varepsilon_{OX}}{C_{OX}} \tag{4.1}$$

where A is the gate area (cm^2), ε_{OX} is the permittivity of the oxide material (F/cm), and C_{OX} is the oxide capacitance (F) measured by C-V curve in strong accumulation region.

4.2.1.2 Doping Concentration

The doping concentration (N_D or N_A) of the epitaxial layer where the MOS capacitor is fabricated on can be calculated using the following equation:

$$N = \frac{2}{q\varepsilon_S A^2 \left(\frac{\Delta 1/C^2}{\Delta V_G}\right)} \tag{4.2}$$

where q is the electron charge (C), ε_S is the permittivity of the substrate material (F/cm), A is the gate area (cm^2), C is the measured capacitance (F) and V_G is the gate voltage (V). The epitaxial layer doping concentration (N) is related to the reciprocal of the slope of the $1/C^2$ plotted as a function of V_G as shown in Figure 4.4. The intersection of the $1/C^2$ versus V_G plot is the build-in potential, V_{bi}. The background doping concentration N can be found from the gradient of the $1/C^2$ versus V_G plot. Depending on the dopant uniformity and the quality of the oxide layer, the C-V curve could be distorted and the gradient of the $1/C^2$ versus V_G plot may not be linear. Therefore, this method is only

used as a guideline to estimate the doping concentration of the epitaxial layer.

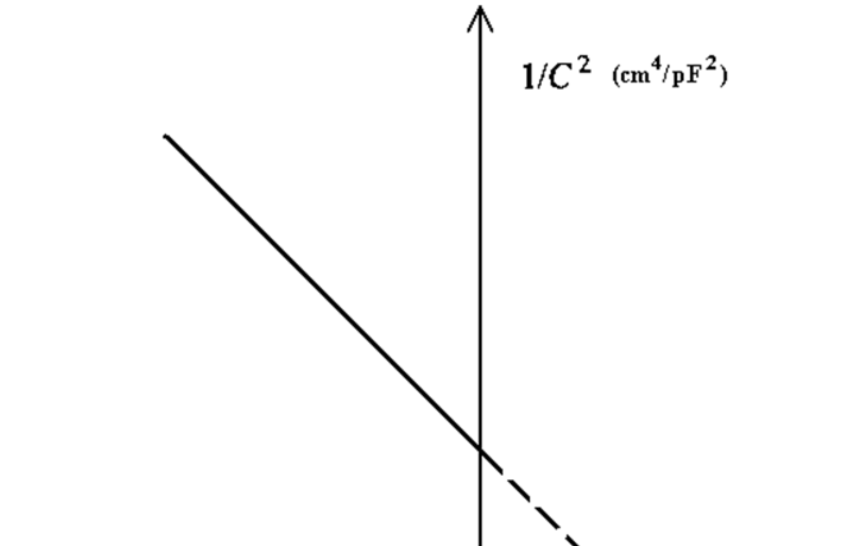


Figure 4.4: $1/C^2$ versus V_G plot used to determine the background concentration and built-in potential of a semiconductor junction.

4.2.1.3 Flat-band Voltage

For an ideal MOS capacitor, the flat-band voltage (V_{FB}) is zero. For a non-ideal MOS capacitor, the flat-band voltage is determined by the metal-semiconductor work function difference ϕ_{MS} and the various oxide charges as described in [111], however, the values of various charges are not always known. Another easier way to determine V_{FB} is from the $((1/C_{hf})^2)$ versus V_G as shown in Figure 4.5. The flat-band voltage is equal to the lower knee voltage, $V_G = V_{FB}$. This transition is sometimes difficult to determine, so differentiating the curve and finding the maximum slope is usually performed. The first

differentiation generates two peaks and the V_{FB} occurs at the left peak of this differentiated curve as illustrate in Figure 4.5 [111].

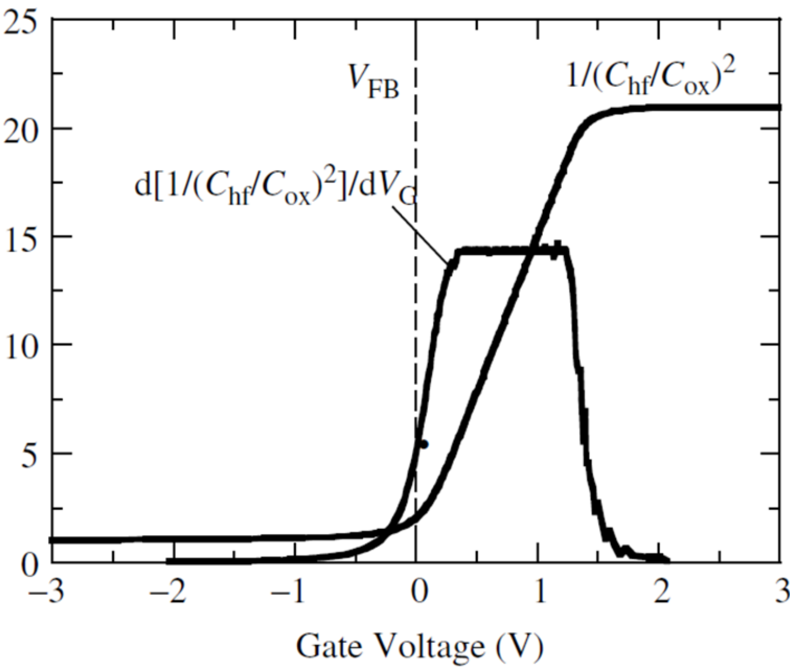


Figure 4.5: High frequency of $1/\left(C_{hf}/C_{OX}\right)^2$ versus gate voltage plot, and the differentiation of the curve showing the flat-band voltage V_{FB} [111].

4.2.1.4 Interface Trap Density

Interface trapped charge, also known as interface traps or states are the major obstacle for the silicon carbide devices to achieve high channel mobility. The origin of these charges is not well understood but mainly is related to dangling bonds and carbon clusters at the semiconductor/insulator interface [112]. These interface traps capture electrons and holes, in addition, the charge traps also act as Columbic scatting centres which would

decrease the effective channel mobility of MOSFET. In this section three commonly used C-V characterisation techniques to extract the interface trap density are discussed.

4.2.1.4.1 High Frequency Capacitance Method

The high frequency method is also called the Terman method, which was one of the first methods for determining the interface trap density. It is assumed that at a sufficiently high frequency (usually 1 MHz) the interface traps do not respond and will not affect the capacitance, however, they do respond to the slowly varying dc gate bias. This will cause the high frequency C-V curve to stretch out as the gate bias is swept from accumulation to inversion regions. Figure 4.6 illustrates the theoretical C-V curve and the stretch out C-V curve [46].

This method is based on the extraction of the experimental surface potential ψ_S versus gate voltage curve, by comparing the experimental C-V curve with the theoretical C-V curve. From ψ_S versus V_G curve, the derivative $(d\psi_S)(dV_G)$ can be found. The interface trap density can be determined from the following equation:

$$\mathrm{D_{it}}\left(\psi_S\right) = \frac{1}{q\mathrm{A}}\left(C_{\mathrm{OX}}\left[\left(\frac{d\psi_S}{dV_G}\right)^{-1} - 1\right] - C_S\left(\psi_S\right)\right) \tag{4.3}$$

where C_S is the semiconductor capacitance, and the exact doping concentration of the semiconductor must be known in order to calculate $C_S(\psi_S)$ relation.

4.2.1.4.2 Combined High-Low Frequency Capacitance Method

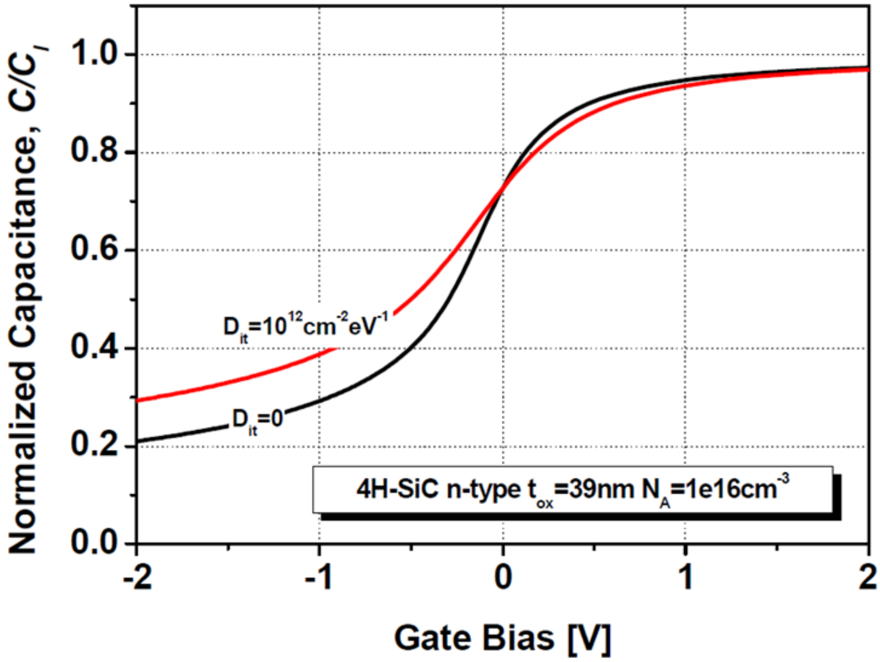


Figure 4.6: Theoretical C-V curve (shown in black) compared with the C-V curve with interface trap (shown in red) [46].

The combined high and low frequency C-V curves can obtain a measured semiconductor capacitance C_{S} which eliminates the need for a theoretical computation of C_{S} [113]. In the high-low frequency C-V technique, capacitance is measured at two different frequencies One frequency low enough so that all the interface traps can respond to the signal and one high enough so that all the traps at the given surface potential cannot respond to the signal. The interface trap density can be determined from the following equation:

$$\mathrm{D_{it}}\left(\psi_{\mathrm{S}}\right) = \frac{1}{q\mathrm{A}}\left(\left[\frac{C_{\mathrm{lf}}C_{\mathrm{OX}}}{C_{\mathrm{OX}} - C_{\mathrm{lf}}}\right] - \left[\frac{C_{\mathrm{hf}}C_{\mathrm{OX}}}{C_{\mathrm{OX}} - C_{\mathrm{hf}}}\right]\right) \tag{4.4}$$

The interface trap density obtained from this equation is only accurate over a limited

range of the band gap. This typically corresponds to an energy about 0.2 eV from the majority carrier band edge. Figure 4.7 shows a high frequency and low frequency curves of one of the fabricated 4H-SiC devices.

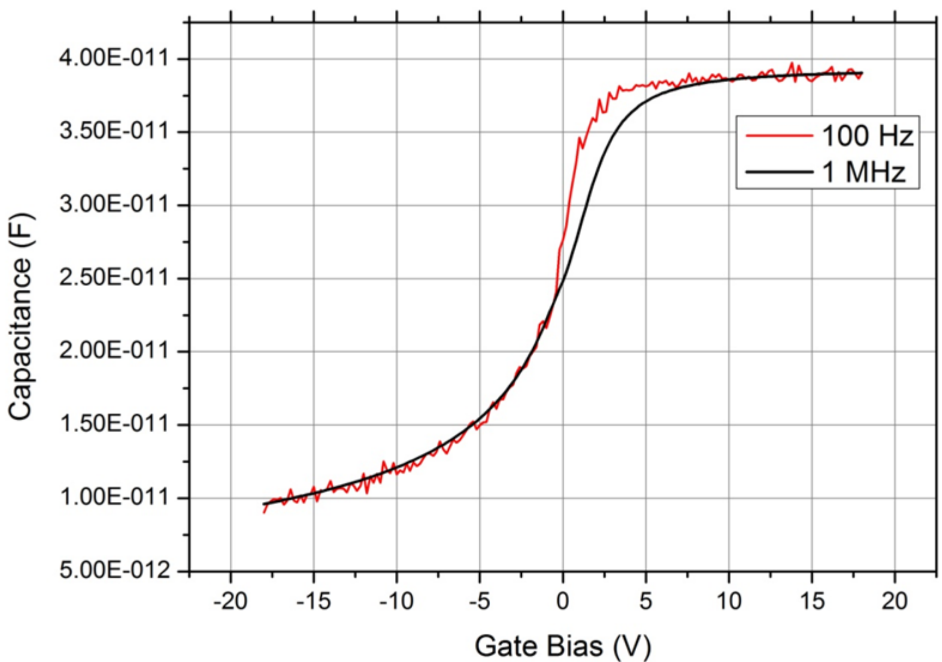


Figure 4.7: High and low frequency C-V curves showing the offset of capacitance values due to interface traps.

The interface trap density is usually plotted against the energy band gap position. The position of the Fermi level with respect to the majority carrier band edge at the semiconductor surface can be determined as a function of gate bias:

$$\frac{E_{\mathrm{C}} - E_{\mathrm{T}}}{q} = \frac{E_{\mathrm{G}}}{2q} + \psi_{\mathrm{S}} - \phi_{\mathrm{B}} \tag{4.5}$$

so

$$E_C - E_T = \frac{E_G}{2} - kTU_S + kTU_F \tag{4.6}$$

where U_S is the normalised surface potential and U_F is the normalised Fermi potential.

4.2.2 Field-Effect Mobility

4H-SiC MOSFETs have historically been plagued by very low channel mobility that results from a high density of interface traps at the SiC/SiO_2 interface. It is important to improve the channel mobility of MOSFETs in order to fully utilise the full potential of silicon carbide devices. The field-effect mobility is determined from the transconductance, which is defined by

$$g_m = \frac{\partial I_D}{\partial V_G} \mid V_D = \text{constant} \tag{4.7}$$

We know that the drain current with $Q_n = C_{OX}(V_G - V_{TH})$ is

$$I_D = \frac{W}{L}\mu_{eff} C_{OX}(V_G - V_{TH}) V_{DS} \tag{4.8}$$

So the transconductance is taken to be

$$g_m = \frac{W}{L}\mu_{FE} C_{OX} V_{DS} \tag{4.9}$$

Mobility can be solved, it is known as the field-effect mobility

$$\mu_{\mathrm{FE}} = \frac{Lg_{\mathrm{m}}}{WC_{\mathrm{OX}}V_{\mathrm{DS}}} \tag{4.10}$$

where W and L are the channel width and length of the MOSFET, C_{OX} is the oxide capacitance which can be determined by knowing the oxide thickness and V_{DS} is the drain voltage which is kept at 100 mV for the mobility extraction in this work.

4.2.3 Current-Voltage (I-V) Measurements

The current-voltage (I-V) measurement is one of the most important measurements for contact assessment and semiconductor device characterisation. The I-V characterisation was a key measurement technique in this work being use to analyse the performance of the contacts and devices. Low-current (up to 100 mA) measurements have been performed at the University of Warwick using an Agilent Technologies B1500A Semiconductor Parameter Analyser. The probe station was setup for either lateral or vertical device measurement with four probes, where two probes were used for force and two for sense, to prevent the probe resistance affecting the results.

To perform a simple voltage sweep, the analyser provides a known voltage across the device and measures the current being passed through it. The amount of current allowed to pass through the device is limited by the power rating of each Source Measuring Unit (SMU) used. The measurement data will be stored within its memory and can be exported

via various media for further data analysis.

4.2.4 Contact Resistance Measurements

It is important to characterise the resistance of metal-semiconductor contact especially for power devices, since high contact resistivity would increase the total on resistance and power loss in the form of heat across semiconductor devices. The resistance of metal-semiconductor ohmic contacts is of particular interest. An ohmic contact between two conductors normally has linear current-voltage (I-V) curve as with Ohms law. The contacts must be able to supply the necessary current, and the voltage drop across the contact should be small compare to voltage drops across the active device region. There are several techniques that have been developed for accessing the electrical characteristics of metal-semiconductor contacts [111], a widely-used technique and the one that has been applied in this work, is the Transmission Line Method (TLM).

Before introducing the ohmic contact test structures, the contact resistance must be defined. Figure 4.8 shows the cross-sectional representation of a semiconductor substrate with implanted layer. Two metal contacts are denoted as A and B in the figure. Total resistance R_{T} between two points A and B are divided into three components: resistance of metallic conductor R_{m}, the contact resistance R_{c}, and the semiconductor resistance R_{s}. This can be expressed by the following equation:

$$R_{\mathrm{T}} = 2R_{\mathrm{m}} + 2R_{\mathrm{c}} + R_{\mathrm{s}} \tag{4.11}$$

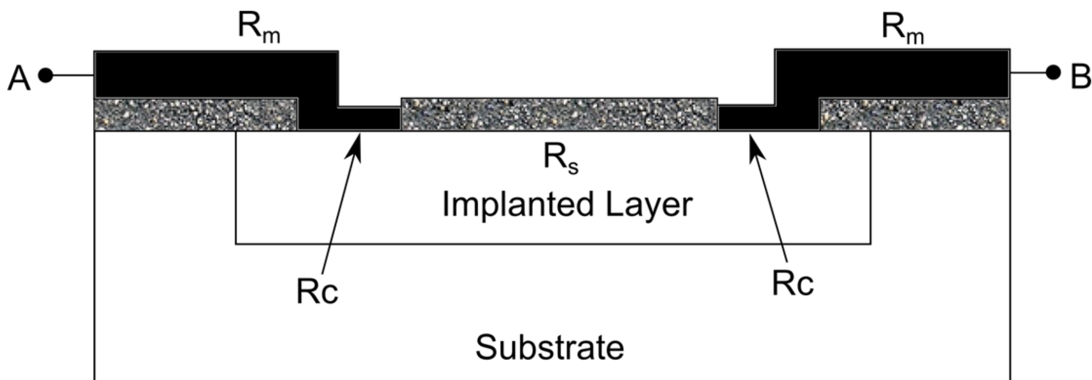


Figure 4.8: Cross-sectional schematic of semiconductor showing metallic contact on an implanted layer with associated resistances: metal resistance R_{m}, contact resistance R_{c} and semiconductor resistance R_{s}.

The most widely used technique to determine the contact resistivity is the transmission line model (TLM) technique. This structure consists of two large contact pads at either end of the arrangement, separated by a number of smaller contacts pads in between. Figure 4.9 illustrates the TLM test structure, which has number contact pads with unequal spacing. The theory is that when the distance between adjacent contact pads is varied,

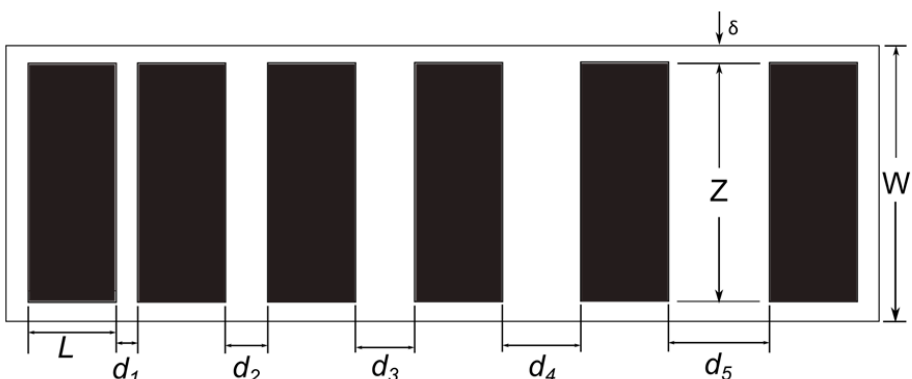


Figure 4.9: Transfer length method test structures.

the sheet resistance, R_{s} is changing whilst the contact resistance, R_{c} remains the same.

This allows the extraction of both sheet and contact resistance. The total resistance between any two contacts is given by

$$R_{\mathrm{T}} = \frac{R_{\mathrm{sh}} d}{\mathrm{Z}} + 2R_{\mathrm{c}} \approx \frac{R_{\mathrm{sh}}}{\mathrm{Z}} \left(d + 2L_{\mathrm{T}} \right) \tag{4.12}$$

where L_{T} is the transfer length, which can be defined as the distance over which most of the current transfers from the semiconductor into the metal or from the metal into the semiconductor. Equation 4.12 assumes that the contact length L is $\geq 1.5L_{\mathrm{T}}$, where

$$L_{\mathrm{T}} = \sqrt{\rho_{\mathrm{C}} / R_{\mathrm{sh}}} \tag{4.13}$$

In which ρ_{C} is specific contact resistance, and R_{sh} is the sheet resistance.

The total resistance (R_{T}) is measured for various contact spacing (d_{x}), and plotted against d as illustrated in Figure 4.10. From this plot, sheet resistance can be extracted from the slope $\Delta R_{\mathrm{T}}/\Delta \mathrm{d} = R_{\mathrm{sh}}/\mathrm{Z}$, the contact resistance R_{c} from the intercept at $\mathrm{d} = 0$, which is R_{T}=$2R_{\mathrm{c}}$, and the specific contact resistance ρ_{C} from the intercept at $R_{\mathrm{T}} = 0$, which gives $-d = 2L_{\mathrm{T}}$.

However, the problem of the TLM contact measurement technique is that equation 4.12 assumes the sheet resistance underneath the contact is the same as between contacts. But after annealing, which is typically required for forming the ohmic contacts to 4H-SiC, the sheet resistance underneath the contact will differ from sheet resistance between contacts.

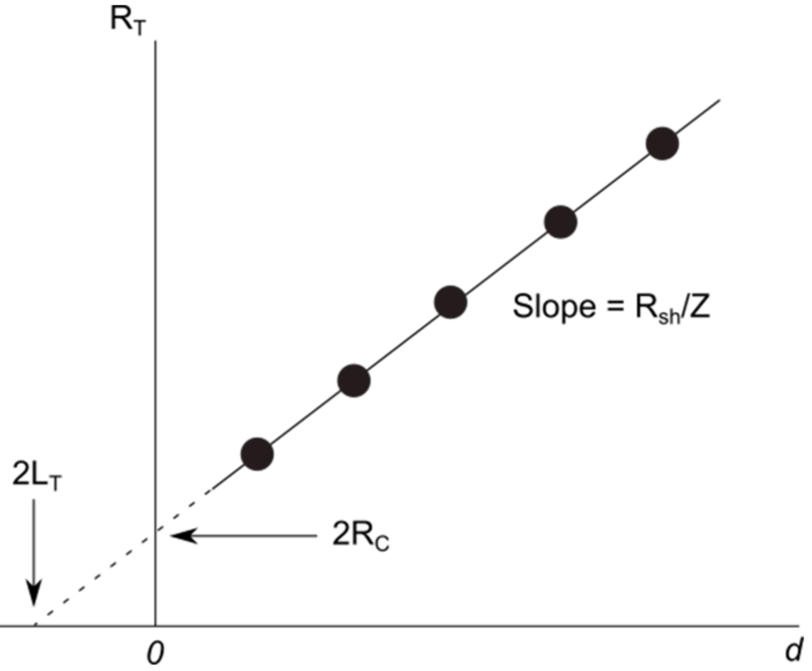


Figure 4.10: Transfer length method plot of total resistance as a function of contact spacing.

A modified expression for the contact resistance and total resistance are as those discussed in [114]:

$$R_{\mathrm{c}} = \frac{\rho_{\mathrm{C}}}{L_{\mathrm{Tk}}} \coth\left(L/L_{\mathrm{Tk}}\right) \tag{4.14}$$

and

$$R_{\mathrm{T}} = \frac{R_{\mathrm{sh}} d}{\mathrm{Z}} + 2R_{\mathrm{c}} \approx \frac{R_{\mathrm{sh}} d}{\mathrm{Z}} + \frac{2R_{\mathrm{sk}} L_{\mathrm{Tk}}}{Z} = \frac{R_{\mathrm{sh}}}{\mathrm{Z}} \left[d + 2\left(R_{\mathrm{sk}}/R_{\mathrm{sh}}\right) L_{\mathrm{Tk}}\right] \tag{4.15}$$

where R_{sk} is the sheet resistance under the contact and the transfer length is given by

$$L_{\mathrm{Tk}} = (\rho_{\mathrm{C}}/R_{\mathrm{sk}})^{1/2} \quad (4.16)$$

The R_{T} versus d plot still gives R_{sh} and R_{c} values, however, ρ_{C} cannot be determined from the intercept at R_{T}=0 since now it becomes $2L_{\mathrm{Tk}}\,(R_{\mathrm{sk}}/R_{\mathrm{sh}})$ and R_{sk} is unknown. In order to determine ρ_{C} we require additional resistance R_{ce} called end resistance. The end resistance measurement is done by measuring voltage between contacts 2 and 3 with the current flowing from 1 to 2, as illustrated in Figure 4.11. The end resistance R_{ce} is simply V/I, in relating to the TLM parameters is found to be

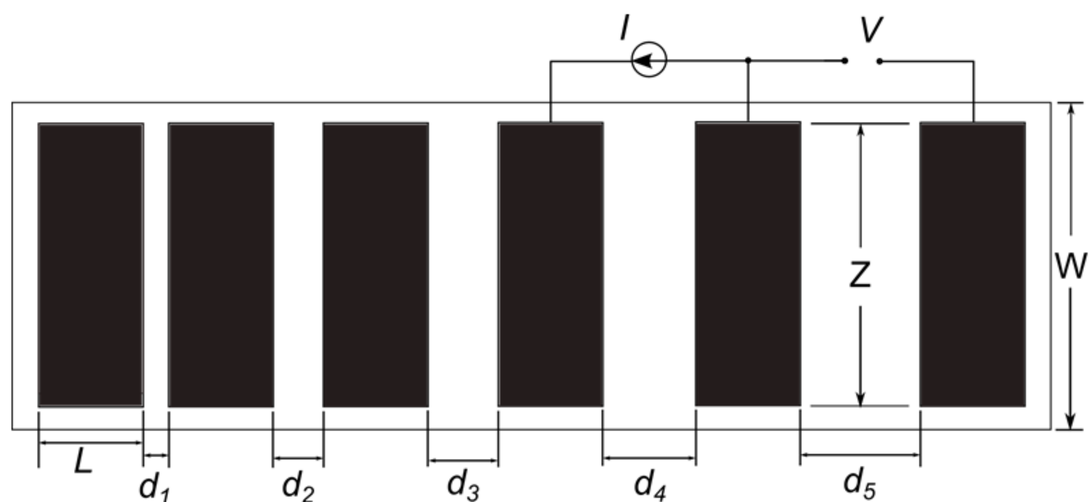


Figure 4.11: Transfer length method contact end resistance test structure.

$$R_{\mathrm{ce}} = \frac{V}{I} = \frac{\sqrt{R_{\mathrm{sk}}\rho_{\mathrm{C}}}}{\mathrm{Zsinh}\,(L/L_{\mathrm{Tk}})} = \frac{\rho_{\mathrm{C}}}{ZL_{\mathrm{Tk}}\mathrm{sinh}\,(L/L_{\mathrm{Tk}})} \quad (4.17)$$

Therefore

$$\frac{R_{ce}}{R_c} = \frac{1}{\cosh\left(L/L_{Tk}\right)} \tag{4.18}$$

L_{Tk} can be determined and thus ρ_C

The correct extraction of electrical contact parameter is based on the assumption of constant electrical and geometrical contact parameters across the sample. However, in practice, these parameters will vary across the sample due to presence of defects in the semiconductor. It is therefore useful to have multiple test structures across the sample to reduce the measurement error. Another error we need to consider is the gap δ between the edge of the contact pads and the periphery of the mesa-etched TLM test structure, illustrated in Figure 4.9. As $\delta \neq 0$ in fabricated TLM structure, there will be current flow and crowding in the gap region δ, and this can lead to incorrect intercepts of $R_T - \mathrm{d}$ plot. However, the effects of lateral current flow and current crowding can be neglected if $\delta \ll \mathrm{Z}$ as shown by [115].

4.3 Summary

In this Chapter, both the electrical and physical characterisation techniques utilised in this work that have been presented. The characterisation techniques presented are important as they allow extraction of many important semiconductor parameters such as specific

contact resistivity, surface roughness, interface trap density and doping concentration.

The Current-Voltage (I-V) and the Capacitance-Voltage (C-V) characterisation techniques are widely used throughout the work in this thesis, their methodology and apparatus used have briefly summarised. The Capacitance-Voltage (C-V) characterisation technique is introduced since this method can give us important information about the interface trap between the oxide and semiconductor, which affect the threshold voltage, on-state resistance and the mobility of MOSFET.

The contact resistance measurement technique and the test structure were discussed. Transfer length method test structure were introduced and proved to be important since specific contact resistivity measurement is the key to verify the contact formation in this work. The limitation of the TLM technique and the modify version of the expression using the end resistance for more accurate estimation of the contact resistivity were also discussed.

Chapter 5 Fabrication Process Development for 4H-SiC Devices

In this Chapter, the fabrication processes required for 4H-SiC MOSFETs that have been developed are presented. Firstly, the fabrication and characterisation of carbon capping layer on 4H-SiC to suppress the step bunching on 4H-SiC was carried out. Next, a study into the ion implantation and activation on 4H-SiC was presented. Different post-implantation annealing temperatures and time was carried out to find out the optimum conditions to give the best result on MOSFETs mobility. Following this, TLM structures were fabricated and characterised to determine the low resistance and reliable ohmic contacts to both p-type and n-type 4H-SiC.

5.1 Carbon Capping Layer

SiC is much more difficult to process than Si because of the strong chemical bonding between silicon and carbon atoms. Thermal diffusion which is typically used for selective

doping of Si devices cannot be used on SiC due to its low diffusion coefficients of impurities [116]. Therefore, the ion implantation is the only practical way of achieving selective doping of SiC. However, ion implantation will cause significant lattice damage and a large proportion of implanted ions will reside at interstitial sites resulting poor dopant activation rate. Post implantation annealing at high temperature (>1500°C) is usually required to repair the damage to the crystal lattice and electrically activate lattice sites [117, 118]. However, the high temperature annealing will cause surface roughening which is also referred to as step bunching. Another undesirable effect of high temperature post implantation annealing is the out-diffusion of implanted species, especially Boron which has been confirmed by many researchers [119–121]. There are several techniques to suppress SiC surface roughening and dopant out-diffusion, such as annealing with a silane overpressure [122] or use of capping layers such as carbon/graphite [123, 124], AlN [125], and SiO_2. All of these techniques have been shown to suppress the step bunching formation on SiC. Among all these techniques the carbon capping layer is the cheapest and easiest to implement and can cover any mesa-etched SiC sidewalls without any difficulty, unlike the AlN capping layer technique which does not work well on mesa structure sidewalls [125]. The use of thermally grown SiO_2 was also limited by the oxide melting point of 1610°C [126]. The carbon capping layer technique was chosen to use in this work for the protection of SiC surfaces during post-implantation annealing.

5.1.1 Fabrication Process

The 4H-SiC used in this study were N-type epitaxial layer with thickness of 10 μm and doping concentration of 2×10^{16} cm^{-3} supplied by Norstel AB. Samples were cleaned with standard organic and RCA cleaning (details of cleaning process are discussed in Appendix B) before deposition of photoresist. Different photoresists can be used to form a capping layer provided it gives reasonable thickness to cover all structures on the wafer after baking. AZ-5214E (1.4 μm) was used to form the capping layer by spinning at 4000 rpm for 60 seconds, and pre-bake at 90°C for 3 minutes and blank exposure of the whole surface. The samples were then baked at three different temperatures (115°C, 150°C and 200°C) with 30 minutes hold at each temperature. When applied to the mesa-etched surface, the AZ-5214E photoresist will need to be spun, pre-baked and exposed multiple times in order to fully cover the mesa sidewalls. Alternatively, a much thicker SPR-220-7 photoresist (7 μm) can be used which only require one layer. Conversion of the photoresist layer into carbon was achieved by baking the photoresist at 800°C for 40 minutes in nitrogen rich environment in a Carbolite annealing furnace as shown in Figure 5.1. Samples were put in a graphite box first as shown in Figure 5.2 before loading into the annealing furnace. After the annealing, photoresist will turn black, mirrorlike carbon/graphite layer, which is about 10 nm thinner than the original photoresist film.

A Carbolite CTF 18/300 high temperature advanced tube furnace as shown in Figure 5.1 was used for the high temperature post-implantation annealing. After the graphite

Figure 5.1: Carbolite CTF 18/300 high temperature advanced tube furnace.

layer is formed, samples were placed in a graphite box and cap as shown in Figure 5.2. Annealing was carried out at atmospheric pressure under argon flow in the ceramic tube, which had been previously purged and pumped out. The samples were annealed at various temperatures and times from 1600°C to 1700°C for 30, 45 and 60 minutes. Removal of the carbon capping layer is achieved by oxygen plasma ashing using Inductively Couple Plasma (ICP) etcher as shown in Figure 5.3.

5.1.2 Effects on 4H-SiC Surface Roughness

Atomic force microscopy (AFM) was used to examine the surface roughness of the 4H-SiC samples for both with and without carbon capping layer protection after high temperature

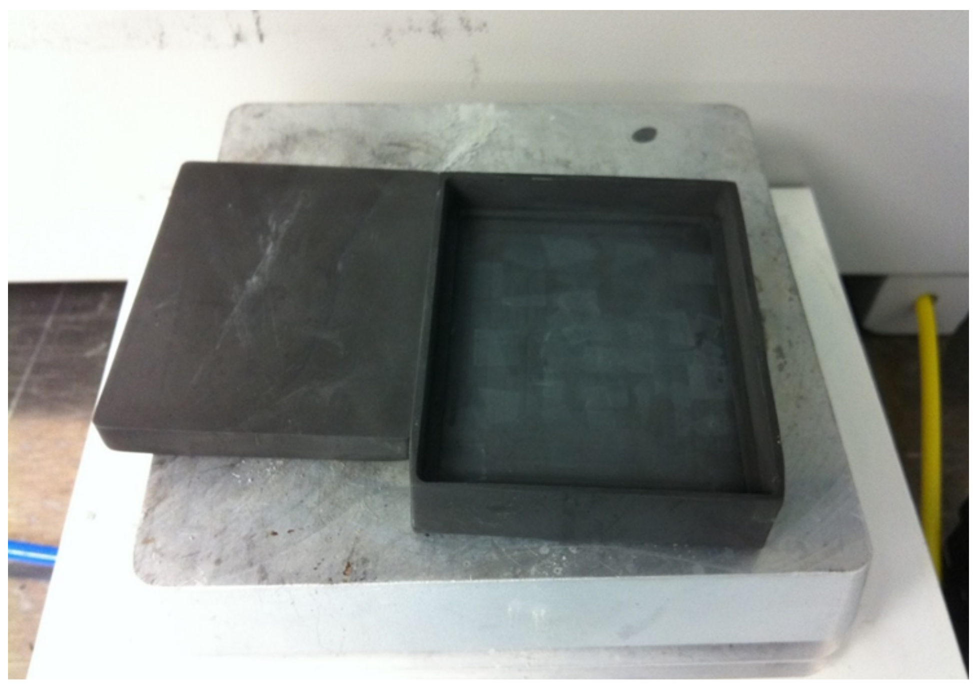


Figure 5.2: Graphite box and cap used for post-implantation annealing.

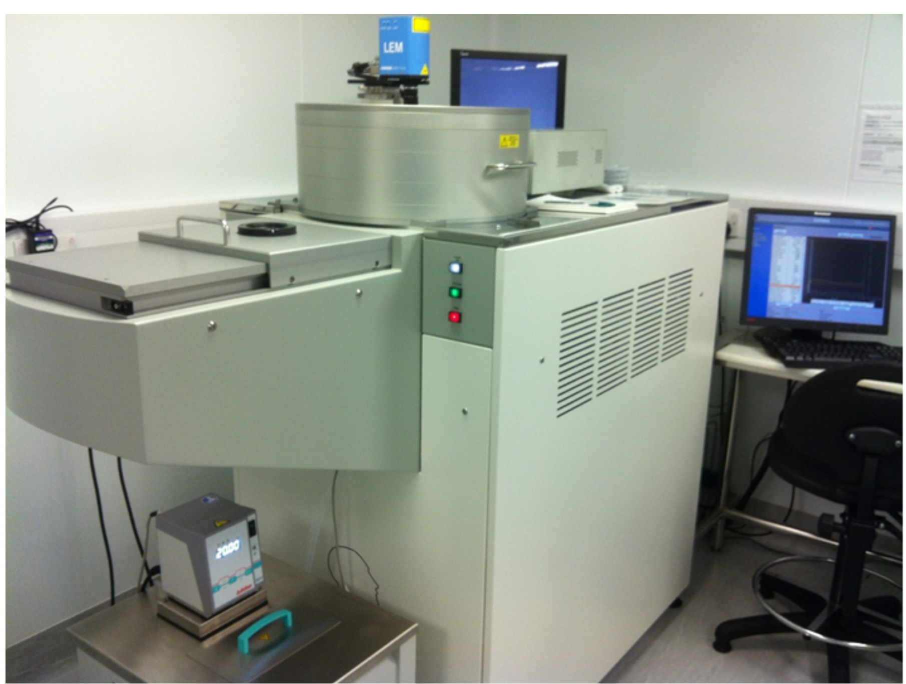
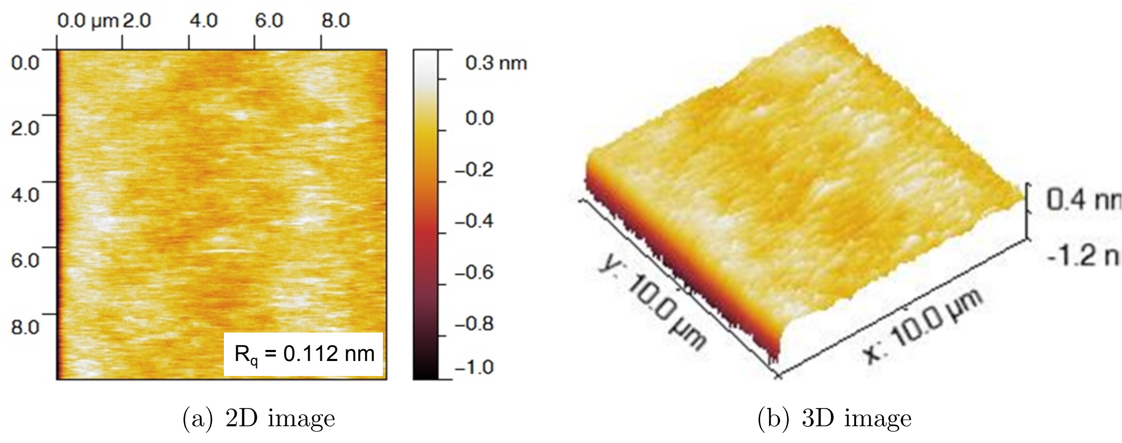


Figure 5.3: Inductively Couple Plasma (ICP) etcher in the clean room.

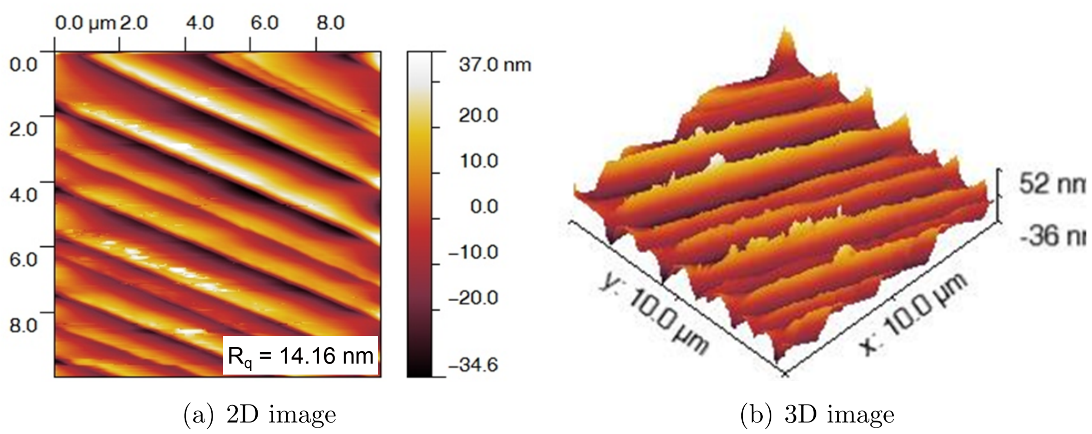
post-implantation annealing. Two 4H-SiC samples were cleaned using organic and RCA cleaning, and one of sample is deposited with SPR-220-7 thicker photoresist and then converted to a carbon capping layer using the process discussed in Section 6.1.1. Both samples were then put in the Carbolite CTF 18/300 high temperature furnace for post-implantation annealing at 1650°C for 1 hour. After the annealing was finished, carbon capping layer was then removed in the ICP etcher using oxygen plasma ashing for 40 minutes. AFM measurement were carried out to measure the samples surface roughness before the annealing, after the annealing without carbon capping layer and after the annealing with carbon capping layer. Results are shown in Figure 5.4 to Figure 5.6.



(a) 2D image (b) 3D image

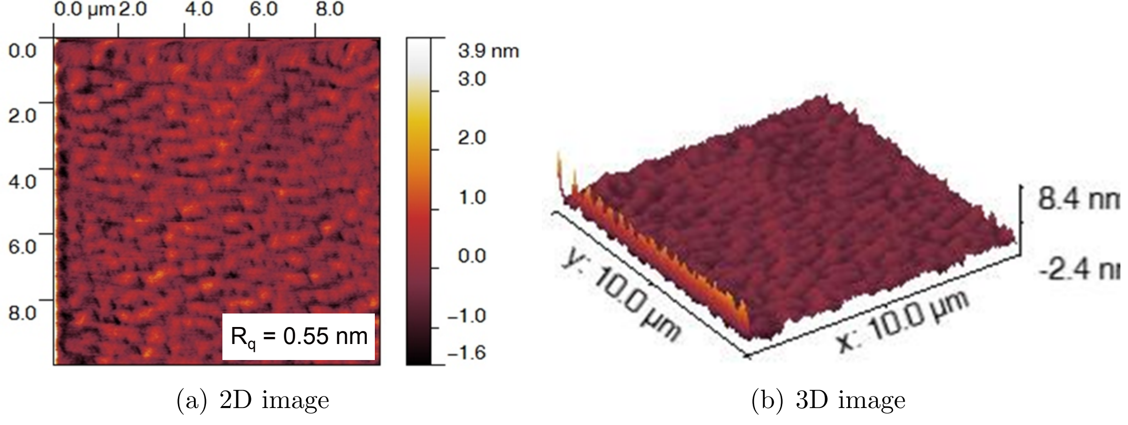
Figure 5.4: AFM scan on the original sample before annealing.

The AFM measurements were performed in the 10 μm × 10 μm area as shown in Figure 5.4 to Figure 5.6. It is seen that before the post-implantation annealing the sample has surface roughness of about 0.112 nm RMS. After the post-implantation annealing without the carbon capping layer protection, the surface shows large step bunching across the



(a) 2D image (b) 3D image

Figure 5.5: AFM scan on the sample after annealing at 1650°C for 1 hour without carbon capping layer.



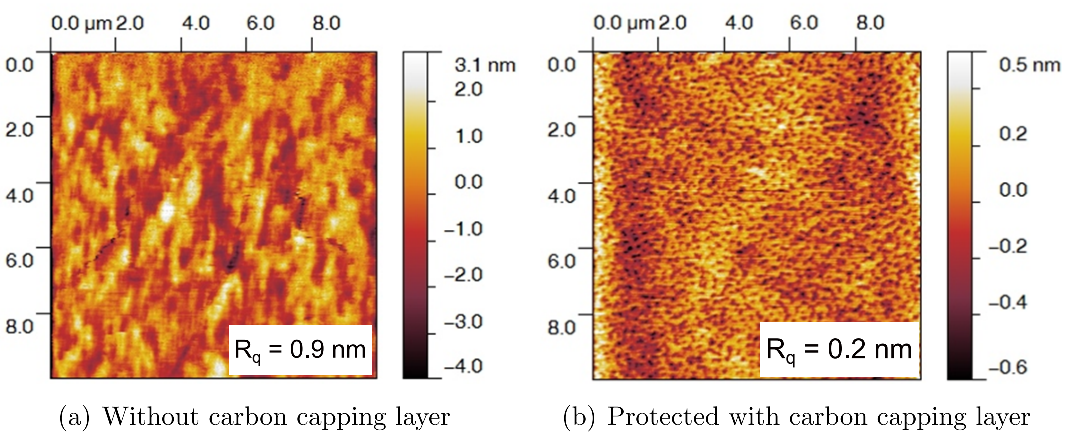
(a) 2D image (b) 3D image

Figure 5.6: AFM scan on the sample after annealing at 1650°C for 1 hour with carbon capping layer.

whole sample with roughness value increase to 14.16 nm RMS. The protected surface by using carbon capping layer, on the other hand, was planar with surface roughness of about 0.55 nm RMS. This value is larger than that of a virgin sample before annealing but is in good agreement with the results published in other literature [123, 127]. This results show that the properly converted carbon/graphite capping layer can effectively protects

SiC surface from step bunching.

Figures 5.7 shows the AFM measurement results on samples that have been annealed at 1600 C for 45 minutes with and without the carbon capping layer protection. It is seen that the step bunching has been eliminated by annealing at lower temperature and shorter time even without the carbon capping layer protection as shown in Figure 5.7(a). With the carbon capping layer protection, the surface roughness is reduced from 0.9 nm

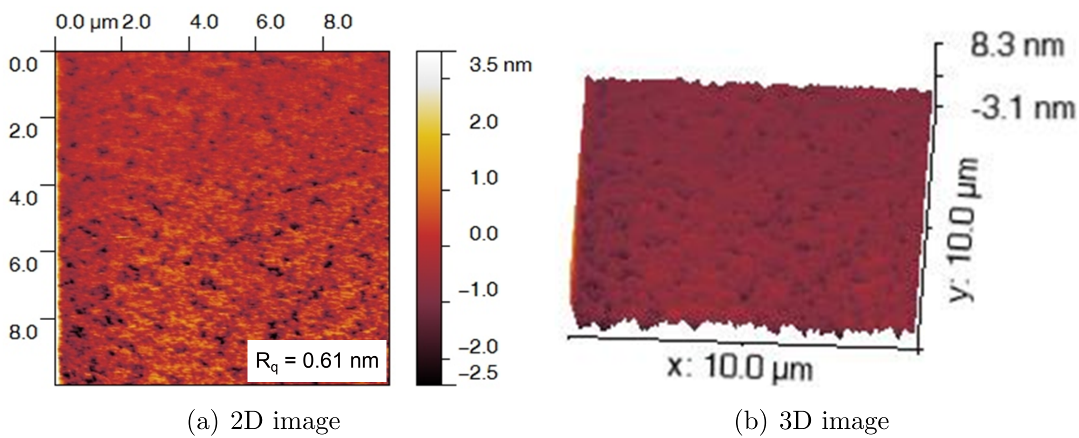


(a) Without carbon capping layer (b) Protected with carbon capping layer

Figure 5.7: The surface of 4H-SiC wafer after post-implantation annealing at 1600°C for 45 minutes.

RMS to 0.2 nm RMS as shown in Figure 5.7(b). Post-implantation annealing at 1700°C for 30 minutes were also carried out on SiC sample, results are shown in Figure 5.8. It can be seen that with the carbon capping layer protection, the surface roughness is about 0.61 nm RMS even after 1700°C annealing.

Table 5.1 summarise the above surface roughness results of a 4H-SiC sample both with and without carbon capping layer. From the AFM measurement results for samples



(a) 2D image (b) 3D image

Figure 5.8: AFM scan on the sample after annealing at 1700°C for 30 minutes with carbon capping layer.

Table 5.1: Surface roughness values of a 4H-SiC sample at different annealing temperature and time both with and without carbon capping layer.

Annealing Temperature and Time	R_q Without Carbon Cap	R_q With Carbon Cap
1600°C 45 minutes	0.9 nm	0.2 nm
1650°C 1 hour	14.16 nm	0.55 nm
1700°C 30 minutes	N/A	0.61 nm

annealed at 1600°C, 1650°C and 1700°C, it can be concluded that carbon capping layer effectively protects SiC surface from step bunching and limits the surface roughness to below 1 nm RMS. It is seen that the step bunching is related to the annealing temperature and time. Step bunching start appearing at 1650°C and beyond, but it did not appear when annealed at 1600°C.

5.1.3 Effects on 4H-SiC MOSFET Channel Mobility

In the practical vertical power MOSFETs, ion implantation is used to from the n-type source region, as well as the P-type body. Post implantation annealing at high temperature (>1600°C) is then required to electrically activate the implanted species. Under these extreme thermal conditions the morphology of the surface where the inversion channel is formed can be severely degraded as shown by the step bunching illustrated in previous Section. Therefore, carbon capping layer was used to protect the surface during the post-implantation annealing. However, whether this carbon-based capping layer would benefit the electrical performance of the MOSFET is still under debate. While Haney et al. [128] observed that the annealing temperature between $1200-1800$°C with a graphite cap do not have significant impact on the channel mobility, Naik et al. [129] reported that the use of a carbon capping layer can lead to a lower channel mobility. Frazzetto et al. [130] recently also showed that Al-implanted lateral 4H-SiC MOSFETs processed without a carbon capping layer during post-implantation annealing at 1650°C have higher peak channel mobility (40 cm^2/V.s) than the devices fabricated using carbon capping layer (24 cm^2/V.s). Figure 5.9 shows the results from the literature [130] of field effect mobility versus gate bias for lateral 4H-SiC MOSFET annealed at 1650°C with and without carbon capping layer.

Similar experiments were carried out in this work to examine this peculiar behaviour of the channel mobility on lateral MOSFETs. Two 4H-SiC lateral MOSFETs (0001 face)

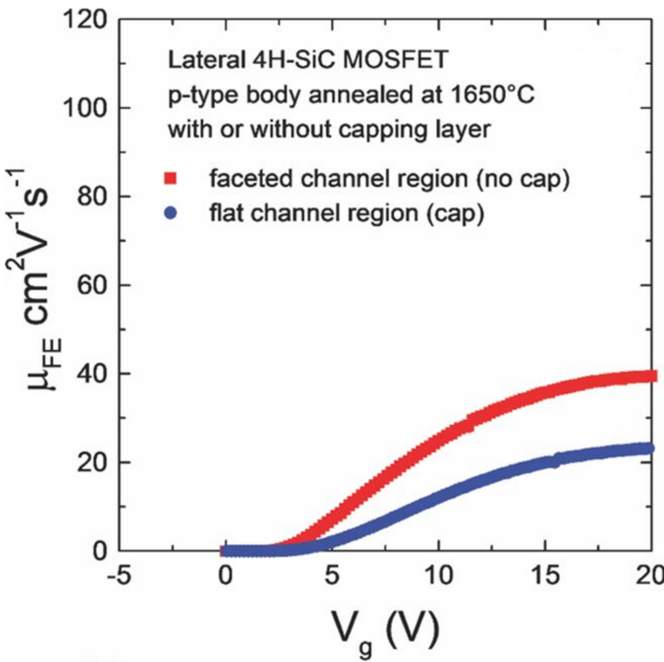


Figure 5.9: Field effect mobility versus gate bias for lateral 4H-SiC MOSFETs with and without carbon capping layer [130].

were fabricated using Al implanted p-body with doping concentration of $1{\times}10^{18}$ cm^{-3} and N implanted source region with doping concentration of $5{\times}10^{18}$ cm^{-3}, with gate oxide thickness of 50 nm by dry thermal oxidation at 1400°C for 1 hour. Details of the MOSFETs structure and the fabrication process are discussed in Chapter 7. Post-implantation annealing was performed for both samples at 1650°C for 1 hour with one sample protected with carbon capping layer. Results of field effect mobility versus gate bias are shown in Figure 5.10.

From fabricated 4H-SiC lateral MOSFET results here at Warwick as shown in Figure 5.10, it is seen that there is not much difference in the peak field effect mobility between the lateral MOSFETs fabricated with and without the carbon capping layer. The field

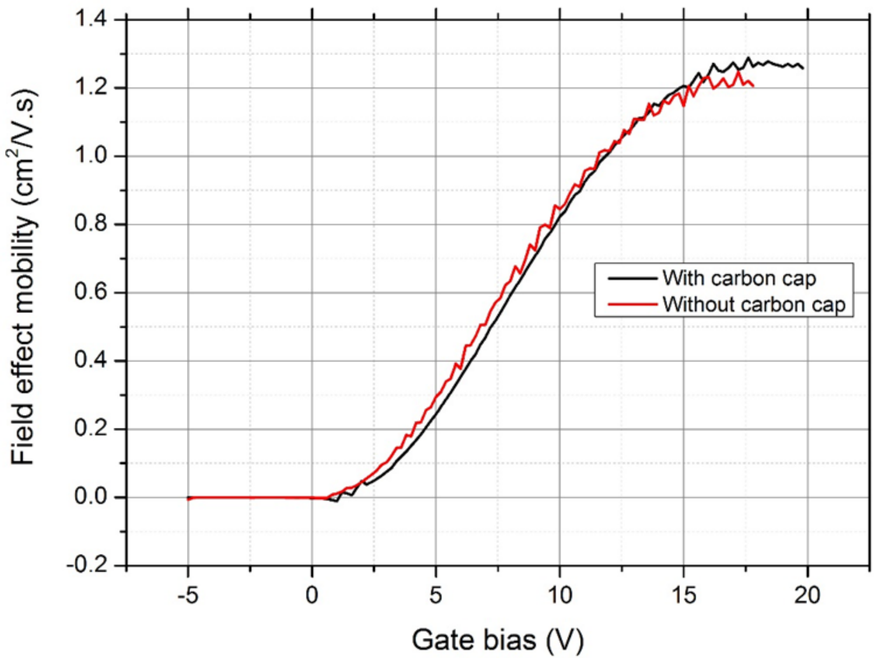


Figure 5.10: Field effect mobility versus gate bias for the fabricated 4H-SiC lateral MOSFETs with and without carbon capping layer.

effect mobility values for both samples are around 1.3 $cm^2/V.s$, which significantly lower than devices reported in the literature. The reason for such low mobility value is mainly due to the high defect density near the SiC/SiO_2 interface as discussed in Chapter 2. Because of such poor mobility values for both samples, it is difficult to tell whether the carbon capping layer has any impact on their electrical performance. Based on the current literature results and our fabrication result, it can be concluded that the use of carbon capping layer could either reduce the channel mobility or have no impact the electric performance on 4H-SiC MOSFETs, but it certainly will not improve the electric performance of devices.

5.2 Ion Implantation and Activation

As discussed in Section 5.1, because of the strong chemical bonding in SiC, the thermal diffusion which is typically used for selective doping of silicon devices cannot be simply applied to the fabrication of 4H-SiC devices. This is due to the low diffusion coefficients of the main dopant species that are required for the fabrication of 4H-SiC devices. As such, ion implantation is the only practical way of achieving the selective doping of 4H-SiC devices.

The implanted dopants species have a shorter projected range in 4H-SiC compared to dopant in Si. This means higher implant energies (in the range of keV to MeV) are required to achieve a junction depths up to 1 μm. For the doping of p-type 4H-SiC, aluminium (Al) and boron (B) are the most commonly used implanted species. Although boron is the preferred option for forming deeper junctions because of its lower atomic mass, it has suffered from strong out-diffusion after post-implantation annealing if surface was not protected by capping layer which has been observed by several authors [119–121]. On average, boron has projected range of 0.6 μm at an implant energy of 360 keV and 0.4 μm for aluminium. Although aluminium has smaller junction depth compare to boron, it has the advantage of having a shallower ionisation energy with respect to the edge of the valence band in 4H-SiC (200 meV for aluminium compared to 330 meV for boron [131]), which means that lower sheet resistances are achievable with aluminium doped 4H-SiC compare to boron doped 4H-SiC because of the larger p-type carrier concentration in the

freeze-out temperature region.

For the n-type 4H-SiC, the common implanted species are nitrogen (N) and phosphorous (P). At an implant energy of 360 keV, these dopant species have projected ranges of 0.5 μm and 0.3 μm respectively, making nitrogen more suitable when deep junctions are required because of its lower atomic mass. Phosphorous, however is approximately an order of magnitude lower in sheet resistance than that which is achieved for nitrogen implants. This is because of its high electrical activation rate even at low annealing temperature (1300°C) as reported in [87, 132].

Ion implantation allows accurate control of the charge introduced into the semiconductor material. However, the implantation process will cause damage to the crystal structure of the semiconductor, with C and Si atoms being knocked out of their lattice positions, ending up on interstitial lattice sites. Higher implantation energies will cause greater damage to both the semiconductor surface and lattice, and also creates defects in the implanted regions of the semiconductor [88], which will affect the device performance.

It is found that only a small proportion of implanted ions will end up on substitutional lattices sites where they are electrically active, with a high proportion of dopant atoms residing on interstitial sites thus being electrically inactive [133]. To activate these dopants atoms as well as to repair the damage to the crystal lattice, a high temperature thermal annealing is required as discussed earlier in this chapter. For n-type dopants activation the anneal temperature of around 1300°C is usually required, whilst for p-type dopant activation the anneal temperature are significantly higher, being found to be around

1500°C and 1700°C for aluminium and boron respectively [89].

In order to investigate the effect of difference post-implantation annealing temperature on our MOSFETs, two lateral MOSFETs were fabricated with post-implantation annealing temperature of 1650°C for 1 hour and 1600°C for 45 minutes respectively. Details of MOSFETs fabrication process and implantation profiles are discussed in Chapter 7. It is seen from Figure 5.11 that the channel mobility values of both samples are almost the same at about 1.2 $cm^2/V.s$, this indicates that the post-implantation annealing temperature of 1600°C for 45 minutes is sufficient for activating both n-type and p-type dopants of our MOSFETs in this case. Therefore, for the 4H-SiC devices fabricated in this work, post-implantation annealing temperature at 1600°C for 45 minutes was used to activate all implants dopants.

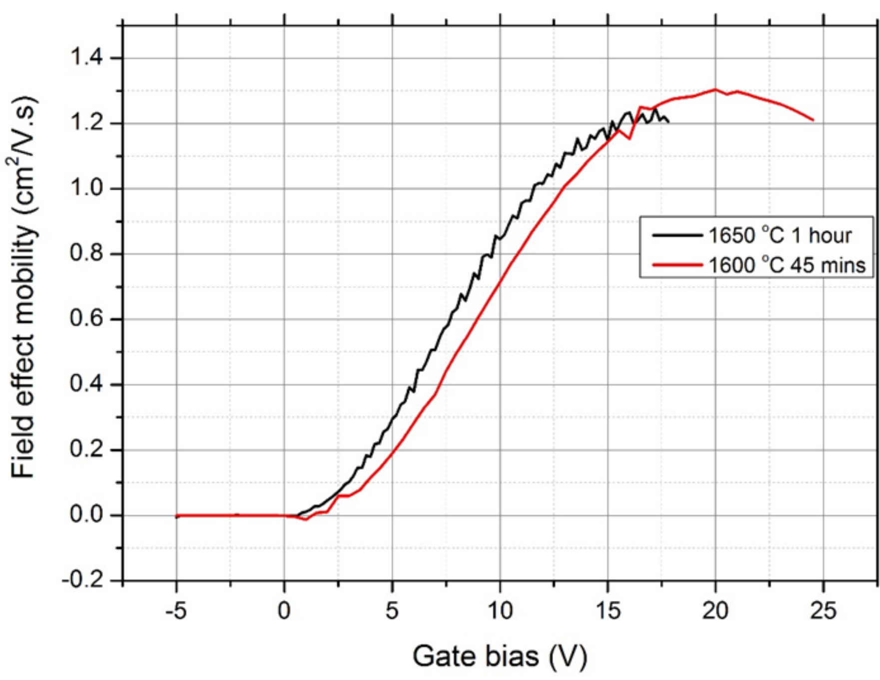


Figure 5.11: Field effect mobility as a function of the gate bias for the fabricated 4H-SiC lateral MOSFETs at different post-implantation annealing temperature of 1650°C for 1 hour and 1600°C for 45 minutes.

5.3 Ohmic contact Study for 4H-SiC

A good ohmic contact to 4H-SiC is important if low on-state power losses are to be realised for 4H-SiC devices. As discussed in Chapter 2, it is difficult to form a reliable and low resistance ohmic contacts to 4H-SiC, particularly for p-type 4H-SiC because of the poor dopant activation and ionisation. Therefore, a process has been optimised to achieve low specific contact resistivity for both n-type and p-type implanted 4H-SiC material. In this work, metal deposition for ohmic contacts has been achieved using an Electron Beam Evaporator Deposition system. Annealing of contacts has been performed using a rapid thermal anneal (RTA) furnace in argon filled environment, and the electrical performance

of these contacts has been measured using the TLM technique discussed in Chapter 4.

5.3.1 Fabrication Process for TLM Structures

The dimensions of the TLM structure fabricated in this work are illustrated in Figure 5.12. The first step of processing the TLM structures is the cleaning of the 4H-SiC samples

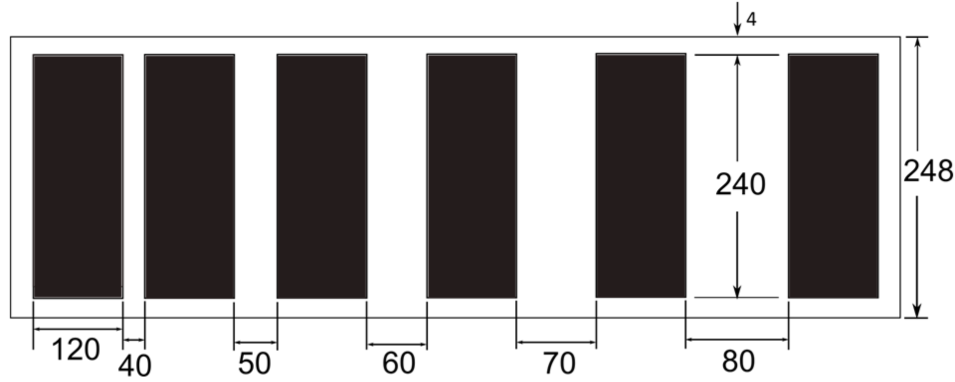


Figure 5.12: Fabricated 4H-SiC TLM structures (all dimensions are in μm).

using standard organic and Radio Corporation of America (RCA) cleans as outlined in Appendix B. Then one micron of tetraethyl orthosilicate (TEOS) SiO_2 was deposited to serve as the etching mask layer using the low pressure chemical vapour deposition (LPCVD) system as shown in Figure 5.13. The TLM features were defined using the photolithography process of negative photoresist as described in Appendix C, and a Karl Suss MJB3 photo-mask aligner was used as shown in Figure 5.14. The TEOS SiO_2 was then etched using the reactive-ion etching (RIE) process (CF_4/O_2 based) from the ICP etcher to open up windows for TLM features. After that the photoresist was removed in O_2 plasma, the exposed SiC was then etched to a depth of about 500 nm using the 50

Figure 5.13: LPCVD system (Thermco Systems^{TM}) used to deposit SiO_2 on SiC.

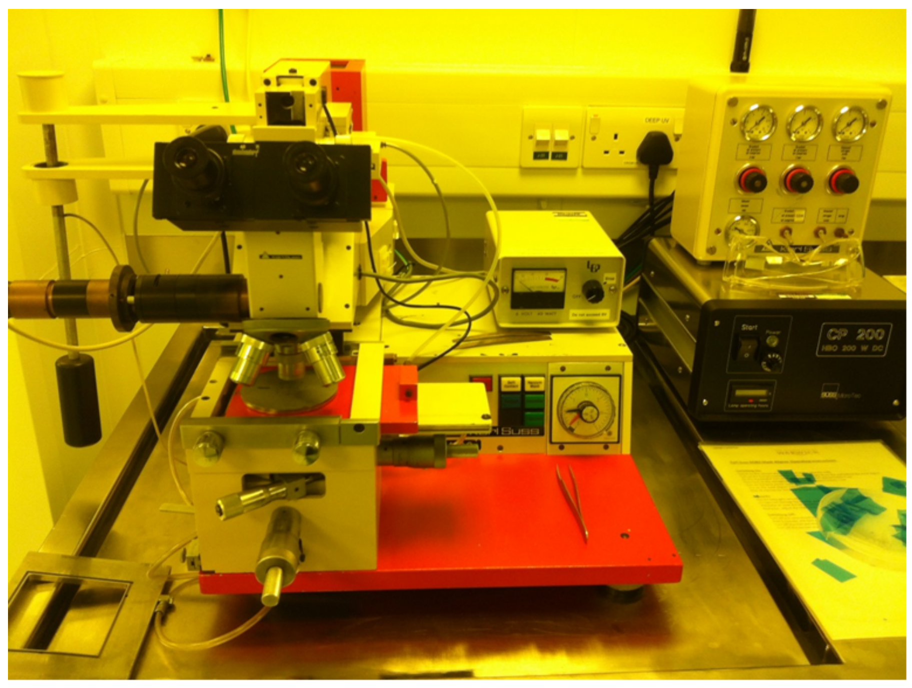


Figure 5.14: Karl Suss MJB3 photo-mask aligner.

SCCM SF_6 + 3 SCCM O_2 1000 W ICP program. Once the TLM structures had been defined, the TEOS SiO2 mask was removed in hydrofluoric acid (HF). A second layer of TEOS SiO_2 was then deposit with thickness of one micron and again use the standard photolithography process of negative photoresist to define the TLM contact pad regions. The TEOS SiO_2 was then etched away through to the SiC surface using RIE etching and 10:1 buffered oxide etch (BOE) was used to remove the remaining SiO_2 and to create a small undercut, which facilitates easier lift-off for the subsequent metallisation process. After rinsing in DI water, samples were deposited with titanium and nickel of 30 nm and 100 nm respectively at a base pressure of 2×10^{-7} Torr using the Electron Beam Evaporator Deposition system as shown in Figure 5.15, and lift-off the unwanted metals and photoresist in acetone using an ultrasonic bath. Finally, the samples were annealed in the Rapid Thermal Annealing (RTA) furnace as shown Figure 5.16 at 1000°C for 2 minutes to form an ohmic contact. Table 5.2 shows the TLM fabrication process flow with two-dimensional cross-sectional diagram and process description of each step.

Figure 5.15: Electron Beam Evaporator Deposition system.

Figure 5.16: Rapid Thermal Annealing (RTA) furnace in the clean room.

Table 5.2: 4H-SiC TLM fabrication process flow.

Cross-sectional diagram	**Fabrication process**
i. TEOS SiC	Deposit 1 μm TEOS SiO_2 as TLM isolation etch mask.(Cleaning before TEOS deposition)
ii. Photoresist TEOS SiC	Deposita layer of photoresist on top of TEOS SiO_2.
iii. PR TEOS SiC	Photolithography to open the window for TEOS SiO_2 and SiC etching.
iv. PR TEOS SiC	1. RIE etching for TEOS SiO_2. 2. Remove photoresist. 3. ICP etching for exposed SiC to a depth of 500 nm.

Continued on next page

Table 5.2 – continued from previous page

Cross-sectional diagram	Fabrication process
v. SiC	Remaining TEOS SiO_2 removed in HF.
vi. TEOS SiC	Deposit 1 μm TEOS SiO_2 layer.
vii. Photoresist TEOS SiC	Deposit photoresist on top of TEOS SiO_2.
viii. TEOS SiC	1. Photolithography to open metal contact windows. 2. RIE etch TEOS SiO_2 and then BOE to finish off
ix. Metal SiC	Metal deposition with Ti/Al 30/100 nm.
	Continued on next page

Table 5.2 – continued from previous page

Cross-sectional diagram	Fabrication process
x. Metal / SiC	1. Metal lift off in acetone. 2. RTA anneal at 1000°C for 2 mintues.
xi. Al / Ti/Ni / SiC	1. Pattern with gate metal mask and deposit Al of 1 μm and lift off in acetone. 2. RTA anneal at 1000°C for 2 mintues.

5.3.2 Electrical Characterisation Results

To electrically characterise the metal-semiconductor contacts described in this chapter, an Agilent Technology B1500A Semiconductor Parameter Analyser has been used with four probes measurement, all measurement are taken under dark conditions at room temperature. The metal scheme that was investigated was Ti/Ni, with corresponding thickness of 30/100 nm. It then went through a RTA annealing at 1000°C for 2 minutes to form an ohmic contact on both n-type and p-type 4H-SiC. The use of nickel (Ni) based alloys for the n-type SiC contact metal has been widely studied [89–91], and the

typical specific contact resistances to n-type 4H-SiC is in the order of $10^{-6}\ \Omega \cdot cm^2$ as discussed in Chapter 2. Although it is more difficult to form the ohmic contact on p-type 4H-SiC, the Ti/Ni metal scheme with RTA annealing at 1000°C for 2 minutes still shows acceptable specific contact resistances in the order of $10^{-3}\ \Omega \cdot cm^2$. And because in this work we are focusing on fabricating 4H-SiC power MOSFETs, it is more important to have a good ohmic contact on n-type 4H-SiC which is for the source and drain contacts. The p-type ohmic contact in the 4H-SiC power MOSFET is used to short-circuiting the N+ source and P+ region in order to suppress the parasitic N+/P/N bipolar transistor when MOSFET is under blocking mode.

Figure 5.17 shows the I-V characteristics of unannealed Ti/Ni ohmic contact scheme on n-type 4H-SiC material, and Figure 5.18 shows the I-V characterises of Ti/Ni ohmic contact scheme annealed at 1000°C for 2 minutes on n-type 4H-SiC material with nitrogen doping concentration of 1×10^{20} cm^{-3}. It is seen that without the annealing the TLM structures had a rectifying I-V characteristics and the ohmic behaviour was achieved using an annealing temperature of 1000°C for 2 minutes. The specific contact resistivity of the n-type 4H-SiC using this metal contact scheme after annealing is about $3\times10^{-5}\ \Omega \cdot cm^2$.

The surface morphology of the TLM structures were observed before and after the annealing in the RTA furnace using the optical microscope as shown in Figure 5.19. It is seen that before the annealing the metal looks shiny and silver coloured, which was expected. However, after the annealing the metal surfaces became rough and looks brown colour as shown in Figure 5.19(b). This indicates that the annealing process has had a

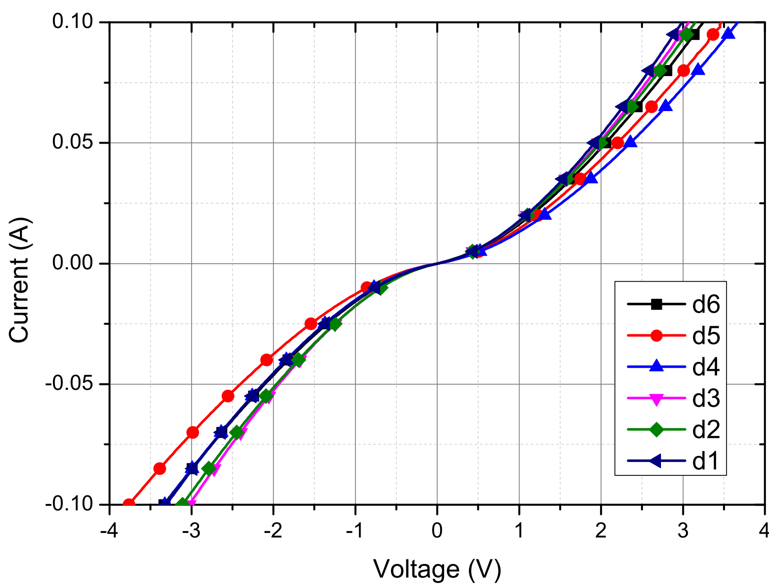


Figure 5.17: Rectifying I-V characteristics of unannealed Ti/Ni ohmic contact scheme on n-type 4H-SiC (d1 to d6 refer to contact spacings as shown in Figure 5.12).

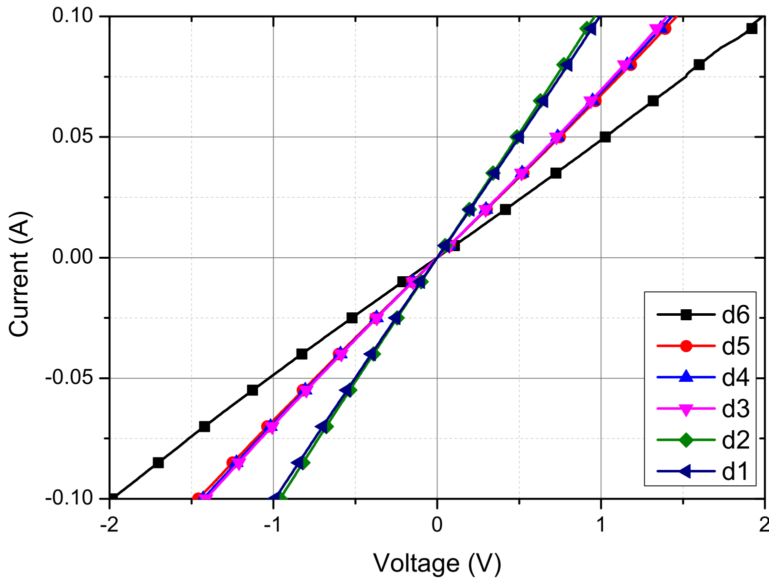
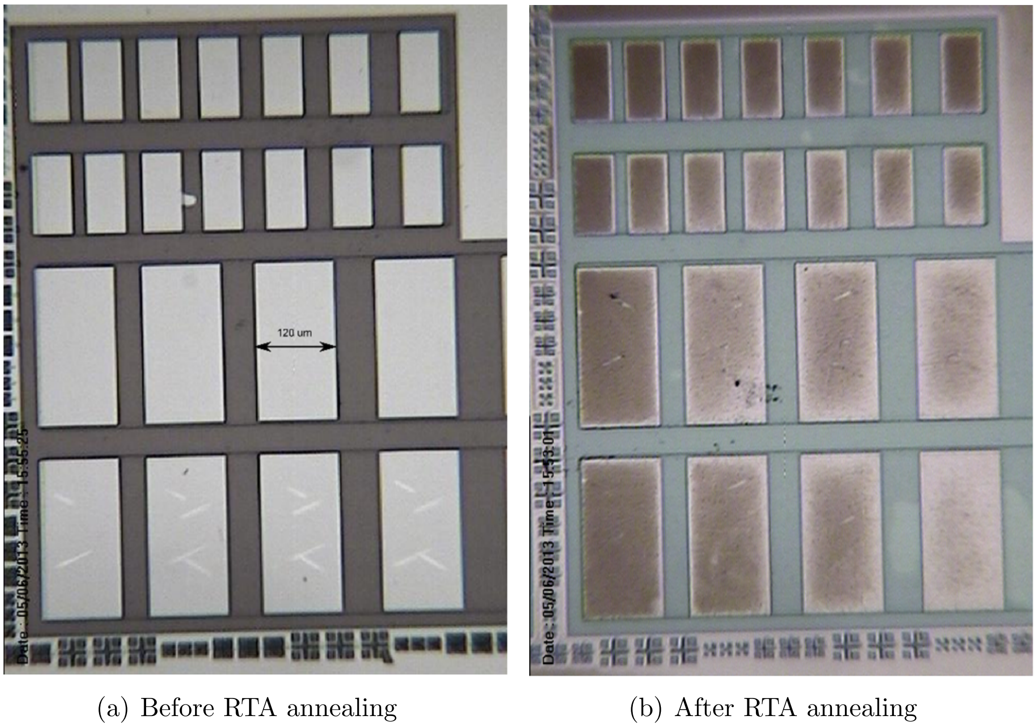


Figure 5.18: I-V characteristics of annealed Ti/Ni ohmic contact scheme (1000°C for 2 minutes) on n-type 4H-SiC (d1 to d6 refer to contact spacings as shown in Figure 5.12).

significant effect on the structures and composition of the metal scheme. It is found by authors [13, 134] that the Ti layers might reduce or prevent the formation of unreacted C atoms by forming the Ti_3SiC_2 compounds at the metal/SiC interface after reaction between the contact materials and SiC. This formation of Ti_3SiC_2 corresponds to a lower specific contact resistance.



(a) Before RTA annealing

(b) After RTA annealing

Figure 5.19: Surface morphology of TLM structures on n-type 4H-SiC with Ti/Ni metal scheme.

Ohmic contact on p+ 4H-SiC with aluminium doping concentration of $2{\times}10^{19}$ cm^{-3} has also been investigated using the same Ti/Ni contact scheme. It is found that using the same Ti/Ni contact scheme the TLM structures still has ohmic behaviour with the specific contact resistivity of about $6{\times}10^{-3}\ \Omega \cdot \mathrm{cm}^2$. Although this value is higher than

most of the results reported in literature [13, 134–136] which are in the order of 10^{-4} to 10^{-5} $\Omega \cdot \text{cm}^2$, the result is still acceptable for the purpose of this work because it is the ohmic contact on the n-type 4H-SiC which we are concerning as it will have impact on the on-state performance of the 4H-SiC power MOSFETs.

5.4 Summary

In this Chapter, the development of the fabrication processes required for realising high voltage 4H-SiC MOSFET has been presented. The key processes are the fabrication of carbon capping layer, post-implant activation annealing and ohmic contact on 4H-SiC. The oxidation and the post oxidation annealing process are discussed in Chapter 7. The investigation into the use of the capping layer to suppress the step bunching on 4H-SiC due to high temperature post implantation annealing was first discussed. Among all other capping layer techniques (such as using AlN or thermally grown silicon oxide) the carbon capping layer is the cheapest and easiest to fabricate and can cover the mesa-etched SiC sidewalls without any difficulty. The fabrication process of the carbon capping layer were discussed, followed by the surface roughness measurement using the atomic force microscopy (AFM) to examine the surface roughness for both with and without carbon capping layer samples after post-implantation annealing. It can be concluded that carbon capping layer can effectively protects SiC surface from step bunching and limit the surface roughness to blow 1 nm RMS. Step bunching is found at 1650°C annealing

temperature for 1 hour and beyond, but it did not appear when annealed at 1600°C for 45 minutes. Although the carbon capping layer can suppress the step bunching during the post-implantation annealing, it has no significant impact on the channel mobility of the MOSFET as shown by our fabricated MOSFETs result.

Next, a study into the ion implantation and activation on 4H-SiC was presented. Results show that there is no significant difference in terms of channel mobility of 4H-SiC lateral MOSFETs between the post-implantation annealing at 1650°C for 1 hour and 1600°C for 45 minutes. This suggest that the annealing temperature of 1600°C for 45 minutes is sufficient for activating both n-type and p-type dopants in the 4H-SiC MOSFETs in this case.

Finally, TLM structure were fabricated and characterised to determine the ohmic contacts to both p-type and n-type 4H-SiC. The fabrication process of the TLM structures was first outlined, along with the geometrical details of the TLM structures. The electrical characterisation results of the fabricated TLM structures were presented next. The I-V characteristics of the n-type 4H-SiC TLM structures show that the unannealed Ti/Ni contact scheme suffered from rectifying behaviour. By annealing the sample at 1000°C for 2 minutes, ohmic behaviour was observed with a specific contact resistivity of around $3\times10^{-5}\ \Omega\cdot\text{cm}^2$. The surface morphology of the TLM structures were also observed before and after the annealing in the RTA furnace using the optical microscope. It is seen that before the annealing the metal looks shiny and silver colour. However, after the annealing the metal surfaces became rough and looks brown colour, which indicates

that the annealing process has had a significant effect on the structures and composition of the metal scheme and the formation of Ti_3SiC_2 after the annealing corresponds to a lower specific contact resistance as reported by some authors [13, 134].

Chapter 6

Fabrication and Characterisation of 4H-SiC MOS capacitors and Schottky diodes

In this Chapter, the fabrication and characterisation of 4H-SiC MOS capacitors and Schottky diodes are presented. First, details of the fabrication process of MOS capacitors using N_2O and phosphorous passivation are presented. The C-V characterisation results for the MOS capacitors fabricated under different oxidation and passivation conditions are given. The interface traps density (D_{it}) were then extracted and compared using both Terman and High-Low C-V methods. Following this, the design and fabrication process of the Schottky diodes with various JTE structures are discussed. Reverse breakdown performance analysis on Schottky diodes with various JTE structures are presented.

6.1 4H-SiC MOS Capacitors Fabrication

The 4H-SiC material used for the fabrication of MOS capacitors were obtained from Norstel AB [137]. All materials were specified with micropipe density of less than 1 cm-2

with crystal orientation of (0001). Epitaxial layer with thickness of 10 μm were grown on 4° off-axis 4H-SiC substrate with doping concentration of 2×10^{16} cm^{-3}. These wafers were diced into 8mm $\times$ 8mm chips for subsequent processing. The MOS capacitors have circle shapes with diameters ranging from 1000 to 400 μm on the photomask design as shown in Figure 6.1.

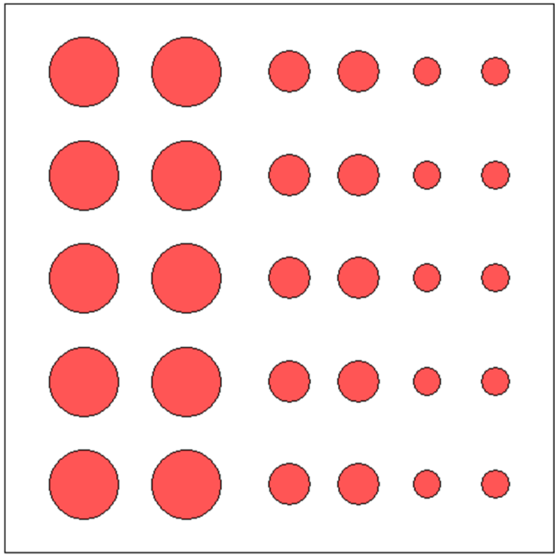


Figure 6.1: Photomask design for MOS capacitor fabrication with diameters of 1000, 600 and 400 μm.

Before fabrication of MOS capacitors, samples were cleaned using the standard organic, Piranha and Radio Corporation of America (RCA) cleaning processes, the details of which are described in Appendix B. Thermal oxidation of the samples was performed at 1400°C for 1 hour to give approximately 50 nm of oxide using the high temperature oxidation furnace in the clean room as shown in Figure 6.2. After the cleaning process outlined in Appendix B, SiC wafers are SiC wafers are immediately transferred to our

Figure 6.2: High temperature oxidation furnace in the clean room.

unique high temperature oxidation furnace for dry oxidation. Wafer are loaded at around 600°C with Argon gas flows and the temperature is raised to the oxidation temperature with ramping rate of 5°C per minute. Oxidation is then carried out with 20% oxygen in argon environment. The oxidation is followed by a one hour argon anneal or N_2O anneal. This post oxidation annealing is important for reducing the interface traps density between the SiO_2/SiC layers because it helps the out-diffusion of remaining carbon in the oxide. Different post oxidation anneal techniques have also found to be effective in reducing the interface state density as well as increasing the field effect mobility of SiC devices [16,53,138]. After the anneal, the temperature is ramped down at 5°C per minute in argon to 600°C. Figure 6.3 illustrates the standard thermal oxidation process used in

this work, which gives approximately 50 nm of oxide. Following this, the backside SiO_2

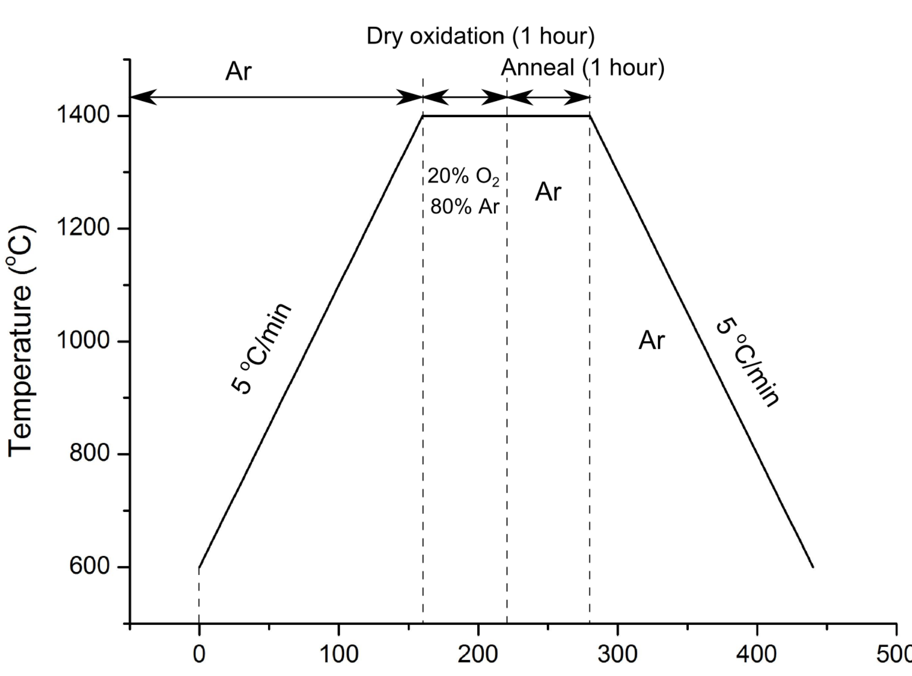


Figure 6.3: Standard thermal oxidation at 1400°C to grow ~ 50nm of SiO_2 on 4H-SiC.

was removed in the ICP etcher and the backside ohmic contact was formed by evaporating titanium and nickel of 30 nm and 100 nm and then annealed at 1000°C for 2 minutes using the rapid thermal annealing furnace (RTA) as discussed previously in Chapter 5.

The next process step was the metallisation of the top SiC surface. After carrying out a standard photolithography process using MJB3 photo-mask aligner, aluminium of 500 nm was evaporated onto the samples and the MOS capacitor structures were formed by lift-off process in acetone using the ultrasonic bath. Details of MOS capacitor fabrication process flow is illustrated in Table 6.1.

Table 6.1: : 4H-SiC MOS capacitor fabrication process flow.

Cross-sectional diagram	**Fabrication process**
i. SiO_2 / 4H-SiC	1. Clean sample using RCA solution. 2. Grow SiO_2 in the high temperature oxidation furnace.
ii. SiO_2 / 4H-SiC	1. Post oxidation anneal or passivate oxide in N_2O or phosphorous. 2. Remove the back oxide in the ICP etcher.
iii. SiO_2 / 4H-SiC / Ti/Ni ohmic contact	Deposite Ti/Ni of 30 nm/100nm and anneal at 1000°C for 2 minutes.
iv. PR / PR / SiO_2 / 4H-SiC / Ti/Ni ohmic contact	Photolithography to open windows for MOS capacitor structures.
	Continued on next page

Table 6.1 – continued from previous page

Cross-sectional diagram	Fabrication process
v.	Deposit Al of 500 nm on the top.
vi.	Lift off metal in acetone in ultrasonic bath.

6.1.1 N_2O Passivation and N_2O grown oxide

As discussed in previously in Chapter 2, the post oxidation annealing in N_2O after the oxide grown or the direct growth oxide under N_2O can effectively passivate the interface traps between the SiO_2/SiC interface. In this Section, the post oxidation annealing (or passivation) process on 4H-SiC MOS capacitors using N_2O ambient is discussed.

After thermally grown oxide in the high temperature oxidation furnace, 4H-SiC samples were then immediately loaded in the high temperature oxidation furnace again for

post oxidation annealing. Samples are loaded at around 600°C with argon gas flows at 5 L/min to prevent any oxygen flow in the furnace and the temperature is raised to the require annealing temperature (1200°C, 1300°C, 1400°C and 1500°C respectively) with a ramping rate of 5°C per minute. Annealing is then carried out in an 20% N_2O (1 L/min) and 80% Ar (4 L/min) environment for 30 minutes, 1 hour, 2 hours and 4 hours respectively. After the anneal, the temperature is ramped down at 5°C per minute in argon (5 L/min) to 600°C. Figure 7.3 illustrates the N_2O post oxidation annealing process at 1400°C for 1 hour used in this work.

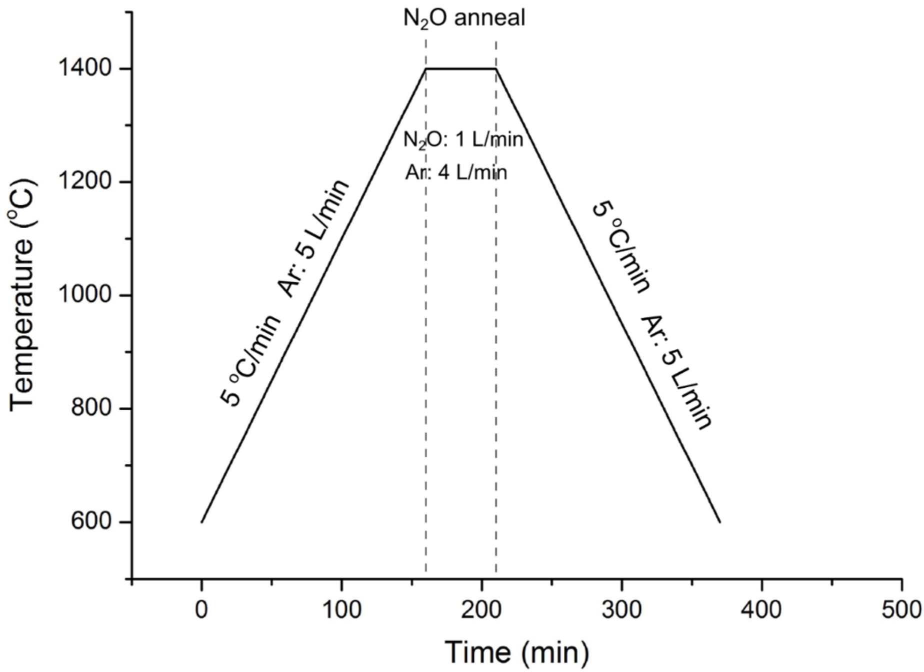


Figure 6.4: Example of N_2O post oxidation annealing process at 1400°C for 1 hour.

Oxide directly grown under N_2O environment have also been investigated as some literature have reported that the directly grown oxides in N_2O environment exhibit better

electrical properties compared to that of N_2O post oxidation treatment under identical time and temperature conditions [16, 85]. Directly grown oxide in N_2O environment at 1300°C and 1400°C have been carried out in this work using the high temperature oxidation furnace. The N_2O oxidation process and gas flow rate are the same as those used for N_2O post oxidation annealing as shown in Figure 7.3.

6.1.2 Phosphorous Passivation

Significant progress has been made with respect to interface passivation over the last decade, specifically with post oxidation annealing or direct growth in NO or N_2O environments, which provide a channel mobility of around $20 - 35$ cm^2/V.s for 4H-SiC (0001) MOSFET [50, 51, 54]. However, this value is still only 4% of the bulk mobility of 4H-SiC (∼800 − 100 cm^2/V.s) [139], and the channel resistance in state-of-the-art 4H-SiC power MOSFETs still contribute to about half the total conduction loss [140]. Some reports have indicated that phosphorous passivation is more effective than NO or N_2O passivation, providing peak mobilities of $80-90$ cm^2/V.s [53,141] and even up to 108 cm^2/V.s [69] for 4H-SiC MOSFETs fabricated on the conventional (0001) Si-face. The peak mobility can be even higher on the (1120) a-face of about 125 cm^2/V.s as reported in [52].

The phosphorous passivation used in this work is performed by using the solid SiP_2O_7 phosphorous planar diffusion source (PDS) provided by Saint-Gobain and annealed at 1000°C for 2 hours with nitrogen flows at 5 L/min. The furnace used for phosphorous

passivation is shown in Figure 6.5. Samples were annealed using the arrangement shown

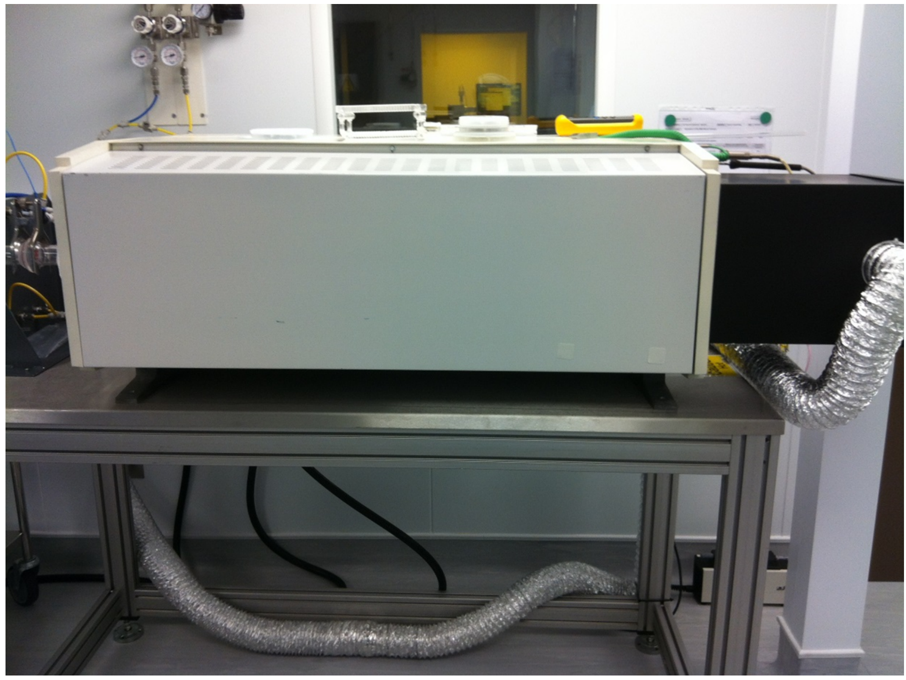


Figure 6.5: Annealing furnace use for phosphorous passivation.

in Figure 6.6 for a planar diffusion source (PDS) that decomposes to produce a P_2O_5 passivating ambient. Both phosphorous PDS and Si carrier wafer are vertically placed next to each other on a wafer carrier boat, samples are mounted on the Si carrier wafer by deposit photoresist and then baked at 200°C for 3 minutes.

The SiP_2O_7 PDS will decompose into SiO_2 and phosphorous pentoxide under high temperature as shown by the following reaction:

$$SiP_2O_7 + 1000°C \rightarrow SiO_2 + P_2O_5 \tag{6.1}$$

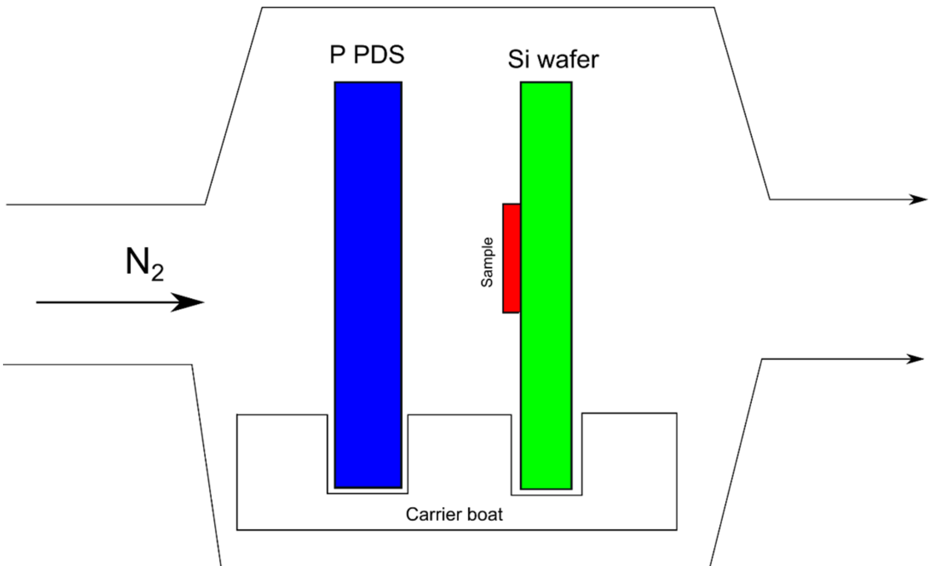


Figure 6.6: Schematic of process inside the PDS furnace.

After phosphorous passivation the oxide is no longer SiO_2 but is converted to phosphosilicate glass (PSG) which is a polar material as discussed in [53]. This PSG layer can passivate the interface traps between SiO_2 and 4H-SiC by suppressing the Coulomb scattering effect, which is the dominant carrier scattering mechanism for the MOSFETs without POA and with N_2O POA as discussed in Chapter 5.

6.1.3 Combined N_2O and Phosphorous Passivation

The combined N_2O and phosphorous passivation was also investigated in this work. After thermally grown oxide in the high temperature oxidation furnace, samples were then loaded in the high temperature oxidation furnace again for post oxidation annealing in N_2O at 1300C for 4 hours. Details for N_2O passivation process are discussed in Section

6.1.1. After the N_2O passivation, the samples were mounted on a Si carrier by spinning a layer of photoresist and baked at 200°C for 3 minutes. Following this, Si carrier was loaded in the annealing furnace for phosphorous passivation at 1000°C for 2 hours as discussed in previous section 6.1.2.

6.2 Interface Trap Density and Breakdown Characteristics

In this Section, the interface trap density of 4H-SiC MOS capacitors fabricated under different post oxidation conditions in this work have been extracted and compared. Both high frequency capacitance method and the combined high-low frequencies capacitance method have been used. The advantages and limitations of both C-V techniques have been looked at. The background theory of both C-V techniques were discussed in Chapter 4 of this thesis.

6.2.1 High Frequency Capacitance Method

The high frequency method (also called the Terman method) is one of the first methods for determining the interface trap density. This method uses only high frequency (1 MHz) C-V curve and compares it with the ideal C-V curve which is generated with knowledge of the oxide thickness, gate metal contact area and doping concentration of the drift region.

It is assumed that at high frequency the interface traps do not respond, however they do respond to the slowly varying dc gate bias. As the interface trap occupancy changes with gate bias, this will cause the high frequency C-V curve to stretch out along the gate voltage axis. Figure 6.7 shows the difference between the ideal C-V curve and the experimental C-V curve for the MOS capacitor fabricated at 1400°C for 1 hour without passivation, and Figure 6.8 shows the C-V curves for MOS capacitor fabricated with N_2O passivation at 1300°C for 4 hours. Note that the curve for the MOS capacitor with interface traps (experimental curve) has been translated to cross the ideal curve at zero gate bias.

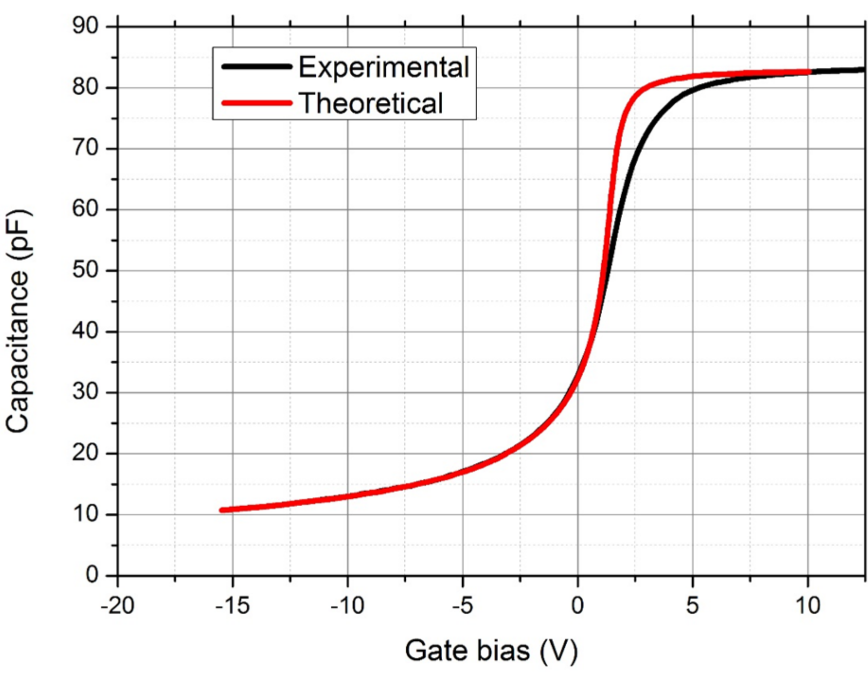


Figure 6.7: Theoretical and ideal C-V curves for the MOS capacitor fabricated at 1400°C for 1 hour (taken at 1 MHz).

From Figures 6.7 and 6.8, it is seen that the interface traps produce a distortion in

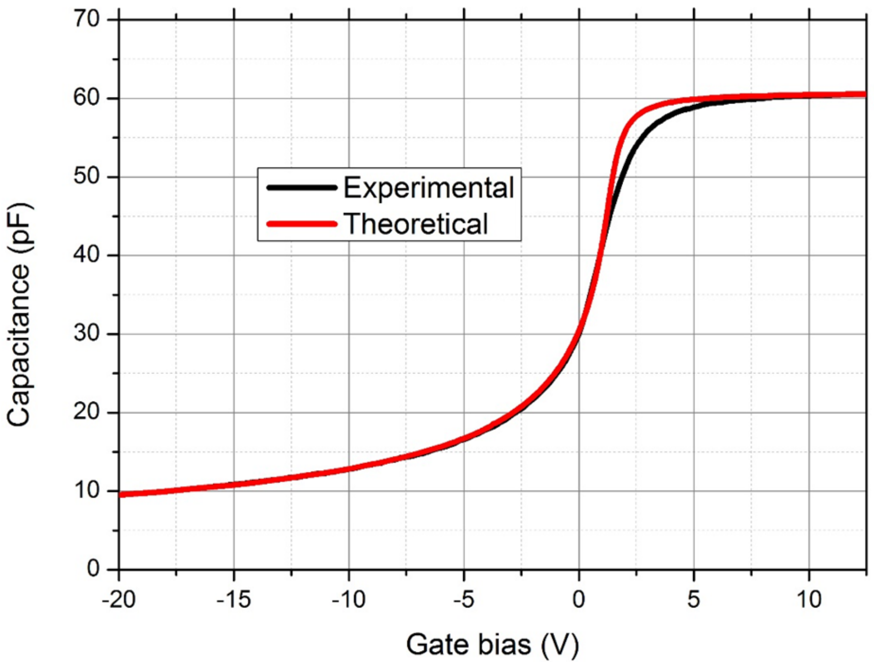


Figure 6.8: Theoretical and ideal C-V curves for the MOS capacitor fabricated with N_2O POA at 1300°C for 4 hours (taken at 1MHz).

the shape of the C-V curve. Higher interface trap density will have a larger distortion in the C-V curve. MOS capacitors fabricated with N_2O POA at 1300°C for 4 hours has less distortion compare with those fabricated without any POA at 1400°C for 1 hour. Figure 6.9 shows the interface trap density (D_{it}) extracted using the Terman method for MOS capacitors fabricated with different nitridation conditions.

Results from Figure 6.9 show that in general the samples with N_2O POA treatment have lower interface trap density than the one just oxidised at 1400°C for 1 hour without N_2O passivation. Increasing the N_2O POA temperature will reduce the interface trap density except for the N_2O POA at 1500°C, which has highest interface trap density of all samples as shown in Figure 6.9. This indicates that excess carbon atoms or carbon

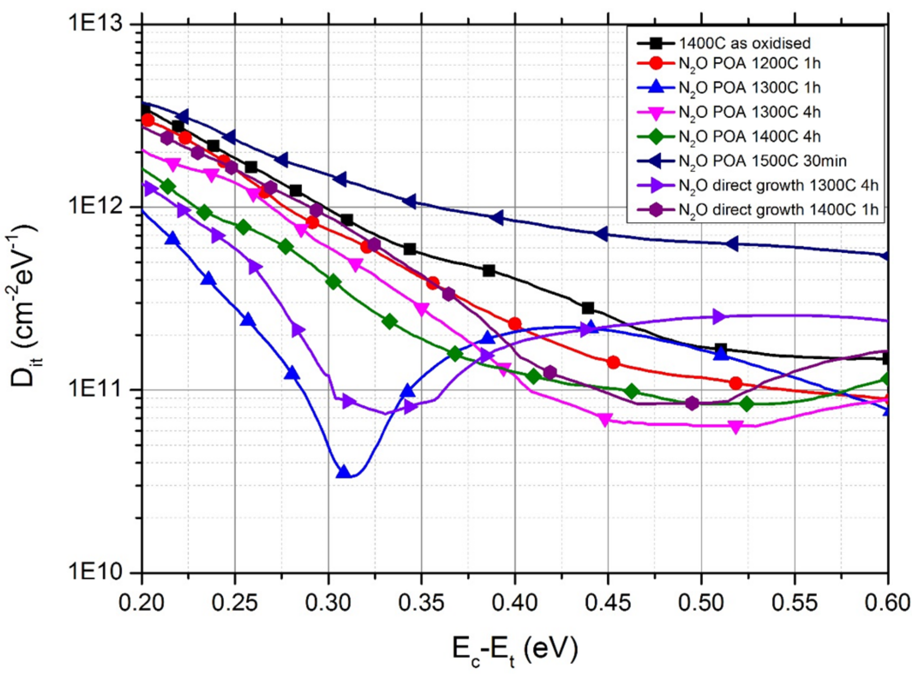


Figure 6.9: Interface trap densities extracted using Terman method for MOS capacitors fabricated with different nitridation conditions.

clusters could remain at or near the SiO_2-SiC interface after N_2O POA at 1500°C for 30 minutes as discussed in [16], which could be due to either the annealing time is too short for strong Si $\equiv$ N bonds to form and passivate the excess interface traps, or the oxidation is so fast that there is a lot more carbon released during the thermal oxidation than the removal of carbon and associated complex silicon oxycarbon bonds [16]. For the samples with directly grown oxide in N_2O, it is seen that for the same nitridation condition of 1300°C for 4 hours, the sample with directly grown oxide in N_2O has lower D_{it} than the sample with N_2O POA. This interesting finding has been reported by others in [16, 85] where the directly grown oxides in nitrogen rich environment exhibit better electrical properties compared to their counterparts post oxidation anneal in the same

gas. The sample with N_2O directly grown oxide at 1400°C for 1 hours, however, did not show further decrease of D_{it} but rather have D_{it} similar to those with N_2O POA at 1200°C for 1 hour. Therefore, the optimum temperature for N_2O direct grown oxide to give lowest value of D_{it} is at 1300°C.

From Figure 6.9 it is seen that some of the D_{it} curves are not smooth straight lines but with dip in the middle. This is caused by the noise from the C-V measurement and this noise will increase after the differentiation for the surface potential when calculating the D_{it} using the Terman method as discussed in Chapter 4. Therefore, filtering and smoothing data may be required when using Terman method to extract the interface trap density if original C-V data is noisy.

Other MOS capacitors with phosphorous POA has also been investigated and compared with the N_2O POA samples. Figure 6.10 shows the difference between the ideal C-V curve and the experimental C-V curve for the MOS capacitor fabricated with phosphorous passivation at 1000°C for 2 hours. It is seen that the difference between the ideal C-V curve and the experimental C-V are much smaller than the previous just oxidised without POA and the N_2O POA samples as shown in Figures 6.7 and 6.8. This indicates that the phosphorous POA sample has the lowest interface trap density of all MOS capacitors fabricated in this work. Figure 6.11 shows the interface trap density extracted using Terman method for MOS capacitors fabricated with N_2O POA, phosphorous POA and the combined N_2O and phosphorous POA.

From Figure 6.11 it is seen that the MOS capacitor sample with phosphorous POA

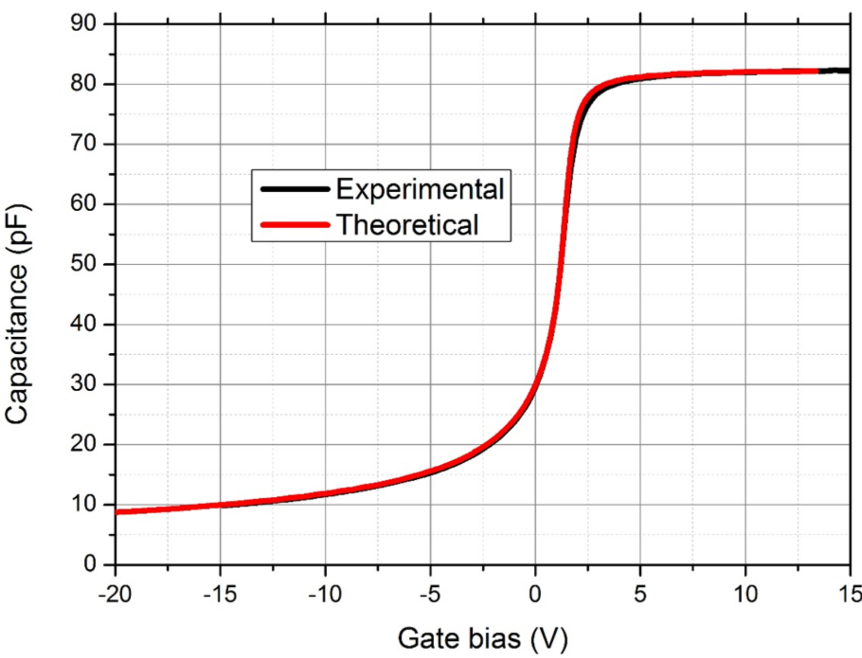


Figure 6.10: Theoretical and ideal C-V curves for the MOS capacitor fabricated with phosphorous POA at 1000°C for 2 hours.

has the lowest D_{it} compare with other MOS capacitors fabricated using different POA conditions, which is about 5×10^{11} cm^{-2}eV^{-1} at 0.2 eV away from the conduction band edge. The MOS capacitor fabricated with N_2O POA has D_{it} of about 1×10^{12} cm^{-2}eV^{-1}, which higher than the phosphorous POA sample but still lower than the sample just oxidised at 1400°C for 1 hour without any POA treatment which is about 5×10^{12} cm^{-2}eV^{-1} at 0.2 eV. Results also shown that using the combined N_2O and phosphorous POA will not further reduce the D_{it}, but rather the D_{it} is limited to the range similar to that of using N_2O POA.

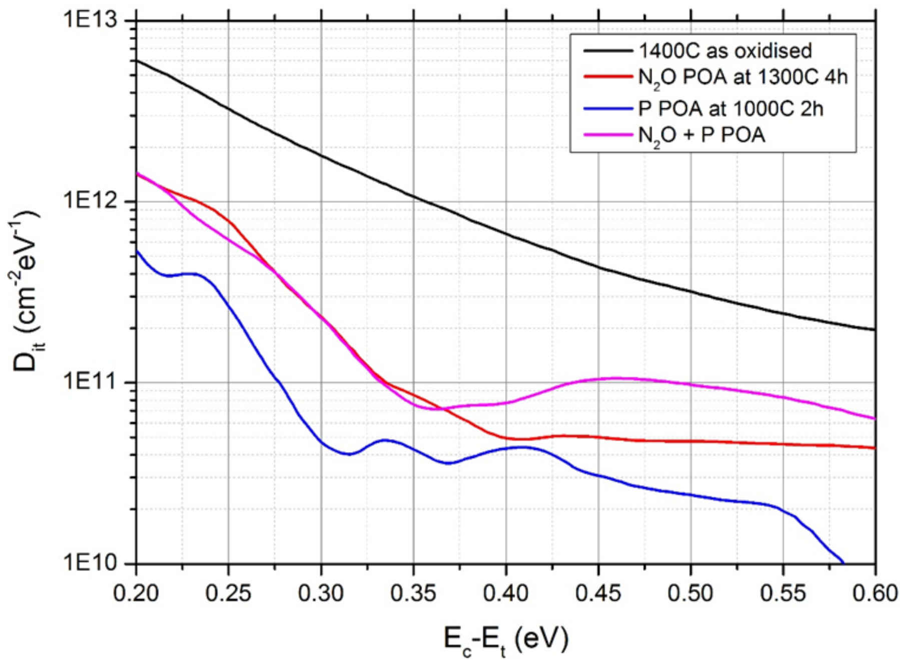


Figure 6.11: Interface trap density extracted using Terman method for MOS capacitors fabricated with N_2O POA, phosphorous POA and combined N_2O and phosphorous POA.

6.2.2 Combined High-Low Frequency Capacitance Method

Another way to extract the interface trap density (D_{it}) is called the combined high-low frequency capacitance method, which uses two different frequencies: one frequency low enough that so that all the interface traps can respond to the signal and one high enough so that all the traps at the given surface potential cannot respond to the signal. In this work, 200 Hz and 1 MHz are chosen for the high-low frequencies measurement. The equation to extract the D_{it} using high-low frequency capacitance method is discussed in Chapter 4. The high-low frequency capacitance method is the most widely used method for D_{it} extraction in the literature because of its simplicity. Although this method may potentially underestimate the D_{it} value [49], it was used in this work as a benchmark to

compare with the D_{it} results generated from Terman method and those from the literature.

Figures 6.12 and 6.13 show the high and low frequencies C-V curves for MOS capacitor fabricated at 1400°C oxidation for 1 hour without POA and N_2O POA at 1300°C 4 hours respectively. It is seen that there is slight distortion of the low frequency C-V

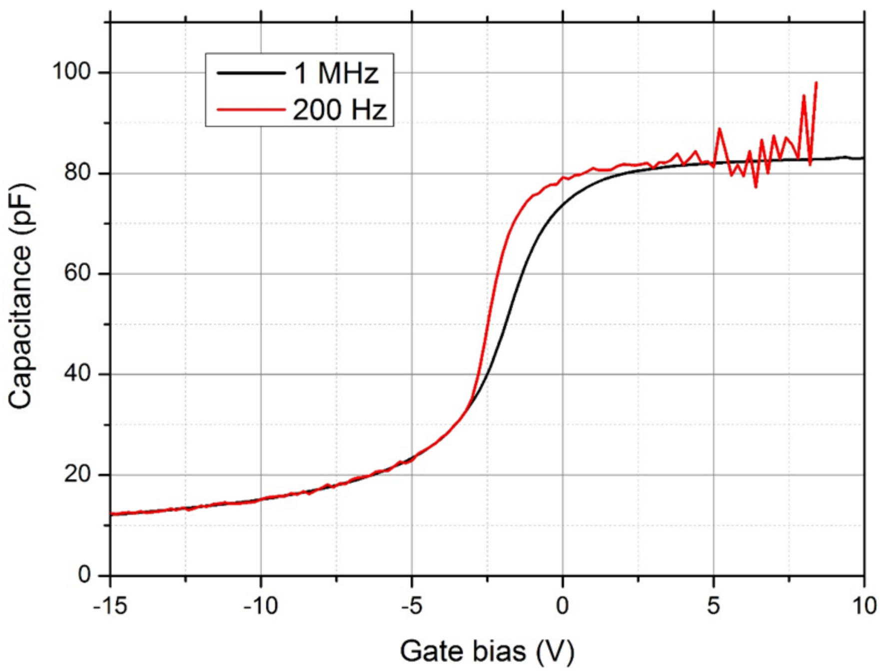


Figure 6.12: High-low frequencies capacitance measurement for MOS capacitor fabricated at 1400°C oxidation for 1 hour without POA.

curve compare to the high frequency C-V curve due to the interface traps respond to low frequency signal. MOS capacitor fabricated using N_2O POA at 1300°C for 4 hours show less distortion to the high frequency C-V curve compare to that of fabricated at 1400°C oxidation for 1 hour without POA. This indicates that MOS capacitors fabricated with N_2O POA will give lower D_{it} than those fabricated without POA, similar to the results

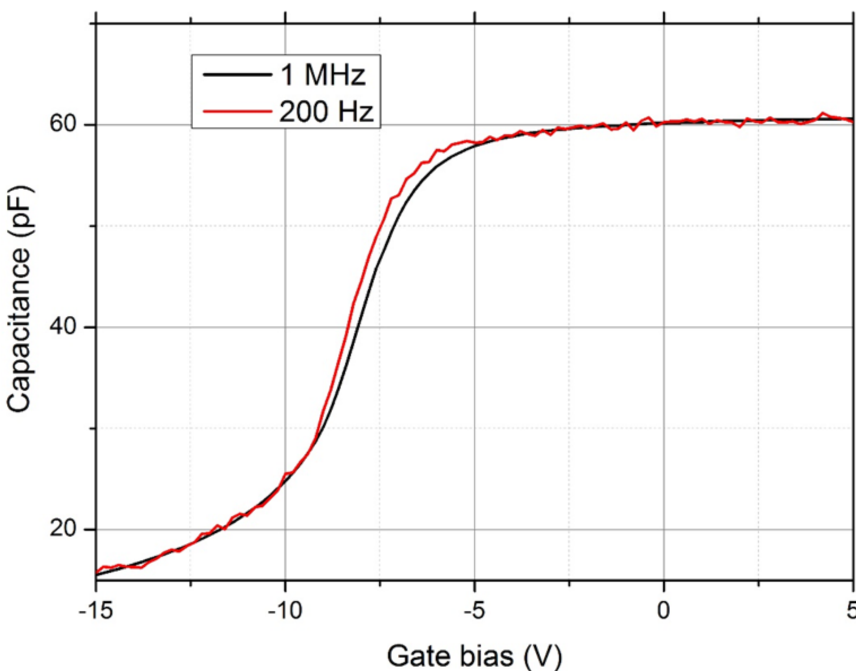


Figure 6.13: High-low frequencies capacitance measurement for MOS capacitor fabricated with N_2O POA at 1300°C for 4 hours.

found by using Terman method as discussed in previous section. Figure 6.14 shows the interface trap densities of MOS capacitors fabricated at various N_2O POA temperatures and time using the high-low frequency capacitance method.

From Figure 6.14 it is seen that the MOS capacitors fabricated with N_2O POA treatment all have lower interface trap density than the one fabricated at 1400°C oxidation temperature for 1 hour without POA. In general, increase the N_2O POA temperature will reduce the interface trap density except that for the N_2O POA at 1500°C, which is about 5×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV higher than the D_{it} obtained from N_2O POA at 1300°C and 1400°C. N_2O POA time does not seem to have significantly impact on the reduction of D_{it}. Unlike the results shown by using the Terman method, the D_{it} difference between the

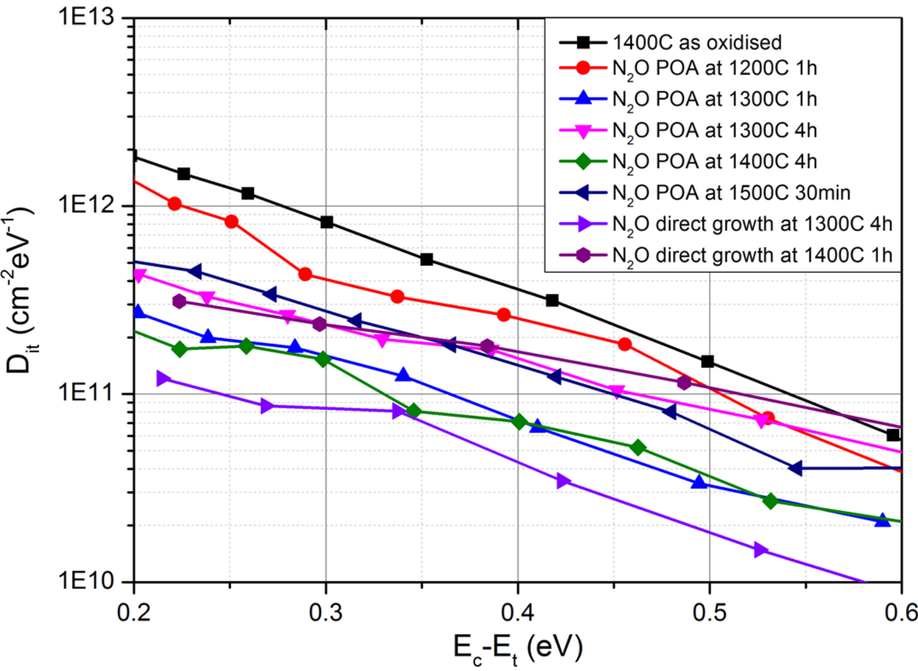


Figure 6.14: Interface trap densities extracted using high-low frequency capacitance method for MOS capacitors fabricated at various N_2O POA temperatures and time.

N_2O POA at 1300°C for 1 hour and N_2O POA at 1300°C for 4 hours is relatively small by using the high-low frequency capacitance method as shown in Figure 6.14. The lowest D_{it} is given by the MOS capacitor fabricated with N_2O direct growth oxide at 1300°C for 4 hour, which is about 1×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV from the conduction band edge. Similar to the results obtained from Terman method, the sample with directly grown oxide in N_2O has lower D_{it} than the sample with N_2O POA for the same temperature and time. By comparing the results obtained from both Terman and high-low C-V methods, it is observed that nitridation at temperature of 1300°C 4 hours (both direct growth oxide and POA) in general has the best results for lowering the D_{it}. Although nitridation at 1400°C will produce lower D_{it} in some cases, the results are inconsistent between samples

and more importantly the oxidation rate at 1400°C is much faster than at 1300°C, which makes it more difficult to control the thickness of the oxide that is important for the MOSFETs fabrication.

MOS capacitors fabricated with phosphorous POA has also been investigated. Figure 6.15 shows the high frequency and low frequency C-V curves for the MOS capacitor fabricated with phosphorous POA at 1000°C for 1 hour. It is seen that the difference

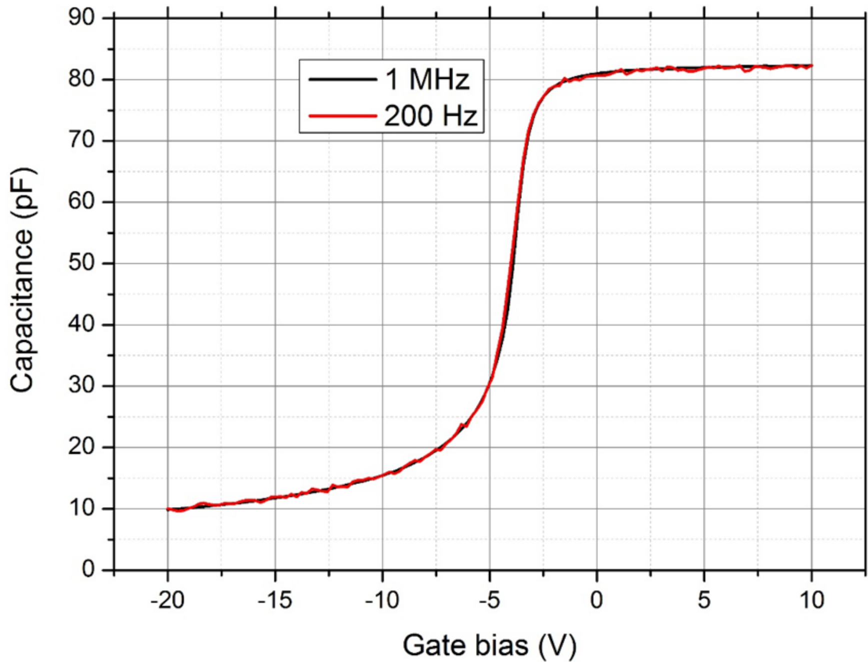


Figure 6.15: High-low frequencies capacitance measurement for MOS capacitor fabricated with phosphorous POA at 1000°C for 2 hours.

between the high frequency and low frequency is very small, two curves look almost identical. This indicates that the phosphorous POA has successfully passivated most the interface trap charges of the MOS capacitor and therefore provides the lowest D_{it}

values among all other POA conditions used this work. This result is consistent for both Terman and high-low frequency capacitance methods. Figure 6.16 shows the interface trap density extracted using high-low frequency capacitance method for MOS capacitors fabricated with N_2O POA, phosphorous POA and the combined N_2O and phosphorous POA.

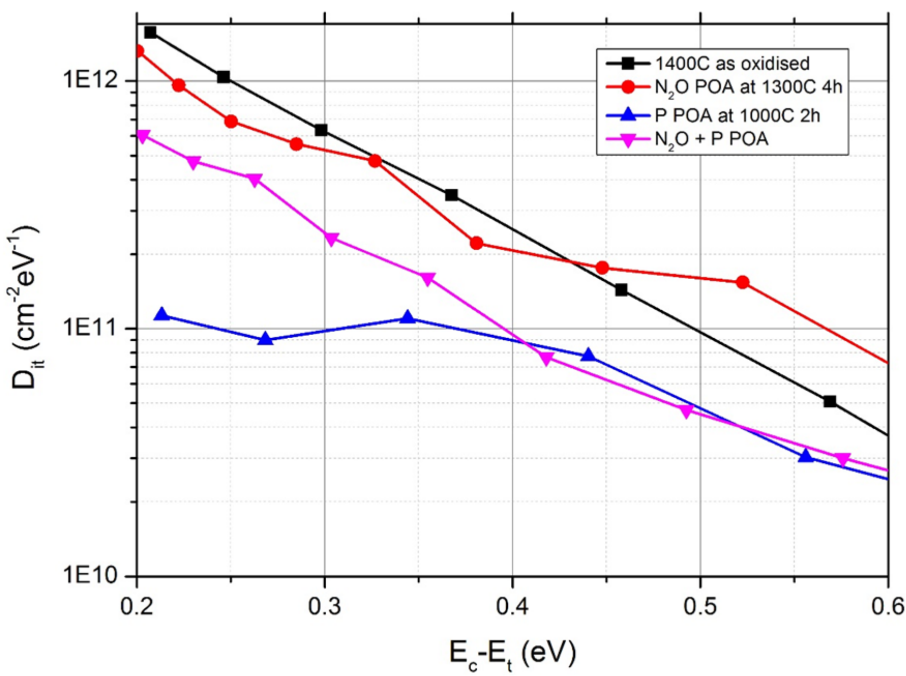


Figure 6.16: Interface trap density extracted using high-low frequency capacitance method for MOS capacitors fabricated with N_2O POA, phosphorous POA and combined N_2O and phosphorous POA.

Results from Figure 6.16 are similar to those obtained using Terman method shown in Figure 6.11. The MOS capacitors with phosphorous POA has the lowest D_{it} compare with others using different POA conditions. The D_{it} extracted using the high-low frequency capacitance method for the phosphorous POA MOS capacitor is about 1×10^{11} $cm^{-2}eV^{-1}$

at 0.2 eV away from the conduction band edge, which is significantly lower than the N_2O POA samples. Similar to the results obtained by using Terman method, the combined N_2O and phosphorous POA did not further reduce the D_{it} beyond those achieved using phosphorous POA, but nonetheless it is still lower than the one just with N_2O POA.

By comparing both Terman and high-low frequency capacitance methods, it is seen that D_{it} values obtained from the high-low frequency capacitance method are, in general, lower than those obtained from the Terman method. The energy level of a trap in the bandgap of silicon carbide is determined by the position of the Fermi level at a given gate bias voltage. Since silicon carbide has a wide bandgap (3.2 eV), only the interface traps with energies between E_c - 0.6 eV can respond to a quasi-static signal at room temperature. For a more accurate extraction of D_{it}, it is common practise to extract the interface trap density from near the conduction band edge (0.2 eV) to 0.6 eV.

It is still debatable whether or not the high-low frequency method is more accurate than the Terman method. The advantage of using the high-low frequency method to extract the D_{it} is that it produces less noise and smoother curve compare to the Terman method, and does not need to know the substrate characteristics for the extraction of ideal C-V curve. The disadvantage is that it requires both high and low frequencies C-V curves available, which in some cases difficult to achieve because of the large noise generated during the low frequency (200 Hz) C-V measurement. The low frequency measurement is susceptible to noise, particularly if the oxide layer quality of the device is poor or there is defect within the SiC which may cause large leakage current and early breakdown of

oxide layer. The recent published paper [49, 142, 143] indicated that the D_{it} determined from the high-low frequency capacitance method underestimates the D_{it} values, because of the large standard deviation of surface potential in SiC MOS structure and the very fast states do respond to 1 MHz or even higher frequency at room temperature [49]. Although not within the scope of this work, the conductance method and the new $C - \psi_s$ method proposed by [49] which give more accurate determination of D_{it} could be useful for future research.

6.2.3 Breakdown Characteristics of N_2O and Phosphorous Annealed Oxides

In spite of the significant improvement of the interface trap density and the channel mobility of MOS devices after phosphorous POA, there are still some concerns related to this POA treatment, such as the threshold voltage instability under bias-temperature stress and high leakage current compare to NO POA oxide as reported in [31]. In this section, the I-V characterises of phosphorous POA MOS capacitors are compared to the N_2O annealed and the without POA MOS capacitors.

Figure 6.17 shows the oxide breakdown characteristics of MOS capacitors fabricated with N_2O POA, phosphorous POA and the combined N_2O and phosphorous POA. Each set of I-V curve data is average of at least 5 MOS capacitors. It is seen that the oxide breakdown electric field is approximately 8 MV/cm for MOS capacitor fabricated with dry

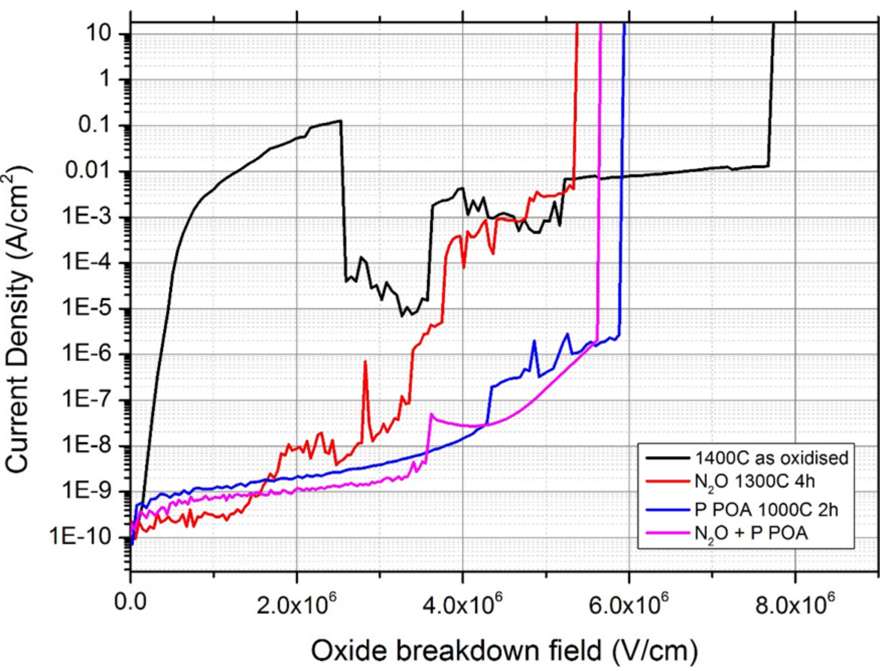


Figure 6.17: I-V characteristics of MOS capacitors fabricated without POA, N_2O POA at 1300C 4 hours, phosphorous POA and combined N_2O and phosphorous POA.

oxidation at 1400°C for 1 hour without POA. After the N_2O POA and phosphorous POA the oxide breakdown field is reduced to around 5.3 MV/cm and 6 MV/cm respectively. The oxide after phosphorous POA shows slightly higher breakdown electric field than those of N_2O POA, and the leakage current of phosphorous POA sample is also lower than that of N_2O POA in general as shown in Figure 6.17. The N_2O POA sample shows smaller leakage current than phosphorous POA sample only at small gate voltage bias with oxide field less than 1.6 MV/cm, after that the leakage current of N_2O POA sample will be higher than the phosphorous POA sample. It is also noticed that although sample fabricated with dry oxidation at 1400°C for 1 hour without POA has the highest oxide breakdown field of about 8 MV/cm, it also has the highest leakage current. This indicates

that oxide quality and reliability for sample without POA treatment are not as good as to those subject to POA treatments, particularly under high temperature. The results of combined N_2O and phosphorous POA are similar to those of just using phosphorous POA with oxide breakdown field of around 5.8 MV/cm.

6.3 4H-SiC Schottky Diodes with JTEs Fabrication

In this section, the fabrication and characterisation of 4H-SiC Schottky diodes with various JTE designs are presented. First, details of the photomask design and epitaxial structures of Schottky diodes are presented. Following this, a discussion of the fabrication process and the reverse breakdown characteristics for the 1 kV Schottky diodes with different JTE designs (single zone JTE and space-modulated JTE) is given.

6.3.1 Photomask Design

A set of mask plates have been designed using Tanner Tools L-Edit software [144] and manufactured at Compugraphics, UK [145] to enable the fabrication of high voltage Schottky diodes. The design of a single 14×14 mm die, which is duplicated across a three inch wafer mask is shown in Figure 6.18. The mask design contains three different sizes of Schottky diodes (100 μm, 300 μm and 1000 μm in diameter), each has the junction termination extension structure design of single zone JTE, space-modulated JTE (SMJTE) and no JTE structures. And there two different sizes of JTE structure involved, one with 200

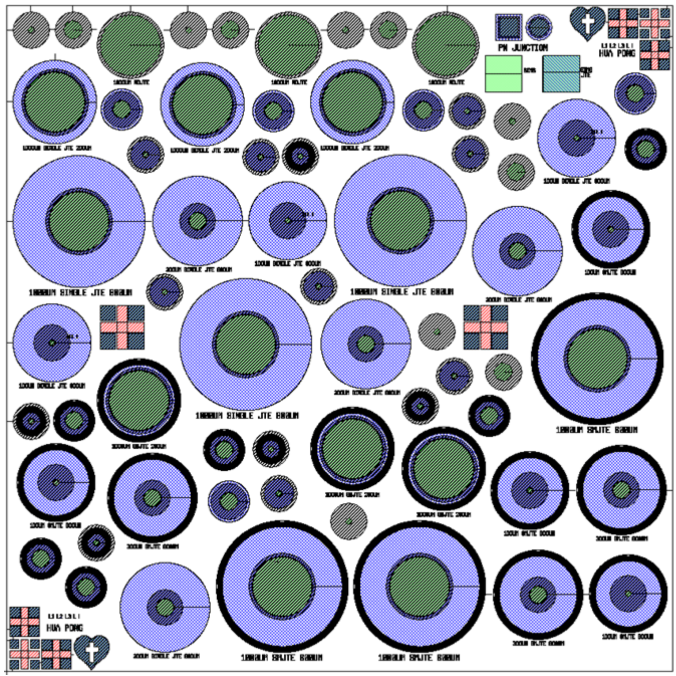


Figure 6.18: Die design for Schottky diode fabrication.

μm in total width and the other with 600 μm. In addition to the Schottky diode devices, there are two MOS capacitor structures and SIMS measurement structures which used to characterise the doping profile of the JTE implantation.

6.3.2 Fabrication Process

The 4H-SiC material for the Schottky diodes were obtained from Norstel AB [137], same as those used for MOS capacitors fabrication. Epitaxial layer thickness and doping concentration are 10 μm and 2×10^{16} cm^{-3} respectively. After epitaxial growth, the wafers have been laser-cut into 14 $\times$ 14 mm chips for subsequent processing.

As for every devices fabrication, the first process in the Schottky diode fabrication was

the cleaning of the 4H-SiC samples using the standard organic, Piranha and RCA cleaning processes as outlined in Appendix B. Following this, S1818 photoresist was deposit on the samples and use the standard photolithography process as outlined in Appendix C to open the window for the alignment marks, and the samples were etched in the ICP etcher for the depth of about 50 nm. After the etching, the photoresist was removed in an O2 plasma, which following by the deposit of 500 nm of TEOS oxide on the samples, this served as the mask for ion implantation. A further 100 nm of Ni was evaporated onto the sample using our Electron Beam Evaporator Deposition system. Using the standard photolithography process with S1818 photoresist, the implantation windows for the JTE structures were patterned onto the sample surface. The Ni was etched using Aqua Regia solution (nitric acid (HNO_3), hydrochloric acid (HCl) and DI water in the ratio 1:5:6), then the exposed TEOS oxide was etched using the reactive-ion etching (RIE) process as discussed in Chapter 5. After the oxide etching, the samples were sent away for ion implantations of the JTE regions for the required doping concentrations by CuttingEdge Ions LLC [146]. Three different set ion implantations were carried out for Schottky diode samples, and details for each ion implantation profiles are illustrated in Table 6.2.

After the ion implantation, the TEOS oxide and the Ni layers were removed in BOE (10% HF) solution and Aqua Region solution respectively. Following this, carbon capping layer was formed onto the sample using the process as discussed in Chapter 5 to protect the surface before the implant activation annealing. After carrying out the annealing at 1650°C for 30 minutes to activate the dopants, the carbon capping layer was removed

Table 6.2: Ion implantation profiles for the JTE regions of 4H-SiC Schottky diodes, for low-dose (LD JTE2), medium-dose (MD JTE1) and high-dose (HD JTE3)

	MD JTE1	**LD JTE2**	**HD JTE3**
Implant Species	Aluminum	Aluminum	Aluminum
Total doping concentration (cm^{-3})	3×10^{17}	2×10^{17}	4×10^{17}
Energy (keV), Dose (cm^{-2})	570, 0.8×10^{13} 380, 0.52×10^{13} 260, 0.35×10^{13} 180, 0.26×10^{13} 120, 0.19×10^{13} 75, 0.14×10^{13}	570, 0.5×10^{13} 380, 0.33×10^{13} 260, 0.22×10^{13} 180, 0.17×10^{13} 120, 0.12×10^{13} 75, 0.09×10^{13}	570, 1×10^{13} 380, 0.65×10^{13} 260, 0.44×10^{13} 180, 0.32×10^{13} 120, 0.25×10^{13} 75, 0.16×10^{13}

in O_2 plasma. Next, a thin layer of sacrificial oxide (50 nm) were grown in the high temperature oxidation furnace and then removed in BOE. After this, 500 nm of TEOS oxide was deposited again on the sample to form as a field oxide for the Schottky diode. Standard photolithography process was used to pattern the active area window, which then the exposed TEOS oxide was etched in the ICP etcher using the RIE etching process. Following this, the remaining photoresist was removed using solvent clean in the ultrasonic bath.

The final step was metallisation process for both Schottky contact and the backside ohmic contact. A layer of Ti/Ni with thickness of 30 nm and 100 nm were evaporated on the backside the samples, which then annealed in the rapid thermal annealing (RTA) furnace to form the ohmic contact as discussed in Chapter 5. Finally, the photolithography process using negative photoresist (AZ5214E) as outlined in Appendix C was used to pattern the top side the samples, Ni layer of 500 nm were deposited to form a Schottky

contact and the unwanted metal and photoresist was removed via the lift-off process in acetone in the ultrasonic bath.

6.3.3 Reverse I-V Characterisation Results

In this Section, the reverse I-V characteristics of the Schottky diodes with different JTE designs are presented. The reverse breakdown voltage of these devices with different JTE designs have been evaluated by means of reverse I-V measurements at room temperature using the high voltage breakdown test rig as shown in Figure 6.19, which was designed and built by our research group in the University of Warwick.

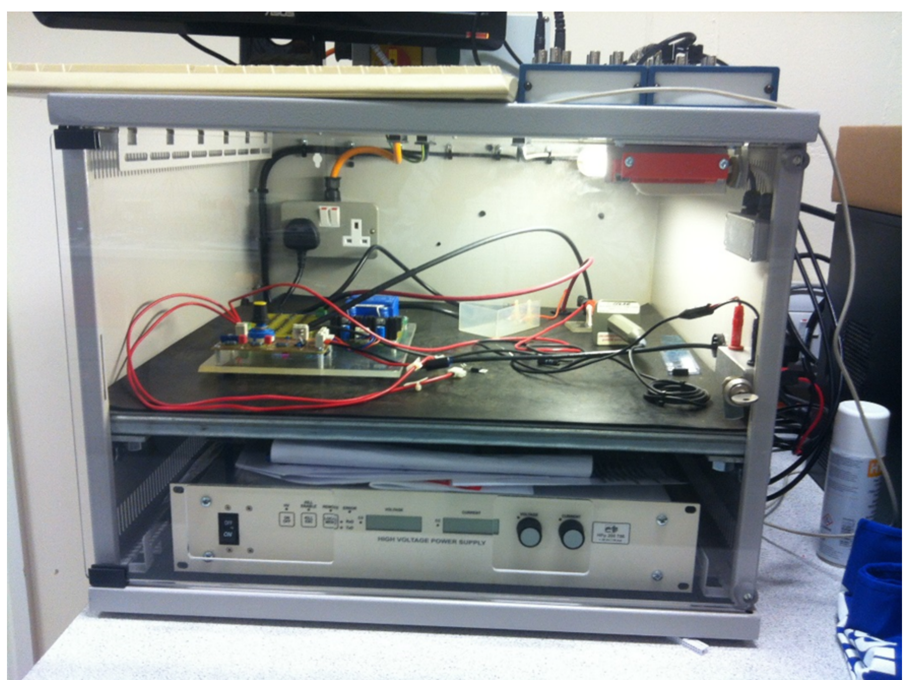


Figure 6.19: High voltage breakdown test rig with power supply goes up to 20 kV.

Although the power supply unit of the high voltage breakdown test rig is capable of

suppling voltage of up to 20 kV, the breakdown test rig is limited to 10 kV in this work due to the limitation of the NI Data Acquisition (DAQ) system which has maximum input voltage of 10 V and the high voltage probe which has attenuation factor of 1000. Nevertheless, this voltage rating is sufficient for the breakdown voltage required in this work. For high voltage breakdown test (10 kV) on devices without packaging, the devices are usually submerged in the insulating liquid (oils or fluorinated hydrocarbons) to prevent arcing. Since the Schottky diodes fabricated in this work have maximum voltage rating of 1 kV, there is no need to use the insulating liquid when performing the breakdown voltage measurement.

The reverse I-V characteristics of the Schottky diodes with JTE doping concentration of 3×10^{17} cm^{-3} (MD JTE1) are shown in Figure 6.20. From the results, it is seen that the breakdown voltage of the Schottky diode without the JTE structure is only about 100 V, which is much smaller than the simulated values as discussed in Chapter 3. With the 200 μm length single zone JTE structure, the breakdown voltage has increased to about 600 V, which is about 54% of the ideal one-dimensional parallel-plane value. The breakdown voltage will increase to about 700 V by increasing the length of the single zone JTE structure to 600 μm as shown in Figure 6.20. The highest breakdown voltage was achieved with the use of the SMJTE JTE structure, which is about 960 V, 86% of the ideal one-dimensional parallel-plane breakdown voltage. The breakdown measurement results have proven that the SMJTE structure can indeed increase the breakdown performance of the devices as shown from the simulation results in Chapter 3. The 600 μm length

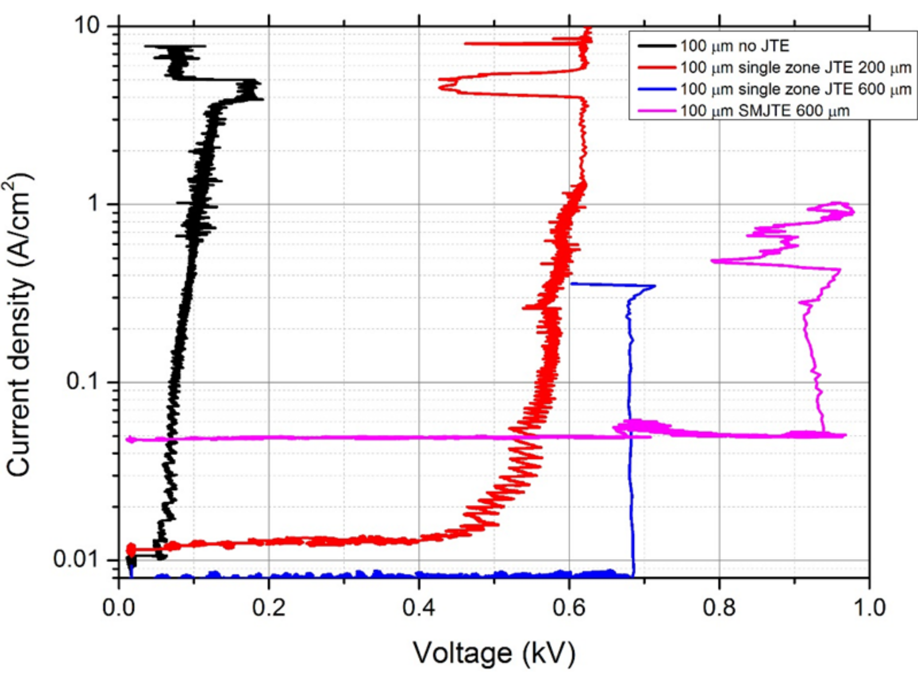


Figure 6.20: Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 3×10^{17} cm^{-3} (medium-dose JTE1).

SMJTE structure was initially designed for the 10 kV 4H-SiC devices, it is also applicable to the 1 kV devices as illustrated by both simulation and the experimental results.

Figure 6.21 and Figure 6.22 show the reverse I-V characteristics of the Schottky diodes with JTE doping concentrations of 2×10^{17} cm^{-3} (LD JTE2) and 4×10^{17} cm^{-3} (HD JTE3). For the Schottky diodes with low-dose JTE structure, breakdown voltage of both the single zone JTE and SMJTE structures are roughly the same, which is about 200 V as shown in Figure 6.21. For the Schottky diodes with high-dose JTE structure, the SMJTE structure shows higher breakdown voltage of about 580 V than the single zone JTE of about 150 V as shown in Figure 6.22. Results have demonstrated that the SMJTE structure not only gives high breakdown voltage but also has wider optimum doping window than the single

zone JTE structure as shown from the simulation results in Chapter 3. The forward I-V characteristics of the Schottky diode is also shown in Figure 6.23.

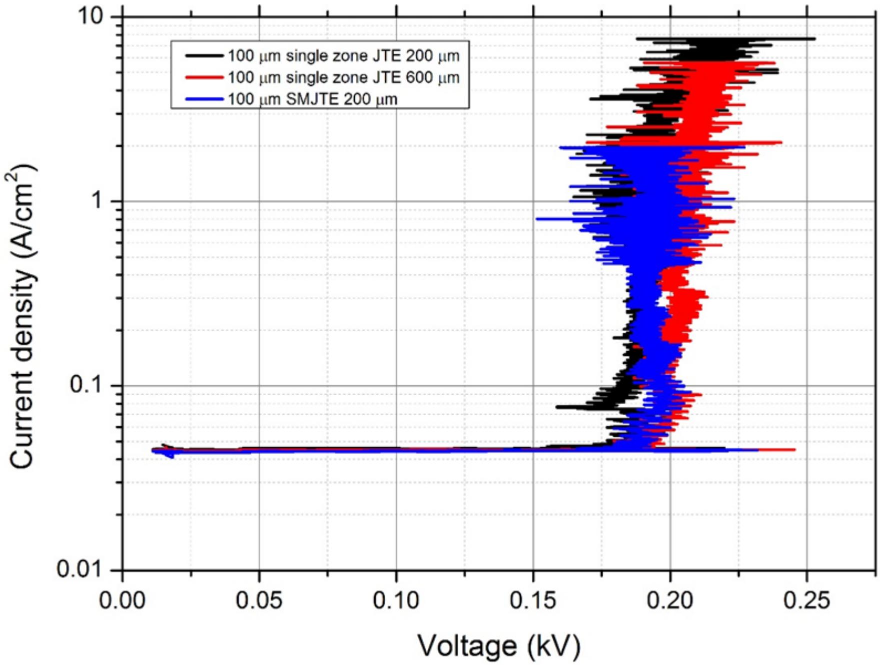


Figure 6.21: Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 2×10^{17} cm^{-3} (low-dose JTE2).

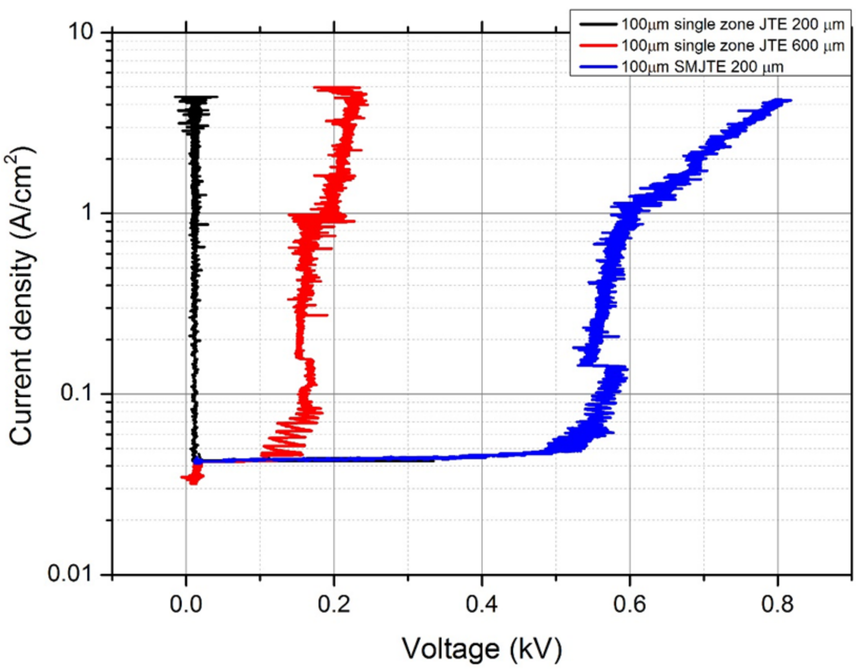


Figure 6.22: Reverse I-V characteristics of the 4H-SiC Schottky diodes with JTE doping concentration of 4×10^{17} cm^{-3} (high-dose JTE3).

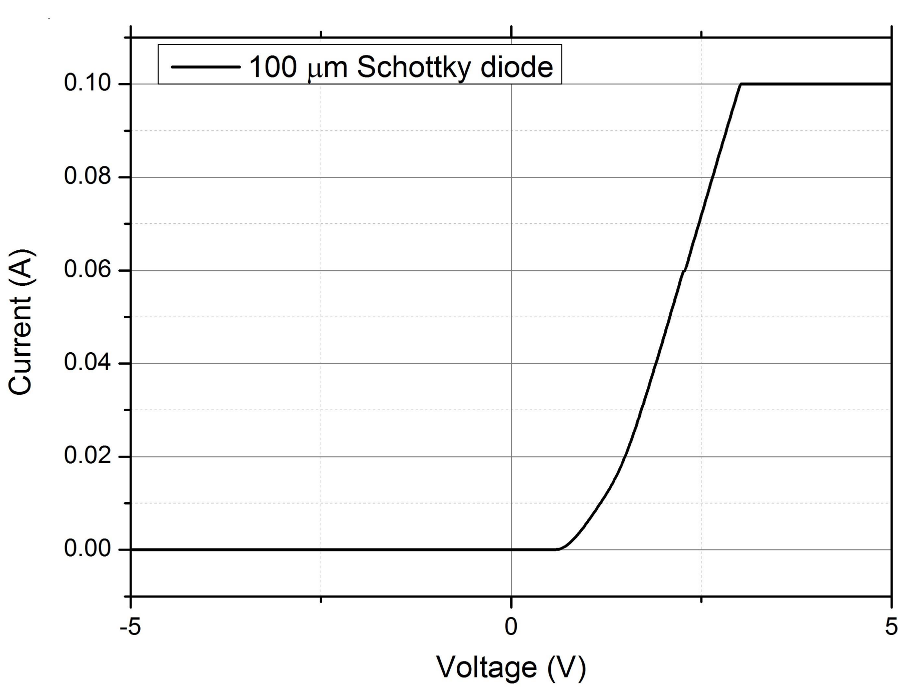


Figure 6.23: Forward I-V characteristics of the 4H-SiC Schottky diodes.

6.4 Summary

In this Chapter, the fabrication and characterisation of both 4H-SiC MOS capacitors and Schottky diodes have been presented. The photomask design and fabrication process of 4H-SiC MOS capacitors were first outlined, following by introducing the two advanced passivation techniques to reduce the interface trap density (D_{it}), namely the N_2O and phosphorous passivations or the combine of both techniques. In particular, the novel phosphorous passivation which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) instead of conventional $POCl_3$ is main focus of this work. Following this, the C-V characterisation for the MOS capacitors fabricated under 1400°C for 1 hour oxidation and different passivation conditions are analysed and compared. The interface traps density (D_{it}) were then extracted and compared using both Terman and High-Low C-V methods. It is seen that from both Terman and high-low C-V methods, the MOS capacitors with N_2O POA treatment have lower interface trap density than the one without POA treatment. In general, increasing the N_2O POA temperature will reduce the interface trap density except that for the N_2O POA at 1500°C. By comparing the results obtained from both Terman and high-low C-V methods, it is observed that nitridation at temperature of 1300°C 4 hours (both direct growth oxide and POA) in general has the best results for lowering the D_{it}. The MOS capacitors with phosphorous POA has the lowest D_{it} of all MOS capacitors fabricated in this work, which is about 1×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV away from the conduction band edge using high-low C-V method. The combined

N_2O and phosphorous POA did not further reduction of D_{it} beyond those achieved using phosphorous POA, but nonetheless it is still lower than the one just with N_2O POA. The advantage and disadvantage of both Terman and high-low C-V methods were also discussed. In general, the D_{it} values obtained from the high-low C-V method are lower and have much smoother curves than those obtained from the Terman method.

Chapter 7

Fabrication and Characterisation of 4H-SiC Lateral MOSFETs

Development of novel techniques to improve the channel mobility and the oxide quality of 4H-SiC MOSFETs are the main focused in this work, which include the use of our unique high temperature oxidation furnace and different passivation techniques as discussed in Chapter 6. In this Chapter, the fabrication and characterisation of 4H-SiC n-channel lateral MOSFETs are presented. First, details of the photomask design and the MOSFET cell structure are presented. Following this, the discussion of fabrication process and the electrical characterisation results for the 4H-SiC MOSFETs with different oxidation and passivation conditions is given, which follows the chronological evolution of these devices. First generation devices have been fabricated with a box-like implantation profile for the p-body region, and the effect of different implant activation temperatures on the channel mobility have been investigated. High temperature oxidation (1500°C) and N_2O nitridation techniques were also investigated. A second generation lateral MOSFETs have

been fabricated with a retrograde doping profile for the p-body region, which is the same as the doping profile used in the vertical power MOSFET. The impact of sacrificial oxide thickness and the effect of a novel phosphorous passivation technique on the channel mobility has also been investigated. Oxide breakdown tests were carried out on the lateral MOSFETs to examine the reliability of the gate oxide with different passivation conditions.

7.1 Photomask Design

The design of lateral MOSFET photomask is much simpler than the vertical power MOSFET design since there are less fabrication steps involved. The photomask plates were designed using Tanner Tools L-Edit software [144] and manufactured at Compugraphics, UK [145] as were other photomask used in this work. In total, there are four main steps (four mask plates) required for the fabrication of the lateral MOSFETs in this work: the etch of alignment marks, the implantation for source/drain, the metallisation of source and drain contacts and the metallisation of gate contact. The design of a single die is 5mm $\times$ 5mm with total of 17 lateral MOSFETs across the die as shown in Figure 7.1. The dimensions of the MOSFET structure are shown in Figure 7.2.

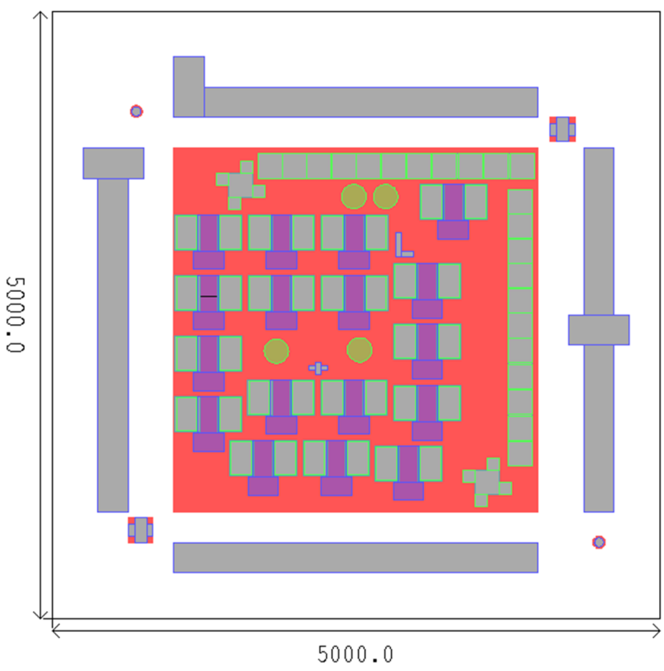


Figure 7.1: Die design for lateral MOSFET fabrication.

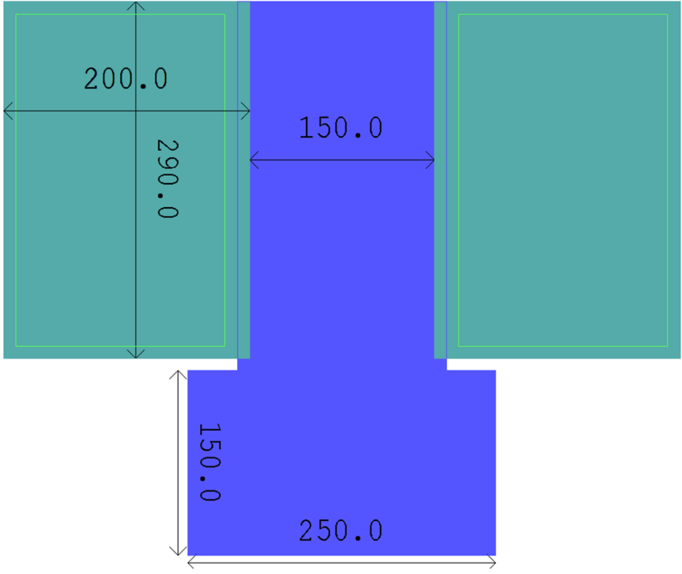


Figure 7.2: Dimensions of lateral MOSFET structure (in μm).

7.2 Fabrication Process

The 4H-SiC material used to fabricate MOSFETs were obtained from Norstel AB [137] and is the same as that used for MOS capacitors and Schottky diodes fabrication. The wafer with epitaxial layer thickness and doping concentration of 10 μm and 2×10^{16} cm^{-3} was used for the first generation of lateral MOSFETs. For the second generation of lateral MOSFETs, the wafer with epitaxial layer thickness and doping concentration of 30 μm and 4×10^{15} cm^{-3} were used, which is the same as those used for the vertical power MOSFET fabrication as discussed in Chapter 8. After epitaxial growth, the 4 inch wafers were laser-cut into 4 quarters for subsequent processing.

The first process in the lateral MOSFETs fabrication was the cleaning of the 4H-SiC wafers using the standard SiC cleaning process as outlined in Appendix B. Following this, wafers were sent away for a blanket ion implantation by CuttingEdge Ions LLC [146] for the p-body region with box-like doping profile for the first generation lateral MOSFETs, and with retrograde doping profile for second generation of lateral MOSFETs. Details of both ion implantation energies and doses are shown in Table 7.1 and their doping profiles predicted by the SRIM [147] simulations are illustrated in Figures 7.3 and 7.4.

After the p-body implantation, alignment marks were patterned using the standard photolithography process with S1818 photoresist and etched to a depth of about 1 μm using the ICP etcher. Following this, photoresist was removed in acetone and a 500 nm layer of TEOS oxide was deposited on the wafers followed by a 500 nm layer of Ni which

Table 7.1: Ion implantations with the box-like doping profile and the retrograde doping profile.

	Box-like doping profile	**Retrograde doping,profile**
Implant Species	Aluminum	Aluminum
Implant Temperature (°C)	650	650
Total doping concentration (cm^{-3})	1×10^{18}	4×10^{18} at the bottom and 2×10^{16} at the surface
Energy (keV), Dose (cm^{-2})	500, 2.2×10^{13} 350, 1.1×10^{13} 250, 1.1×10^{13} 150, 9.5×10^{12} 80, 6.5×10^{12} 35, 3×10^{12}	350, 8×10^{13} 230, 4×10^{13} 30, 1×10^{11}

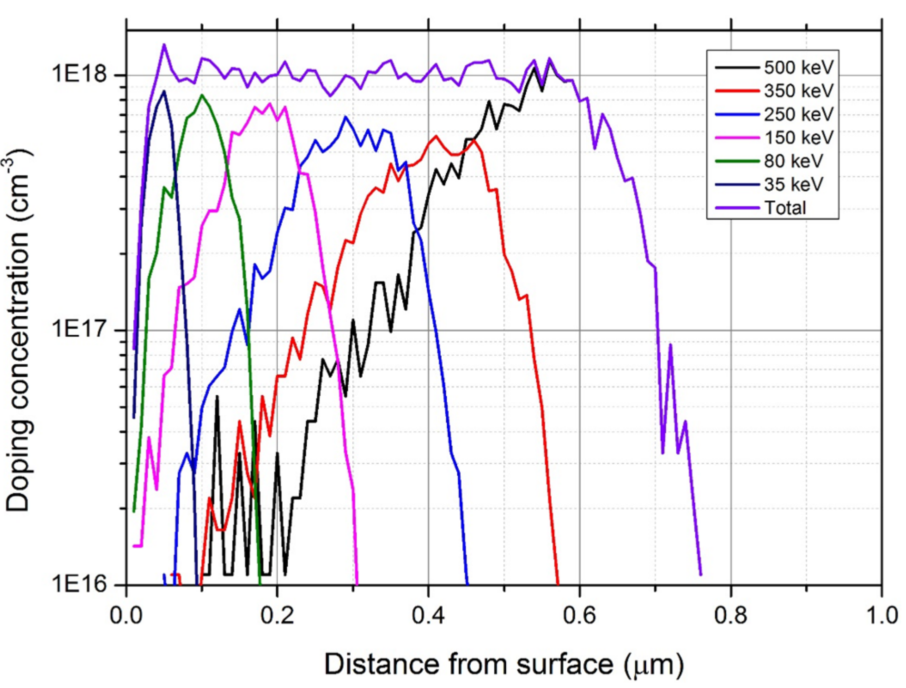


Figure 7.3: Simulated implanted box-like profile for p-body region of lateral MOSFETs.

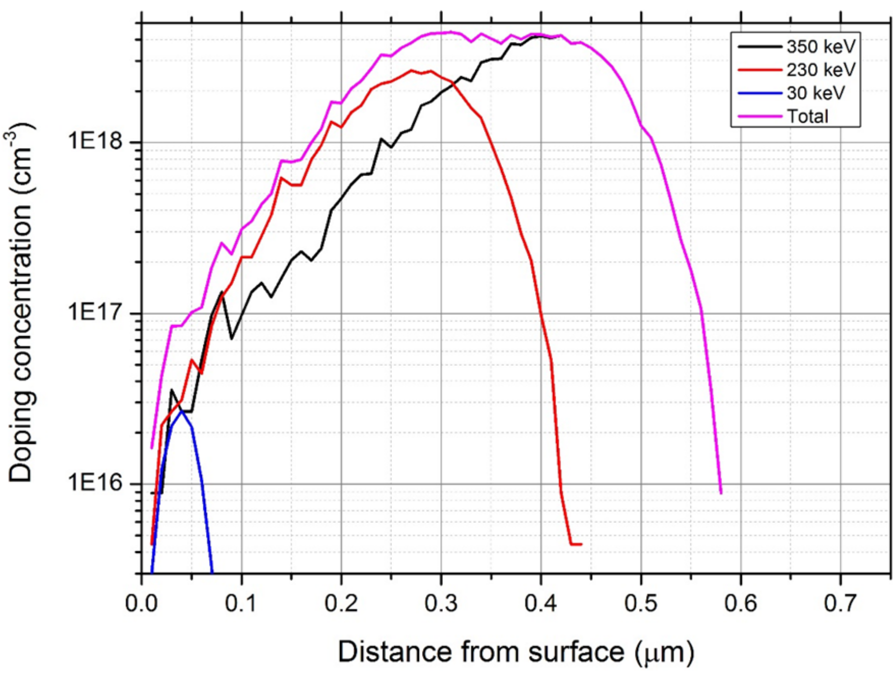


Figure 7.4: Simulated implanted retrograde profile in p-body region of lateral MOSFETs used in the second generation devices.

is used as masking layer for the source and drain region implantations. Following this, the standard photolithography process with S1818 photoresist was used to pattern the source and drain regions for ion implantation. The Ni was etched using Aqua Regia solution and the exposed TEOS oxide was etched using the reactive-ion etching (RIE) process as discussed in Chapter 5. After the oxide etching, the wafers were sent away again for ion implantations for the source and drain regions of the lateral MOSFETs with nitrogen doping concentration of 5×10^{19} cm^{-3}. Figure 7.5 shows the SRIM simulated doping profile of the source and drain regions.

After the ion implantation was completed the samples were laser-cut into 5mm$\times$5mm chips and followed by the removal of Ni in Aqua Regia solution and the TEOS oxide

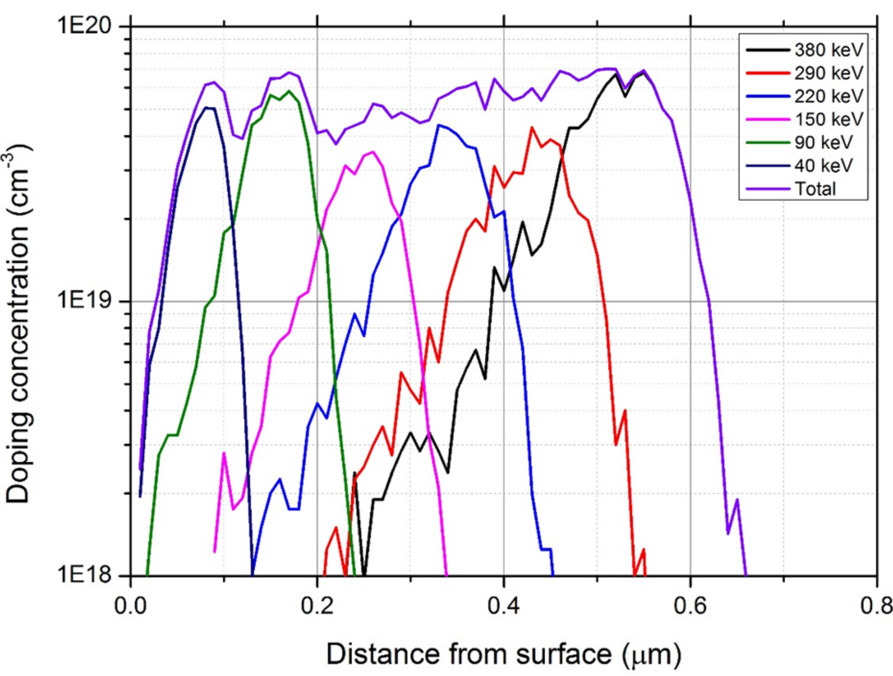


Figure 7.5: Simulated implanted box-like profile for source and drain regions of lateral MOSFETs.

in BOE (10% HF). Next, gate oxide of approximately 50 nm was grown in the high temperature oxidation furnace after the standard SiC clean process was performed as outlined in Appendix B. After this, the standard photolithography process using negative photoresist (AZ5214E) was used to pattern the source and drain of the lateral MOSFETs. MOSFET samples were then dip into the BOE for short time (2∼3 minutes depending on oxide thickness) to remove the oxide on the source and drain area. Following this, Ti and Ni with thickness of 30 nm and 100 nm were evaporated onto the samples, the unwanted metals and photoresist were then removed via an ultrasonic lift-off process in acetone. Samples were loaded into the rapid thermal annealing (RTA) furnace straight after the lift off process and annealed at 1000°C for 2 minutes in an argon atmosphere to form the ohmic

contacts. After this, negative photoresist (AZ5214E) process was used again to pattern the gate of the lateral MOSFETs, following which a layer of 500 nm thick aluminium was evaporated on the sample to form the gate contact metal. The unwanted aluminium and photoresist were then removed via an ultrasonic lift-off process in acetone. The fabrication process flow with cross sectional diagrams of lateral MOSFETs are illustrated in Table 7.2. Figure 7.6 shows the picture fabricated 4H-SiC lateral MOSFET under microscope.

Table 7.2: 4H-SiC lateral MOSFET fabrication process flow (not to scale).

Cross-sectional diagram	Fabrication process
i. P-body implant / 4H-SiC	P-body blanket implantation (Standard SiC cleaning process carried out beforehand).
ii. Photoresist / P-body implant / 4H-SiC	**Mask1** Deposit S1818 photoresist and pattern to form the alignment marks.

Continued on next page

Table 7.2 – continued from previous page

Cross-sectional diagram	Fabrication process
iii. Photoresist; P-body implant; 4H-SiC	Etch the 4H-SiC to form the alignment marks and isolate p-body regions from other devices in the ICP etcher .
iv. Ni; TEOS; Ni; TEOS; Ni; TEOS; 4H-SiC	1. Remove photoresist in acetone. 2. Deposit TEOS and Ni for the masking layers for implantation.
v. Photoresist; Ni; TEOS; Ni; TEOS; Ni; TEOS; 4H-SiC	**Mask2** Deposit photoresist and pattern to form the source and drain areas.
vi. Ni; TEOS; Ni; TEOS; Ni; TEOS; 4H-SiC	1. Etch Ni in Aqua Regia solution and TEOS in the ICP etcher using RIE programme. 2. Remove photoresist and O2 plasma.

Continued on next page

Table 7.2 – continued from previous page

Cross-sectional diagram	Fabrication process
vii. 4H-SiC	1. Implant source and drain regions. 2. Remove Ni in Aqua Regia solution and TEOS in BOE (10% HF).
viii. 4H-SiC	Grow gate oxide of ~50nm in the HiTech furnace.
ix. Photoresist Oxide 4H-SiC	**Mask3** 1. Pattern source and drain window using negative photoresist AZ5214E. 2. Etch oxide in BOE for 2~3 minutes.
x. Ti/Ni Oxide Ti/Ni 4H-SiC	1. Deposit Ti/Ni source and drain contacts and lift off in acetone using ultrasonic bath. 2. RTA anneal at 1000°C for 2 minutes.

Continued on next page

Table 7.2 – continued from previous page

Cross-sectional diagram	Fabrication process
xi.	**Mask4** Pattern gate window using negative photoresist AZ5214E.
xii.	Deposit Al gate contact and lift off in acetone using ultrasonic bath.

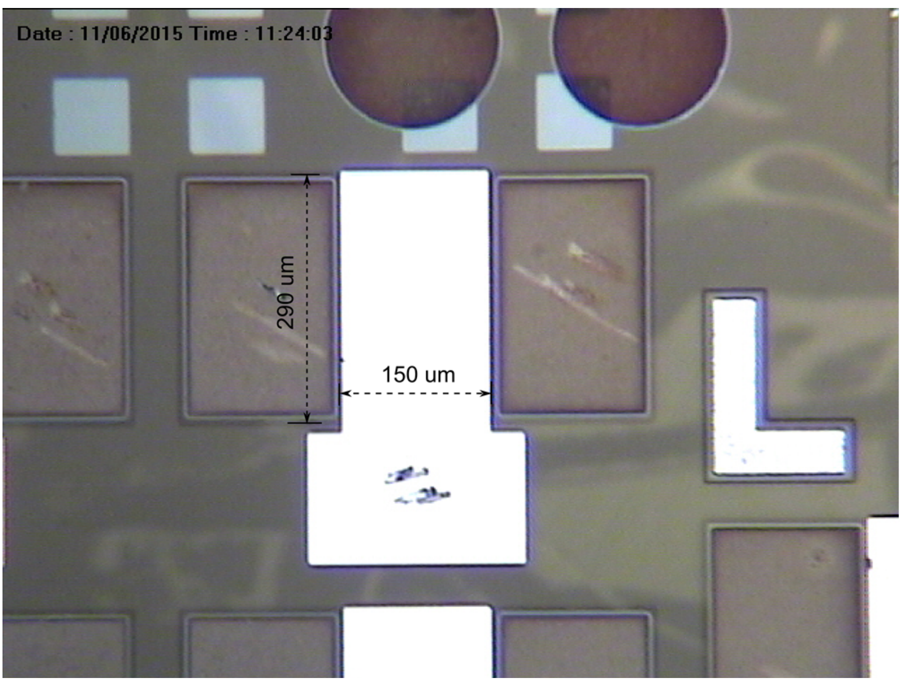


Figure 7.6: Top view of the fabricated 4H-SiC lateral MOSFET from the microscope.

7.3 First Generation 4H-SiC Lateral MOSFETs

The first generation 4H-SiC lateral MOSFETs were fabricated with box-like p-body doping profile with total doping concentration of 1×10^{18} cm^{-3}. Though this means that the channel mobility values will not be representative of the mobility values for the vertical power MOSFET which uses a retrograde p-body doping profile, the effect of implant activation temperature and N_2O passivation conditions on the channel mobility can still be evaluated, and used as a benchmark for future device iterations.

7.3.1 Effect of High Temperature Oxidation

As discussed in Chapter 2, the conventional standard quartz oxidation furnace which designed for Si is limited to a maximum operation temperature of 1100°C-1200°C. However, because of the much slower oxidation rate of SiC than Si, even at 1200°C the oxidation rate is still slow. Our unique high temperature oxidation furnace which is capable of going up to a 1500°C oxidation temperature enables us to have a much faster oxidation rate. It is reported in the literature [82,83] that dry oxidation of SiC at high temperature (≥1200°C) can reduce the interface trap density (D_{it}). Naik and Chow [83] have indicated a reduction in D_{it} by oxidising at 1400°C, although their corresponding MOSFETs have a mobility of ∼2 cm^2/V.s. Recent publications [32,33] shows that the D_{it} can be reduced to about 2×10^{11} $cm^{-2}eV^{-1}$ by oxidation up to 1500°C and 1600°C under a low oxygen flow rate, and the corresponding MOSFETs have peak field effect mobility of about 40 cm^2/V.s. In this work, high temperature oxidation at 1400°C and 1500°C on the lateral MOSFETs have been investigated and their corresponding field effect mobility have been compared.

Two lateral MOSFETs have been fabricated using the process outlined in section 7.2 with gate oxide grown under 1400°C for 1 hour and 1500°C for 30 minutes respectively. The thermal oxidation process for 1400°C is shown in Figure 7.7, as discussed in Chapter 2. The oxidation temperature is raised with a ramping rate of 5°C per minute with Argon gas flows (5 L/minute), and maintained for 15 minutes to make sure the furnace achieves

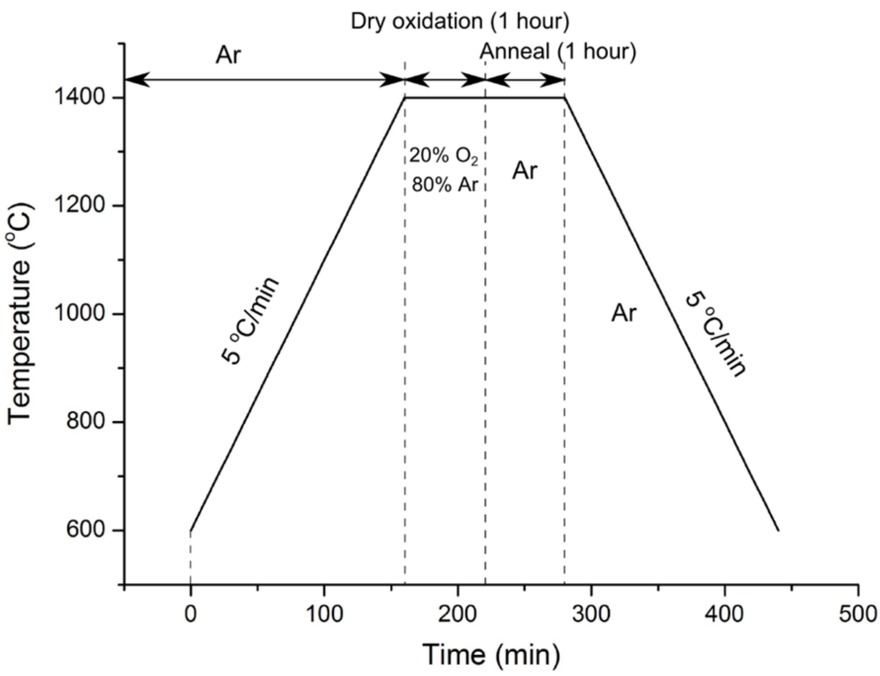


Figure 7.7: Standard thermal oxidation at 1400°C to grow ∼50 nm of SiO_2 on 4H-SiC.

the oxidation temperature before turning on the oxygen valve. Oxidation is carried out with 20% oxygen in argon environment (O_2 flow rate of 1 L/minute and Ar flow rate of 4 L/minute). The oxidation is followed by a one hour argon anneal with the oxygen switched off and argon flow rate of 5 L/minute, and the temperature is then ramped down to 600°C at a rate of 5°C per minute. The oxide thickness after 1400°C for 1 hour is between 45 to 50 nm, and the oxide thickness after 1500°C for 30 minutes is between 30 to 35 nm. The field effect mobility against gate bias for both MOSFETs are shown in Figure 7.8.

From Figure 7.8 it is seen that the field effect mobility for both thermal oxidation at 1500°C and 1400°C are very similar, which is around 1.1 to 1.3 $cm^2/V.s.$ There

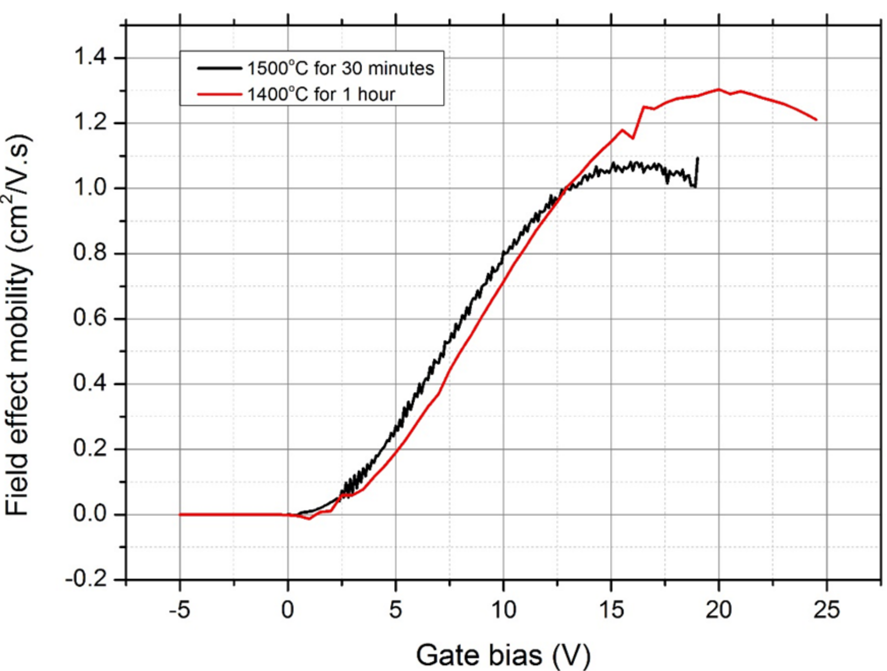


Figure 7.8: Field effect mobility as a function of gate bias for the 4H-SiC lateral MOSFETs with thermal oxidation at 1500°C for 30 minutes and at 1400°C for 1 hour.

is no significant improvement in terms of channel mobility by using higher oxidation temperature at 1500°C than the standard 1400°C oxidation. Without any passivation treatments such as N_2O or phosphorous discussed in Chapter 6, the field effect mobility for the 4H-SiC lateral MOSFETs are all around 1.2 $cm^2/V.s$, which is close to the value reported in literature [83] at about 2 $cm^2/V.s$ by oxidising at 1400°C. Therefore, the enhanced oxidation rate at high temperature may reduce the interface states at the 4H-SiC/SiO_2 interface attributed to the carbon clusters at the interface due to incomplete oxidation because of slow thermal oxidation rates of 4H-SiC [83], however, the reduction of interface states by high oxidation temperature does not necessary means that the field effect mobility will be increased as shown by our lateral MOSFETs fabrication results.

7.3.2 N_2O Post Oxidation Annealing and N_2O grown oxide

It is widely known in SiC research community that thermally grown oxides annealed in nitric oxide (NO) or nitrous oxide (N_2O) can reduce the interface trap density and increase the channel mobility. Directly grown oxide in N_2O environment has also been reported by some authors [16,85], which it exhibits better electrical properties compared to that of post oxidation annealing under the same temperature and time. In this section, different N_2O post oxidation annealing conditions for the lateral MOSFETs have been investigated and compared with their corresponding interface trap density from MOS capacitors.

Lateral MOSFETs have been fabricated using the process outlined in Section 7.2 with gate oxide grown under 1400°C for 1 hour, and instead of the argon anneal after the oxidation process, N_2O post oxidation anneal was carried out with flow rates of 1L/minute and Ar flow rates of 4 L/minute. Table 7.3 summarised the different oxidation and N_2O post oxidation annealing (POA) conditions used for the first generation of 4H-SiC lateral MOSFETs and their corresponding field effect mobility and threshold voltage values. Figure 7.9 and Figure 7.10 show the transfer characteristics of the lateral MOSFETs fabricated and their field effect mobility against the gate bias.

Table 7.3: Summary of first generation of 4H-SiC lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions.

Gases	**Oxidation temperature [°C]**	**Oxidation time [hour]**	**POA temperature [°C]**	**Annealing time [hour]**	**Oxide thickness [nm]**	**Field effect mobility [cm^2/V.s]**	$V_{\mathbf{TH}}$ **[V]**
O_2	1200	7.5	n/a	n/a	23	n/a	n/a
O_2	1400	1	n/a	n/a	48	1.2	11
O_2	1400	1	1200	1	65	4	15
O_2	1400	1	1300	1	43	16	6
O_2	1400	1	1300	2	46	16	6
O_2	1400	1	1300	4	50	17	6
O_2	1400	1	1400	1	56	13	8
O_2	1400	1	1400	4	77	15	7
O_2	1400	1	1500	0.5	135	14	19
O_2	1500	0.5	n/a	n/a	30	1	7.5
N_2O	1300	4	n/a	n/a	41	19	0
N_2O	1400	1	n/a	n/a	30	16	0

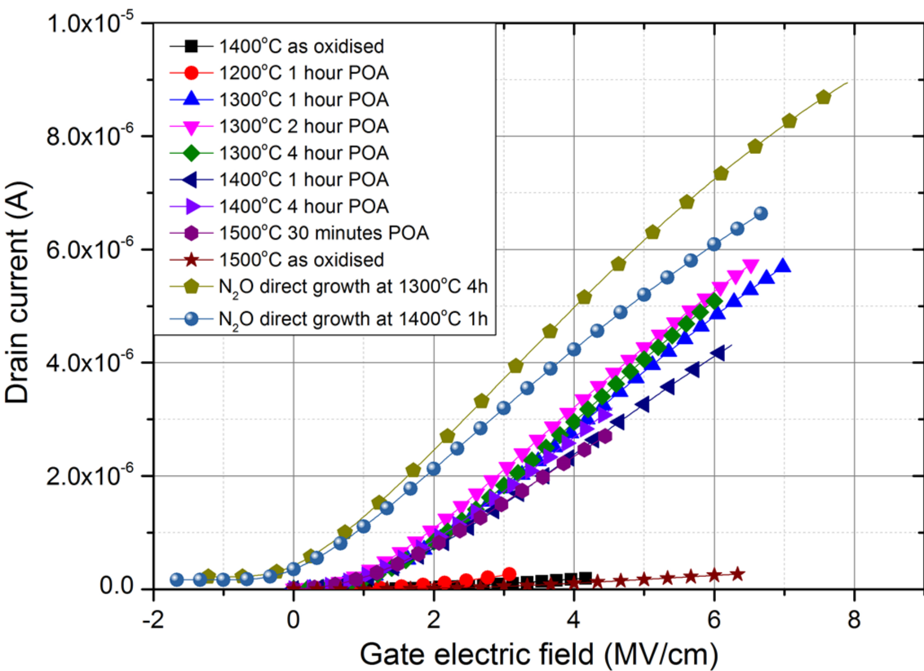


Figure 7.9: Transfer characteristic of lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions.

From the above results it is seen that the 4H-SiC lateral MOSFET without the N_2O post oxidation annealing treatment has the lowest field effect mobility, which is about 1.2 $cm^2/V.s$. Increasing the N_2O post oxidation annealing temperature, the field effect mobility and the output current also increase. After 1200°C of N_2O post oxidation annealing for 1 hour, the field effect mobility has increased to 4 $cm^2/V.s$. The highest field effect mobility for the N_2O post oxidation anneal samples was found to be at 1300°C for 4 hours, which is about 17 $cm^2/V.s$. Different N_2O post oxidation annealing time (1 hour, 2 hours and 4 hours) at 1300°C on the 4H-SiC lateral MOSFETs were also investigated, it is found that the N_2O post oxidation annealing time have little effect on the field effect mobility of the MOSFETs, which the field effect mobility N_2O post oxidation anneal at

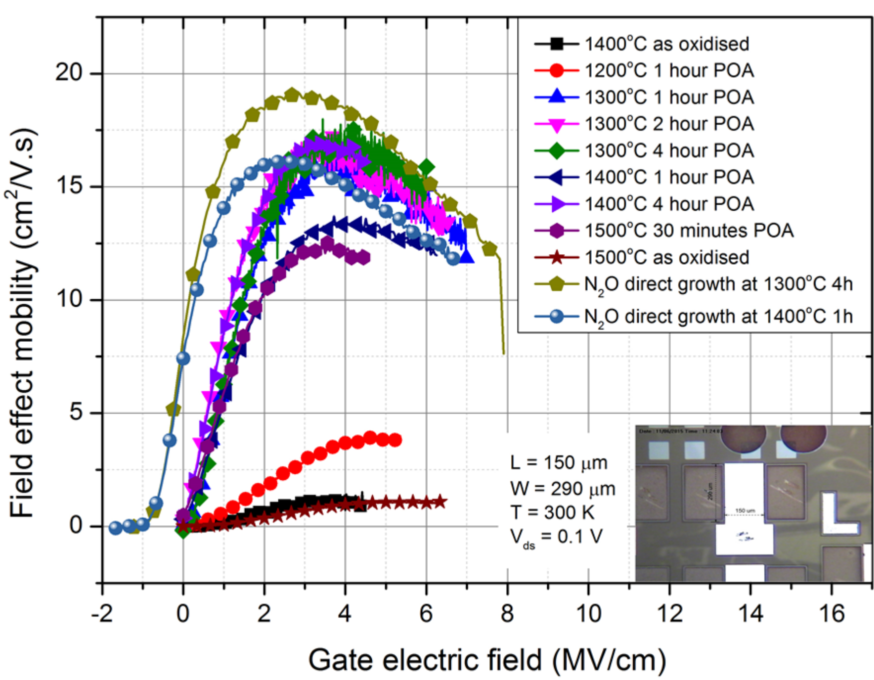


Figure 7.10: Field effect mobility versus gate voltage of lateral MOSFETs with different oxidation and N_2O post oxidation annealing conditions.

1300°C for 1 hour is 16 $cm^2/V.s$. One thing to notice is that further increase the N_2O post oxidation annealing temperature to 1400°C and 1500°C will actually reduce the field effect mobility as shown in Figure 7.10. MOSFETs with higher field effect mobility will have higher transconductance value as seen discussed in Chapter 4, this is also observed from our fabricated 4H-SiC lateral MOFETs as shown in Figure 7.9. Two MOSFETs samples with directly grown oxide in N_2O were also investigated. It is seen that MOSFETs with directly grown oxide in N_2O exhibit better electrical properties than those of annealed in the same gas. For the nitridation condition of 1300°C for 4 hours, the MOSFETs with direct growth oxide have field effect mobility of about 19 $cm^2/V.s$ whereas the MOSFETs with annealed oxide have field effect mobility of about 17 $cm^2/V.s$.

The threshold voltage of lateral MOSFETs were also seen to be changing with different of N_2O post oxidation annealing conditions. MOSFET fabricated at 1400°C oxidation for 1 hour without N_2O post oxidation annealing has threshold voltage of about 11 V. After the N_2O post oxidation annealing at 1200°C for 1 hour, the threshold voltage is increased to about 15 V due to the increase of negative trapped charge near the 4H-SiC/SiO_2 interface during oxidation [33] and the effect of N_2O passivation of interface trap charge is much slower at lower post oxidation annealing temperature (1200°C). However, increase the N_2O annealing temperature to 1300°C, the threshold voltage is reduced to about 6 V as shown in Table 7.3. The reduced threshold voltage after N_2O post oxidation annealing temperature at 1300°C is due to the reduction in the trapped negative charge density near the SiO_2/SiC interface and the exposure of positive oxide charge [33]. The lowest threshold voltage ($V_{TH} \approx 0$ V) is observed for the MOSFETs with direct growth oxide under N_2O environment at 1300°C and 1400°C, which also indicates a further reduction in the trapped negative charge and exposure of more positive oxide charge. The reduction in negative trapped charge is also reflected by the field effect mobility of about 19 cm^2/V.s compare to the MOSFET without passivation with field effect mobility of only about 1.2 cm^2/V.s as shown in Figure 7.10.

The interface trap densities extracted from the 4H-SiC MOS capacitors with different N_2O post oxidation annealing conditions are already shown in Chapter 6. From Figure 6.14 in Chapter 6, it is seen that MOS capacitor fabricated at 1400°C oxidation for 1 hour without N_2O post oxidation annealing has the highest interface trap density (D_{it}).

Increasing the N_2O nitridation temperature will reduce the D_{it}, except for the process performed at 1500°C for 30 minutes. This is because the oxidation rate of SiC at 1500°C is much faster than at 1400°C resulting much thicker oxide layer. The released carbon atoms during oxidation of SiC will accumulate into carbon cluster acting as interface traps [16] and the nitridation process to remove the interstitial carbon and carbon clusters is less effective at 1500°C for 30 minutes because of the much thicker oxide layer and the shorter nitridation time. The lowest D_{it} was found to be with N_2O direct growth oxide at 1300°C for 4 hours, which is about 1.2×10^{11} cm^{-2}eV^{-1} at $E_C - E_T = 0.2$ eV. The lowest D_{it} corresponds to the highest field effect mobility for the lateral MOSFET as shown in Figure 7.10. However, for the N_2O post oxidation annealing samples the lowest D_{it} was found to be at 1400°C 1 hour, which does not give the highest field effect mobility for the MOSFETs. The indicates that the lowest D_{it} obtained after the N_2O post oxidation annealing does not necessary result in the highest field effect mobility for the MOSFETs, although the difference between them are very small. Nevertheless, the N_2O post oxidation annealing does indeed results in lower D_{it} and higher field effect mobility than the samples without N_2O post oxidation annealing. Overall, lower the interface trap density the higher the field effect mobility for the 4H-SiC MOSFETs.

7.4 Second Generation 4H-SiC Lateral MOSFETs

The second generation 4H-SiC lateral MOSFETs were fabricated with the retrograde p-body doping profile having a peak doping concentration of 4×10^{18} cm^{-3} at the bottom of the doping profile (0.4 μm from the surface) and gradually reduced doping concentration toward the surface where it is reduced to doping concentration of 2×10^{16} cm^{-3} as illustrated in Figure 7.4. This doping profile was used on the vertical power MOSFETs to form as a P+ shielding region to protect the channel region from high electric field developed in the drift region and to maintain the low threshold voltage of the device as discussed in Chapter 3. In this section, the impact of sacrificial oxide thickness on channel mobility of the lateral MOSFETs were investigated. Following this, the N_2O and the novel phosphorous passivation to improve the channel mobility of the lateral MOSFETs were looked at. Finally, the oxide breakdown measurements at room temperature on the lateral MOSFETs with different post oxidation conditions were carried out to check their oxide reliability.

7.4.1 Impact of Sacrificial Oxide Thickness on Channel Mobility

The purpose of growing a sacrificial oxide is to remove a thin layer of the SiC material from its surface in order to have better surface roughness or to achieve a certain surface doping concentration by etching away the oxide. Due to the nature of the retrograde doping profile, different thickness of sacrificial oxide will lead to different p-body doping

concentration at the surface, which will affect the threshold voltage and the on-state characteristics of the device. To investigate the effect of different sacrificial oxide thickness on the lateral MOSFETs, different sacrificial oxide thickness were grown and then removed in BOE (10% HF) prior to the fabrication of the lateral MOSFETs. Figure 7.11 shows the field effect mobility versus gate bias for the lateral MOSFETs with different sacrificial oxide thickness, and Figure 7.12 shows the peak field effect mobility versus the oxidation time of the sacrificial oxide. The sacrificial oxide was grown using the high temperature oxidation furnace as shown in Figure 6.2 with dry oxidation at 1400°C in a diluted oxygen environment (O_2: 1 L/min and Ar: 4 L/min) as shown in Figure 7.7.

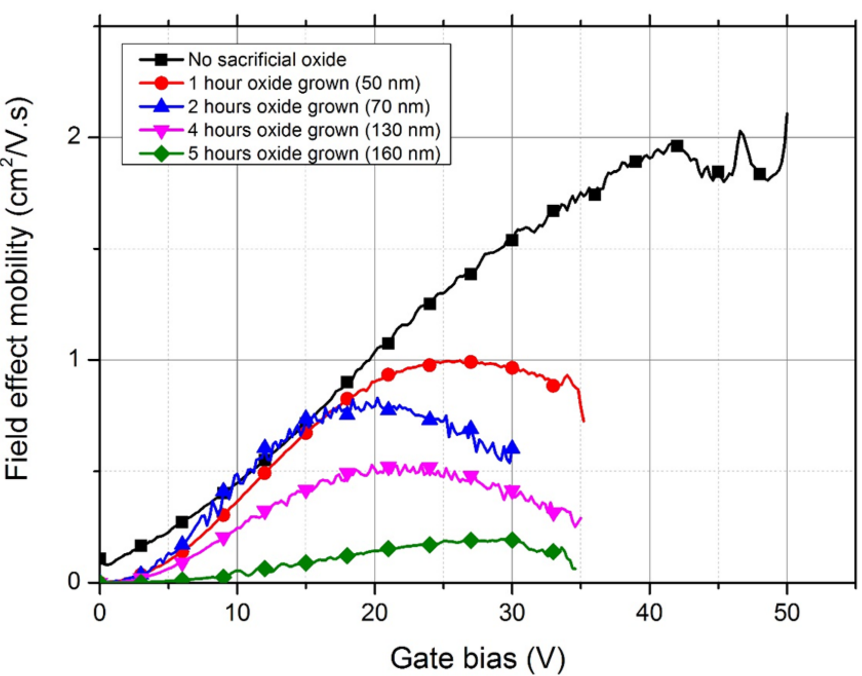


Figure 7.11: Field effect mobility versus gate bias for the lateral MOSFETs with different sacrificial oxide thickness.

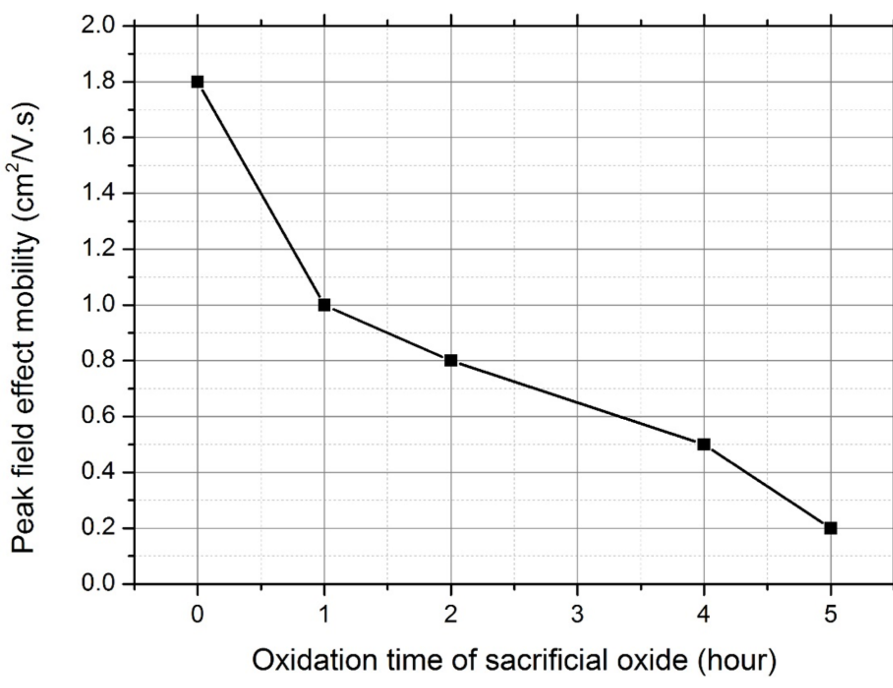


Figure 7.12: Peak field effect mobility versus oxidation time of sacrificial oxide.

From Figures 7.11 and 7.12 it is seen that the thinner the sacrificial oxide the better the field effect mobility of the MOSFETs. Lateral MOSFETs fabricated without the sacrificial oxide have the highest peak field effect mobility, which is about 1.8 $cm^2/V.s$. As the sacrificial oxidation time increases, the peak field effect mobility reduced linearly as shown in Figure 7.12. This observation indicates that the interface trap density caused by the excess carbon released during the thermal oxidation as discussed in Chapter 6 will increase as the sacrificial oxidation time increases. And these excess carbon either as isolated atoms or in the form of clusters will remain at the SiO_2/SiC interface even after the sacrificial oxide is removed in BOE (10% HF). Therefore, for the lateral MOSFETs and vertical power MOSFETs which have the retrograde p-body doping profile, the sacrificial

oxide process was not used in this work due to reduction of the channel mobility.

7.4.2 N_2O and The Novel Phosphorous Passivation

The use of N_2O and phosphorous passivation techniques on the pre-grown oxides have been proven to be effective in reducing the interface trap density on 4H-SiC MOS capacitor as shown in Chapter 6. The best results for lowering the D_{it} using N_2O post oxidation annealing technique was found to be at temperature of 1300°C for 4 hours. The novel phosphorous passivation technique which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) has resulted in the lowest D_{it} so far in this work, which is about 1×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV away from the conduction band edge using high-low C-V method. In this section, the field effect mobility of lateral MOSFETs fabricated using the N_2O POA at 1300°C for 4 hours and the phosphorous POA are illustrated and compared.

N_2O POA at 1300°C for 4 hours have been used on the lateral MOSFETs with different sacrificial oxide thickness as those shown in Figure 7.11. Figure 7.13 shows the field effect mobility against the gate bias for the 4H-SiC lateral MOSFETs after N_2O POA at 1300°C for 4 hours with different sacrificial oxide thickness. From Figure 7.13 it is seen that after the N_2O POA the field effect mobility has increased from a single digit mobility ($\sim$1 cm^2/V.s) to average of about 15 cm^2/V.s. The highest peak field effect mobility is observed for the lateral MOSFETs without doing the sacrificial oxide which is about 17 cm^2/V.s. It is also found that the mobility will decrease if the sacrificial oxidation time

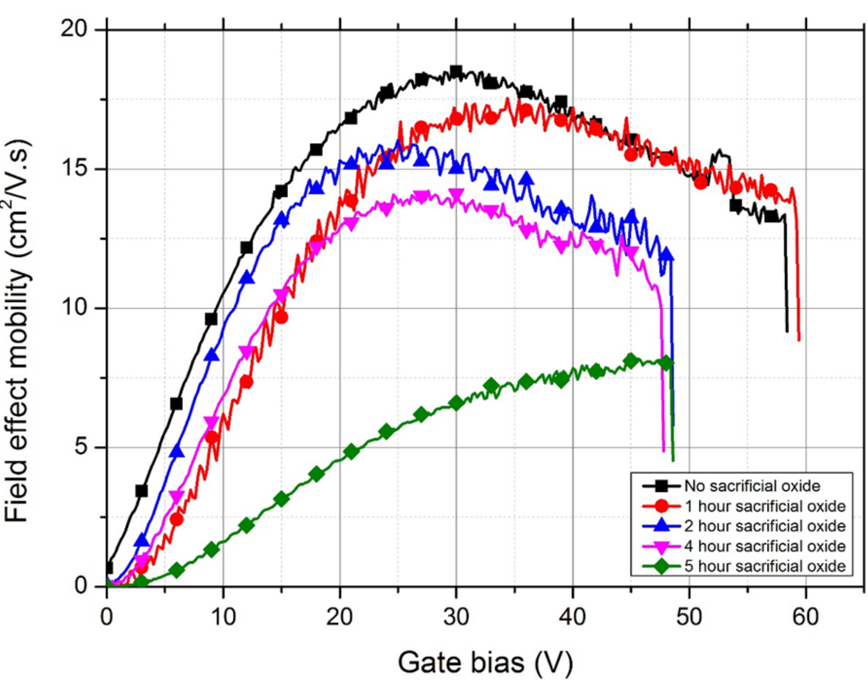


Figure 7.13: Field effect mobility against the gate bias for the 4H-SiC lateral MOSFETs after N_2O POA at 1300°C for 4 hours for different sacrificial oxide thickness.

is increased, which is similar to the MOSFETs without the N_2O POA as shown in Figure 7.11. These results show that N_2O POA at 1300°C for 4 hours is effective in increasing the field effect mobility of the lateral MOSFETs, which is corresponding to the reduction of D_{it} between the SiO_2/SiC as discussed in Chapter 6. It is also seen that although the N_2O POA at 1300°C for 4 hours can greatly increase the field effect mobility, it is still limited by the thickness of the sacrificial oxide grown on the 4H-SiC. Therefore, the sacrificial oxide process was not employed in the fabrication of MOSFETs in this work.

The novel phosphorous passivation technique which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) was also used to fabricate the lateral MOSFETs. Two batches of lateral MOSFETs were fabricated separately at different time and without

using sacrificial oxide process. The first batch of lateral MOSFETs were fabricated with three different post oxidation annealing conditions: the standard thermal oxidation at 1400°C for 1 hour, the N_2O POA at 1300°C for 4 hours and the phosphorous POA at 1000C for 2 hours after the standard thermal oxidation process. The second batch of lateral MOSFETs was fabricated similarly to the first batch of lateral MOSFETs but with the combined N_2O and phosphorous POA instead of the standard thermal oxidation at 1400°C for 1 hour condition. Figure 7.14 shows the field effect mobility and the drain current against the gate bias for the first batch of lateral MOSFETs, and Figure 7.15 shows the similar curves for the second batch of lateral MOSFETs.

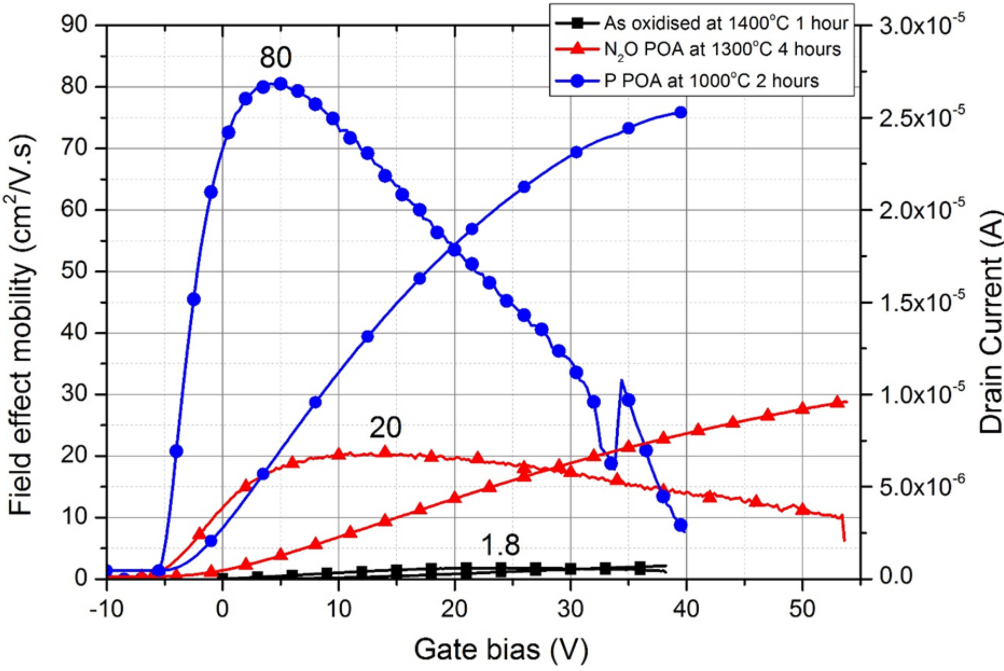


Figure 7.14: Field effect mobility and the drain current against the gate bias for the first batch of lateral MOSFETs.

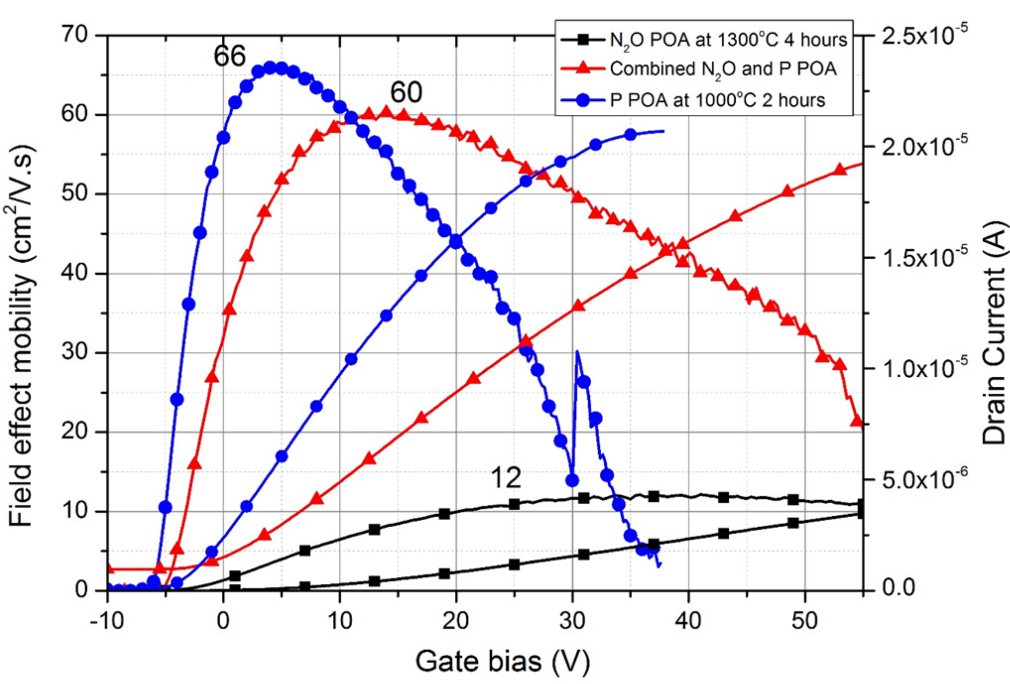


Figure 7.15: Field effect mobility and the drain current against the gate bias for the second batch of lateral MOSFETs.

From Figure 7.13 it is seen that the lateral MOSFETs with N_2O POA at 1300°C for 4 hours had a peak field effect mobility of 20 cm^2/V.s and the peak field effect mobility of 80 cm^2/V.s was obtained after the phosphorous POA at 1000°C for 2 hours, which is the highest field effect mobility seen so far on the implanted p-body region of 4H-SiC (0001) MOSFETs similar to those reported by Sharma [31] on lateral MOSFETs with epitaxial grown p-body region. Compare to the single digit field effect mobility (1.8 cm^2/V.s) for the MOSFETs fabricated at 1400°C for 1 hour without post oxidation annealing, the phosphorous POA technique can dramatically increase the field effect mobility which is almost 50 times higher in peak field effect mobility. The phosphosilicate glass (PSG) which converted from the SiO_2 after the phosphorous passivation have demonstrated

its superiority in reducing interface traps compare to the N_2O or NO POA techniques as discussed in Chapter 6 and in [31]. N_2O POA technique also shows a significant improvement in field effect mobility which is about 20 $cm^2/V.s$.

For the second batch of lateral MOSFETs as shown in Figure 7.15, it is seen that both the N2O POA at 1300°C for 4 hours and the phosphorous POA at 1000°C for 2 hours result lower field effect mobility than the first batch of lateral MOSFETs under the same POA conditions as shown in Figure 7.14. The reason for these differences are not clear, but could be due to many different factors such as the cleanliness of samples before high temperature gate oxidation and the conditions of the high temperature oxidation furnace after prolonged usage. Nevertheless, the trend of improvement in the field effect mobility after the phosphorous POA at 1000°C for 2 hours compare to the N_2O POA at 1300°C for 4 hours is the same as those in the first batch of lateral MOSFETs. It is also noticed that the combined N_2O and phosphorous POA technique did not show further improvement in the field effect mobility but rather has a lower field effect mobility than the phosphorous POA at 1000°C for 2 hours, which is similar to their corresponding interface traps density results as shown in Figure 6.16 in Chapter 6.

The only drawback, however, from Figure 7.14 and Figure 7.15 is that negative threshold voltage (~ -5 V) after the post oxidation annealing. The negative threshold voltage means that the device is normally-on which is not ideal for the application point of view. The reduction of threshold voltage is due to the positive charge within the oxide or the interface between the SiO_2/SiC. The threshold voltage will shift if the device is measured

under bias temperature stress as discussed in [53] for the phosphorous passivated 4H-SiC MOSFETs. The negative threshold voltage and its instability under temperature stress problems can be solved by using a thin layer of SiO_2 which converted into PSG and then capped by a thick SiO_2 layer as reported in [31]. Another way to shift the threshold voltage to positive is to use a thicker SiO_2 layer and reduce the phosphorous annealing time.

7.4.3 Oxide Breakdown Electric Field

Oxide breakdown tests were also carried out on the lateral MOSFETs with both N_2O and phosphorous POAs. Figure 7.16 shows the gate leakage current density against the oxide electric field for the 4H-SiC lateral MOSFETs with different POA conditions. The breakdown tests were set up by connecting the source and drain together with Vds =0 V to make sure the device is off before biasing with positive gate voltage until the gate leakage current exceed the compliance limit of 10 mA. From Figure 7.16 it is seen that the breakdown electric field density for the lateral MOSFETs with N_2O POA at 1300°C for 4 hours and phosphorous POA at 1000°C for 2 hours are all above 10 MV/cm at room temperature. There is no significant reduction in terms of oxide breakdown field after the N_2O and phosphorous POA. The MOSFETs with phosphorous POA show even higher oxide breakdown field than the MOSFETs as oxidised at 1400°C for 1 hour without POA, which is about 13 MV/cm although its leakage current at the oxide electric field less than

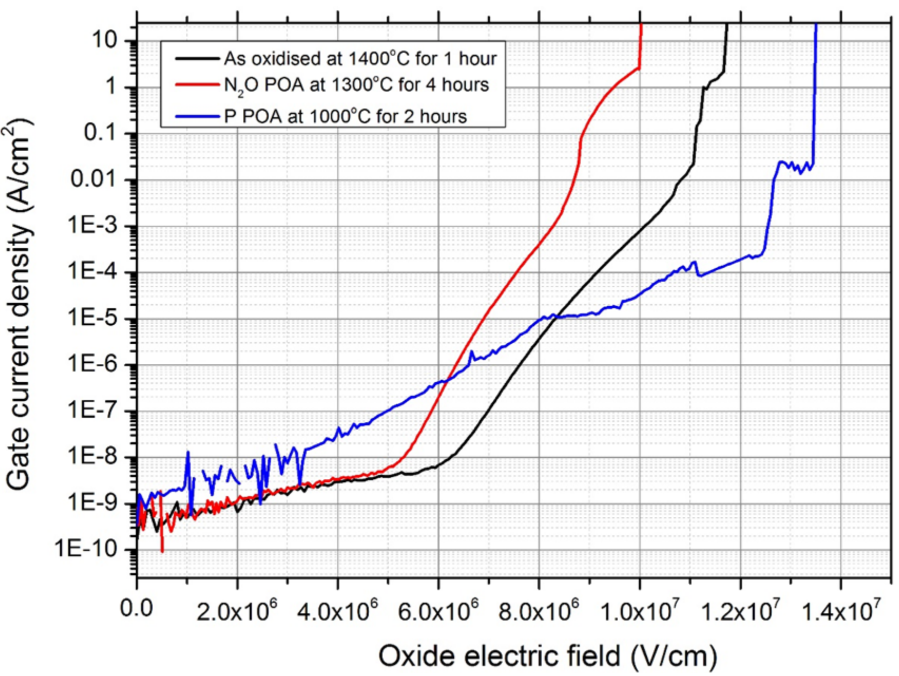


Figure 7.16: Gate current density versus oxide electric field for the lateral MOSFETs with different POA conditions.

6 MV/cm is slightly higher than the lateral MOSFETs without POA and with the N_2O POA.

7.5 Temperature Dependence of the Field Effect Mobility

In order to better understand the mechanism governing the carrier transport in the 4H-SiC MOSFETs, the temperature dependence of the field effective mobility in the 4H-SiC have been studied. In this work, lateral MOSFETs measurements were also performed under different temperatures ranging from 300 K to 500 K. Temperature variation measurement

were carried out using our variable temperature probe station as shown in Figure 7.17. Figure 7.18 and Figure 7.19 show the field effect mobility versus the gate bias for the lateral MOSFETs with phosphorous POA and N_2O POA under different temperatures. It is seen that as the temperature increases the threshold voltage will decrease as expected due to the increase in the intrinsic carrier concentration [44].

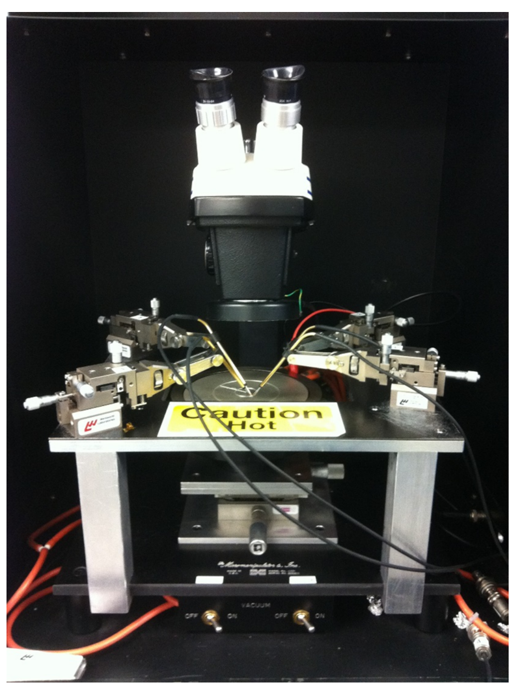


Figure 7.17: Variable temperature probe station set up in the clean room.

From Figure 7.18 and Figure 7.19, it is seen that the lateral MOSFETs without POA and with N_2O POA have their channel mobility directly proportional to the measurement temperatures, however, the channel mobility is inversely proportional to the measurement temperature for the lateral MOSFETs with the phosphorous POA. The field effect mobility as a function of the temperature for 4H-SiC MOSFETs fabricated using different

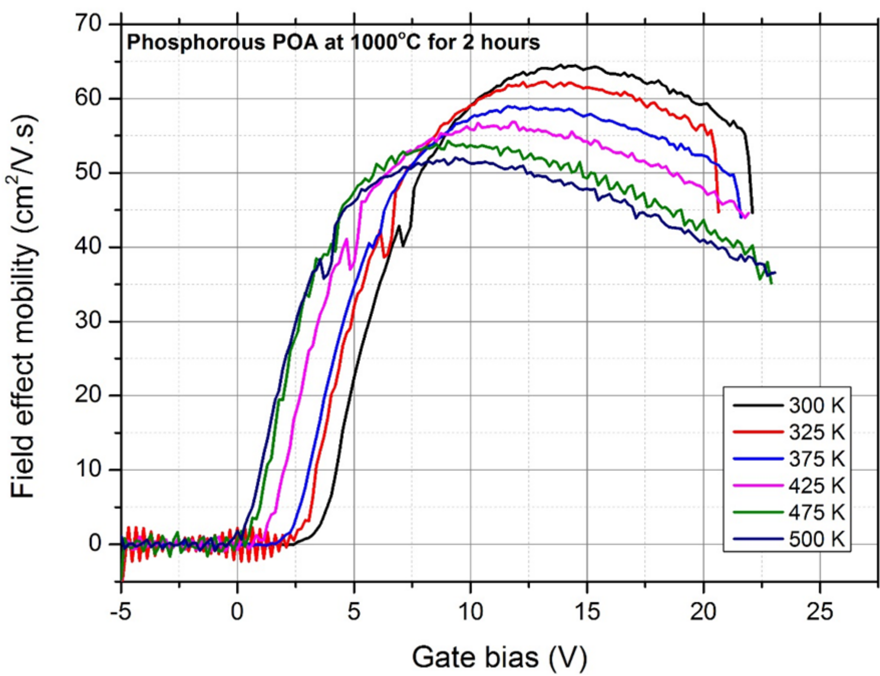


Figure 7.18: Field effect mobility versus the gate bias for the lateral MOSFETs with phosphorous POA at 1000°C for 2 hours under different temperatures.

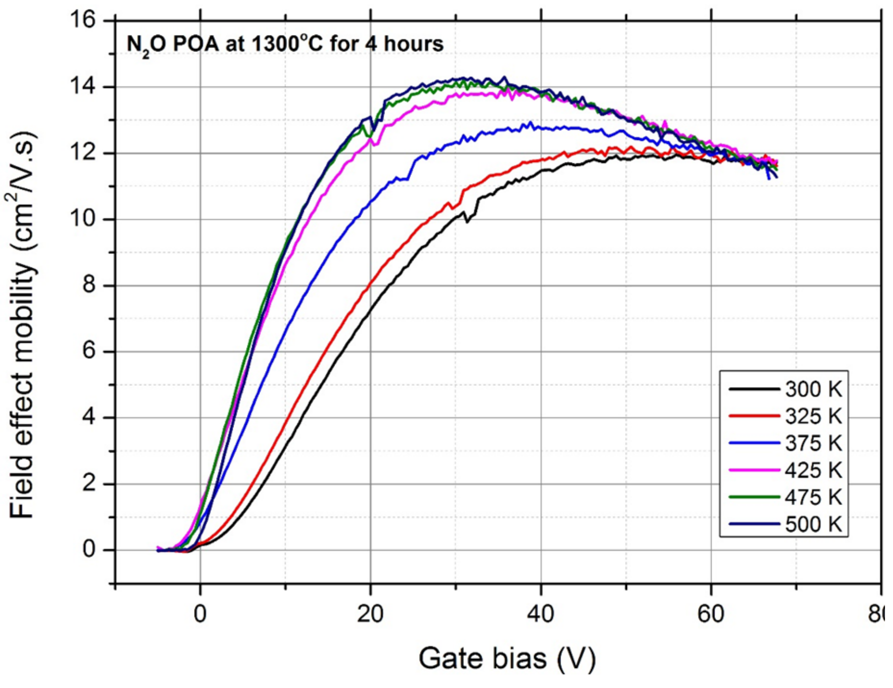


Figure 7.19: Field effect mobility versus the gate bias for the lateral MOSFETs with N_2O POA at 1300°C for 4 hours under different temperatures.

passivation techniques are summarised in Figure 7.20. Both passivation processes have been demonstrated to be effective in improving the channel mobility of 4H-SiC MOSFETs and lowering of the interface trap density. In particular, passivation using phosphorous diffusion source has been found to be able to achieve peak channel mobility of about 70 cm^2/V.s for implanted P-body 4H-SiC MOSFETs on (0001) Si face, which is almost three times more than the values obtained from N_2O annealing.

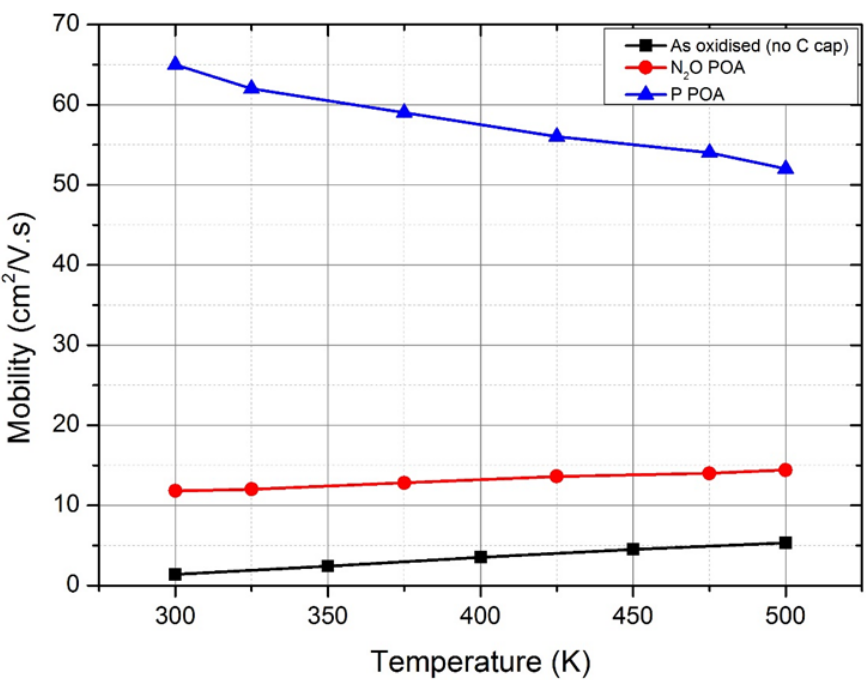


Figure 7.20: Temperature dependence of the field effect mobility for the 4H-SiC MOSFETs with no POA, N_2O POA and phosphorous POA treatments.

The temperature dependence of channel mobility is dominated by two factors: phonon scattering and ionised impurity scattering (also called Coulomb scattering). As the temperature increases, thermal vibrations (phonons) within a semiconductor increase and

caused increased scattering, which results in a decrease of channel mobility. For the effect of Coulomb scattering, however, decreases with increasing temperature due to the average thermal speed of the carriers being higher. The carriers spend less time near an ionised impurity as they pass and the scattering effect is thus reduced, therefore channel mobility is increased. From the experimental data shown in Figure 7.20, it is seen that sample without POA and sample with N_2O POA show similar trend which the channel mobility increases with the temperature, this suggests that carrier transport in the channel is governed by Coulomb scattering. On the other hand, the phosphorus POA sample shows opposite trend, which the channel mobility decrease with increase of temperature. This shows that phonon scattering dominates over the other scattering phenomena in the case of phosphorus POA.

The channel mobility being independent of the surface morphology is explained by the positive temperature coefficient of the channel mobility as discussed in [69], which indicates that the Coulomb scattering plays the key role in the limitation of the channel mobility, independent of the surface morphology. It is also observed that after nitridation process of the gate oxide in N_2O, irrespective of the interface roughness originating by post-implantation annealing, the MOSFET channel mobility increases with the temperature due to the dominant effect of Coulomb scattering. For this reason and the ease of fabrication, the carbon capping layer was not used on the MOSFETs fabrication in this work.

7.6 Summary

In this Chapter, the fabrication and characterisation of 4H-SiC lateral MOSFETs have been presented. After outlining the details of the photomask design and the fabrication processes of the 4H-SiC lateral MOSFETs, the electrical characterisation results for the 4H-SiC MOSFETs with different oxidation and passivation conditions are given, which follows the chronological evolution of these devices.

The first generation 4H-SiC lateral MOSFETs were fabricated with box-like p-body doping profile with total doping concentration of 1×10^{18} cm^{-3}. The effect of different implant activation temperatures on the channel mobility has been investigated. It is found that implant activation annealing temperature at 1600°C for 45 minutes is sufficient for activating both n-type and p-type dopants in the 4H-SiC MOSFETs, there is little difference in terms of field effect mobility between the MOSFETs activated at 1600°C for 45 minutes and at 1650°C for 1 hour, which is about 1.2 cm^2/V.s as shown Figure ??. In order to increase the channel mobility of the 4H-SiC lateral MOSFETs, the high temperature oxidation (1500°C) and the N_2O post oxidation techniques were investigated. Although the enhanced oxidation rate at high temperature may reduce the interface states at the 4H-SiC/SiO_2 interface as reported in [83], the difference between the peak field effect mobility for lateral MOSFETs oxidised at 1400°C for 1 hour and at 1500°C for 30 minutes is very small. N_2O nitridation, both annealing of thermally grown oxides and direct growth in N_2O have been investigated. 1300°C for 4 hours nitridation has found to

be the most effective in increasing the field effect channel mobility and reducing threshold voltage of 4H-SiC MOSFETs. The highest field effect mobility was found at the N_2O direct growth oxide at 1300°C for 4 hours, which is about 19 $cm^2/V.s$. It also results the lowest threshold voltage compare to other N_2O POA conditions due to the reduction in negative trapped charge density near the SiO_2/SiC interface and the exposure of positive oxide charge [33]. Compared to the corresponding interface trap density results from 4H-SiC MOS capacitor as shown in Chapter 6, it can be seen that in general, lower the interface trap density will result in higher field effect mobility for the 4H-SiC MOSFETs.

The second generation 4H-SiC lateral MOSFETs were fabricated with retrograde p-body doping profile, which is the same doping profile used on the vertical power MOSFETs to form as a P+ shielding region as discussed Chapter 3. The impact of sacrificial oxide thickness on channel mobility of the lateral MOSFETs was investigated. It was found that the thinner the sacrificial oxide had the better field effect mobility of the MOSFETs, and lateral MOSFETs fabricated without the sacrificial oxide have the highest peak field effect mobility. Similar trends were also observed for the lateral MOSFETs with N_2O POA at 1300°C for 4 hours, which the highest field effect mobility is observed for the lateral MOSFETs without the sacrificial oxide. The novel phosphorous passivation technique which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) was also used to fabricate the lateral MOSFETs. Results show that the peak field effect mobility of approximately 80 $cm^2/V.s$ was obtained after the phosphorous POA at 1000°C for 2 hours, which is the highest field effect mobility seen so far on the implanted P-body

region of 4H-SiC (0001) MOSFETs. SiO_2 is converted to the phosphosilicate glass (PSG) after the phosphorous passivation, which can successfully passivate most of the interface trap charges as shown in Chapter 6 and dramatically increase the field effect mobility of the 4H-SiC lateral MOSFETs. The combined N_2O and phosphorous POA technique was also investigated. Results show that it has smaller peak field effect mobility than the phosphorous POA but has higher field effect mobility than the N_2O POA, which corresponding to their D_{it} results from the MOS capacitors as discussed in Chapter 6. The only drawback, however, is the negative threshold voltage (~ -5 V) after the phosphorous POA at 1000°C for 2 hours, which means that the devices would be normally-on devices. The reduction of threshold voltage is due to the positive charge within the oxide or in the interface between the SiO_2/SiC. It is also observed that the threshold voltage and channel mobility reduce with increase of measurement temperature due to the increase in the intrinsic carrier concentration.

Finally, the oxide breakdown measurements at room temperature on the lateral MOSFETs with different post oxidation conditions were carried out to check their oxide reliability. The oxide breakdown fields are all above 10 MV/cm for MOSFETs with both N_2O POA and phosphorous POA. No degradation of oxide quality has been observed for the MOSFET with phosphorous POA, although the leakage current is slightly higher than the MOSFET with N_2O POA and without POA at the oxide electric field less than 6 MV/cm, the MOSFETs with phosphorous POA at 1000°C for 2 hours have the highest oxide breakdown field.

Chapter 8 Fabrication and Characterisation of 4H-SiC Vertical MOSFETs

Following the fabrication and characterisation of 4H-SiC lateral MOSFETs, vertical MOSFETs designed for blocking high voltage are presented in this Chapter. Firstly, the details of the mask design, the 4H-SiC material used and the different MOSFET cell structures are presented. Following this, the discussion of fabrication process and the electrical characterisation results for the 4H-SiC vertical MOSFETs is given, which follows the chronological evolution of these devices as with Chapter 7. First generation device were fabricated on a 10 μm thick n-type epitaxial layer with the gate oxide grown at standard thermal oxidation at 1400°C for 1 hour. SIMS analysis has been used to determine the doping profiles of the vertical MOSFETs. Forward characteristics of the fabricated vertical MOSFETs were measured and compared with the simulation values. Second generation devices were fabricated on a 30 μm thick n-type epitaxial layer, and used the N_2O POA at 1300°C for 4 hours on the pre-grown gate oxide to improve the channel mobility

and to increase the output current.

8.1 Photomask Design

The design of the vertical MOSFET mask set is much more complicated than for the lateral devices shown in Chapter 7. This is because there are more implantation and etching steps involved for the vertical MOSFET. In total, there are 12 masks involved in the design, which are

- Alignment marks
- P-well implantation
- JFET implantation
- Source implantation
- P+ implantation
- JTE implantation
- Gate oxide window
- Source contact window
- Source metal
- Gate metal

- Contact pad
- Edge bead

As with the lateral MOSFET design show in Chapter 7, the mask plates were designed using the Tanner Tools L-Edit software and were manufactured at Compugraphics, UK. There are two different die designs across the three inch wafer mask, and both dies have the same dimension of 16 × 16 mm. One of the die is a vertical MOSFETs with 2 μm channel length which were placed on the left half of the three inch wafer mask, and the second die design was for vertical MOSFETs with 5 μm channel length which were placed on the right half of the three inch wafer mask as shown in Figure 8.1. Figure 8.2 and Figure 8.3 shows the die designs for vertical MOSFETs with 2 μm and 5 μm channel lengths.

As seen from Figure 8.2 and Figure 8.3 there are a range of sizes of vertical MOSFETs, which correspond to different current rating of the devices. Vertical MOSFETs were designed from 0.1 A to 1 A current output, and a high current is achieved by connecting many single cell MOSFETs in parallel. For the 2 μm channel vertical MOSFETs, two different sizes of single cells were designed. The small single cell has cell pitch dimensions of 31 × 310 μm and the longer single cell has cell pitch dimensions of 31 × 950 μm. The 0.1 A current device consists of 18 small single cells and the 1 A current device consists of 58 large single cells. For the 5 μm channel vertical MOSFETs, the small single cell is designed with pitch area of 37 × 310 μm and the longer single cell is designed with

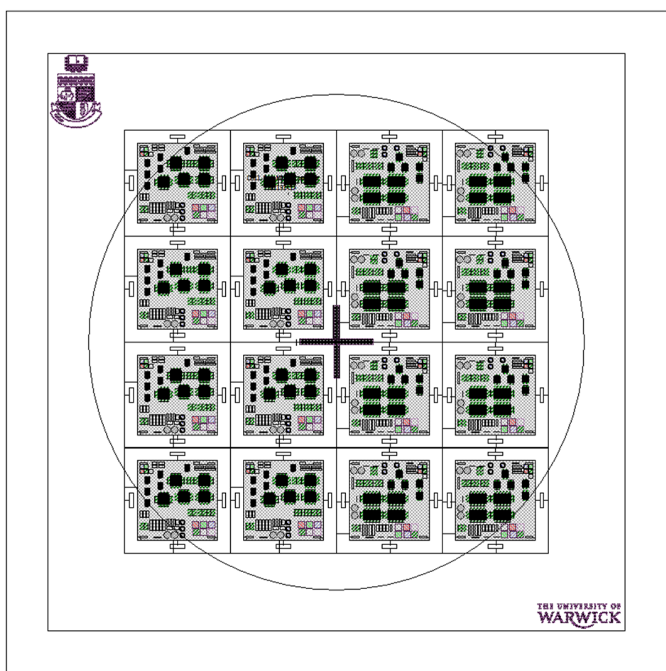


Figure 8.1: Mask plate design overview of the vertical MOSFETs.

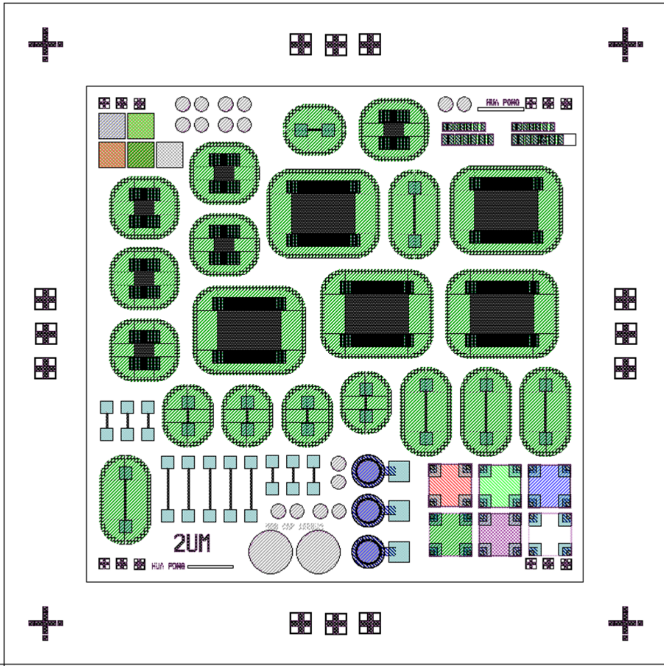


Figure 8.2: Die design for the vertical MOSFETs with 2 μm channel length

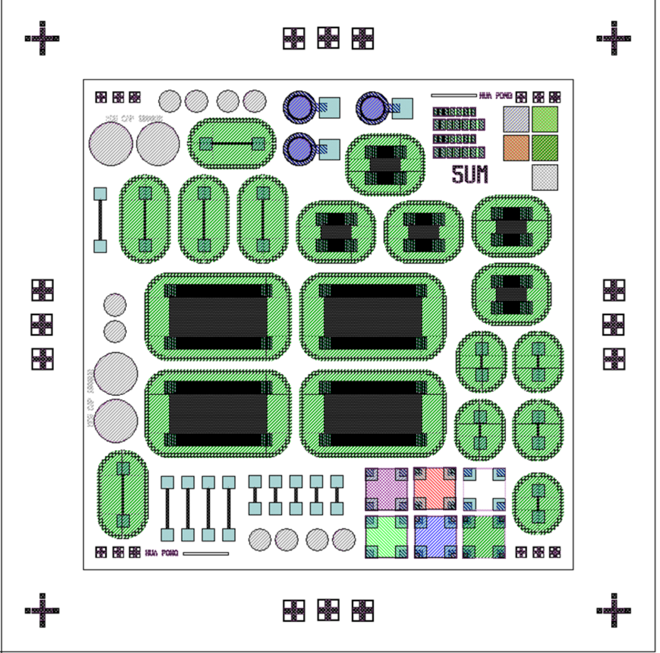


Figure 8.3: Die design for the vertical MOSFETs with 5 μm channel length

pitch area of 37 $\times$ 950 μm. The 0.1 A current device consists of 23 small single cells and the 1 A current device consist of 74 longer single cells. In both 2 μm and 5 μm channel MOSFETs designs, the small single cell has cell length of 310 μm and the longer single cell has cell length of 950 μm, which in theory the current of longer single cell is about three times larger than the current of small single cell. The mask design also consist of other test structures such as MOS capacitor, TLM structures, Van der Pauw and SIMS test structures as shown in Figure 8.2 and Figure 8.3.

8.2 Fabrication Process

The 4H-SiC material used to fabricate vertical MOSFETs were also obtained from Nortstel AB [137]. Epitaxial layer thickness and doping concentration are 10 μm and 2×10^{16} cm^{-3} for the first generation of lateral MOSFETs. For the second generation of vertical MOSFETs, epitaxial layer thickness and doping centration are 30 μm and 4×10^{15} cm^{-3} respectively. Four inch wafers were laser-cut into 4 quarters for processing until the ion-implantations have finished, which then laser-cut into 16 $\times$ 16 mm for subsequent processing. In this work, the JFET region and the JTE implantations steps for the vertical MOSFETs fabrication were omitted due to the high cost involved for each implantation and time limitation.

Details of vertical MOSFETs fabrication process flow with cross sectional diagrams are outlined in Appendix A. The cleaning and implantation processes are similar to the lateral MOSFET fabrication as discussed previously in Chapter 7. After all the ion implantation were completed, wafers were laser-cut into 16 $\times$ 16 mm chips and followed by removing TEOS oxide in HF and then annealed at 1650°C for 45 minutes to activate the implant species. Following this, samples were cleaned using the standard SiC cleaning process as outlined in Appendix B and 1 μm of TEOS oxide was deposited on SiC surface as the field oxide layer. Standard photolithography process with S1818 photoresist was used to pattern the gate oxide region, and the exposed TEOS oxide were etched using the RIE program in the ICP etcher as discussed in Chapter 5. After the oxide etching, samples

were loaded into the high temperature oxidation furnace to grown approximately 50nm gate oxide at 1400°C for 1 hour. N_2O POA at 1300°C for 4 hour was also performed after the gate oxide grown for the second generation of vertical MOSFETs. After gate oxide grown, source contact regions were patterned using the standard photolithography process with S1818 photoresist and the exposed oxide were etched in the ICP etcher. Following this, a thicker photoresist (AZ9260) with different photolithography process as outlined in Appendix C was used to pattern the source metal region. Ti and Ni of 30 nm and 100 nm were evaporated onto the samples and the unwanted metals and photoresist were then removed via an ultrasonic lift-off process in acetone. After this, the back oxide of samples were removed in the ICP etcher using the RIE process, which followed by evaporate Ti and Ni of 30 nm and 100 nm again to form the drain contact of the vertical MOSFETs. Samples were then loaded into the rapid thermal annealing (RTA) furnace and anneal at 1000°C for 2 minutes in an argon atmosphere to form the ohmic contacts for both source and drain of the vertical MOSFETs. Next, the gate contact region of the vertical MOSFETs were patterned using the AZ9260 photoresist again, following which a layer of 500 nm thick aluminium was evaporated on the samples to form the gate contact metal. The unwanted aluminium and photoresist were then removed via an ultrasonic lift-off process in acetone. Finally, the contact pad region was patterned using the standard photolithography process with S1818 photoresist, and a layer of 1 μm thick aluminium was evaporated on the samples to form the contact pad for both gate and source of vertical MOSFETs. The lift-off process was used to remove the unwanted aluminium and

photoresist. Figure 8.4 and Figure 8.5 show the fabricated single finger and multi-fingers vertical MOSFETs.

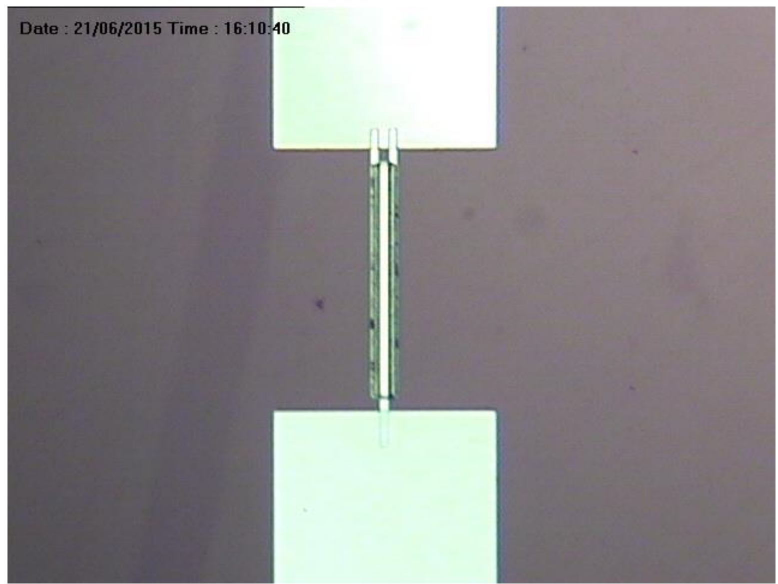


Figure 8.4: Fabricated SiC single finger vertical MOSFETs.

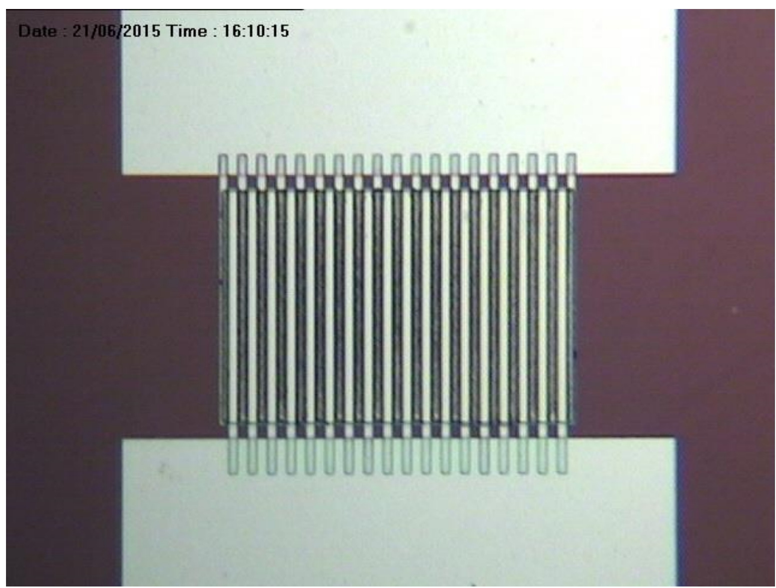


Figure 8.5: Fabricated SiC multi-fingers vertical MOSFETs.

8.2.1 Challenges in the Fabrication Process

One of greatest challenges in fabricating the vertical MOSFETs is to accurately align the photomasks onto the sample due to the small feature size and the long finger MOSFET structure design. Since the smallest feature for the alignment is 2 μm on the photo mask, which is difficult to align accurately by using the conventional Karl Suss MJB3 mask aligner as shown in Figure 5.14 in Chapter 5, a new mask aligner which provides higher precision was therefore required for the fabrication of vertical MOSFETs. SUSS MicroTec MA/BA8 mask aligner as show in Figure 8.6, which is recently bought by our research group is capable of patterning structures below 0.5 μm with high resolution optics [148].

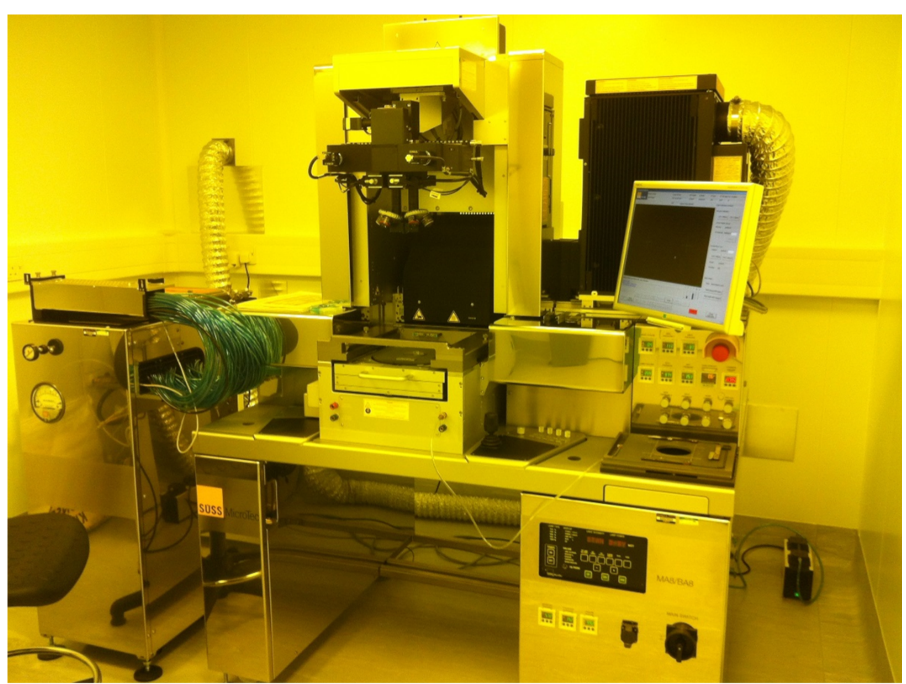


Figure 8.6: Suss MicroTec MA/BA8 mask aligner.

Although alignment accuracy is much better with the use of new MA/BA8 mask

aligner, as the number mask layer increases the chances of getting misalignment also increases. It is therefore important to design the alignment marks such that each subsequent layer is aligned to the first layer of the alignment marks without any other material in between (such as TEOS oxide and metals). Figure 8.7 shows the smallest alignment mark with gap of 2 μm before the P-well implantation and Figure 8.8 shows the same alignment mark after the P+ implantation with TEOS oxide.

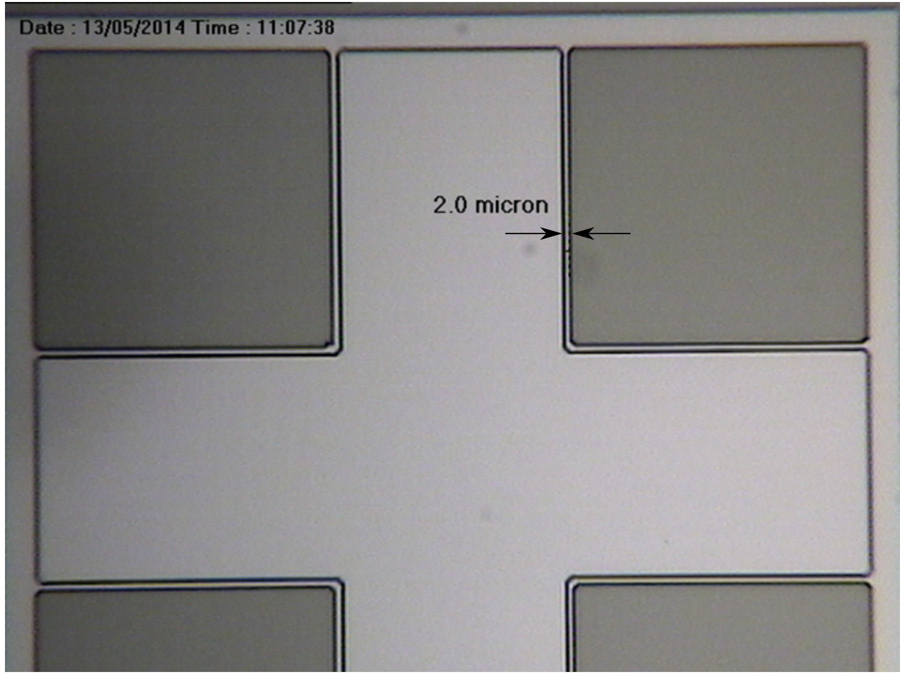


Figure 8.7: Alignment mark with gap of 2 μm before the P-well implantation.

From Figure 8.7 it is seen that the alignment mark is clearly visible and almost perfectly aligned before it was sent away for implantation, however, after been through few processing steps with different mask layers, at the end of the P+ implantations without removing the TEOS layer the alignment mark become harder to see clearly on the

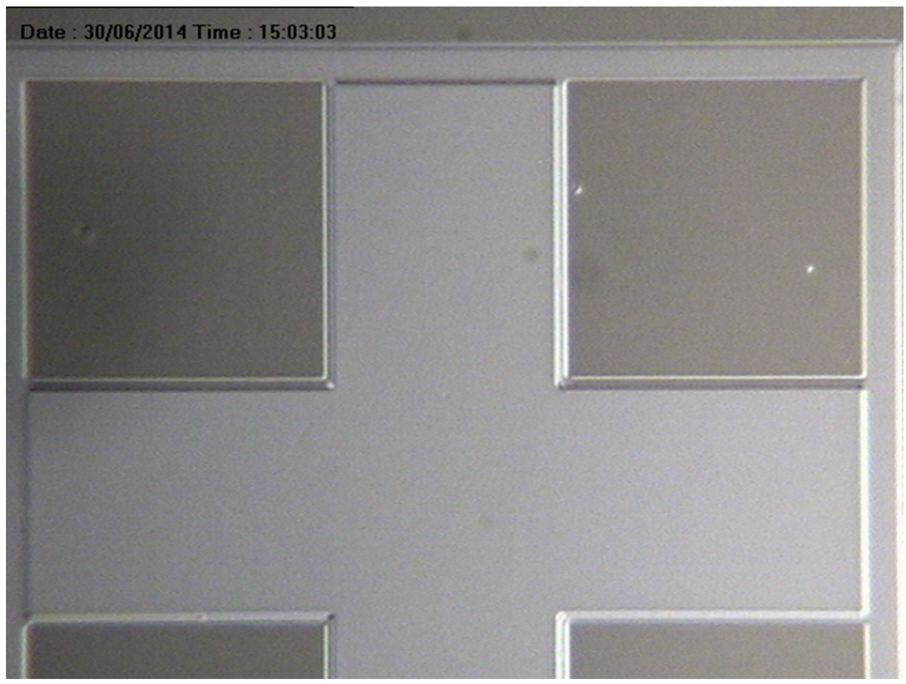


Figure 8.8: Alignment mark after the P+ implantation with TEOS oxide on top.

edges. This is due to the increased thickness of the sample by the TEOS oxide layer, and misalignment is likely to happen because of this. Figure 8.9 shows an example of small misalignment of multi fingers vertical MOSFETs between the gate and source metal, which cause the device not to work. Figure 8.10 shows multi fingers vertical MOSFETs without misalignment between the gate and source metals. It was found that one of the main causes of failure was contact between the gate and the source metals as shown in Figure 8.9. Therefore, in order to fabricate a working vertical MOSFET each fabrication step has to be carefully cleaned and aligned before any etching or metals deposition takes place.

Another challenge in the fabrication of vertical MOSFETs is to effectively develop the

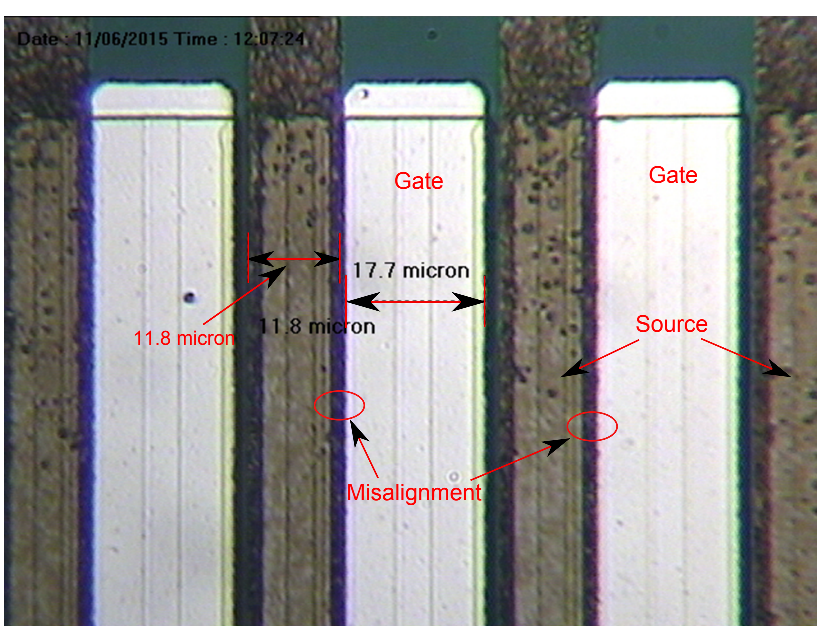


Figure 8.9: Small misalignment of multi fingers vertical MOSFETs after the lift-off process, which shows the source metal (grey colour) in contact with the gate metal (white colour).

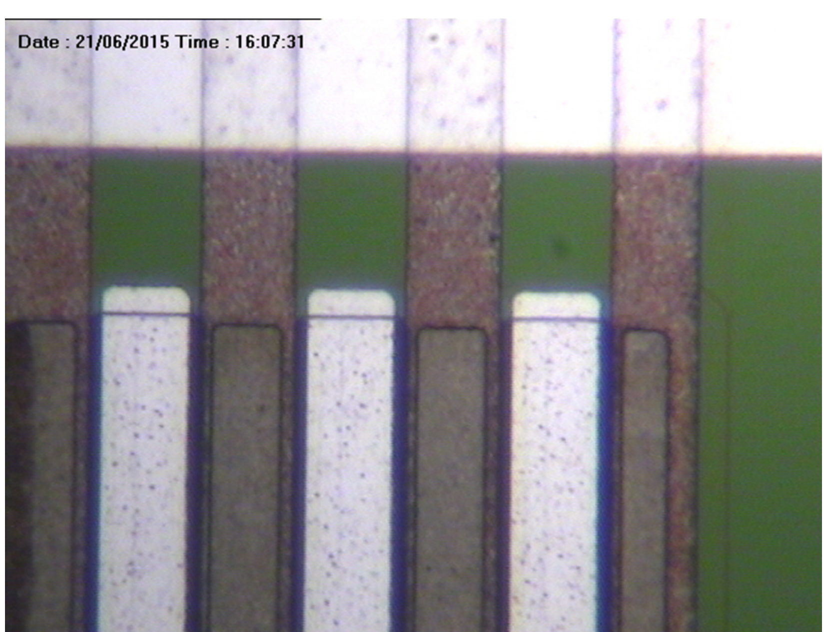
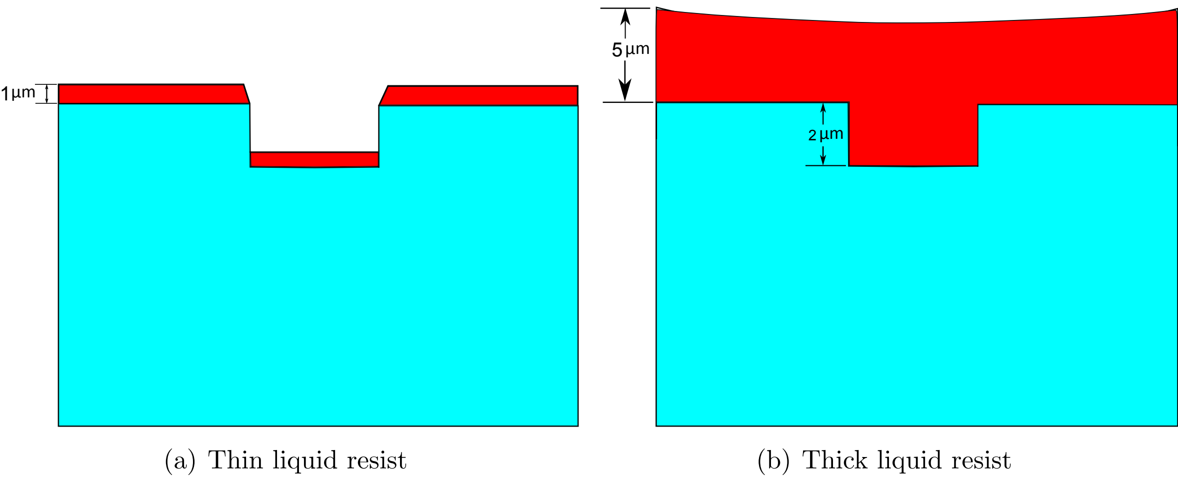


Figure 8.10: Multi fingers vertical MOSFETs without misalignment between the source (grey colour) and the gate (white colour) metals.

photoresist in the narrow and deep trench part of the structure without causing striations or over-development of the sidewalls. The standard photolithography process using S1818 photoresist as outlined in Appendix C has a thickness of about 1.8 μm with single layer coating, which is too thin to cover the edges at the trench boundary. On the other hand, if a very thick photoresist is used, it is difficult to develop it in the deep trench. Figure 8.11 illustrates the schematic view of photoresist pattern in the deep trench with a thin photoresist and a thick resist. Figure 8.12 shows the vertical MOSFET patterned using our standard photolithography process using S1818 photoresist. It can be seen that the S1818 photoresist in the trenches was not fully developed and some photoresist is left on the sidewalls of the trenches. The undeveloped photoresist left on the sidewalls will cause any deposited metal to peel off from the surface after the metal depositions and lift-off process as shown in Figure 8.13. To overcome this problem, a different type of photoresist and lithography process was developed in this work. A thicker photoresist of AZ9260 ($\sim$5 μm) with faster spinning speed and longer spin time to give a thinner layer photolithography process was used. Details of the AZ9260 photolithography process is discussed in Appendix C.

Apart from the fabrication challenges mentioned above, material defects will also cause failures of the devices. Figure 8.14 shows the typical defect seen on the 4H-SiC materials used in this work. It is not clear what kind of defect exactly and how they were formed but it is believe to be a micropipe defect which is common in SiC crystals and it is one of the major factors limiting the extent of the successful applications of SiC [149]. On



(a) Thin liquid resist

(b) Thick liquid resist

Figure 8.11: Schematic view of photoresist patterns in the deep trench with (a) thin liquid resist (b) thick liquid resist.

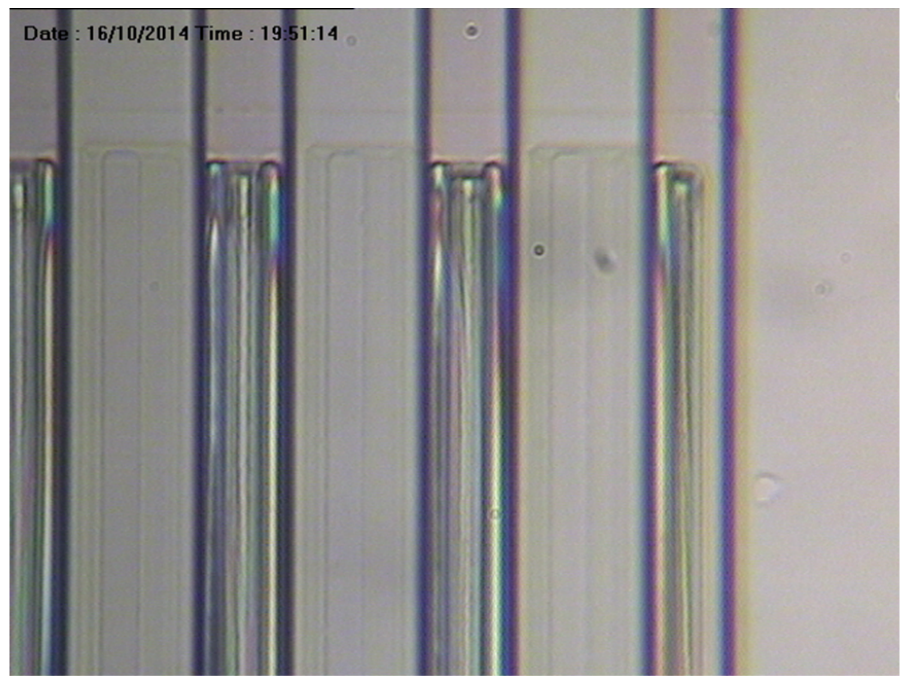


Figure 8.12: Multi fingers vertical MOSFET source metal regions patterned using the standard photolithography process with S1818 photoresist.

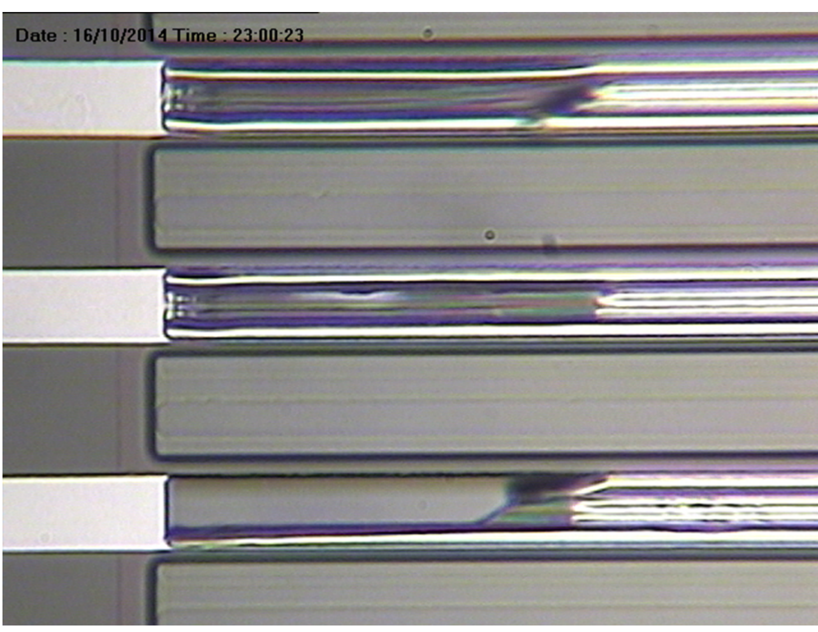


Figure 8.13: Multi fingers vertical MOSFET source metals after lift-off process, which shows the peel off of metals in the trench regions.

average there are about 3 to 4 of this defects on a quarter of a 4 inch SiC wafer obtained from Norstel AB [137], which said to have micropipe density of <1 cm^{-2}.

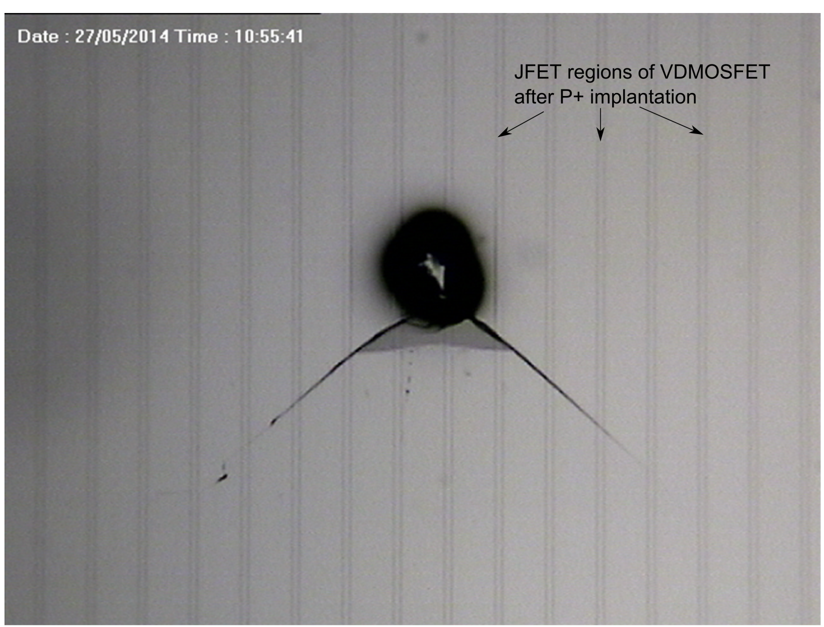


Figure 8.14: Typical defect seen on the 4H-SiC material used in this work.

8.3 First Generation of 4H-SiC Vertical MOSFETs

The first generation 4H-SiC vertical MOSFETs were fabricated on a 10 m thick n-type epitaxial layer with doping concentration of 2×10^{16} cm^{-3}, which is the same material used for the fabrication of lateral MOSFETs as discussed in Chapter 7. Gate oxide were grown at standard thermal oxidation at 1400°C for 1 hour without any post oxidation annealing, which gives an oxide thickness of about 50 nm. The P-body, N+ source and P+ regions doping concentrations are those as shown in Section 7.2 in Chapter 7.

8.3.1 SIMS Analysis

In order to determine the profile of the implanted dopants and to compare with the simulated doping profile, SIMS measurement have been carried out. Figure 8.15 shows the experimental as-implanted aluminium retrograde doping profile compared to the SRIM simulated profile. It can be seen that the experimental SIMS profile is very close to the simulated SRIM profile, except that a higher surface concentration and a more gradual tail. The widening of the measured profile is believed to be caused by the diffusion of Al into the bulk after the annealing process (1600°C for 45 minutes) [118] and may also partially due to the mixing effects from the primary ion beam during SIMS profiling [150]. The physical mechanism behind of the accumulation of Al atoms at the surface is not yet clear. One possible suggestion is that the concentration of Si and C vacancies are generated near the surface by the Al implantation itself. This production of vacancies leads to a steep vacancy gradient, which may force the Al atoms to preferentially migrate to the surface as discussed in [118]. Another possible suggestion which reported by Fisher [13] is because of the a thin (10 nm) layer of Au deposited onto the 4H-SiC when performing the SIMS measurements. This thin layer of Au is used to minimise sample charging issues in order to obtain a constant secondary ion beam current [110]. The Au used was not ultra-pure and is expected to contain some aluminium. The N+ source and P+ regions doping concentrations were shown in Figure 8.16 and Figure 8.17 respectively. It is seen that these two implant profiles exhibited similar deviations from the corresponding

simulated profiles. From figure 8.16 it is seen that the peak doping concentration of the implanted nitrogen doping profile at the surface is slightly lower than the simulated peak doping concentration, which is about 4×10^{19} cm^{-3} instead of 1×10^{20} cm^{-3} from the SRIM simulation, and the nitrogen implants also has longer diffusion tail into bulk of the SiC compare to the aluminium implants.

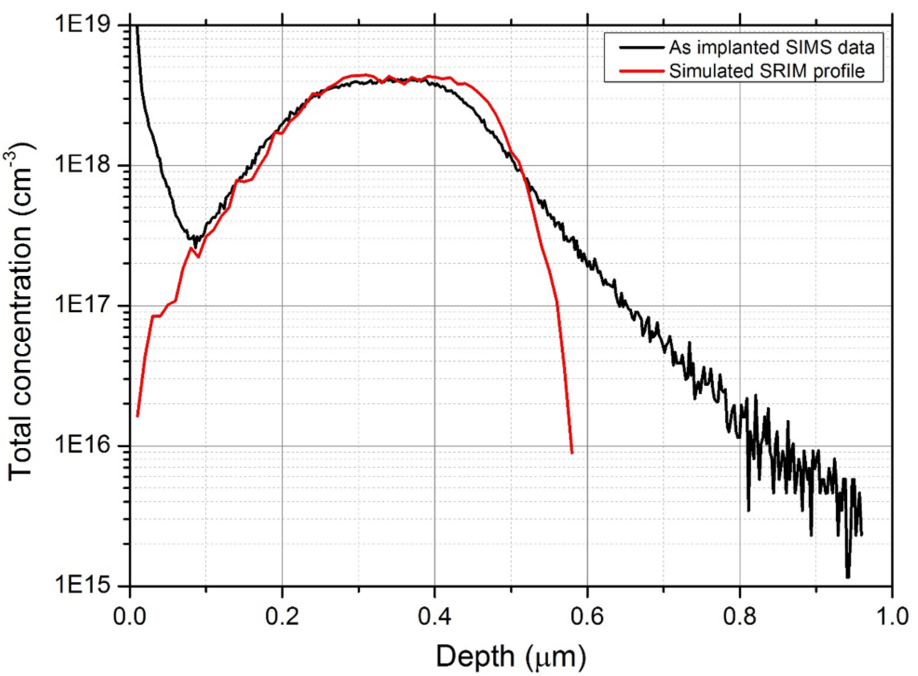


Figure 8.15: Experimental and simulated implanted aluminium retrograde doping profile for P-body region in 4H-SiC.

8.3.2 Forward I-V Characterisation Results

The forward I-V characteristics of the first generation vertical MOSFETs are presented in this Section at room temperature and up to 0.1 A current, which is the current limit of

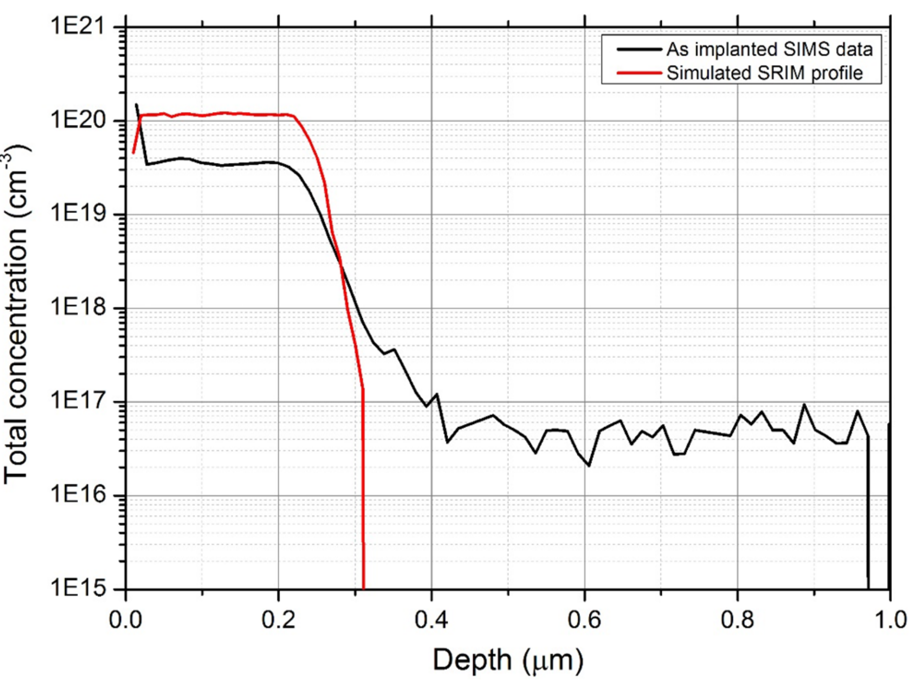


Figure 8.16: Experimental and simulated implanted nitrogen box-like doping profile for N+ source region in 4H-SiC.

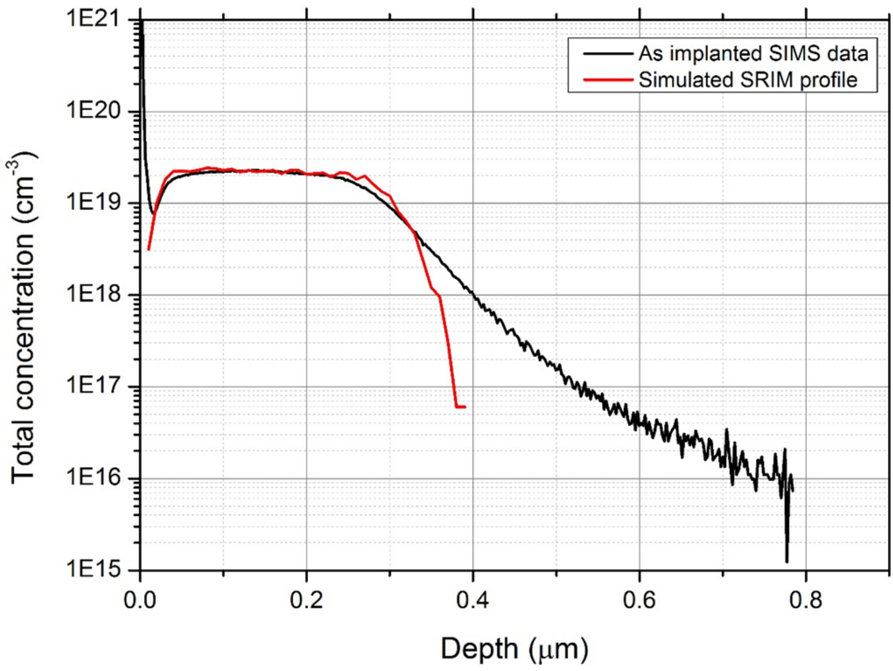


Figure 8.17: Experimental and simulated implanted aluminium box-like doping profile for P+ region in 4H-SiC.

the parameter analyser. The first generation devices are fabricated with gate oxide grown at 1400°C for 1 hour without post oxidation annealing. Figure 8.18 and Figure 8.19 show the output characteristics of both small and longer single cell vertical MOSFETs with 2 μm channel length. It is seen that for the small single cell vertical MOSFET with cell length of 310 μm, the maximum drain current at gate voltage of 20 V is about 7×10^{-6} A. For the longer single cell vertical MOSFET which has cell length of 950 μm, the maximum drain current at gate voltage of 20 V is about 3×10^{-5} A which is about 4 times higher than the small single cell vertical MOSFET. The larger output current is expected from the longer single cell MOSFET due to the much longer cell length. Figure 8.20

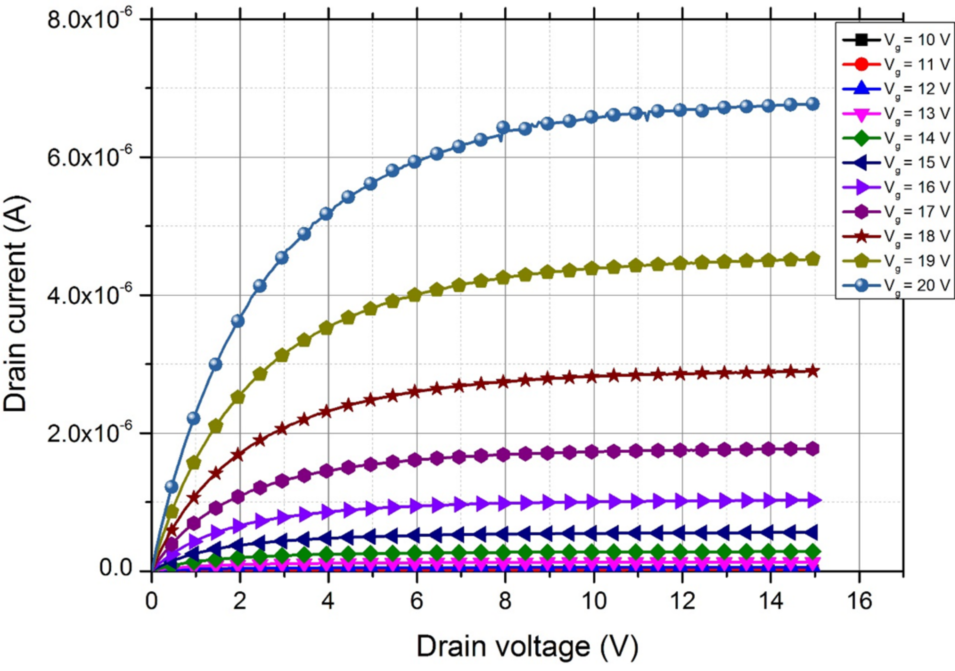


Figure 8.18: Output characteristics of small single cell vertical MOSFETs with 2 μm channel length.

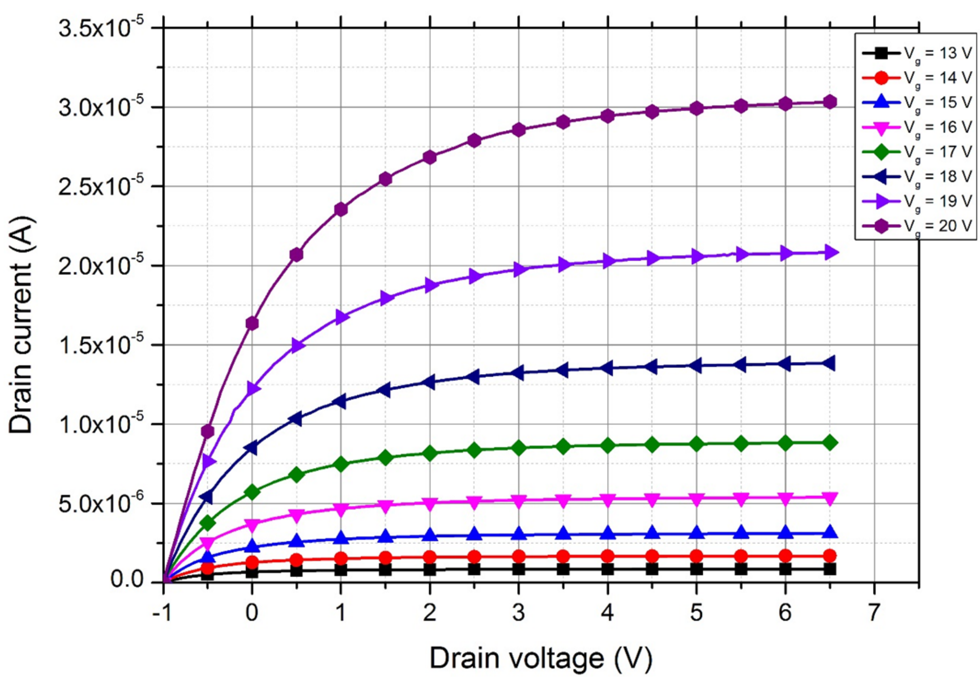


Figure 8.19: Output characteristics of longer single cell vertical MOSFETs with 2 μm channel length.

shows the transfer characteristics of both small and longer single cell vertical MOSFETs at drain voltage of 0.1 V. It is seen that the threshold voltage is about 16 V for both sizes of MOSFETs, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in the Table 7.3 in Chapter 7.

Although most of the single cell MOSFETs were working for the first generation devices, no working devices have been found for the multi-fingers MOSFETs (0.1 A and 1 A devices). The working of single cell MOSFETs indicate that the problem of the devices failure was not due to the misalignment or fabrication process error. The exact cause for the low yield of the multi-fingers vertical MOSFETs is it still not clear, however it is believed that the poor oxide quality could be the problem as the gate oxide area increases

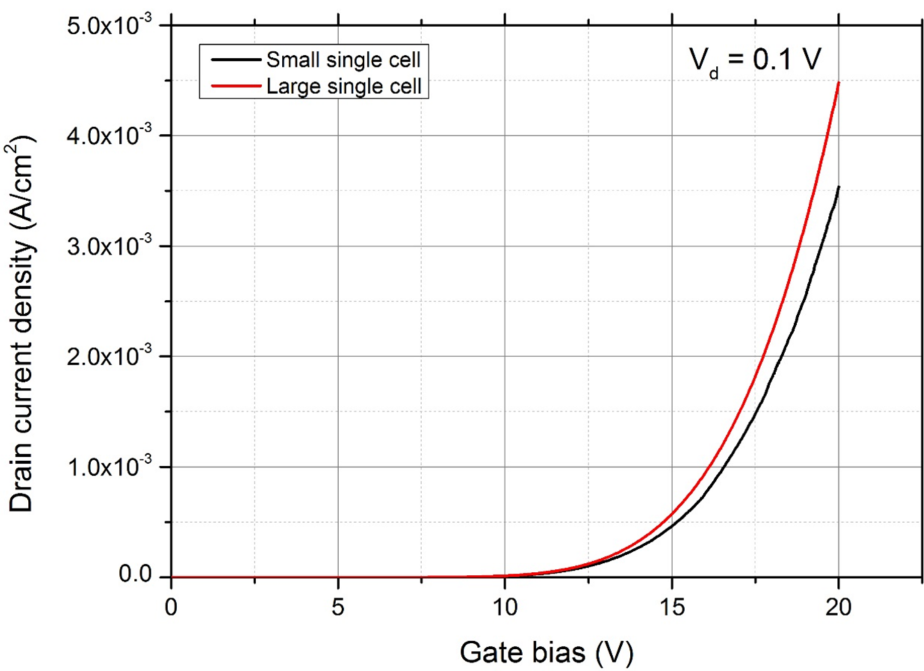


Figure 8.20: Transfer characteristics of single cell vertical MOSFETs with 2 μm channel length.

the chance of having defect in the oxide is increased. Another possible reason for the low yield of the multi-fingers MOSFETs is the defects on the SiC material as discussed in previous Section.

8.4 Second Generation of 4H-SiC Vertical MOSFETs

The second generation 4H-SiC vertical MOSFETs were fabricated on a 30 μm thick n-type epitaxial layer with doping concentration of 4×10^{15} cm^{-3}. Gate oxide were grown at standard thermal oxidation at 1400°C for 1 hour with N_2O post oxidation anneal at 1300°C for 4 hours to improve the channel mobility as discussed in Chapter 7. The P-body, N+ source and P+ regions doping concentrations are same as those used for the

first generation of 4H-SiC vertical MOSFETs as discussed in Section 8.3. In this section, the vertical MOSFETs fabricated using the N_2O post oxidation annealing was examined and compared with those without N_2O POA as shown in Section 8.3.

8.4.1 Forward I-V Characterisation Results

The forward I-V characteristics of the second generation vertical MOSFETs are presented in this Section at room temperature and up to 0.1 A current, which is the current limit of the parameter analyser. Figure 8.21 and Figure 8.22 show the output characteristics of both small and longer single cell vertical MOSFETs with 2 μm channel length after N_2O POA at 1300°C for 4 hours.

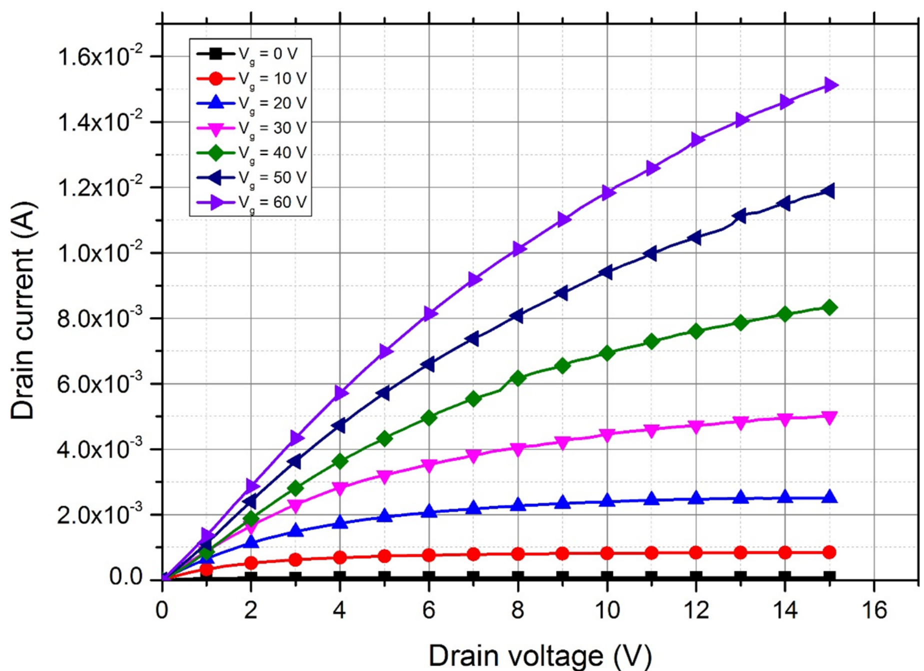


Figure 8.21: Output characteristics of small single cell vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours.

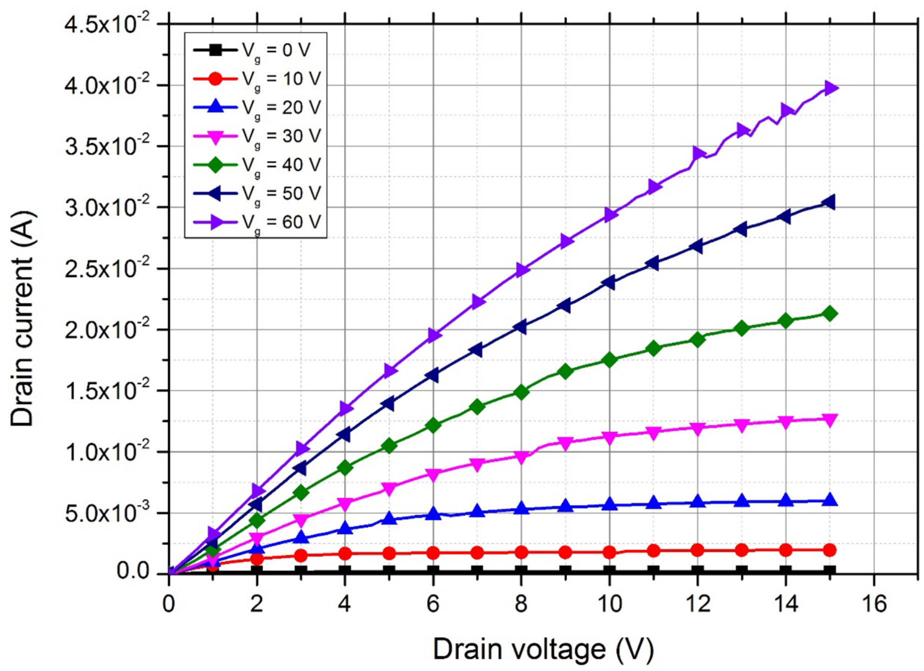


Figure 8.22: Output characteristics of longer single cell vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours.

From Figure 8.21 and Figure 8.22 it is seen that the devices are still working even at the gate voltage of 60 V, this is because of the much thicker oxide produced after the N_2O post oxidation annealing which is about 101 nm measured from the ellipsometer. For the small single cell vertical MOSFETs with cell length of 310 μm, the maximum drain current at gate voltage of 20 V is about 2.5×10^{-3} A. For the longer single cell vertical MOSFET which has cell length of 950 μm, the maximum drain current at gate voltage of 20 V is about 6×10^{-3} A which is about 3 times higher than the small single cell vertical MOSFET. Compare to the vertical MOSFETs without the N_2O POA as shown in Figure 8.18 and Figure 8.19, the vertical MOSFETs with N_2O POA at 1300°C for 4 hours show significantly higher output current, which is more than 400 times increase in

the maximum output current for the small single cell vertical MOSFET at gate voltage of 20 V. These results confirm that the N_2O POA technique is effective in reducing the interface trap density (D_{it}) between the oxide and the SiC as discussed in Chapter 7, the reduction of the D_{it} will increase the output current and therefore reduce the total on-state resistance of the device. Figure 8.23 shows the transfer characteristics of both small and longer single cell vertical MOSFETs after N_2O POA at 1300°C for 4 hours at drain voltage of 0.1 V.

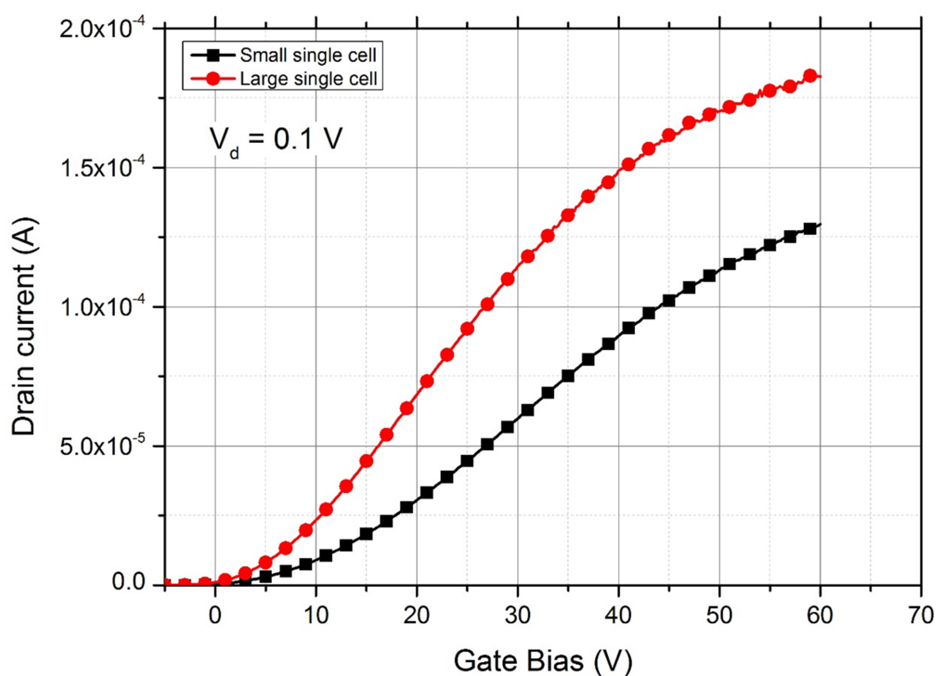


Figure 8.23: Transfer characteristics of single cell vertical MOSFETs with 2 μm channel length after N_2O POA at 1300°C for 4 hours.

From Figure 8.23 it is seen that the threshold voltage is roughly between 5 to 10 V for both sizes of single cell vertical MOSFETs after the N_2O POA at 1300°C for 4

hours, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in the Table 7.2 in Chapter 7. It is also found that there are 3 out of 6 of 0.1 A multi-fingers vertical MOSFETs working after the N_2O POA at 1300°C for 4 hours, which is significant improvement compare to the single cell vertical MOSFETs fabricated without the N_2O POA. Figure 8.24 shows the output characteristics of one of the 0.1 A multi-fingers vertical MOSFETs. It is seen that the maximum drain current at gate voltage of 20 V is about 4.5×10^{-2} A, which is exactly 18 times larger than the small single cell vertical MOSFETs, as the 0.1 A multi-fingers vertical MOSFETs involves 18 of the small single cell vertical MOSFETs. Results show that the vertical MOSFETs have higher drain current and higher the number of working devices when fabricated using the N_2O POA at 1300°C for 4 hours than those fabricated without using N_2O POA. The threshold voltage is also reduced from 16 V to around 5 V after the N_2O POA on the longer single cell vertical MOSFET, which is similar to what has been observed from the lateral MOSFETs fabrication as discussed in Chapter 7. However, the largest 1 A multi-fingers vertical MOSFETs are still not working. It is believed that the oxide quality is still the main issue, since a much larger area is covered by the 1 A multi-finger device and it has a higher chance of having defects in the oxide and SiC wafer.

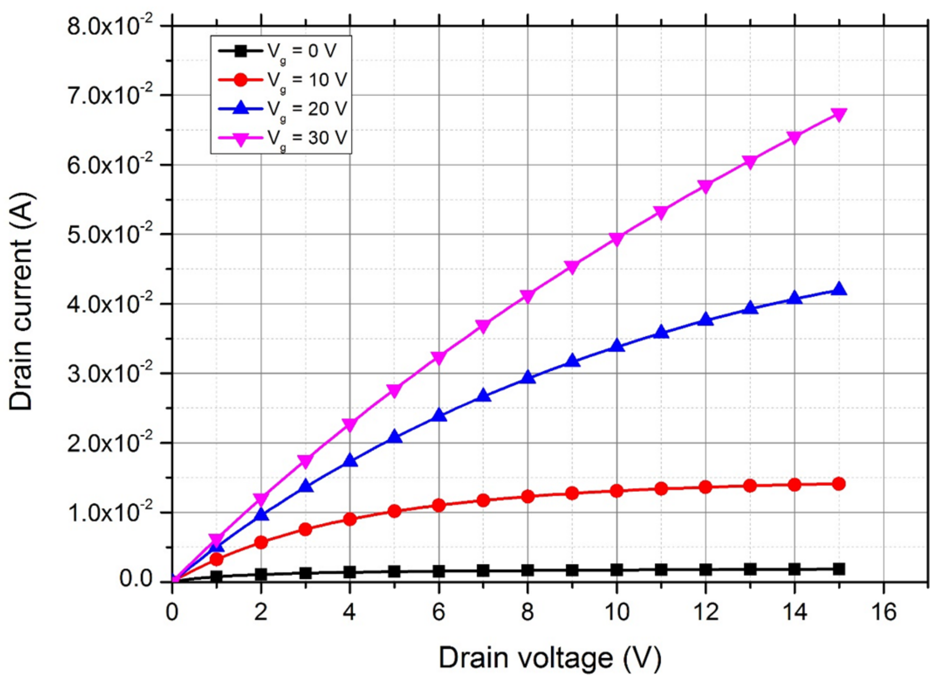


Figure 8.24: Output characteristics of 0.1 A multi-fingers vertical MOSFETs with 2 μm channel after N_2O POA at 1300°C for 4 hours.

8.5 Summary

In this Chapter, the fabrication and characterisation of 4H-SiC vertical MOSFETs has been presented. First, the mask design and the fabrication process of the 4H-SiC vertical MOSFETs were outlined, the challenges in the fabrication process such as small alignment gap between the source and the drain contacts, the photoresist development problem for a narrow and deep trench structures and the defects on the 4H-SiC were discussed. After that, the SIMS measurements were carried out on the three implanted dopants to compare with simulated SRIM doping profiles. Results show that the SIMS profile is similar to the simulated SRIM profile, except that a higher surface concentration and a more gradual tail. Vertical power MOSFETs have been successfully fabricated with both single cell and

small multi-fingers cell VDMOSFETs working. The small alignment gap challenge for the vertical MOSFET fabrication has been overcome by using our new MA/BA8 mask aligner which provides much higher precision, and the photoresist development issue for the narrow and deep trench part of the structure has been overcome by using the much thicker photoresist (AZ9260) with faster spinning speed.

The first generation of 4H-SiC vertical MOSFETs were fabricated with the gate oxide grown at standard thermal oxidation at 1400°C for 1 hour without any post oxidation annealing, which gives oxide thickness of about 50 nm. Both small and longer single cell vertical MOSFETs with a 2 μm channel length were measured and compared. Results show that the maximum drain current at gate voltage of 20 V for the longer single cell vertical MOSFET is about 4 times higher than the small single cell vertical MOSFET. The larger output current is expected from the longer single cell MOSFET because of the much longer cell length (950 μm for the longer single cell and 310 μm for the small single cell). The threshold voltage is about 16 V for both sizes of single cell of MOSFETs, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in the Table 7.3 in Chapter 7. It is also found that although most of the single cell MOSFETs were working, the yield of the multi-fingers vertical MOSFETs (0.1 A and 1 A devices) were very low. Only 1 out 6 of the 0.1 A multi-fingers vertical MOSFETs were working and none of the 1 A multi-fingers vertical MOSFETs were working. It is believed that the low yield of the multi-fingers vertical MOSFETs is due to the poor oxide quality, and as the gate oxide area increases the chance of having defect in the oxide also increases.

Defects on the SiC material could also be the reason for the low yield of the multi-fingers MOSFETs.

The second generation of devices were fabricated with the N_2O post oxidation annealing at 1300°C for 4 hours after the oxide were grown at 1400C for 1 hour. Results show that the maximum drain current at gate voltage of 20 V for the large single cell vertical MOSFET is about 3 times higher than the small single cell vertical MOSFET, which is similar to the first generation devices. The second generation devices shown significantly higher output current than the first generation devices, which is more than 400 times larger in the maximum output current at gate voltage of 20 V. Although the channel mobility of vertical MOSFET cannot be easily extracted unlike the lateral MOSFET, the results still confirm that N_2O POA technique is effective in reducing the interface trap density (D_{it}) between the oxide and the SiC. The threshold voltage is also reduced to around 5 V after the N_2O POA at 1300°C for 4 hours, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in the Table 7.3 in Chapter 7. Some of the small multi-fingers devices (0.1 A) were also working in the second generation devices, which have proven that the first generation device failure was mainly due to the poor oxide quality. Although the largest 1 A multi-fingers vertical MOSFETs still not working, the total number of working devices for both single cell and multi-fingers vertical MOSFETs have increased and the performance of the devices were improved compared to the first generation devices. It is believed that the oxide quality is still the main issue for the large 1 A multi-fingers devices, since much larger area is covered by the 1 A

multi-fingers device, the chance of having defects in the oxide and SiC is also increased significantly. Future work will need to investigate these issues, and the re-design of the masks for high current (>1 A) vertical MOSFETs may be required.

Chapter

9 Conclusions and Future Work

In this final Chapter, the general conclusions of the research conducted in this thesis are presented. Some key contributions of this research, which focuses on improving the channel mobility by development of novel techniques such as using our unique high temperature oxidation furnace and post oxidation anneal process to improve the interface between the oxide and semiconductor have been summarised. In addition, future work is suggested which may help overcome some of the existing obstacles inhibiting the successful realisation of high current (>1 A) vertical MOSFETs and techniques which can further improve the channel mobility of the vertical MOSFETs.

9.1 Conclusions

The overall aim of the research presented in this thesis was to design and fabricate 4H-SiC power MOSFETs for high voltage applications. Due to the advantages of 4H-SiC over Si

for power semiconductors, it is expected that this advancement of high voltage 4H-SiC MOSFETs has the potential to replace the silicon IGBT incumbent device with superior performance, which is a key parameter in high power converter design and will enable a transformation of global power networks.

A key parameter of a power semiconductor device is its efficiency, which means that the power losses need to be as small as possible. The first step of designing the power MOSFET was to optimise the cell structure such that the total on-state resistance of the device can be minimised. As discussed in Chapter 3, the channel resistance and the accumulation resistance will increase when the width of JFET region is increased, however, the JFET and drift region resistances will reduce if the width of JFET region is increased. From the theoretical calculations and the numerical simulation results, it is seen that the JFET region width of 2 μm will result low on-resistance and acceptable breakdown voltage and is therefore chosen for the design of vertical MOSFET. The shielded planar inversion-mode MOSFET structure, which proposed by Baliga [101] was used in this work, since the conventional planar power MOSFET is not suitable for the development of silicon carbide devices because of the much larger bandgap of silicon carbide and the much smaller intrinsic carrier concentration than the silicon.

In order to achieve high breakdown voltage of 4H-SiC devices, edge termination at the periphery of devices are required to minimise the electric field build up in the edges. There are many types of terminations for SiC devices which have been published in literature, and the most commonly used edge termination technique is the junction termination

extension (JTE) because of its easy to fabricate and effective in improving breakdown voltage. In this work, different JTE structures have been designed and simulated including single-zone JTE, space modulated JTE (SMJTE) and the novel two-step mesa JTE structures. It was found that for the same doping concentration the SM two-zone JTE and SMJTE have higher breakdown voltage than the single zone JTE. With SM two zones JTE, the device could achieve up to 97% of the ideal parallel plane voltage and gives a wider optimum JTE dose window than single zone JTE and SMJTE structures. However, it has a disadvantage of having more implantation steps which result in higher cost. Similar to the two-step mesa JTE structure although it could achieve up to 99% of the ideal parallel plane breakdown voltage and provides widest optimum doping window, its complexity in design and fabrication makes it the least attractive to use on real device fabrication. Therefore, for the cost saving and ease of fabrication, the SMJTE structure was used in the fabrication in this work as it provides good breakdown voltage and wider JTE dose window than the conventional single zone JTE. Simulations on 1 kV and 3.3 kV shielded inversion-mode vertical MOSFETs with and without SMJTE structure were also performed. For 1 kV and 3.3 kV shielded planar VD-MOSFETs, the channel resistances are the major contributor on the total on-resistance, and so it is important to increase the channel mobility of the 4H-SiC MOSFET in order to reduce the total on-resistance. However, for a 10 kV shielded planar VD-MOSFETs the channel resistance is negligible compare to the longer drift region resistance, which takes up about 90% of the total on-resistance.

Before any 4H-SiC devices can be fabricated, it is necessary to develop fabrication processes and overcome some of the challenges first such as forming carbon capping layer to protect the SiC surface, post implant activation annealing investigation and forming ohmic contacts on 4H-SiC. The use of the capping layer to suppress the step bunching on 4H-SiC due to high temperature post-implantation annealing was investigated. It is seen that carbon capping layer can effectively protect SiC surface from step bunching and limit the surface roughness to below 1 nm RMS from the atomic force microscopy (AFM) measurement. Severe step bunching was observed above 1650°C annealing for 1 hour, but it did not appear when annealed at 1600°C for 45 minutes. One interesting finding when comes to lateral MOSFETs fabrication was that although the carbon capping layer can suppress the step bunching during the post-implantation annealing, it has no significant impact on the channel mobility of the MOSFET as discussed in Chapter 5 and decrease of channel mobility after using carbon capping layer was reported in [130]. Next, a study into different post-implantation annealing temperature on 4H-SiC was carried out. Post-implantation annealing at 1650°C for 1 hour and 1600°C for 45 minutes have been performed on 4H-SiC lateral MOSFETs. No significant difference in terms of channel mobility was observed between the two annealing conditions. Following this, the ohmic contact on both n-type and p-type 4H-SiC were achieved by fabrication and characterisation of TLM structures. Results show that the unannealed Ti/Ni contact scheme suffered from rectifying behaviour. By annealing the sample at 1000°C for 2 minutes, ohmic behaviour was observed with a specific contact resistivity of 3.18×10^{-5}

$\Omega \cdot cm^2$ for the n-type 4H-SiC and about 6.25×10^{-3} $\Omega \cdot cm^2$ for the p-type 4H-SiC. Because the focus of this work is the fabrication of 4H-SiC MOSFETs, it is the ohmic contact on n-type 4H-SiC which is the main concern in this work.

After the development of key fabrication processes discussed in Chapter 5 had reached a level deemed sufficient for device fabrication, the fabrication of 4H-SiC MOS capacitors and Schottky diodes could commence. MOS capacitors were designed and fabricated using the advanced passivation techniques, namely the N_2O and phosphorous passivations or a combination of both techniques to reduce the interface trap density (D_{it}). A novel phosphorous passivation technique which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) instead of conventional POCl3 is main focus of this work. The D_{it} were extracted using both Terman and High-Low C-V methods. Results show that MOS capacitors with N_2O POA treatment have lower interface trap density than one without POA, different nitridation temperatures were also performed and the best results were found at 1300°C for 4 hours (both direct growth oxide and POA). The MOS capacitors with phosphorous POA has the lowest D_{it} of all MOS capacitors fabricated in this work, which is about 1×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV away from the conduction band edge using high-low C-V method. The combined N_2O and phosphorous POA did not show any further reduction in the D_{it}, but nonetheless it is still lower than the one just with N_2O POA as shown in Chapter 6. Reverse I-V breakdown characteristics of MOS capacitors were also performed, it is seen that the oxide breakdown electric field is approximately 8 MV/cm for MOS capacitor fabricated with dry oxidation at 1400°C for 1 hour without POA.

Further POA treatments in either N_2O or phosphorous will reduce the breakdown electric field to about 5~6 MV/cm, however, their leakage current is much smaller compare to the MOS capacitor fabricated without POA as shown in Chapter 6. Schottky diodes with different JTE structures (single zone JTE and SMJTE JTE) were also fabricated to test the breakdown performance of the devices using the high voltage test rig which designed and built by our research group in the University of Warwick. Results show that the breakdown voltage of the 1 kV rated Schottky diode without the JTE structure is only about 100 V. With the 200 μm length single zone JTE structure, the breakdown voltage has increased to about 600 V. Increase the length of JTE will increase the breakdown voltage to about 700 V by increasing the length of the single zone JTE structure to 600 μm. The highest breakdown voltage was achieved with the use of the SMJTE JTE structure, which is about 960 V, 86% of the ideal one-dimensional parallel-plane breakdown voltage. The SMJTE structure also provides wider optimum doping window than the single zone JTE structure as shown in Chapter 6. The SMJTE structure have proven to be effective in improving the breakdown voltage of SiC devices from both simulation and experimental measurements results. The SMJTE structure with 600 μm JTE length was designed for the high voltage (>10 kV)SiC devices as discussed in literature [59, 67]. Although it was applied to the 1 kV Schottky diode in this work, the effectiveness of the SMJTE was also confirmed for the 1 kV devices. Therefore, the SMJTE structure can be a promising termination technology for 4H-SiC power devices.

After the fabrication of 4H-SiC MOS capacitors using the N_2O and phosphorous pas-

sivation techniques, which proven to be effective in reducing the interface trap density (D_{it}) as shown in Chapter 6, 4H-SiC n-channel lateral MOSFETs were fabricated using the same N_2O and phosphorous techniques. The first generation 4H-SiC lateral MOSFETs were fabricated with box-like p-body doping profile. Different implant activation annealing temperature on lateral MOSFETs were first investigated, it is seen that there is little difference in field effect mobility between the MOSFETs activated at 1600°C for 45 minutes and at 1650°C for 1 hour, which is about 1.2 $cm^2/V.s$ as shown in Chapter 7. High temperature oxidation at 1500°C using the high temperature oxidation to reduce the D_{it} was first looked at. It is found that although the enhanced oxidation rate at high temperature may reduce the interface states at the 4H-SiC/SiO2 interface as reported in [83], the difference between the peak field effect mobility for lateral MOSFETs oxidised at 1400°C for 1 hour and at 1500°C for 30 minutes is very small. N_2O POA at temperature vary from 1200°C to 1500°C have been investigated, and the best field effect mobility was also found at N_2O POA at 1300°C for 4 hours, which is about 17 $cm^2/V.s$. N_2O POA at 1300°C for 4 hours also results the lowest threshold voltage compare to other N_2O POA conditions. The second generation 4H-SiC lateral MOSFETs were fabricated with retrograde p-body doping profile, which is the same doing profile as the vertical MOSFETs. The impact of sacrificial oxide thickness on channel mobility of the lateral MOSFETs were investigated. It is found that the thinner the sacrificial oxide the better the field effect mobility of the MOSFETs. The novel phosphorous passivation technique which uses the solid SiP_2O_7 phosphorous planar diffusion source (PDS) was also used to

fabricate the lateral MOSFETs. Results show that the highest peak field effect mobility of approximately 80 $cm^2/V.s$ was obtained after the phosphorous POA at 1000°C for 2 hours, which is the highest field effect mobility seen so far on the implanted P-body region of 4H-SiC (0001) MOSFETs. The peak field effect mobility for the MOSFETs with combined N_2O and phosphorous POA is less than the MOSFET with phosphorous POA but higher than the MOSFET with N_2O POA, which corresponding to their D_{it} results from the MOS capacitors as discussed in Chapter 6. The only drawback, however, is the negative threshold voltage (~-5 V) after the phosphorous POA at 1000°C for 2 hours. This reduction of threshold voltage is due to the positive charge within the oxide or in the interface between the SiO_2/SiC. Oxide breakdown measurements at room temperature were also carried out for the lateral MOSFETs with different post oxidation conditions. Results show that the oxide breakdown field are all above 10 MV/cm for MOSFETs fabricated at 1400°C for 1 hour without POA, and both with N_2O POA and with phosphorous POA. MOSFETs with phosphorous POA show even higher oxide breakdown field than the MOSFETs without POA, which is about 13 MV/cm. This novel phosphorous passivation using solid SiP_2O_7 phosphorous planar diffusion source (PDS) was proven to be more effective in reducing interface traps compared to the conventional NO/N_2O passivation. Mobility is about 4 times higher than the N_2O passivation. This significant improvement in channel mobility will be enable us to realise the full potential of SiC technology.

The final Chapter focusses on the fabrication and characterisation of the vertical power MOSFETs. The mask design and the fabrication process of the 4H-SiC vertical MOSFETs

were first outlined. The challenges in the fabrication process of 4H-SiC vertical MOSFET were explained, such as the small alignment gap between the source and the drain contacts, the photoresist development problem for a narrow and deep structures and the defects on the 4H-SiC. The use of our new MA/BA8 mask aligner and the development of using thicker photoresist photoresist (AZ9260) with faster spinning speed have overcome these challenges.

The first generation of 4H-SiC vertical MOSFETs were fabricated using standard thermal oxidation at 1400°C for 1 hour without any post oxidation annealing. Results show that the maximum drain current at gate voltage of 20 V for the longer single cell vertical MOSFET is about 4 times higher than the small single cell vertical MOSFET, which is expected as the longer single cell MOSFET is three times longer than the small single cell. The threshold voltage is about 16 V for both size of devices, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in Chapter 7.

The second generation of 4H-SiC vertical MOSFETs were fabricated using N_2O post oxidation annealing at 1300°C for 4 hours. Compare to the first generation of vertical MOSFETs, the vertical MOSFETs with N_2O POA at 1300°C for 4 hours show significantly higher output current, which is more than 400 times increase in the maximum output current for the small single cell vertical MOSFET at gate voltage of 20 V. The threshold voltage is also reduced to around 5 V after the N_2O POA at 1300°C for 4 hours, which is similar to the lateral MOSFETs fabricated at the same conditions as shown in Chapter 7. Results confirm that N_2O POA technique is effective in reducing the interface trap

density (D_{it}) between the oxide and the SiC. It is also found that the yield of the multi-fingers devices have also increased, which is more than 60% improvement compare to the single cell vertical MOSFETs fabricated without the N_2O POA. Although the largest 1 A multi-fingers vertical MOSFETs were not working, the total number of working devices for both single cell and multi-fingers devices have increased and the performance of the devices were improved compared to the first generation devices. Future work will need to investigate these issues and may need to re-design the masks in order to achieve higher current devices.

9.2 Future Work

The promising results presented in this thesis and by various research groups in recent years illustrate the maturing of 4H-SiC power device technology. 1.2 kV 4H-SiC MOSFETs have been commercialised by few companies [8, 34] and are beginning to compete with silicon components in the markets, however, there still remains huge scope for further improvements in high voltage (3.3 kV) 4H-SiC power MOSFETs before they can fully commercialised. In this section, areas for future research and developments that are required to improve the performance, reliability and feasibility of high voltage 4H-SiC MOSFETs have been identified.

The numerical simulations of the devices in this thesis have been limited to 1- and 2-D analysis for both forward and reverse breakdown characteristics. In future, for more

comprehensive analysis of the behaviour of 4H-SiC device structures, the use of 3-D simulations should be applied since the reverse breakdown simulations for the more elaborate JTE structure cannot be accurately modelled in 2-D structures. Device modelling and simulation for 4H-SiC devices can also be done using the process simulator such as Silvaco Athena [151]. Due to the relative immaturity of 4H-SiC process modelling compared to Si and the lack of comprehensive empirical data, the process simulation was not used in this work. However, as the amount of experimental data for 4H-SiC processing is continually accumulating, and process models for 4H-SiC are gradually becoming more robustly defined, the use of these process models could be used in future to obtain more accurate electrical simulation results.

Although significant progress has been made in the device fabrication process used in this work, there are still more work can be done to further build on the experimental findings presented in this thesis. Ohmic contact on 4H-SiC particularly on p-type material still require further work to reduce the contact resistivity, although for the purpose of MOSFETs fabrication in this work p-type ohmic contact is not a major concern, it is great importance for bipolar 4H-SiC devices such as P-i-N diode. Investigation into different metals stack and annealing process may be required in order to achieve good ohmic contact on both p-type and n-type 4H-SiC at the same time on the 4H-SiC MOSFETs. Furthermore, the stability of these contacts under high temperature should be investigated if the devices is expected to operate at high temperature. Another aspect of device fabrication that require further work is the edge termination for 4H-SiC vertical power

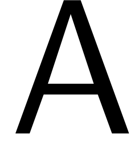
MOSFETs. Although the design of SMJTE structure have proven to be effective in reducing the electric field crowding at the edges and increase the breakdown voltage on the Schottky diodes, the fabrication of 4H-SiC vertical MOSFETs will need to include the SMJTE structure in the future for the demonstration of high voltage 4H-SiC vertical MOSFETs.

The novel phosphorous passivation process has shown the potential to succeed as an effective passivation process because of the lower interface trap density and higher channel mobility than the N_2O passivation process. However, there are still additional experiments that should be carried out for the phosphorous passivation process. Firstly, the post oxidisation annealing temperature and time have yet to be optimised, higher annealing temperature and longer time may result higher channel mobility. Secondly, the bias-temperature stress measurements need to be carried out to check the oxide reliability after the passivation, and finally, other passivation techniques such as thin layer of PSG layer with TEOS oxide on top as those reported in [29] and other elements from group V of the periodic table like arsenic (As) and antimony (Sb) can be investigate in future.

Although 4H-SiC vertical power MOFETs have been successfully demonstrated with both single finger cell and multi-fingers cell (0.1 A) structures working, there still remain many works to done to further improve the performance and reliability of 4H-SiC vertical MOSFETs. The low yield of the multi-fingers vertical MOSFET is the main challenge in this work, particularly for the high current (1 A) vertical MOSFET. Future work will need to investigate these issues including the re-design of the photomasks to have less

number of multi-fingers cell structure and also increase the length of the single finger cell structure. Phosphorous and other passivation techniques on the vertical MOSFETs will also need to be investigated in the future.

Appendix



A Vertical MOSFET Process Flow

Table A.1: Vertical MOSFET Process Flow.

Cross-sectional diagram	Plan view	Process steps
L1: Alignment N- N+		1. Clean the wafer using standard SiC cleaning process. 2. Photolithography to pattern the alignment marks. 3. Etch the wafer in the ICP etcher. 4. Remove the photoresist in acetone and O_2 ash in the ICP etcher. Blow dry with N_2.
		Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L2: P-well P-Well P-Well N- N+		1. Deposit TEOS oxide of 2 μm. 2. Photolithography to pattern the P-well regions. 3. Etch oxide using ICP ethcer. 4. Send off for P-well ion implantation
L3: JFET P-Well P-Well N- N+		1. Remove oxide in HF and deposit TEOS of 2 μm. 2. Photolithography to pattern the JFET regions. 3. Etch oxide using ICP etcher 4. Send off for JFET ion implantation

Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L4: N+ source		1. Remove oxide in HF and deposit TEOS of 2 μm. 2. Photolithography to pattern the N+ source regions. 3. Etch oxide using ICP etcher 4. Send off for N+ source ion implantation.
L5: P+ source		1. Remove oxide in HF and deposit TEOS of 2 μm. 2. Photolithography to pattern the P+ source regions. 3. Etch oxide using ICP etcher 4. Send off for P+ source ion implantation

Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L6: JTE		1. Remove oxide in HF and deposit TEOS of 2 μm. 2. Photolithography to pattern the JTE regions. 3. Etch oxide using ICP etcher 4. Send off for JTE ion implantation

Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L7: Gate oxide		1. Remove oxide in HF and anneal at 1650°C for 45 minutes to activate implanted species. 2. Deposit TEOS of 1 μm as field oxide. 3. Photolithography to pattern the gate oxide regions. 4. Etch oxide using ICP ethcer. 5. Remove the photoresist in acetone and O_2 ash in the ICP etcher. Blow dry with N_2. 6. Grow gate oxide in the HiTech furnace
		Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L8: Source window		1. Photolithography to pattern the source window regions using AZ9260 thick photoresist. 2. Etch oxide using ICP etcher to open window for source contact.
L9: Source metal		1. Photolithography to pattern the source metal regions using AZ9260 thick photoresist. 2. Deposit source metals of Ti 30nm and Ni 100nm and lift off in acetone using ultrasonic bath.

Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
Drain metal		1. Remove the back oxide using the ICP etcher. 2. Deposit drain metals Ti 30nm and Ni 100nm on the back. 3. Anneal at 1000°C for 2 minutes to form the ohmic contacts.
L10: Gate metal		1. Photolithography to pattern the gate metal regions using AZ9260 thick photoresist. 2. Deposit gate metal of Al of 500 nm and lift off in acetone using ultrasonic bath.

Continued on next page

Table A.1 – continued from previous page

Cross-sectional diagram	Plan view	Process steps
L11: Same as above		1. Photolithography to pattern the contact pad regions. 2. Deposit Al of 1 μm and lift off.

Note: The JFET and JTE implantations steps were not used in this work for the vertical MOSFETs fabrication due to the high cost involved and time limitation. Edge bead mask was also used to remove the photoresist on the edges of the sample.

Appendix B Silicon Carbide Device Cleaning Process

This Appendix details the 4H-SiC wafer cleaning process that has been employed for device fabrication work presented in this thesis. The standard SiC cleaning process refers to all Organic cleaning, Piranha cleaning and RCA cleaning processes which carried out in subsequent order.

B.1 Organic Cleaning

1. Place sample in acetone for 5 minutes in ultrasonic bath, rinse in deionised (DI) water and blow dry using nitrogen gas.
2. Place sample in isopropanol for 5 minutes in ultrasonic bath, rinse in DI water and blow dry using nitrogen gas.
3. Place sample in acetone for 5 minutes in ultrasonic bath, rinse in DI water and blow

dry using nitrogen gas.

4. Place sample in methanol for 5 minutes in ultrasonic bath, rinse in DI water and blow dry using nitrogen gas.

5. Place sample in methanol for 5 minutes in ultrasonic bath, rinse in DI water and blow dry using nitrogen gas.

6. Place sample in BOE (10% HF) solution for 5 minute to remove oxide, rinse in DI water and blow dry using nitrogen gas.

B.2 Piranha Cleaning

1. Place sample in sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in the ratio 1:1 for 15 minutes, rinse in DI water.

2. Place sample in BOE (10% HF) solution for 1 minute, rinse in DI water.

B.3 RCA Cleaning

1. Place sample in RCA 1 solution (ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and DI water in the ratio 1:1:3) at temperature of 80°C for 15 minutes, rinse in DI water.

2. Place sample in BOE (10% HF) solution for 1 minute, rinse in DI water.

3. Place sample in RCA 2 solution (hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and DI water in the ratio 1:1:3), rinse in DI water.

4. Place sample in BOE (10% HF) solution for 1 minute, rinse in DI water and blow dry using nitrogen gas.

Appendix

C Standard Photolithography Processes

This Appendix details the standard photolithography processes for both positive and negative photoresists that have been employed for the device fabrication in this work.

C.1 Positive Photoresist Process

Shipley S1818 photoresist was used in this work, which has average thickness of about 1.8 μm. For the positive photoresist, the portion of the photoresist that is exposed to ultraviolet (UV) light becomes soluble to the photoresist developer. The portion of the photoresist that is unexposed remains insoluble to the photoresist developer. The photolithography process for this photoresist is outlined as follows:

1. Deposit Primer onto to the surface of the sample using a pipette, leave for 1 minute and blow dry in N_2.

2. Place sample on spinner chuck, deposit S1818 photoresist using a pipette. Spin at 500 rpm for 2 seconds followed by 4000 rpm for 7 seconds.

3. Place sample on hot plate at 120°C for 3 minutes.

4. Align sample with the relevant photomask using Karl Suss MJB3 mask aligner and expose in UV light for 10 seconds.

5. Develop sample using MF319 solution for 45 seconds, rinse in DI water then blow dry in N_2.

C.2 Negative Photoresist Process

A negative photoresist is a type of photoresist in which portion of the photoresist that is exposed to UV light becomes insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer. AZ5214E image reversal photoresist was used in this work, which has average thickness of about 1.4 μm. The photolithography process for this photoresist is outlined in the as follows:

1. Deposit Primer onto to the surface of the sample using a pipette, leave for 1 minute and blow dry in N_2.

2. Place sample on spinner chuck, deposit AZ5214E photoresist using a pipette. Spin at 300 rpm for 5 seconds followed by 4000 rpm for 30 seconds.

3. Place sample on hot plate at 115C for 1 minutes.

4. Expose sample on Karl Suss MJB3 mask aligner through relevant photomask for 7.5 seconds, or on Suss MicroTec MA/BA8 mask aligner with UV light intensity of 40 mJ/cm^2.

5. Place sample on hot plate at 120C for 2 minutes.

6. Flood exposure of sample for 15 seconds in Karl Suss MJB3 mask aligner or with UV light intensity of 250 mJ/cm^2 in Suss MicroTec MA/BA8 mask aligner.

7. Develop sample using MF319 solution for 50 seconds if exposed with Karl Suss MJB3 mask aligner, or for 30 seconds if exposed with Suss MicroTec MA/BA8 mask aligner. Rinse in DI water then blow dry in N_2.

C.3 Thick Photoresist (AZ9260) Photolithography Process

A thick photoresist (AZ9260) with thinner layer photolithography process was used for the fabrication of vertical MOSFETs in this work as discussed in Chapter 8. The photolithography process for this photoresist is outlined as follows:

1. Place sample on hot plate at 115°C for 3 minutes.

2. Deposit Primer onto to the surface of the sample using a pipette, leave for 1 minute and blow dry in N_2.

3. Place sample on spinner chuck, deposit AZ9260 photoresist using a pipette. Spin at 300 rpm for 5 seconds followed by 6000 rpm for 1 minute.

4. Place sample on hot plate at 110°C for 2 minutes.

5. Remove sample from hot plate and leave for 10 minutes.

6. Expose sample on Suss MicroTec MA/BA8 mask aligner with UV light intensity of 1800 mJ/cm^2.

7. Develop sample using AZ726MIF solution for 6 minutes, rinse in DI water and blow dry in N_2.

8. Expose sample on Suss MicroTec MA/BA8 mask aligner through relevant photomask with UV light intensity of 900 mJ/cm^2.

9. Develop sample using AZ726MIF solution for 6 minutes, rinse in DI water and blow dry in N_2.

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