Proceedings Paper:
Efika, IB, Nwobu, CJ and Zhang, L (2014) Reactive power compensation by modular multilevel flying capacitor converter-based STATCOM using PS-PWM. In: 7th IET International Conference on Power Electronics, Machines and Drives. PEMD 2014, 08-10 Apr 2014, Manchester, UK. Institution of Engineering and Technology (IET) . ISBN 978-1-84919-815-8

https://doi.org/10.1049/cp.2014.0504

Reactive Power Compensation by Modular Multilevel Flying Capacitor Converter-Based STATCOM Using PS-PWM

I.B Efika, C.J Nwobu †, L Zhang †*

**University of Leeds, United Kingdom, el09ibe@leeds.ac.uk, el08cjn@leeds.ac.uk*

Keywords: Modular multilevel cascade converter, Pulse Width Modulation, STATCOM, Flying capacitor.

Abstract

This paper presents a simulation study into the implementation of a modular multi-level flying capacitor converter as a STATCOM. The converter modulation scheme applied is based on Phase Shifted PWM and the two scenarios which require compensation are investigated to verify this topology. The two scenarios are PCC voltage regulation through reactive power compensation and power oscillation damping through reactive current compensation. Simulation results verify the performance of the chosen topology.

1 Introduction

The continuous evolution of the power grid to a more dynamic nature, although reckoned as positive, is presenting several challenges that need be resolved. The continuous interconnections of distributed sources to provide redundancy in power supply may lead to voltage instability as well as increased short-circuit cases in the grid networks. On the load side, the rise of more industrial consumers on the grid also presents an issue due to the nature of their loads (drives and traction systems) which are normally predominantly reactive and non-linear. Without compensation, the presence of reactive current on the line will result in a low power factor and voltage drift away from the required range. Also power oscillations could be introduced into the power system when variable loads (iron smelter) draw current from the supply that modulate at sub-harmonic frequencies. The resulting scenario causes voltage swell or drop proportional to the load current, interconnected line impedance and frequency. STATCOM is an effective device in high voltage high power network in overcoming the above stated problems.

Recent developments have led to the topology of modular multilevel cascaded converters (MMCC) which are considered most suitable for higher power STACOM applications. This topology offers flexibility of extension by using complete converter units/modules/bridges to form each phase leg and this eliminates the requirement of complicated multi-winding phase-shifted line-frequency transformers [1, 2]. The attractive feature of this topology is its modularity and scalability to easily reach medium- and high-voltage levels, while greatly improving ac side power quality. In addition it has a fault-tolerant capability in that it can bypass a faulty circuit and be reprogrammed to generate reduced voltage. The circuit devices (both switching and clamping) in MMCC are rated only to the power levels experienced at module-level, hence high power converters can be achieved using moderately lower-rated switching devices.

This paper presents a variant of the Modular Multilevel Cascade Converter (MMCC), the Modular Multilevel Flying Capacitor Converter (MMFCC). In this form, the 2-level sub-module which is the current norm is replaced with a 3-level flying capacitor circuit "FCC" module [3]. This conforms to the single star bridge – variant circuit structure (MMCC-SSBC) [4]. So far in literature no work has been published on STATCOM with this configuration. Some work has been done with regards to investigating the converter structures for high power applications and pulse width modulation and space vector schemes [5-7]whilst most of other STATCOM schemes implemented focus mainly on the Cascaded H-bridge MMCC topology[4, 8, 9].

The focus in this paper is on using the MMFCC as a shunt-connected STATCOM for voltage control in a power network. Asides functioning as a "proof of concept", another aim of this is to capture and present the advantages of the proposed topology for this application, which is the optimal utilization of devices (capacitors, switches, etc.) of lower rating for such an implementation. The switching devices here are operated at low switching frequency; hence giving reductions in switching losses and subsequently converter losses. The system investigated and operation scenarios including the injected disturbances will be described. The converter structure and its control scheme are described. The details of the modulation scheme has been covered in [5], so only the applied phase shifted pulse-width modulation technique would be discussed in brief.

2 Power System Configuration

The proposed MMFCC-STATCOM is applied to a simulated power system with the configuration detailed in Table 1.

Component	Description
Supply Side	25kV,100MVA
STATCOM	DC rating (per module): 1.2kV, 1000μF Module Flying Capacitor: 600V, 560μF Converter AC Side Primary: 2.4kV Converter AC Side Secondary: 25kV 1.8 – 5.2MW (Power Factor = 0.9)
Static Load	1MW (Active Power Only)
Variable Load	1.8 – 5.2MW (Power Factor = 0.9)

Table 1: Power System Configuration for MMFCC-STATCOM

The power network is a three phase balanced system rated at 25kV, 100MVA, 50Hz which is coupled via a 23km pie-section transmission line (0.1Ω, 1.05mH, 10nF per km) to the point of common coupling (PCC). A line diagram of the system is as shown in Figure 1(a). Also connected at the PCC are two loads rated at 600 V a variable load with a power factor of 0.9, via a (125:3) step-down transformer. The static load is rated at 1MW and is a representation of normal/linear loads connected to the grid. The 600 V variable loads shown represents an industrial power consumer operating a device which introduces a large and pulsating current such as is evident with electrolytic plating industries. The current variation at PCC was kept at about 40% of 3.1MVA average at the rate of 10Hz. This allows the investigation of the STATCOM compensation for power oscillations on the line during scenario testing.

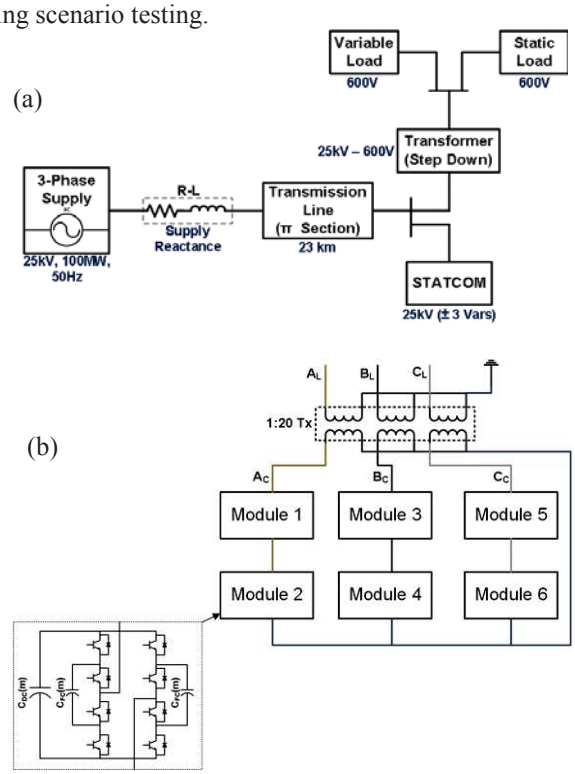

Figure 1: (a) Power system application line diagram, (b) Converter Circuit diagram.

2.1 Circuit Configuration of MMFCC-STATCOM

The MMFCC-STATCOM converter topology is as shown in Figure 1(b) and conforms to the single star bridge - variant of the MMCC (MMCC-SSBC) structure in [4]. This structure consists of three arms which provide the three-phase voltages. Each converter arm consists of a stack of serially connected 5-level FC modules ($+V_{DC}$ to $-V_{DC}$) and in the presented work 2-modules are cascaded to produce nine discrete output voltage levels per phase. It is coupled to the power lines through a 1:20 three-phase transformer primary (A_C, B_C, C_C) and secondary (A_L, B_L, C_L) windings in star - floating star configuration. This provides converter isolation and is adequate as the investigation considered here is assumed that the system is under balanced operating conditions.

Each module bus capacitor, C_{DC}, and the module flying capacitors, C_{FC}, set as 1000 µF and 560µF respectively. Based on control requirements, each module capacitor experiences a DC voltage of 1.25 kV and the corresponding flying capacitor half of this voltage at 625 V. At a switching frequency of 250Hz the voltage deviation is between +0.4%, -1% for the DC capacitor and +0.6%, -1.2% for the flying capacitors.

These are considered realistic sizes for the investigations to achieve the minimal voltage deviations, even during large reactive power disturbances and at low switching frequency.

3 MMFCC-STATCOM Control Scheme

Reactive power compensation control is needed to achieve power factor correction. This may be obtained through voltage regulation/support, or flicker mitigation (power oscillation damping). Based on this, the compensator controllers must provide the following functions.

- DC Bus voltage balancing control,
- AC voltage regulation control, and
- Compensation Current Control

These functions are described in detail in subsections 3.1 -3.3.

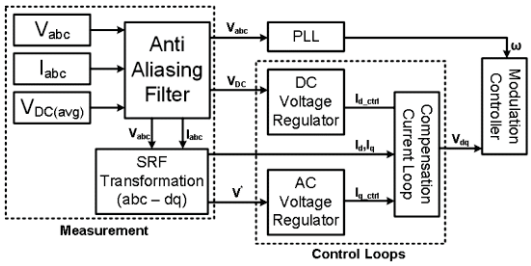

Figure 2: High level system control diagram

A crucial requirement for the control scheme to perform the above functions properly is that it must remain synchronized with the PCC voltage under all system operating conditions and as well, must remain synchronised quickly when system disturbances occur. To realize these requirements, the simulated controller was developed to comprise of the following parts:

- A Synchronous Reference Frame - Phase Locked Loop (SRF-PLL) for synchronizing the converter voltages (i.e. voltages at the terminals AC, BC, CC) with the voltage at the point of common coupling.

- Measurement systems for accurate acquisition of the voltages and currents as well as converting such values to the synchronous reference (d-q) frame as required

The control scheme block diagram is as shown in Figure 2.

3.1 DC Bus Voltage Balancing Control

The DC Bus voltage per module is maintained by a capacitor and the controller used must maintain voltage balancing

across each phase. The block diagram of the DC bus voltage controller is as shown in Figure 3(a).

The control variables ($V_{dc(avg)}$, $V_{dc(ref)}$) are used to maintain the voltage at the DC bus of each module. To ensure clarity, $V_{dc(avg)}$ refers to the average voltage across the three converter phase arms which can be calculated using (1)

$$V_{dc(avg)} = \frac{\sum_{i=1}^{6} Vdc\_M(i)}{3} \quad (1)$$

where, i = number of modules and $V_{dc}\_M(i)$ represents voltage across each individual module.

$V_{dc(ref)}$ is a set-point provided to the DC bus voltage controller, and is calculated from the equivalent/actual DC bus voltage $V_{dc(ref\_equiv)}$ across each arm of the converter i.e. the combination of independent DC bus arrangement in the converter topology. The relationship between $V_{dc(ref)}$ and $V_{dc(ref\_equiv)}$ is shown in (2) because at each fundamental cycle two out the three phases are in operation.

$$V_{dc(ref)} = \frac{2}{3} V_{dc(ref\_equiv)}. \quad (2)$$

As a result of (2) and considering the transformer turn ratio for the 25kVA power system (1:20), $V_{dc(ref\_equiv)}$ is calculated as 2250 and would result in a $V_{dc(ref)}$ set-point of 1500. The DC reference voltage is compared with this value and the error is parsed into the P+I regulator in order to generate the d-component of the current control vector. Using [10], the proportional and integral gain K_p and K_i were chosen as 0.001, 0.15 respectively.

3.2 AC Voltage Control

The AC voltage regulator is as shown in Figure 3(b). The AC Voltage regulation loop aims to maintain the required AC voltage at the PCC. $I_{q(ctrl)}$ is generated based on the difference between the PCC voltage and the desired AC voltage set point $V_{AC(ref)}$. V^* represents the measured magnitude of the AC voltage calculated using the d and q component of the three phase voltage vector as shown in (3).

$$V^* = \sqrt{\left(V_d^2\right) + \left(V_q^2\right)} \quad (3)$$

The proportional and integral gain K_p and K_i were chosen as 0.55, 2500 respectively.

3.3 Compensation Current Controller

The compensation current generated by the STATCOM provides a means of regulating the voltages at the two terminals; at the AC side to influence reactive power flow and at the converter DC side to compensate the converter losses. In Figure 3(c), the d and q components (I_d, I_q) are measured at the PCC whilst the $I_{d(ctrl)}$, $I_{q(ctrl)}$ components are measured feedback control signals derived, passed through the P+I regulators. The output from the P+I controller is the control voltage reference required fed to the pulse-width modulation controller for the converter to achieve compensation. The proportional and integral gain K_p and K_i were chosen as 0.8, 200 respectively.

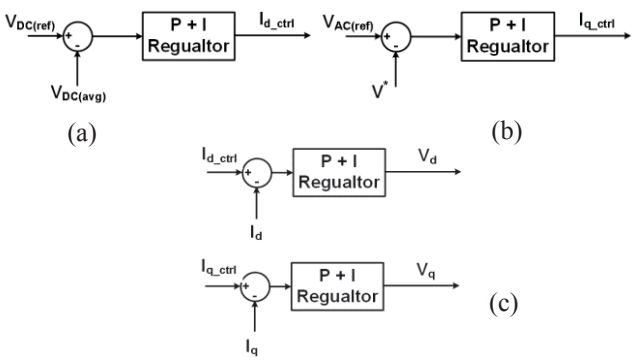

Figure 3: Low level system controllers: (a) Capacitor DC bus voltage regulator control, (b) AC voltage regulator control, (c) Compensation Current controller.

4 Phase Shift PWM for MMFCC-STATCOM

Modulation controls for this topology have already been investigated in detail in [5, 6] and phase Shift PWM control will be discussed here in brief. For this investigation a unipolar phase-shifted PWM (PS-PWM) scheme is applied for the MMFCC-STATCOM. This technique is considered most appropriate for two main reasons; open-loop natural capacitor balancing and good spectral quality of output voltage at low switching frequency. An overview of the modulation controller adopted is as shown in Figure 4.

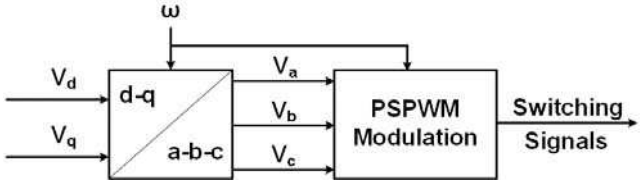

Figure 4: Block diagram for modulation controller

Unlike the classical PS-PWM scheme which uses only one reference signal, the proposed technique uses two modulation reference signals 180^0 phase displaced and compared simultaneously to n carrier waves phase shifted by a constant angle θ_c at the same magnitude and frequency. The number of carrier waves n is equivalent to the number of distinct voltage levels between zero and phase peak.

The switching signals from the modulation technique are applied as such; each 5-level FC module is recognised as an entity comprising of four half-bridge cells (one cell is defined as a complementary switch pair in a half-bridge circuit). At the left-hand side (LHS) of the two cascaded FCC modules, we have 4 unit cells (complimentary switching pairs Module 1: S_1 – S_4, S_2 – S_3, and Module 2: S_5 – S_8 and S_6 – S_7)

likewise on the right-hand side (RHS) there are another 4 unit cells (complimentary switching pairs Module 1: $S_9 - S_{12}$, $S_{10} - S_{11}$, and Module 2: $S_{13} - S_{16}$ and $S_{14} - S_{15}$). For clarity they would be referred to LHS 4 units and RHS 4 units.
The positive reference signal is applied to the LHS 4 units and its negative or 180^0 phase shifted reference signal to the RHS 4 units. The interceptions of positive reference signal with one carrier wave generates switching signals for one cell in LHS whilst interceptions of 180^0 phase shifted reference signal with the same carrier wave generates switching signal for the opposite cell in RHS.

The PSPWM technique and switching signal generated are as shown in Figure 5(a-e). An odd modulation frequency index (m_f) is best chosen to eliminate the even harmonic in the output waveform. Here the switching frequency is at 250Hz $(m_f = 5)$. In addition, the proposed scheme improves hardware computation efficiency as the number of carriers required reduces by a factor of two when compared to the classical PSPWM.

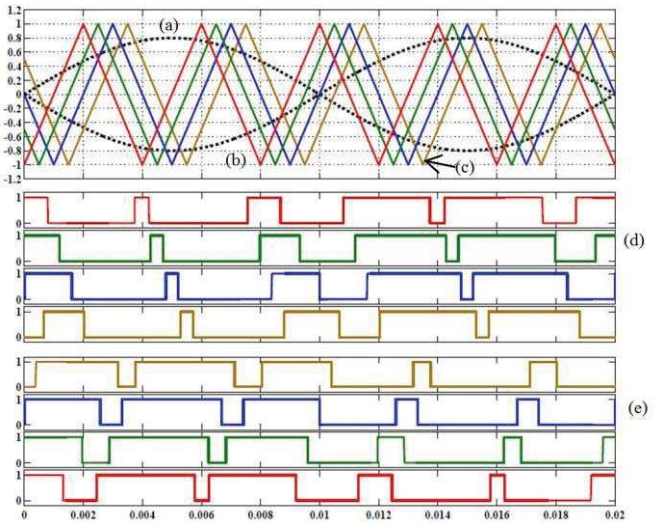

Figure 5: Simulation Results PSPWM for MMFCC: (a) Reference signal, (b) Anti-phase reference signal, (c) Triangular carrier signals, (d) Switching signal generated by comparing b and c, (e) Switching signal generated by comparing a and c.

5 Analysis and Simulation Results

Matlab Simulink was used to perform investigations based on the systems configuration outlined earlier and two different scenarios were simulated. First, voltage regulation when PCC variation is at ± 6% the nominal value. Next, power oscillation damping when the variable load draws an oscillating power at 10Hz. Total Simulated time is 1 second, Converter Switching frequency = 250Hz. At the start of the simulation, the supply voltage (25kV) is kept at 1.077 p.u (i.e. 26.9kV) while the STATCOM was initialized at 1 p.u. This enabled the realization of start-up procedures required to achieve steady state such as the charge-up of the module DC bus capacitors as well as the module flying capacitors. Converter start/charge-up was completed at approximately 0.04 seconds (2 fundamental cycles) while complete system steady state was achieved at approximately 0.08s (4 Fundamental cycles). All investigations are performed under balanced conditions as such, only Phase A waveforms are shown for clarity.

5.1 PCC Voltage Regulation based on MMFCC-STATCOM

At time t = 0.2 s, the voltage at the source is increased by 800V (+ 0.06 p.u) while at time t = 0.3 s, the voltage is reduced by 800 V (- 0.06 p.u). The primary side voltage and current converter waveforms are shown in Figure 6. At t = 0.2s, the STATCOM absorbs quadrature power (inductive operation) from the line, consequently compensating for the voltage increase. The inductive operation of the converter causes the inverter voltage to drop this as shown between the time interval ($0.2 < t < 0.3$). At t = 0.3 s, the STATCOM supplies quadrature power (capacitive) in order to return the voltage to its nominal value. This capacitive operation of the STATCOM converter causes the inverter voltage to rise as shown between the time interval ($0.3 < t < 0.4$). The response of the STATCOM converter to supply or absorb reactive power is fast around half a fundamental cycle.

Figure 7 shows the load voltage and current waveforms as well as the load side and converter side active and quadrature power waveforms successively. At t = 0.2 s, the STATCOM converter supplies inductive quadrature current, hence absorbing a reactive power of 2.85 MVar from the PCC. A portion (2.8 MVar) is absorbed for the purpose of voltage regulation while 0.05 MVar is used to supply the STATCOM converters DC side. At t = 0.3 s, the STATCOM supplies capacitive quadrature current, subsequently generating reactive power to maintain nominal voltage operation.

Figure 8 shows the resulting control signals at the different control blocks and as shown voltage regulation achieved between the time intervals ($0.2 < t < 0.3$) and ($0.3 < t < 0.4$).

Figure 9 shows the DC bus balancing across the capacitors of one module. The DC Bus voltage controlled to a nominal value of 1250 V across the 1000μF capacitor. As such, this would result in a converter transformer secondary voltage of 25 kV. At the time interval ($0.2 < t < 0.4$), the module bus capacitors experienced a voltage variation of 60 Volts (4.8%) while the flying capacitors experienced a deviation of approximately 62 Volts (9.9%). As noticed natural balancing occurs using PSWPM and the currents flowing through the flying capacitors were of an average value of zero. The peak to peak variation is 1kA (kilo-Amp) and imply capacitors need be rated at least (2 kA). This arrangement although suitable for simulation investigations is impractical, and need to be adjusted for practical purposes. As a solution/adjustment, more modules can be stacked per phase and as well the transformer ratio reduced.

5.2 Power Oscillating Damping based on MMFCC-STATCOM

In order to demonstrate this in Matlab-Simulink, during the time interval (0.15 < t <0.45), a variable load (shown in Figure 5.1) draws a current which pulsates at 10 Hz between 2kA and 5kA (i.e. 1.8MVA and 4.5MVA) at 600 Volts and a power factor of 0.9, resulting in voltage fluctuation of ±800 Volts (± 4%) at the point of common coupling. This would normally cause light bulbs to flicker and may even damage sensitive equipment connected.

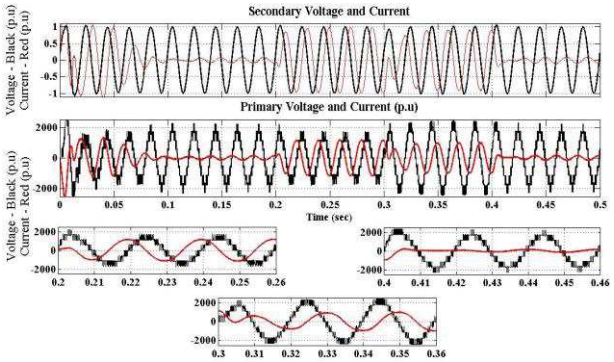

Figure 5: Converter Side Waveforms

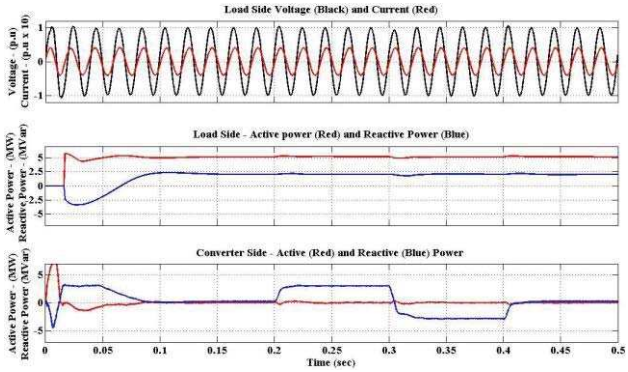

Figure 6: Load Side Waveforms

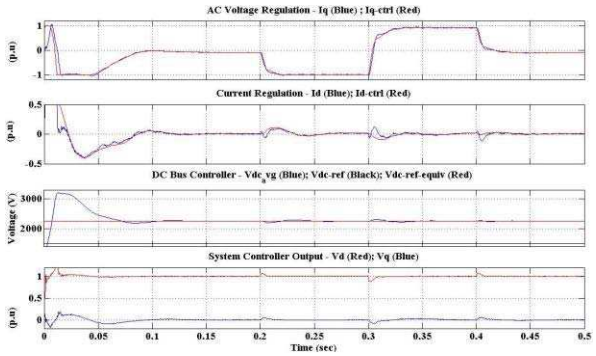

Figure 7: Power System Control Signals

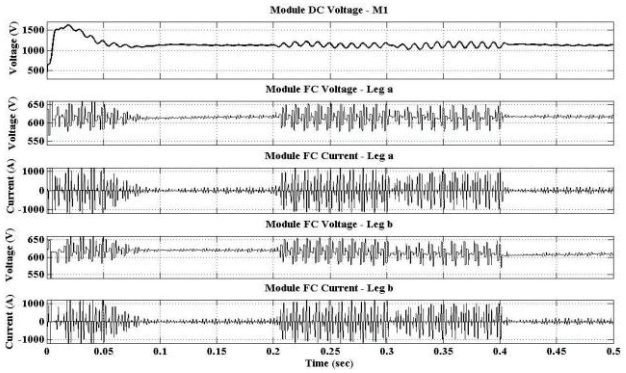

Figure 8: DC Capacitor Waveforms

To mitigate the situation the STATCOM controller is initiated at t = 0.3. This was done in order to observe the effect of the disturbance to the system voltages and currents without compensation between the time interval (0.15 < t < 0.3) and with compensation between the time interval (0.3 < t < 4.5). Results obtained from this scenario investigation are shown in Figure 9 – Figure 12.

In Figure 9, the power oscillations are evident in the supply side current which result in slight voltage oscillations on the PCC voltage. However from the time t = 0.3 till end of simulation, although the current still oscillates due to power demand, the voltage oscillations no longer exist.

The primary side voltage and current converter waveforms are shown in Figure 10. At 0.15 < t < 0.15 s, the converter secondary voltage (also the PCC voltage) shows a variation of (±0.04 p.u) due to the power oscillations. At 0.3 < t < 0.45 s, when the STATCOM controller initiates this reduces the PCC voltage fluctuation to (± 0.007 p.u). This is realized by injecting a current modulated to pulsate at the same frequency as the power oscillation. This current is varied between capacitive quadrature current to support when the power swings low (i.e. supplying reactive power) and inductive quadrature current to absorb when the power swings high. The response of the STATCOM converter to supply or absorb reactive power is fast around half a fundamental cycle.

Figure 11 shows the load voltage and current waveforms as well as the load side and converter side active and quadrature power waveforms successively. At t = 0.3 s, it is shown that the converter real power is maintained at zero under all conditions, while quadrature power is supplied or absorbed in order to compensate for power oscillation.

Figure 12 shows the resulting controls signals at the different control blocks and as shown the AC voltage regulator variables from the time t = 0.3 s, modulate at the same frequency as the load power oscillations in order to support the PCC voltage.

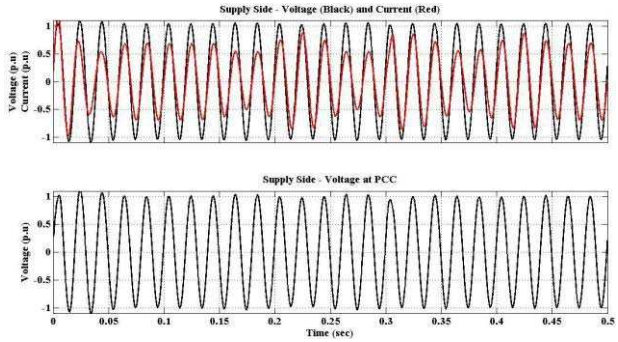

Figure 9: Power Supply (Line) Waveforms

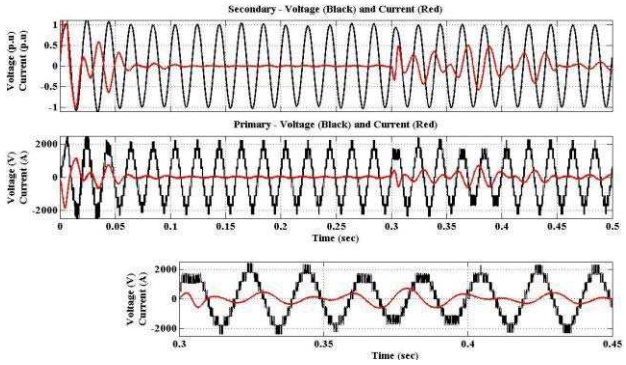

Figure 10: Converter Side Waveforms

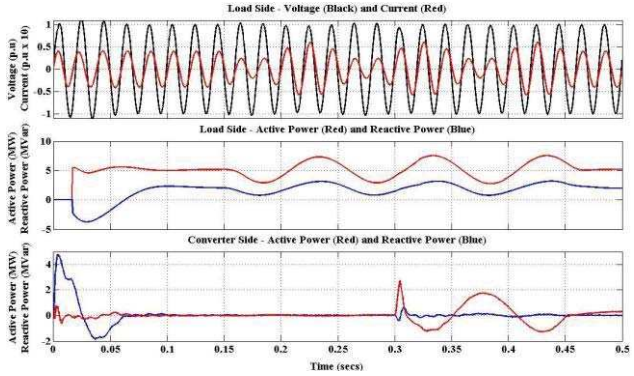

Figure 11: Load Side Waveforms

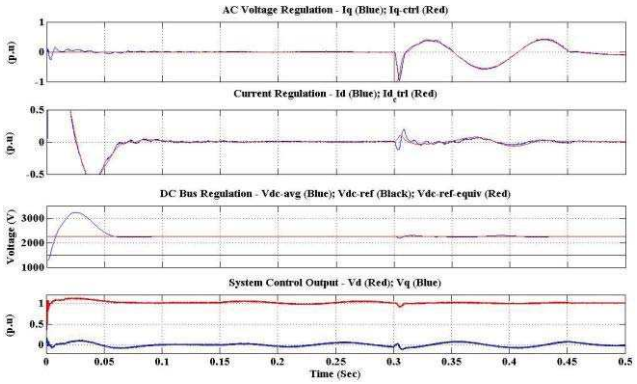

Figure 12: Power System Control Signals

6 Conclusion

This paper has discussed a MMFCC based STATCOM for reactive power control of a simulated 25kV 100MVA power system. Phase Shifted PWM scheme has been used to modulated the MMFCC converter. Simulation results for two different scenarios under this STATCOM control has verified that this topology is plausible and its operation for voltage regulation and power oscillation damping are shown with response times seen to be about 0.01s respectively when a disturbance is introduced. This paves the route for further investigations of the MMFCC in different high power applications.

References

[1] H. P. Mohammadi and M. T. Bina, "A Transformerless Medium-Voltage STATCOM Topology Based on Extended Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 1534-1545, 2011.

[2] D. Sixing and L. Jinjun, "A Study on DC Voltage Control for Chopper-Cell-Based Modular Multilevel Converters in D-STATCOM Application," *Power Delivery, IEEE Transactions on,* vol. 28, pp. 2030-2038, 2013.

[3] I. B. Efika and L. Zhang, "A Cascaded Flying Capacitor Multilevel Converter for HVDC and FACTs," in *Universities High Voltage Network (UHVNet)*, Winchester 2011.

[4] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3119-3130, 2011.

[5] I. B. Efika, L. Zhang, A. Watson, and J. Clare, "A Multi-level Multi-modular Flying Cpapcitor Voltage Source Converter," in *IECON 2013 - 39th Annual Conference on IEEE Industrial Electronics Society*, Vienna Austria, 2013.

[6] I. B. Efika, L. Zhang, A. Watson, and J. Clare, "An overlapping multi-hexagon space vector modulation scheme for modular multilevel cascade converters," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-11.

[7] C. J. Nwobu and L. Zhang, "Lifting wavelet transform and energy operator synchronization for a flying capacitor multi-level inverter based active power filter," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[8] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *Industry Applications, IEEE Transactions on,* vol. 48, pp. 720-729, 2012.

[9] F. Z. Peng, Q. Wei, and C. Dong, "Recent advances in multilevel converter/inverter topologies and applications," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 492-501.

[10] K. Ogata, *Mordern Control Engineering*: Prentice Hall, 1997.