

Original citation:

Chen, Han, Gammon, P. M., Shah, V. A., Fisher, Craig A., Chan, Chun, Jahdi, Saeed, Hamilton, Dean P., Jennings, Michael, Myronov, Maksym, Leadley, D. R. (David R.) and Mawby, P. A. (Philip A.) (2015) Cryogenic characterization of commercial SiC Power MOSFETs. In: Silicon Carbide and Related Materials 2014, Grenoble, France, Sep 2014. Published in: Materials Science Forum, 821-823 pp. 777-780.

Permanent WRAP URL:

<http://wrap.warwick.ac.uk/77866>

Copyright and reuse:

The Warwick Research Archive Portal (WRAP) makes this work by researchers of the University of Warwick available open access under the following conditions. Copyright © and all moral rights to the version of the paper presented here belong to the individual author(s) and/or other copyright owners. To the extent reasonable and practicable the material made available in WRAP has been checked for eligibility before being made available.

Copies of full items can be used for personal research or study, educational, or not-for-profit purposes without prior permission or charge. Provided that the authors, title and full bibliographic details are credited, a hyperlink and/or URL is given for the original metadata page and the content is not changed in any way.

Publisher's statement:

<http://www.scientific.net/>

<http://www.scientific.net/MSF.821-823.777>

A note on versions:

The version presented here may differ from the published version or, version of record, if you wish to cite this item you are advised to consult the publisher's version. Please see the 'permanent WRAP URL' above for details on accessing the published version and note that access may require a subscription.

For more information, please contact the WRAP Team at: wrap@warwick.ac.uk

Cryogenic Characterization of commercial SiC power MOSFETs

H. Chen^{1,a*}, P.M. Gammon^{1,b}, V.A. Shah^{1,2}, C.A. Fisher¹, C. Chan¹, S. Jahdi¹,
D.P. Hamilton¹, M.R. Jennings¹, M. Myronov², D.R. Leadley², P.A. Mawby¹

¹ School of Engineering, University of Warwick, Coventry, CV4 7AL, UK

² Department of Physics, University of Warwick, Coventry, CV4 7AL, UK

^a Han.Chen@warwick.ac.uk

^b P.M.Gammon@warwick.ac.uk

Keywords: Cryogenic, Silicon Carbide, MOSFET, Static, Switching

Abstract. The cryogenic performance of two commercially available SiC power MOSFETs are presented in this work. The devices are characterised in static and dynamic tests at 10 K intervals from 20-320 K. Static current-voltage characterisation indicates that at low temperatures threshold voltage, turn-on voltage, on-state resistance, transconductance, and the body diode turn-on voltage all increase while saturation current decreases. Dynamic, 60 V, 3A switching tests within the cryogenic chamber are also reported and the trends of switching speed, losses, and total power losses, which rise at low temperature, are presented. Overall, both MOSFETs are fully operable down to 20 K with both positive and negative changes in behaviour.

Introduction

Low temperature power electronics is of particular interest for space applications [1] and increasingly, in the potential co-location of control electronics next to a high-current superconducting device in, for example, the field winding of a synchronous machine [2]. Previously, the performance of both unipolar and bipolar Si power devices have been measured and modelled down at cryogenic temperatures [3,4]. Significant research has been conducted on the performance of SiC devices at high temperatures [5], though very little has been reported [6-8] of the operation of SiC devices at cryogenic temperatures. However, the shallow nitrogen donor in SiC means that freeze-out effects in unipolar SiC devices should occur at very low temperature, making cryogenic operation possible. In this work, two SiC power MOSFETs manufactured by Cree and Rohm are characterised. The results of static and switching tests on these devices at cryogenic temperature will be presented, extracting key parameters that

Experiment Setup

In the static test, 1200 V, 40 A Rohm (SCT2080KE) and Cree (CMF20120) MOSFETs are placed inside a cryogenic vacuum chamber (see Fig.1), to which a liquid helium cooler and the vacuum system are connected and the ambient temperature can be taken down to below 20 K. A temperature sensor and heating stage inside the chamber is linked to a temperature control unit connected to a PC, and hence the temperature can be automatically set from 20-320 K. The PC also controls the Agilent parameter analyser, and using LabVIEW software, it is used to automate the measurement process and temperature intervals.

In the dynamic test, a custom ‘chopper cell’ circuit, depicted in Figure 1, containing each MOSFET, the gate drive, the smoothing capacitors and respectively a Rohm SCS206AG Schottky diode and a Cree C3D06060 Schottky are placed in the chamber as shown in Fig.1. Dots in Fig.1 refer to voltage (red) and current (green) sense points measured by an oscilloscope. A standard double pulse measurement is applied to the circuit from the frequency generator, the inductor charging to 3 amps, before two switching events that occur at 125 kHz.

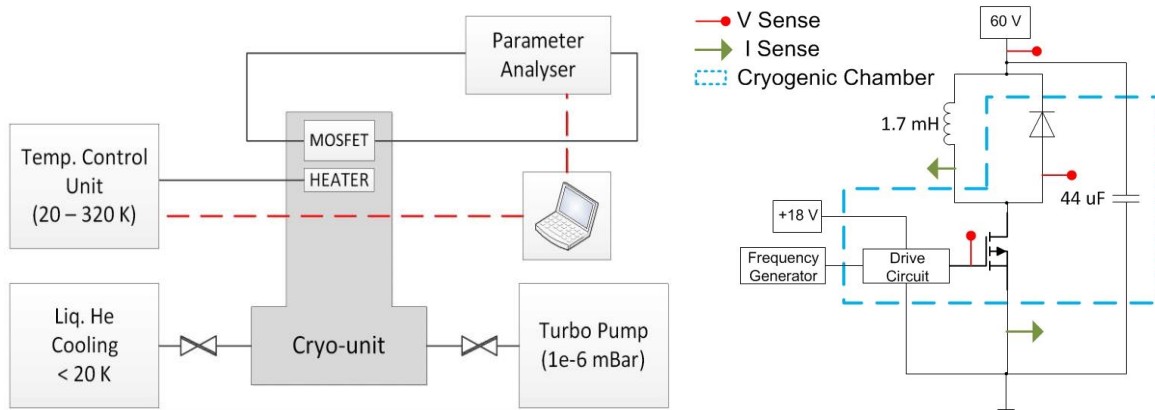


Fig.1 Left, the cryo setup for the static tests. Right, the cryo PCB used in the dynamic test.

Results of Static Tests

In the first of the static tests, Fig.2 and Fig.3 show the I_{DS} - V_{DS} plots of Cree and Rohm MOSFET at different temperatures, as they turn on, from gate voltages (V_{GS}) of 0, 5 and 10 V. The plots with $V_{GS}=0V$ give the temperature dependence of the body diode, essentially a p-i-n diode when the MOSFET is reverse biased. The turn-on voltage of the body diode can be seen to increase with decreasing temperature. This effect occurs at any temperature, the result of intrinsic carrier concentration (n_i) being exponentially proportional to temperature and where the saturation current, $J_0 \propto n_i^2/N_D$ [9]. A similar effect can be seen in the forward characteristics of the MOSFET and Fig.4 shows the sub-threshold current for both MOSFETs at $V_{GS}=V_{DS}=5V$. The exponential rise in this subthreshold current ($I_{DS,ST}$) with temperature is again linked to n_i as $I_{DS,ST} \propto \left(\frac{kT}{q}\right)^2 \frac{n_i^2}{N_A^{1.5}}$ [9].

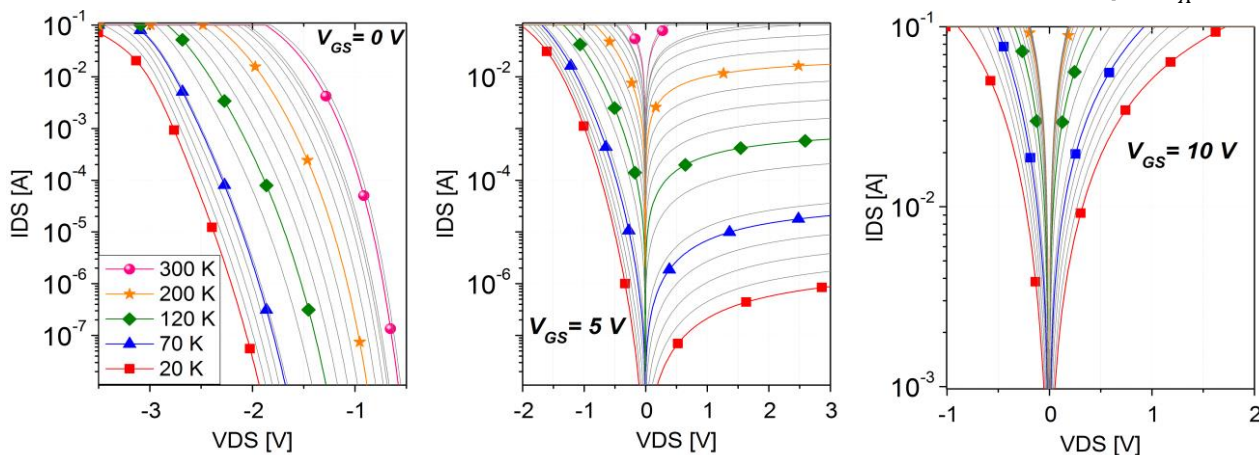


Fig.2 I_{DS} against V_{DS} of Cree MOSFET at different temperatures with varied gate voltage

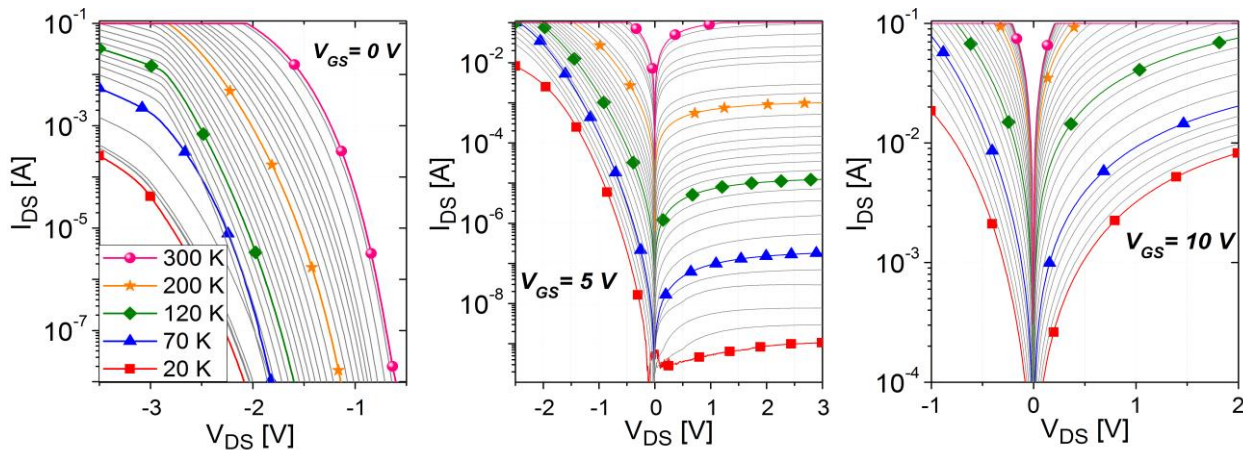


Fig.3 I_{DS} against V_{DS} of Rohm MOSFET at different temperatures with varied gate voltage

The turn-on voltage (V_{ON}) of both MOSFETs can be derived from the first test, which we define here as the voltage on the drain when the drain-source current reaches 0.1 A, with 20 V on the gate. Fig.5 shows that for both MOSFETs that V_{ON} is stable at 0.2V down to 80 K, below which they both rapidly increase. At 20 K, the V_{ON} has reached 0.4V for the Cree device, 1.2V for the Rohm device. The substantial increase is the first evidence of carrier freeze-out which effects series resistance and depletion region widths as, below 150 K, the number of ionized dopants exponentially decays.

A second static test was performed to determine the threshold voltage (V_T) and transconductance (g_m). With V_{DS} fixed at 20 V, the gate voltage was swept up from 0 V until I_{DS} reached 2A. A linear relationship between V_{GS} and I_{DS} allows the extraction of transconductance ($g_m=[dI_{DS}/dV_{GS}]_{MAX}$) while V_T is defined here as the zero current voltage when dI_{DS}/dV_{GS} is extrapolated to $I_{DS}=0$ [9]. Both characteristics follow the linear, inversely proportional relationship with temperature that is reported in their respective datasheets. These effects, like the subthreshold behaviour, are again due to the degraded concentration of intrinsic carriers at low temperature. However, below 190 K a sharp increase in both plots for the Cree MOSFET can be seen. We propose that this is due to the high ionisation energy of SiC acceptors, which means that the p-type channel suffers freeze-out effects at relatively high temperature. This has two effects, firstly causing the p-type channel to become fully depleted as the number of ionised holes in the channel drop below the number in both the source and JFET regions. Having overcome this effect with the increased V_T however, the channel region forms with minimal increase in V_{GS} , as there are fewer majority carriers to deplete.

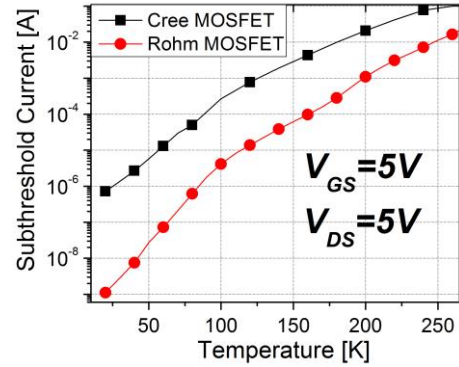


Fig.4 Temperature dependence of subthreshold current of the MOSFETs

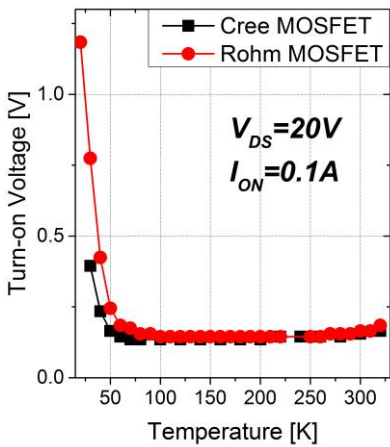


Fig.5 Turn-on voltage versus temperature

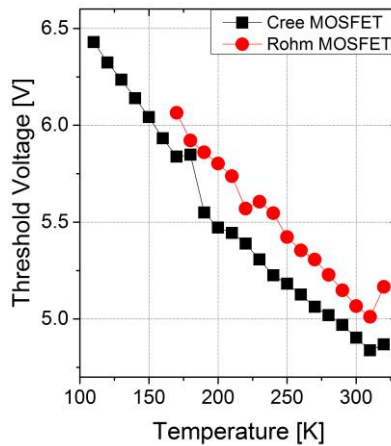


Fig.6 Threshold voltage against temperature

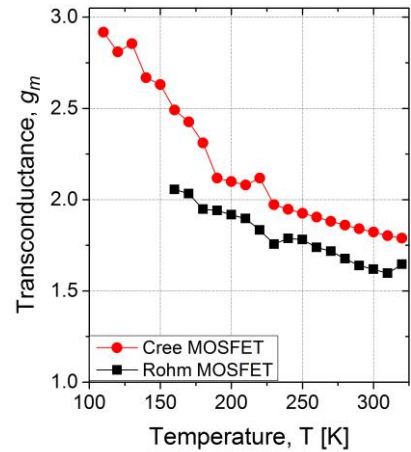


Fig.7 Transconductance against temperature

Results of Dynamic Tests

Switching speed, switching losses, conduction losses and total power loss were extracted from 60V/3A dynamic tests. As shown in Fig.8, the switching speed of the Cree MOSFET is relatively unaffected by the temperature, while the switching speed of the Rohm MOSFET tends to be slower at lower temperature. The reduction in switching speed could be attributed to the widening of the depletion region beneath the gate as temperature drops, and effect that would decrease both input capacitances C_{GS} and C_{GD} .

Fig.9 displays cumulative power losses accrued over one switching cycle, for each MOSFET at 30 and 220 K, found by multiplying the instantaneous values of V_{DS} and I_{DS} . The plots suggest that the majority of the energy lost is in the switching process, specifically turn-on, though the Rohm MOSFET can be seen to suffer massive conduction, and turn-off losses at 30 K, the result of freeze-out and hence massively increased resistance. In Figure 10, total power losses and the portion attribute to switching are compared for all measured temperatures. The conduction losses may be inferred from the difference in the two values. The Cree device can be seen to remain consistent down to 70 K, before switching losses rise slightly at 50 K. Below 150 K, the Rohm MOSFET much more effected, with both losses ramping steeply.

Conclusion

Cryogenic characterisation was carried out on two commercial SiC power MOSFETs, both of which continued to function to below 50 K. Static tests showed the effects of decreasing intrinsic carrier concentration on the subthreshold characteristics, while freeze-out effects were seen to increase turn-on voltage transconductance and threshold voltage. Meanwhile, increased switching and conduction loss was observed in the dynamic tests, particularly in the Rohm device, the Cree device operating very consistently down to 50K.

References

- [1] R.L. Patterson et al, *Journal de Physique IV (Proceedings)*, vol. 12 pp. 207 (2002).
- [2] A.J. Forsyth et al, *J. Power Electronics, IET*, vol. 5, pp. 739 (2012).
- [3] R. Singh and B.J. Baliga, *Cryogenic Operation of Silicon Power Devices*, Kluwer, (1998).
- [4] R. Singh and B.J. Baliga, *Proceedings of ISPSD '92*, pp.339 (1992)
- [5] P.G. Neudeck et al, *Proceedings of the IEEE*, vol.90, no.6, pp.1065 (2002)
- [6] P.M. Gammon et al., *Materials Science Forum*, vol. 778 pp. 863 (2014).
- [7] P. M. Gammon, et al., *Journal of Applied Physics*, vol. 114, pp. 223704 (2013).
- [8] L. Cheng et al, *Proceedings of ISPSD '05*, pp.231, (2005).
- [9] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices, 3rd Ed*, Wiley, New York, pp 95, 314 (2007).

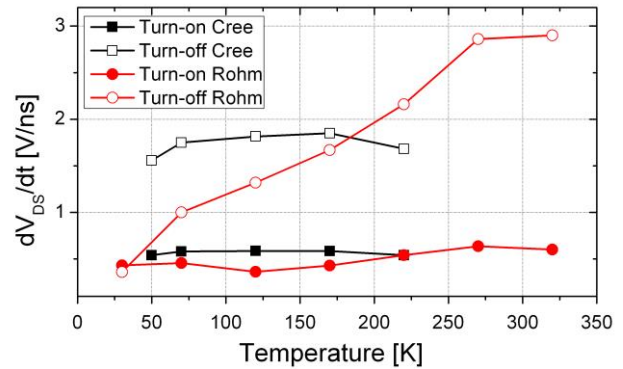


Fig.8 Switching speed against temperature

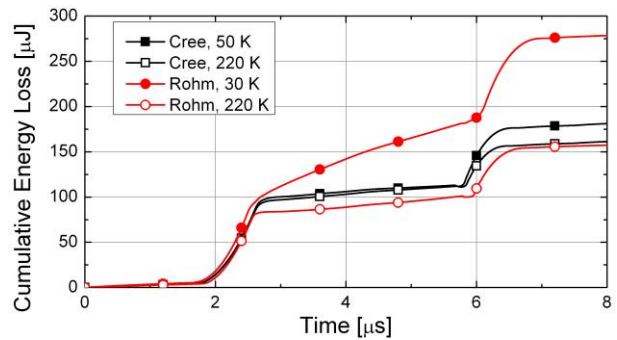


Fig.9 Cumulative energy losses with time over one switching cycle

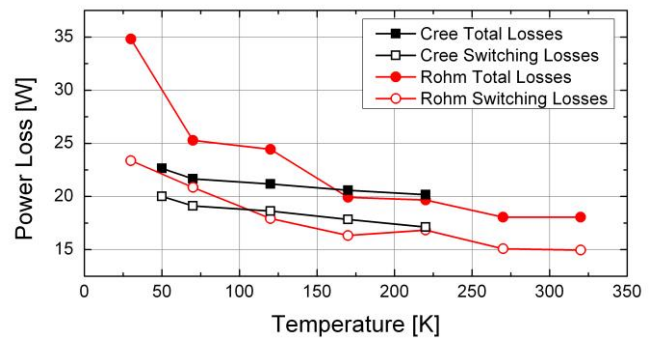


Fig.10 Total Power losses versus temperature