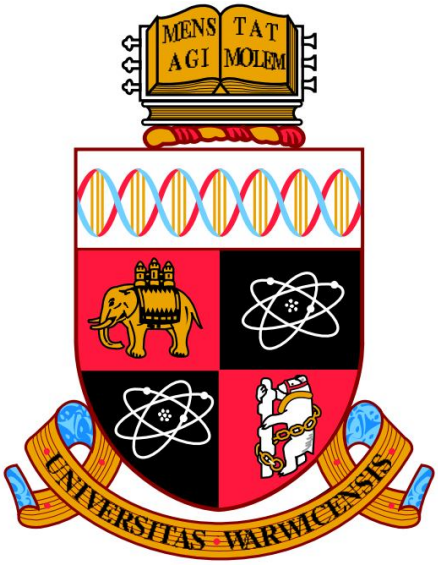
Modular Multilevel Converter: Submodule Dimensioning, Testing Method, and Topology Innovation



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DECLARATION

The work presented in this thesis is based on research carried out by the candidate in the School of Engineering, the University of Warwick, the UK. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all the candidate's own work unless referenced to the contrary in the text. The work presented in Chapter 3 and Chapter 4 has been partly published in C1 (list of publications by the candidate can be found in Chapter 1.7) and is submitted for further review for journal (J1). Some of the work presented in Chapter 5 has been published in C2. Majority of the work presented in Chapter 6 has been published in J2. The work presented in Chapter 7 has been published in (C4) and (J3). The work presented in Chapter 8 has been published in (C5) and (J4).

SUMMARY

The modular multilevel converter (MMC) is being developed as a core technology for the next generation of high-power, voltage source converters (VSCs). The focus of this thesis lies in the SM dimensioning, testing method and topology innovation for the MMC.

First, the thesis presents a new submodule (SM) capacitor selection method, considering the three main voltage requirements: the maximum capacitor voltage, the voltage ripple and the SM voltage capability. The effect of the arm inductor is included. A quick way to estimate the capacitor ripple current stress is also provided to check the selection.

Second, the thesis proposes two model assisted SM testing schemes for the MMC. The prototype SM can be thoroughly tested according to the targeted operating modes without having to build a complete MMC. During the test, the converter arm current can be faithfully achieved, which contains not only the fundamental frequency component, but also dc offset and harmonic circulating current components. One scheme is the uncompensated testing scheme, which uses fewer devices, and has simpler control and faster transient dynamics. The other is the compensated testing scheme, which requires much lower dc supply voltage, smaller coupling inductance, and provides higher current tracking accuracy in steady state. Both testing schemes have been verified through simulation and experiments.

Third, the thesis proposes a compact SM topology for the MMC based on stacked switched capacitor (SSC) architecture. Feasibility study shows that the total physical volume of all capacitors in each SM can be reduced by more than 40% without significantly increasing the power loss. Design concept and control principles are presented. Practical considerations for a high-voltage, high-power system are also provided, which are demonstrated through experiments on a scaled down laboratory prototype SM.

Finally, this thesis evaluates the offshore 50/3 Hz ac power transmission and the use of back-to-back (B2B) MMC for frequency conversion. The high-level design of a B2B MMC is presented. System performance is briefly evaluated using computer simulation.

NOMENCLATURE

ac	alternative current
dc	direct current
rms	root mean square
B2B	back-to-back
BJT	bipolar junction transistor
CCSC	circulating current suppression controller
CSC	current source converter
EMC	electromagnetic compatibility
ESL	equivalent series inductance
ESR	equivalent series resistance
FB	full-bridge
GD	gate driver
GTO	gate turn-OFF thyristor
HB	half-bridge
HVAC	high voltage alternative current
HVDC	high voltage direct current
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
LF	low frequency
LPF	low pass filter
MLCC	multi-layer ceramic capacitor
MMC	modular multilevel converter
MOSFET	metal oxide semiconductor field effect transistor
MPPF	metalized polypropylene film
OP	system operating point that varies with m and φ
PCC	point of common coupling
PI	proportional-integral
PR	proportional-resonant
PSC-PWM	phase-shifted carrier-based PWM
PSU	power supply unit
PWM	pulse width modulation
SCR	short circuit ratio
SiC	silicon carbide

SM	submodule
SSC	stacked switched capacitor
STATCOM	static VAr compensation
STC	system operator transmission owner code
THD	total harmonic distortion
VSC	voltage source converter
XLPE	cross-linked polyethylene
i	indexing parameter
j	indexing parameter
k	indexing parameter
A	magnitude of the ac component at fundamental frequency in "arm current"
A_e	a system coefficient defined in (4.18)
C	capacitance
C_0	backbone capacitor capacitance
C_1	supporting capacitor capacitance (high voltage one)
C_2	supporting capacitor capacitance (low voltage one)
C_{ori}	capacitor capacitance in an original HB-SM
C_{SM}	capacitance of SM capacitor
$D_{1/2}$	upper/lower diode in a HB-SM
$Diff_W$	difference between W_{armdc} and W_{base} in p.u. based on W_{base}
$Diff_{W\_e}$	estimated $Diff_W$
ε	capacitor voltage ripple (peak to average) in p.u.
$e_{arm\_cap\sim}$	periodic energy variation in arm capacitors
$e_{arm\_cap\sim p.u.}$	p.u. value of $e_{arm\_cap\sim}$ based on W_{base}
$E_{arm\_cap\sim p.u.max}$	maximum value of $e_{arm\_cap\sim p.u.}$ for a certain OP
$E_{arm\_cap\sim p.u.min}$	minimum value of $e_{arm\_cap\sim p.u.}$ for a certain OP
$E_{con,k}$	conduction loss, $k=T$ for IGBT or $k=D$ for diode
e_j	inner emf generated by MMC phase units
E_p	$p=TswOn$ for IGBT switch-ON loss, $p=TswOff$ for IGBT switch-OFF loss and $p=Drec$ for diode reverse recovery loss
$Error_{cap}(.)$	relative error in the value of f_{cap} when neglects $Diff_W$
$Error_{ripple\_DiffW}(.)$	relative error in the value of f_{ripple} when neglects $Diff_W$
$Error_{ripple\_Vripplep.u.}(.)$	Relative error in the value of f_{ripple} with various $V_{ripplep.u.}$ settings
$E_{swtot,p}$	total switching loss, $p=TswOn$, $p=TswOff$ or $p=Drec$
$f(.)$	function defines the shape of the arm energy variation
$f_{cap}(.)$	function describes the C_{SM} demand for the SM voltage capability

	requirement
$f_{excess}(.)$	function describes the C_{SM} demand for the maximum voltage requirement
$f_{ICripple}(.)$	function describes the capacitor ripple current stress requirement
f_{max}	maximum value of f for a certain OP
f_{min}	minimum value of f for a certain OP
$f_{ripple}(.)$	function describes the C_{SM} demand for the voltage ripple requirement
f_s	sampling frequency of the test platform
f_{sw_max}	maximum switching frequency of the FB converter
H_{band}	hysteresis band
H_{sig}	hysteresis control signal
I_0	device current
I_{2f}	peak current of the 2nd order circulating currents
$i_{arm\_p/nj}$	instantaneous upper (p) or lower (n) arm current of phase j
i_{arm_ref}	arm current reference
I_{dc}	converter dc current
i_{diffj}	inner difference current of phase j
I_e	magnitude of high frequency current due to hysteresis switching
i_{error}	current tracking error
dI_{error_delay}	maximum step of i_{error} during a switch-delay period
dI_{error_max}	maximum step of i_{error} during a sampling period
i_j	converter ac output current of phase j
ΔI_{max}	permitted maximum current error
dI_{max}	the maximum current change in a ΔT
I_s	rms value of the ac side current
i_{SM}	SM current
i_{aux}	auxiliary SM current
i_{SMC}	SM capacitor current
$I_{thres+/-}$	current threshold
φ	power factor angle in the ac side
φ_0	initial phase angle
φ_{arm_cap}	actual power factor angle when considers the arm inductors
$k_{\Delta Imax}$	current tracking error constant
K_{dc}	ratio between NV_{SMdc} and V_{dc}
K_i	integral gain
K_p	proportional gain
k_{SMCac}	ratio between the p-p prototype SM voltage ripple and its rated dc voltage
k_{auxCac}	ratio between the p-p auxiliary SM voltage ripple and its rated dc voltage

L	coupling inductor inductance
L_0	initial inductance for calculation
L_{arm}	inductance of arm inductor
L_{max}	maximum inductance for the coupling inductor
m	voltage modulation index
m_{arm_cap}	actual modulation index when considers the arm inductors
N	number of SMs in each arm
N_{on}	number of inserted SMs
P_{ac}	converter ouptut active power
p_{arm_cap}	instantaneous power into arm capacitors
P_{con}	average conduction loss power
P_s	apparent power
Q_{ac}	converter output reactive power
R	ON-state resistance of IGBT/diode
R_{arm}	parasitic resistance representing all converter Ohmic losses
R_s	starting resistor
S	switch
T	period of a fundamental cycle
$T_{1/2}$	upper/lower transistor in a HB-SM
ΔT	sampling period of the test platform
$u_{arm\_p/nj}$	instantaneous upper (p) or lower (n) arm voltage of phase j
u_{diffj}	difference voltage of phase j
V_0	IGBT/diode junction voltage
$v_{\sim}$	total SM capacitor voltage ripple of one arm (=$Nv_{SM\sim}$)
$v_{\sim p.u.}$	p.u. value of $v_{\sim}$ with respect to NV_{SMdc}
$V_{\sim p.u.max}$	maximum value of $v_{\sim p.u.}$ for a certain OP
$V_{\sim p.u.min}$	minimum value of $v_{\sim p.u.}$ for a certain OP
$\widehat{V}_{\sim p.u.n}$	amplitude of the nth order component in $v_{\sim p.u.}$
v_{auxC}	auxiliary SM capacitor voltage
v_{auxout}	auxiliary SM output voltage
v_{bus}	energy buffer dc bus voltage
v_C	capacitor voltage
V_{CE}	device collector-emitter voltage
V_{CE_ref}	device reference V_{CE} in datasheet for switching loss calculation
v_{conv_j}	converter ac output voltage of phase j

V_{Crated}	capacitor rated voltage
V_{dc}	converter pole-to-pole dc bus voltage
$V_{\text{excessp.u.}}$	voltage excess in p.u. based on V_{SMdc}
v_{FB}	FB converter output voltage
v_j	device ON-state voltage drop, j=CE for IGBT or j=F for diode
v_{L}	coupling inductor voltage
V_{Lmax}	maximum coupling inductor voltage
V_{Lmin}	minimum coupling inductor voltage
V_{r}	capacitor rated voltage
$V_{\text{ripplep.u.}}$	voltage ripple (peak-peak) in p.u. based on V_{SMdc}
V_{s}	rms value of the ac side phase voltage
V_{s} (Chapter 7)	full-bridge converter dc supply voltage
v_{SM}	average $v_{\text{SM}ij}$ of all SMs in one arm
$v_{\text{SM}ij}$	SM capacitor instantaneous voltage of SM i in arm j
$v_{\text{SM~}}$	average $v_{\text{SM~}ij}$ of all SMs in one arm
$v_{\text{SM~}ij}$	ac components (voltage ripple) of $v_{\text{SM}ij}$
$\widehat{V}_{\text{SMCac}}$	amplitude of prototype SM capacitor voltage ripple
v_{SMC}	prototype SM capacitor voltage
v_{SMout}	SM output voltage
V_{auxCdc}	auxiliary SM capacitor rated dc voltage
$\widehat{V}_{\text{auxCac}}$	amplitude of auxiliary SM capacitor voltage ripple
V_{SMdc}	average $V_{\text{SMdc}ij}$ of all SMs in one arm
V_{SMCdc}	SM rated dc voltage
$V_{\text{SM\_dcmax}}$	maximum SM dc bus voltage
$V_{\text{SM\_dcmin}}$	minimum SM dc bus voltage
$V_{\text{SMdc}ij}$	time average (dc component) of $v_{\text{SM}ij}$
v_{SMdiff}	output voltage difference between the auxiliary SM and the prototype SM
v_{SMtot}	total SM capacitor voltage of one arm
V_{thres}	threshold voltage
ω	fundamental angular frequency
ω_{e}	angular frequency of high frequency current due to hysteresis switching
$w_{\text{arm\_cap}}$	instantaneous energy storage in arm capacitors
$W_{\text{armdc\_cap}}$	time average (dc component) of $w_{\text{arm\_cap}}$
W_{base}	base arm energy storage

1 INTRODUCTION

1.1 History of HVDC Transmission

In 1876, Thomas Alva Edison established his research laboratory at Menlo Park, New Jersey. Six "jumbo dynamos" of 100 kW were built, each connected directly to a high-speed steam engine and capable of lighting 1,200 light bulbs. On 4th Sept. 1882, the New York financial district became the first place in the world to be lit by electricity [1]. The electric era had begun, using direct current (dc).

The development of high voltage dc (HVDC) technologies started to accelerate in the 1950s. Two major players were Russia and Sweden. Russia needed high-power long-distance HVDC transmissions to economically connect its vastly distributed population centres. Sweden needed subsea dc to supply its islands with cheap hydropower from the mainland. The first commercial HVDC system order was for the link between the island of Gotland in the Baltic and the Swedish mainland [1, 2]. Interestingly, since Gotland had no local generation, the dc link has to start this region without relying on any external network, which is usually referred to as *black start*. To solve the problem, the brilliant engineers

installed a 30 MVA synchronous condenser at the inverter station on Gotland.

Today, the demand for HVDC transmission is much higher than ever before, for a number of reasons. Firstly, the need to transmit large amounts of electric energy over long distances is increasing [3]. The best and most cost-effective renewable resources (hydro, wind and solar) are often found far from load centres. Also, electricity market liberalization is progressing in many countries, leading to longer distance trading for economic reasons [3]. Transmission losses with long-distance ac systems (up to 500 kV) together with stability, right-of-way, and infrastructure permitting problems can cause difficulties. Secondly, increasing amounts of energy resources are located offshore like wind and marine power. Due to the massive reactive charging current in ac cables, the transmission distance is largely limited [4, 5]. HVDC in general can help to solve the above technical challenges. When compared with HVAC, the most common arguments favouring HVDC include the following [2]:

- Lower overall investment costs in long-distance transmission;
- Lower losses due to the absence of reactive power flow and the use of only two power lines instead of three in HVAC systems.
- The potential for asynchronous interconnection;
- Higher system controllability and stability, helping to prevent cascading disturbances;
- Enhanced environmental solutions (less space taken).

1.2 Recent Developments in Power Semiconductor Devices

Before the 1970s, mercury arc technology dominated. Figure 1.1 shows a six-pulse converter valve group for the Gotland link, using mercury-arc valves [1]. Due to the complexity and high costs of construction and maintenance, the solid-state semiconductor-

based switches took over from mercury arc valves in the late 1970s [1]. The first thyristor was installed in the Gotland link for an additional 10 MW power upgrade [6].

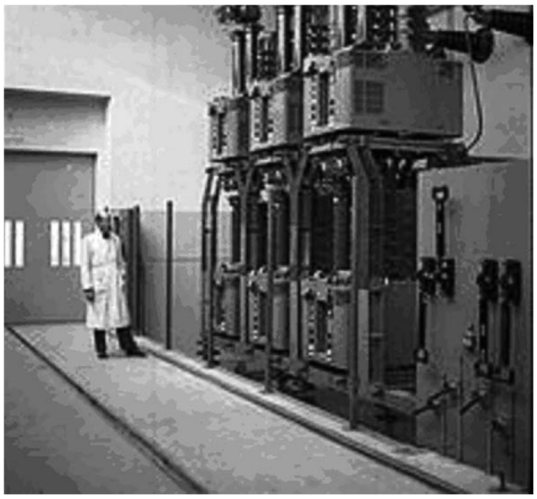

Figure 1.1: A six-pulse converter valve group for the Gotland link

1.2.1 Thyristor valve

Thyristors, or silicon-controlled rectifiers are a family of power semiconductor devices which are extensively used in power electronic circuits [7]. Conventional thyristors are designed without a gate-controlled turn-OFF capability. In normal operations, the thyristor can only recover from a conducting state to a non-conducting state when the current is brought to zero by other means. The gate turn-OFF thyristors (GTOs) and integrated gate commutated thyristors (IGCT) are designed to have both controlled turn-ON and turn-OFF capabilities.

Compared to transistors, thyristors usually have lower conduction loss and higher power handling capability. Currently, the current capability of one thyristor can be higher than 4 kA, and the voltage blocking capability can be higher than 8 kV [8].

Conventional GTOs were the most frequently used gate controlled semiconductors in high-voltage and high-power applications. However, their bulky and expensive snubber

circuits, complex gate driver, as well as the relatively high power to drive are their major disadvantages. The IGCT was developed based on the conventional GTO structure with an improved gate driver, packaging, and turn-OFF process. The IGCT has very high voltage blocking capability that can be up to 10 kV.

1.2.2 Insulated gate bipolar transistor (IGBT)

The insulated gate bipolar transistor (IGBT) improved significantly ever since its first commercial demonstration in 1983 [9, 10]. Today, for high-voltage high-power applications, its blocking voltage can be 3.3 kV, 4.5 kV and even 6.5 kV with 1.5 kA, 1.2 kA and 0.75 kA conducting current respectively. The major problem for the IGBT is its high switching losses at high switching frequency [11].

There are two types of packaging for 3.3 kV, 4.5 kV and 6.5 kV IGBTs: i.e. the module packaging and the press-pack packaging. In the module design, each chip is covered by a very thin (a few micrometers) aluminium metallization layer. The IGBT and diode chips are connected by aluminium wires that are bonded to the chip metallization layer using ultrasonic soldering [9]. As an example, 450 wires are required in a 3.3 kV, 1.2 A IGBT module. To protect the wire bond soldering, the power module is filled with silicone gel [12].

The major advantage of the module packaging is the full insulation of the base plate, leading to simple cooling and low packaging costs. However, its major drawbacks are the poor power cycling capability, the undefined failure mode after short circuits that cannot be turned off, and the possible explosion during the failure mode [12].

To overcome these disadvantages, ABB, Fuji, Eupec, and Toshiba developed the press-pack IGBTs. The current and heat flow through the devices are achieved by press contacts. The press-pack structure will behave as a short circuit after the IGBT and/or diode chips

have been destroyed, which is preferable in applications with redundant series-connected devices in stacks. In such a case, the converter can continue its operation until the planned system services. The avoidance of explosion during the failure and the possible increased reliability are major advantages of the press-packs. However, their shortcomings are the increased costs and the required insulation between each switch and the cooling system [12].

1.2.3 Future trends

Silicon carbide (SiC) will be a future material for power semiconductors due to its marvellous physical properties such as its wide energy gap, high breakdown electric field, high thermal conductivity, high saturated electron drift velocity, high inertness to chemical reaction, and its high pressure and radiation resistance [12]. Calculated and measured electrical and thermal characteristics of SiC devices promise a drastic reduction in ON-state and switching losses and an operation at a junction temperature of up to T_j = 600 °C. SiC thyristors have been successfully developed which can offer low ON-state voltage and multi-kilohertz switching at high temperatures even for a 10-25 kV blocking voltage [13]. Such high-voltage devices will have important utility applications in the future because they can greatly reduce the number of series connected devices as compared to silicon, leading to a huge reduction in size, weight, control complexity, and cooling requirement of power electronics systems. Also system efficiency and reliability can be largely improved [7].

1.3 Power Converters

1.3.1 Current source converter (CSC)

As the name indicates, the current source converter (CSC) likes to see a stiff dc current

source at the input (ideally with infinite *Thevenin* impedance). The current source can be achieved by connecting a large inductor (inductance) in series with a variable voltage source that is controlled by a current feedback loop. With a stiff dc current source, the ac output currents will not be affected by load conditions. Since power semiconductor devices in a CSC must withstand reverse voltage, symmetric voltage blocking devices such as thyristors are usually used [11].

CSCs have been the only HVDC transmission solution for many decades and they are still the first choice for bulk power transmission at the GW-level [14-16]. A CSC is usually based on a 12-pulse bridge configuration as shown in Figure 1.2. Three ac connectors are on the left hand side and two dc terminals are on the right hand side. Two of such 12-pulse bridges are usually connected in series to form the positive and negative terminals of the dc bus as shown in Figure 1.3. The advantage of such a structure is that one pole can continue to transmit power in the case that the other one is out of service for whatever reason. Each system can operate on its own as an independent system with the earth return [14]. Projects at a dc voltage of ±800 kV are also termed ultra-high voltage (UHV) dc systems and they usually consist of two such series connected 12-pulse bridges per pole.

The advantages of the CSC-HVDC system include a high overload capability, excellent robustness, reliability and low operational losses. The total loss of an ac transmission system with 6.4 GW capacity at 1,000 kV is around 7% per 1,000 km, while the line loss of a ±800 kV HVDC with the same capacity is only 3.5%. Even when the 0.7% converter losses per station are included, the total loss of a CSC-HVDC system is still much lower than the HVAC option [16].

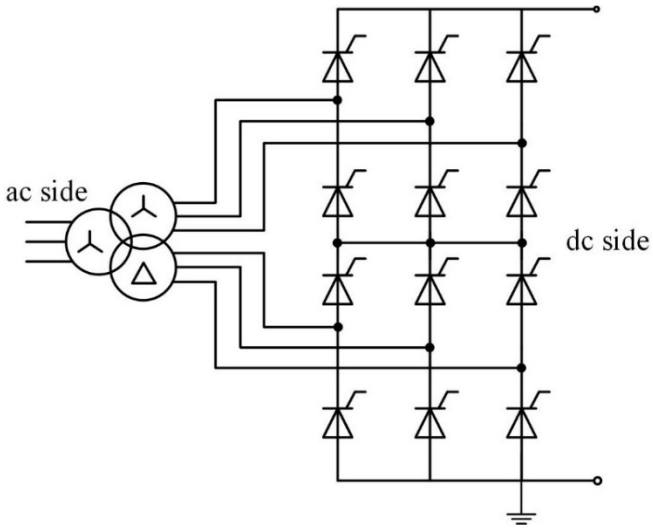

Figure 1.2: A 12-pulse converter bridge [16].

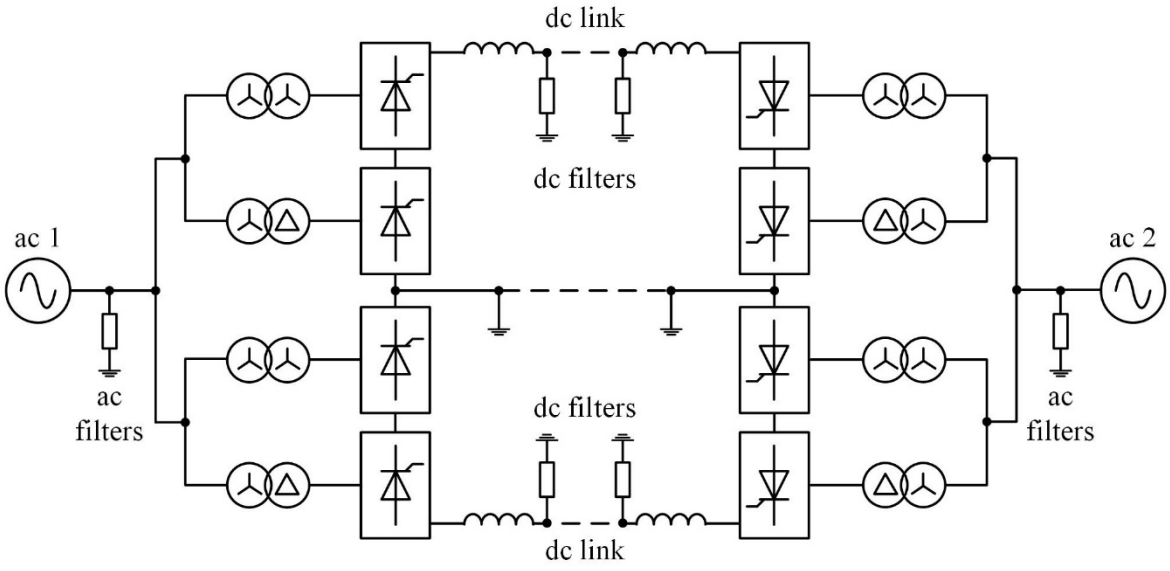

Figure 1.3: A bipolar CSC-HVDC system with one 12-pulse bridge per pole [14].

Although the CSC-HVDC serves the transmission industry well, it has a number of drawbacks:

- First, the ac outputs contain significant low order harmonics, which will cause various power quality problems, leading to higher losses and the malfunction of sensitive loads [11]. Massive filters are necessary on both the ac side and dc side for smooth power outputs [2].
- Second, due to the absence of the turn-OFF capability in the thyristor, the commutation of the switch is driven by the interconnected ac grid and the current is always lagging, i.e. keeps absorbing reactive power from the grid. As a result, massive reactive power compensation equipment is required on the ac side.
- Third, the direction of the power flow cannot be reversed by reversing the dc current due to the switch configuration. The change of power flow direction can only be achieved through a change in dc polarities. As a result, the relatively cheap and light polyethylene insulated dc cables are not suitable due to their poor fast polarity reversal capability [16]. This is also one of the major obstacles to building a multiterminal dc grid using CSC technology.
- Finally, the CSC-HVDC is sensitive to the strength of the interconnected ac system. Particularly at the inverter side, slight disturbances in the ac system may lead to commutation failure in the converter. Consecutive commutation failures may lead to system breakdown.

1.3.2 Voltage source converter (VSC)

Voltage source converters (VSCs), as the name indicates, receive dc voltage at one side and convert it to ac voltage on the other. A VSC prefers a stiff dc voltage source at the input (ideally zero Thevenin impedance) which is usually achieved using large capacitors [11].

Ever since the first VSC project (±10 kV, Hellsjon experimental project) was built in 1997, the voltage and power ratings of VSCs have steadily increased. Currently, VSC systems with ratings of up to ±320 kV, 1 GW are technically achievable [2]. Figure 1.4 shows the simplest VSC topology, i.e. the two-level ac/dc converter (with IGBT/diode modules). In VSCs, the power semiconductor switches always remain forward-biased due

to the dc bus voltage V_{dc}, and therefore, not only IGBTs, but all other self-controlled forward or asymmetric blocking switches, such as GTOs, BJTs, power MOSFETs, and IGCTs can be used. A diode is always connected across the device to achieve free reverse current flow and ensure the four-quadrant operation of the converter. Since the blocking voltage of currently available IGBT modules is only up to 6.5 kV, in order to block the voltage up to a few hundred kV, large amounts of IGBT modules are directly connected in series as shown in the dashed box in Figure 1.4. Typically, VSCs are controlled through pulse width modulation (PWM) techniques, among which the sinusoidal PWM (SPWM) is the simplest and thus is commonly adopted for industrial converters [11].

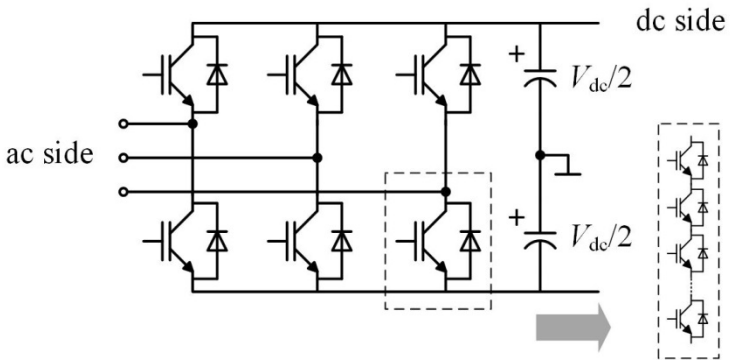

Figure 1.4: Diagram of a two-level VSC

When compared with the thyristor-based CSC-HVDC system, the IGBT-based VSC-HVDC system has the following benefits [17]:

- Both the amplitude and phase angle of ac output voltages can be controlled independently, offering independent and rapid control of the active and reactive power. The fast dynamic can help to enhance the transient stability of the inter-connected ac grid;
- Owing to the self-commutation capability of the IGBT, VSCs can operate in all four quadrants of the *P*-*Q* operating plane without external reactive power compensation;

- VSCs can operate with weak ac networks with a low short circuit ratio (SCR). They are able to start a dead network without any auxiliary equipment, which is usually referred to as *black start*;
- Power reversal can be achieved through reversing the dc current instead of the dc voltage polarities, which is critical for a multiterminal dc grid [18];
- Due to the high frequency of switching, the harmonics that need to be filtered are at high frequencies and thus the filtering demands are largely reduced;

On the other hand, two- and three-level VSCs have their own disadvantages:

- In order to achieve the high voltage rating, large amounts of IGBTs are connected in series, demanding very complex gating and protection schemes [19, 20];
- The PWM process requires the simultaneous switching of series-connected devices at high frequencies (one to a few kHz), leading to significant power losses (typically 1.6% per station [21]). This is one major reason why the CSC-HVDC is still preferable for bulk power transmissions.

The situation began to change with the advent of the modular multilevel converter (MMC), which was a milestone in VSC technology. This concept was first proposed by R. Marquardt [22] in 2001 and in 2010 the first MMC project started commercial operations, i.e. the *Trans Bay Cable* in the United States rated at ±200 kV, 400 MW.

Figure 1.5 shows a typical configuration of a dc to three-phase ac MMC system. A 'valve' in the converter arms is no longer a single IGBT/diode module but a controllable VSC itself, which is usually referred to as *submodule* (SM) or *cell*. A SM can be a half-bridge (HB) converter as shown in the dashed line box (Figure 1.5), a full-bridge (FB) converter, or it can appear in other forms [23]. Direct series connection of power switches is no longer needed. Each SM can be switched as low as the ac line frequency leading to increased efficiency and reduced cooling demands. Typical losses for one MMC station can be less than 1.0% [19, 24]. The large number of steps in the synthesized ac voltage

waveform provides low distortion and good EMC performance. Hence, harmonic filters become a thing of the past for both the ac side and dc side.

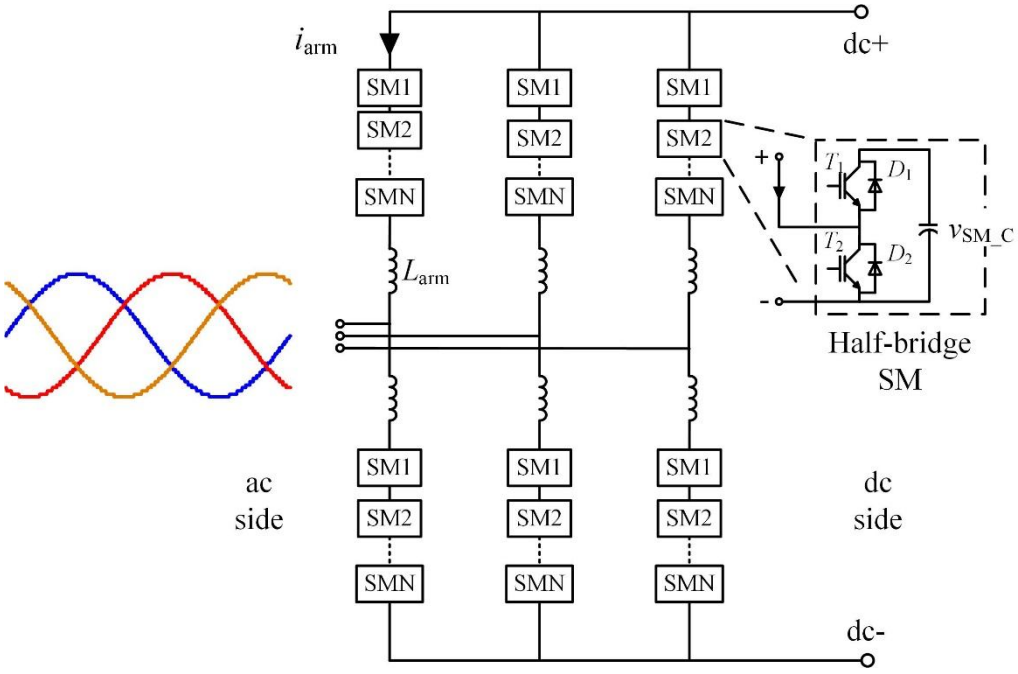

Figure 1.5: Typical configuration of a dc to three-phase ac MMC system

1.4 Offshore Wind Power Integration

One major application of HVDC transmission is the integration of offshore wind power. When compared with onshore wind, offshore wind has higher and more constant wind speeds, and lower direct visual and environmental impacts [25]. The UK has been the world leader in offshore wind since October 2008, with as much capacity already installed as the rest of the world combined [26]. With 4.2 GW capacity currently in operation, the total offshore generation capacity in the UK waters provides over 13 TWh of electricity annually. Industry projections see a total of around 6 GW of capacity installed by 2016 and around 10 GW by 2020, at which point offshore wind will supply 8% to 10% of the UK's electricity annually [26].

Trends in offshore wind can be concluded as further, deeper and larger [27]. Due to environmental laws and the limited space close to shore, wind farms tend to be built further from shore at the distance greater than 200 km. This greater distance usually leads to deeper water at the site but also has the potential for larger wind farms. The deeper water requires new foundation solutions to safely install wind turbines at relatively low cost. The greater distance means that HVAC technology is no longer a suitable option for power transmission to shore. This can be explained by the massive capacitive charging current in ac cables which will significantly limit the transmission distance [4]. One option is to use HVDC and another is the recently proposed low-frequency ac transmission [4, 28]. Many aspects must be considered when selecting the technology for power integration and transmission, including the installation costs of the offshore platform, the costs of the converter equipment, as well as the operation and maintenance costs.

1.5 Research Objectives and Contribution

This research considers the dimensioning, testing and topology innovation of the MMC SMs. The main research objectives are as follows:

- Identify and quantify dimensioning criteria for SM capacitors in the MMC, which are the system's major energy storage elements;
- Develop a new testing method for the MMC SMs taking advantage of the system's modularity. The test can be performed with, preferably, one or a few SMs without a complete MMC system;
- Explore new SM circuits for the MMC with features specifically suitable for space-limited applications such as offshore platforms or urban substations.

The thesis makes the following original contributions to the wider research in this topic area:

- A novel method to select MMC SM capacitors, especially in applications of HVDC transmission and static VAr compensation (STATCOM). The method can help to understand the effects of the MMC's operating mode and different design parameters on the demand of SM capacitor capacitance and rated voltage. It also provides a comprehensive understanding of how SM capacitors will limit the operating region of the converter;
- An evaluation of the offshore 50/3 Hz ac power transmission and the use of back-to-back MMC system for frequency conversion;
- A novel model assisted SM testing scheme for an MMC. The SMs can be thoroughly tested without a complete MMC;
- A compensated model assisted SM testing scheme with significantly reduced dc power supply and coupling inductor demands;
- A compact SM topology based on the stacked switched capacitor (SSC) architecture. The total physical volume of capacitors in each SM can be reduced by more than 40% without significantly increasing the power loss.

1.6 Outline of Thesis

The outline of the thesis is as follows: Following this introductory chapter, Chapter 2 reviews the basic operation and control of the MMC. Three different kinds of capacitors are reviewed and compared in Chapter 3. The metalized polypropylene film (MPPF) capacitor is a popular choice for MMC SMs and its main ageing mechanisms are reviewed. The new capacitor selection method is presented in Chapter 4. Chapter 5 evaluates the offshore 50/3 Hz ac power transmission and the use of back-to-back MMC for frequency conversion. Chapter 6 presents a novel model assisted SM testing scheme, and Chapter 7 provides the compensated model assisted SM testing scheme. The SSC based MMC SM is proposed in Chapter 8, and finally, the conclusions from this research and suggestions for

future work are presented in Chapter 9.

1.7 List of Publications

C1. **Y. Tang**, L. Ran, O. Alatise, and P. Mawby, "Capacitor selection for modular multilevel converter," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, Pittisburgh, PA, USA, pp. 2080-2087, (2014).

J1. **Y. Tang**, L. Ran, O. Alatise, and P. Mawby, "Capacitor selection for modular multilevel converter," submitted to *IEEE Trans. Ind. Appl.* with ID 2015-PEDCC-0222.R1.

C2. **Y. Tang**, P. B. Wyllie, J. Yu, X. M. Wang, L. Ran, and O. Alatise, "Offshore low frequency ac transmission with back-to-back modular multilevel converter (MMC)," in *AC and DC power transmission*, *2015 IET*, *Proc. 11th Int. Conf.*, Birmingham, UK, pp. 1-8, (2015).

C3. P. B. Wyllie, **Y. Tang**, L. Ran, T. Yang, and J. Yu, "Low frequency ac transmission – elements of a design for wind farm connection," in *AC and DC power transmission*, *2015 IET*, *Proc. 11th Int. Conf.*, Birmingham, UK, pp. 1-5, (2015).

J2. **Y. Tang**, L. Ran, O. Alatise, and P. Mawby, "A model assisted testing scheme for modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, Jan. 2016.

C4. **Y. Tang**, L. Ran, O. Alatise, and P. Mawby, "Design and control of a compensated submodule testing scheme for modular multilevel converter," accepted by *Applied Power Electronics Conference & Exposition (APEC)*, *2016 IEEE* with ID 1639.

J3. **Y. Tang**, L. Ran, O. Alatise, and P. Mawby, "A compensated model assisted testing scheme for modular multilevel converter," *IEEE Trans. Power Electron.*, accepted on 28th Dec. 2015.

C5. **Y. Tang**, M. Chen, and L. Ran, "Design and control of a compact modular

multilevel converter (MMC) submodule structure with reduced capacitor size using the stacked switched capacitor architecture," accepted by *Applied Power Electronics Conference & Exposition (APEC)*, *2016 IEEE*.

J4. **Y. Tang**, M. Chen, and L. Ran, "A compact MMC submodule structure with reduced capacitor size using the stacked switched capacitor architecture," *IEEE Trans. Power Electron.*, accepted on 13th Dec. 2015.

(C for conference, J for journal)

2 REVIEW OF THE MODULAR MULTILEVEL CONVERTER

The story of the modular multilevel converter (MMC) dates back to the middle of the 1990s when the Robicon Corporation, presently a part of Siemens, put a medium-voltage high-power motor drive with a multilevel PWM inverter into practical use. The per-phase circuit configuration of this multilevel inverter was based on the cascade connection of the ac terminals of modular single-phase full-bridge (FB) inverter cells [29, 30]. The emergence of this topology surprised and impressed motor drive research scientists and engineers due to its scalability and very low output distortions. However, each floating FB-cell has to be powered by a complicated, multi-winding, phase-shifted, line-frequency transformer.

Another advance of the cascaded H-bridge inverter topology was found in the area of reactive power control when Lai and Peng [31, 32] presented a static VAr compensator (STATCOM) also in the middle of 1990s. This was followed by a battery energy storage system for motor drives [33]. The major advantage of this topology is the absence of the complicated multi-winding phase-shifted line-frequency transformer while the disadvantage

is the need for separate dc sources for active power conversion.

In 2001, based on the research advances in cascaded FB-cell inverters, Marquardt and co-authors [34, 35] first presented the concept of the *modular multilevel converter* (MMC) and its basic operating principle. After 10 years of development, the MMC has become the most attractive multilevel converter topology for both medium- and high-power applications [20, 36]. When compared with other VSC topologies, the salient features of the MMC can be summarized as follows:

- Modularity and scalability to meet any voltage level requirement and is independent of fast developing power devices;
- High reliability due to the flexibility of redundancy;
- High efficiency due to reduced switching frequency for each device;
- Superior harmonic performance which significantly reduces or eliminates the need for passive filtering;
- Absence of central dc bus capacitors;
- No direct series connection of the semiconductor devices [37].

2.1 Basic Operation Principle

2.1.1 Basic operation principles of MMC

Figure 2.1(a) shows the basic idea of a multilevel converter [38]. The ac output voltage V_{conv} is achieved by an appropriate number of series-connected pre-charged capacitors. The larger number of capacitors that are used for the same dc bus voltage V_{dc}, the smaller the size of voltage steps and the smaller the related voltage gradients that can be achieved. This also leads to a smaller proportion of harmonics and high frequency noises.

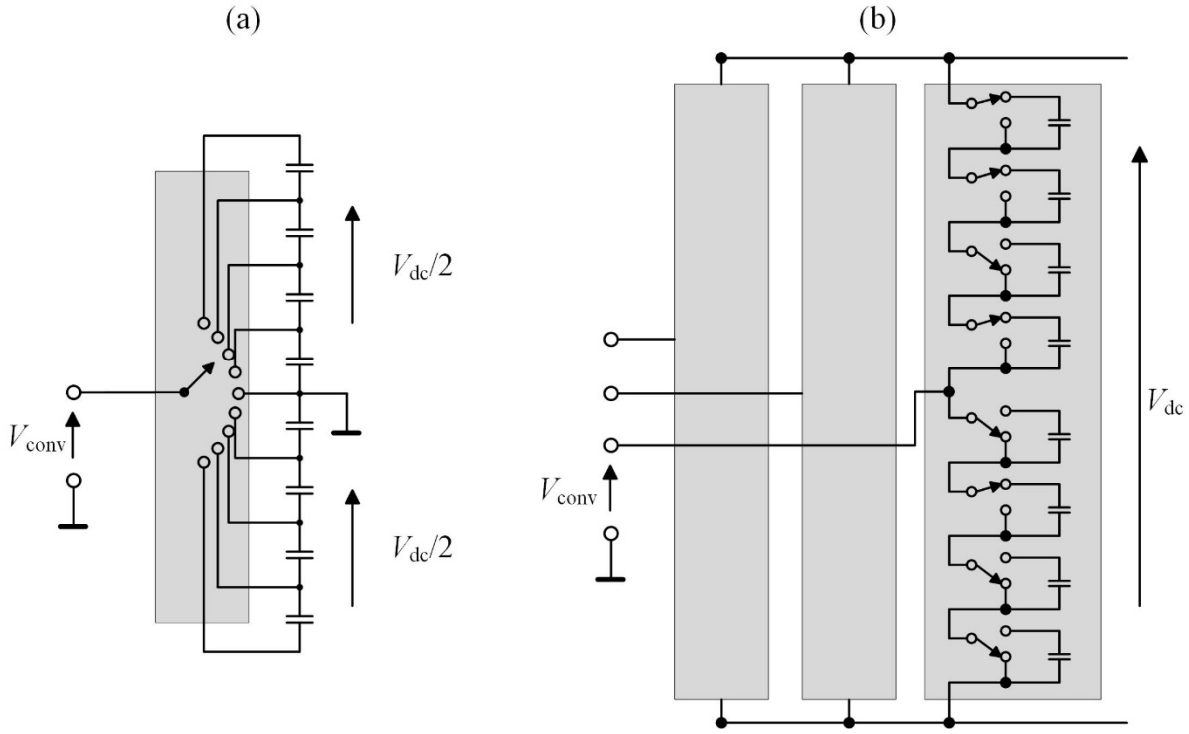

Figure 2.1: (a) Basic representation of a multilevel converter; (b) the MMC's approach

Figure 2.1(b) shows the MMC's approach to multilevel operation. There are three *phase units* corresponding to the three phases in the interconnected ac grid. Each phase unit has two converter *arms*, namely an upper arm and lower arm. Each converter arm consists of tens to a few hundred submodules (SMs) connected in series. Each SM itself is an independent VSC with usually a floating reservoir dc capacitor. SMs in each arm in total are able to withstand the entire converter dc bus voltage V_{dc}. Each SM can output either positive or zero voltage (sometimes negative with certain SM topologies) to the arm circuit in order to synthesize the desired arm voltage u_{arm}. As shown in Figure 2.2, through appropriate SM switching strategies, the arm voltage is usually a sinusoidal waveform with a dc offset equal to half the dc bus voltage. u_{arm_p} is the upper (positive) arm voltage while u_{arm_n} is the lower (negative) arm. The figure shows that the ac output voltage of each phase unit (v_{conv_a} for phase *a*) is achieved collaboratively by the upper and lower arms together. At the same time,

the total output voltage of the two arms is approximately equal to the dc bus voltage V_{dc}. In other words, the three-phase ac voltages and the dc bus voltage in an MMC can be independently controlled. Arm inductors L_{arm} are inserted as shown in Figure 2.2 to limit the current surge caused by the voltage difference when switching the SMs. In certain cases, arm inductors can also help to limit fault currents.

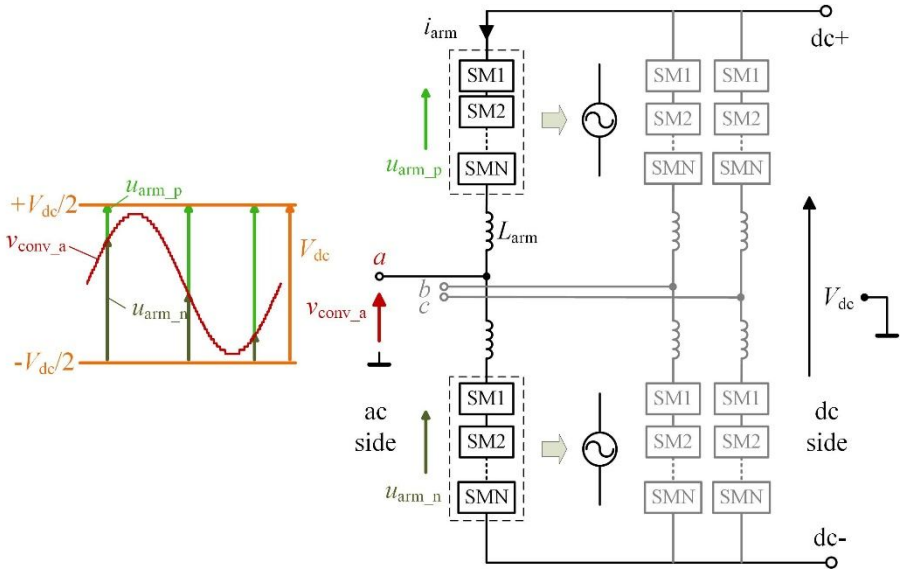

Figure 2.2: Typical output waveforms of an MMC

2.1.2 Basic operation principles of half-bridge SM

As the very basic element in an MMC, basic operation principles of the SM are introduced in this section. The duty of each SM is to output the desired voltage (usually positive or zero) when requested to synthesize the desired arm voltage. Among all the SM topologies, the half-bridge (HB) SM has been the most popular SM adopted for the MMC [39]. This is due to the presence of only two semiconductor switches in each SM, leading to a lower number of devices, simpler circuit configuration, reduced control complexity, and higher system efficiency. Hereafter, the basic operation principles of the HB-SM will be firstly introduced. Other SM topologies will then be briefly discussed and compared at the end.

Figure 2.3 shows the circuit diagram of a HB-SM, where T_1/D_1 represents the upper

IGBT/diode module and T_2/D_2 stands for the lower IGBT/diode module. In normal operations, through switching the upper and lower power switches, the SM capacitor C is either connected to the output port AB or bypassed, and the SM output voltage v_{SM} will be equal to either the capacitor voltage v_C or 0. There are a total of six operating states for each HB-SM as shown in Figure 2.4 and Table 2.1 depending on the switching states of T_1/D_1 and T_2/D_2 ('1' means turn-ON and '0' means OFF) as well as the direction of the SM current i_{SM}.

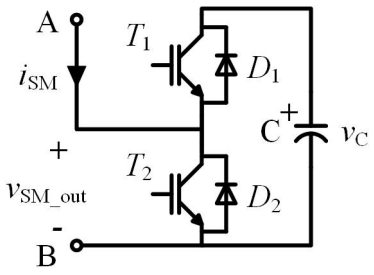

Figure 2.3: Circuit diagram of a HB-SM

A. "SM blocked" – both switches are OFF

In situations such as the system energizing, a fault, or deadbands between the upper and lower switches, both the upper and lower switches will be in an OFF-state. In such a case (State 1 or 2), the SM output voltage can be either v_C or 0 depending on the direction of i_{SM}. For example, when the current flows into the SM (from A to B), due to the blocked T_2, the current can only flow through D_1 and charge the capacitor, and v_{SM_out} will be equal to v_C. When i_{SM} is negative, it will flow through D_2 and v_{SM_out} will be 0 (the ON-state voltage is neglected).

B. "SM bypassed" – T_1/D_1 is OFF, T_2/D_2 is ON

During normal operations, when the SM is required to output '0' voltage (State 3 or 4), T_1/D_1 will be turned OFF and T_2/D_2 will be turned ON. The SM capacitor will be always bypassed regardless of the direction of i_{SM}. Hence, States 3 and 4 are referred to as the *SM*

bypassed mode. More specifically, when i_{SM} flows into the SM, since T_2 is turned ON, i_{SM} will flow through T_2 instead of the blocked D_1 by the forward-charged capacitor. When i_{SM} flows out of the SM, the case will be the same as State 2 in that i_{SM} will flow through D_2 and v_{SM_out} will be 0.

C. "SM switched-in" – T_1/D_1 is ON, T_2/D_2 is OFF

When the SM is required to output the SM capacitor voltage v_C, T_1/D_1 will be turned ON and T_2/D_2 will be turned OFF. In such a case, the capacitor will always be switched into the arm circuit, being either charged or discharged depending on the direction of i_{SM}. Hence, States 5 and 6 are referred to as the *SM switched-in* mode. More specifically, when i_{SM} flows into the SM, since T_2 is OFF, the case is the same as State 1 in that i_{SM} will flow through D_1 and charge the capacitor. When i_{SM} flows out of the SM, the capacitor will be discharged through T_1 and D_2 is blocked by the capacitor.

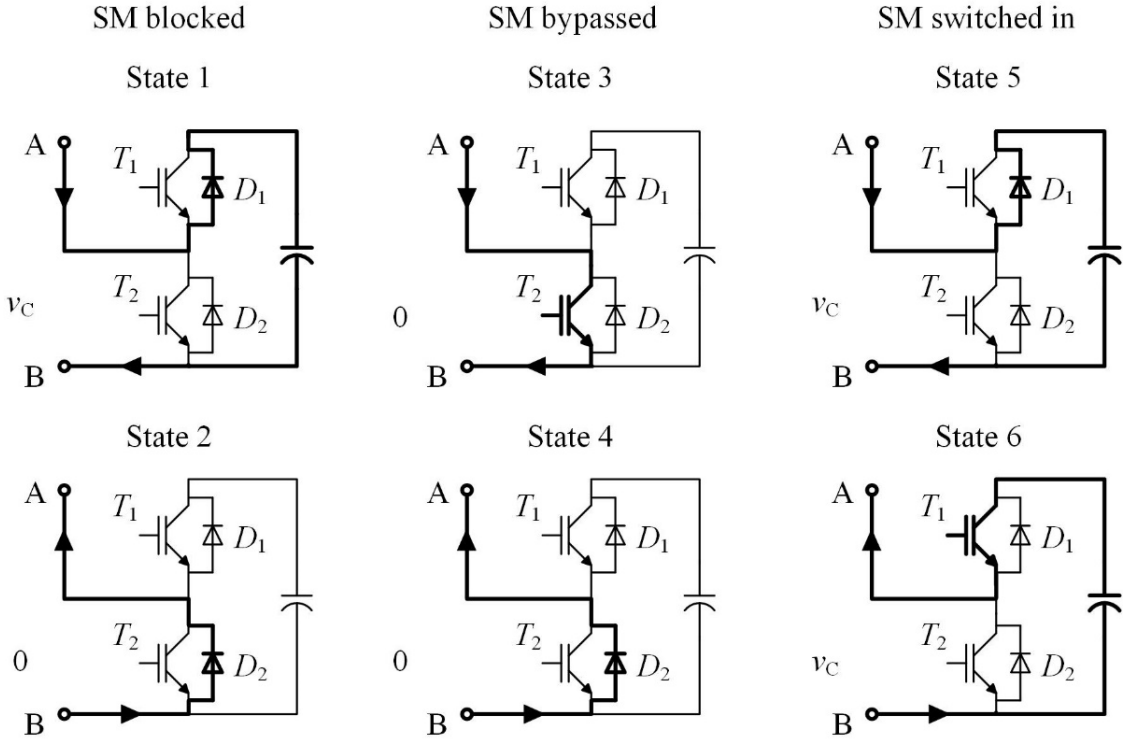

Figure 2.4: Six operating states of a HB-SM

State	SM status	Switching states T_1T_2	i_{SM}	v_{SM_out}	Conducting device	Capacitor state
1	blocked	00	in (A to B)	v_C	D_1	charging
2		00	out (B to A)	0*	D_2	bypassed
3	bypassed	01	in (A to B)	0	T_2	bypassed
4		01	out (B to A)	0	D_2	bypassed
5	switched-in	10	in (A to B)	v_C	D_1	charging
6		10	out (B to A)	v_C	T_1	discharging

(*the ON-state voltage is neglected)

Table 2.1: Six operating states of a HB-SM

2.2 Mathematical Model of MMC

Figure 2.5 gives a single-phase equivalent circuit of the MMC. In addition to the controllable voltage source corresponding to the arm voltage and the arm inductor L_{arm}, a parasitic resistance R_{arm} is added to represent all the converter Ohmic losses [40]. V_{dc} and I_{dc} are the total dc bus voltage and dc current respectively. v_{conv_j} (j=a,b,c) is the converter ac side voltage of phase j at point O whereas i_j is the corresponding ac output current. The arm voltages generated by the SMs are expressed as u_{arm_pj} and u_{arm_nj} for the upper arm and lower arm in phase j, respectively.

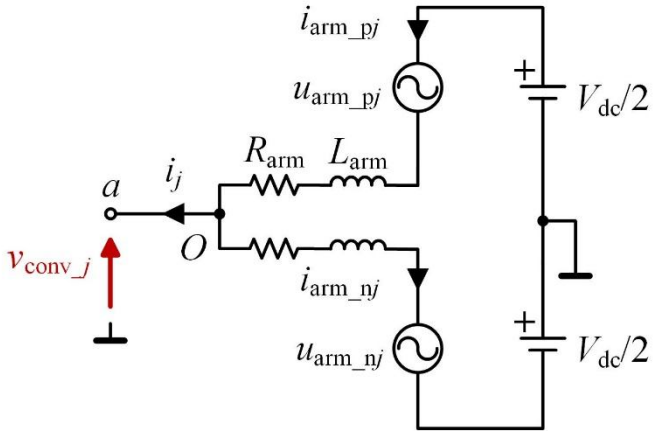

Figure 2.5: Single-phase equivalent circuit of an MMC [19]

As shown in Figure 2.5, the relationship between the arm currents $i_{\text{arm\_p}j}$, $i_{\text{arm\_p}j}$ and the converter ac output current i_j can be written as

$$i_{\text{arm\_p}j} - i_{\text{arm\_n}j} = i_j . \tag{2.1}$$

All the reference directions are as shown in Figure 2.5. Assuming that the sum of the two arm currents is $2i_{\text{diff}j}$, that is

$$i_{\text{arm\_p}j} + i_{\text{arm\_n}j} = 2i_{\text{diff}j} . \tag{2.2}$$

Rearranging (2.1) and (2.2) gives the following

$$i_{\text{arm\_p}j} = i_{\text{diff}j} + \frac{1}{2} i_j \tag{2.3a}$$

$$i_{\text{arm\_n}j} = i_{\text{diff}j} - \frac{1}{2} i_j . \tag{2.3b}$$

(2.3a) and (2.3b) indicate that the ac line current is equally shared between the upper and lower arms. Also, there is a common component that only flows through the converter arms without affecting the ac outputs. This common current is usually referred to as the *inner difference current* or $i_{\text{diff}j}$ (for phase j).

The voltage relationships of both the upper and lower arms in phase j can be written as

$$v_{\text{conv\_}j} = \frac{V_{\text{dc}}}{2} - u_{\text{arm\_p}j} - L_{\text{arm}} \frac{di_{\text{arm\_p}j}}{dt} - R_{\text{arm}} i_{\text{arm\_p}j} \tag{2.4a}$$

$$v_{\text{conv\_}j} = -\frac{V_{\text{dc}}}{2} + u_{\text{arm\_n}j} + L_{\text{arm}} \frac{di_{\text{arm\_n}j}}{dt} + R_{\text{arm}} i_{\text{arm\_n}j} . \tag{2.4b}$$

Through the sum of (2.4a) and (2.4b) and substituting (2.1), the *ac output dynamics* of the MMC can be characterized as

$$v_{\text{conv\_}j} = e_j - \frac{R_{\text{arm}}}{2} i_j - \frac{L_{\text{arm}}}{2} \frac{d}{dt} i_j \tag{2.5}$$

where e_j is the *inner emf* generated in phase j and is expressed as

$$e_j = \frac{u_{\text{arm\_n}j} - u_{\text{arm\_p}j}}{2}. \tag{2.6}$$

The difference of (2.4a) and (2.4b) and substituting (2.2) gives the *inner dynamics* of the MMC as

$$L_{\text{arm}} \frac{d}{dt} i_{\text{diff}\,j} + R_{\text{arm}} i_{\text{diff}\,j} = \frac{V_{\text{dc}}}{2} - \frac{u_{\text{arm\_p}j} + u_{\text{arm\_n}j}}{2}. \tag{2.7}$$

Equation (2.5) and (2.7) confirm that the MMC's ac output dynamics and inner dynamics can be independently controlled. In (2.7), the difference voltage $u_{\text{diff}j}$ is defined as

$$u_{\text{diff}\,j} = L_{\text{arm}} \frac{d}{dt} i_{\text{diff}\,j} + R_{\text{arm}} i_{\text{diff}\,j} = \frac{V_{\text{dc}}}{2} - \frac{u_{\text{arm\_p}j} + u_{\text{arm\_n}j}}{2} \tag{2.8}$$

which is used to control the inner difference current $i_{\text{diff}j}$ without affecting the ac outputs.

2.3 Ac Output Control of MMC

Equation (2.5) for all three phases can be written as

$$\begin{cases} e_a - v_{\text{conv\_}a} = \dfrac{R_{\text{arm}}}{2} i_a + \dfrac{L_{\text{arm}}}{2} \dfrac{d}{dt} i_a \\ e_b - v_{\text{conv\_}b} = \dfrac{R_{\text{arm}}}{2} i_b + \dfrac{L_{\text{arm}}}{2} \dfrac{d}{dt} i_b \\ e_c - v_{\text{conv\_}c} = \dfrac{R_{\text{arm}}}{2} i_c + \dfrac{L_{\text{arm}}}{2} \dfrac{d}{dt} i_c \end{cases}. \tag{2.9}$$

When a balanced steady state condition is assumed, the MMC's ac output dynamics in the *dq* frame can be derived through applying the *Park* transformation [41, 42] to (2.9) as

$$\begin{cases} \dfrac{L_{\text{arm}}}{2} \dfrac{d}{dt} i_{\text{d}}(t) = -\dfrac{R_{\text{arm}}}{2} i_{\text{d}}(t) + \omega \dfrac{L_{\text{arm}}}{2} i_{\text{q}}(t) - v_{\text{conv\_d}}(t) + e_{\text{d}}(t) \\ \dfrac{L_{\text{arm}}}{2} \dfrac{d}{dt} i_{\text{q}}(t) = -\dfrac{R_{\text{arm}}}{2} i_{\text{q}}(t) - \omega \dfrac{L_{\text{arm}}}{2} i_{\text{d}}(t) - v_{\text{conv\_q}}(t) + e_{\text{q}}(t) \end{cases} \tag{2.10}$$

where ω is the ac side fundamental line frequency. Through the *Laplace* transformation, (2.10) can be written in the frequency domain as

$$\begin{cases} \dfrac{\left(R_{\text{arm}}+sL_{\text{arm}}\right)}{2} i_{\text{d}}(s) = e_{\text{d}}(s) - v_{\text{conv\_d}}(s) + \omega \dfrac{L_{\text{arm}}}{2} i_{\text{q}}(s) \\ \dfrac{\left(R_{\text{arm}}+sL_{\text{arm}}\right)}{2} i_{\text{q}}(s) = e_{\text{q}}(s) - v_{\text{conv\_q}}(s) - \omega \dfrac{L_{\text{arm}}}{2} i_{\text{d}}(s) \end{cases} . \tag{2.11}$$

According to (2.11), the *dq* frame based mathematical model of the MMC at the ac side can be represented as shown in Figure 2.6. The desired ac output currents can then be achieved by the appropriate inner emf. One way to derive the required inner emf is by using the PI control as

$$e_{\text{d}}^{*} = v_{\text{conv\_d}} - \omega \frac{L_{\text{arm}}}{2} i_{\text{q}} + \left[K_p \left(I_{\text{d}}^{*} - i_{\text{d}} \right) + K_i \int \left(I_{\text{d}}^{*} - i_{\text{d}} \right) dt \right] \tag{2.12a}$$

$$e_{\text{q}}^{*} = v_{\text{conv\_q}} + \omega \frac{L_{\text{arm}}}{2} i_{\text{d}} + \left[K_p \left(I_{\text{q}}^{*} - i_{\text{q}} \right) + K_i \int \left(I_{\text{q}}^{*} - i_{\text{q}} \right) dt \right] \tag{2.12b}$$

where superscript * stands for the reference value.

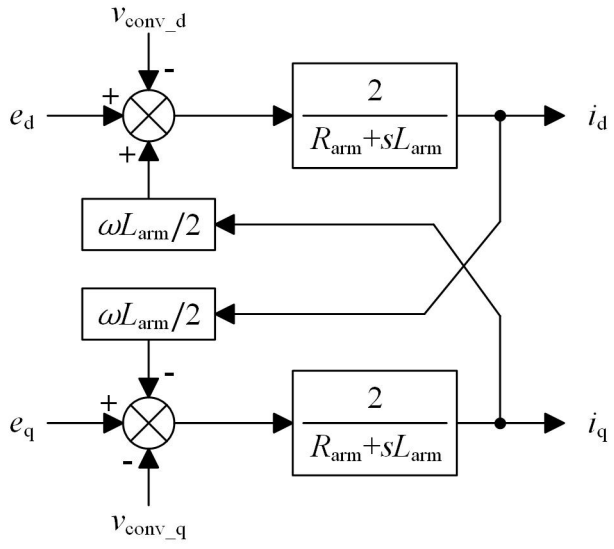

Figure 2.6: *dq* frame based mathematical model of an MMC at the ac side

Once e^{*}_{d} and e^{*}_{q} are acquired, their values are transformed back to the *abc* frame. The required arm voltages to achieve e^{*}_{d} and e^{*}_{q} can be derived with (2.6) and (2.8) as

$$u^*_{\text{arm\_p}\,j} = \frac{V_{\text{dc}}}{2} - e^*_j - u^*_{\text{diff}\,j} \tag{2.13a}$$

$$u^*_{\text{arm\_n}\,j} = \frac{V_{\text{dc}}}{2} + e^*_j - u^*_{\text{diff}\,j} \tag{2.13b}$$

Note that the $u_{\text{diff}j}$ is used to control the MMC's inner dynamics. Its reference value is derived in Chapter 2.6.

If the MMC is to control active (P^*_{ac}) and reactive (Q^*_{ac}) power at the point O in Figure 2.5, I^*_{d} and I^*_{q} in (2.12a) and (2.12b) can be derived by

$$I^*_{\text{d}} = P^*_{\text{ac}} / (1.5 v_{\text{conv\_d}}) \tag{2.14a}$$

$$I^*_{\text{q}} = -Q^*_{\text{ac}} / (1.5 v_{\text{conv\_d}}) . \tag{2.14b}$$

Finally, the MMC's overall ac output control diagram is shown in Figure 2.7.

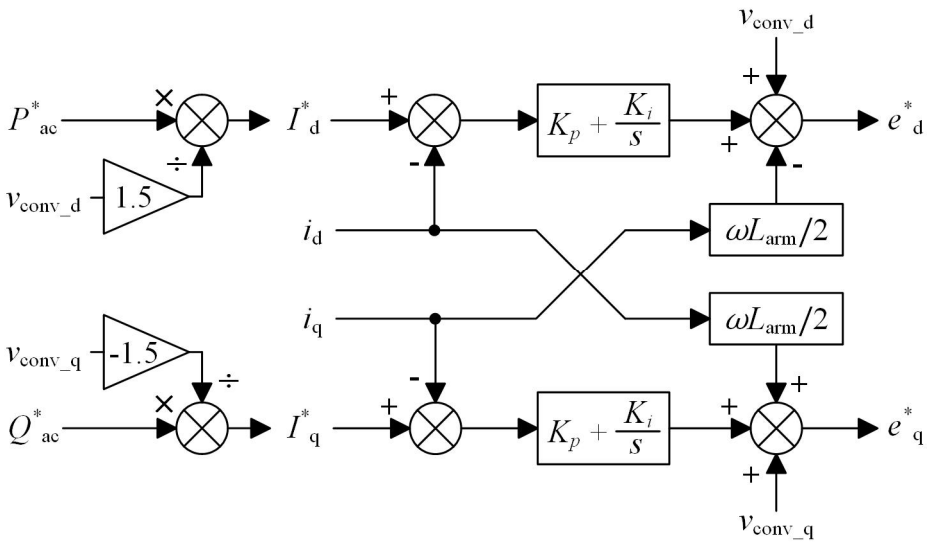

Figure 2.7: MMC's overall ac output control diagram

2.4 Modulation Scheme

The required arm voltages to achieve the desired ac outputs are derived in (2.13a) and (2.13b). The modulation scheme is used to decide on the required number of SMs for each arm to synthesize the required arm voltage. Generally, published modulation schemes can be categorized as follows [39]:

2.4.1 Direct modulation

The simplest modulation scheme is the *direct modulation*, using an open-loop modulator based on a PWM approach [39, 43, 44]. The required arm voltages for each phase unit are used to derive two complementary sinusoidal reference waveforms as given by

$$\begin{cases} n_{\text{arm\_p}j} = N\dfrac{u^{*}_{\text{arm\_p}j}}{V_{\text{dc}}} \\ n_{\text{arm\_n}j} = N\dfrac{u^{*}_{\text{arm\_n}j}}{V_{\text{dc}}} \end{cases} \tag{2.15}$$

where N is the number of SMs in each arm. $n_{\text{arm\_p}j}$ and $n_{\text{arm\_n}j}$ are the reference waveforms, which are compared with the *phase disposition* (PD) carriers as shown in Figure 2.8 to determine the number of SMs to be inserted in the next control cycle. The direct modulation is very simple and robust. However, the resulting circulating currents are high, leading to an increased device rating and power losses [39, 45].

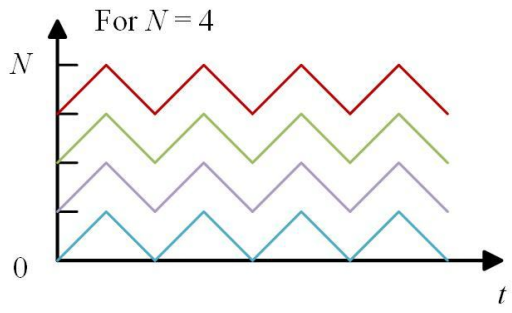

Figure 2.8: Waveforms of phase disposition (PD) carriers

2.4.2 Nearest level control (NLC)

The *nearest level control* (NLC) can be categorized as direct modulation. It is emphasized here due to its effectiveness in the control of an MMC with a very large number of SMs [46, 47]. When compared with the direct modulation, PD carriers are no longer used. In the NLC scheme, the reference waveforms given by (2.15) are directly sampled and the nearest integral value is taken as the number of inserted SMs in the next control cycle. Due to the absence of PD carriers, the NLC is very fast especially with a very large number of SMs. Detailed analysis of the NLC can be found in [46].

2.4.3 Indirect modulation

Indirect modulations can be further categorized into closed loop and open loop schemes. When compared with direct modulations, rather than using the nominal dc bus voltage (V_{dc}) to derive the reference waveform, the indirect approach uses the actual total capacitor voltage in each arm [39], which is either measured (closed loop [48]) or estimated (open loop [49]). The reference waveform is also compared with the PD carriers to decide on the number of SMs to be inserted.

The indirect modulation allows SMs to operate with their time average voltages being different from the natural equilibriums. Using this approach, the low ac output voltages can be achieved whiling maintaining the large number of voltage steps. Also, the controller allows the converter to operate with an imbalance in the energy storagies in different arms, when operating at low output frequencies or with a faulty SM [45]. When compared with the closed loop scheme, the main advantage of open loop indirect modulation is the substantial saving in communication resources since the capacitor voltage data does not have to be transmitted to the main controller. However, the major difficulty is the accurate estimation of parameters that are necessary to describe the system dynamics [45].

2.4.4 Phase-shifted carrier-based PWM technique (PSC-PWM)

The *phase-shifted carrier-based PWM* (PSC-PWM) modulation is proposed and discussed in [36, 50, 51]. In this technique, each SM is controlled separately using its capacitor voltage measurement. A unique reference waveform is generated for each SM and compared with its own triangular carrier to generate gate signals. The main advantage of PSC-PWM is that no SM capacitor voltage balancing control is required since each SM is independently controlled. Nevertheless, a large implementation effort is necessary for the communication between the SMs and the central controller. In addition, very powerful computation capabilities are required when the number of SMs is high [39, 45].

2.4.5 Modified PSC-PWM technique [19]

In the conventional PSC-PWM, since each SM is controlled separately, it will be problematic for capacitor voltage balancing if the characteristics of each SM are not exactly the same [19]. To solve this problem, Tu *et al.* [19] presented a modified PSC-PWM scheme in which the SMs in one arm are all controlled together. Similar to direct modulation, the reference waveforms derived by (2.15) are compared with N triangular carriers, and each carrier is shifted by an angle of $360^{o}/N$ as shown in Figure 2.9, to derive the number of SMs to be inserted (N_{on}). ω_{cr} is the angular frequency of the carrier. A voltage balancing control is then used to decide on the exact SMs to be inserted. This modulation technique is adopted in the rest of this thesis due to its good performance when the MMC has a moderate number of SMs (N=10 to 20).

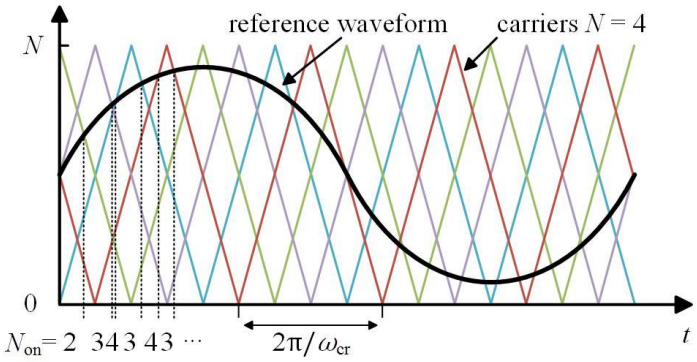

Figure 2.9: Modified PSC-PWM technique

2.5 SM Capacitor Voltage Balancing

In normal operations, with certain modulation schemes such as the modified PSC-PWM, an additional SM capacitor voltage balancing controller is required to balance and maintain the SM capacitor voltage at a certain level. Various methods have been published to achieve this objective [52, 53]. One common voltage balancing technique is based on a *sorting algorithm* [24].

Measurements of all SM capacitor voltages as well as the arm current are needed for the sorting algorithm. In each control cycle, all SM capacitor voltages will be recorded and sorted in ascending order. If the arm current is positive that charges the inserted SM capacitors, the SMs with the lowest capacitor voltages will be switched in and charged. If the arm current is negative, the SMs with the highest capacitor voltages will be switched in and discharged. With this approach, all SM capacitor voltages in one arm will conform to each other.

The main drawback of the sorting algorithm is the resulting high switching frequency for each device [19]. Even if the number of inserted SMs in the two consecutive control cycles is the same, the SMs may still be switched that the number of newly inserted SMs equals the number of newly bypassed SMs. In order to solve this problem, Tu *et al.* [19] proposed a

modified sorting algorithm that aimed to reduce the switching frequency. In this method, the switching of the SMs only occurs when the required number of inserted SMs changes. Figure 2.10 shows the operating principle of the reduced switching-frequency voltage-balancing algorithm:

- If the newly required number of inserted SMs (N_{on}) equals the number derived in the last control cycle (N_{on_old}), and ΔN_{on} is 0, then none of the SMs will have their state changed;
- If extra SMs need to be switched in during the next control cycle, and ΔN_{on} is positive, then no switching is required for those already inserted SMs. The conventional sorting algorithm will only be applied to those currently bypassed SMs;
- If some currently inserted SMs need to be bypassed in the next control cycle, and ΔN_{on} is negative, no additional bypassed SMs will be switched in. Only the currently inserted SMs will be bypassed using the conventional sorting algorithm.

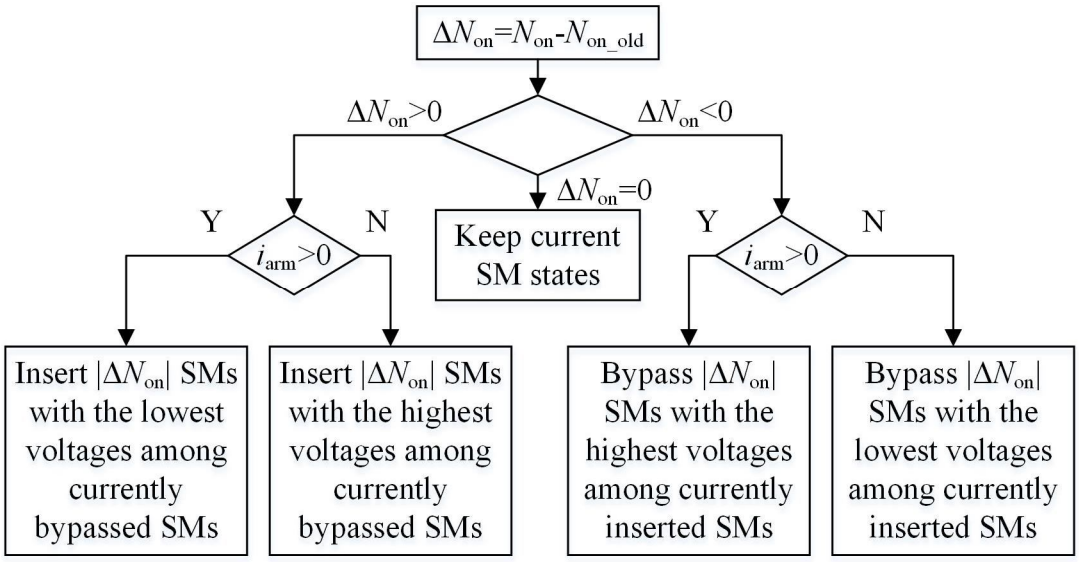

Figure 2.10: Reduced switching-frequency voltage-balancing algorithm [19]

2.6 Circulating Current Control

Circulating currents are part of the inner difference currents as defined in (2.2), and they will circulate within the three phase units without affecting the ac and dc side outputs. It has been shown that the circulating currents in the MMC are generated by the inner difference voltages among the phase units [54, 55]. Since the circulating currents will lead to excessive power losses and increase the SM capacitor voltage ripple [39, 56], these currents can be controlled by the inner difference voltages shown in (2.8).

Various techniques have been proposed to control the circulating currents [19, 40, 48-50, 54]. The indirect modulation technique [48-50] as described in Chapter 2.4 will inherently limit the circulating currents. Harnefors *et al.* [40] used a proportional (P) controller to suppress the circulating currents. However, both the above methods can only reduce the circulating currents rather than eliminate them.

Tu *et al.* [19, 56] proposed a method to eliminate the circulating currents based on the *dq* frame with a pair of PI controllers. Since the circulating currents in steady state are found to be majorly at 2nd order with negative sequence (amplitude of the 4th order is only 2% of the 2nd order and higher orders are even smaller [55]), the inner difference currents for all phase units can be expressed by

$$\begin{cases} i_{\text{diff}\,a} = \dfrac{I_{\text{dc}}}{3} + I_{2f}\sin\left(2\omega t + \varphi_0\right) \\ i_{\text{diff}\,b} = \dfrac{I_{\text{dc}}}{3} + I_{2f}\sin\left(2\omega t + \varphi_0 + \dfrac{2\pi}{3}\right) \\ i_{\text{diff}\,c} = \dfrac{I_{\text{dc}}}{3} + I_{2f}\sin\left(2\omega t + \varphi_0 - \dfrac{2\pi}{3}\right) \end{cases} \tag{2.16}$$

where I_{dc} is the converter dc current and is evenly distributed among the three phase units, I_{2f} the peak current of the 2nd order circulating currents, and φ_0 is the initial phase angle.

As shown in (2.16), it is possible to transform the three circulating currents into two dc

components in a double line-frequency, negative-sequence *dq* frame using the *Park* transformation. Rewriting (2.8) for all three phases yields

$$\begin{bmatrix} u_{\text{diffa}} \\ u_{\text{diffb}} \\ u_{\text{diffc}} \end{bmatrix} = L_{\text{arm}} \frac{d}{dt} \begin{bmatrix} i_{\text{diffa}} \\ i_{\text{diffb}} \\ i_{\text{diffc}} \end{bmatrix} + R_{\text{arm}} \begin{bmatrix} i_{\text{diffa}} \\ i_{\text{diffb}} \\ i_{\text{diffc}} \end{bmatrix}. \tag{2.17}$$

Substituting (2.16) into (2.17) and applying the *Park* transformation at the double line-frequency, negative-sequence yields

$$\begin{bmatrix} u_{\text{diffd}} \\ u_{\text{diffq}} \end{bmatrix} = L_{\text{arm}} \frac{d}{dt} \begin{bmatrix} i_{2f\text{d}} \\ i_{2f\text{q}} \end{bmatrix} + \begin{bmatrix} 0 & 2\omega L_{\text{arm}} \\ -2\omega L_{\text{arm}} & 0 \end{bmatrix} \begin{bmatrix} i_{2f\text{d}} \\ i_{2f\text{q}} \end{bmatrix} + R_{\text{arm}} \begin{bmatrix} i_{2f\text{d}} \\ i_{2f\text{q}} \end{bmatrix}. \tag{2.18}$$

where u_{diffd} and u_{diffq} are the *dq* components of the inner difference voltages. $i_{2f\text{d}}$ and $i_{2f\text{q}}$ are the *dq* components of the circulating currents. The system transfer function of the circulating currents can then be derived by applying the *Laplace* transformation to (2.18) and is shown in Figure 2.11.

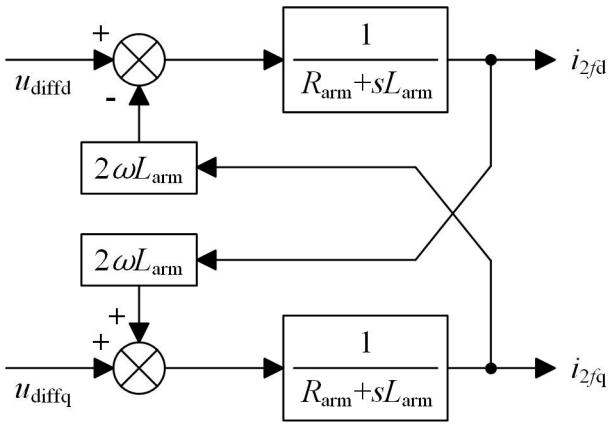

Figure 2.11: System transfer function of the MMC's inner dynamics

The structure of the circulating current suppressing controller is shown in Figure 2.12. In order to eliminate the circulating currents, two PI controllers are used for the *d* axis and *q* axis respectively with both references $I^*_{2f\text{d}}$ and $I^*_{2f\text{q}}$ set to zero [19]. The derived inner difference voltage references u^*_{diffd} and u^*_{diffq} are then transformed back to the *abc* frame

using the inverse *Park* transformation and added to (2.13a) and (2.13b) to obtain the desired voltages for the upper and lower arms. Finally, Figure 2.13 shows the overall control structure of the MMC.

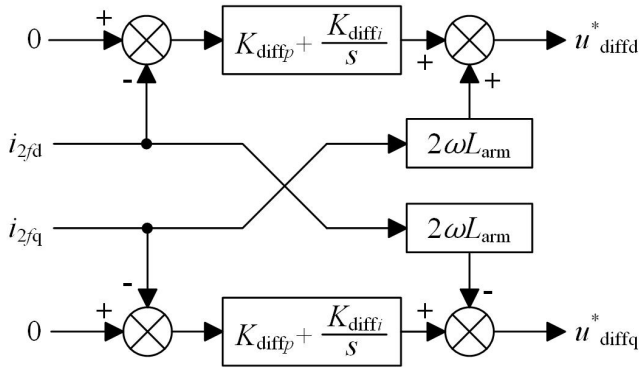

Figure 2.12: Diagram of the circulating current suppressing controller (K_{diffp} and K_{diffi} are the gains for the proportional and integral control respectively)

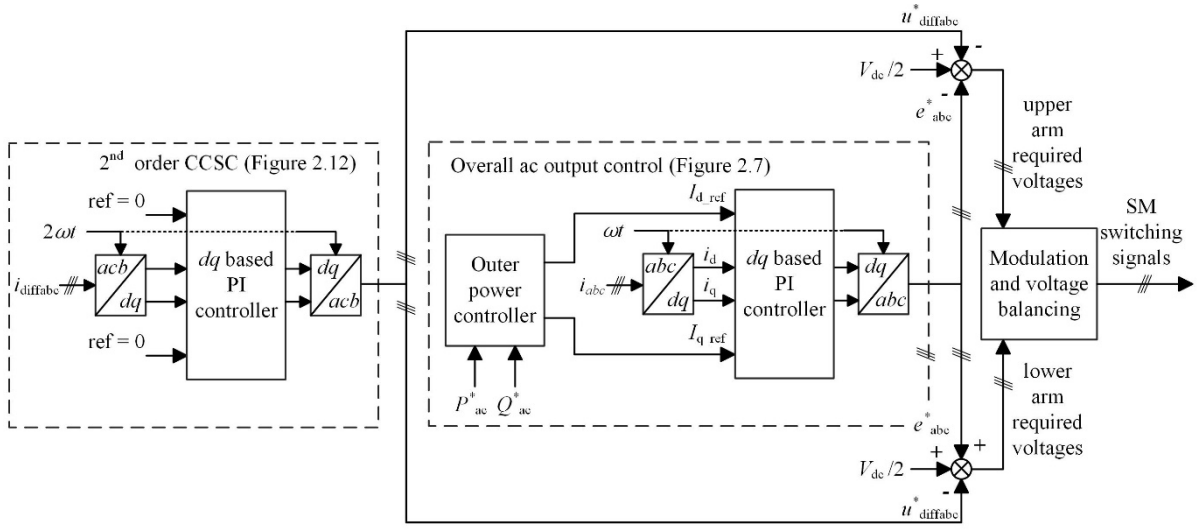

Figure 2.13: Overall control structure of the MMC

2.7 System Pre-charge and Starting

Before normal operations, all SM capacitors are required to be charged to their nominal voltage to avoid a large inrush of current at the instant of the start, which may threaten the system's safe operations [57].

For a single SM, its voltage to ground is usually not the maximum SM capacitor voltage but may vary from zero to hundreds of kilovolts depending on its switching status. Due to the extreme insulation requirements, it is very difficult to use a ground-referenced power source to supply the control boards and gate drivers (GDs) in a SM. Instead, the power to supply the auxiliary circuits is usually drawn from the local SM capacitor [58, 59] as shown in Figure 2.15.

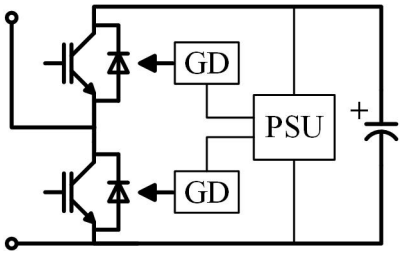

Figure 2.14: Gate driver units (GDs) and power supply unit (PSU) in each SM

The major problem of this configuration (Figure 2.14) is that the local power supply unit (PSU) will not operate until the capacitor voltage increases up to 20% to 30% of its nominal voltage [58, 59]. In other words, at the beginning of the start-up process, the entire MMC is in a 'dead' status such that no control or switching of power switches will work. SM capacitors are usually charged all together as a diode bridge until their voltages rise up to the minimum level required by the local PSUs. After that, all SMs can then be controlled and smoothly charged to the nominal value. Hence, the pre-charge process of the MMC can be divided into uncontrolled and controlled stages, which are described as follows.

2.7.1 Uncontrolled pre-charge process

As shown in Figures 2.15 and 2.16, the converter can be pre-charged from either the dc or the ac side. In both cases, a resistor-contactor arrangement is added to either the dc terminals [57] or the ac output points [57, 60, 61] to limit the inrush current. When the MMC is energized by the pre-charged dc bus (Figure 2.15), since all the power switches are blocked,

all the SM capacitors will be charged simultaneously through the free-wheeling diode D_1 (see to Figure 2.3). As there are a total of $2N$ SMs in each phase unit, the maximum attainable capacitor voltage during this process is $V_{dc}/2N$ when the redundant SMs are excluded [57].

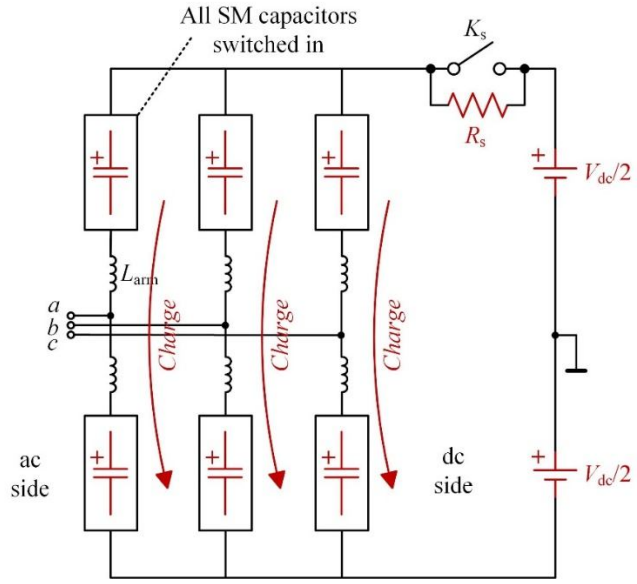

Figure 2.15: Uncontrolled pre-charge from the dc side [57]

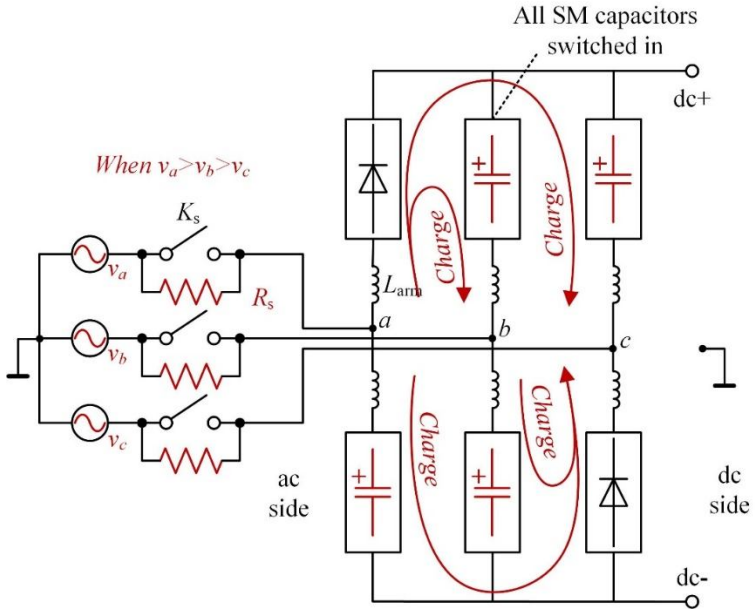

Figure 2.16: Uncontrolled pre-charge from the ac side [57]

When the MMC is energized from the ac side, the pre-charge process is as shown in Figure 2.16. Again, all the power switches are blocked due to insufficient SM capacitor voltages. At every instant, in either one of the three upper arms, the arm with the highest ac phase voltage will be bypassed by the free-wheeling diode D_2 in all SMs (see Figure 2.3) whereas the other two upper arms will be charged through D_1. For the three lower arms, the arm with the lowest ac phase voltage will be bypassed while the other two lower arms will get charged. At the end of the uncontrolled pre-charge process, the maximum voltage of each SM capacitor will be equal to the amplitude of the ac line-to-line voltage divided by N, which is around 80% of the nominal voltage of the SM capacitor.

2.7.2 Controlled pre-charge process

At the end of the uncontrolled pre-charge process, SM capacitor voltages are still lower than the desired level. At this point, all the local PSUs are in normal operation and the controlled pre-charge will begin. In the controlled pre-charge process, the limiting resistors are all bypassed and the charging current are controlled by the method proposed in [57]. After all the SM capacitors are charged to the desired level, the pre-charge process will stop and the MMC can start normal operations.

2.8 Operation under Unbalanced Grid Conditions

The majority of the technical literature on the modelling and control of an MMC primarily assumes balanced grid conditions [24, 37, 62]. The control of an MMC under unbalanced grid conditions has been reported in [63-66]. Under unbalanced grid conditions, the primary control objectives are: 1) to keep the ac side currents balanced by suppressing the negative-sequence components; 2) to maintain the dc bus voltage constant; 3) to control the circulating currents and 4) to balance the SM capacitor voltages [39].

Saeedifard and Iravani [63] proposed the use of the control strategy, which was mainly applied in the conventional two-level VSCs [67, 68], in the MMC under unbalanced grid conditions. In such a case, MMC's ac side dynamics can be visualized as the positive- and the negative-sequence subsystems. Each subsystem is independently controlled based on the *dq* reference frame.

The control of the circulating currents is unique in the MMC even under unbalanced grid conditions. In such a case, the circulating current suppression controller proposed in [19] will not be able to eliminate the circulating currents due to the additional positive- and zero-sequence components. The proportional controller proposed in [40] is still effective with good stability however the circulating currents still cannot be entirely eliminated. In order to solve this problem, Moon *et. al.* [66] proposed a control method based on the proportional-integral-resonant (PIR) controller. Three PIR controllers are used to control the positive- and negative-sequence circulating currents in the three phase units and another PIR to reduce the zero-sequence circulating current and the dc current ripple.

2.9 Other SM Topologies

The main reason for SM topology innovation is the lack of dc side short-circuit fault handling capability in the commonly adopted HB-SM. In an MMC with HB-SMs during a dc fault, fault currents from the ac side will flow through the free-wheeling diode D_2 (see Figure 2.3) in all SMs and cannot be controlled. Due to the lack of a mature and economically viable dc circuit breaker (CB), the fault currents can only be turned OFF by ac side CBs and the entire HVDC transmission system has to be shut down, which is currently one of the major obstacles for the development of the multiterminal HVDC grid [69, 70]. State-of-the-art SM topologies with dc fault handling capability are reviewed below.

2.9.1 Full-bridge SM

The idea of the full-bridge (FB) SM topology came from the cascaded H-bridge (CHB) converters which were commonly adopted for ac motor drives [30] or reactive power compensation like STATCOM. The circuit diagram of a FB-SM is shown in Figure 2.17(a). In its normal operations, the FB-SM operates similar to a HB-SM such that the SM output voltage is either the capacitor voltage v_C or zero. In the case of a dc fault, the FB-SM can output $-v_C$ to withstand the ac grid voltage and block the fault current. However, a FB-SM requires twice the number of semiconductors in the conduction path, leading to much higher power losses and higher converter costs than a HB-SM based system [62].

To solve this problem, Merlin *et at.* [71-73] proposed a hybrid topology between the two-level VSC and the MMC by combining stacks of FB-SMs with director switches, referred to as the *Alternative Arm Converter* (AAC). Since only one arm is active in each phase unit for every half fundamental cycle, the AAC requires less number of SMs per arm than the MMC with HB-SMs. The total number of semiconductor devices is around 60% more than that in a HB based MMC [71]. The total power loss of an AAC is only slightly higher than that of the HB based MMC during active power conversions, and while the converter generates or absorbs reactive power, the total loss of an AAC can be 40% to 50% higher than that of an MMC [73].

2.9.2 Clamp-diode SM

Marquardt also proposed the clamp-double (CD) SM as shown Figure 2.17(b) to achieve the dc fault handling capability [62, 74]. In its normal operations, the switch S_5 is always ON and each CD-SM is equivalent to two series-connected HB-SMs. The number of devices in the conduction path of a CD-SM is 75% of that in a FB-SM, leading to lower power losses than the latter. During a dc fault, the S_5 will be blocked and the two capacitors C_1 and C_2 will

be connected in parallel, hence the CD-SM based MMC can only utilize half of the possible SM capacitor voltages to block the fault current.

2.9.3 Cross-connected SM

Based the CD-SM topology, Nami *et al.* [75] connected the two HB-SMs in a crossed fashion as shown in Figure 2.17(c), which is the cross connected (CC) SM. The advantage of this structure is a symmetrical 5-level output voltage ($2v_C$, v_C, 0, $-v_C$ and $-2v_C$) such that all the SM capacitor voltages can be used to block the fault current. However, the two clamp switches (S_5 and S_6) must tolerate twice the capacitor voltage, leading to the need for series connected power switches and also higher power losses.

2.9.4 Three-level SM

Combining the concepts of the CD-SM and CC-SM, Li *et al.* [76] proposed the three-level (TL) SM as shown in Figure 2.17(d). In its normal operations, the switches S_5 and S_6 are always ON and each TL-SM is equivalent to two HB-SMs connected in series. During a dc fault, all the switches will be OFF and the two capacitors C_1 and C_2 are connected in series to block the fault. The advantages of the TL-SM are:

- the required voltage blocking capabilities of all the switches (including diodes) are only the peak capacitor voltage (v_{C1} or v_{C2});
- both C_1 and C_2 can be used to block the fault.

When part of the HB-SMs (slightly less than half) in an MMC are replaced by the TL-SMs, the additional conduction loss of such a hybrid system will be 44% more than that of a HB-SM (only) based MMC.

2.9.5 Future trends

Apart from the demand for the dc-side short-circuit fault-handling capability, SM topology innovation is also driven by other motivations. One trend is towards a more compact and lightweight SM for space limited applications such as urban substations and offshore platforms. A novel SM structure based on a recently proposed stacked switched capacitor (SSC) architecture is proposed in Chapter 8. It is shown that the total volume of capacitors in each SM can be reduced by more than 40% without significantly increasing the power loss. This new structure is demonstrated based on the original HB-SM. However, it could also be applied to the above SM structures with dc-side short-circuit fault-handling capability.

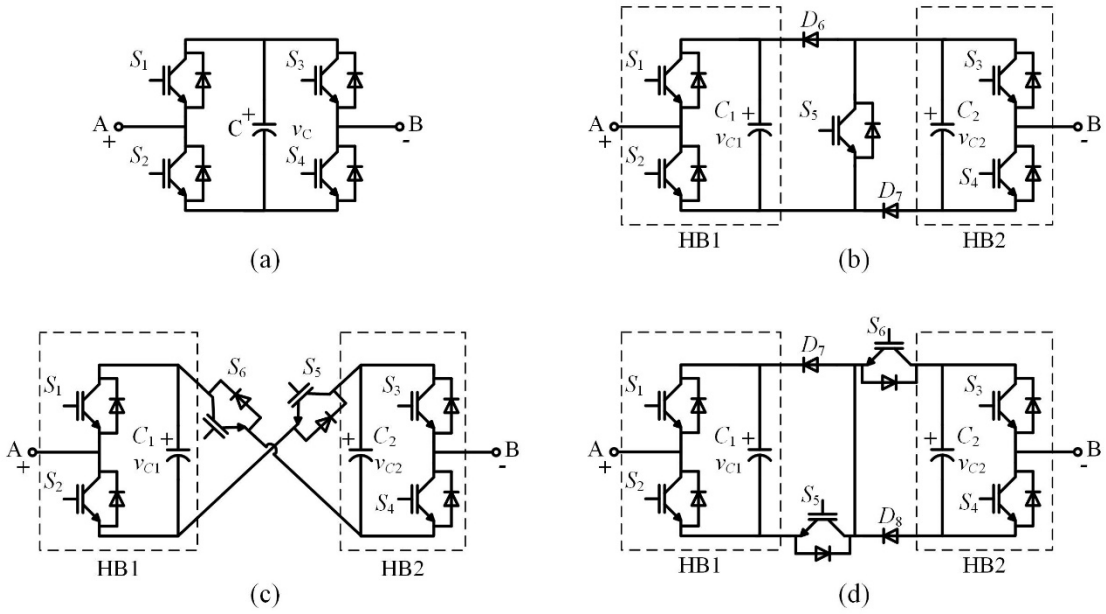

Figure 2.17: Various SM topologies: (a) full-bridge; (b) clamp-double; (c) cross-connected; and (d) three-level SM

3 CAPACITOR STUDY

In MMCs, when compared with the conventional two-level VSC, the bulk dc-link capacitor that is usually used for filtering and energy storage has been replaced by small reservoir capacitors distributed in SMs. Each SM capacitor acts as an independent voltage source that tends to offer a nearly constant dc voltage while absorbing the imbalanced power between the ac side and dc side of the converter. Since the imbalanced power is usually large and mainly at low frequencies, the capacitance has to be large to suppress the large voltage ripple, leading to a large and heavy SM capacitor, which usually accounts for over 50% of the size and 80% of the weight of an SM as shown in Figure 3.1. Hence, in an MMC, SM capacitors account for a significant part of the system in terms of size, weight, and cost.

The imbalanced power will also cause stresses on the capacitor, including high voltage stress, large voltage, and current ripples, as well as high temperature that may lead to accelerated ageing and eventually breakdown of the capacitor. Since the stability of the SM largely depends on the stability of SM capacitors, selecting the right SM capacitor is indeed a major issue that needs further investigation.

This chapter reviews and compares three types of capacitor that are commonly adopted

in power electronics applications, i.e. electrolytic capacitors, ceramic capacitors, and film capacitors. The aim is to provide a comprehensive understanding of their characteristics and provide guidance necessary for the development of the SM capacitor selection procedure presented in the next chapter.

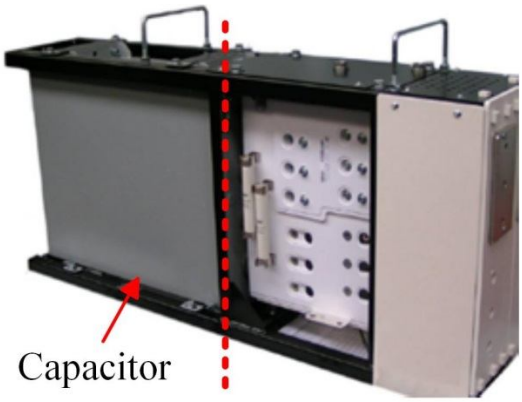

Figure 3.1: A SM from Alstom

3.1 Capacitor Basics

Three types of capacitors are commonly adopted in applications of power electronics, which are aluminium electrolytic capacitors, high capacitance multilayer ceramic capacitors (MLCC), and film capacitors [77]. All capacitors can be represented by the simplified model shown in Figure 3.2 [78, 79].

Figure 3.2: Simplified model of a capacitor

The equivalent series resistance (ESR) represents all the resistance in the capacitor, including the electrodes, connectors, leads, as well as Ohmic losses in the dielectrics. In an MMC SM, the current passing through the SM capacitor will be equal to the entire arm current while being switched in. When such a large current flows through the ESR, this may

lead to excessive heat dissipation and a temperature rise that may affect the capacitor's safe operation. Hence, the ESR of the chosen capacitor must be as small as possible.

The equivalent series inductance (ESL) depends on the number of supply lines to the electrodes and the winding construction. It is usually small in the operating frequency range of MMC SMs (50 Hz to 500 Hz) and thus can be ignored during the SM capacitor selection process.

3.2 Electrolytic Capacitor

Electrolytic capacitors are the most popular type for the use in dc bus applications due to their large capacitance values [78-81]. The electrolytic capacitor has a high dielectric constant typically 8 to 8.5 versus the film capacitor which is typically around 2.2 for poly-propylene, leading to more capacitance per given volume and much higher energy density [82]. However, due to the thickness limitations of the dielectric (aluminium oxide), its maximum nominal voltage is only around 600 V [82]. For applications with higher voltages, the connection of capacitors in series is required with extra voltage balancing circuits. Moreover, when operated at a high voltage (500 V), the resistivity of the electrolyte will be 5 kΩ·cm versus 0.15 kΩ·cm for lower operating voltages, which limits the rms ripple current capability at 20 mA per μF [82]. Last but not least, electrolytic capacitors are usually polarized and it is necessary to ensure that they are placed in the correct direction [83]. Failure to do so will result in potential explosions of the capacitor.

3.3 Ceramic Capacitor

Ceramic capacitors are the most widely used passive components in modern electronics, among which the multilayer ceramic capacitor (MLCC) dominates [84]. The major applications of ceramic capacitors include resonant circuits, filters, power supply bypass, and

decoupling. The properties of ceramic capacitors vary significantly depending on the type of dielectric used. Some types offer high (capacitance) precision and stability but have low energy densities, and others have high peak energy densities but wide capacitance tolerances [83, 84].

Ceramic capacitors have been extensively used in low-power applications. They can operate with high ambient temperature. However, they have a number of major shortcomings. First, ceramic capacitors are usually very small (capacitance) due to the difficulty in firing large ceramics [84]. Secondly, parameters such as the capacitance value, dissipation factor, and ESR are usually not stable but strongly depend on the applied voltage and operating temperature. The variations can be up to a magnitude. Although the recent release of CeraLink from EPCOS-TDK [85] indicates the interest of industries in extending the scope of MLCC towards higher power dc bus applications with larger capacitance, its ESR at low frequency (< 1 kHz) can be up to a few hundred mΩ, making it an inappropriate option for MMC SMs which usually switch at low frequencies.

3.4 Film Capacitor

Film capacitors can be further categorized into foil film, metalized film and a hybrid structure [86]. A foil film capacitor has high current carrying and *dv*/*dt* capability due to its thick foil. A metalized film capacitor with its self-healing property can provide higher stability in use. Loss of capacitance and eventual open circuit have been found to be the common failure modes of metalized film capacitors and may be regarded as preferable to the short circuit failure mode of the foil film capacitor [77, 87].

3.4.1 Properties of the MPPF capacitor

Various types of polymers can be the dielectric such as *polyethylene terephthalate* (PET),

also known as *polyester*, and *polycarbonate* as well as *polypropylene* (PP). Featuring a low dissipation factor, low cost, high ripple current capability and high stability in wide temperature and frequency ranges [88], metalized polypropylene film (MPPF) capacitors can be a suitable choice for MMC SMs.

As shown in Figure 3.3, an MPPF capacitor consists of two polypropylene films coated with a few nanometre thickness of aluminium, zinc or other metal particles acting as the anode and cathode plates. They are offset and usually wound tightly in a cylindrical roll in order to prevent air voids. The fine particles of the selected metal are sprayed onto both ends of the roll making contact with alternating layers to form the corresponding electrodes.

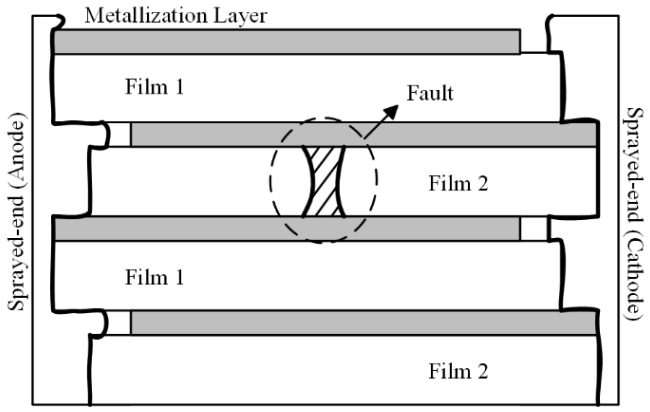

Figure 3.3: Structure of a metalized polypropylene film (MPPF) capacitor

3.4.2 Self-healing of the MPPF capacitor

Defects such as embedded foreign particles or micro-flaws in the polypropylene film can result in weak spots that will lead to the localized breakdown of the dielectric due to the electric field concentration as shown in Figure 3.3. The breakdown event results in a short period of discharge and the thin metallization layer near the defect site can be rapidly vaporized and blown away due to the high temperature. The site then becomes electrically isolated and the fault is prevented from triggering a catastrophic failure. The process is usually referred to as '*self-healing*' or '*clearing*'.

3.4.3 Ageing mechanisms of the MPPF capacitor

Although MPPF capacitors are very reliable due to their self-healing capability, they are not free of failures. A good understanding of their ageing mechanisms is useful in order to select the right capacitor to ensure the reliability of the converter system.

Self-healing, electrochemical corrosion and disconnection from the 'sprayed ends' are found to be the three major ageing mechanisms in MPPF capacitors [89-92]. The first two lead to capacitance loss and an increase in the dissipation factor, tanδ. The self-healing energy has been found to be affected by the electrode thickness, layer pressure, applied voltage, and temperature. Generally, the greater is the clearing energy, the greater the clearing damage. Shaw *et al.* [89] found that the self-healing energy increases exponentially at a power of 4.7 with the applied voltage. Self-healing also occurs in the process of corona discharge. Nye *et al.* [93] and Tomago *et al.* [94] found that when a sufficiently high ac voltage is applied, the occluded air in the film winding may ionize and the resultant hot spots will eventually puncture the dielectric. High ac voltage has been found to be responsible for electrochemical corrosion as well. When the applied ac voltage is above a certain level, the localized conversion of aluminium layer into aluminium oxide can be observed [95]. Thus, both the maximum voltage and the voltage ripple must not exceed the limits to avoid cumulative damage during operation.

The ripple current must also be given adequate attention since the above two ageing processes accelerate with rising temperature [89, 95]. High current stress may also cause the weakening of the connection of the metallization layer from the 'sprayed ends' leading to higher contact resistance [90]. As all the arm current in an MMC will pass through an inserted capacitor, a proper design arrangement must be used for high power applications.

3.4.4 Energy density and ripple current capability of the MPPF capacitor

Figure 3.4 shows the energy density (J/litre) (calculated by ½CV^2/Volume, where C is the rated capacitance and V is the rated dc voltage) versus the rated dc voltage (at 70°C) of 240 commercial metalized film capacitors from eight manufacturers (AVX, Cornell, Electronicon, Illinois Capacitor, IXYS, Panasonic, TDK EPCOS and Vishay as listed in Table 3.1). Their rated voltages are from 75 V to 3600 V, and their capacitance values are from 1.8 μF to 5540 μF. When the rated voltage is less than 400 V, the polyester film is usually used as the dielectric. It has a lower cost but lower energy density (less than 60 J/litre). When the rated voltage is higher than 450 V, the MPPF is used and the energy density increases with the rated voltage until 1000 V where the peak energy density is reached (approx. 350 J/litre). Bond's presentation in 2013 [96] gave similar findings and showed that the maximum energy density of the present state-of-the-art MPPF capacitors for dc-link applications is around 360 J/litre.

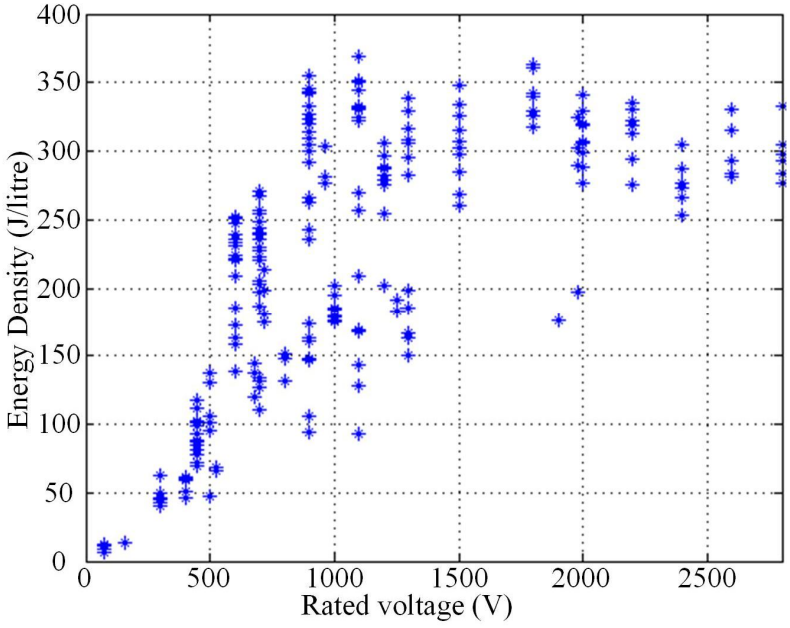

Figure 3.4: Energy density study (I) of commercial metalized film capacitor products

Figure 3.5 further plots the energy density against the rated voltage and capacitance. It

shows that the energy density tends to decrease with lower capacitance. This can be explained by the higher proportion of non-film components such as the capacitor case and electrodes in a small (capacitance) capacitor compared to those in a large one.

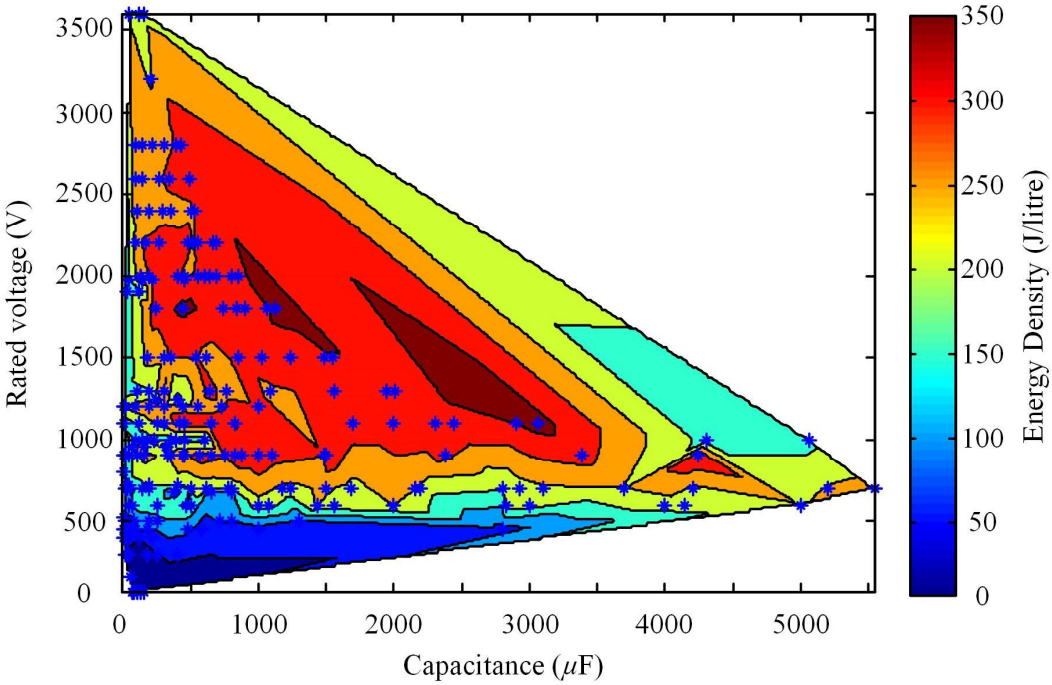

Figure 3.5: Energy density study (II) of commercial metalized film capacitor products

The ripple current (rms) capability of the sampled capacitors was also analyzed, which is defined as the ratio between the permitted ripple current in rms and the rated capacitance. The units are usually A/mF (medium- to high-power system) or mA/μF (low-power system). The study raises a number of key points that are described as follows:

- For the majority of MPPF capacitors, the ripple current capability ranges from 100 A/mF to 400 A/mF;
- For certain MPPF capacitors, the ripple current capability can be as low as 10 A/mF such as the PK16 XC series from Electronicon. These capacitors may be specially designed for higher energy density. It shows that the MPPF capacitor's ripple current capability is not guaranteed to be sufficient for MMC applications at all events. A check of the SM capacitor's ripple current stress is necessary during the design.

- For a certain type of capacitor with the same rated voltage, some manufacturers offer two options with slightly different capacitance. Usually, the option with lower capacitance (5% to 10% less) will have much higher ripple current capability (twice). The selection of capacitors will be the trade-off between the above two properties.
- For a certain type of capacitor with the same rated voltage, the ripple current capability tends to decrease with increasing capacitance. This can be explained as that more film layers have to be rolled or stacked together to increase the capacitance, making it much harder for the heat in the centre to dissipate. In extreme cases, the temperature in the centre can be more than 10 ºC higher than the case [97], leading to faster ageing even when the case temperature is not high. Hence, a proper heat dissipation arrangement is required for SM capacitors with very large capacitance.

3.5 Summary

The characteristics of three types of capacitors are analysed and compared in this chapter. Electrolytic capacitors have high energy density. Their major disadvantages are their relatively short lifetime, high ESR and very low ripple current capability. Ceramic capacitors can operate at much higher temperature and have good reliability. However, it is still difficult to manufacture products with large capacitance. In addition, properties (capacitance and ESR) of certain ceramics are not stable, and will significantly change with the applied voltage and ambient temperature. The MPPF capacitor is currently the most suitable choice for MMC SMs due to their low cost, low ESR (even at low frequencies), high ripple current capability and high stability in wide temperature and frequency ranges. The ageing mechanisms of MPPF capacitors were also reviewed. This study indicates the necessity to consider the maximum voltage, voltage ripple, as well as the ripple current stress when selecting SM capacitors.

Manufacturer	Datasheet link
Metalized Polyester Film	
AVX	http://www.eccmec.it/wp-content/uploads/2012/05/ Catalogo-AVX-Medium-Power-Film-Capacitors1.pdf
Metalized Polypropylene Film (MPPF)	
AVX	http://www.eccmec.it/wp-content/uploads/2012/05/ Catalogo-AVX-Medium-Power-Film-Capacitors1.pdf
Electronicon	http://www.electronicon.com/fileadmin/inhalte/pdfs/downloadbereich/Katalog/neue_Kataloge_2011/200.003-020070.pdf http://www.electronicon.com/fileadmin/inhalte/pdfs/downloadbereich/Katalog/neue_Kataloge_2011/200.003-020030.pdf
TDK	http://en.tdk.eu/inf/20/50/ds/B2562_.pdf http://en.tdk.eu/inf/20/20/db/fc_2009/MKP_B32774_778.pdf
Illinois	http://www.illinoiscapacitor.com/pdf/seriesDocuments/ MDCL%20series.pdf
Panasonic	https://industrial.panasonic.com/lecs/www-data/pdf/ ABD0000/ABD0000CE62.pdf
CDE	http://www.cde.com/resources/catalogs/BLC.pdf http://www.cde.com/resources/catalogs/947D.pdf
IXYS UK	http://www.westcode.com/publicity/prod_lit/flyer09.pdf
VISHAY	http://www.vishay.com/docs/26015/mkp1848cdclink.pdf

Table 3.1: Datasheets of the sampled capacitors

4 CAPACITOR SELECTION FOR MMC

As shown in Figure 4.1, a typical dc to three-phase ac MMC consists of six arms, each with a string of SMs. In order to synthesize the required ac side voltage, the SMs in the arm are switched in or bypassed to generate the desired arm voltage. Every SM, which is usually of a HB circuit, acts as a dc voltage source and requires a large capacitor. From a converter operation point of view, the quality of the ac side output voltage waveform depends on the stability of the capacitor voltage. However, the capacitor needs to absorb low order harmonics that cause not only large voltage variations but also stresses on the capacitor. From the capacitor point of view, it must withstand all the stresses on it: e.g. the maximum voltage, and the voltage as well as the current ripple stresses. In addition, it is important to ensure that the capacitor voltage will permit the targeted MMC operation. It has been noticed that the minimum voltage of the capacitor can become so low during variation that there is not enough voltage storage in the arm to synthesize the desired arm voltage, causing loss-of-control of the converter. In an MMC, SM capacitors account for a significant part of the

system in terms of size, weight and cost. Selection of the SM capacitor is indeed a major issue that needs further investigations.

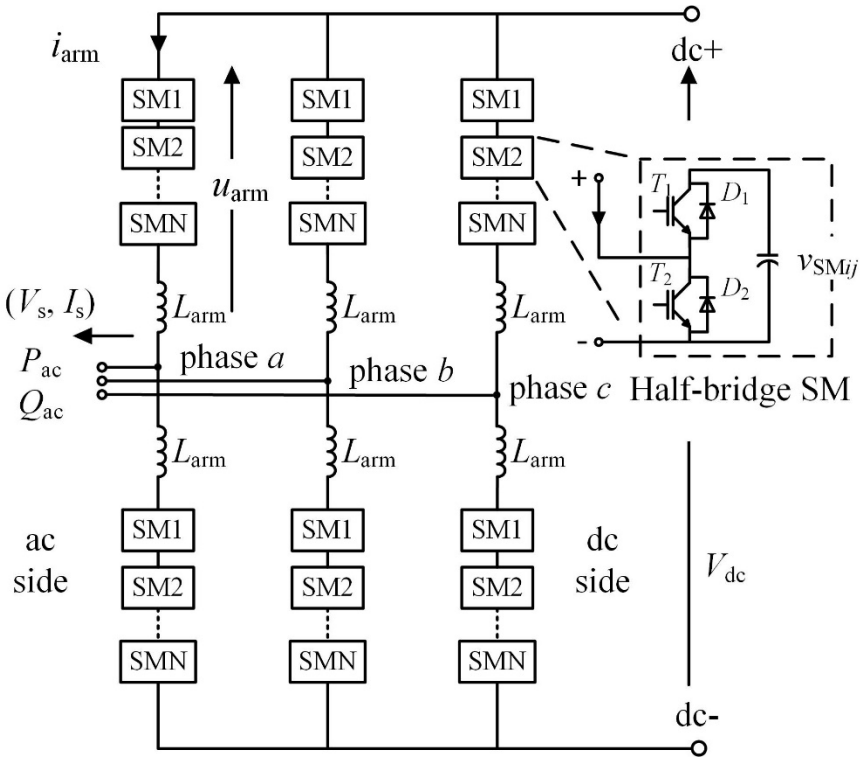

Figure 4.1: Typical structure of an MMC with half-bridge (HB) SM

Characteristics of electrolytic capacitors, ceramic capacitors and film capacitors are studied and compared in Chapter 3. Featuring a low cost, low dissipation and high stability in wide temperature and frequency ranges, MPPF capacitors can be a suitable choice for MMC SMs [77, 88]. The study of their ageing mechanisms indicate the necessicity to consider the maximum capacitor voltage, voltage ripple, as well as the ripple current stress when selecting SM capacitors.

This chapter proposes a new approach based on the estimation of the capacitor voltage ripple. As the design shall include not only the operation status of the converter system but also the safety of the capacitors, Chapter 4.1 briefly reviews the published SM capacitor selection/dimensioning methods. In Chapter 4.2, the analytical expression for the actual

capacitor voltage ripple is derived through the arm energy variation. In order to facilitate the design for applications with various power ratings, values in the model are normalized. In Chapter 4.3, the voltage ripple model is used to derive the required capacitance for three voltage constraints: the maximum capacitor voltage, the voltage ripple, and the SM voltage capability. In addition, the capacitor ripple current stress is also taken into account in capacitor selection. Although this current stress is not capacitance sensitive, the study found it strongly dependent on the operating point (OP) of the converter system. In Chapter 4.4, all capacitance demand functions for the voltage constraints as well as the ripple current stress function are summarized as design curves to reveal how they would change with the OP. The analysis also shows how those constraints would limit the operating region of the system. In Chapter 4.5, a capacitor selection procedure is proposed. Two design examples are presented in Chapter 4.6 with computer simulation to show the validity and ease of use of the proposed procedure. In Chapter 4.7, the capacity of the system is scaled down for experiment verification. A 200 V, 10 A prototype SM is tested in the laboratory. Chapter 4.8 concludes this chapter.

4.1 Review of Published SM Capacitor Selection/Dimensioning Methods

The first and basic capacitor dimensioning method was introduced in [22, 35]:

$$C_{\mathrm{SM}} = \frac{P_{\mathrm{s}}}{3mN\omega\varepsilon V_{\mathrm{SMdc}}^2}\left[1-\left(\frac{m\cos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \tag{4.1}$$

where $P_{\mathrm{s}}=P/\cos\varphi$ is the apparent power of the converter, m the voltage modulation index [defined in (4.14)], N the number of SMs per arm, ω the fundamental frequency, ε the capacitor voltage ripple (peak to average), V_{SMdc} the time average of SM capacitor voltage,

and φ the power factor angle in the ac side. Equation (4.1) offers a simple way to derive the required capacitance, but only the capacitor voltage ripple is considered in the design.

Ilves *et al.* [98] presented a method to derive the required SM capacitance to limit the maximum capacitor voltage. This method also requires that the SM voltage capability requirement shall be satisfied, which states that the total SM capacitor voltage in one arm must be enough to synthesize the required arm voltage at any time in order to deliver the desired ac side phase voltage. However, this method is yet to consider the capacitor voltage ripple, as large voltage ripples may lead to extensive corona discharge and electrochemical corrosion. They may also add to the difficulty of the circulating current suppression control and affect the converter's safe operations.

Barnklau *et al.* [99] proposed a SM capacitor dimensioning method based on equations of energy variation in converter arms. Given the type of the capacitor, sufficient capacitance is selected to ensure that the voltage ripple and the maximum voltage are within the limits. The use of the method is complicated and, like [100] which gives a simpler procedure, the method is yet to include the SM voltage capability requirement.

Perhaps no published method has considered the ripple current stress. As the MMC's operation and the capacitor specification constraints are more completely included, the procedure of the capacitor selection tends to be more complicated. Based on the analysis of the interactions in the MMC, this chapter proposes a more straightforward method to include all the main electrical constraints in the SM capacitor selection.

4.2 Analytical Modeling of the SM Voltage Ripple

As shown in Figure 4.1, the three ac terminals of the MMC are connected to the positive and negative dc busbars through three upper and lower arms respectively. Each arm acts as a filter that absorbs the imbalanced power between the ac and dc sides of the MMC. In steady state, this will cause the energy stored in SM capacitors and hence the capacitor voltage to vary periodically. This section focuses on the derivation of an analytical expression for the SM capacitor voltage ripple based on the periodic arm energy variation.

The instantaneous capacitor voltage $v_{SMij}(t)$ of the $j^{th} \in [1,2, \ldots,N]$ (N is the total number of SMs in one arm) SM in arm $i \in [1,2,\ldots,6]$ can be expressed as

$$v_{SMij}(t) = V_{SMdcij} + v_{SM\sim ij}(t) \tag{4.2}$$

where V_{SMdcij} is the time average of $v_{SMij}(t)$ over a fundamental cycle. The time average of the ac components, i.e. the voltage ripple, $v_{SM\sim ij}$ (t), is zero. For clarity, a symmetrical assembly and balanced operation of the MMC is assumed, meaning that the voltages and currents in all arms are only time shifted with respect to each other. If not specified, all analysis is conducted in the steady state. In addition, SM capacitor voltages in the same arm are assumed to be the same, which can be achieved by various voltage balancing algorithms [19]. Hence, in the rest of the chapter, only the upper arm of phase a is analyzed and subscripts i and j are omitted. (1) changes to

$$v_{SM}(t) = V_{SMdc} + v_{SM\sim}(t)\,. \tag{4.3}$$

The total capacitor voltage in the arm, i.e. the voltage available for arm output is

$$v_{SMtot}(t) = \sum_{j=1}^{N} v_{SMij}(t) = NV_{SMdc} + Nv_{SM\sim}(t)\,. \tag{4.4}$$

where N is the number of SMs in the arm. $Nv_{SM\sim}(t)$ is referred to as the arm's total capacitor

voltage ripple that can also be written as

$$v_{\sim}(t) = N v_{\mathrm{SM}\sim}(t) \tag{4.5}$$

NV_{SMdc} stands for the total dc voltage stored in the arm. In certain cases, NV_{SMdc} may be controlled to be different from the converter pole-to-pole dc-link voltage V_{dc} [98]. In order to consider this, the factor K_{dc} is introduced and equals

$$K_{\mathrm{dc}} = \frac{NV_{\mathrm{SMdc}}}{V_{\mathrm{dc}}} \tag{4.6}$$

where the nominal value of K_{dc} is 1.0. For each OP, V_{SMdc} or $K_{\mathrm{dc}}V_{\mathrm{dc}}/N$ is used as the reference value of the capacitor voltage. Hence, the capacitor voltage ripple in p.u. can be written as

$$v_{\sim\mathrm{p.u.}}(t) = \frac{v_{\mathrm{SM}\sim}(t)}{V_{\mathrm{SMdc}}} = \frac{v_{\sim}(t)}{NV_{\mathrm{SMdc}}}. \tag{4.7}$$

The energy base W_{base} for a converter arm is defined below using the reference capacitor voltage.

$$W_{\mathrm{base}} = \frac{1}{2} N C_{\mathrm{SM}} \left(\frac{K_{\mathrm{dc}} V_{\mathrm{dc}}}{N} \right)^2 = \frac{1}{2} \frac{C_{\mathrm{SM}}}{N} K_{\mathrm{dc}}^2 V_{\mathrm{dc}}^2 \tag{4.8}$$

where C_{SM} is the SM capacitance to be determined. Note that in normal operation, the average stored energy in all capacitors in the arm $W_{\mathrm{armdc\_cap}}$ would be different from the base energy storage W_{base} even when the average capacitor voltage is kept at $K_{\mathrm{dc}}V_{\mathrm{dc}}/N$. The difference between $W_{\mathrm{armdc\_cap}}$ and W_{base} would vary from OP to OP. That is the reason W_{base} is chosen as the reference instead of $W_{\mathrm{armdc\_cap}}$.

The instantaneous capacitor energy storage in one arm can be derived from the arm available voltage in (4.4):

$$w_{\mathrm{arm\_cap}}(t) = \frac{1}{2} \frac{C_{\mathrm{SM}}}{N} \left[NV_{\mathrm{SMdc}} + v_{\sim}(t) \right]^2. \tag{4.9}$$

For each OP, $w_{\mathrm{arm\_cap}}(t)$ can also be written in terms of its time average $W_{\mathrm{armdc\_cap}}$ and ac

components as

$$w_{\text{arm\_cap}}(t) = W_{\text{armdc\_cap}} + e_{\text{arm\_cap}\sim}(t) \tag{4.10}$$

where $e_{\text{arm\_cap}\sim}(t)$ is the periodic capacitor energy variation in the arm (capacitors only, excluding the arm inductors) corresponding to the power exchange into and out of the arm capacitors, $p_{\text{arm\_cap}}(t)$. Equating (4.9) to (4.10) gives

$$W_{\text{armdc\_cap}} + e_{\text{arm\_cap}\sim}(t) = \frac{1}{2}\frac{C_{\text{SM}}}{N}\left[NV_{\text{SMdc}} + v_{\sim}(t)\right]^2. \tag{4.11}$$

Dividing both sides by the base energy storage W_{base} gives

$$e_{\text{arm\_cap}\sim\text{p.u.}}(t) + \frac{W_{\text{armdc\_cap}}}{W_{\text{base}}} = 1 + 2v_{\sim\text{p.u.}}(t) + v^2_{\sim\text{p.u.}}(t) \tag{4.12}$$

where $e_{\text{arm\_cap}\sim\text{p.u.}}(t)$ is the p.u. arm energy variation (capacitor) with respect to W_{base}. Note that the time average of either $e_{\text{arm\_cap}\sim\text{p.u.}}(t)$ or $v_{\sim\text{p.u.}}(t)$ is zero, which is not the case for $v^2_{\sim\text{p.u.}}(t)$. With non-zero $v_{\sim\text{p.u.}}(t)$, $v^2_{\sim\text{p.u.}}(t)$ would contain a dc offset. In such a case, $W_{\text{armdc\_cap}}$ would be higher than W_{base} as shown in (4.12). The difference between the two values in p.u. is defined as *Diff*W and can be derived by

$$Diff_W = \frac{W_{\text{armdc\_cap}} - W_{\text{base}}}{W_{\text{base}}} = \overline{v^2_{\sim\text{p.u.}}(t)} = \frac{1}{2}\sum_n \hat{V}^2_{\sim\text{p.u.n}} \tag{4.13}$$

where $\hat{V}_{\sim\text{p.u.n}}$ is the magnitude of the n^{th} order component in $v_{\sim\text{p.u.}}(t)$. $Diff_W$ is constant for a certain OP and may vary from one OP to another.

As $[e_{\text{arm\_cap}\sim\text{p.u.}}(t)+Diff_W]$ is always greater than -1, $v_{\sim\text{p.u.}}(t)$ can be solved from (4.12) as

$$v_{\sim\text{p.u.}}(t) = -1 + \sqrt{\frac{e_{\text{arm\_cap}\sim}(t) + W_{\text{armdc\_cap}}}{W_{\text{base}}}} = -1 + \sqrt{1 + e_{\text{arm\_cap}\sim\text{p.u.}}(t) + Diff_W} \tag{4.14}$$

while the other root is less than -1 and thus discarded.

Equation (4.14) offers a way to calculate the instantaneous capacitor voltage ripple. Derivation of the arm energy variation $e_{\text{arm\_cap}\sim}(t)$ is well documented in [98-100] using the

integration of the power exchange $p_{arm\_cap}(t)$. This power can be derived as the product of the arm current $i_{arm}(t)$ and the arm output voltage $u_{arm\_cap}(t)$ as

$$p_{arm\_cap}(t) = u_{arm\_cap}(t) i_{arm}(t). \tag{4.15}$$

Note that the arm output voltage is only the voltage synthesized by SM capacitors, excluding the arm inductor voltage. The reference polarity and direction of $u_{arm\_cap}(t)$ and $i_{arm}(t)$ are marked in Figure 4.1. Hence, $e_{arm\_cap\sim}(t)$ can be derived as

$$e_{arm\_cap\sim}(t) = \int_0^{\tau} p_{arm\_cap}(\tau) d\tau. \tag{4.16}$$

4.3 Derivation of Capacitance Demand Functions and Ripple Current Stress Function

This part focuses on the derivation of the capacitance demand functions to satisfy the three voltage requirements using the analytical model of the capacitor voltage ripple. Although the capacitor ripple current stress is not capacitance sensitive, it is vital in capacitor selection. Hence, the relation between the ripple current stress and the OP of the MMC will also be derived. Equations (4.14), (4.15) and (4.16) can be applied to all types of MMCs so long as the arm current $i_{arm}(t)$ and the arm output voltage $u_{arm\_cap}(t)$ are known. In order to show how the proposed method can be applied, the system in Figure 4.1 is used as a design example, which is a typical structure for applications such as HVDC converters and static VAr compensation (STATCOM).

Assumptions are made in the analysis: the number of converter levels is high enough to give sinusoidal ac side phase voltage and current with rms magnitudes of V_s and I_s respectively; the high frequency components caused by SM switching are not considered. All devices are treated as ideal. The third order harmonic voltage injection is not considered. As

this chapter focuses on the SM capacitance requirements of the MMC, the arm inductors are firstly neglected. A method to include the arm inductor effect for specific designs will be introduced later. The arm voltage can be expressed as

$$u_{\text{arm\_cap}}(t) = u_{\text{arm}}(t) = \frac{V_{\text{dc}}}{2} - \frac{V_{\text{dc}}}{2} m \sin(\omega t) \tag{4.17}$$

where ω is the fundamental angular frequency and the modulation index m is defined as

$$m = 2\sqrt{2}\frac{V_{\text{s}}}{V_{\text{dc}}}. \tag{4.18}$$

Note that m must not be larger than 1 for MMCs with half-bridge SMs and without third order harmonic voltage injection.

If the converter is controlled in such a way that there are no harmonics in the circulating current [19], the arm current can be expressed as [98]

$$i_{\text{arm}}(t) = \frac{\sqrt{2}I_{\text{s}}}{4} m\cos\varphi + \frac{\sqrt{2}I_{\text{s}}}{2}\sin(\omega t - \varphi). \tag{4.19}$$

where φ is the ac side power factor angle. In certain cases that the third harmonic voltage injection is applied for operating region extension or the harmonic current injection is used to shape the capacitor voltage ripple and reduce the capacitor capacitance [55,98,101], (4.17) and (4.19) can be updated accordingly. The following SM capacitor sizing calculations still apply.

Substituting (4.17) and (4.19) into (4.15) and then (4.16) gives the arm energy variation as

$$e_{\text{arm\_cap}\sim}(t) = \frac{\sqrt{2}I_{\text{s}}V_{\text{dc}}}{\omega} f(m,\varphi,t) \tag{4.20a}$$

$$\begin{aligned} f(m,\varphi,t) = \frac{1}{16}[&-4\cos(\omega t - \varphi) \\ &+2m^2\cos\varphi\cos(\omega t) + m\sin(2\omega t - \varphi)] \end{aligned} \tag{4.20b}$$

where $f(m, \varphi, t)$ defines the shape of the arm energy variation (capacitor) that is invariant from cycle to cycle for a certain OP(m, φ). The magnitude of the arm energy variation varies with the ac and dc sides output status of the MMC regardless of the inner structure. In order to relate the arm energy variation to the capacitor voltage ripple, the p.u. arm energy variation is derived through dividing both sides of (4.20a) by the base energy storage in (4.8) as

$$e_{\text{arm\_cap}\sim\text{p.u.}}(t) = \frac{2\sqrt{2}NI_{\text{s}}}{\omega C_{\text{SM}} K_{\text{dc}}^2 V_{\text{dc}}} f(m,\varphi,t)\,. \tag{4.21}$$

According to (4.14) and (4.21), for future reference, two extremes of $v_{\sim\text{p.u.}}(t)$ at each OP are

$$V_{\sim\text{p.u.max}} = -1 + \sqrt{1 + E_{\text{arm\_cap}\sim\text{p.u.max}} + Diff_W} \tag{4.22a}$$

$$V_{\sim\text{p.u.min}} = -1 + \sqrt{1 + E_{\text{arm\_cap}\sim\text{p.u.min}} + Diff_W} \tag{4.22b}$$

where

$$E_{\text{arm\_cap}\sim\text{p.u.max}} = A_e f_{\max}(m,\varphi) = A_e \max\left[f(m,\varphi,t)\right]_{t\in T} \tag{4.23a}$$

$$E_{\text{arm\_cap}\sim\text{p.u.min}} = A_e f_{\min}(m,\varphi) = A_e \min\left[f(m,\varphi,t)\right]_{t\in T} \tag{4.23b}$$

$$A_e = \frac{2\sqrt{2}NI_{\text{s}}}{\omega C_{\text{SM}} K_{\text{dc}}^2 V_{\text{dc}}} \tag{4.24}$$

and T is the period of a fundamental cycle that equals ($\omega/2\pi$).

4.3.1 Requirement according to maximum capacitor voltage

In order to prevent fast ageing, the rated capacitor voltage V_{Cr} must be greater than the maximum voltage experienced in operation at all times, that is

$$V_{\text{Cr}} > v_{\text{SM}\sim}(t)\,. \tag{4.25}$$

The allowable maximum voltage excess V_{excess} is defined as the difference between the

rated capacitor voltage and the SM rated dc voltage V_{SMdc}. Its p.u. value, $V_{\text{excessp.u.}}$, can be written as

$$V_{\text{excessp.u.}} = \frac{V_{\text{Cr}} - V_{\text{SMdc}}}{V_{\text{SMdc}}}. \tag{4.26}$$

If $V_{\text{excessp.u.}}$ is known according to the limits of the selected capacitors or other hardware, the following condition must be satisfied:

$$V_{\sim\text{p.u.max}} \le V_{\text{excessp.u.}}. \tag{4.27}$$

Substituting (4.22a) into (4.27) gives the minimum required C_{SM} for the maximum voltage requirement as

$$C_{\text{SM}} \ge \frac{\sqrt{2}NI_{\text{s}}}{\omega K_{\text{dc}}^2 V_{\text{dc}}} f_{\text{excess}}(m, \varphi, V_{\text{excessp.u.}}, Diff_W) \tag{4.28a}$$

$$f_{\text{excess}}(m, \varphi, V_{\text{excessp.u.}}, Diff_W) = \frac{f_{\max}(m, \varphi)}{\frac{V_{\text{excessp.u.}}^2}{2} + V_{\text{excessp.u.}} - \frac{Diff_W}{2}}. \tag{4.28b}$$

4.3.2 SM voltage capability requirement

The SM voltage capability requirement states that the total SM capacitor voltage in one arm must be enough to synthesize the required arm voltage at any time in order to deliver the desired ac side phase voltage, that is

$$v_{\text{SMtot}}(t) \ge u_{\text{arm\_cap}}(t) \ge 0. \tag{4.29}$$

Substituting (4.4) and (4.17) into (4.29) gives

$$NV_{\text{SMdc}} + v_{\sim}(t) \ge \frac{V_{\text{dc}}}{2} - \frac{V_{\text{dc}}}{2} m \sin(\omega t) \ge 0. \tag{4.30}$$

Dividing both sides by the total SM rated voltage NV_{SMdc} gives

$$1 + v_{\sim\text{p.u.}}(t) \ge \frac{1}{2K_{\text{dc}}} - \frac{1}{2K_{\text{dc}}} m \sin(\omega t) \ge 0. \tag{4.31}$$

Note that NV_{SMdc} equals $K_{\mathrm{dc}}V_{\mathrm{dc}}$ when required.

Substituting (4.14) into (4.31) and squaring both sides of the equation lead to

$$e_{\mathrm{arm\_cap\sim p.u.}}(t) \geq \frac{1}{K_{\mathrm{dc}}^2}\left(\frac{1}{2}-\frac{1}{2}m\sin\omega t\right)^2 - 1 - Diff_W = g(m,t,Diff_W,K_{\mathrm{dc}}). \qquad (4.32)$$

When K_{dc} is equal to or greater than 1.0, $g(.)$ is always negative with non-zero $Diff_W$. However, when K_{dc} is set to low values for certain reasons, $g(.)$ may be positive. The physical meaning of the two cases will be discussed later. When $g(.)$ is negative, substituting (4.21) into (4.32) results in

$$\frac{2\sqrt{2}NI_{\mathrm{s}}}{\omega C_{\mathrm{SM}}K_{\mathrm{dc}}^2V_{\mathrm{dc}}}f(m,\varphi,t) \geq g(m,t,Diff_W,K_{\mathrm{dc}}). \qquad (4.33)$$

Rearranging (4.33) gives

$$C_{\mathrm{SM}} \geq \frac{\sqrt{2}NI_{\mathrm{s}}}{\omega K_{\mathrm{dc}}^2V_{\mathrm{dc}}}\frac{2f(m,\varphi,t)}{g(m,t,Diff_W,K_{\mathrm{dc}})}. \qquad (4.34)$$

As the equation must be satisfied at all times during a cycle T, C_{SM} must be no smaller than the maximum value of the right hand side of (4.34). In order to comply with (4.28a) and (4.28b), $f_{\mathrm{cap}}(.)$ is defined as the capacitance demand function for the voltage capability requirement, which can be derived as

$$f_{\mathrm{cap}}(m,\varphi,Diff_W,K_{\mathrm{dc}}) = \max\left[\frac{2f(m,\varphi,t)}{g(m,t,Diff_W,K_{\mathrm{dc}})}\right]_{t\in T,g(.)<0}. \qquad (4.35)$$

And (4.34) then becomes

$$C_{\mathrm{SM}} \geq \frac{\sqrt{2}NI_{\mathrm{s}}}{\omega K_{\mathrm{dc}}^2V_{\mathrm{dc}}}f_{\mathrm{cap}}(m,\varphi,Diff_W,K_{\mathrm{dc}}). \qquad (4.36)$$

When $g(.)$ is positive, (4.36) and (4.35) become

$$C_{\mathrm{SM}} \leq \frac{\sqrt{2}NI_{\mathrm{s}}}{\omega K_{\mathrm{dc}}^2V_{\mathrm{dc}}}f_{\mathrm{cap}}(m,\varphi,Diff_W,K_{\mathrm{dc}}) \qquad (4.37)$$

$$f_{\text{cap}}(m,\varphi,Diff_W,K_{\text{dc}}) = \min\left[\frac{2f(m,\varphi,t)}{g(m,t,Diff_W,K_{\text{dc}})}\right]_{t\in T,g(.)>0}. \quad (4.38)$$

The difference between (4.36) and (4.37) is explained in Figure 4.2. When $g(.)$ is always negative, the arm output voltage is always lower than the total average SM capacitor voltage NV_{SMdc} or $K_{\text{dc}}V_{\text{dc}}$ as in Figure 4.2(a). In such a case, the voltage ripple must be small enough to ensure that the total SM capacitor voltage is always enough for the arm output, especially when $v_{\text{SM}\sim}(t)$ is negative. That is the reason C_{SM} has an allowable minimum boundary. This case is common in applications including HVDC, STATCOM, and motor drive in the steady state. This minimum C_{SM} exists in all operation region of the system.

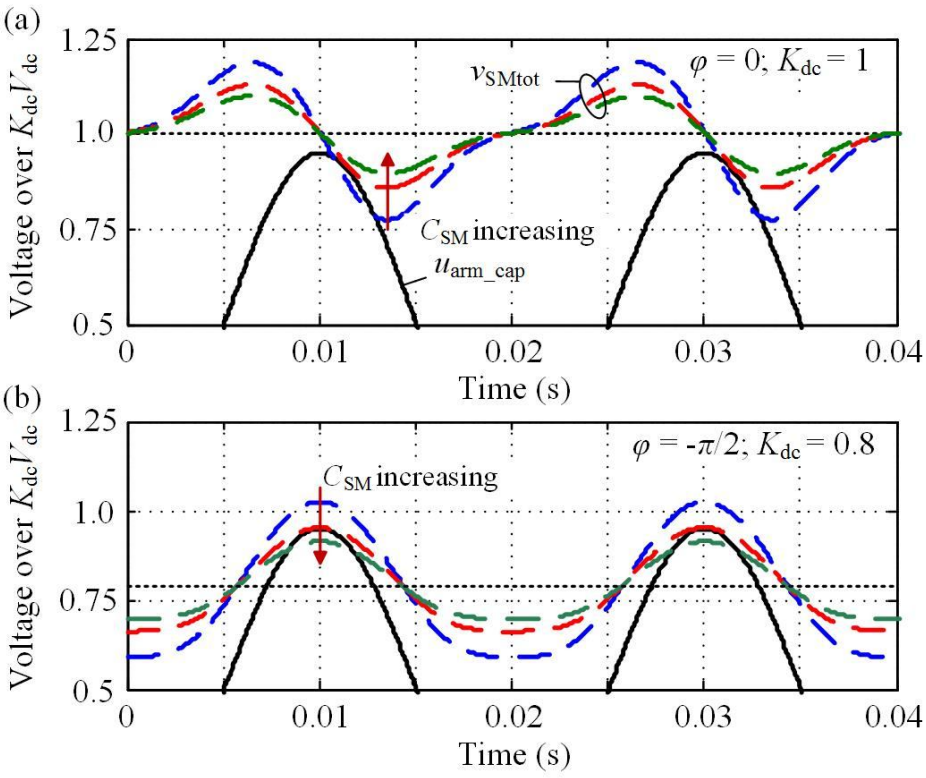

Figure 4.2: Illustration of the relations between the arm output voltage $u_{\text{arm\_cap}}$ and the total available voltage v_{SMtot}

Figure 4.2(b) shows another case that $g(.)$ would be positive sometimes in the cycle. In such a case, the arm output voltage will be larger than $K_{\text{dc}}V_{\text{dc}}$ during certain period of time.

As shown in the figure, in order to satisfy the voltage capability requirement, C_{SM} needs to be as small as possible in order to have larger voltage ripple to allow for the high arm output voltage. That is the reason C_{SM} may also have an upper boundary as in (4.37). This phenomenon can be only found when the converter drives inductive loads. Such property of the MMC is usually used in variable-speed drives during motor starting to reduce the capacitance demand when ω is small [102, 103].

4.3.3 Capacitor voltage ripple requirement

Corona discharge and electrochemical corrosion effects set the limit of capacitor ac voltage, i.e. the voltage ripple (refer to Chapter 3.4.3 [93-95]). In addition, large voltage ripple will add to the difficulty of the circulating current suppression control and may affect the converter's stability. If the allowable voltage ripple in p.u. $V_{\text{ripplep.u.}}$ (peak-to-peak) is known, the following condition must be satisfied at all times:

$$V_{\sim\text{p.u.max}} - V_{\sim\text{p.u.min}} \le V_{\text{ripplep.u.}} . \tag{4.39}$$

Substituting (4.22a), (4.22b), (4.23a) and (4.23b) into (4.39) gives:

$$\begin{aligned} &\left[f_{\max}(m,\varphi) - f_{\min}(m,\varphi)\right]^2 A_e^2 \\ &\quad - 2\left[f_{\max}(m,\varphi) + f_{\min}(m,\varphi)\right] V_{\text{ripplep.u.}}^2 A_e \\ &\quad + V_{\text{ripplep.u.}}^4 - 4V_{\text{ripplep.u.}}^2 \left(1 + Diff_W\right) \le 0 \end{aligned} \tag{4.40}$$

As A_e is always positive as shown in (4.24), (4.40) requires

$$A_e \le \frac{2\left[f_{\max}(m,\varphi) + f_{\min}(m,\varphi)\right] V_{\text{ripplep.u.}}^2 + \sqrt{\Delta}}{2\left[f_{\max}(m,\varphi) - f_{\min}(m,\varphi)\right]^2} \tag{4.41}$$

where

$$\begin{aligned} \Delta = {} & 16 f_{\max}(m,\varphi) f_{\min}(m,\varphi) V_{\text{ripplep.u.}}^4 \\ & + 16\left[f_{\max}(m,\varphi) - f_{\min}(m,\varphi)\right]^2 \left(1 + Diff_W\right) V_{\text{ripplep.u.}}^2 \end{aligned} .$$

Substituting (4.24) into (4.41) gives:

$$C_{\mathrm{SM}} \geq \frac{\sqrt{2}NI_{\mathrm{s}}}{\omega K_{\mathrm{dc}}^2 V_{\mathrm{dc}}} f_{\mathrm{ripple}}(m,\varphi,V_{\mathrm{ripplep.u.}},Diff_W) \tag{4.42a}$$

$$f_{\mathrm{ripple}}(m,\varphi,V_{\mathrm{ripplep.u.}},Diff_W) = \frac{4\left[f_{\max}(m,\varphi)-f_{\min}(m,\varphi)\right]^2}{2\left[f_{\max}(m,\varphi)+f_{\min}(m,\varphi)\right]V_{\mathrm{ripplep.u.}}^2+\sqrt{\Delta}}. \tag{4.42b}$$

4.3.4 Ripple current

In normal operation, the arm current $i_{\mathrm{arm}}(t)$ will pass through all the SMs switched in the same arm. In other words, the current through a SM capacitor, $i_{\mathrm{SMC}}(t)$ is just segments of $i_{\mathrm{arm}}(t)$ during the capacitor-switched-in intervals. Without knowing the switching pattern, detailed expression of $i_{\mathrm{SMC}}(t)$ is hard to derive. Nonetheless, once the arm voltage in (4.17) and the total SM capacitor voltage in the arm are known, the average switching duty for each SM is determined. Together with the arm current in (4.19), the rms value of $i_{\mathrm{SMC}}(t)$ can be estimated as follows.

Figure 4.3(a) shows typical waveforms in a SM capacitor. The solid line is the actual instantaneous capacitor voltage ripple of SM j in arm i, and the dashed line the average capacitor voltage of all SMs in that arm. In a balanced system, capacitor voltages in the same arm are controlled to be close to each other and approximately equal to the average between them. Figure 4.3(b) and (c) show zoomed views of switching cycle p with a duration of $T_{0\mathrm{p}}$. Generally, the switching duration varies from cycle to cycle. For simplicity, the capacitor current is first assumed constant as shown in Figure 4.3(c). Since at the end of the switching cycle both $v_{\mathrm{SM}ij\sim}$ and $v_{\mathrm{SM}\sim}$ increase by the same amount, the following holds true:

$$I_{\mathrm{SMC}ij}T_{\mathrm{inp}} = I_{\mathrm{arm}}T_{\mathrm{inp}} = I_{\mathrm{SMCave}}T_{0\mathrm{p}} \tag{4.43}$$

where I_{SMCave} is the average capacitor current [refer to Figure 4.3(c)] and T_{inp} the SM switched-in period in the switching cycle p. Note that during T_{inp}, the actual capacitor current I_{SMC} equals the arm current.

If the capacitor current is not constant and the SM would switch multiple (k) times in a fundamental cycle T, its rms value can be derived by

$$I_{\mathrm{SMC\_RMS}} = \sqrt{\frac{1}{T}\int_0^T i_{\mathrm{SMC}ij}^2(t)dt} = \sqrt{\frac{1}{T}\sum_{p=1}^{k}\int_{\tau_{0(\mathrm{p}-1)}}^{\tau_{0\mathrm{p}}} i_{\mathrm{SMC}ij}^2(t)dt} = \sqrt{\frac{1}{T}\sum_{p=1}^{k}\int_{\tau_{\mathrm{in}(\mathrm{p}-1)}}^{\tau_{\mathrm{inp}}} i_{\mathrm{arm}}^2(t)dt} \quad (4.44)$$

where $\tau_{0(\mathrm{p}-1)}$ is the beginning of the switching cycle p and $\tau_{0\mathrm{p}}$ is the end. $\tau_{\mathrm{in}(\mathrm{p}-1)}$ is the beginning of the switched-in instant in switching cycle p and τ_{inp} is the end. In high voltage high power applications, k usually ranges from 3 to 5, while in medium voltage applications, k may have higher values. As shown in Figure 4.3(e), if any SM switched-in period [$\tau_{\mathrm{in}(\mathrm{p}-1)}$, τ_{inp}] is evenly divided into M sections (M can be assumed to be infinity), (4.44) can be further written as

$$\sqrt{\frac{1}{T}\sum_{p=1}^{k}\int_{\tau_{\mathrm{in}(\mathrm{p}-1)}}^{\tau_{\mathrm{inp}}} i_{\mathrm{arm}}^2(t)dt} = \sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\int_{\tau_{\mathrm{inp}(\mathrm{q}-1)}}^{\tau_{\mathrm{inpq}}} i_{\mathrm{arm}}^2(t)dt}\,. \quad (4.45)$$

As M is large, in each section q [$\tau_{\mathrm{inp}(\mathrm{q}-1)}$, τ_{inpq}] the current can be treated as constant. The duration of the section q equals T_{inp}/M. Then, substituting (4.43) into (4.45) yields

$$\begin{aligned}\sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\int_{\tau_{\mathrm{inp}(\mathrm{q}-1)}}^{\tau_{\mathrm{inpq}}} i_{\mathrm{arm}}^2(t)dt} &= \sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\frac{T_{\mathrm{inp}}}{M} I_{\mathrm{arm}}^2\Big|_{t=\tau_{\mathrm{inp}(\mathrm{q}-1)}}} \\ &= \sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\frac{T_{0\mathrm{p}}}{M} I_{\mathrm{arm}}\Big|_{t=\tau_{\mathrm{inp}(\mathrm{q}-1)}} I_{\mathrm{SMCave}}\Big|_{t=\tau_{\mathrm{inp}(\mathrm{q}-1)}}}\,.\end{aligned} \quad (4.46)$$

The last expression in (4.46) indicates that the integration of I^2_{arm} over T_{inp}/M is equivalent to the integration of ($I_{\mathrm{arm}}I_{\mathrm{SMCave}}$) over $T_{0\mathrm{p}}/M$. Hence, (4.46) can be written into a continuous format as

$$\sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\frac{T_{0\mathrm{p}}}{M} I_{\mathrm{arm}}\Big|_{t=\tau_{\mathrm{inp}(\mathrm{q}-1)}} I_{\mathrm{SMCave}}\Big|_{t=\tau_{\mathrm{inp}(\mathrm{q}-1)}}} = \sqrt{\frac{1}{T}\sum_{p=1}^{k}\sum_{q=1}^{M}\int_{\tau_{0\,\mathrm{p}(\mathrm{q}-1)}}^{\tau_{0\,\mathrm{pq}}} i_{\mathrm{arm}}(t) i_{\mathrm{SMCave}}(t)dt} \quad (4.47)$$

Note the approximation is conducted in each section divided by M instead of the switching cycle decided by k. So long as SM capacitor voltages are well balanced, this approximation applies even when k is low, such as 2. Equation (4.47) further leads to

$$I_{\text{SMC\_RMS}} = \sqrt{\frac{1}{T}\int_0^T i_{\text{arm}}(t) i_{\text{SMCave}}(t) dt} \tag{4.48}$$

where $i_{\text{SMCave}}(t)$ can be derived by

$$i_{\text{SMCave}}(t) = C_{\text{SM}} \frac{dv_{\text{SM}\sim}(t)}{dt}. \tag{4.49}$$

Substituting (4.7) and (4.14) into (4.49) gives $i_{\text{SMCave}}(t)$. Substituting the resultant equation into (4.48) gives

$$I_{\text{SMC\_RMS}} = I_{\text{s}} f_{I_{\text{Cripple}}}(m, \varphi, V_{\text{ripplep.u.}}, Diff_W, K_{\text{dc}}) \tag{4.50a}$$

$$f_{I_{\text{Cripple}}}(m, \varphi, V_{\text{ripplep.u.}}, Diff_W, K_{\text{dc}}) = \sqrt{\frac{1}{T}\int_0^T \frac{\frac{i_{\text{arm}}(t)}{I_{\text{s}}} \frac{C_{\text{SM}} K_{\text{dc}} V_{\text{dc}}}{2NI_{\text{s}}} \frac{de_{\text{arm\_cap\sim p.u.}}(t)}{dt}}{\sqrt{1 + e_{\text{arm\_cap\sim p.u.}}(t) + Diff_W}} dt}. \tag{4.50b}$$

Note that I_{s} is taken outside the root sign for normalization.

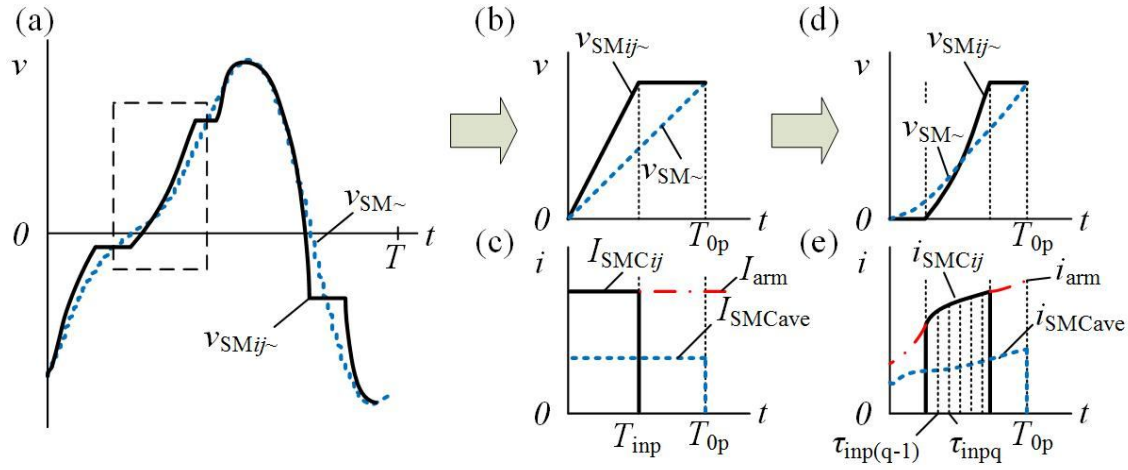

Figure 4.3: Illustrations for derivation of capacitor ripple current stress: (a) Typical SM capacitor voltage ripple (solid line) and average voltage ripple of all SMs in the arm; (b) zoomed view of the capacitor voltage ripple in switching cycle p with duration $T_{0\text{p}}$ and constant SM capacitor current as shown in (c); (d) zoomed view of the capacitor voltage ripple in switching cycle p with duration $T_{0\text{p}}$ and actual SM capacitor current as shown in (e)

4.3.5 Effect of the arm inductor

In the derivation of the above functions, the arm inductors are neglected. However, in order to avoid resonance and limit the rising rate of the arm currents especially during a dc side fault, the inductance of arm inductors is usually not trivial [55]. Neglecting this may lead to over/underestimation of C_{SM} and affect the safe operation. Generally, the arm inductor causes an effect that in order to compensate the voltage on the inductor, the actual arm voltage synthesized by SMs in (4.17) changes to:

$$u_{\mathrm{arm\_cap}}(t) = \frac{V_{\mathrm{dc}}}{2} - \frac{V_{\mathrm{dc}}}{2} m \sin(\omega t) - \frac{V_{\mathrm{dc}}}{2} K_L \cos(\omega t - \varphi) \tag{4.51a}$$

$$K_L = \frac{\sqrt{2}\omega I_{\mathrm{s}}}{V_{\mathrm{dc}}} L_{\mathrm{arm}} . \tag{4.51b}$$

Instead of re-calculating the voltage and ripple current requirement functions, (4.51a) is rearranged as

$$u_{\mathrm{arm\_cap}} = \frac{V_{\mathrm{dc}}}{2} - \frac{V_{\mathrm{dc}}}{2} m_{\mathrm{arm\_cap}} \sin\left(\omega t + \beta\right) \tag{4.52a}$$

$$m_{\mathrm{arm\_cap}} = \sqrt{m^2 + K_L^2 + 2mK_L \sin\varphi} \tag{4.52b}$$

$$\beta = \arctan\frac{K_L \cos\varphi}{m + K_L \sin\varphi} \tag{4.52c}$$

$$\varphi_{\mathrm{arm\_cap}} = \beta + \varphi \tag{4.52d}$$

where $m_{\mathrm{arm\_cap}}$ and $\varphi_{\mathrm{arm\_cap}}$ are the updated modulation index and power factor angle for arm capacitors when the arm inductor effect is included.

4.4 Evaluation of Capacitance Demand Functions and Ripple Current Stress Function

As shown in (4.28a), (4.36) or (4.37) and (4.42a), the required C_{SM} for a certain voltage constraint is the product of a coefficient related to the converter's specifications (N, I_s, ω, K_{dc} and V_{dc}) and a function of the operating point. In the following, the functions $f_{excess}(.)$ in (4.28b), $f_{cap}(.)$ in (4.35) or (4.38) and $f_{ripple}(.)$ in (4.42b) are referred to as the capacitance demand functions. For the same reason, $f_{ICripple}(.)$ is referred to as the ripple current stress function. By changing the parameters in these functions, the effects of the MMC's operation mode and different design parameters ($V_{excessp.u.}$ and $V_{ripplep.u.}$) on the demand of C_{SM} as well as the ripple current stress can be included. It will in return help to give a comprehensive understanding of how the SM capacitance and the capacitor's ripple current capability will limit the operating region of the converter. For this insight, the three capacitance demand functions and the ripple current stress function will be analyzed in this part.

Before the detailed analysis, two points are clarified. Firstly, for simplicity, time average of the SM capacitor voltage V_{SMCdc} is treated constant and K_{dc} is set to its nominal value 1.0. In practice, if K_{dc} is set to other values, the analysis is still valid as long as K_{dc} is updated. In addition, once the system parameters are decided, K_{dc} can also be adjusted in normal operation for certain control objective. Equation (4.28a), (4.36) or (4.37) and (4.42a) can be used to find the suitable values for K_{dc} to ensure the system's safe operation by checking whether the selected C_{SM} is still sufficient. Secondly, all capacitance demand functions include $Diff_W$, which depends on the magnitudes of the harmonic components in the capacitor voltage ripple, as in (4.13). Without the exact value of C_{SM}, the voltage ripple is not known and $Diff_W$ cannot be accurately calculated. To solve the problem, two methods are given to estimate the value of $Diff_W$. The relative errors are also analyzed in detail.

4.4.1 Estimation of $Diff_W$

One way to estimate $Diff_W$ for a certain OP is through the allowable voltage ripple $V_{\text{ripplep.u.}}$. As shown in (4.41), if the voltage ripple requirement is satisfied, the upper boundary of the design variable A_e [defined in (4.24)] can be derived. Substi-tuting the resultant A_e into (4.21) and then into (4.14), the voltage ripple can be roughly estimated. Note $Diff_W$ is usually very small compared with $e_{\text{arm\_cap\sim p.u.}}(t)$. It is neglected in the estimation. Then the value of $Diff_W$ can be derived using (4.13). Simple computer programming can facilitate the calculation. In practice, if the actual voltage ripple is smaller than the permitted value, the estimated $Diff_W$ will be larger than the actual value. This method gives every good accuracy when the voltage ripple is less than 50% peak-peak, which is common in applications such as HVDC and STATCOM. If the voltage ripple is not the limiting parameter, the actual voltage ripple can be estimated through other voltage constraints. For instance, if the maximum voltage constraint dominates, the voltage ripple is approximately equal to twice of V_{excess}.

In order to show how the value of $Diff_W$ will affect the voltage and the ripple current functions, a simpler estimation of $Diff_W$ is used. In the example system as in Figure 4.1, assuming that all harmonic circulating currents are eliminated, the capacitor voltage ripple $v_{\sim\text{p.u.}}(t)$ would mainly contain a fundamental component and a 2nd order harmonic with lower amplitude [20%-40% of the fundamental depending on the OP]. Higher order harmonics have smaller amplitudes and can be neglected. Hence, $Diff_W$ can be estimated using (4.13) as

$$Diff_{W\_e} = \frac{1}{2}\left[\underbrace{\left(\hat{V}_{\sim\text{p.u.1}}\right)^2}_{1st\ order} + \underbrace{\left(0.4\hat{V}_{\sim\text{p.u.1}}\right)^2}_{2nd\ order}\right]. \tag{4.53}$$

If the amplitude of the 2nd order harmonic voltage ripple is actually less than 40% of the first order, (50) estimates the maximum $Diff_W$ for a certain $V_{\sim\text{p.u.1}}$. Also, note that the peak-peak ripple of $v_{\sim\text{p.u.}}(t)$ is always larger than $2\hat{V}_{\sim\text{p.u.1}}$. When $\hat{V}_{\sim\text{p.u.1}}$ is 0.05, 0.1, 0.15, 0.2

or 0.25, $Diff_{W\_e}$ will be 0.0015, 0.0058, 0.0130, 0.0232 or 0.0363 respectively.

4.4.2 Capacitance demand function – $f_{excess}(.)$

For the maximum capacitor voltage requirement, $f_{max}(m,\varphi)$ is depicted in Figure 4.4 for m = 0.7, 0.8 and 0.9 and φ over 0 to 2π. With certain $V_{excessp.u.}$ and $Diff_W$, values of $f_{excess}(.)$ can be derived by (4.28b). Figure 4.4 shows that due to the change of the phase angle between the arm current and arm voltage, the shape of the SM capacitor voltage ripple varies accordingly. As an example, the SM capacitor will have higher peak when the converter generates lagging reactive power than the case when the converter consumes the same amount of reactive power.

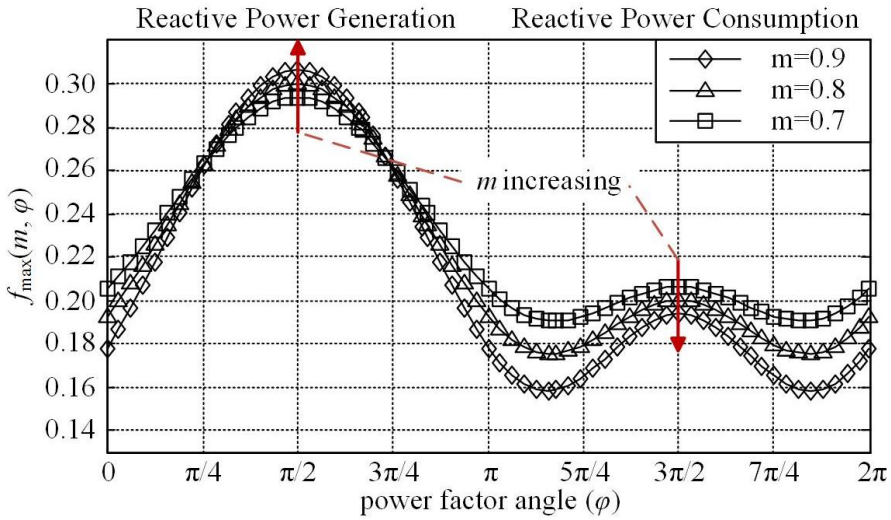

Figure 4.4: $f_{max}(m,\varphi)$ when m equals 0.7, 0.8 and 0.9 with φ varies from 0 to 2π

4.4.3 Capacitance demand function – $f_{cap}(.)$

The values of $f_{cap}(m, \varphi, Diff_W, K_{dc})$ are depicted in Figure 4.5. Since K_{dc} is set to 1.0, as shown in Figure 4.2(a), the arm output voltage is always lower than the total SM capacitor dc voltage. Hence, the capacitance demand functions in (4.35) and (4.36) are used. The marked lines show the values of $f_{cap}(.)$ with $Diff_W$ setting to 0 while the unmarked lines show the values with $Diff_W$ setting to two estimated values. Figure 4.5 shows that the demands of

capacitance vary significantly with different OP (m, φ) of the system. As the OP changes, the process to charge or discharge the capacitor would vary accordingly. For instance, when the converter generates lagging reactive power, the capacitor is charged to the maximum by the arm current when the peak arm voltage is required. However, when the converter consumes reactive power, the capacitor is discharged to the minimum when the required arm voltage is high. That is the reason that for a fixed modulation index m, larger C_{SM} is required when the converter consumes reactive power in order to limit the voltage drop and ensure sufficient SM voltages available for output. Moreover, since higher values of m indicate higher peak arm voltage as in (4.17), for a certain φ, especially when the converter consumes reactive power, larger C_{SM} is required. Hence, as shown in (4.36), in applications such as a STATCOM that is designed to consume reactive power, the capacitance demand can be reduced by increasing K_{dc}. Note that this action may violate the maximum voltage constraint and the energy storage level of the system would still increase if capacitors with higher rated voltage has to be used. In such a case, the selection of capacitor is a trade-off between choosing capacitors with higher rated voltage or larger capacitance.

The unmarked dotted and dashed lines in Figure 4.5 show $f_{cap}(.)$ with non-zero $Diff_W$ settings. The two circles in Figure 4.5 indicate that neglecting $Diff_W$ would lead to overestimation of C_{SM} as can also be seen in (4.32) and (4.35). Figure 4.6 shows the relative error in the value of $f_{cap}(.)$ due to neglecting $Diff_W$, defined as

$$Error_{cap}(m,\varphi,Diff_W)=\frac{f_{cap}(m,\varphi,0,1)-f_{cap}(m,\varphi,Diff_W,1)}{f_{cap}(m,\varphi,Diff_W,1)}. \qquad (4.54)$$

When $Diff_W$ is large (=0.0232) and with high m settings, the error can be large especially when the converter consumes reactive power. When $Diff_W$<0.0058 ($V_{ripplep.u}$<0.2), the error of overestimation will be less than 5%. Hence, for MMCs with small voltage ripples ($V_{ripplep.u}$≤0.2), the marked lines in Figure 4.5 can be directly used for manual calculation

with Figure 4.6 for error compensation. For MMCs with larger voltage ripples, it would be more accurate to estimate $Diff_W$ using the method offered in Chapter 4.4.1 for each OP and calculate the exact $f_{cap}(.)$ values using (4.35) or (4.38). Simple computer programming can facilitate the calculation.

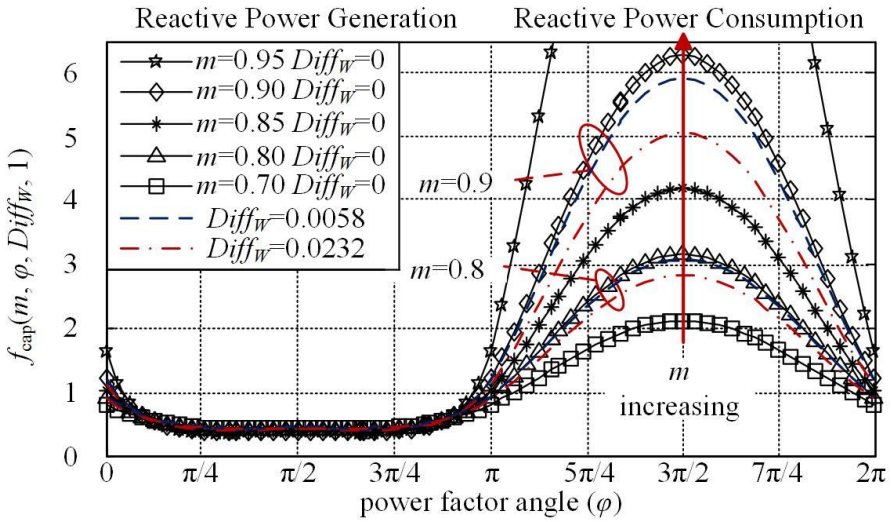

Figure 4.5: $f_{cap}(m,\varphi,Diff_W,1)$ with various m and φ. $Diff_W$=0 for marked black lines; $Diff_W$ =0.0058 for unmarked blue lines and $Diff_W$=0.0232 for red lines

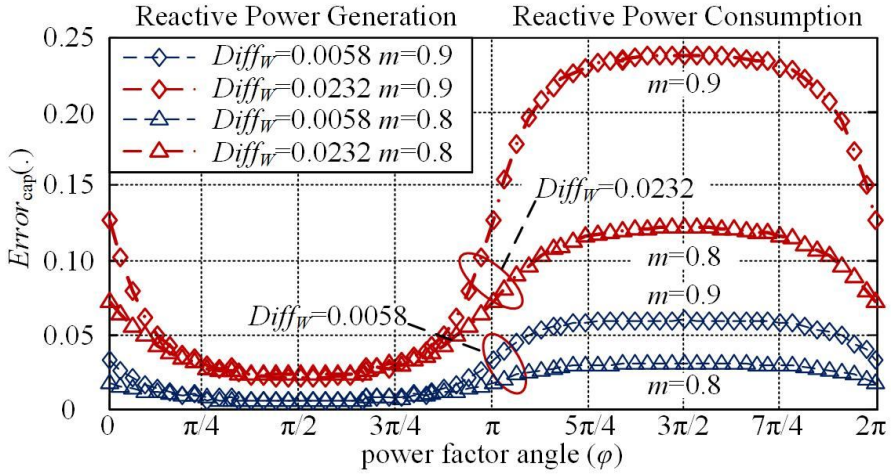

Figure 4.6: The relative error in $f_{cap}(m,\varphi,Diff_W,1)$ when neglects $Diff_W$

4.4.4 Capacitance demand function – $f_{\text{ripple}}(.)$

For the voltage ripple requirement, as the value of $f_{\text{ripple}}(.)$ is, to a large extend, inversely proportional to the allowable $V_{\text{ripplep.u.}}$, the product of $f_{\text{ripple}}(.)$ and $V_{\text{ripplep.u.}}$ is analyzed to reveal the impacts of other design variables and the OP on the capacitance demand. Figure 4.7 shows the values of $f_{\text{ripple}}(.)\times V_{\text{ripplep.u.}}$ with $V_{\text{ripplep.u.}}$=0.2, m=0.7, 0.8 and 0.9, and φ over 0 to 2π. Again, the marked lines correspond to $Diff_W$=0 while the dashed lines correspond to $Diff_W$=0.0058. Figure 4.7 shows that reactive power calls for higher C_{SM} demand. In active power conversion, the demand of C_{SM} drops with increasing m. The zoomed view shows that neglecting $Diff_W$ would also lead to a slight over-estimation of C_{SM}. The relative error is defined in (4.55) and shown in Figure 4.8.

$$Error_{\text{ripple\_}Diff_W}(m,\varphi,V_{\text{ripplep.u.}},Diff_W) = \frac{f_{\text{ripple}}(m,\varphi,V_{\text{ripplep.u.}},0)-f_{\text{ripple}}(m,\varphi,V_{\text{ripplep.u.}},Diff_W)}{f_{\text{ripple}}(m,\varphi,V_{\text{ripplep.u.}},Diff_W)}. \quad (4.55)$$

Figure 4.8 shows that the error introduced by neglecting $Diff_W$ is very small. Even if $Diff_W$ is as large as 0.0232, the error of the overestimation is still less than 1.3%. The error is almost the same for different m settings. For MMCs with smaller voltage ripples, $Diff_W$ will be smaller and the relative error will be much lower. In other words, even without the exact value of $Diff_W$, the marked lines in Figure 4.7 can be directly used in manual calculation. The capacitance to meet the voltage ripple requirement can be derived with very high accuracy.

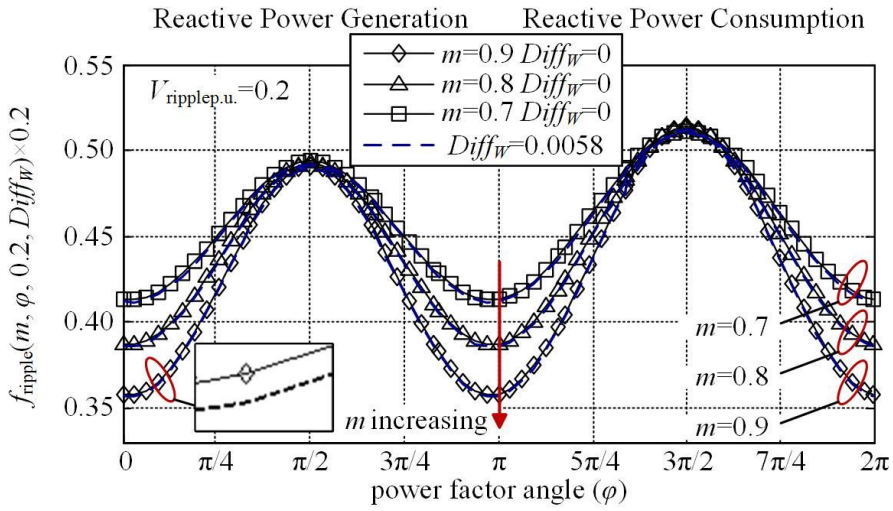

Figure 4.7: $f_{ripple}(m,\varphi,V_{ripplep.u.},Diff_W)\times V_{ripplep.u.}$ when $V_{ripplep.u.}$=0.2; $Diff_W$=0 and 0.0058

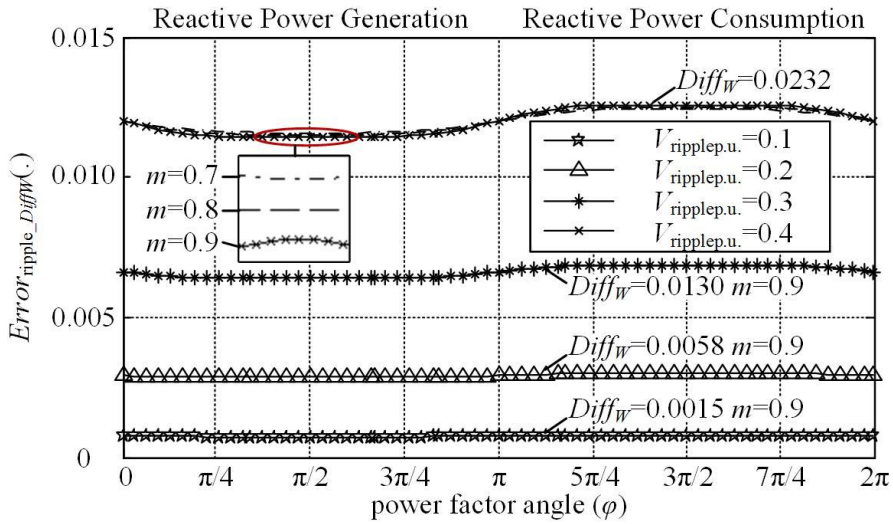

Figure 4.8: Relative error in $f_{ripple}(m,\varphi,V_{ripplep.u.},Diff_W)$ when neglects $Diff_W$

Figure 4.9 shows the values of $f_{ripple}(.)\times V_{ripplep.u.}$ with m=0.9 and different $V_{ripplep.u.}$ settings. The figure indicates that the value of $f_{ripple}(.)\times V_{ripplep.u.}$ is nearly constant at the same OP (m, φ). Hence, for the convenience of fast manual calculation, the design curves in Figure 4.7 ($V_{ripplep.u.}$=0.2) can be directly used even for different $V_{ripplep.u.}$. The difference between $f_{ripple}(.)\times V_{ripplep.u.}$ and $0.2f_{ripple}(m, \varphi, 0.2, 0)$, is included in (4.56) and shown in Figure 4.10.

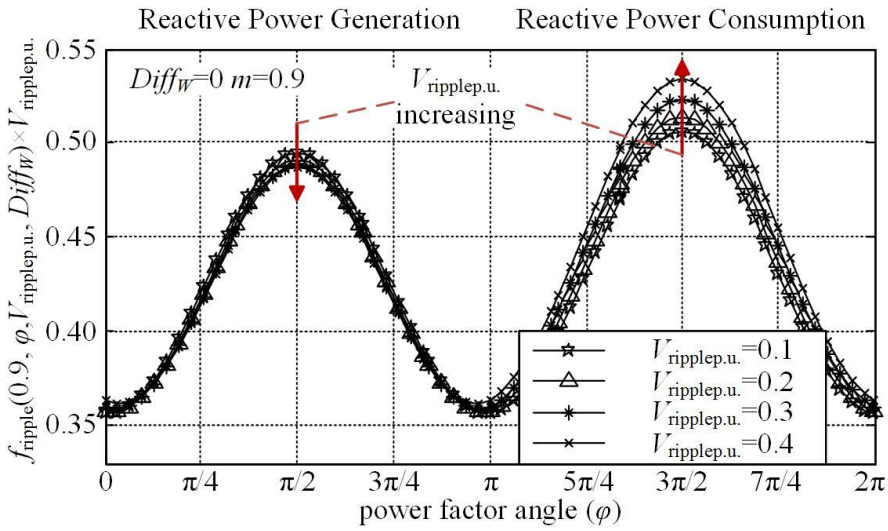

Figure 4.9: $f_{ripple}(m,\varphi,V_{ripplep.u.},Diff_W)\times V_{ripplep.u.}$ when m=0.9 and $Diff_W$=0

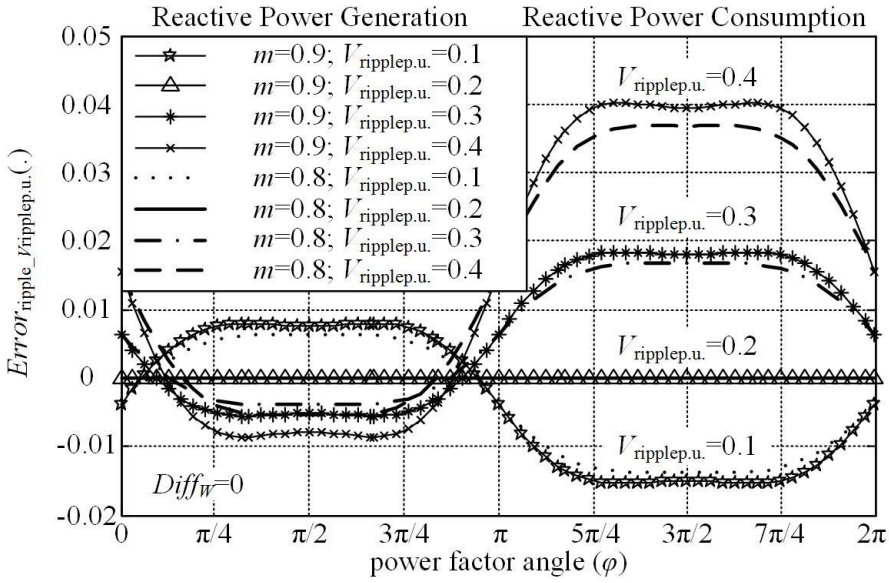

Figure 4.10: The relative error in the value of $f_{ripple}(m,\varphi,V_{ripplep.u.},0)\times V_{ripplep.u.}$ with respect to $f_{ripple}(m,\varphi,0.2,0)\times 0.2$ with different $V_{ripple.p.u.}$

$$Error_{ripple\_V_{ripplep.u.}}(m,\varphi,V_{ripplep.u.}) = \frac{V_{ripplep.u.}f_{ripple}(m,\varphi,V_{ripplep.u.},0)-0.2f_{ripple}(m,\varphi,0.2,0)}{0.2f_{ripple}(m,\varphi,0.2,0)} \quad (4.56)$$

where $Error_{ripple\_V_{ripplep.u.}}(.)$ is referred to as the relative error with respect to $0.2f_{ripple}(m,\varphi,0.2,0)$. In manual calculations, the required C_{SM} to satisfy the voltage ripple requirement can be

also derived as

$$C_{\mathrm{SM}} \geq \frac{\sqrt{2}NI_{\mathrm{s}}}{\omega K_{\mathrm{dc}}^{2}V_{\mathrm{dc}}} \times \frac{0.2 f_{\mathrm{ripple}}(m,\varphi,0.2,0)}{V_{\mathrm{ripplep.u.}}}\left(1+Error_{\mathrm{ripple\_}V_{\mathrm{ripplep.u.}}}\right) \tag{4.57}$$

4.4.5 Ripple current stress function – $f_{\mathrm{ICripple}}(.)$

Substituting (4.21) and (4.24) into the ripple current stress function $f_{\mathrm{ICripple}}(.)$ in (4.50b) gives

$$f_{I_{\mathrm{Cripple}}}(m,\varphi,V_{\mathrm{ripplep.u.}},Diff_{W},K_{\mathrm{dc}}) = \sqrt{\frac{1}{T}\int_{0}^{T}\frac{\frac{\sqrt{2}}{K_{\mathrm{dc}}}\frac{i_{\mathrm{arm}}(t)}{I_{\mathrm{s}}}\frac{df(m,\varphi,t)}{\omega dt}}{\sqrt{1+A_{e}f(m,\varphi,t)+Diff_{W}}}dt} \ . \tag{4.58}$$

As shown in (4.58), the ripple current stress function would depend on the system's operating point and the design variable K_{dc} as well as A_{e}. As shown in (4.41), if the actual voltage ripple equals $V_{\mathrm{ripplep.u.}}$, A_{e} would equal to the right side of (4.41) that only related with $V_{\mathrm{ripplep.u.}}$ and OP(m, φ). Based on that, Figure 4.11 shows how the value of $f_{\mathrm{ICripple}}(.)$ would change with varying OP(m, φ) and $V_{\mathrm{ripplep.u.}}$. In the calculation, $Diff_{W}$ is set to the values estimated in Chapter 4.4.1.

Figure 4.11 shows the ripple current stress function that equals the ratio between the rms ac output current and the rms capacitor ripple current for the example system as in Figure 4.1. The marked lines show that reactive power and lower modulation index m give rise to higher ripple current stress. The zoomed view indicates that $V_{\mathrm{ripplep.u.}}$ and $Diff_{W}$ only have limited effects on the ripple current stress. Changes between cases when $V_{\mathrm{ripplep.u.}}$ equals 0.1 and 0.4 are always less than 1%. It indicates that the ripple current stress is not sensitive to the capacitance.

Note that some OPs may not exist in practice, such as when m=0.9, $V_{\mathrm{ripplep.u.}}$=0.4 and φ=3π/2, as the voltage capability requirement will be violated. Hence, in actual designs, all capacitor demand functions shall be collaboratively used to ensure safe operation.

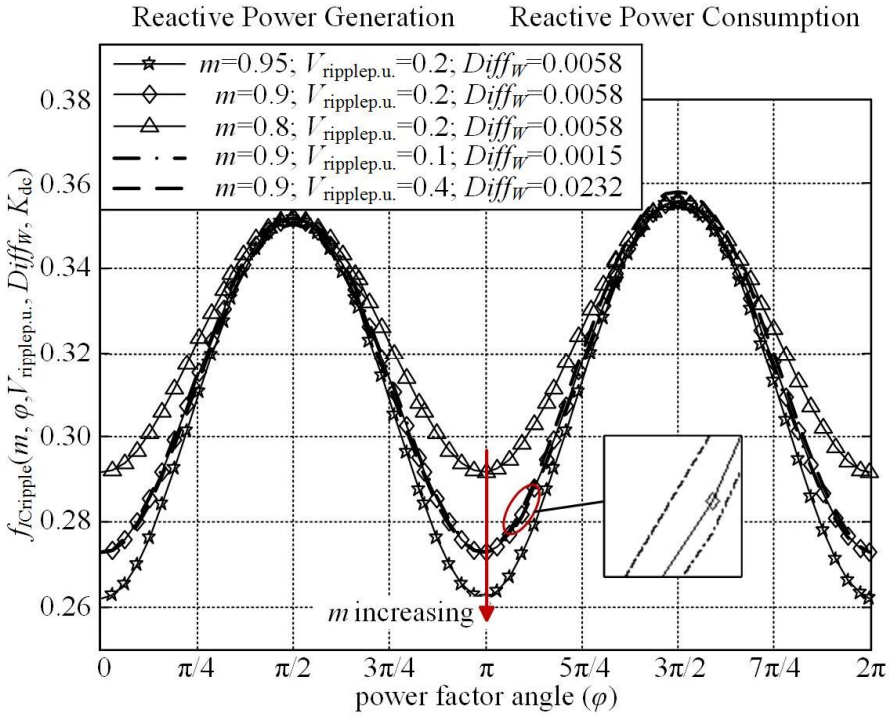

Figure 4.11: Ripple current stress function $f_{ICripple}(.)$

For the convenience of comparing the ripple current stress between different designs and selecting capacitors with suitable ripple current capability, the ripple current stress can be expressed in terms of A/mF, which can be derived by the ratio between the estimated rms ripple current in (4.50a) and the required SM capacitance given by (4.28a), (4.36), (4.37) or (4.42a). For instance, when the required C_{SM} is given by the voltage ripple requirement as in (4.42a) when $V_{ripplep.u.}$=0.2, the ripple current stress in A/mF ranges from 63 A/mF to 69 A/mF for V_{SMdc}=2 kV with varying OP(m, φ). For SM with other rated voltage, the derived values can be adjusted accordingly by scaling using the new rated voltage.

Note the capacitor ripple current capability provided in datasheets is usually for high frequency such as 10 kHz. Current with lower frequency meets a higher value of ESR, leading to degraded ripple current capability [86]. The worst case would be that when all the harmonics in the ripple current are treated as the lowest frequency i.e. the fundamental

frequency (50 or 60 Hz). The value 69 mA/μF multiplied by a penalty factor such as 1.3 suggests that the worst-case ripple current stress at 10 kHz would be around 90 A/mF.

4.5 Procedure of Capacitor Selection

4.5.1 Capacitance and rated voltage

Two quantities are determined first for the SM capacitor: the capacitance C_{SM} and the rated voltage. The C_{SM} must be large enough to limit the voltage ripple and satisfy the voltage capability requirement. The capacitor rated voltage must be higher than the maximum instantaneous voltage in operation. In order to show how the three voltage constraints will affect the C_{SM} selection, as an example, the values of $f_{excess}(.)$ and $f_{ripple}(.)$ are sketched and compared tot $f_{cap}(.)$ in Figure 4.12 for various m, $V_{excessp.u.}$, $V_{ripplep.u.}$, $Diff_W$ and φ over 0 to 2π.

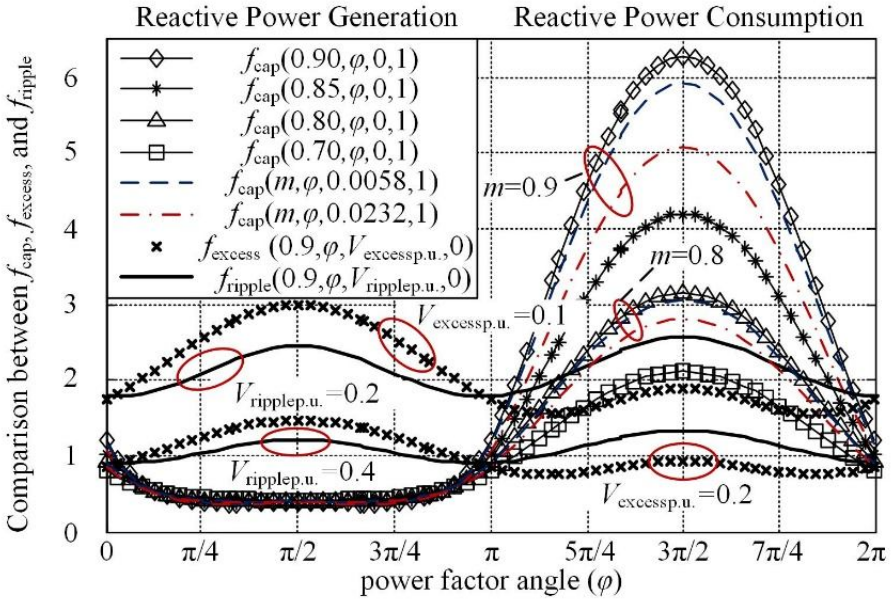

Figure 4.12: Comparison between $f_{cap}(.)$, $f_{excess}(.)$ and $f_{ripple}(.)$ for capacitor selection

The selection of C_{SM} starts with satisfying the voltage ripple requirement (4.42a) or (4.57). The chosen C_{SM} can then be adjusted to satisfy the other two requirements. For the

voltage capability requirement, when the converter generates reactive power, the chosen C_{SM} maybe already enough as in Figure 4.12. When the converter consumes reactive power, the C_{SM} may have to be updated to the value from (4.36). For the maximum voltage requirement, $V_{excessp.u.}$ is usually decided by the voltage limits of other devices in the SM such as power switches. The chosen C_{SM} given by $f_{ripple}(.)$ in (4.42a) [or (4.57)] or $f_{cap}(.)$ in (4.36) must be compared with the value given by (4.28a) and updated to the higher. Generally, the voltage limits of other devices are enough to withstand the peak capacitor voltage for applications with small voltage ripples, such as HVDC converters. The required capacitance to satisfy $V_{excessp.u.}$ may be much smaller than the value given by the other two voltage constraints. I.e., in normal operation $V_{excessp.u.}$ will never be reached. In order to avoid oversized capacitor, one way to select the capacitor rated voltage V_{Crated} is according to the maximum voltage using (4.22a) and (4.23a) as

$$V_{SMmax} = \frac{K_{dc}V_{dc}}{N}\sqrt{1 + A_e f_{max}(m,\varphi) + Diff_W} \tag{4.59}$$

where A_e can be derived by (4.24) using C_{SM} derived for the voltage ripple or the voltage capability requirement as

$$A_e = \frac{2\sqrt{2}NI_s}{\omega C_{SM\_f\,ripple(cap)} K_{dc}^2 V_{dc}}. \tag{4.60}$$

Hence, the capacitor rated voltage V_{Crated} can be derived by:

$$V_{Crated} \geq \frac{K_{dc}V_{dc}}{N}\sqrt{1 + \frac{2\sqrt{2}NI_s f_{max}(m,\varphi)}{\omega C_{SM\_f\,ripple(cap)} K_{dc}^2 V_{dc}} + Diff_W}\ . \tag{4.61}$$

In order to facilitate manual calculation, Table I lists a few values of $f_{cap}(.)$, $f_{ripple}(.)$ and $f_{max}(.)$ for future references.

φ	P>0	$3\pi/2$	-0.5	-0.3	-0.1	0	0.1	0.3	0.5	$\pi/2$
	P<0		3.64	3.44	3.24	π	3.04	2.84	2.64	
	Q	Reactive Power Consumption				Q=0	Reactive Power Generation			
m 0.95	f_{cap}	12.53	6.33	4.27	2.37	1.64	1.14	0.65	0.46	0.38
	f_{ripple}	2.58	0.385	1.80	1.73	1.71	1.71	1.75	1.85	2.46
	f_{max}	0.191	0.149	0.152	0.162	0.170	0.180	0.202	0.226	0.309
m 0.9	f_{cap}	6.28	3.33	2.39	1.54	1.21	0.94	0.62	0.47	0.39
	f_{ripple}	2.57	1.99	1.87	1.81	1.79	1.79	1.83	1.92	2.46
	f_{max}	0.194	0.158	0.161	0.171	0.178	0.187	0.207	0.229	0.306
m 0.8	f_{cap}	3.16	1.84	1.43	1.07	0.92	0.79	0.60	0.49	0.40
	f_{ripple}	2.57	2.10	2.00	1.95	1.94	1.94	1.97	2.04	2.46
	f_{max}	0.200	0.175	0.178	0.186	0.192	0.200	0.216	0.235	0.300

(K_{dc}=1.0, $Diff_W$=0, $V_{ripplep.u.}$=0.2 in calculations)

Table 4.1: Capacitance reference values

4.5.2 Summary of capacitor selection procedure

The procedure for the capacitor selection is summarized in Figure.13. First, basic system design specifications for each OP (m, φ) are required. They are the dc-link voltage (V_{dc}), constant K_{dc}, number of SMs in each arm (N), SM rated dc voltage (V_{SMdc}), permitted voltage excess ($V_{excessp.u.}$), permitted voltage ripple ($V_{ripplep.u.}$), ac side fundamental angular frequency (ω) and rms ac side current (I_s). Note that ω is usually constant for grid applications. V_{dc}, V_{SMdc}(K_{dc}) and I_s may vary from OP to OP. For different OPs, the capacitance and rated voltage are decided separately. Then, adjust the modulation index and power factor angle according to (4.52b) and (4.52d) to include arm inductor effect. After that, select the C_{SM} according to (4.42a) or (4.57), (4.36) or (4.37), and (4.28a) to satisfy the voltage ripple, voltage capability and the maximum voltage requirements. If the maximum voltage requirement gives the highest C_{SM}, the capacitor rated voltage V_{Crated} can be chosen according to $V_{excessp.u.}$. Otherwise, it shall be derived using (4.61). At the end, (4.48) and (4.58) can be used to check the ripple current stress and choose the capacitor accordingly.

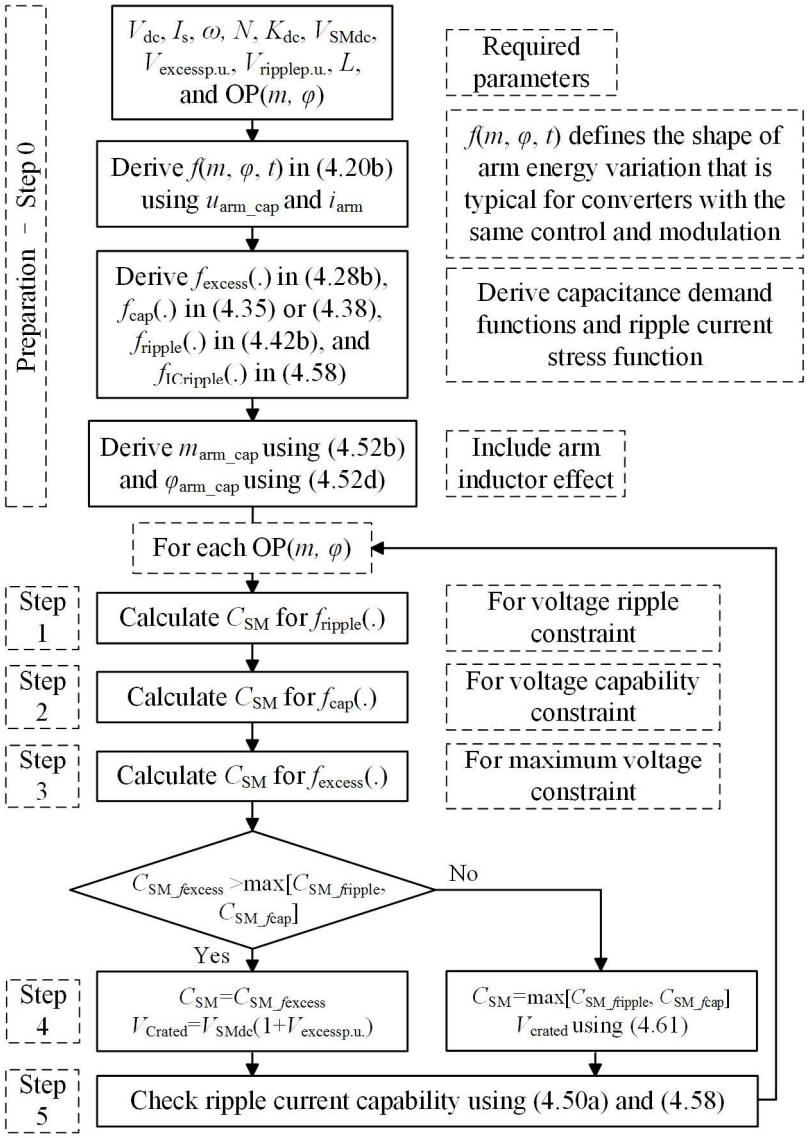

Figure 4.13: Flow chart for capacitor selection

4.6 Design Examples and Simulation Verification

In order to illustrate the validity of the proposed method, a set of design examples for grid-connected MMCs is presented. The converter model is built in MATLAB/Simulink, which is connected to a three-phase, 22 kV (line-to-line, rms), 50 Hz ac grid without a coupling transformer. The dc bus voltage is 40 kV pole-to-pole. There are 20 SMs in each arm and the arm inductor is 16.2 mH. The system specifications are listed in Table 4.2. Two design

examples are given: 1) the converter is to invert 19.1 MW active power at PF = 0.95 leading to 0.95 lagging, and 2) the converter works as a STATCOM to generate or absorb 20.11 MVAr reactive power with respect to the ac grid. The active power P_{ac} and reactive power Q_{ac} are measured at the converter output point as shown in Figure 4.1.

Item	Value
Grid voltage	22 kV, line-line rms, 50Hz
Rated voltage at output point	18 kV, phase peak
Rated capacity	20.11 MVA
Arm inductance	16.2 mH
Number of SMs	20 per arm
dc bus voltage V_{dc}	40 kV (pole-to-pole)
SM rated dc voltage	2 kV (K_{dc}=1.0)
Example 1: Inverting 19.1 MW at PF=0.95 leading to 0.95 lagging	
Example 2: STATCOM: ±20.11 MVAr reactive power (Q)	

Table 4.2: Specifictions of the design examples

4.6.1 Design example 1: inverter

In the first example, the converter is required to be capable of inverting 19.1 MW active power at PF=0.95 leading to 0.95 lagging. The short circuit ratio (SCR) of the ac grid is set to 5 to emulate a relatively weak connection point. The SM dc voltage ripple is limited to 0.2p.u. peak-to-peak or 400 V for the entire operation region. Table 4.3 lists the ac side line current I_s, power factor angle φ and modulation index m for different possible OPs. The corresponding required C_{SM} is then derived using (4.36) and (4.42a) for the SM voltage capability and voltage ripple requirements respectively. $Diff_W$ in the calculation is estimated by the method offered in Chapter 4.4.1.

PF	0.95	0.988	1.0	0.988	0.95	0.944	0.922
	Lagging Q generation			Leading Q consumption			
S (MVA)	20.11	19.33	19.1	19.33	20.11	19.06	16.3
P (MW)	19.1					18	15
Q (MVAr)	6.28	3	0	-3	-6.28		
I_s (A)	497	492	500	523	565	536	458
φ	0.32	0.16	0	-0.16	-0.32	-0.34	-0.40
φ_{arm}	0.40	0.25	0.1	-0.05	-0.20	-0.22	-0.30
m	0.95	0.93	0.9	0.87	0.84	0.84	0.84
m_{arm}	0.99	0.95	0.91	0.87	0.82	0.82	0.81
$C_{SM\_f_{cap}}$ (mF)	0.585	0.794	1.068	1.354	1.613	1.602	1.527
$C_{SM\_f_{ripple}}$ (mF)	1.946	1.925	2.000	2.168	2.471	2.365	2.044

Table 4.3: Design parameters of design example 1

Table 4.3 shows that the converter output voltage will drop with the decrease of lagging reactive power (Q) generation or the increase of Q consumption. This leads to increasing ac output current to keep the same active power. As shown in Figure 4.5, the C_{SM} demand for the SM voltage capability requirement (f_{cap}) will increase with increasing Q consumption but it will drop with decreasing m. The calculations show that the highest C_{SM} for f_{cap} is met at the highest Q consumption point with the rated active power (P), which indicates that the increase of Q consumption as well as higher I_s has more significant effect on the C_{SM} rather than the decreasing m in this case. According to Figure 4.7 and (4.42), the decrease of m, increase of Q consumption or increase of I_s calls for larger C_{SM} to limit the voltage ripple. This is why the highest C_{SM} demand for the voltage ripple requirement is also met at the highest Q consumption point. As the active power decreases, the C_{SM} demands for both requirements drop due to the decreasing I_s. Hence, the highest C_{SM}=2.471 mF in the entire operating region is the choice of the system. Once the capacitance is decided, (4.60) is used to find the maximum capacitor voltage, which is 2188 V at the highest Q generation point. Since this voltage is derived assuming that all SM capacitor voltages in one arm equal to their average value instantaneously, in order to allow for the deviation caused by the limited

switching frequency for each SM, the rated capacitor voltage must be chosen slightly higher than this. The maximum capacitor ripple current stress (rms) in the entire operating region is estimated to be 165.4 A at the highest Q consumption point using Figure 4.11.

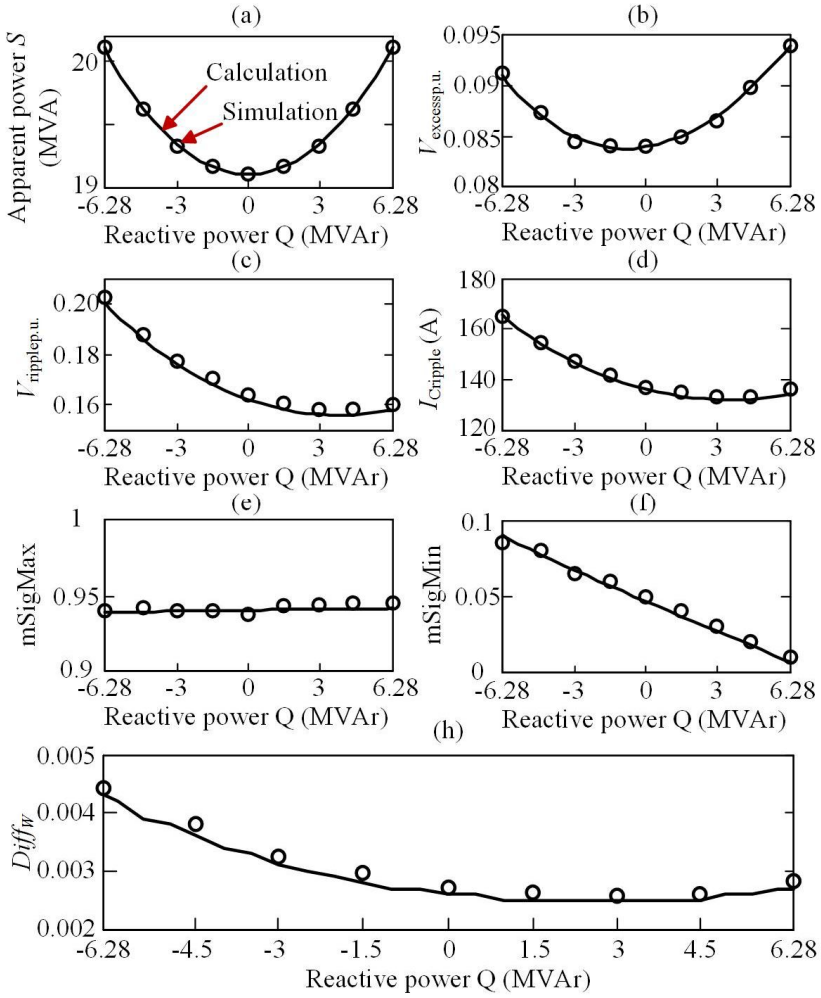

Figure 4.14: Calculation and simulation results of design example 1

Figure 4.14 shows the calculation (solid line) and simulation (circle) results of the design example 1. As the reactive power changes from -6.28 MVAr (consuming) to 6.28 MVAr (generating), with peak active power, the apparent power of the MMC varies between 19.1 MVA and 20.11 MVA [Figure 4.14(a)]. In this range, simulation results of the voltage excess $V_{excessp.u.}$ [Figure 4.14(b)], voltage ripple $V_{ripplep.u.}$ [Figure 4.14(c)] and capacitor ripple

current (rms) I_{Cripple} well agree with the analytical calculations. The slight increase of the voltage ripple in the simulation is caused by 1) the 3rd order harmonic in the arm voltage brought by the harmonic circulating current suppression controller, and 2) other high order harmonics introduced by switching the SMs. The error between the simulation and calculation is always less than 2%. Figure 4.14(e) and (f) are the maximum and minimum values of the modulation signal mSig(t) of one arm, which is defined as

$$\text{mSig}(t) = \frac{u_{\text{arm}}(t)}{NV_{\text{SMdc}}\left[1 + v_{\sim\text{p.u.}}(t)\right]}. \tag{4.62}$$

$N\times$mSig(t) (the closest integer) equals the number of SMs to be inserted in the next control cycle. To ensure safe operation, mSig(t) must be within 0 to 1. Again, the simulation results well agree with the calculations.

Fig.14(h) shows that the estimation of $Diff_W$ by substituting (4.14) (with $Diff_W$=0) into (4.13) gives very good accuracy. The reason that the calculations are always slightly less than the simulation results is because of the neglected $Diff_W$ in (4.13).

4.6.2 Design example 2: STATCOM

In this example, the converter works as a STATCOM to generate or consume 20.11 MVAr reactive power with respect to the ac grid. The SCR of the ac grid is set to 20 in order to have similar converter output voltages and currents as in the design example 1 to compare the design considerations. Table 4.4 lists the corresponding design parameters. In the first group, the permitted SM capacitor voltage ripple is set to 0.2p.u. Even though the SM voltage capability requirement calls for higher C_{SM} when the converter consumes lagging reactive power, C_{SM} derived from (4.36) is still smaller than that derived from (4.42a) to satisfy the voltage ripple requirement. This can be explained by the much lower m_{arm} when Q equals -20.11 MVAr. The C_{SM} demands for other OPs with reduced capacity are all less than

3.34 mF due to lower ac current. Hence, C_{SM} = 3.34 mF is selected for the system.

In order to illustrate the effect of Q consumption on the C_{SM} demand for the SM voltage capability requirement, the second group in Table 4.4 shows the design parameters when the permitted voltage ripple is extended to 0.3p.u. In this case, at the highest Q consumption point, C_{SM} given by (4.36) exceeds the value given by (4.42a). Hence, C_{SM}=2.81 mF is selected for this system.

PF	0			0	
$V_{ripplep.u.}$	0.2			0.3	
S (MVA)	20.11			20.11	
P (MW)	0			0	
Q (MVAr)	20.11	-20.11		20.11	-20.11
I_s (A)	523	582		523	582
φ	1.571	-1.571		1.571	-1.571
φ_{arm}	1.571	-1.571		1.571	-1.571
m	0.906	0.814		0.906	0.814
m_{arm}	1	0.71		1	0.71
$C_{SM\_f_{cap}}$ (mF)	0.440	2.810		0.440	2.810
$C_{SM\_f_{ripple}}$ (mF)	2.880	3.340		1.910	2.262

Table 4.4: Design parameters of design example 2

Table 4.5 shows that the simulation results of the design example 2 agree well with the calculations in all aspects. Note that in the system with larger allowable voltage ripple, at the highest Q consumption point, the maximum modulation signal mSigmax equals 1, indicating that the SM capacitor voltages in converter arms are just enough for arm voltage output. Since C_{SM} in this case is chosen by the SM voltage capability requirement, which is larger than the value required by the voltage ripple requirement, the actual voltage ripple is smaller than the design specification.

Results	Cal.	Sim.	Cal.	Sim.		Cal.	Sim.	Cal.	Sim.
S (MVA)	20.11					20.11			
P (MW)	0					0			
Q (MVAr)	20.11		-20.11			20.11		-20.11	
$V_{excessp.u.}$	0.107	0.107	0.080	0.080		0.129	0.128	0.098	0.097
$V_{ripplep.u.}$	0.172	0.173	0.200	0.201		0.203	0.207	0.241	0.244
$I_{Cripple}$ (A)	184	184	207	208		184	185	207	209
mSigmax	0.904	0.90	0.906	0.91		0.886	0.9	1.000	1.00
mSigmin	0	0	0.007	0.01		0	0	0.133	0.14
$Diff_W$	0.004	0.004	0.0032	0.0033		0.0057	0.0058	0.0073	0.0076

Table 4.5: Calculation and simulation results of design example 2

4.7 Experimental Verification

The 21-level MMC system is scaled down to 35 kVA with 4 kV pole-to-pole dc and 2.2 kV (line-to-line) ac side voltages in order to verify the proposed capacitor dimensioning method through experiment. The system is designed to rectify or invert 35 kW active power (PF=1). A prototype HB-SM with 200 V (K_{dc}=1) rated voltage is built and tested using the model assisted SM testing scheme proposed in Chapter 6. Design specifications are concluded in Table 4.6.

Experiment example: Inverting or rectifying 35 kW (PF=1)	
Item	**Value**
Dc bus voltage V_{dc}	4 kV (pole-to-pole)
Grid voltage	2.2 kV, line-to-line rms, 50Hz
Rated voltage at output point V_s	1.273 kV, phase rms
Modulation index m	0.9
Rated capacity	35 kVA
Power factor angle	0/π
Rated line current I_s	9.17 A
Arm inductance	88 mH
Number of SMs	20 per arm
SM rated dc voltage	200 V (K_{dc}=1.0)
$V_{ripplep.u.}$	0.2 peak-to-peak

Table 4.6: Design parameters for experiment

In order to invert or rectify 35 kW active power when PF=1 and m=0.9, the rated ac side line current I_s equals 9.17 A_{rms}. The actual modulation index m_{arm} and power factor angle φ_{arm} are m_{arm}=0.9, and φ_{arm}=0.1 for inverting or φ_{arm}=3.04 for rectifying according to (4.52b) and (4.52d). If the p.u. permitted voltage ripple is set to 0.2 peak-to-peak, according to Table 4.1, f_{cap}=0.94 and f_{ripple}=1.79. The C_{SM} is then selected according to the voltage ripple requirement, which is 370 μF according to (4.42a). The maximum capacitor voltage is estimated to be 220.3 V using (4.61). According to (4.58) or Figure 4.11, $f_{ICripple}$ equals 0.273, and the capacitor ripple current (rms) is estimated to be 2.5 A, taken as 50 Hz.

Figure 4.15 gives a picture of the prototype HB-SM under test. The SM has two IKW30N60T IGBT/diode modules as the upper and lower switches. The capacitor used in the experiment is from EPCOS with 373 μF capacitance. Details of the test platform can be found in Chapter 6.

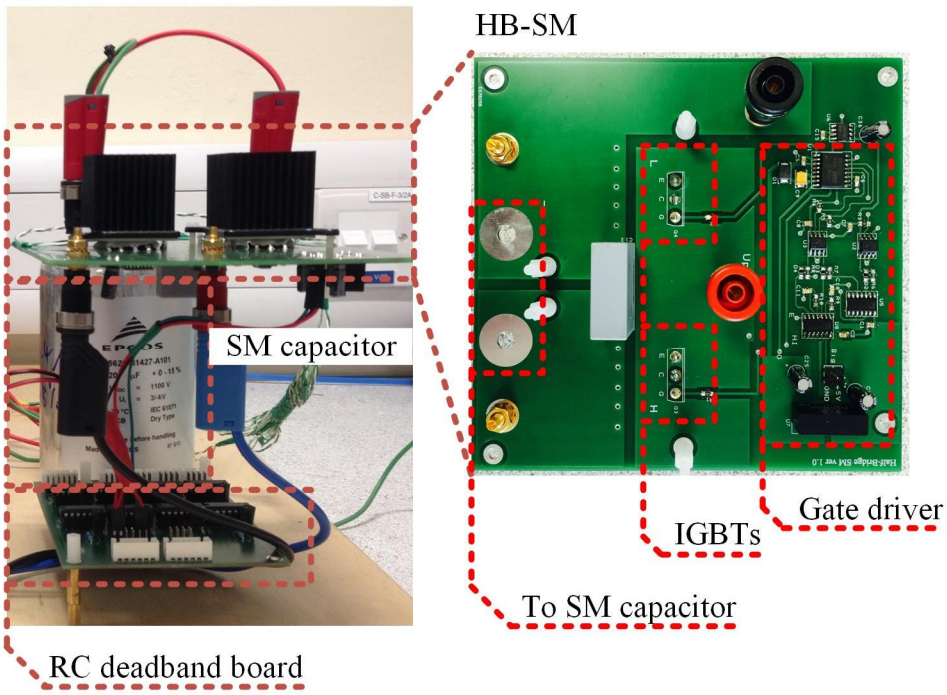

Figure 4.15: Picture of the prototype HB-SM

Figure 4.16 and 4.17 show the experiment waveforms of the tested SM for rectifying and inverting respectively. The top green curve in both figures is the SM capacitor voltage, which verifies the design accuracy for both the maximum voltage and voltage ripple. The small deviations are due to the limited SM switching frequency. The rms value of the SM capacitor current in the case of rectifying is measured to be 2.5 A and in the case of inverting is 2.49 A. Both measurements agree with the estimated 2.5 A_{rms}.

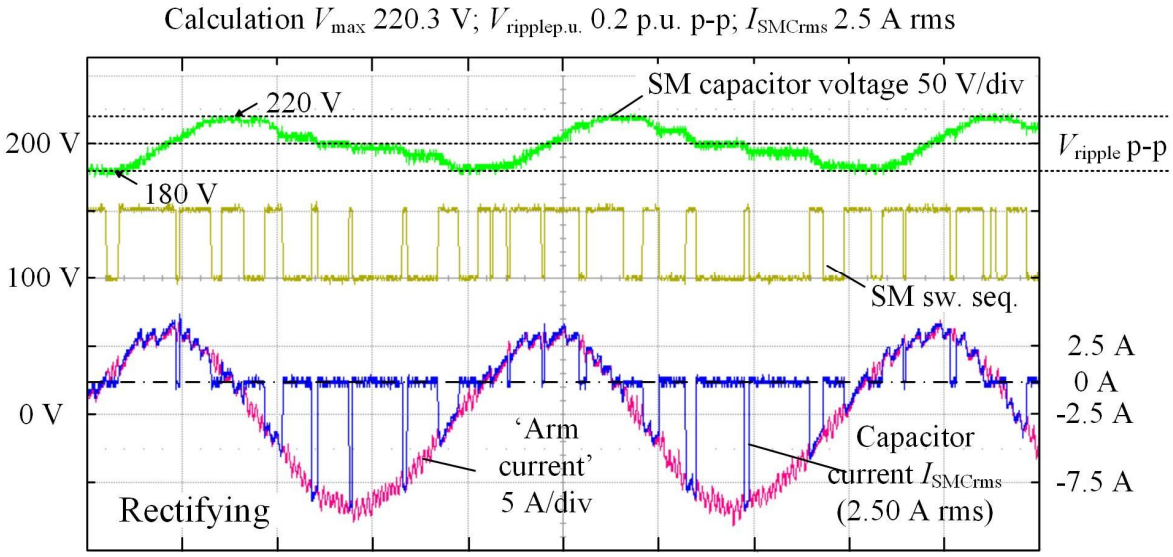

Figure 4.16: Experiment results for rectifying: (green) SM capacitor voltage, 50 V/div, -2 div offset; (yellow) SM switching sequence (i.e. upper IGBT switching sequence); (red) 'arm current', 5 A/div, -1.5 div offset; (blue) SM capacitor current, 5 A/div, -1.5 div offset; horizontal axis 5 ms/div.

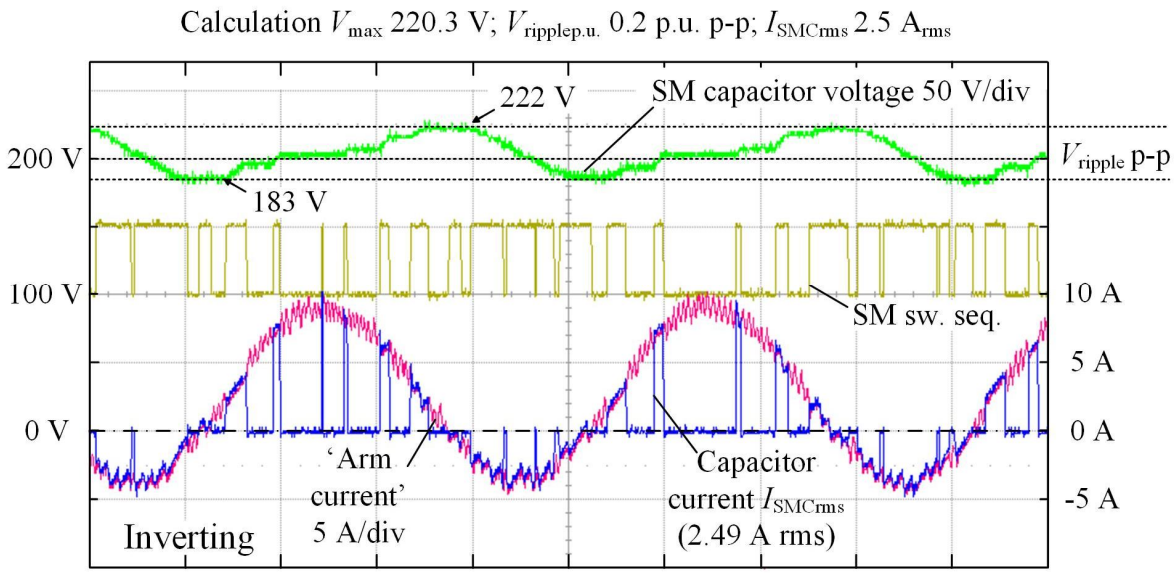

Figure 4.17: Experiment results for inverting: (green) SM capacitor voltage, 50 V/div, -2 div offset; (yellow) SM switching sequence (i.e. upper IGBT switching sequence); (red) 'arm current', 5 A/div, -2 div offset; (blue) SM capacitor current, 5 A/div, -2 div offset; horizontal axis 5 ms/div.

4.8 Summary

This chapter proposes a new approach to derive the requirements on the capacitor for MMC SMs based on the estimation of the capacitor voltage ripple. According to the MPPF capacitor's ageing mechanisms and the operational characteristics of the MMC, the capacitor selection procedure concurrently considers three voltage requirements: the maximum capacitor voltage, the voltage ripple, and the SM voltage capability to select the required capacitor capacitance and rated voltage. In addition, a quick way to estimate the capacitor ripple current stress is also presented. The maximum possible ripple current stress (rms) is found to be 90 A/mF for SMs with 2 kV rated voltage and $V_{ripplep.u.}$=0.2.

The effects of the MMC's operation mode and different design parameters ($V_{\text{excessp.u.}}$ and $V_{\text{ripplep.u.}}$) on the demand of SM capacitance are also analyzed. It gives a comprehensive understanding of how the SM capacitance will limit the operation region of the converter. Generic curves and tables are presented to facilitate engineering design with good accuracy. Simulation and experimental results verify the validity and demonstrate the application of the proposed method. It is hoped that the study and the results would be useful to engineers designing and optimizing MMC converter systems.

5 EVALUATION OF OFFSHORE 50/3 HZ AC POWER TRANSMISSION AND BACK-TO-BACK MMC FOR FREQUENCY CONVERSION

The United Kingdom has been devoting itself to the development of offshore wind. Not only will the size of wind farms increase to a few hundreds of MW, the distance to shore will also be longer than 100 km. 50 Hz ac is commonly considered as unsuitable for offshore transmission due to the massive charging current [4]. Quite a few research studies have been published evaluating the use of dc power transmission for offshore wind integration with either point-to-point or multiterminal configuration [25, 104, 105]. Problems are revealed as an increasing number of HVDC projects are implemented.

As a spin-off of the thesis, this chapter will look into an alternative power transmission technology – 50/3 Hz ac, and evaluate the use of back-to-back (B2B) MMC for frequency conversion. A comparison between three transmission technologies: dc, 50 Hz ac and 50/3 Hz ac in terms of reliability and transmission losses will be presented first. After that a brief review on frequency converters will be given. Then, a high-level design of a B2B MMC system is presented especially focusing on the capacitor selection using the method presented in Chapter 4. System performance is briefly evaluated using computer simulation both in steady state and under fault conditions.

5.1 Comparison: dc, 50 Hz ac and 50/3 Hz ac

5.1.1 Overview

Figure 5.1 gives a typical configuration of an offshore point-to-point HVDC transmission system. HVDC has been commonly regarded as the best option for middle- to long-distance offshore power transmission. However, a few years of operational experience made some industries think twice before putting new offshore HVDC projects on the agenda.

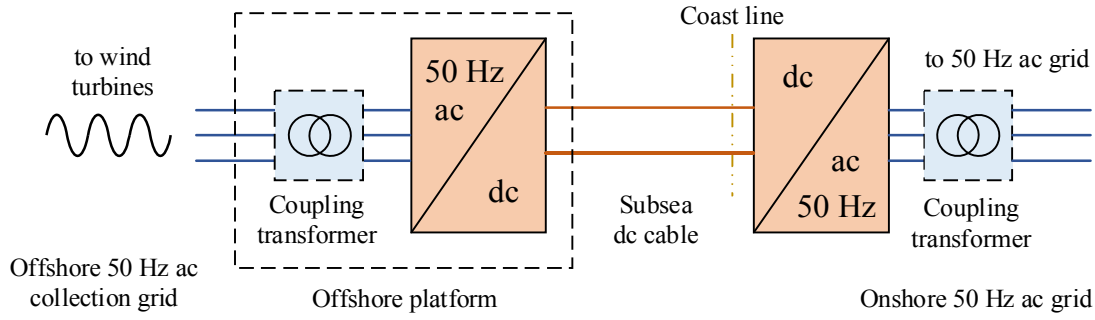

Figure 5.1: Typical configuration of an offshore point-to-point HVDC system

With advantages such as low cost, less maintenance demand, environmental friendliness and no fire hazards, the cross-linked polyethylene (XLPE) insulated cable took the place of the oil-filled cable in offshore or underground power transmission [106]. Researchers found

that when a dc voltage is applied to the XLPE cable, the prominent space charge accumulation that increases with the applied voltage would lead to insulation breakdown. As a result, lifetime of the dc XLPE cables is reported as being much shorter than estimated and thus the voltage level for the deployed systems is generally limited [107, 108].

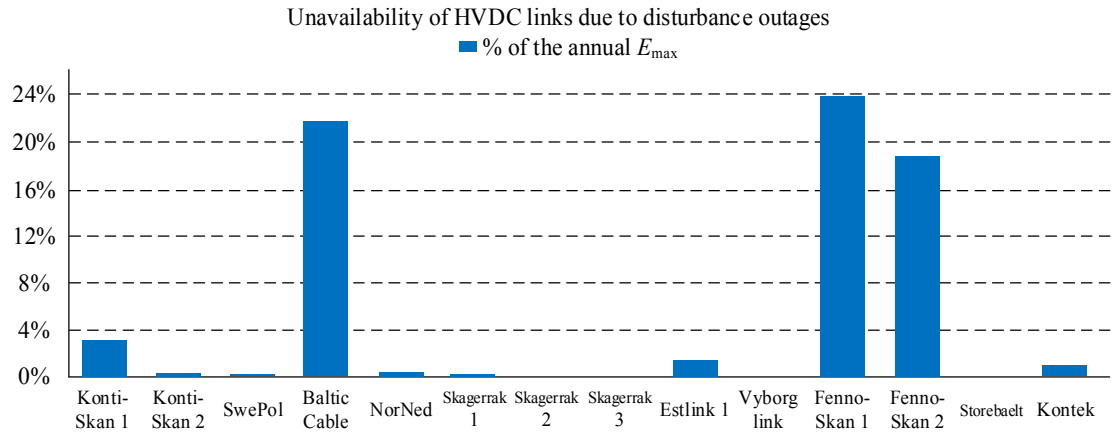

Figure 5.2: Percentage distribution of unavailability due to disturbance outages of HVDC projects in the Nordic grid in year 2012 [109]

Another problem with the HVDC transmission is the difficultly of building a multi-terminal HVDC grid due to the lack of reliable and economically achievable dc circuit breakers and dc/dc transformers [110]. Figure 5.2 shows the unavailability over annual E_{max} due to outages of HVDC projects in the Nordic grid in year 2012 [109]. E_{max} is the maximum energy that can be transmitted through an HVDC link without any outages or limitations. As shown in the figure, the unavailability rates for three projects were much higher than the rest. Two of them were caused by cable faults. Due to the complexity and difficulty related to fault diagnosis, transportation and repair work for those cables, the duration of such outages usually lasts several weeks. During such outages, the transmission link may only be capable of operating at half the rated capacity or even get totally shutdown. As a result, the energy from the interconnected wind farms will be wasted. If multiterminal

configuration is available, such losses could have been reduced.

50 Hz ac power transmissions have been commonly used to connect small-scale offshore wind farms that are close to shore. Multiterminal offshore grid is achievable with mature ac circuit breakers and transformers readily available. The major problem is that due to the massive capacitive charging current, the transmission distance of 50 Hz ac is usually below 50 km [5].

If the operating frequency reduces to 50/3 Hz, the transmission distance can be more than tripled. Figure 5.3 gives two possible topologies for offshore 50/3 Hz ac transmission. For topology 1, the entire offshore grid operates at 50/3 Hz and the frequency converter is only onshore. For topology 2, voltages in the offshore collection grid are converted back to 50 Hz using a frequency converter installed on the offshore platform. The topology 2 is a plug-and-play option that no modification is required for the interconnected wind turbines and other equipment. However, the offshore converter indicates much higher installation and maintenance costs. The major advantage of topology 1 is its smaller, lighter and much cheaper offshore platform. The converter station is only onshore leading to largely reduced control complexity and maintenance costs. However, the rest of the offshore collection grid must operate at 50/3 Hz. Besides, the reduced operating frequency will lead to larger and heavier transformers. Our research found that the increment in both size and weight will be more than 70% [111].

Note when the operating frequency drops down to 50/3 Hz, it would take up to 3 times of the time for the current to cross zero in the case of a short circuit fault. In addition, in a 50/3 Hz network as shown in Figure 5.3, each terminal is a fully controlled frequency converter that the fault current would be as low as twice the rated value. To maintain the arc generated by the small fault current for much longer time becomes a challenge. Otherwise, the arc

would extinguish before the natural current zero crossing, leading to very high *di*/*dt* and overvoltage at the inductive load as well as the circuit breaker, which would cause damages. This phenomenon is usually referred to as the *current chopping*. To solve the problem, manufactures tend to cut the nozzle of the circuit breaker shorter in order to keep the insulation gas flowing at a lower speed to maintain the arc. In other words, in order to build a 50/3 Hz multiterminal network, the 50 Hz circuit breakers are still effective with minor modifications if necessary. Nearly a century of operating experience with low frequency electrification railway systems such as those utilized in Sweden, Germany or eastern US could help with the utilization of the 50/3 Hz transmission in offshore renewable power integration [112].

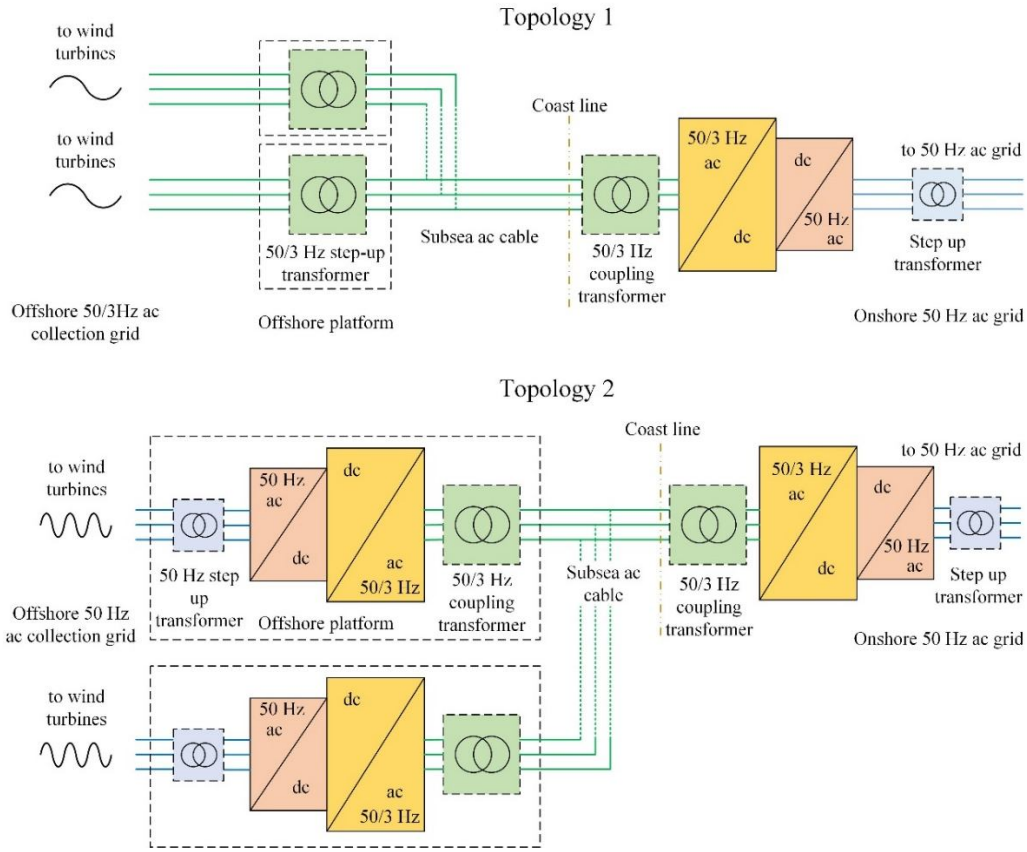

Figure 5.3: Two topologies for offshore 50/3 Hz ac power transmission

5.1.2 Simulation of the three transmission technologies

A group of simulations aiming at comparing the transmission capability and efficiency of the three transmission technologies has been performed. Simulation models are shown in Figure 5.4. Both 50 Hz and 50/3 Hz ac systems use a fixed three-phase voltage source with a 0.1 mH coupling inductor at the sending end to emulate the interconnected wind farms. The voltage is fixed at 132 kV line-to-line (rms). The receiving end uses a controllable voltage source to absorb 250 MW active power from the network at unity power factor. A 110 MVAr shunt reactive power compensation can be connected to the receiving end of the 50 Hz ac system through a manual switch.

The dc system uses only two cables, one for the positive pole and the other for the negative. The sending end uses two fixed dc voltage sources each rated at 107.7 kV equaling to the peak phase voltage in the ac system. The load is a resistor with 176.3 Ω resistance, absorbing 250 MW power from the network.

Cables in all systems use the same type of single core XLPE insulated cable. Note that the effects of prominent space charge accumulation when high dc voltage is applied are not considered. The dc pole-to-neutral voltage is set to the peak phase voltage (107.7 kV) in the ac systems. The total transmission distance is 200 km, which is modelled by four identical π-sections, each representing a 50 km section. Detailed cable parameters are listed in Table 5.1.

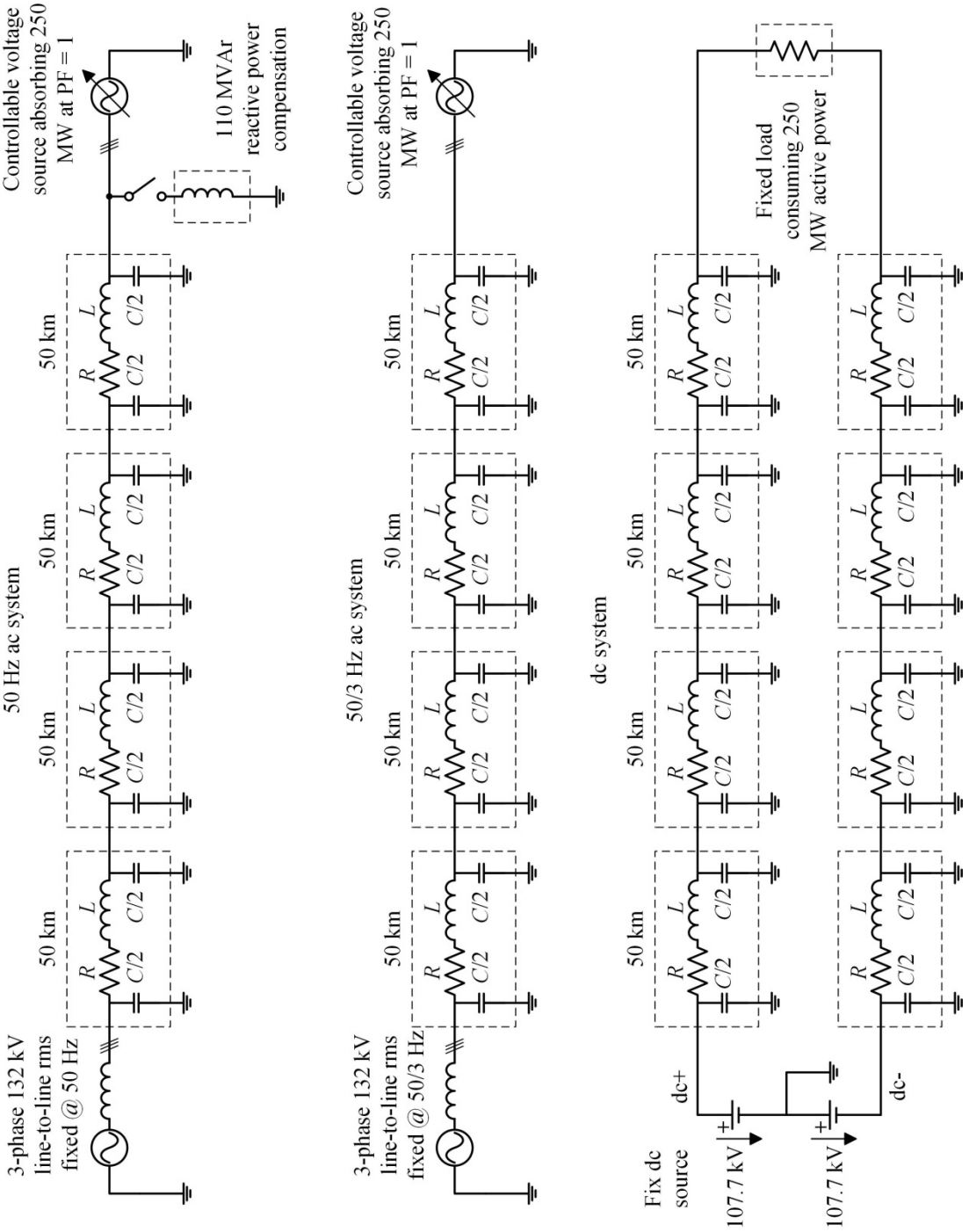

Figure 5.4: Simulation models of the three transmission technologies: top to bottom, 50 Hz ac, 50/3 Hz ac and dc systems

Item	50 Hz ac	50/3 Hz ac	dc
Voltage (kV)	132 (line-to-line, rms)		107.7
Type	Single core XLPE insulated, 200 km		
Conductor	Copper		
Rated current (A)	1300		
R at 90℃ (Ω/km)	0.014	0.012	0.0115
L trefoil (mH/km)	0.325		
C (μF/km)	0.29		

Table 5.1: Cable parameters

Simulation results are concluded in Table 5.2. With no compensation, reactive power of the 50 Hz ac is 290 MVAr at the sending end. Current at this point (1700 A rms) largely exceeds the rated 1300 A, rms. Voltage at the receiving end equals 87.2 kV (phase-to-neutral rms), which exceeds the ±10% limit as required in the UK Grid Code (CC, 2014). In order to keep both the current and voltage within the limits, a 110 MVAr shunt reactor is connected at the receiving end. Simulation results of the 50 Hz ac power transmission with 110 MVAr reactive power compensation are also shown in Table 5.2. In such a case, the maximum current in the cable drops below the limit and the voltage is always within the limit as well. For the 50/3 Hz ac system, no reactive power compensation is required. The maximum current is only 1184 A rms and the voltage difference between the two ends is less than 2%. For the dc system, both the current and voltage are within the limits.

Table 5.2 also lists I^2R losses of the three transmission systems. In the 50 Hz ac system with compensation, the total Ohmic loss is 11.1 MW or 4.4% of the rated 250 MW power. In the 50/3 Hz ac system, the loss reduces to 9.3 MW or 3.7% and in the dc system, the loss is only 6.5 MW or 2.6%. The low loss in the dc system is due to the reduced number of cables and lower dc resistance. The loss in the 50/3 Hz ac is 85% of that in the 50 Hz ac largely due to the reduced skin effect and hence lower cable resistance. Also, the current stress is lower in the 50/3 Hz ac due to less charging current.

Item		Sending end	50 km	100 km	150 km	200 km before compens-ation	Receiv-ing end	Loss I^2R (MW)
50 Hz no compens-ation	**P** (MW)	263.4	258.2	254.6	252		250	13.6 (5.4%)
	Q (MVAr)	-287.4	-239.7	-171.5	-89.1		0	
	V (kV_{rms})	76.6	81.6	85.1	87		87.2	
	I (A_{rms})	1697	1440	1203	1024		956	
50 Hz 110 MVAr compens-ation	**P** (MW)	261.1	257.9	255.3	252.8	250	250	11.1 (4.4%)
	Q (MVAr)	-140.7	-82	-17.3	47.3	106	0	
	V (kV_{rms})	76.4	78.1	78.4	77.3	74.8	74.8	
	I (A_{rms})	1294	1155	1088	1109	1210	1114	
50/3 Hz	**P** (MW)	259.3	256.9	254.2	252.2		250	9.3 (3.7%)
	Q (MVAr)	-77.7	-58.3	-38.7	-19.2		0	
	V (kV_{rms})	76.2	76.0	75.7	75.3		74.7	
	I (A_{rms})	1184	1155	1133	1120		1116	
dc	**P** (MW)	256.5	254.8	253.2	251.6		250	6.5 (2.6%)
	Q (MVAr)							
	V (kV_{rms})	107.7	107	106.3	105.6		105	
	I (A_{rms})	1191	1191	1191	1191		1191	

Table 5.2: Simulation results of the three transmission systems: 50 Hz ac, 50/3 Hz ac and dc (250 MW with 200 km distance)

5.1.3 Conclusion of the transmission technology comparison

Table 5.3 concludes the comparison of the three offshore power transmission technologies. The dc system has no transmission distance limit due to absent of charging current. The cable loss is the lowest. Only two cables are needed for power transmission instead of three, leading to lower installation costs. The major drawbacks are the difficulty of building an offshore multiterminal HVDC network due to the lack of reliable and economically achievable dc circuit breakers and dc/dc transformers as well as the vulnerable dc cable due to prominent space charge accumulation. In addition, the offshore converter platform calls for high installation and maintenance costs.

The 50 Hz ac is the simplest and most mature technology. The offshore multiterminal network is achievable. No offshore converter platform is required. The major problem is the

short transmission distance due to the massive charging current.

The 50/3 Hz ac technology inherits major advantages from the 50 Hz ac. The offshore multiterminal network is also achievable. The converter station is only onshore with the topology 1. The transmission distance can be up to 330 km with no reactive power compensation. As a conclusion, the 50/3 Hz ac can be a promising candidate to fill the gap between the dc and 50 Hz ac technologies for offshore middle-distance power transmission.

Type	dc	50 Hz ac	50/3 Hz ac
Transmission distance	Any	< 80 km* (w/o compensation)	< 330 km* (w/o compensation)
Reactive power compensation demand	Not applicable	High (for 200 km transmission)	None (for 200 km transmission)
Cable loss	Low	Medium	85% of 50 Hz ac
Circuit breaker	Not mature	Mature ac circuit breaker	Mature ac circuit breaker with minor modifications
Transformer	No dc/dc (ac standard)	Standard	Large
Offshore multiterminal network	Difficult	Yes	Yes
Cable	Permanent space charge accumulation	Reliable	Reliable
Converter	Onshore & offshore	None	Onshore for topology 1

(Green indicates advantage, orange neutral and red disadvantage. *the transmitted active power must be higher than 85% of the rated capacity at 132 kV_{rms} line-to-line)

Table 5.3: Conclusion of the transmission technology comparison: 50 Hz ac, 50/3 Hz ac and dc (250 MW with 200 km distance)

5.2 Brief Review of Frequency Converters

Previous studies on low frequency (LF) ac power transmissions have examined magnetic forms of frequency conversion including frequency triplers, variable frequency transformers

(VFT) and rotary converters. The frequency tripler has simple structure but the efficiency is only 80%. Both the VFT and rotary converter contain rotating machines, which require regular maintenance [111, 113, 114].

Another way of frequency conversion is based on the solid-state semiconductors. One is the cycloconverter that has been widely used in motor drive systems. The cycloconverter is already a mature technology and has relatively low cost. Hence, it is suggested for frequency conversion in the 50/3 Hz ac transmission system [110]. A cycloconverter is basically a group of thyristor based CSC-HVDC systems with the 'dc-link voltage' varying according to a 50/3 Hz sinusoidal reference [115]. Three sets of three-phase 50 Hz ac to one-phase 50/3 Hz CSC systems work collaboratively to generate the three-phase 50/3 Hz outputs.

Similar to a CSC-HVDC system, the principle problem with the cycloconverter is the commutation failure [116]. When it operates as an inverter, the firing angle together with the commutation angle is very close to 180^{o}. If there is a voltage drop at the 50 Hz side or a sudden current increase in the system, the angle may be larger than 180^{o}. The polarity of the 50 Hz side voltage will change and it is not possible anymore for the thyristor to commutate until the next voltage cycle. Consecutive commutation failures may lead to system breakdown. As a result, the cycloconverter has very poor fault ride-through capability and requires a strong interconnection grid. Furthermore, the highly distorted output waveforms and poor power flow control capability call for massive filters and auxiliary control equipment.

As introduced in Chapter 2, the MMC inherits all merits from VSCs such as independent control of active and reactive power, black start and improved ac side fault ride-through capabilities. The large number of steps in the synthesized ac side voltage waveform produces a low distortion level and good EMC performance. The passive filters can be largely reduced

or eliminated. The switching frequency for each device is low and the system efficiency can be higher than 99% per station. In order to convert power between 50/3 Hz and 50 Hz ac, two ac/dc MMCs are connected in a back-to-back manner. One converts the power from 50/3 Hz ac to dc and the other converts it from dc to 50 Hz ac.

Table 5.4 concludes the comparison between the cycloconverter and the B2B MMC. Major problems of the cycloconverter are the poor fault ride-through capability and the demand of a strong interconnected grid, while the major problem faced by the B2B MMC is the insufficient practical experience. As the wind power interconnection points are usually not strong, the B2B MMC is preferable especially for cases with strict stability requirement.

Note that the HB-SM based B2B MMC may suffer from a dc side short-circuit fault. However, the chance of a dc side fault in a back-to-back system could be low due to the short dc busbar. Even if a dc side fault happens, the faulted terminal can be isolated by both the 50 Hz side and 50/3 Hz side circuit breakers. If a multiterminal offshore network is avaiblable, the power from the interconnected wind farm could be transmitted to shore through other healthy terminals.

Cycloconverter	**B2B MMC**
Mature technology	New technology
Reliable components	Relatively reliable components Reliable modular structure
High efficiency	Slightly high conduction loss
Offshore multiterminal grid is achievable	
Large footprint	Small footprint
Massive filtering demands	Low/no filtering demands
Require reactive power compensation	No reactive power compensation demand
Require external voltage control	No external voltage control demand
Require strong grid connection	Capable of connecting to any grid
Poor ac fault ride-through capability	Excellent ac fault ride-through capability

(Green indicates advantage, orange neutral and red disadvantage.)

Table 5.4: Comparison between cycloconverter and B2B MMC

5.3 High-level Design of a B2B MMC Frequency Converter

The objective of the high-level design is to evaluate the impacts of frequency reduction on the size and weight of the system. A B2B MMC is two ac/dc MMCs connected in a back-to-back manner with a short dc busbar instead of long dc cables or transmission lines. Theoretically, due to the frequency drop in the 50/3 Hz ac / dc side of the converter (referred to as 50/3 Hz side for simplicity), the size of passive components (capacitance for SM capacitors and inductance for arm inductors) would be three times of that in the dc / 50 Hz ac side of the converter (referred to as 50 Hz side). However, the case may differ in practice. The following section will investigate the capacitor selection considerations of a 50/3 Hz to 50 Hz B2B MMC frequency converter.

Figure 5.5 gives a diagram of a 50/3 Hz to 50 Hz B2B MMC frequency converter. Two ac/dc MMCs are connected in a back-to-back manner. The 50/3 Hz side converts power from 50/3 Hz ac to dc and the 50 Hz side converts the power from dc to 50 Hz ac. As discussed in Chapter 4, parameters such as power rating, operating frequency, voltage ripple allowance and the system's operating point will affect the SM capacitance demand. Figure 5.6 shows the reactive power capability requirements of the converter at the interface point of the onshore grid required by the STC [117]. It requires the 50 Hz side to be capable of supplying the rated active power when the power factor (PF) ranges from 0.95 leading to 0.95 lagging at the point of common coupling PCC_{50Hz} (see Figure 5.5). As there is no standard on the offshore 50/3 Hz ac network currently, the 50/3 Hz side is designed to be able to transmit the rated power at unity power factor. Results may differ if the 50/3 Hz side is required to have certain reactive power capabilities, but the design procedure in Chapter 4 still applies.

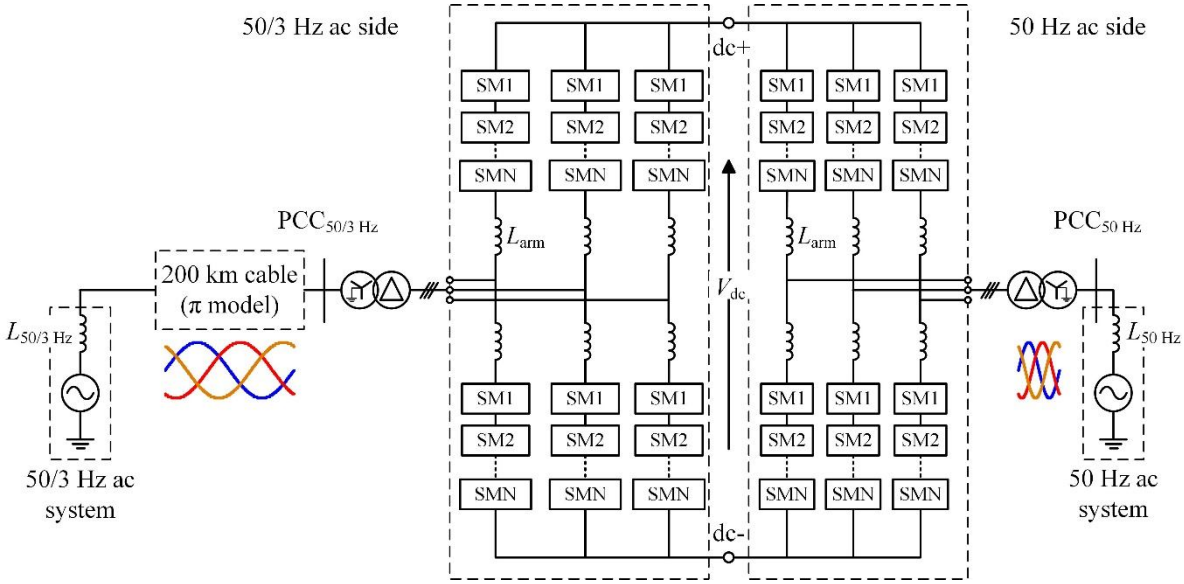

Figure 5.5: Diagram of a 50/3 Hz to 50 Hz B2B MMC system

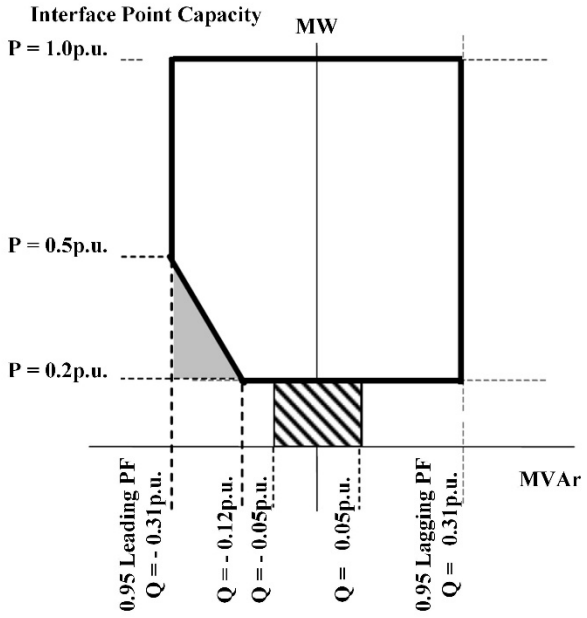

Figure 5.6: Reactive power capability requirements for transmission systems at the interface point [117]

System specifications are given in Table 5.5. Design parameters are concluded in Table 5.6. The coupling transformer has a voltage ratio of 1:1 with 0.1p.u. leakage inductance. All per unit values are based on the corresponding ac side rated voltage and current. As the rated voltage in both ac grids equal to 107.7 kV (phase-to-neutral, peak), the converter dc bus voltage is set slightly higher or ±120 kV and the modulation index m equals 0.9. SM rated dc voltage is set to 2 kV so that the mature 3.3 kV IGBT power module can be used. 120 SMs are required for each arm to withstand the 240 kV pole-to-pole converter dc bus voltage. The total number of SMs in one side of the converter is 796 if 10% redundancy is included. The arm inductance is chosen to be 0.2p.u. for both sides of the converter to avoid resonance and limit change rate of arm currents (di/dt) especially during a fault [55, 118].

Item	**50 Hz**	**50/3 Hz**
Grid voltage (50 Hz)	107.7 kV (phase-to-neutral, peak)	
Grid voltage (50/3 Hz)	107.7 kV (phase-to-neutral, peak)	
Rated modulation index m	0.9	
Dc bus voltage	±120 kV	
Dc current	1040 A	
Filter (ac and dc)	None	
Coupling transformer	YgΔ, 1:1, X_L = 0.1p.u.	
Rated capacity	261 MVA	250 MVA
Rated active power	250 MW	250 MW
Reactive power	±78 MVAr	0
Rated line current I_s	1146 A_{rms}	1097 A_{rms}

Table 5.5: Specifications of the 50/3 Hz to 50 Hz B2B MMC frequency converter

Item	50 Hz	50/3 Hz
Dc bus voltage	±120 kV	
Number of SM per arm	120	
Total number of SM	792 (10% redundancy)	
SM rated dc voltage	2000 V	
SM rated current	920 A_{rms}, 1156 A_{peak}	894 A_{rms}, 1120 A_{peak}
Capacitance	4.8 mF	13.1 mF (2.73×)
Max. voltage ripple	20% peak-to-peak	
Rated voltage	> 2237 V	> 2220 V
Capacitor ripple current stress	> 325 A_{rms}	> 300 A_{rms}
Arm inductor	44.4 mH (0.2p.u.)	133.2 mH (0.2p.u.)

Table 5.6: Design parameters of the B2B MMC frequency converter

The capacitor selection procedure presented in Chapter 4 is used. The permitted SM capacitor voltage ripple is set to 20% peak-to-peak of the SM rated dc voltage. Assuming that the modulation index m at the converter output point is kept at 0.9 at all times for both sides of the converter. The design procedure is similar to the one shown in Table 4.3. The 50 Hz side is required to invert the rated active power at the PCC_{50Hz} when φ_{50Hz} is from -0.3 rad to +0.3 rad and m_{50Hz}=0.9 at all times. When arm inductor and coupling transformer effects are included, the updated modulation index and power factor angle for a few operating points are derived as $m_{arm50Hz}$=0.86, $\varphi_{arm50Hz}$=0 for m_{50Hz}=0.9, φ_{50Hz}=-0.3 rad; $m_{arm50Hz}$=0.94, $\varphi_{arm50Hz}$=0.3 rad for m_{50Hz}=0.9, φ_{50Hz}=0; and $m_{arm50Hz}$=1, $\varphi_{arm50Hz}$ =0.57 rad for m_{50Hz}=0.9, φ_{50Hz}=-0.3 rad using (4.40b) and (4.40d). According to Figure 4.9, at the above operating points, the voltage ripple requirement calls for larger capacitance than the voltage capability requirement. For the above three operating points (m_{50Hz}=0.9, φ_{50Hz} =-0.3 rad, 0 and +0.3 rad), f_{ripple} is derived to be 1.845, 1.762 and 1.825 respectively. The SM capacitance is derived to be 4.8 mF using (4.27a). The maximum capacitor voltage is estimated to be 2237 V when φ_{50Hz}=+0.3 rad using (4.33).

The 50/3 Hz side is only required to rectify the rated active power at unity power factor. When arm inductor and coupling transformer effects are included, $m_{\text{arm50/3Hz}}$ and $\varphi_{\text{arm50/3Hz}}$ are derived to be 0.94 and 2.85 respectively. At this operating point, $f_{\text{cap}} = 0.64$ and $f_{\text{ripple}} = 1.762$. The SM capacitance is derived using (4.27a) to be 13.1 mF. This value is slightly less than 3 times of the 50 Hz side due to the absence of the reactive power capability requirement. The maximum capacitor voltage is estimated to be 2220 V using (4.33). The capacitor ripple current stresses for both sides are estimated to be 325 A for the 50 Hz side and 300 A for the 50/3 Hz side using (4.38a).

The estimated volume and weight of one SM capacitor in both sides of the converter are listed in Table 5.7. All parameters are drawn from the datasheets in [119, 120]. The total volume and weight of all SM capacitors in the 50 Hz side are 55,480 litters and 41.3 tons, and those in the 50/3 Hz ac side are 122,900 litters and 94.7 tons. Hence, the total weight of all SM capacitors in the 250 MW B2B MMC frequency converter is 136 tons, which is 86% {[136/(41.3+94.7/3)]-1} more than that of a B2B MMC operating at 50 Hz ac on both sides.

Side	**Rated voltage**	**Capacitance** (Required value)	**Dimensions** L × W × H (mm)	**Weight**
50 Hz	2400 V	2×2.6 mF (4.8 mF)	340×125×820×2 69.7 L	51.9 kg
50/3 Hz		2×7 mF (13.1 mF)	520×175×880×2 154.4 L	119 kg

Table 5.7: SM capacitor volume and weight estimations of the 50/3 Hz to 50 Hz B2B MMC frequency converter

5.4 Simulation of the B2B MMC Frequency Converter

A model of the designed B2B MMC frequency converter is built in Matlab/Simulink to have a comprehensive understanding of the system's performance in steady state and under fault conditions.

A few modifications are made in the simulation model. Firstly, the number of SMs in each arm is reduced to 20 to increase computation speed (with the redundant SMs neglected). By doing that, each SM has a new rated dc voltage of 12 kV, and the original upper switch and lower switch in each SM are thought to have six 3.3 kV, 1.5 kA IGBT modules [121] connected in series. The SM capacitance of the 50 Hz side is adjusted to 0.8 mF and that of the 50/3 Hz side is changed to 2.19 mF. The rest parameters are kept the same as shown in Table 5.6.

In order to keep the converter output currents balanced under unbalanced grid conditions, ac side currents in both sides of the B2B MMC are collaboratively controlled by decoupled positive-sequence and negative-sequence subsystems as presented in [63]. Each subsystem is independently controlled based on a *dq* reference frame. Bandwidth of the controller in the 50/3 Hz side is set to a third of that in the 50 Hz side. The harmonic circulating currents are controlled by the proportional controller presented in [40] due to its simplicity and stability under unbalanced grid conditions. The modified PSC-PWM modulation technique and the reduced switching-frequency voltage-balancing algorithm proposed in [19] are adopted.

5.4.1 Simulation results: steady state

Figure 5.7 shows waveforms of the B2B MMC frequency converter in steady state operation. The 50/3 Hz side rectifies 250 MW active power from the offshore network at unity power factor (measured at the $PCC_{50/3Hz}$). The 50 Hz side injects all the active power into the

onshore grid and generates additional 78 MVAr lagging reactive power at the PCC_{50Hz}. Figure 5.7(a) to (d) show the converter output voltage and current waveforms at both the PCC_{50Hz} and $PCC_{50/3Hz}$. With similar switching frequency for each device (approx. 250 Hz) in both sides of the converter, the total harmonic distortion (THD) of the 50/3 Hz side outputs is lower than that of the 50 Hz side outputs. This is because of the better filtering effect of the arm inductors and coupling transformers with higher inductance values in the 50/3 Hz side. In other words, the 50/3 Hz ac side can be switched at a much lower frequency for loss reduction while the quality of voltage and current outputs is still comparable with the 50 Hz side. Figure 5.7(e) and (f) show SM capacitor voltage waveforms in both sides of the system. The voltage ripples are all close to the permitted 20% peak-to-peak range when the converter operates at the maximum capacity.

Figure 5.8 shows the average valve losses in both sides of the converter for a given period. The 50/3 Hz side operates as a rectifier and hence the diodes contribute to the major losses. The total loss power in the 50/3 Hz ac side (1.18 MW) is slightly lower than the 50 Hz side (1.28 MW). The overall efficiency of the B2B MMC frequency converter is around 99%, excluding losses in the arm inductors and coupling transformers.

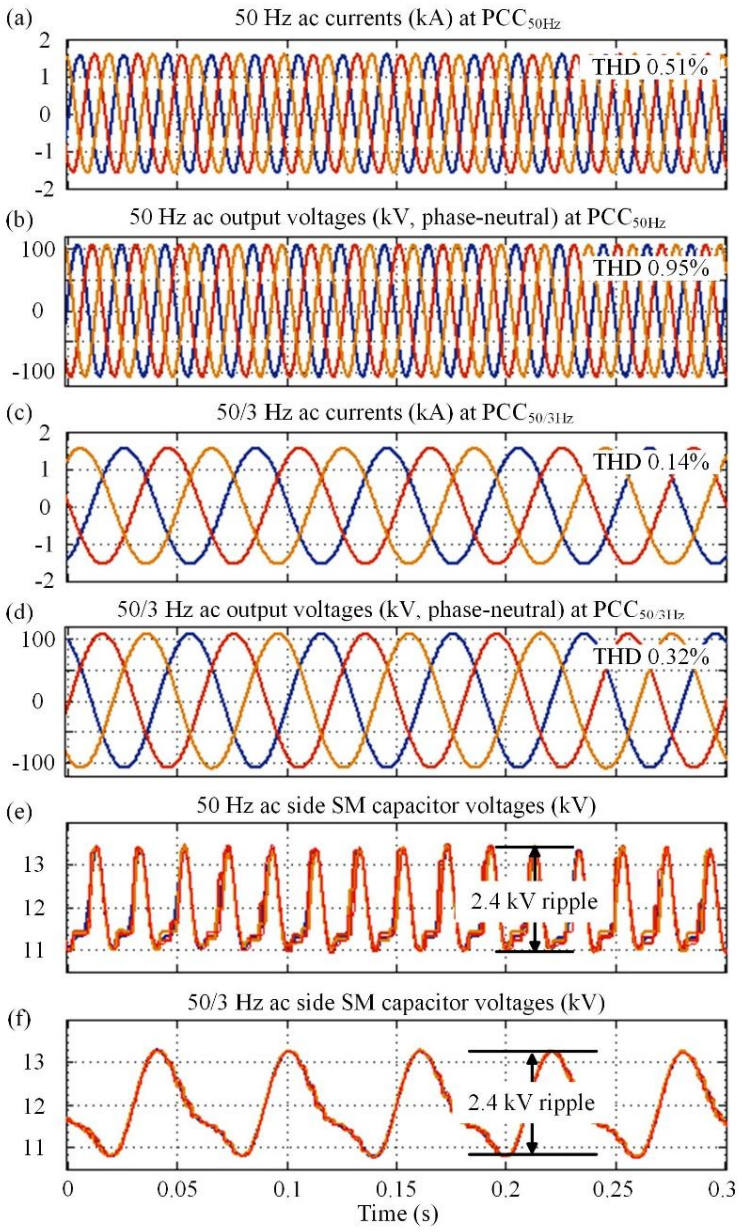

Figure 5.7: Steady-state waveforms of the B2B MMC frequency converter

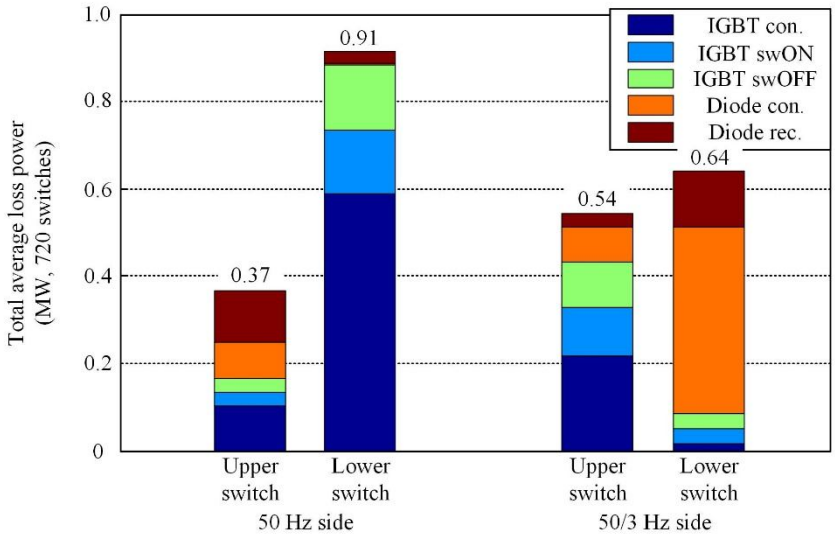

Figure 5.8: Semiconductor power losses

5.4.2 Fault response: 50 Hz side unbalanced low voltage fault

Figure 5.9 shows the system responses when a 0.8p.u. voltage drop (down to 0.2p.u.) is applied to phase *a* of the 50 Hz grid at the PCC_{50Hz}. The p.u. value is based on the 50 Hz side rated voltage. The fault lasts for 100 ms and the voltage is recovered back to 0.9p.u. After another 150 ms, the 50 Hz side grid voltage is fully recovered. Figure 5.9(a) and (b) show the current and voltage responses at the PCC_{50Hz}. With the help of the dual-sequence current controller, the converter ac currents are always well balanced. Since the input power from the 50/3 Hz side remains unchanged during the fault but the power output capability of the 50 Hz side is limited by the faulted phase *a*, amplitudes of the 50 Hz side ac currents are slightly increased to balance the power and keep the dc bus voltage constant. Figure 5.9(c) and (d) show that the 50/3 Hz ac side outputs remain unaffected during the fault. Both output currents and voltages are well controlled and balanced at the $PCC_{50/3Hz}$ indicating the successful fault ride-through of the system.

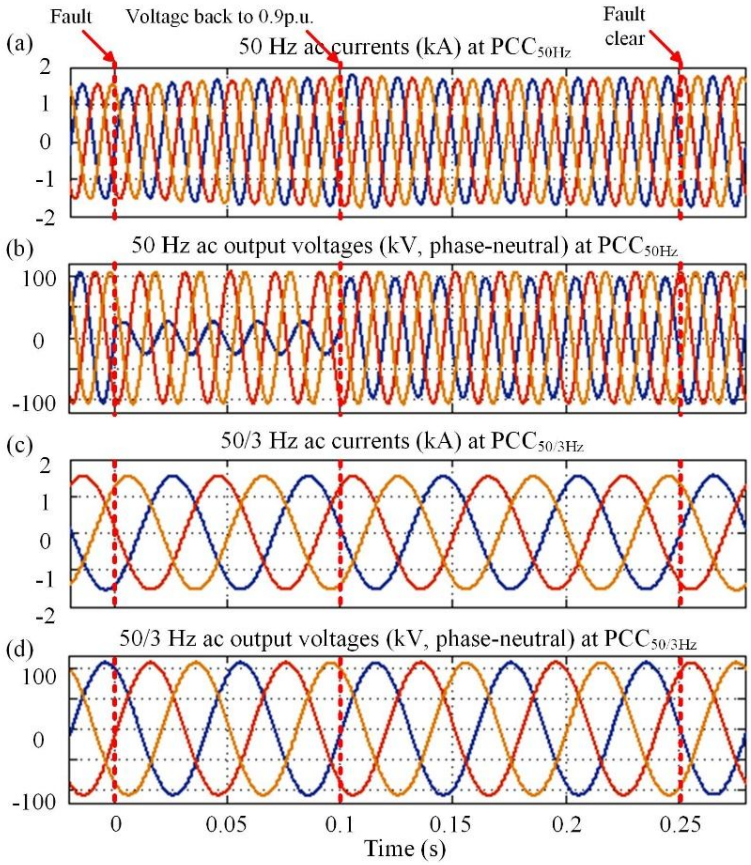

Figure 5.9: 50 Hz side unbalanced low voltage fault in phase *a*: (a) and (b) 50 Hz side output currents and voltages at the PCC_{50Hz}; (c) and (d) 50/3 Hz ac side output currents and voltages at the $PCC_{50/3Hz}$

SM capacitor voltages in both sides of the converter (in phase *a* upper arm) are shown in Figure 5.10(a) and (b). Due to the limited power output capability of the faulted 50 Hz side, SM capacitor voltages in this side rise immediately after the fault, leading to increasing dc bus voltage synthesized by the upper and lower arms. As a result, the dc bus current [Figure 5.11(d)] starts to decrease, which reduces the output power of the healthy 50/3 Hz side. SM capacitor voltages in this side start to increase as well due to the imbalanced power. When the fault is cleared, the responses of SM capacitor voltages are similar but in a reverse direction. SM capacitor voltages in the 50 Hz side decrease first leading to increasing dc bus

current and then decreasing 50/3 Hz side SM capacitor voltages. The above process shows the unique dc dynamics of the B2B MMC system, which include not only the central dc bus capacitor (if any) but also the bulk energy storage distributed in SMs in both sides of the converter. If the controller to regulate the dc bus voltage is not well tuned, the controller dynamics may be too slow and the SM capacitor voltages will go over the limit, leading to overvoltages. Figure 5.11(a) and (b) show the arm currents in both sides of the converter (in phase *a* upper arm). During the fault, all arm currents are well controlled, indicating no overcurrent hazards of devices.

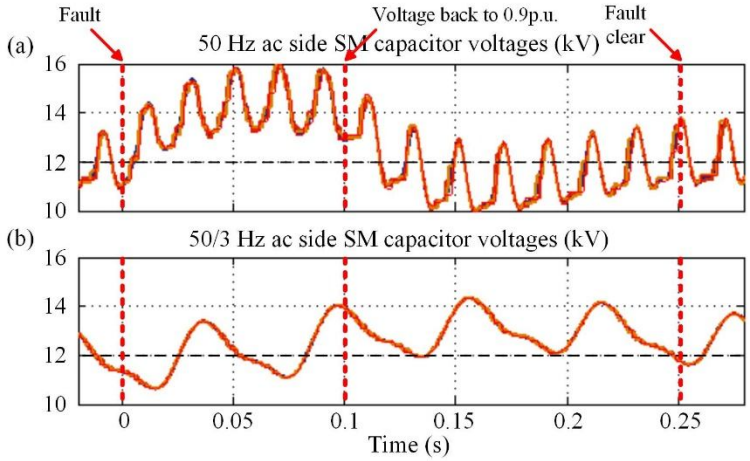

Figure 5.10: SM capacitor voltages during 50 Hz side unbalanced low voltage fault

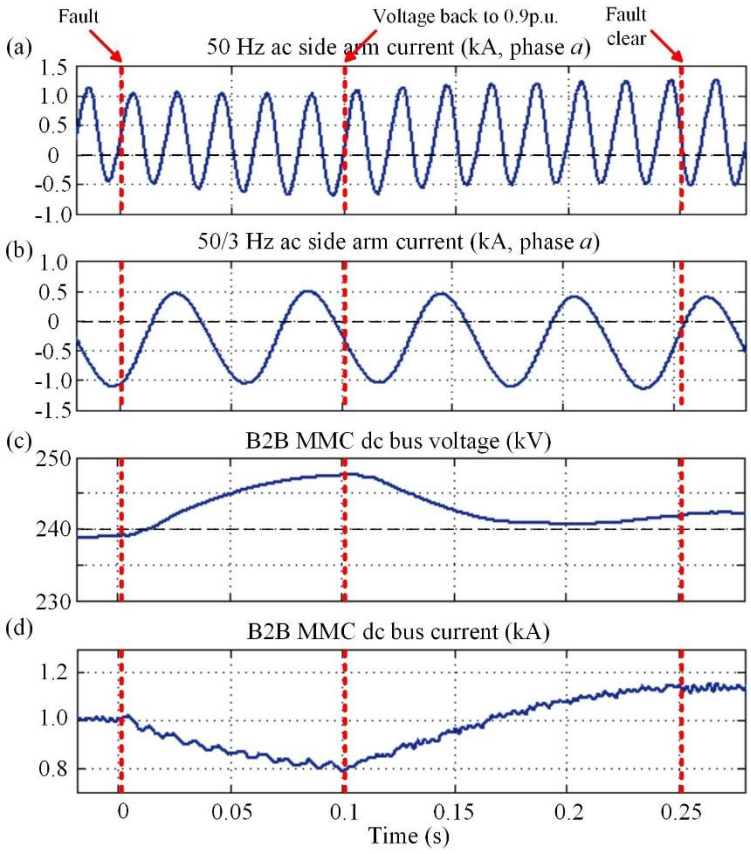

Figure 5.11: 50 Hz side unbalanced low voltage fault in phase *a* (continue): 50 Hz side (a) and 50/3 Hz side (b) arm currents, (c) dc bus voltage, (d) dc bus current

5.4.3 Fault response: 50/3 Hz side unbalanced fault

In this simulation, a single-line-to-ground fault is applied to phase *a* of the 50/3 Hz cable system at 100 km to shore. The fault starts at 0.1 s and is cleared at 0.27 s. Figure 5.12 shows ac output currents and voltages on both sides of the converter. Figure 5.12(a) and (b) show that during the fault, the 50 Hz side ac output currents and voltages are well controlled and balanced, indicating the successful fault ride-through of the 50 Hz side owing to the isolation of the dc bus. The slight decrease of current amplitudes is due to the reduced power input from the 50/3 Hz side. Figure 5.12(c) shows the 50/3 Hz side output currents that are well balanced during the fault owing to the dual-sequence current controller.

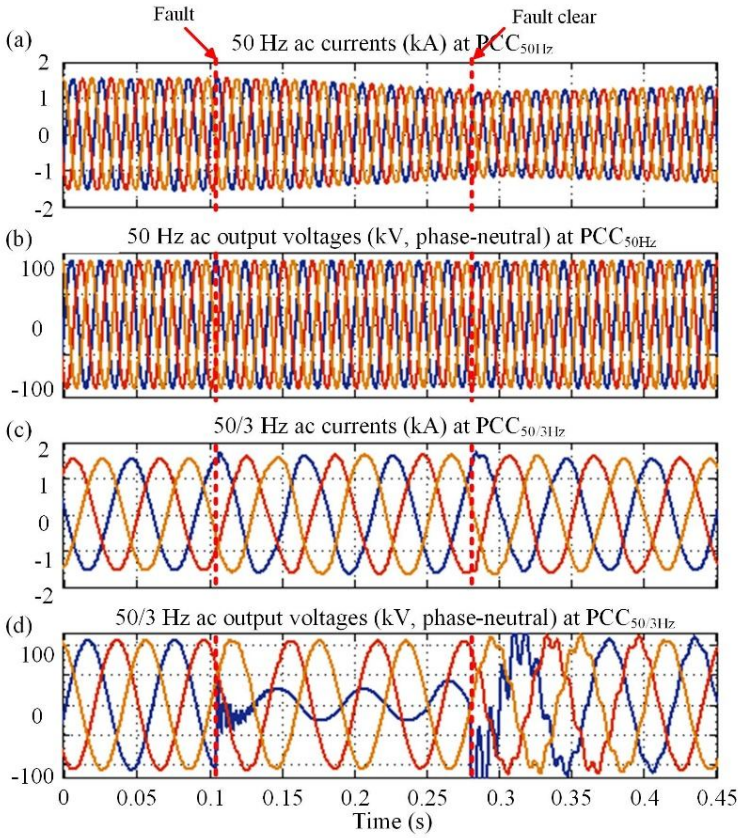

Figure 5.12: 50/3 Hz side unbalanced single-line-to-ground fault in phase *a*: (a) and (b) 50 Hz side output currents and voltages at the PCC_{50Hz}; (c) and (d) 50/3 Hz side output currents and voltages at the $PCC_{50/3Hz}$

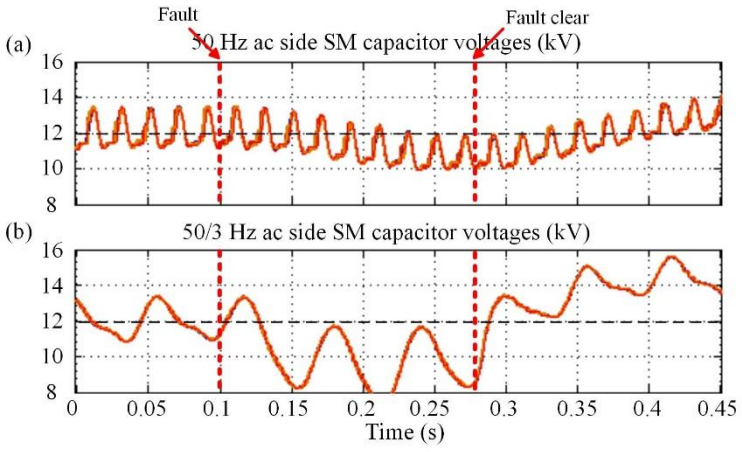

Figure 5.13: SM capacitor voltages during 50/3 Hz side unbalanced fault

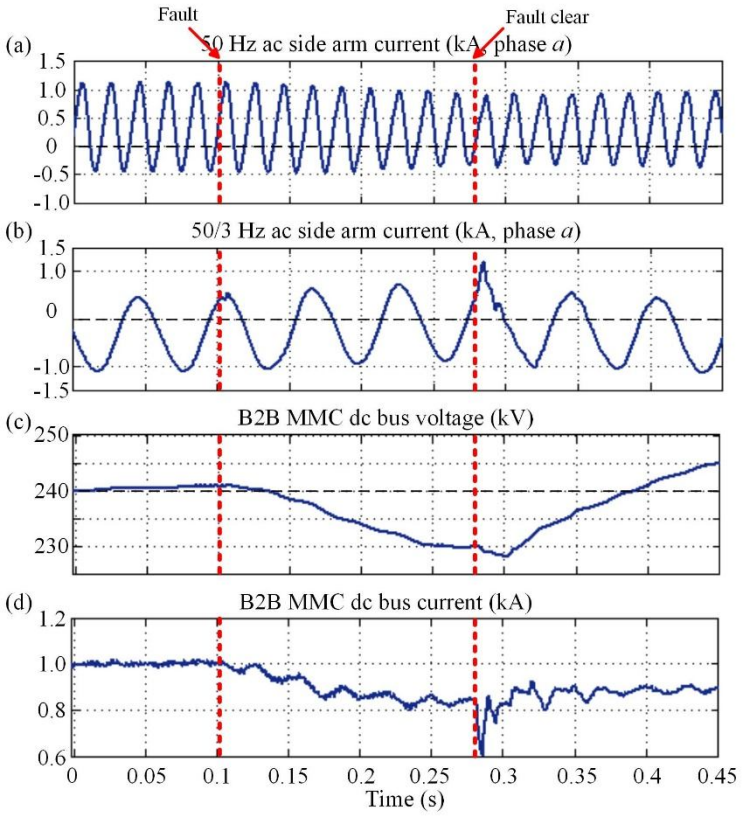

Figure 5.14: 50/3 Hz side unbalanced single-line-to-ground fault in phase *a* (continue): 50 Hz side (a) and 50/3 Hz side (b) arm currents, (c) dc bus voltage, (d) dc bus current

Figure 5.12(d) shows the 50/3 Hz side output voltages at the $PCC_{50/3Hz}$. Fluctuations can be found when the fault happens and when it is cleared. When the fault happens, oscillations between the capacitance and inductance in the cable (π-model) will cause small fluctuations in the voltage at the $PCC_{50/3Hz}$. When the fault is cleared, voltage of the faulted phase *a* suddenly increases to the rated value. When the voltage is around its positive (or negative) peak, the lower arm (or the upper arm) in phase *a* in the 50/3 Hz side has to synthesize a large arm voltage [refer to (2.13a) and (2.13b)]. However, at this moment as shown in Figure 5.13(b), SM capacitor voltages in the arm are only 70% of the rated value due to the fault. There is insufficient SM voltage storage to synthesize the desired arm voltage. As a result, the total output voltage of both the upper and lower arms in the phase unit is much lower

than the dc bus voltage, leading to a current surge in the arm current [Figure 5.14(b)]. This also leads to the fluctuations in the converter ac output voltages at the $PCC_{50/3Hz}$ [Figure 5.12(d)] as well as in the dc bus current [Figure 5.14(d)]. One way to avoid this problem is to stabilize the faulted 50/3 Hz side SM capacitor voltages before increasing the converter output voltages.

5.5 Summary

This chapter evaluates the 50/3 Hz ac technology for offshore power transmission and the B2B MMC for frequency conversion. Three types of transmission technologies are compared for middle distance (200 km) offshore power transmission. The dc is found to be the most efficient option and is capable of transmitting power over the longest distance. It requires fewer cables indicating lower capital costs. Major drawbacks of dc are the difficulty of building an offshore multiterminal HVDC grid due to the lack of reliable and economically achievable dc circuit breakers and dc/dc transformers and the vulnerable dc XLPE cable due to the prominent space charge accumulation. In addition, the offshore converter platform calls for high installation and maintenance costs. The 50 Hz ac is the simplest and most mature option, but its cost-effective transmission distance is less than 50 km due to the massive charging current. Finally, the 50/3 Hz ac is shown to be a promising candidate for offshore power transmission with distances from 100 km to 250 km. Its cable loss is lower than that of the 50 Hz option and the multiterminal grid is achievable with mature ac circuit breakers (with minor modifications if necessary) and transformers.

The cycloconverter and the B2B MMC are compared for frequency conversion. Major advantages of the B2B MMC are the excellent controllability, output quality, and fault ride-through capability. A high-level design of a ±120 kV_{dc} 250 MW B2B MMC is presented,

which converts power between the 50/3 Hz offshore network and the 50 Hz onshore network. Total weight of SM capacitors in the system is 86% more than that of a B2B MMC operating at 50 Hz ac on both sides. Computer simulations show the system performance both in steady state and under fault conditions. Semiconductor losses in both the 50/3 Hz and the 50 Hz sides of the converter are similar. The overall system efficiency is around 99%, excluding losses in arm inductors and coupling transformers. Simulation under fault conditions found that the dc dynamics of the B2B MMC must be given enough attention when designing the dc voltage regulator. Otherwise, SM capacitor over- or under-voltage may occur, which would affect the system's safe operations.

6 A MODEL ASSISTED SM TESTING SCHEME FOR MMC

The MMC is being developed as a core technology for the next generation of high power VSCs. Potential applications include VSC-HVDC systems for a large-scale offshore or onshore wind connection. As presented in Chapter 2, recent research on the MMC has mainly been at the system level including the operating principles, SM capacitor voltage balancing control, circulating current mechanism and its suppression. Detailed study on the electromagnetic and electro-thermal behavior of a SM at the component level has been rare in spite of the fact that it is important for design optimization. One possible reason is due to the difficulty of testing a SM without a complete MMC system. The novel model assisted testing scheme presented in this chapter can test a SM individually before the complete MMC is built. The tested SM's behavior and stress pattern will very closely emulate the practical situation when operating in a complete MMC system.

6.1 Review of Published SM Testing Schemes

In practice, prior to building a complete converter system, both the manufacturer and operator are keen to understand the stress conditions that the SMs are subject to. To build a complete system with a few hundred levels for experiment purpose is time consuming and costly. Power supplies as well as galvanic isolation with voltage level up to a few hundred kilovolts are hard to provide.

An experimental MMC system with largely reduced levels is commonly adopted for control algorithm verification [36, 40]. However, such a system is difficult to predict the performance of the SMs if they are going to be installed in a system with much more levels. The switching pattern will be different leading to different SM output characteristics, such as SM capacitor voltage, electromagnetic and electro-thermal characteristics, etc.

To solve the problem, Gao *et al.* [122], Tang *et al.* [123] and Feng *et al.* [124] proposed a testing scheme to test the SM individually. As shown in Figure 6.1, the testing circuit uses an auxiliary HB-SM (converter) with a dc voltage source to test the prototype HB-SM. A coupling inductor L is installed in between to limit the current change rate (di/dt). Since both SMs are only capable of outputting either the capacitor voltage v_{SM_C1} (v_{SM_C2}) or zero voltage, in order to generate a sinusoidal 'arm current' that flows through them, the two SMs have to switch cooperatively and the resulting switching frequency will be very high (much higher than that in a complete MMC). As a result, both of the electromagnetic and electro-thermal behaviors of the power switches and other components in the prototype SM will deviate from the practical situation when the SM is installed in a complete MMC.

Wang and Chu [125] presented a simplified SM testing scheme as shown in Figure 6.2. Compared with the one shown in Figure 6.1, the auxiliary SM is removed and the voltage of the dc source is reduced to half of the SM rated dc voltage. Through switching the prototype

SM alone, a nearly sinusoidal 'arm current' can be generated. However, the switching frequency is still very high. In addition, the entire 'arm current' will pass through the dc source, indicating very high current carrying capability and power demands of the source.

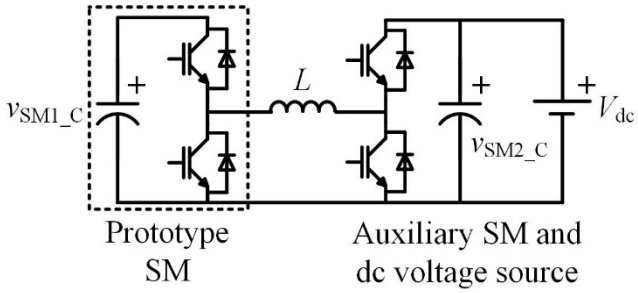

Figure 6.1: Single SM testing scheme proposed in [122], [123] and [124]

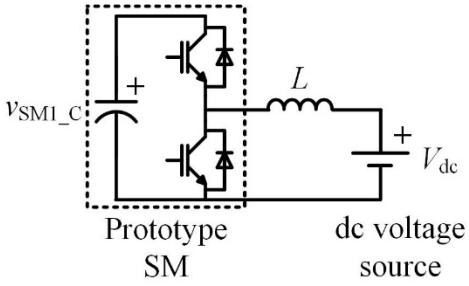

Figure 6.2: Single SM testing scheme proposed in [125]

Instead of using a dc voltage source, Modeer *et al.* [126] used an ac voltage source to generate the sinusoidal 'arm current'. Two identical HB-SMs are connected in series and always switched in opposition to achieve impedance cancellation. As a result, the total output voltage of the two SMs (v_{AB}) will equal to one SM capacitor voltage at all times. Theoretically, the time-average of v_{AB} will be constant and can be compensated by the dc capacitor voltage V_{Ct} leaving only the ac components in either of the two SM capacitors. An ac voltage is added through a coupling transformer to balance the capacitor ac voltage ripples and generate a sinusoidal 'arm current' to circulate in the testing circuit. This testing scheme allows the SM switching frequency to be in the same range, three to five times of the fundamental, as in an actual complete MMC. The major drawback is that an 'arm current'

with a dc offset cannot be generated through the coupling transformer. Hence, this testing scheme is only capable of testing SMs for reactive power compensation applications, such as a STATCOM.

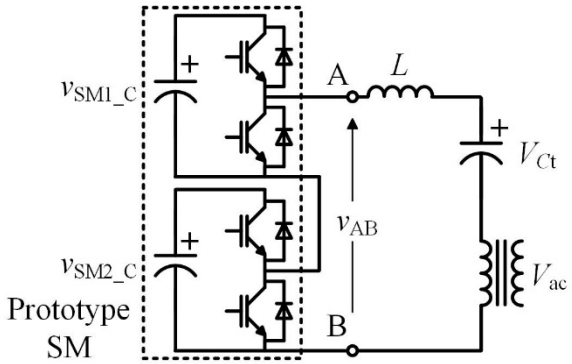

Figure 6.3: Single SM testing scheme proposed in [126]

The model assisted SM testing scheme proposed in this chapter aims to test the SMs without a complete MMC. The tested SM's behavior and stress pattern can very closely emulate the practical situation when operating in a complete MMC. During the test, the 'arm current' can be generated with not only the fundamental frequency component, but also the dc offset and the circulating harmonic components. In the rest of the chapter, Chapter 6.2 explains the proposed model assisted SM testing scheme, and presents a method to establish and maintain the SM capacitor dc (time-average) voltage without affecting synchronization between signals. A FB converter with current hysteresis control is used to set up the 'arm current'. Parameter selection for the coupling inductor and the FB converter is provided in Chapter 6.3 taking into account the current tracking performance, and the switching as well as the sampling frequencies. In Chapter 6.4, simulation results are used to show the effectiveness and accuracy of the proposed testing scheme. In Chapter 6.5, a prototype test platform is presented. Experiment results are given in Chapter 6.6. A steady-state electro-thermal behavior study of a small-scale prototype SM is also reported to demonstrate one application of the proposed testing scheme. Chapter 6.7 concludes the chapter.

6.2 Basic Concept and Control Strategy

6.2.1 Basic concept and structure

In an MMC, as shown in Figure 4.1, the current passing through all the SMs in any of the six arms must equal to that arm's arm current i_{arm}. This arm current, in a steady state, consists of a sinusoidal component at the fundamental frequency with a dc offset depending on the system's operating point and additional harmonic components (mainly the 2nd order). In a well-balanced system, the six arm currents have identical shape with only phase shifts between each other. Also with the SM capacitor voltage balancing control presented in Chapter 2.5, the voltage and current stresses of all SMs are similar with only phase shift differences. In other words, experiments on one or a few SMs in an MMC system can well predict the behavior and performance of the rest. From the view point of the SM (or a few SMs in the same arm) to be tested, if the current flowing through the SM(s) is equal to the arm current and the switching sequence(s) is equivalent to what it would be in a complete MMC system, the output characteristics (SM capacitor voltage, electromagnetic and electro-thermal characteristics) will be representative of the SM(s) installed in a complete MMC system. In other words, if the rest of the converter system is represented by a black box that is capable of providing the 'arm current' and the corresponding switching sequence(s), the behavior of the SM(s) to be tested will remain the same. This black box equivalent is sketched in Figure 6.4.

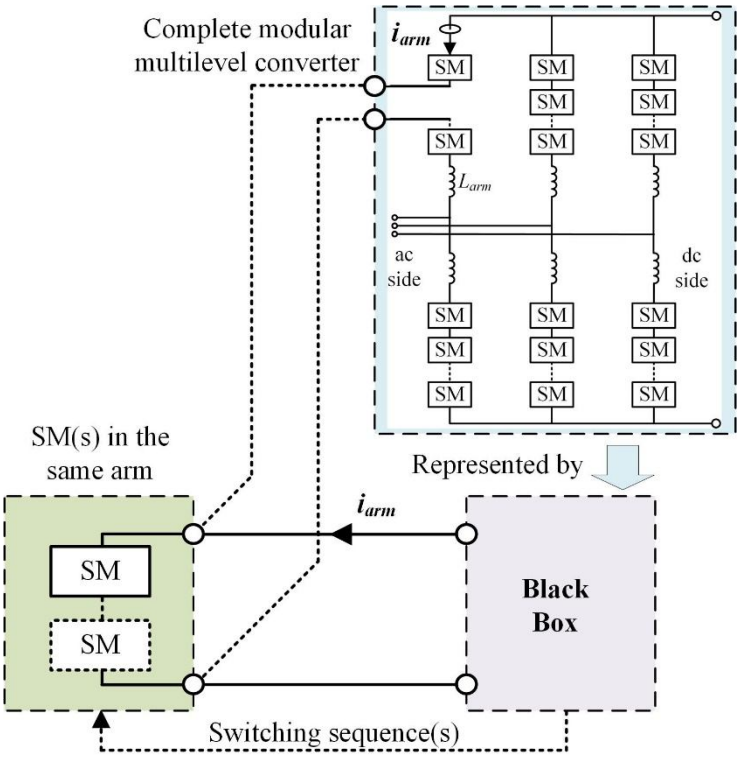

Figure 6.4: Concept of the proposed SM testing scheme

Based on the black box equivalent, Figure 6.5(a) gives a general structure of the SM testing scheme. It requires a controllable current source, the prototype SM(s) and signals of the 'arm current' reference as well as the switching sequence(s) for the SM(s) to be tested. There are two possible ways to run the model assisted SM testing namely with online and offline simulation. With online simulation, a complete MMC model is numerically run in a real-time environment. The 'arm current' reference and the switching sequence(s) are generated and output to the test platform, i.e. the current source and the SM(s) to be tested. The test platform acts as an output power amplifier that also acquires the SM capacitor voltage signal in the physics domain and sends it back to the simulator to close the control loop. The online option provides a convenient way to evaluate the prototype SM(s) in both steady state and transient.

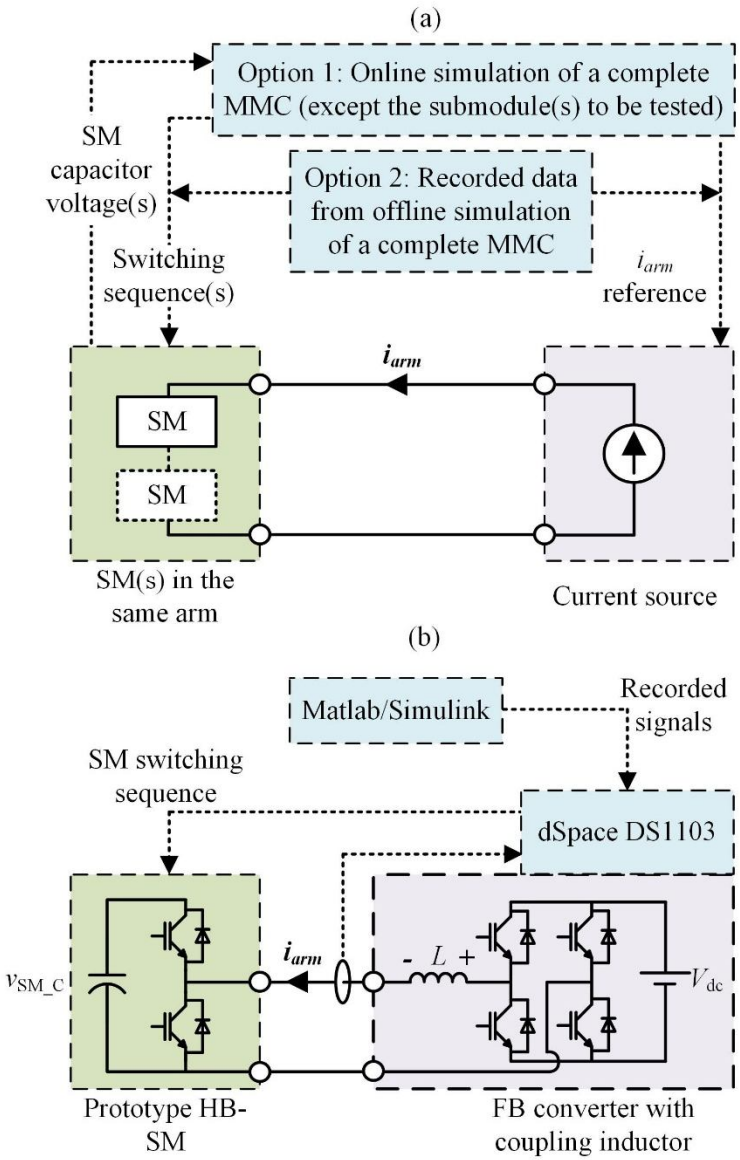

Figure 6.5: (a) Online and offline embodiments of the model assisted SM testing scheme; (b) SM testing scheme adopted in this chapter with a prototype HB-SM

Generally, real-time simulation of a complete MMC is demanding in terms of processing power. If such a real-time simulator is unavailable, the offline testing option offers an alternative to test the SM(s) mainly in steady state. The switching sequence(s) and 'arm current' reference are pre-generated and recorded through computer-aided simulation (using e.g. PSCAD, Matlab/Simulink, or PLECS) of a complete MMC. The recorded signals,

usually sampled over a few seconds, are then used to drive the current source and the prototype SM(s) directly. As shown in Figure 6.5(b), the offline-testing scheme is adopted using Matlab/Simulink as the reference signal generator and dSpace DS1103 as the interface between the master computer and the test platform. A FB converter together with a coupling inductor is used as the current source, which is connected to a prototype HB-SM.

6.2.2 Current control strategy

The control objective of the current source is to ensure that the current flowing into the SM tracks the given reference. For an MMC operating with non-zero active power, a dc offset will exist in the arm current corresponding to the active power exchange between the ac and dc sides. Depending on the circulating current suppression control, the arm current may further contain low order harmonics. Theoretically, current control methods originally designed for single-phase inverters can be applied to this test platform. The PI controller based on a hypothetic synchronous frame is well developed [127, 128], but its limited bandwidth makes it less suitable when the load condition changes fast, as in this application where the SM capacitor is constantly switched in or out. The proportional-resonant (PR) regulator based on a stationary frame offers much faster response [129], but since the controller can only operate with a single frequency, in order to track the current reference with more frequency components, multiple PR controllers have to operate concurrently. As a result, the controller design will be complex and the stability of such a system requires further investigation. In contrast, hysteresis current control offers a simple way to track the current reference with not only fundamental, but also dc as well as other low order harmonics. This method is unconditionally stable with good transient response and accuracy [130, 131]. It is therefore adopted. Simulation results of the test platform showed the hysteresis current controller will be adequate and the error introduced by high order

harmonics due to hysteresis switching is negligible from the viewpoint of the SM under test, as will be explained in Chapter 6.3.

In steady state, the dc component (time-average) of a SM capacitor voltage during the test will ideally be constant for any given 'arm current' and switching sequence. In practice, due to the switch-ON deadband and non-ideal characteristics of power switches, the capacitor dc voltage may not be balanced anymore. The steady-state error of the hysteresis current control, albeit small, will also change the capacitor dc voltage. Hence, a dc voltage regulator is required, which can also help to energize and discharge the SM capacitor.

There are two possible ways to regulate the SM capacitor voltage through either adjusting the switching pattern or the 'arm current'. Since the synchronization between the two signals is essential to guarantee the SM behavior for a certain operating condition, any control method applied must not introduce unpredicted delay to the switching. Hence, the SM capacitor dc voltage is regulated through slightly adjusting the 'arm current' as sketched in Figure 6.6.

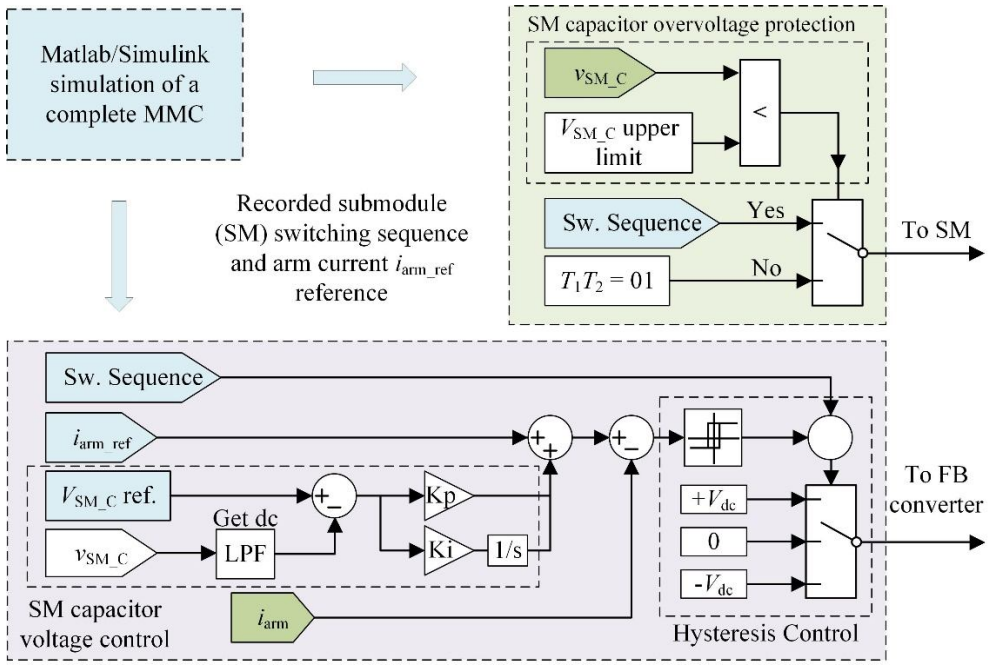

Figure 6.6: Control diagram of the SM test platform (LPF: Low Pass Filter)

Under normal operating conditions, the switching sequence from the complete MMC model simulation is directly fed into the SM under test. For protection purpose, only when the SM capacitor voltage v_{SM_C} is higher than the limit, the capacitor will be protected and by-passed to avoid further charging.

The current reference fed into the FB converter consists of two parts: the 'arm current' reference from the complete MMC system simulation i_{arm_ref}; and a compensation current used to regulate the SM capacitor dc voltage generated by a PI controller. During energizing and discharging the SM capacitor, the proportional gain (K_p) is set large and the integral gain (K_i) is small for fast transient response. When the system reaches steady state, the K_p is largely reduced and K_i is increased so that the dc voltage regulator will then be dominated by the integral part with a very small bandwidth to limit noise.

The current error is defined as the difference between the actual measured 'arm current' and the reference. This current error is calculated and compared with the hysteresis band $\pm H_{band}$. The switching signal of the FB converter is then determined by the current error and the switching sequence of the SM. The hysteresis band is selected by taking account of both the current tracking performance and switching frequency of the FB converter as will be detailed in the next section. The switching (output) scheme for the FB converter is shown in Table 6.1. Note that when the actual current is higher than the reference, the zero voltage output rather than the $-V_{dc}$ is used in order to limit the current error caused during a fixed sampling period while the SM capacitor is switched in.

Current error	**SM output states**	
	0 (Capacitor by-passed)	1 (Capacitor switched-in)
Positive[a]	$+V_{dc}$	$+V_{dc}$
Negative[a]	$-V_{dc}$	0

[a] Indicate larger/smaller than the +/- hysteresis band.

Table 6.1: Switching (output) scheme for the FB converter

6.3 Components Selection for the Current Source

The selection of components is introduced in this section. Firstly, different current dynamics depending on the voltage across the coupling inductor are analyzed. There are two rates of current change with time that are considered when selecting the coupling inductance (L) and the dc source voltage of the FB converter (V_{dc}). The selection process was adopted for two design examples. One is for the experiment described in this chapter and the other is for a SM with higher power level that can be used for a practical HVDC application.

6.3.1 Current dynamics

Table 6.2 lists all the possible current dynamics in the test bench corresponding to the voltage across the coupling inductor. When the SM capacitor is bypassed, the FB converter will output positive or negative V_{dc} depending on the current error; the current will rapidly increase or decrease accordingly. The voltage can also be zero during the deadband of the switches in both the SM and the FB converter. The duration of the deadband is usually less than 10 μs. Its effect can be neglected when compared with the switching frequency of the FB converter (around 5 kHz) and the SM (250 Hz). When the SM capacitor is switched in and the current is above its reference, the FB converter can output $-V_{dc}$ or zero to reduce the current, however, the $-V_{dc}$ output is not in use because of the much larger current change caused during a fixed sampling period. Finally, when the current is below its reference while the SM capacitor is switched in, the current will slowly increase since the voltage on the inductor is only the difference between the dc source voltage of the FB converter and the SM capacitor voltage.

FB converter output	SM output	
	0	v_{SM_C}
	Voltage on the coupling inductor	
$-V_{dc}$	$-V_{dc}$	$-V_{dc}$ - v_{SM_C} (Not in use)
0	0 (only during deadbands)	$-v_{SM\_C}$
$+V_{dc}$	$+V_{dc}$	V_{dc} - v_{SM_C}

Table 6.2: Different coupling inductor voltages

6.3.2 Components selection

Taking into account the variation of the 'arm current' reference, the change rates of the current error between the actual current and its reference can be categorized into fast and slow groups as shown in Figure 6.7 (region 1-2: fast and region 3: slow). $\pm\Delta I_{max}$ is the permitted current error, $\pm H_{band}$ is the hysteresis band, dI_{max} is the error between the above two values and ΔT is the sampling period. The selection of the inductance and the dc source voltage of the FB converter must consider both change rates.

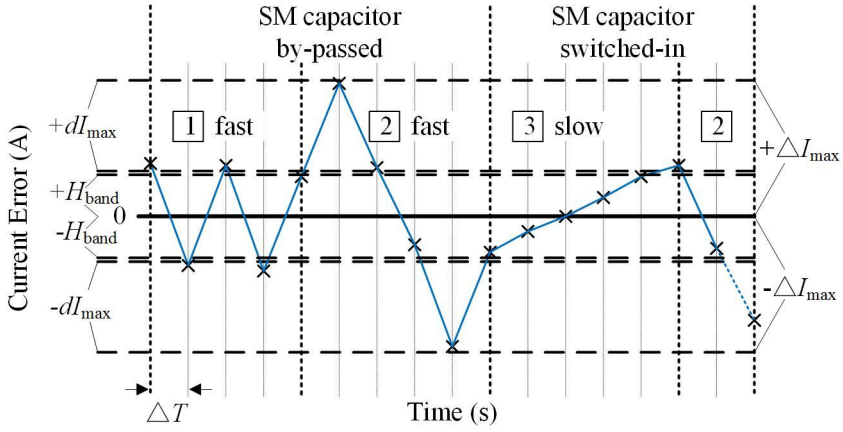

Figure 6.7: Different types of current error dynamics

A. Selection of the permitted current error $\pm\Delta I_{max}$

As region 2 in Figure 6.7 shows, the largest current error is most likely to occur when it changes at the fastest rate. With a limited sampling frequency, the current error will be much larger than the hysteresis band $\pm H_{band}$. The permitted maximum current error $\pm\Delta I_{max}$ is

decided first. One way to determine the permitted current error is according to the resulting error in the experiment outputs, such as losses in the power switches. In this test platform, the conduction losses of the SM IGBT and diode dominate since their switching frequency is relatively low. Here is one way to estimate the error in the conduction loss introduced by the current ripple due to hysteresis switching. If the device's ON-state voltage is simplified as a linear model, i.e. (V_0+RI_0), where V_0 stands for the IGBT/diode junction voltage, R a fixed ON-state resistance of the IGBT/diode and I_0 the device current (simplified as a constant firstly), the average conduction loss for one device over a period of time T can be estimated as:

$$P_{\text{con}} = \frac{1}{T}\int_0^T I_0\left(V_0 + RI_0\right)dt = V_0 I_0 + RI_0^2 \quad (I_0 > 0) \tag{6.1}$$

If the high frequency ripple around the local current I_0 is expressed as a single component $I_e\sin(\omega_e t+\varphi)$, the average conduction loss over the same period T (much longer than $2\pi/\omega_e$) is then:

$$\begin{aligned} P_{\text{con}} &= \frac{1}{T}\int_0^T \left[I_0 + I_e\sin\left(\omega_e t+\varphi\right)\right]\left\{V_0 + R\left[I_0 + I_e\sin\left(\omega_e t+\varphi\right)\right]\right\}dt \\ &= I_0 V_0 + RI_0^2 + \frac{RI_e^2}{2} \end{aligned} \tag{6.2}$$

($RI_e^2/2$) is the error in the conduction loss introduced by the hysteresis switching. In practice, the device current I_0 is not constant and the relative error varies with the magnitude of the current. A relatively accurate estimation of the error can be obtained by integrating (6.2) over the device's conduction time. For simplicity, as an example, a rough estimation is applied here. For the IGBT/diode adopted in the experiment, as to be listed later in Table 6.4, the value of V_0 is around 20 times of RI_0. The current I_0 uses the dc bias value as the average. If the permitted current error is set to ±1.1 A that is ±10% of the peak 'arm current', I_e equals 1.1 A and the introduced error in the overall conduction loss is estimated to be around 1%.

B. Selection of the hysteresis band ±H_{band}

Once the permitted current error is chosen, in order to consider the additional error due to the limited sampling frequency f_s, the hysteresis band $\pm H_{band}$ is set within $\pm\Delta I_{max}$. The gap between the two bands, referred to as dI_{max} must be no less than the maximum current change in one sampling period ΔT, which can be estimated by

$$dI_{max} \geq \frac{1}{L} V_{dc} \Delta T + \omega A \Delta T \tag{6.3}$$

where L is the inductance, ω the MMC ac side line frequency and A the peak amplitude of the ac component at the fundamental frequency in the 'arm current'. Here, in estimation the harmonic circulating current components are neglected because of their much lower amplitudes.

In order to ensure that the switching frequency of the FB converter is always lower than its upper limit f_{sw_max} for heat dissipation and EMC reasons, the hysteresis band is decided according to the ratio between the two frequencies, i.e. f_s and f_{sw_max}. When the sampling frequency f_s is lower than twice f_{sw_max}, the hysteresis band can be set to zero. The FB converter may switch at every sampling instant as shown in Figure 6.7 region 1. When the sampling frequency is higher than twice f_{sw_max}, and lower than 4 times of f_{sw_max}, the whole width of the hysteresis band ($2H_{band}$) has to be set slightly larger than the dI_{max}. The possible maximum switching frequency of the FB converter then reduces to a quarter of the sampling frequency. As the ratio between the two frequencies further increases, the hysteresis band is set according to the equation below:

$$H_{band} = \begin{cases} \dfrac{1}{2}\left\lfloor \dfrac{f_s}{2f_{sw\_max}} \right\rfloor dI_{max} = \dfrac{\Delta I_{max}}{1 + \dfrac{2}{\left\lfloor \dfrac{f_s}{2f_{sw\_max}} \right\rfloor}}, & f_s \geq 2f_{sw\_max} \\ 0. & 0 < f_s < 2f_{sw\_max} \end{cases} \tag{6.4}$$

The above equation helps to divide the space between the permitted current error $\pm\Delta I_{max}$ into a multiple of dI_{max}. Substituting (6.4) into (6.3), the selection of the inductance and the dc source voltage of the FB converter must satisfy the following equation:

$$\frac{V_{dc}}{L} \le \frac{2\Delta I_{max} f_s}{2+\left\lfloor \frac{f_s}{2f_{sw\_max}} \right\rfloor} - \omega A \tag{6.5}$$

Besides (6.5), as stated above, the rising speed of the controlled 'arm current' must be faster than its reference at any time. With the harmonic components neglected, the fastest rising speed of the reference is when the current crosses its dc average from underneath. At that instant, the slope equals to ωA. The slowest rising speed of the 'arm current' corresponds to the smallest voltage drop on the inductor at that instant. Thus, (6.6) must also be satisfied at all times:

$$\frac{V_{dc} - v_{SM\_C}}{L} > \omega A \tag{6.6}$$

C. Two design examples

Voltage and arm current waveforms of the prototype SM can be derived by computer simulation before test. As shown in Figure 6.8, the SM rated dc voltage in the experiment set up is 200 V and the 'arm current' will contain a -3.1 A dc offset plus a fundamental frequency sinusoidal component with a peak amplitude of 8 A and other harmonics with lower amplitudes. The allowed current error $\pm\Delta I_{max}$ is set at ±10% of the current peak or ±1.1 A. The maximum switching frequency f_{sw_max} of the IGBT power module in the FB converter is set at 6 kHz. The sampling frequency of the dSpace DS1103 platform f_s is 20 kHz. The hysteresis band is thus ±0.37 A and according to (6.4), the possible V_{dc} for a few inductance values L_0 is derived and listed in the first two columns in Table 6.3.

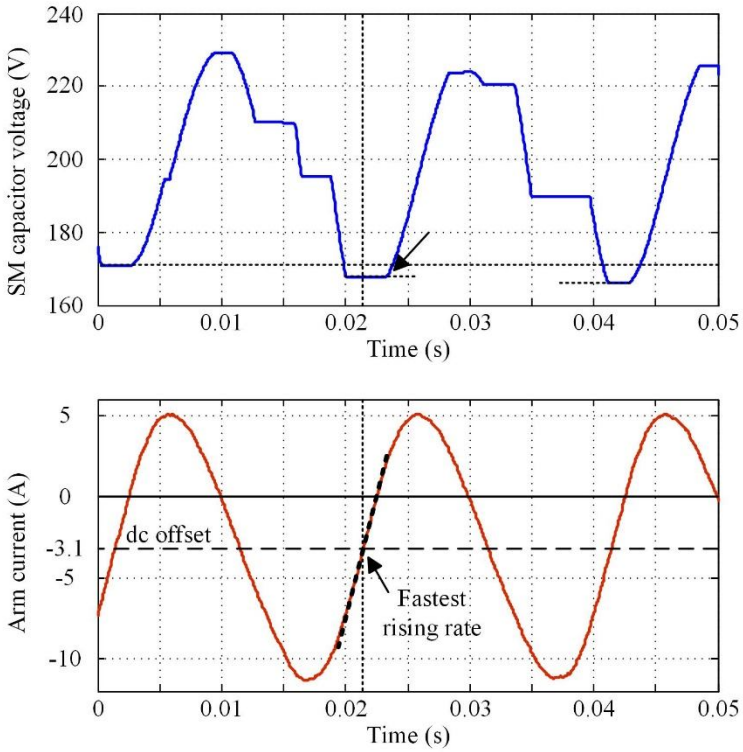

Figure 6.8: Simulated SM capacitor voltage and corresponding arm current

No.	Equation (6.5)		Equation (6.6)	
	L_0	V_{dc}	$V_{dc} - V_{SM\_C}$	L_{max}
1	15 mH	182 V	7 V	2.8 mH
2	18 mH	219 V	44 V	17.5 mH
3	20 mH	243 V	68 V	27 mH
4	25 mH	304 V	129 V	51 mH

Table 6.3: Possible values for dc source voltage and coupling inductance

The next step is to ensure that the slowest rising speed of the controlled current is faster than its reference at the fastest rising point. As shown in Figure 6.8, v_{SM_C} is around 167 V to 175 V when the rising speed of the 'arm current' reaches its maximum. In order to consider the small derivations due to the limited SM switching frequency, the highest value is taken for calculation. According to (6.6), the corresponding voltages and the maximum allowed inductance values L_{max} are derived and given in the last two columns in Table 6.3.

Theoretically, parameters as in No.3 and No.4 groups are all suitable since the maximum allowed inductance L_{max} is larger than the value L_0 (Equation (6.5)). The No.3 group with lower inductance and dc source voltage requirements is already sufficient to test the aforementioned SM and is thus chosen if higher test capacity is unnecessary. After the ranges of the two parameters are decided, simulation can further help to get the optimal values.

The second design example estimates the required inductance and dc source voltage of the FB converter for testing a SM rated at 1000 V_{dc} with peak arm current of 1000 A. The amplitude of the fundamental frequency component in the arm current is estimated to be 700 A. The allowed current error is set to ±5% of the peak arm current. If the FB converter is also based on an IGBT module with 5 kHz maximum optimal switching frequency (with a sampling frequency of 50 kHz), the inductance and dc source voltage are found to be around 4 mH and 1900 V respectively. If the permitted current error can be widened to ±10%, the corresponding inductance and dc source voltage are reduced to 1 mH and 1200 V.

According to the two design examples described above, the dc source voltage of the FB converter is around 20% to 100% higher than that of the SM to be tested depending on the required current tracking accuracy while the current capacity must be at least the same as the current demand of the SM to be tested. With a much higher switching frequency, the cooling system requirements of the FB converter will be higher than that of the SM to be tested. For testing SMs with reduced capacity as shown in the experiment, the increased voltage level as well as larger cooling system is not a problem. For SMs with rated dc voltages lower than 2 kV (with 3.3 kV IGBT/diode module), the device modules with higher voltage levels (4.5 kV or 6.5 kV) are still commercially available for the FB converter. If the SM rated dc voltage is higher than 2 kV, series connection of IGBTs/diodes in the FB converter may have to be used or other multilevel converters can be adopted to replace the FB. The cost of building this versatile test platform may not be low (when compared with the cost of a prototype SM)

however it is believed that this one-off investment can be justified by facilitating the design of an entire MMC system.

6.4 Simulation Verification

This section demonstrates the effectiveness and accuracy of the model assisted SM testing scheme through computer simulation. In the time-domain simulation, a complete MMC model and a test bench model were built in the Matlab/Simulink. Simulation results validated the design of the SM capacitor dc voltage regulator. The power loss simulation showed the testing method to be an effective and accurate way for the SM electro-thermal behavior analysis.

A hypothetic, 21-level, 38 kVA grid-connected MMC with HB-SMs is modelled in the Matlab/Simulink. The converter is connected to a ±2 kV dc-link and a 2.2 kV (line-to-line rms), 50 Hz grid busbar through a three-phase transformer. The arm inductor is 81 mH. All p.u. values are based on ac side rated voltage and current. There are 20 SMs in each arm with a 200 V rated SM dc voltage. All the system parameters are summarized in Table 6.4. For loss analysis, (6.7) and (6.8) are used to calculate the conduction losses of both IGBT and diode, the switch-ON and switch-OFF losses of IGBT and the diode reverse recovery loss respectively [132]:

$$E_{con,k} = \int_{t_1}^{t_2} v_j(i_k, Temperature) \cdot i_k dt \,, \tag{6.7a}$$

$$v_j(i_k) = r_j i_k + V_{0j} \,, \tag{6.7b}$$

$$E_{swtot,p} = \sum_{(t_1,t_2)} \frac{V_{\mathrm{CE}}}{V_{\mathrm{CE\_ref}}} E_p(i_k, Temperature) \,, \tag{6.8a}$$

$$E_p(i_k) = a_p i_k^2 + b_p i_k + c_p \,, \tag{6.8b}$$

where k can be T for IGBT or D for diode; v_j is the device's voltage drop (v_{CE} for IGBT or v_F for diode in the ON state); E_p can be E_{TswOn}, E_{TswOff} or E_{Drec} representing IGBT switch-ON loss, IGBT switch-OFF loss and diode reverse recovery loss respectively. $E_{swtot,p}$ is the total loss for each kind in a given period. Both v_j and E_p are current and temperature dependent. E_p further depends on the blocking voltage V_{CE} at the switching instants. If V_{CE} is different from the one given in the datasheet (V_{CE_ref}), the switching energy is adjusted accordingly as shown in (6.8a). The data for loss simulation is extracted from the datasheets [133] by a curve-fitting method. The junction temperature is chosen as 125°C for all cases to provide a certain safety margin.

Item	Value
Dc bus voltage	4 kV (pole-to-pole)
Grid voltage	2.2 kV line-to-line (rms), 50 Hz
Rated capacity	38 kVA
Transformer inductance	0.1p.u.
Number of SMs	20 per arm
Arm inductance	81 mH
SM rated dc voltage	200 V
SM capacitance	373.3 μF
IGBT/diode module	Infineon IKW30N60T
V_{0CE} / r_{CE}	0.666 (V) / 0.0394 (Ω)
V_{0F} / r_F	0.750 (V) / 0.0250 (Ω)
a_{TswOn} / b_{TswOn} / c_{TswOn}	0 (mJ/A^2) / 0.0175 (mJ/A) / 0 (mJ)
a_{TswOff} / b_{TswOff} / c_{TswOff}	0 (mJ/A^2) / 0.04 (mJ/A) / 0 (mJ)
a_{Drec} / b_{Drec} / c_{Drec}	0 (mJ/A^2) / 0.0175 (mJ/A) / 0 (mJ)
V_{CE_ref}	400 V

Table 6.4: Complete MMC system parameters for simulation

Item	Value
Dc source voltage	240 V
Coupling inductance	20 mH

Table 6.5: Test bench parameters for simulation

A model for the test bench is also built for simulation. The parameters are listed in Table 6.5. According to the components selection process, the dc voltage of the FB converter is set to 240 V and the coupling inductor is chosen as 20 mH. SM parameters are the same as those in the complete MMC model. In steady state, when the converter operates as a rectifier absorbing 38 kW active power from the grid with unity power factor, signals with a duration of one second of both arm current and switching sequence of one SM in the upper arm of phase *a* in the complete MMC model are recorded and then used to run the test bench model.

Figure 6.9 gives the simulation results during the start process. In Figure 6.9 (a) the red line (starting from zero) represents the SM capacitor voltage in the test bench simulation. It ramps up according to a linear reference from 0 to 200 V in 0.25 s. After that, the capacitor dc voltage remains constant and the instantaneous voltage, as shown in the zoomed view, agrees well with the results from the complete model simulation sketched in the blue line. Figure 6.9 (b) compares the currents from both simulations. The current generated by the FB converter model (in red) closely tracks the reference given by the complete model simulation (in blue), as is also shown in the zoomed view. The dc offset with a magnitude of 3.1 A can be clearly seen. The bottom graph is the compensation current generated by the PI controller to regulate the dc component in the capacitor voltage. From 0-0.25 s, K_p and K_i are set to 0.03 A/V and 0.01 A/(V.s) respectively to charge the SM capacitor. After the capacitor dc voltage reaches the reference (200 V), K_p drops down to 0.003 A/V with Ki rising slightly up to 0.02 A/(V.s). The significantly reduced bandwidth of the PI controller helps to limit the noise from the filter of the SM capacitor voltage. In steady state, the compensation current is around 0.15 A_{dc} which is thought to make up for the impact of the current tracking error of the hysteresis control on the SM capacitor voltage. This is because the dc component of the SM capacitor voltage will immediately drop when the voltage regulator is deactivated.

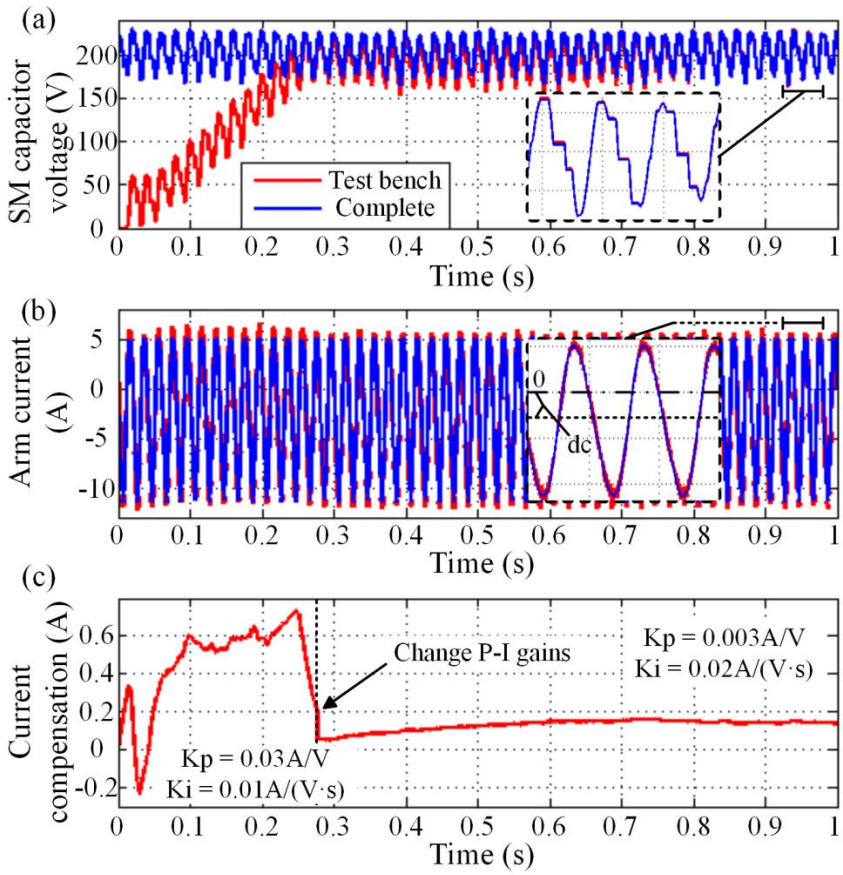

Figure 6.9: Simulation results comparison between the complete and the test bench models during start process: (a) SM capacitor voltage, (b) arm current and (c) current compensation

Table 6.6 presents the power loss simulation results obtained from both the complete system and the test bench models. During the given period, the average power losses for SM switches given by the test bench model are very close to those given by the complete model and the errors around 1.5% agree with the error estimation given in Chapter 6.3.2. The error in the conduction loss of the lower IGBT T_2 is larger than the other values. The reason can be explained that the conduction time of T_2 is short and the current passing through it is small when the converter rectifies active power. Also, the conduction loss error of the lower diode D_2 is minus rather than plus, which is due to the +0.15 A compensation current.

Loss power (W)	**Complete model**	**Test bench model**	**Complete model**	**Test bench model**
	Upper module (T_1/D_1)		Lower module (T_2/D_2)	
IGBT conduction	0.967	0.980 (+1.3%)	0.152	0.158 (+4%)
IGBT switch-ON	0.019	0.018	0.005	0.005
IGBT switch-OFF	0.042	0.041	0.011	0.012
Diode conduction	0.865	0.878 (+1.5%)	3.233	3.180 (-1.6%)
Diode reverse recovery	0.005	0.005	0.018	0.018
Sub-total (difference)	1.896	1.922 (+1.4%)	3.420	3.373 (-1.4%)

Table 6.6: SM semiconductor devices losses comparison between the complete model and the test bench model – rectifying operation, 10 A_{rms} line current

6.5 Experimental Test Platform

A prototype model assisted SM test platform is built and tested experimentally to further verify the validity of the proposed testing scheme. All parameters in the experiment are listed in Table 6.7.

In the first version of the prototype HB-SM, the power module board, the gate driver and other auxiliary control boards are separately designed. Figure 6.10 shows a gate driver board and a RC deadband board. The IR2213 High-and-Low-Side Driver from the International Rectifier designed for HB applications is used. The floating channel can be used to drive an IGBT in the high side that operates up to 1200 V. The gate-driver-enable configuration is to protect the power modules from shorting the dc capacitor using a NAND gate connected to the SD (shutdown) port of the gate driver chip.

Item	Type	Parameters
Dc power supply	Magna-Power Electronics	Rated: 600 V_{max}, 20 A_{max}; Set at 240 V
FB converter	SEMIKRON SK35GD126ET	Rated: 1200 V, IGBT 32 A / diode 23 A at 80 °C
Coupling inductor	Hammond Manufacturing	Rated: 20 mH, 20 A_{dc}
SM rated dc voltage		200 V
SM capacotor	EPCOS B25620-B1427-A101	Rated: 420 μF, 1100 V_{dc}; Actual: 373 μF
SM power module	Two Infineon IKW30N60T	Rated: 600 V, (IGBT & diode) 30 A at 100 °C
Interface	dSpace DS1103	f_s=20 kHz
Temperature recorder	TC-8 thermocouple data logger	
Voltage transducer	LV 25-P	-280 V to 280 V
Current transducer	LA 55-P	-70 A to +70 A

Table 6.7: Parameters for experiment

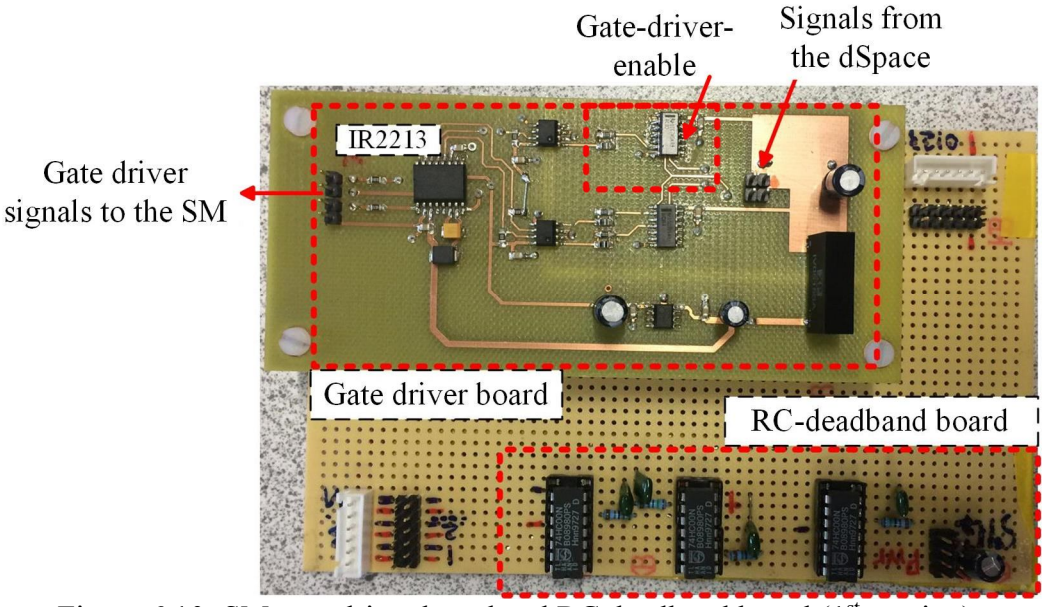

Figure 6.10: SM gate driver board and RC deadband board (1st version)

Figure 6.10 also shows the hardware RC-deadband circuit. In high-voltage high-power applications, a deadband with a duration of a few microseconds is usually added before the turn-ON command in order to avoid shorting the dc bus capacitor. Since the digital output port of the dSpace 1103 is only able to output signals at up to the maximum sampling frequency 20 kHz (50 μs) that is too long for a deadband, an external hardware deadband circuit is required. The RC delay circuit offers the simplest and reliable way to achieve the switch-ON delay externally. The basic principle of the RC swich-ON delay is shown in Figure 6.11 and 6.12. As shown in Figure 6.11, $V_{\text{ON\_min}}$ is the minimum input voltage for the logic device to treat it as a high-level input. If neglecting all propagation delays, the length of the deadband depends on the time constant of the RC circuit, that is

$$t_{\text{on}} = -\ln\left(1-\frac{V_{\text{ON\_min}}}{V_{\text{cc}}}\right)RC \tag{6.7}$$

where V_{cc} is the logic gate supply voltage, R and C the resistance and capacitance in the RC circuit. Figure 6.12 shows the diagram of the entire RC switch-ON delay circuit.

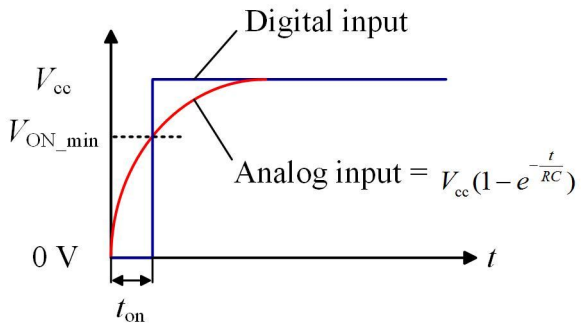

Figure 6.11: Basic principle of RC switch-ON delay

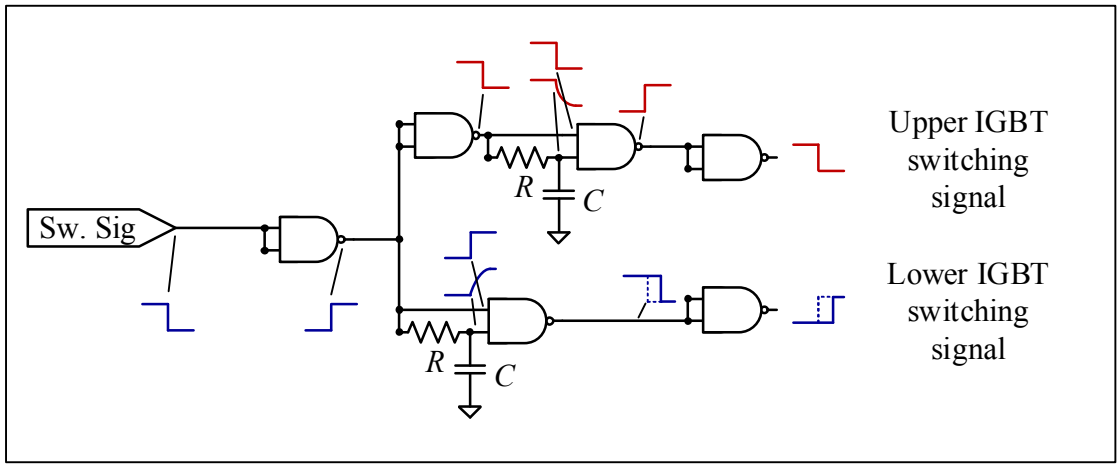

Figure 6.12: Diagram of the RC deadband circuit

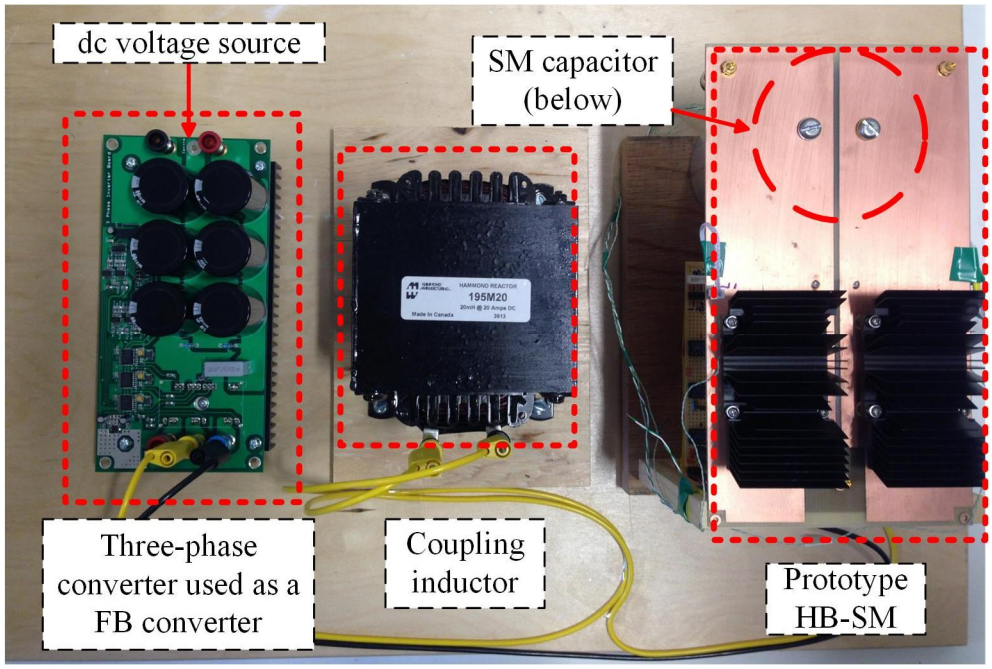

Figure 6.13: Overall view of the prototype test platform

Figure 6.13 shows an overall view of the prototype SM test platform including the FB converter, the coupling inductor, and the prototype SM. The FB converter is a three-phase dc-ac converter that is already available in the lab based on SEMIKRON SK35GD126ET IGBT power module. During the test, one phase is disabled and the converter operates as a FB. The dc voltage source is from Magna-Power Electronics that can supply dc voltage up to

600 V with 20 A current. The coupling inductor is from Hammond Manufacturing with 20 mH inductance. The prototype HB-SM uses two Infineon IKW30N60T IGBT/diode modules, each covered by a single heatsink for the convenience of temperature measurement.

Figure 14 and 15 show the voltage and current measurement boards respectively. The voltage measurement board uses an LEM LV 25-P voltage transducer. The high-side voltage is converted to a very small current with a parallel connected resistor R_1= 20 kΩ. The small current flowing through the primary side of the transducer will induce another current in the secondary side. A measuring resistor R_M=150 Ω is added in the secondary side to convert the current back to voltage signal and send to the oscilloscope and the dSpace. Current range of the primary side is between -14 mA and +14 mA. With the 20 kΩ primary side resistor, the voltage measurement range is from -280 V to 280 V. Maximum heat dissipation of R_1 is calculated to be 3.92 W (I^2R), and power rating of R_1 is chosen to be 5 W. Both R_1 and R_M have high precisions (±1% and ±0.1% respectively) and low temperature coefficients (±20 ppm/^{o}C and ±15 ppm/^{o}C) to achieve high precision. A small capacitor (C=1 μF) is connected in parallel with R_M to filter out the high frequency harmonics. The bandwidth of the voltage measurement board is derived to be 1 kHz and the phase shift for 50 Hz is -2.7^o.

The current measurement board uses an LEM LA 55-P current transducer. The current measuring range is from -70 A to +70 A. The conversion ratio is 1:1000. A high precision resistor (R=100±0.01% Ω) is used in the secondary side to convert the current signal to voltage signal. A small capacitor is also connected in parallel to filter out the high frequency noises. Since the current measurement board is designed to measure the 'arm current', which may contain harmonics as high as 4 kHz due to hysteresis switching, higher bandwidth is chosen (16 kHz) and the capacitance equals 0.1 μF. The phase shift for 50 Hz is -0.2^o. Both voltage and current measurement boards are calibrated before put into use.

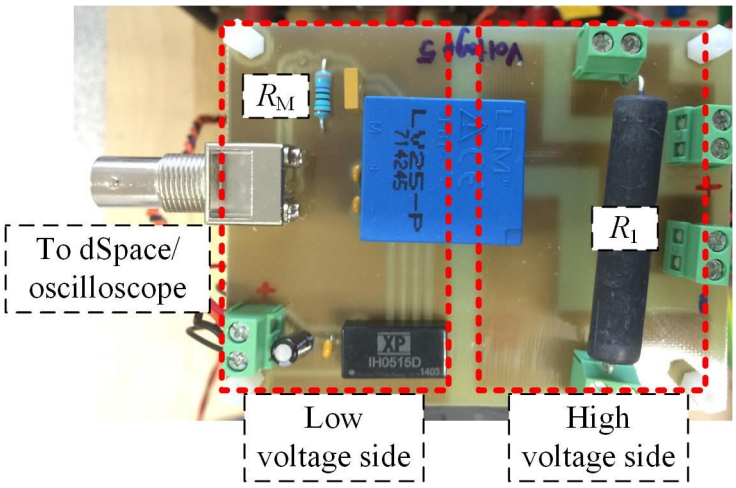

Figure 6.14: Voltage measurement board

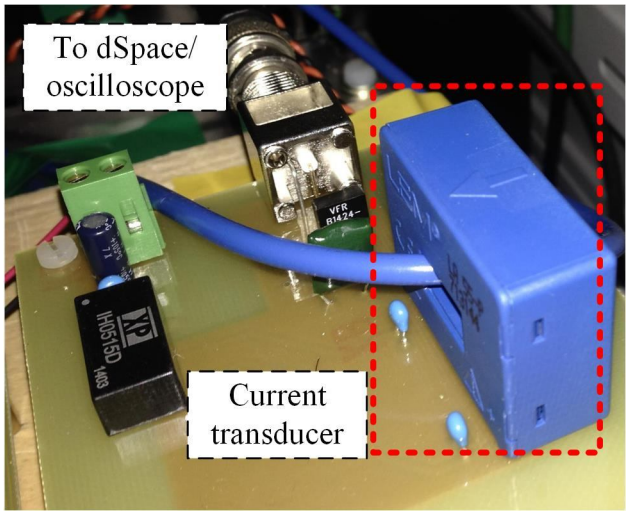

Figure 6.15: Current measurement board

6.6 Experiment Results

Figure 6.16 shows the prototype SM test platform assembled and installed in a protected enclosure. Figure 6.17 shows an oscilloscope snapshot of the experimental results. From top to bottom are the waveforms for the SM capacitor voltage (red), SM switching sequence (blue) and the measured 'arm current' (yellow). The average capacitor voltage over a period is measured to be the set 200 V reference. A dc bias can be clearly seen in the actual 'arm current'.

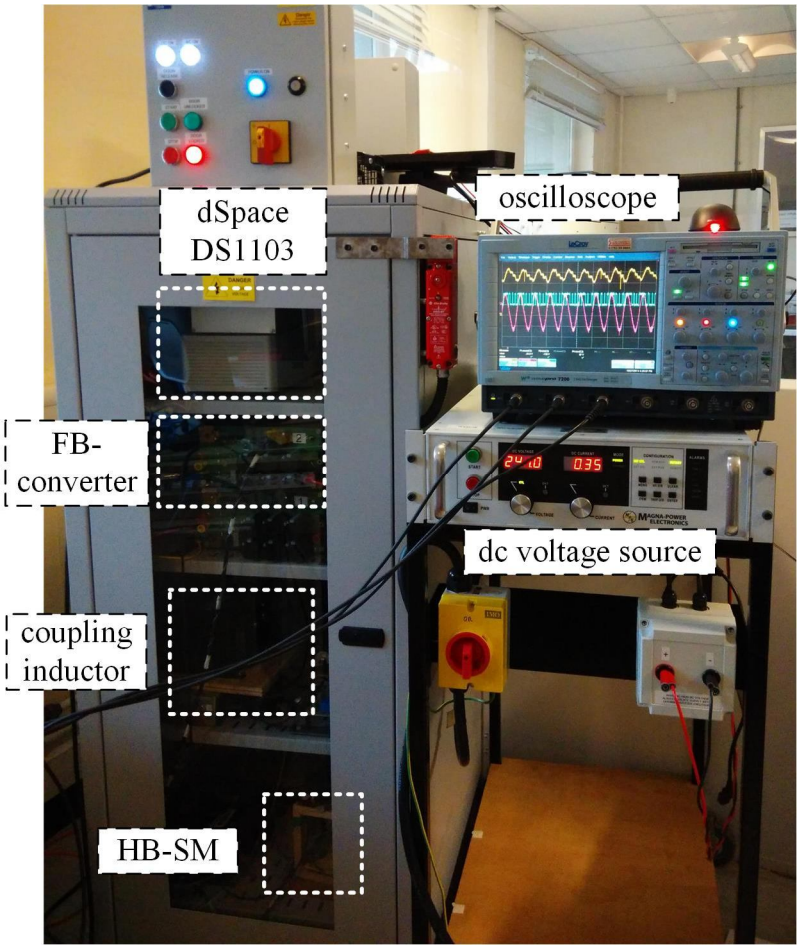

Figure 6.16: SM test platform installed in a protective enclosure

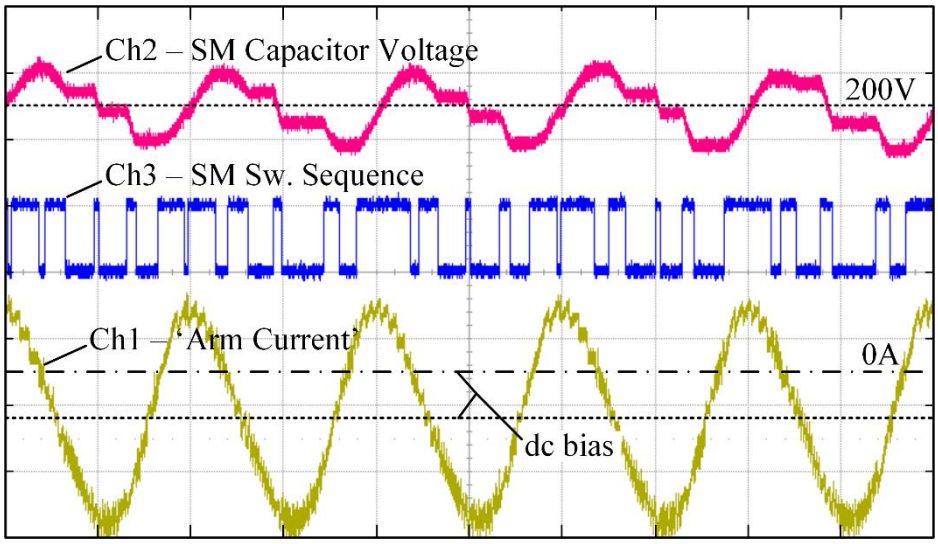

Figure 6.17: Experiment results recorded by the oscilloscope. Horizontal Axis: 10 ms/div. Ch-1-'arm current': 5 A/div, -1.5 div offset (yellow). Ch-2-SM capacitor voltage: 50 V/div, -1.5 div offset (red). Ch-3-SM switching sequence (blue)

Figure 6.18 compares the results from the experiment (solid red) and the simulation of the complete MMC model (dashed blue). Figure 6.18(a) shows that the SM capacitor voltage in the experiment agrees well with the result given by the complete model simulation. In Figure 6.18(b), the current flowing into the SM in the experiment (in red) tightly tracks the given reference (in blue). The two zoomed views give the details of the actual 'arm current' achieved by the hysteresis switching. The zoomed view on the right side shows that even with the slowest rising rate, the actual current is still capable of tracking the reference at its fastest-rising instant, which verifies the components selection process provided in Chapter 6.3.2. The difference between the actual current i_{arm} and the reference (i_{arm_ref} without compensation current) are shown in Figure 6.18(c). The current errors are all within the designed ±1.1 A region. Figure 6.18(d) gives the details of the switching process. The maximum current change in a sampling period is found to be 0.82 A that is slightly larger than the estimated 0.73 A according to (6.3). The error is introduced by the fluctuations in the compensation current.

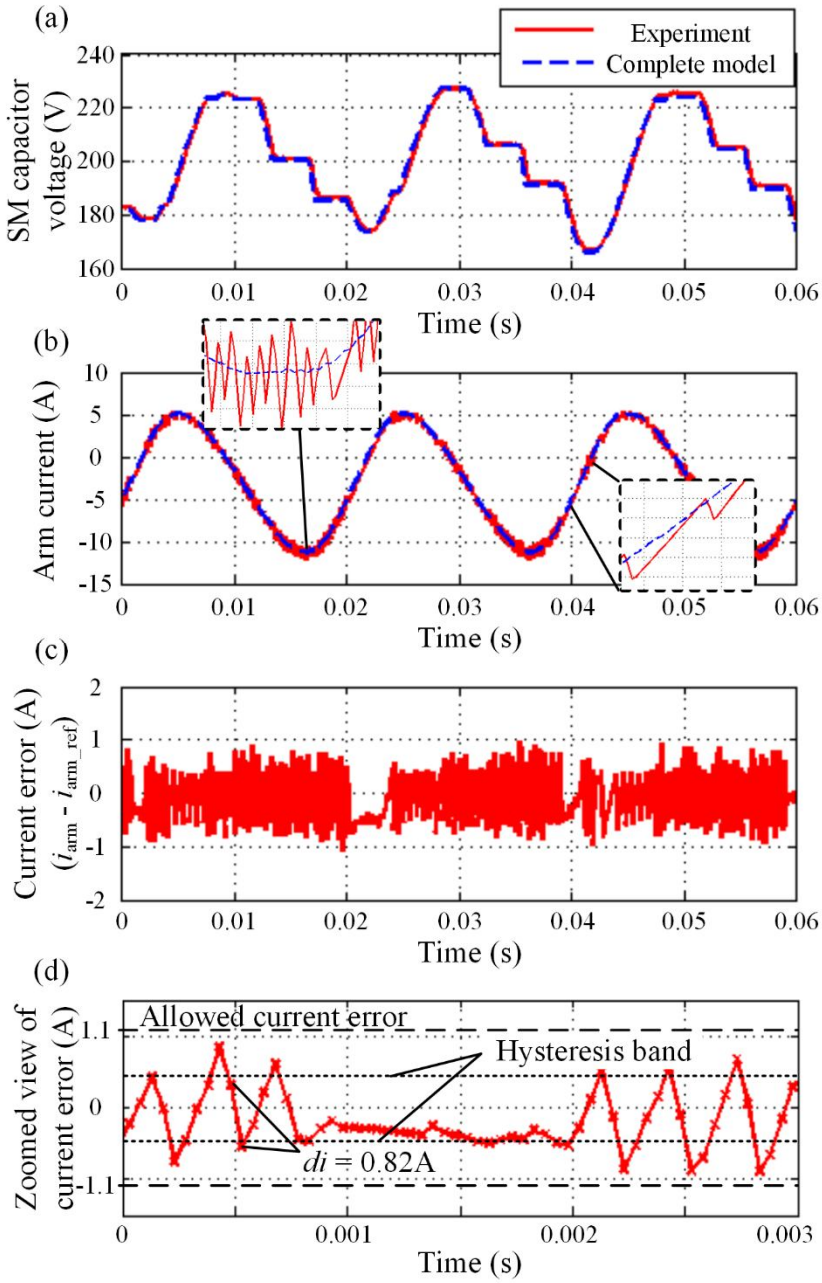

Figure 6.18: Comparison between experiment (solid red) and complete model simulation (dashed blue): (a) SM capacitor voltage; (b) 'arm current'; (c) current error (i_{arm} - i_{arm_ref}); (d) zoomed view of the current error

Figure 6.19 gives the FFT of the current error. The high order harmonics around 1.6 kHz and 4 kHz are due to the hysteresis switching. Their impacts have been shown to be limited on the electro-thermal performance of the SM under test. As shown in the zoomed view, the biggest error is found at the fundamental frequency 50 Hz, which is caused by the phase delay between the actual 'arm current' and its reference. The delay angle is 0.8° within which 0.45° is due to the 20 kHz sampling frequency. 0.2° is introduced by the RC filter in the current sensor and the rest is caused by the hysteresis control itself. The phase delay also causes the error at 100 Hz corresponding to the major circulating current component in the 'arm current'. Besides that, as discussed in the simulation results, the dc error is introduced by the current compensation. Amplitudes of the above errors are small when compared with the peak 'arm current'. If those errors are not acceptable in certain applications, methods such as narrower permitted current error band, faster sampling frequency and/or variable hysteresis band can be adopted.

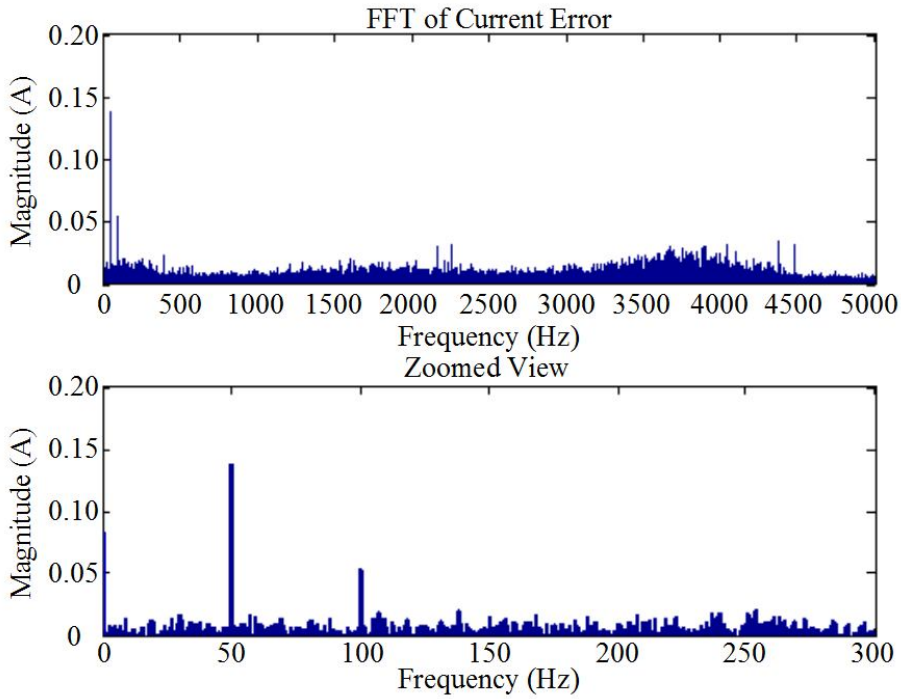

Figure 6.19: FFT of current error (i_{arm}–i_{arm_ref})

6.7 Application: Electro-thermal Behaviour Test

Two sets of electro-thermal behavior tests are shown as a demonstration of the proposed SM testing scheme. One test compares the temperature of two SMs at different locations in the same MMC converter. The other test compares the temperature of the same SM when the MMC converter operates at four different operating points.

6.7.1 Electro-thermal test 1

In the first test, the arm current references and switching sequences of two SMs at different locations in the same MMC converter are recorded by the complete model simulation. The converter operates as a rectifier absorbing 38 kW active power from the ac grid as in the system simulation. In the test, the recordings are run repeatedly for 2500 seconds for both SMs. The temperatures of the upper switch, lower switch and the ambient are recorded and shown in Figure 6.20. The results agree well with the loss simulations (Table 6.6), which show that during rectification, most of the arm current will pass through the diode in the lower switch and thus lead to higher temperature than the upper pair.

According to Figure 6.20, the temperatures of SMs at different locations are similar when the converter system is well balanced. As shown in the top graph in Figure 6.20, for SM No. 1 in the upper arm in phase *a*, the absolute temperature rise above the ambient for the upper switch is 8.73 ºC and that for the lower switch is 14.97 ºC. As the bottom graph shows, for SM No. 10 in the lower arm in phase *b*, the temperature rise for the upper switch is 8.74 ºC and that for the lower switch is 15.63 ºC. Loss simulations show that during the recorded 1 second period, the average power losses for the upper switch of the first SM is 1.95 W and that for its lower switch is 3.38 W. The average power loss for the upper switch of the second SM is 1.92 W and that for its lower switch is 3.43 W. Although the limited experiment time did not allow the temperature of both SMs to reach steady state, the already

derived experiment results agree well with the simulation. The results further demonstrate the accuracy of the test bench in electro-thermal analysis.

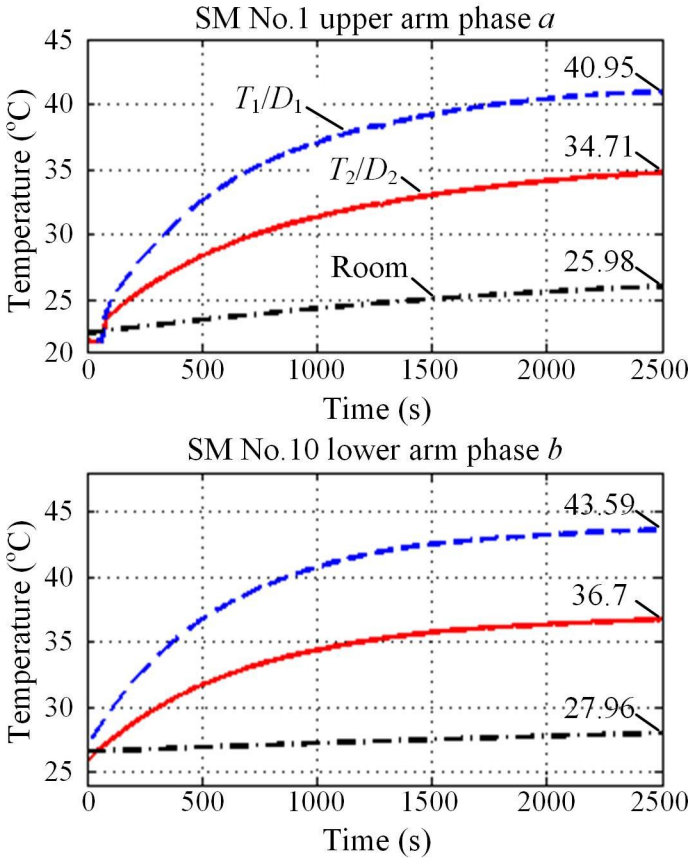

Figure 6.20: Results of electro-thermal test 1: top and bottom figures are temperature recordings for two SMs in the same converter at different locations. The lines are upper IGBT/diode module (T_1/D_1) (solid red), lower IGBT /diode module (T_2/D_2) (dashed blue) temperatures and the room temperature (dashed-dot black)

6.7.2 Electro-thermal test 2

In the second test, the complete converter model is run for four different operating points including rectifying (38 kW), inverting (38 kW), absorbing reactive power (Q) (38 kVAr) and generating reactive power (Q) (38 kVAr) respectively. One second of arm current and switching sequence data pairs are recorded and downloaded to the test platform. Four experimental tests are then run continuously for 1800 seconds. Figure 6.21 shows the final

temperature recordings. The results are also compared with the loss simulations for each case as shown in Table 6.8. This electro-thermal test shows that due to the phase shift of the arm current and switching sequence, when the converter system runs at different operating points, the power losses and the resulting temperature for the upper and lower switches are different. The uneven heat distribution might accelerate the aging process of the semiconductor switches [134]. The complexity of the cooling system design may need to be addressed. Novel HB IGBT/diode module design specialized for MMC application might help to solve the uneven heat distribution problem. The SM testing scheme proposed in this chapter is able to facilitate future research in this direction.

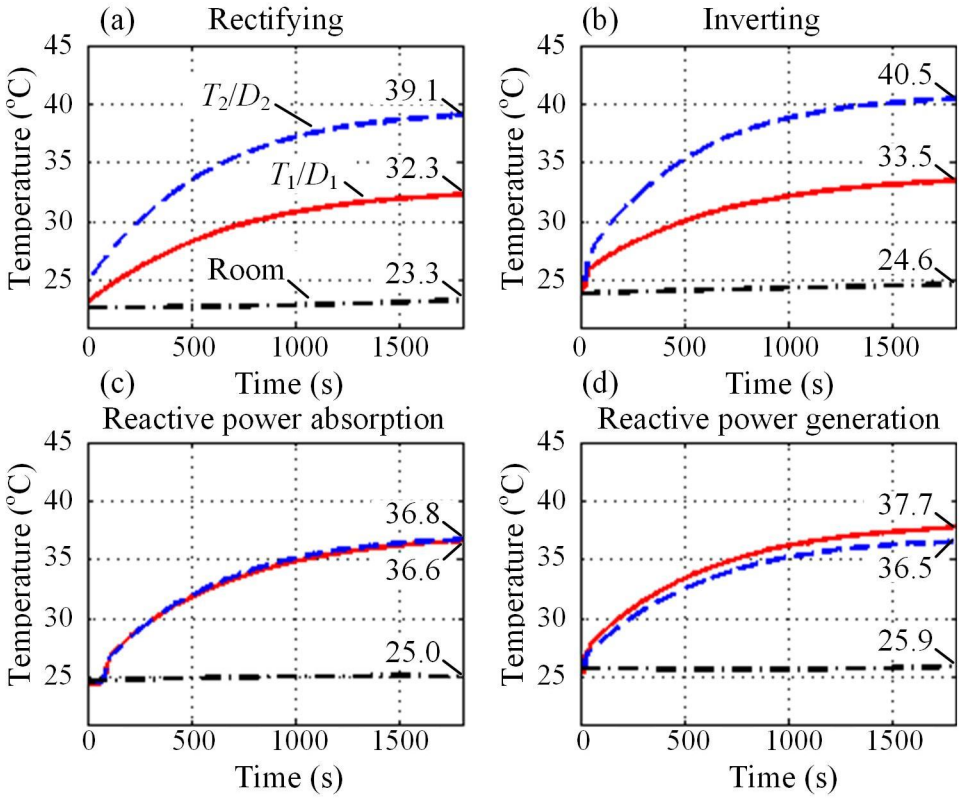

Figure 6.21: Results of electro-thermal test 2: temperature recordings for upper and lower switches when the converter runs at (a) rectifying, (b) inverting, (c) reactive power absorption and (d) reactive power generation. The lines are upper IGBT/diode module (T_1/D_1) (solid red), lower IGBT/diode module (T_2/D_2) (dashed blue) temperatures and the room temperature (dashed-dot black)

Item	**Power loss** (simulation)	**Temp.**[a]	**Power loss** (simulation)	**Temp.**[a]
	Upper module (T_1/D_1)		Lower module (T_2/D_2)	
Rectifying	1.87 W	9.0 ºC	3.45 W	15.8 ºC
Inverting	1.70 W	8.9 ºC	3.71 W	15.9 ºC
Q absorb	2.35 W	11.6 ºC	2.47 W	11.8 ºC
Q generate	2.46 W	11.8 ºC	2.31 W	10.6 ºC

[a]the device temperature subtracts the room temperature

Table 6.8: SM semiconductor devices losses comparison for electro-thermal test 2

6.8 Summary

A novel model assisted SM testing scheme for the MMC is proposed in this chapter. With the help of computer simulation, the arm current passing through the SM and its switching sequence can be recorded and used to run the experiment. As little as one SM is sufficient to run the test for electromagnetic and electro-thermal studies as well as verification of the design. A complete MMC converter is no longer required. Only one dc voltage source is needed to compensate the power losses. The energizing and discharging of the SM capacitor are achieved through the SM dc voltage regulator with no additional auxiliary charging and discharging circuits. Different from the published testing methods, in the proposed testing scheme, both the SM switching sequence and the 'arm current' can be faithfully achieved simultaneously. The 'arm current' could contain not only the fundamental frequency component but also the dc offset and the harmonic circulating current components. Both simulation and experiment show the validity and accuracy of the proposed testing scheme. The synchronization between the 'arm current' and the SM switching sequence is shown to be adequate. This testing method is showed capable of facilitating research, such as SM thermal stability test, optimal cooling system design, optimal switching pattern algorithm, novel SM structure design as well as reliability testing. It is intended to fill the gap between computer simulation and the complete converter experiment in the physics domain.

7 A COMPENSATED MODEL ASSISTED SM TESTING SCHEME FOR MMC

The previous chapter presents a model assisted SM testing scheme for the MMC. The prototype SM can be thoroughly tested without a complete MMC. During the test, the 'arm current' can be faithfully achieved, which contains not only the fundamental frequency component but also dc offset and harmonic circulating current components. However, in order to generate the current in hysteresis control, the dc supply voltage of the FB must be higher than the peak SM capacitor voltage. In some cases, the required dc supply voltage would be more than double the rated voltage of the tested SM, which calls for much higher voltage withstanding capability of the power switches in the FB converter. For tested SMs with rated voltage lower than 2 kV, the required dc supply voltage may be as high as 4 kV. In such a case, IGBT/diode power modules with higher voltage level (such as 6.5 kV) are still commercially available for the FB. However, if the SM rated voltage is higher than 2 kV,

leading to more than 4 kV dc supply voltage, none of the existing IGBT/diode power modules can be directly used. Series connection of power switches in the FB may have to be adopted to withstand the much higher dc supply voltage, leading to complex circuitry and voltage-balancing scheme.

In order to improve the testing capability of the test platform proposed in Chapter 6, this chapter proposes the use of an auxiliary SM to compensate the large dc voltage across the capacitor of the SM under test. By doing that, the dc supply only needs to be higher than the SM capacitor voltage ripple (ac variation) that is much lower than the SM rated voltage, leading to largely reduced demand of the dc supply voltage, the voltage withstanding capability of the power switches as well as the coupling inductor (inductance). The rest of the chapter is organized as follows. Chapter 7.1 introduces the basic structure of the compensated SM testing scheme and its control strategy. As the original capacitor voltage regulator in Chapter 6 has opposite effects on the added auxiliary SM, new voltage control is proposed for the auxiliary SM capacitor. Components selection to implement the current source is provided in Chapter 7.2. After that, the dc supply and coupling inductance demands of the proposed method are compared with the original. In Chapter 7.3, a design example of a test platform to test SMs up to 2000 V rated voltage is given. The testing capability of the same platform while using the original method is also presented. It shows that the proposed method can help to increase the voltage testing capability by more than 5 times with even better current tracking accuracy. Computer simulation verifies the design. In Chapter 7.4, a scaled-down prototype test platform, designed to test SMs with 400 V rated voltage and 14 A current, is built and tested experimentally. Chapter 7.5 concludes the chapter.

7.1 Basic Concept and Control Strategy

7.1.1 Basic concept and circuit diagram

The general concept of the SM testing scheme is described in Chapter 6 as shown in Figure 6.5(a). It requires a controllable current source, prototype SM(s) and signals of the 'arm current' reference as well as the switching sequence(s) for the prototype SM(s) to be tested. There are two ways to run the model assisted SM testing with online or offline simulation. In this chapter, the offline testing scheme is adopted again. The switching sequence(s) and 'arm current' signals are pre-generated and recorded through computer-aided simulation of a complete MMC using Matlab/Simulink. The recorded signals are then used to drive the current source and the prototype SM(s) directly.

Figure 7.1 gives the compensated test platform with offline simulation as proposed in this chapter. The Matlab/Simulink is used as the reference signal generator and a dSpace DS1103 as the interface between the master computer and the test platform. Similar to the uncompensated test platform, the current source consists of a FB converter and a coupling inductor. As the difference, an auxiliary SM is connected in series with the prototype SM in a reverse way. Both SMs have the same current and voltage ratings. Note that the ratings of the auxiliary SM can be higher than the prototype. With the same switching sequence, when the two SM capacitors are switched into the circuit simultaneously, the dc component in both SM output voltages will be cancelled out leaving only the small ac variations (voltage ripples). The voltage ripple of the two SMs would have the same shape but opposite polarities if identical capacitors are used. They are added together and the dc supply voltage V_s only needs to be higher than the total peak voltage ripple to achieve the hysteresis current control. As the SM capacitor voltage ripple is usually very small in MMCs, the required dc supply voltage can be much less than the SM rated voltage.

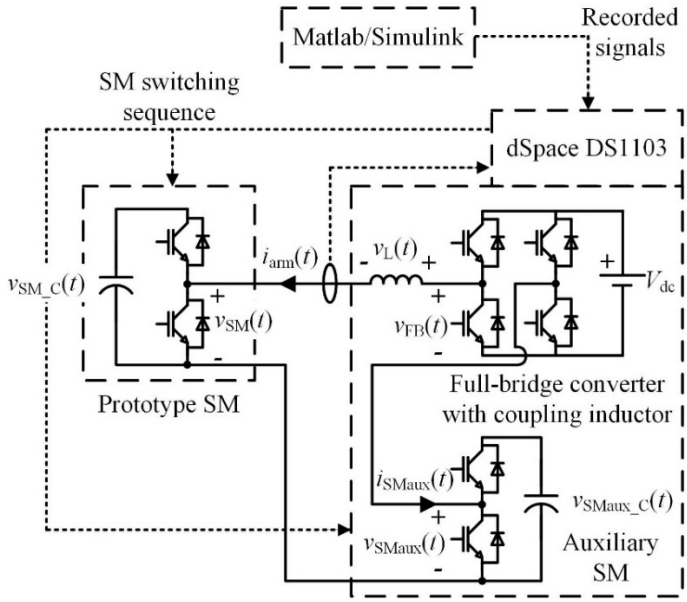

Figure 7.1: Compensated SM testing scheme with prototype SM

7.1.2 Control strategy – hysteresis control

Figure 7.2 shows the control diagram of the proposed test platform. As discussed in Chapter 6, since the PI and PR controllers for single phase inverters can only operate for a single frequency, in order to generate the desired 'arm current' with not only the fundamental but also dc offset and other low order harmonics, multiple PI or PR controllers have to operate concurrently [127-129]. As a result, the controller design is complex. In contrast, the hysteresis current control offers a simple way to track the current reference with multiple components. This method is unconditionally stable with good transient response and accuracy [130, 131]. It is therefore adopted. Simulation results show that the hysteresis current controller is adequate, and the high frequency current tracking errors introduced by the hysteresis switching have negligible impacts on the SM under test.

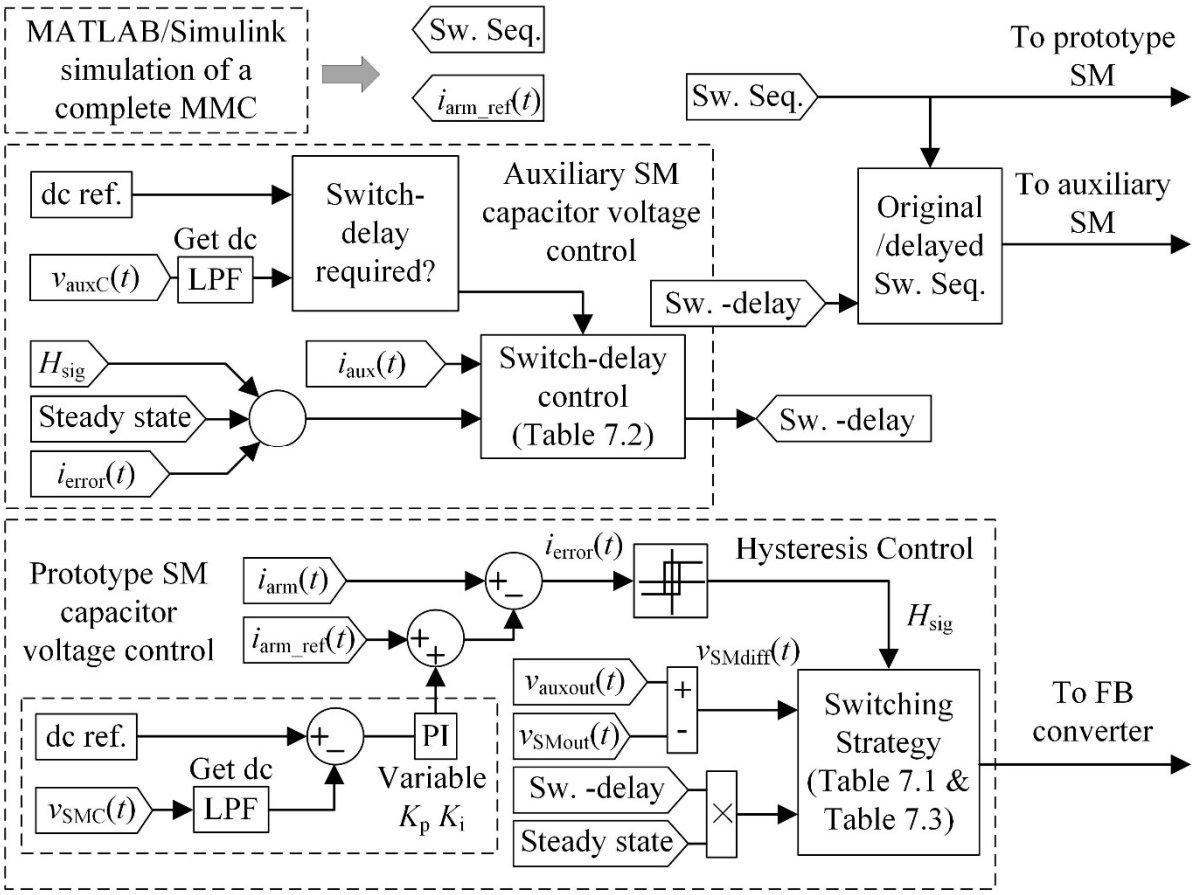

Figure 7.2: Control diagram of the compensated SM test platform

As shown in Figure 7.1, the hysteresis current control can be realized by varying the voltage on the coupling inductor through switching the FB converter. In order to limit the *di*/*dt* of the generated 'arm current', the switching of the FB shall not only consider the current tracking error $i_{error}(t)$, but also outputs of the two SMs. In order to include such effect, as shown in Figure 7.2 (the bottom dashed box), $v_{SMdiff}(t)$ is defined as the output difference of the two SMs due to the reversed-series-connection configuration. The other control variable that affects the switching of the FB is related to capacitor voltage control of the auxiliary SM. In practice, the two SMs will not be switched simultaneously for the reason to become clear later. Simultaneous switching is first assumed in analysis.

$i_{error}(t)$ is the difference between the actual 'arm current' $i_{arm}(t)$ achieved by the hysteresis

switching and its reference $i_{arm\_ref}(t)$. The hysteresis band is defined as $\pm H_{band}$. The selection of H_{band} will be discussed later. When $i_{error}(t)$ is above the hysteresis band $+H_{band}$, the output signal of the hysteresis block will be H_{sig}=1, indicating that the actual 'arm current' needs to be reduced. When $i_{error}(t)$ is below $-H_{band}$, H_{sig} will be 0, indicating that the actual 'arm current' needs to be increased.

According to Figure 7.1, the voltage on the coupling inductor $v_L(t)$ is

$$v_L(t) = v_{FB}(t) + v_{SMdiff}(t) . \tag{7.1}$$

where $v_{FB}(t)$ is the output voltage of the FB. $v_{SMdiff}(t)$ can be derived by

$$v_{SMdiff}(t) = v_{auxout}(t) - v_{SMout}(t) \tag{7.2}$$

where $v_{auxout}(t)$ is the output voltage of the auxiliary SM and $v_{SMout}(t)$ the output voltage of the prototype (see Fig.3 for reference directions). When the capacitor of the auxiliary or the prototype SM is switched into the circuit, the output voltage $v_{auxout}(t)$ or $v_{SMout}(t)$ is about the capacitor voltage $v_{auxC}(t)$ or $v_{SMC}(t)$. When the SM is bypassed, the output voltage is approximately zero.

The switching strategy of the FB converter is simple when both SMs are bypassed. In such a case, the FB will output either $+V_s$ or $-V_s$ when the 'arm current' is too small or too large. When the two SMs are switched into the circuit, as (7.1) shows, the inductor voltage is a combined effect of both the FB output and the outputs of the SMs. When the actual 'arm current' is too small and needs to be increased (H_{sig}=0), $v_L(t)$ must be positive. One way to generate the positive $v_L(t)$ is through switching the FB to have $v_{FB}(t)=V_s$. This applies when $v_{SMdiff}(t)$ is negative or positive but with small amplitude. As $v_{SMdiff}(t)$ further increases, the total voltage ripple of the two SM capacitors is enough to increase the 'arm current' at a comparable rate. In such a case, the FB converter will only output zero voltage to limit the value of $v_L(t)$, which helps to limit the di/dt of the current and also the switching frequency.

As a result, the coupling inductance can be very small and the switching frequency of the FB would only vary in a small range. The threshold voltage to decide whether the FB converter shall output V_s or 0 is defined as V_{thres}. The situation is similar when the actual 'arm current' is too large and needs to be reduced (H_{sig}=1). Due to symmetry, the threshold voltage in this case will be $-V_{thres}$. Detailed output strategies for the FB converter are concluded in Table 7.1.

Prototype and auxiliary SMs are simultaneously switched in/out			
i_{arm} is too small (H_{sig} = 0)		$v_{SMdiff}(t) < V_{thres}$	$v_{SMdiff}(t) \geq V_{thres}$
	$v_{FB}(t)$	$+V_s$	0
	$v_L(t)$	$V_s+v_{SMdiff}(t)$	$v_{SMdiff}(t)$
i_{arm} is too large (H_{sig} = 1)		$v_{SMdiff}(t) \leq -V_{thres}$	$v_{SMdiff}(t) > -V_{thres}$
	$v_{FB}(t)$	0	$-V_s$
	$v_L(t)$	$v_{SMdiff}(t)$	$-V_s+v_{SMdiff}(t)$

Table 7.1: Output strategy for the FB converter (I)

One way to select the threshold voltage V_{thres} for the FB converter to output zero voltage is to ensure that the changing rate of the current is faster than in the case when the FB outputs $\pm V_s$. For instance, when $i_{arm}(t)$ is too small and needs to be increased (H_{sig}=0), the slowest rising rate of $i_{arm}(t)$ in the case when $v_{FB}(t)=V_s$ corresponds to the minimum coupling inductor voltage as

$$V_{Lmin} = V_s + V_{SMdiffmin} \tag{7.3a}$$

$$V_{SMdiffmin} = -\left(\hat{V}_{SMCac} + \hat{V}_{auxCac}\right) \tag{7.3b}$$

where $\hat{V}_{SMCac}$ and $\hat{V}_{auxCac}$ are the amplitudes of the prototype and the auxiliary SM capacitor voltage ripples respectively. For simplicity, the capacitor voltage ripple is assumed symmetrical around its time average (dc component). The small difference between the positive and negative peaks is neglected. Two parameters, k_{SMCac} and k_{auxCac} are defined as the ratio between the peak-to-peak voltage ripple and the rated dc voltage. That is

$$k_{\text{SMCac}} = \frac{2\hat{V}_{\text{SMCac}}}{V_{\text{SMCdc}}} \tag{7.4a}$$

$$k_{\text{auxCac}} = \frac{2\hat{V}_{\text{auxCac}}}{V_{\text{auxCdc}}} \tag{7.4b}$$

where V_{SMCdc} and V_{auxCdc} are the rated dc voltage of the prototype and the auxiliary SM capacitors respectively. In order to achieve better voltage cancellation effect, the rated dc voltage of the auxiliary SM is set to be equal to that of the prototype, i.e.

$$V_{\text{auxCdc}} = V_{\text{SMCdc}}. \tag{7.5}$$

As stated above, when the FB converter outputs zero voltage, the minimum coupling inductor voltage would be equal to V_{thres}. The selection of V_{thres} must be large enough so that the rising rate of $i_{\text{arm}}(t)$ is faster than the slowest case given by (7.3a). On the other hand, since the maximum inductor voltage will be (V_{thres}+V_{s}) when $v_{\text{FB}}(t)$=V_{s}, V_{thres} needs to be chosen as small as possible to limit the maximum current step. Hence, a suitable value for V_{thres} can be derived by substituting (7.3b), (7.4a) and (7.4b) into (7.3a)

$$V_{\text{thres}} = V_{\text{s}} - \frac{1}{2}\left(k_{\text{SMCac}} + k_{\text{auxCac}}\right)V_{\text{SMCdc}} \tag{7.6}$$

where V_{auxCdc} equals V_{SMCdc} when needed.

Due to symmetry, the negative threshold voltage is set at $-V_{\text{thres}}$. In some cases, when both capacitor voltage ripples are so small that the threshold voltage is never met, the FB converter will always output $\pm V_{\text{s}}$.

7.1.3 Control strategy – capacitor voltage control

As discussed in Chapter 6, in steady state, theoretically, time average (dc component) of a SM capacitor voltage will be constant for any given 'arm current' and switching sequence from computer simulation. In practice, due to the switch-ON deadband, non-ideal characteristics of power switches, and current tracking error of the hysteresis control, the

capacitor dc voltage may not be balanced anymore. Certain controllers are required to regulate the capacitor dc voltage. The prototype SM uses the voltage regulator proposed in Chapter 6 through injecting small compensation current into the 'arm current'. The value of the injected current is derived by a PI controller with variable gains. Details of this controller can be found in Chapter 6.2.2.

For the auxiliary SM, however, the aforementioned voltage regulator will have opposite effects on its capacitor dc voltage $v_{auxCdc}(t)$ due to the reversed-series-connection configuration. Positive injected current will actually reduce $v_{auxCdc}(t)$. To solve this problem, Figure 7.3 shows a switch-delay control for the auxiliary SM, which is independent from the prototype SM voltage regulator. The top graph is the current flowing into the auxiliary SM $i_{aux}(t)$ (see Figure 7.1) and the bottom shows its switching sequence, where '1' stands for SM switched-in and '0' means SM bypassed. ΔT is the sampling period of the test platform. When $i_{aux}(t)$ is positive, if a switch-ON delay is applied, the capacitor will not get charged during the delay period, and if a switch-OFF delay is applied, the capacitor will get further charged. In the other case, when $i_{aux}(t)$ is negative, the capacitor will be discharged less or get further discharged if switch-ON or –OFF delay is applied.

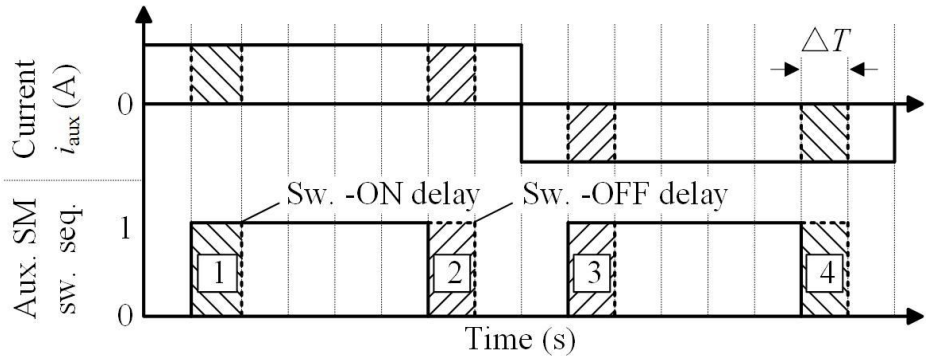

Figure 7.3: Auxiliary SM (aux. SM) capacitor voltage regulator using switch-delay control

Note that when the switching of the auxiliary SM is delayed, the two SMs will be no longer switched simultaneously. $v_{SMdiff}(t)$ will equal to one full SM capacitor voltage, either $v_{SMC}(t)$ or $v_{auxC}(t)$, which is usually much higher than V_s. In such a case, the FB converter will not be able to control the 'arm current' $i_{arm}(t)$ and the dynamics of $i_{arm}(t)$ will be dominated by $v_{SMdiff}(t)$. For instance, when $v_{auxCdc}(t)$ is too high, switch-OFF delay can be applied when $i_{aux}(t)$ is negative to get further discharged. At this moment, only the auxiliary SM capacitor is connected in the circuit and $v_{SMdiff}(t)$ equals $v_{auxC}(t)$ according to (7.2). As V_s is always smaller than $v_{auxC}(t)$, $i_{arm}(t)$ tends to increase in any event. In order to ensure that the current error is always within the allowable band in steady state, the switch-OFF delay can only be applied when $i_{arm}(t)$ actually needs to be increased (H_{sig}=0), and the current tracking error $i_{error}(t)$ is less than a threshold current I_{thres-}. I_{thres-} is usually negative and is set to leave enough margin for $i_{error}(t)$ to increase. If the permitted maximum current tracking error is defined as ΔI_{max} and the maximum current change of $i_{error}(t)$ during a switch-delay period is dI_{error_delay}. The current threshold can be derived as

$$I_{thres-} = \Delta I_{max} - dI_{error\_delay}. \tag{7.7a}$$

In the same case [$v_{auxCdc}(t)$ is too high], when $i_{aux}(t)$ is positive, the switch-ON delay can be applied and the auxiliary SM capacitor will not be charged during the delay period. At this moment, $v_{SMdiff}(t)$ would equal to $-v_{SMC}(t)$ and $i_{arm}(t)$ tends to decrease in any event. Hence, the switch-ON delay can only be applied when $i_{arm}(t)$ actually needs to be reduced (H_{sig}=1) and $i_{error}(t)$ is higher than a positive threshold current I_{thres+}. Similar to (7.7a), the value of I_{thres+} can be derived by

$$I_{thres+} = -\Delta I_{max} + dI_{error\_delay}. \tag{7.7b}$$

Detailed switch-delay strategies for the auxiliary SM are concluded in Table 7.2. As the conditions in the brackets would slow down the dynamics of the voltage control, they are

only applied in steady state. In transient, the switch-delay is used whenever $v_{auxCdc}(t)$ is outside the permitted range. The period of the switch-delay is usually chosen as short as possible to limit the resulting large current error. In this chapter, it equals the sampling period ΔT (50 μs) of the test platform dSpace DS 1103.

$\boldsymbol{v_{auxCdc}(t)}$	$\boldsymbol{i_{aux}(t) \leq 0}$ (flow out)	$\boldsymbol{i_{aux}(t) > 0}$ (flow in)
Too high	Switch-OFF delay ($H_{sig} = 0$ & $i_{error}(t) < I_{thres-}$)[a]	Switch-ON delay ($H_{sig} = 1$ & $i_{error}(t) > I_{thres+}$)[a]
Too low	Switch-ON delay ($H_{sig} = 1$ & $i_{error}(t) > I_{thres+}$)[a]	Switch-OFF delay ($H_{sig} = 0$ & $i_{error}(t) < I_{thres-}$)[a]

[a] Only applied in steady state.

Table 7.2: Switch-delay strategy for the auxiliary SM

Table 7.3 offers another measure to limit the current error during the switch-delay period by compensating the large $v_{SMdiff}(t)$. The FB converter will output $-V_s$ when the switch-OFF delay is used and will output $+V_s$ when the switch-ON delay is used.

Auxiliary SM switch-delay is active (in steady state)		
$H_{sig} = 0$ Sw.-OFF delay	$v_{FB}(t)$	$-V_s$
	$v_L(t)$	$-V_s+v_{auxC}(t)$
$H_{sig} = 1$ Sw.-ON delay	$v_{FB}(t)$	$+V_s$
	$v_L(t)$	$V_s-v_{SMC}(t)$

Table 7.3: Output strategy for the FB converter (II)

7.2 Components Selection to Implement the Current Source

The primary objective of the test platform is to provide the desired 'arm current' and inject it into the prototype SM. Due to the constant switching of the SM capacitor, the load conditions of the FB converter vary frequently. Hence, in order to keep the current tracking error within an allowable range at all times, parameters of the test platform must be carefully chosen. In this section, dynamic characteristics of the 'arm current' generated by the proposed testing method are firstly analyzed and compared with the original method. Based

on the understanding of the current tracking error, a method is provided to select the coupling inductance L and the FB converter dc supply voltage V_s, which can be applied to both testing methods. After that, the component demands and testing capabilities of the two methods are compared in detail.

7.2.1 Current dynamics and tracking error

Figure 7.4 shows the measured characteristics of current and voltage waveforms of the two testing methods. The solid saw-tooth line represents waveforms for the proposed method while the dashed saw-tooth line is for the original method. When the prototype SM capacitor is bypassed (as well as the auxiliary SM capacitor in the proposed method), the coupling inductor voltage $v_L(t)$ will equal the FB output $v_{FB}(t)$ for both methods as in Figure 7.4(b) and (c). When the SM capacitor is switched in, for the original method, the inductor voltage would be equal to either the entire SM capacitor voltage $v_{SMC}(t)$ or the difference between $v_{FB}(t)$ and $v_{SMC}(t)$ depending on the current tracking error thereby leading to unsymmetrical increasing rate and decreasing rate of i_{arm}. For the proposed method, the inductor voltage in such a case would be the difference between $v_{FB}(t)$ and the total voltage ripple $v_{SMdiff}(t)$ or $v_{SMdiff}(t)$ alone in certain cases. Both the increasing rate and the decreasing rate of i_{arm} would depend on $v_{SMdiff}(t)$. For all cases, although the proposed method uses a much lower supply voltage, due to the smaller coupling inductor, the current dynamics in the two methods are similar. The last segment (waveform) for the proposed method shows the current and voltage responses during the switch-delay control. At this moment, one entire SM capacitor voltage, either the prototype or the auxiliary will be applied on the inductor. Components selection for the proposed method shall also consider the switch-delay control in order to keep the current error within the allowable bands at all times.

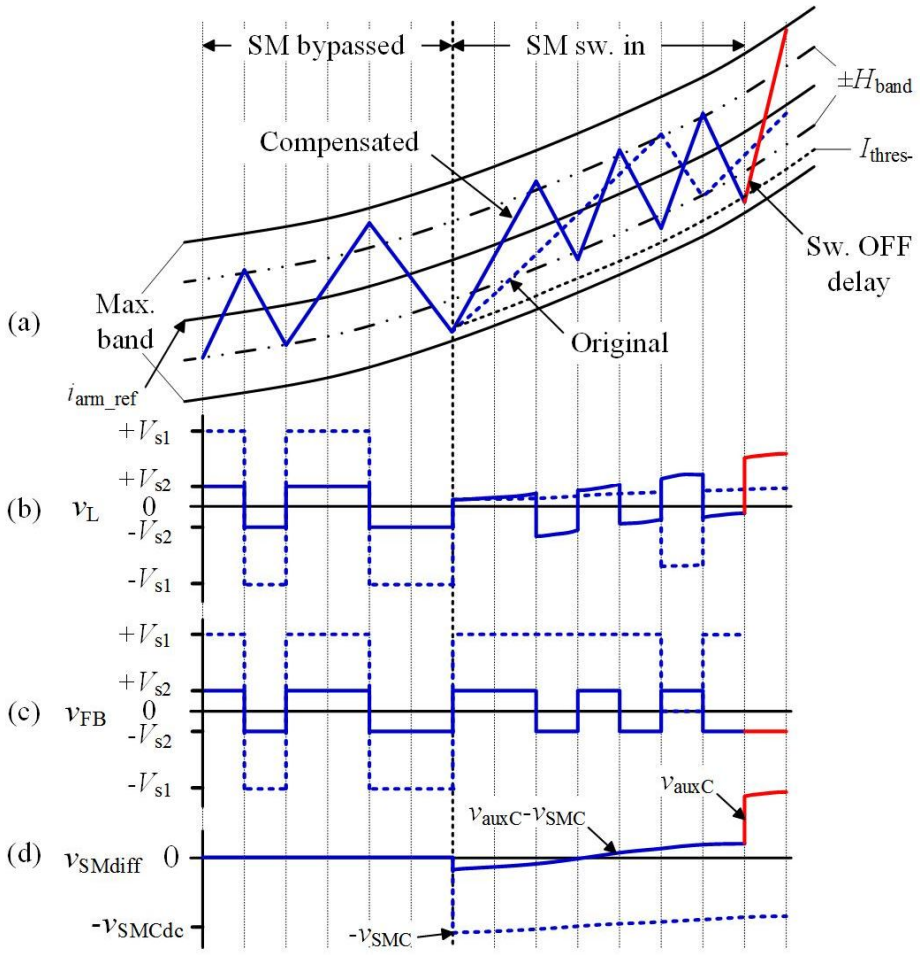

Figure 7.4: Typical current and voltage waveforms in the test bench: (a) typical 'arm current' waveforms; (b) inductor voltages (V_{s1} is the dc supply voltage for the original method and V_{s2} is for the proposed method); (c) FB converter output voltages and (d) SM output voltage difference (for the original method, v_{auxC} always equals 0)

Figure 7.5 shows a typical waveform of the current tracking error $i_{error}(t)$ when using the proposed testing method. The outermost dashed lines define the permitted current error range $[-\Delta I_{max},+\Delta I_{max}]$ that $i_{error}(t)$ must never exceed. The innermost double dashed lines are the thresholds for the hysteresis control. When $i_{error}(t)>+H_{band}$, $H_{sig}=1$ and when $i_{error}(t)<-H_{band}$, $H_{sig}=0$. Due to the limited sampling frequency f_s of the test platform, the actual current error may be much larger than the hysteresis band. That is the reason a margin is left between the outer $\pm\Delta I_{max}$ and inner $\pm H_{band}$. The minimum width of this band equals the

maximum current error step in a sampling period ΔT, i.e. dI_{error_max}. The remaining two double-dots dashed lines are the current thresholds I_{thres+} and I_{thres-} for the auxiliary SM switch-delay control.

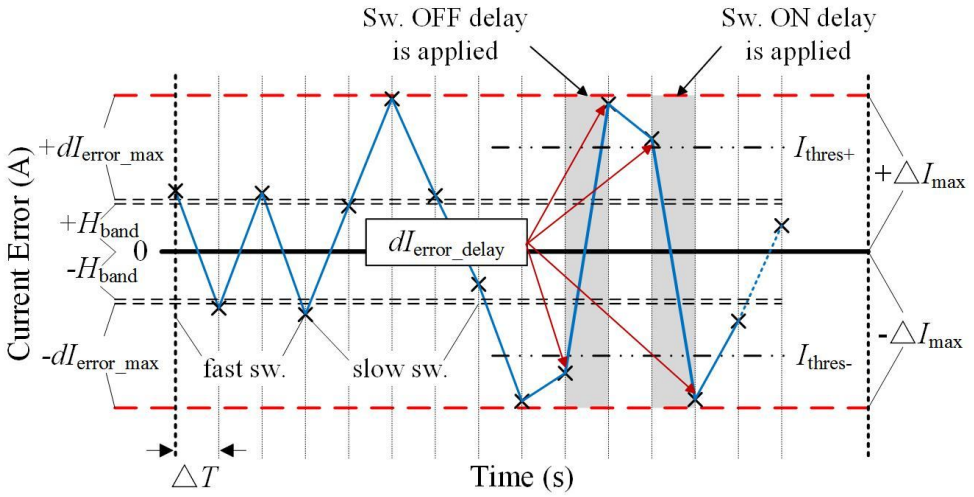

Figure 7.5: A typical waveform of the current error $i_{error}(t)$

7.2.2 Selection of control parameters

The maximum permitted current error $\pm\Delta I_{max}$ defines the current tracking performance of the test platform. One way to determine $\pm\Delta I_{max}$ is according to the resulting error in the experiment outputs, such as losses in the power switches. A detailed selection process can be found in Chapter 6.3.2.A. In order to quantify and compare the current tracking performance of different test platforms, ΔI_{max} can be written as

$$\Delta I_{max} = k_{\Delta I_{max}} A \tag{7.8}$$

where A is the peak amplitude of the fundamental component in the reference 'arm current' and $k_{\Delta Imax}$ is defined as error constant. Usually, $k_{\Delta Imax}$ is around 0.1–0.15 depending on the current tracking accuracy requirement of certain tests. The impact of different $k_{\Delta Imax}$ settings on the component selection will be detailed later.

Once the permitted current error $\pm\Delta I_{max}$ is decided, the hysteresis band $\pm H_{band}$ can be

selected. As the hysteresis band directly decides the switching of the FB converter, one design criterion of $\pm H_{band}$ is to ensure that the upper switching frequency limit of the FB (f_{sw_max}) will never be exceeded for heat dissipation and EMC reasons. As shown by the 'fast switching' in Figure 7.5, in such a case, the FB would change its output at the very sampling instant as the current error is always larger than the hysteresis band [$-H_{band}$,$+H_{band}$]. In such a case, the actual switching frequency will be half of the sampling frequency f_s. If the permitted switching frequency is lower than that value, the width of the hysteresis band must be larger than the maximum current error step dI_{error_max} in a sampling period. This can be derived as

$$dI_{error\_max} = \frac{1}{L} V_{Lmax} \Delta T + \omega A \Delta T \tag{7.9}$$

where V_{Lmax} is the maximum inductor voltage, ω the MMC ac side line frequency. Here, in estimation, the harmonic circulating current components are neglected because of their much lower amplitudes. In cases where the harmonic currents are not small, their effects shall be included. A fixed relation can be found between H_{band} and dI_{error_max} to ensure that f_{sw_max} is never exceeded as

$$H_{band} = \frac{1}{2} \left\lfloor \frac{f_s}{2 f_{sw\_max}} \right\rfloor dI_{error\_max} . \tag{7.10}$$

7.2.3 Selection of component parameters

This section will focus on the selection of the components for the coupling inductance L and the dc supply voltage V_s. Firstly, in order to ensure the current error is always within the permitted range [$-\Delta I_{max}$,$+\Delta I_{max}$], the minimum gap between $\pm\Delta I_{max}$ and $\pm H_{band}$ must equal the maximum current error step dI_{error_max}, given by

$$\Delta I_{max} - H_{band} \geq dI_{error\_max} . \tag{7.11}$$

Substituting (7.9) and (7.10) into (7.11) gives (7.12) as

$$\frac{V_{\mathrm{Lmax}}}{L} \le \frac{2\Delta I_{\max} f_{\mathrm{s}}}{2+\left\lfloor \frac{f_{\mathrm{s}}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - \omega A. \tag{7.12}$$

Note that $\Delta T=1/f_{\mathrm{s}}$. (7.12) gives the upper limit of the ratio between V_{Lmax} and L. Another design criterion is that the rising speed of the 'arm current' must be faster than its reference at any time. With the harmonic components neglected, the fastest rising speed of the reference occurs when the current crosses its dc offset from underneath. At that instant, the slope equals to ωA and (7.13) must be satisfied

$$\frac{V_{\mathrm{Lmin}}}{L} > \omega A \tag{7.13}$$

where V_{Lmin} is the minimum inductor voltage.

Due to symmetry, only the case when $i_{\mathrm{arm}}(t)$ is rising is considered. V_{Lmax} and V_{Lmin} are the maximum and minimum inductor voltage when it is positive (or absolute value). The above equations also apply when $i_{\mathrm{arm}}(t)$ is decreasing.

According to (7.3)-(7.6) and Table 7.1, V_{Lmax} and V_{Lmin} can be derived as

$$V_{\mathrm{Lmax}} = 2V_{\mathrm{s}} - \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)V_{\mathrm{SMCdc}} \tag{7.14a}$$

$$V_{\mathrm{Lmin}} = V_{\mathrm{s}} - \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)V_{\mathrm{SMCdc}}. \tag{7.14b}$$

Note that the auxiliary SM switch-delay control is assumed inactive here.

Substituting (7.14a) and (7.14b) into (7.12) and (7.13) leads to

$$\begin{aligned} \omega LA + \frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)V_{\mathrm{SMCdc}} &< V_{\mathrm{s}} \\ &\le \frac{k_{\Delta I_{\max}} f_{\mathrm{s}} LA}{2+\left\lfloor \frac{f_{\mathrm{s}}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - \frac{\omega LA}{2} + \frac{1}{4}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)V_{\mathrm{SMCdc}}. \end{aligned} \tag{7.15}$$

As the maximum value of (7.15) must be larger than the minimum, leading to the lower limit of the inductance L as

$$L > \frac{\frac{1}{2}\left(k_{\mathrm{SMCac}} + k_{\mathrm{auxCac}}\right)}{\frac{2k_{\Delta I_{\max}} f_{\mathrm{s}}}{2 + \left\lfloor \frac{f_{\mathrm{s}}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - 3\omega} \frac{V_{\mathrm{SMCdc}}}{A} \tag{7.16}$$

where $\Delta I_{\max}$ equals $k_{\Delta I\max} A$ when needed as in (8).

(7.15) and (7.16) give the criteria to choose V_{s} and L for the current source. If the platform is required to test different SMs with various specifications, the inductance can be chosen as the highest value for all cases. Then V_{s} can be decided by (7.15).

Note that, (7.14a) does not include the auxiliary SM switch-delay control. When all parameters are decided, the current thresholds $I_{\mathrm{thres+}}$ and $I_{\mathrm{thres-}}$ can be derived by (7.7a) and (7.7b). If the two thresholds are outside the permitted region $[-\Delta I_{\max}, +\Delta I_{\max}]$, the switch delay period shall be reduced or the supply voltage V_{s} shall be increased to further compensate the large inductor voltage due to the switch-delay control.

7.2.4 Component demands comparison

This section compares the component demands of the two testing methods. In this section, design parameters with subscript '1' are for the original testing method while those with subscript '2' are for the proposed compensated method. For the original method, both (7.12) and (7.13) can be also applied. The maximum inductor voltage V_{Lmax1} can be found in Figure 7.4(b) that equals the dc supply voltage V_{s1}. The minimum inductor voltage V_{Lmin1} (absolute value) would be the dc supply voltage minus the peak SM capacitor voltage. Based on the above analysis, V_{Lmax1} and V_{Lmin1} can be written as

$$V_{\mathrm{Lmax1}} = V_{\mathrm{s1}} \tag{7.17a}$$

$$V_{\mathrm{Lmin1}} = V_{\mathrm{s1}} - V_{\mathrm{SMCmax}} = V_{\mathrm{s1}} - \left(1+\frac{1}{2}k_{\mathrm{SMCac}}\right)V_{\mathrm{SMCdc}}. \tag{7.17b}$$

Substituting (7.17a) and (7.17b) into (7.12) and (7.13) gives

$$\omega L_1 A + \left(1+\frac{1}{2}k_{\mathrm{SMCac}}\right)V_{\mathrm{SMCdc}} < V_{\mathrm{s1}} \le \frac{2\Delta I_{\max} f_{\mathrm{s1}} L_1}{2+\left\lfloor \frac{f_{\mathrm{s1}}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - \omega L_1 A. \tag{7.18}$$

Also, the minimum required inductance can be derived as

$$L_1 > \frac{\left(1+\frac{1}{2}k_{\mathrm{SMCac}}\right)}{\frac{2k_{\Delta I_{\max}} f_{\mathrm{s1}}}{2+\left\lfloor \frac{f_{\mathrm{s1}}}{2f_{\mathrm{sw\_max}}} \right\rfloor} - 2\omega} \frac{V_{\mathrm{SMCdc}}}{A}. \tag{7.19}$$

The dc supply voltage and coupling inductor demand functions of the original method as in (7.18) and (7.19) have the same structure as the demand functions for the proposed method as in (7.15) and (7.16). In the following, the component demands of the two testing methods to test the same SM will be compared using the above equations. As the entire 'arm current' would pass through the coupling inductor and the FB in both testing methods, the current testing capability of two methods are assumed equal. Hence, only the required coupling inductance and the dc supply voltage of the FB are compared.

Figure 7.6 shows a group of comparisons of the required inductance between the two testing methods. The marked curves without a central line stand for the original method while the ones with a central line are for the proposed method. In all cases, the original method requires much larger inductance than the proposed one and both would increase with increasing (V_{SMCdc}/A), which is the ratio between the SM rated voltage and the peak amplitude of the fundamental component in the 'arm current'. Note that this applies only

when the harmonic circulating currents are small and can be neglected. Otherwise, the parameter A shall include not only the amplitude of the fundamental component but also other major harmonic components.

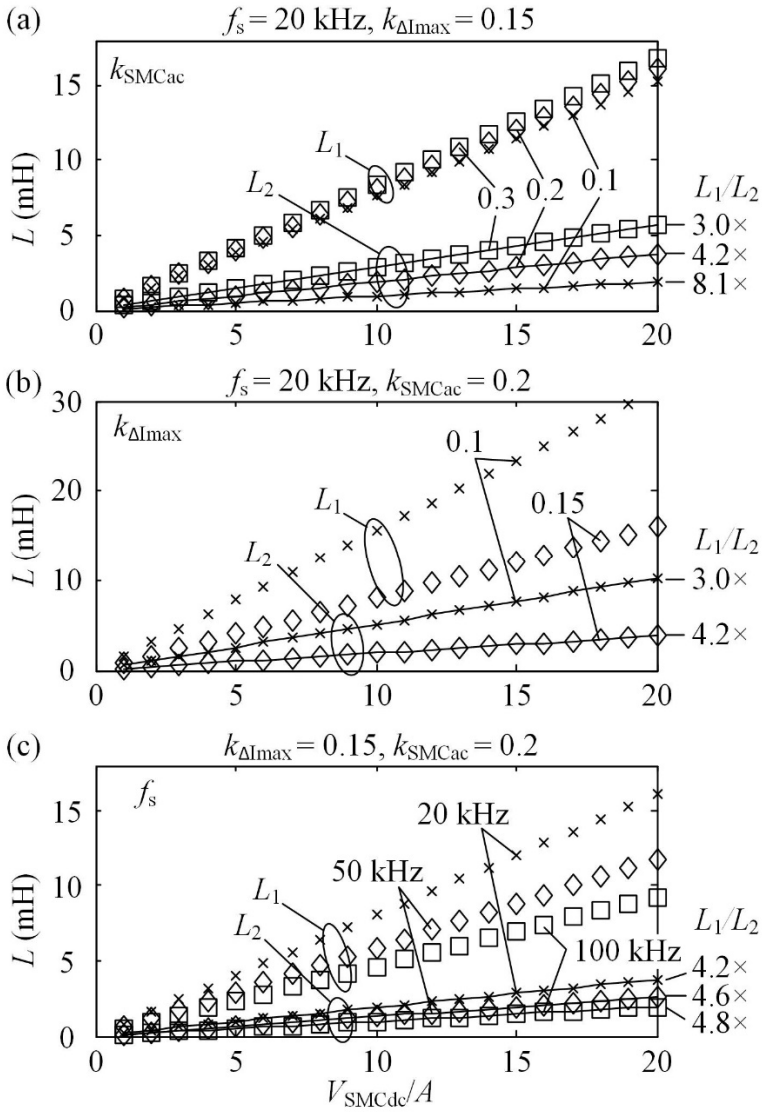

Figure 7.6: Comparison of the coupling inductance demand between the two testing methods with different (a) SM capacitor voltage ripple k_{SMCac}, (b) current tracking accuracy $k_{\Delta Imax}$ and (c) sampling frequency f_s

More specifically, Figure 7.6(a) shows how the inductance demand would vary with different SM capacitor voltage ripple, k_{SMCac}. In the proposed method, the capacitor voltage

ripple of the auxiliary SM is set equal to that of the prototype. As the voltage ripple contributes to a major part of the inductor voltage, the inductance demand is more sensitive to k_{SMCac}. Larger k_{SMCac} will call for larger coupling inductance. As a comparison, for the original method, as the entire SM capacitor voltage will be added to the coupling inductor when being switched in, the impacts of k_{SMCac} on its inductance demand is not as significant. Hence, as calculated on the right side of Figure 7.6(a), the proposed method would offer much larger inductance reduction with small voltage ripple. Figure 7.6(b) shows for both testing methods, larger inductance is needed if higher current tracking accuracy (or smaller $k_{\Delta Imax}$) is required in order to reduce the current step in each sampling period. Another way to reduce the current step is by increasing the sampling frequency f_s as shown in Figure 7.6(c). For both methods, when f_s is increased, smaller inductance is required to test SMs with the same conditions (k_{SMCac} and $k_{\Delta Imax}$). Note the maximum switching frequency of the FB is always limited at 6 kHz.

Figure 7.7 compares the dc supply voltage demand of the two methods. The vertical axis is the ratio between the required V_s and the rated voltage of the SM to be tested. The horizontal axis is the different testing configurations, including k_{SMCac}, $k_{\Delta Imax}$ and f_s. The figures on the left [Figure 7.7(a), (c) and (e)] show the supply voltage demand of the original method and the figures on the right [Figure 7.7(b), (d) and (f)] show the supply voltage demand for the proposed method with identical configurations. In all figures, the curves with 'x' symbols represent the required V_s derived when L equals the minimum value given by (7.16) or (7.19). The curves with 'o' symbols represent the case when L equals twice the minimum value. In addition, the dashed curves are for the minimum V_s and the solid curves are for the maximum V_s, as in (7.15) or (7.18).

As shown in Figure 7.7, in all considered cases, the required supply voltage of the proposed method is always lower than the SM rated voltage while the required V_s of the

original method is always higher than V_{SMCdc}. More specifically, as shown in Figure 7.7(a) and (b), the required V_s of the proposed method is more sensitive to the voltage ripple, k_{SMCac}, as larger voltage ripple calls for higher FB output voltage for the hysteresis control. In addition, as in Figure 7.7(c) and (d), higher current tracking accuracy calls for slightly higher supply voltage for both testing methods as larger coupling inductance is used to achieve the goal. As shown in Figure 7.7(e) and (f), faster sampling would help to reduce the demand of V_s for both methods. Again, the maximum switching frequency of the FB is always limited to 6 kHz.

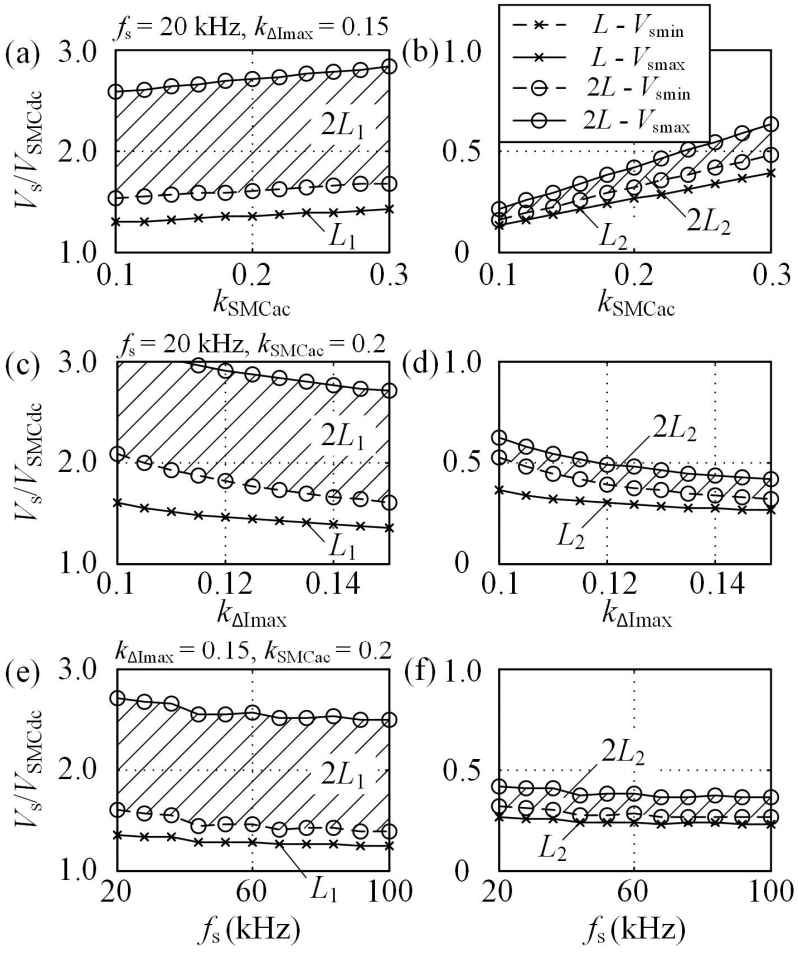

Figure 7.7: Comparison of the dc supply voltage demand between the two testing methods with different (a) and (b) SM capacitor voltage ripple k_{SMCac}, (c) and (d) current tracking error $k_{\Delta Imax}$, (e) and (f) sampling frequency f_s

7.2.5 Testing capability comparison

Figure 7.6 and Figure 7.7 compare the component demands between the two testing methods when the same SM is to be tested, showing that the proposed method requires much less coupling inductance and dc supply voltage for the same testing conditions. Figure 7.8 further compares the testing capability of the two methods when the same test equipment is used, i.e. the same dc supply and coupling inductor. The current carrying capability, the sampling frequency and the maximum switching frequency are also assumed the same. As shown in the figure, the vertical axis V_{SMCdc2}/V_{SMCdc1} is the ratio between the maximum SM rated voltage that can be tested using the proposed method and the original. V_{SMCdc1} is derived when k_{SMCac}=0.2 and $k_{\Delta Imax}$=0.15. There are two ways to calculate V_{SMCdc2}. One is by assuming the same coupling inductance as in the original. The results are shown by curves with 'x' symbols. The other is by assuming the same supply voltage (lower voltage boundary) as in the original. The results are shown by the curves with 'o' symbols. The lower value derived by the two methods is the actual maximum V_{SMCdc2}. Both Figure 7.8(a) and (b) show that the proposed method has a much higher voltage testing capability. Besides the higher voltage capability, as shown in Figure 7.8(b), the proposed method is able to offer higher current tracking accuracy with the same test platform. In both cases, the coupling inductor is the major factor that limits the testing capability improvement of the proposed method. By slightly increasing the coupling inductance, the testing capability of the same platform can be further improved (using the proposed method in this chapter).

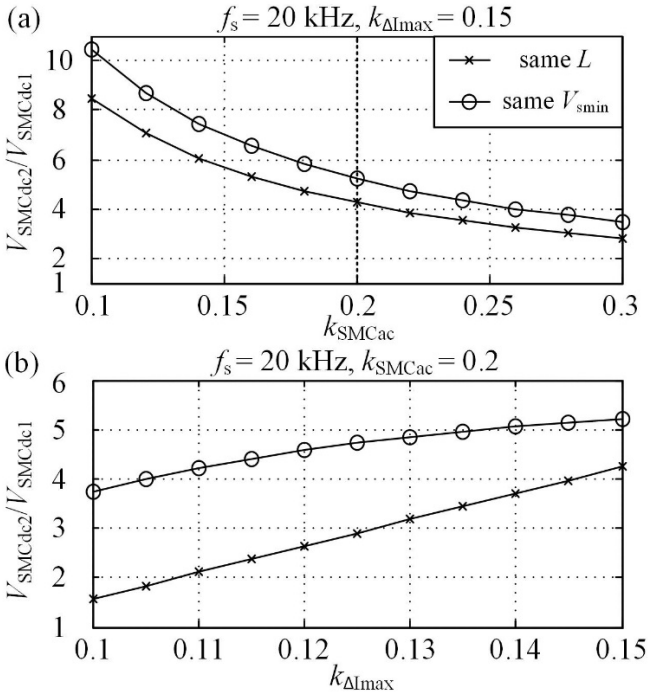

Figure 7.8: Testing capability comparison between the two testing methods with different (a) SM capacitor voltage ripple k_{SMCac} and (b) current tracking error $k_{\Delta Imax}$

7.3 Design example and simulation verification

7.3.1 Design example

This section shows a design of a test platform using the proposed method to test SMs for a hypothetic grid-connected MMC. As a comparison, the testing capability of the platform is then evaluated when the original method is used.

A hypothetic, 21-level, 19.1 MW grid-connected MMC with half-bridge SMs is modelled in Matlab/Simulink. System parameters are summarized in Table 7.4. The converter is connected to a ±20 kV dc-link and a 23 kV (line-to-line rms), 50 Hz ac grid busbar through a three-phase transformer. The arm inductor is 0.2 p.u. All p.u. values are based on ac side voltage and current. There are 20 SMs in each arm with a 2000 V SM rated voltage, V_{SMCdc}. The SM capacitance is designed to be 2.7 mF [86] to give a 15%

peak-to-peak (of V_{SMCdc}) voltage ripple at the rated power. The modulation and voltage balancing control adopt the one proposed in [19]. No third order harmonic voltage injection is used. The harmonic circulating current is assumed eliminated. The arm current can be estimated by [98]

$$i_{arm}(t) = \frac{\sqrt{2}I_s}{4} m\cos\varphi + \frac{\sqrt{2}I_s}{2}\sin(\omega t - \varphi) \tag{7.20}$$

where I_s is the rms value of the rated line current, m the modulation index and the φ the ac side power factor angle. In this design example, I_s = 500 A, m = 0.9 and $\varphi = \pi$. Hence, the design parameter A, which is the peak amplitude of the fundamental component in the arm current, can be derived to be 353.5 A.

Item	Value
dc bus voltage	40kV (pole-to-pole)
Grid voltage	23 kV line-to-line (rms), 50Hz
Rated modulation index	m = 0.9
Rated line current	500 A rms
Rated capacity	19.1 MW (PF = 1)
Transformer inductance	0.1p.u.
Number of SMs	20 per arm
Arm inductance	0.2p.u.
IGBT/Diode module	Infineon FZ1000R33HE3
V_{SMCdc}	2000 V
C_{SM}/C_{aux}	2.7 mF
k_{SMCac}	0.15
A	353.5 A

Table 7.4: Complete MMC system model parameters for simulation

Equation (7.15) and (7.16) are used to find the required supply voltage and coupling inductance for the test platform to run the SM testing with the proposed method. Sampling frequency f_s of the test platform is assumed 20 kHz and the maximum switching frequency f_{sw_max} of the power module in the FB converter is set at 6 kHz. The current error constant $k_{\Delta Imax}$ is set at 0.1 and the permitted current tracking error $\pm\Delta I_{max}$ can be derived to be ±35.4 A according to (7.8). The peak arm current would be 513 A according to (7.20). The

permitted current tracking error is less than 7% of that.

The auxiliary SM is assumed to be the same as the prototype, k_{auxCac} equals k_{SMCac}. The minimum required coupling inductance can be derived by (7.16) to be 2.2 mH. With this minimum inductance, both the maximum and minimum supply voltage equals 545 V according to (7.15). When the auxiliary SM switch-delay control is active, the maximum inductor voltage in such a case equals the difference between one peak SM voltage and V_s, which is 1605 V (=2150 V–545 V). dI_{error_delay} can be derived using (7.9) to be 42 A. Then, the current threshold I_{thres-} equals -6.6 A using (7.7a) and I_{thres+} equals +6.6 A using (7.7b). As both current thresholds are within the permitted band ±35.4 A, even when the switch-delay control is applied, the current tracking accuracy is guaranteed. In normal cases when the switch-delay is not active, dI_{error_max} can be derived to be 23.5 A using (7.9) and the hysteresis band is set to ±11.8 A using (7.10). All design parameters for the test platform using the proposed method are concluded in the second column in Table 7.5.

Item	Value	
	Proposed method	**Original method**
V_{SMCdc} (V_{auxCdc})	2000 V (2000 V)	350 V (-)
k_{SMCac} (k_{auxCac})	0.15 (0.15)	0.15 (-)
A	353.5 A	353.5 A
$k_{\Delta Imax}$	0.1	0.1
f_s	20 kHz	20 kHz
f_{sw_max}	6 kHz	6 kHz
V_s	545 V	545 V
L	2.2 mH	1.51 mH
V_{Lmax}	790 V	545 V
V_{Lmin}	245 V	169 V
ΔI_{max}	±35.4 A	±35.4 A
H_{band}	±11.8 A	±11.8 A
dI_{error_max}	23.5 A	23.5 A
dI_{error_delay}	42 A	-

Table 7.5: Test bench model parameters for simulation

As a comparison, the testing capability of the test platform with the original method is derived as follows. Firstly, as the current testing capability is limited by the current carrying

capability of the power module in the FB and the coupling inductor, the current level of the hypothetic system is assumed unchanged. Other design variables, f_s, f_{sw_max}, k_{SMCac} and $k_{\Delta Imax}$ are kept the same for comparison. One way to derive the maximum SM rated voltage V_{SMCdc1} that can be tested using the original method is to ensure that the supply voltage V_s=545 V is not exceeded. According to (7.18), the following expression must be satisfied as

$$\frac{2k_{\Delta Imax}Af_{s1}L_1}{2+\left\lfloor \frac{f_{s1}}{2f_{sw\_max}} \right\rfloor} - \omega L_1 A \le V_{s2} = 545 . \tag{7.21}$$

Equation (7.21) gives the maximum coupling inductance (L_1=1.51 mH) for the original method, which is less than the required inductance for the proposed method. In practice, the different inductance settings can be achieved by certain configurations, such as tap-changing mechanisms. Substituting L_1=1.51 mH into (7.18) gives V_{SMCdc1} to be 350 V, which is only 17.5% of the voltage that can be tested with the proposed method. The rest of the design parameters of the platform using the original method are derived and listed in the third column in Table 7.5. The hypothetic MMC model is scaled down to ±7 kV dc, 3.34 MW with the rated line current kept at 500 A in order to derive the reference signals for the 350 V rated SM. In steady state, when the two converters operate at their rated power, signals with a duration of one second for both the arm current and switching sequence of one SM in each system are recorded and then used to run the two test bench models respectively.

7.3.2 Simulation results

Figure 7.9 shows the simulation results of the test platform testing a 2000 V rated SM using the proposed method. Figure 7.9(a) shows the system startup with both the prototype SM (red solid line in the middle) and auxiliary SM (green dashed line) capacitor voltages ramping up according to a reference from 0 to 2000 V using the voltage controllers proposed in Chapter 7.1.3. During the charging process, positive injection current will be added to the

'arm current' reference to increase the prototype SM capacitor voltage. As this current injection would have opposite effects on the auxiliary SM capacitor, the ramping speed of v_{auxC} is slower than v_{SMC}. That is the reason why the longer switch-delay period for the auxiliary SM capacitor voltage control is needed during system startup. After the time averages of both v_{SMC} and v_{auxC} reach the set reference (2000 V), the platform switches to the steady-state control according to Table 7.1 to 7.3. During steady state, detailed SM capacitor voltages can be found in Figure 7.9(b). The figure shows that the prototype SM capacitor voltage achieved in the test platform (solid red) perfectly agrees with its reference recorded from the complete model simulation (solid blue). The dashed green line is the capacitor voltage of the auxiliary SM, which has an identical shape as the prototype but opposite polarity. Its average voltage is well controlled to be at the 2000 V reference using the switch-delay control. Figure 7.9(c) shows that the actual 'arm current' generated by the hysteresis switching (red in the back) tightly tracks its reference (blue in the front). Total harmonic distortion (THD) of the reference is 2.24% while that of the actual 'arm current' is 5.21%. The additional harmonics are due to the hysteresis switching.

Figure 7.10(a) shows the injected current to control the prototype SM capacitor voltage. During the system startup, large current is added to the 'arm current' reference to increase v_{SMC}. When the system reaches steady state, the injected current drops down to less than 0.2 A to compensate the small voltage difference caused by current errors. Figure 7.10(b) shows the current tracking error during both system startup and steady state. During the system startup, the switch-delay period is set to 100 μs and the delay control is applied whenever v_{auxCdc} is outside the permitted range for fast response, leading to very large current tracking error. When the system turns to the steady-state control at 2.3 s, the current error immediately reduces to within the permitted range [-35.4 A, +35.4 A]. Figure 7.10(c) shows a zoomed view of the current error. Even when the switch-delay is applied, the current error

is always within the permitted region.

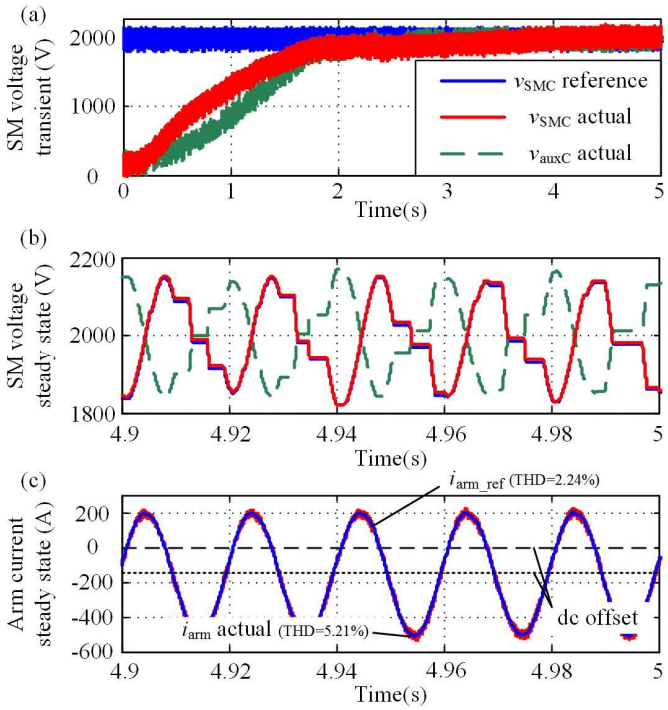

Figure 7.9: Simulation results of the test platform using the proposed method: (a) SM capacitor voltages, (b) SM capacitor voltages in steady state, (c) arm current in steady state

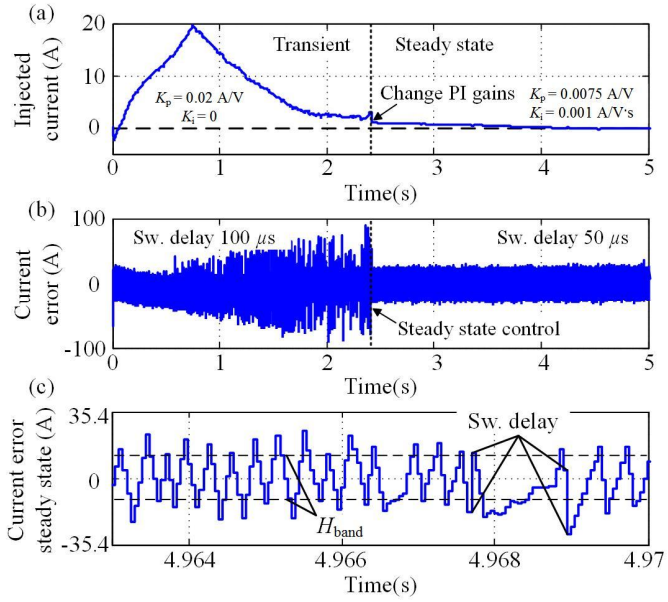

Figure 7.10: Simulation results of the test platform using the proposed method: (a) injected current, (b) current error and (c) current error in steady state

As shown in Table 7.5, with the same test platform, the original method is only able to test SMs with rated voltage up to 350 V. Figure 7.11 compares the current tracking error between simulations using the proposed and the original methods. The SM rated voltage in the simulation of the original method is set to 350 V. Both the 'arm current' and current tracking accuracy are set the same as in the simulation of the proposed method. As shown by the figure, the current errors in Figure 7.11(a) are smaller than those in Figure 7.11(b). Similar results can be found in the harmonic analysis of the current. THD of i_{arm} generated by the proposed method is 5.21% while the THD of its reference i_{arm_ref} is 2.24%. As a comparison, THD of i_{arm} generated by the original method is 5.45% while the THD of its reference i_{arm_ref} is only 1.85%. In other words, even with the same current tracking accuracy setting, the proposed method gives better current tracking performance.

The reason can be explained by Figure 7.12. The vertical axis is the actual inductor voltage divided by the maximum inductor voltage, V_{Lmax1} or V_{Lmax2} for normalization. As shown in Figure 7.12(a), when using the proposed method, the maximum inductor voltage is only met when both SMs are switched into the circuit and their voltage ripples are at the maximum. During the rest of the time, $v_{L2}(t)$ is always less than V_{Lmax2}, leading to smaller current step and hence smaller current error. Although the switch-delay control will lead to very large inductor voltage and large current step, the control only applies in limited situations as in Table 7.2 in steady state. The impacts are negligible. As a comparison, as shown in Figure 7.12(b), when the original method is used, the maximum inductor voltage is met each time when the SM is bypassed. Hence, for around half of the time (SM bypass period, depending on specific control), $v_{L1}(t)$ equals V_{Lmax1} and the current step would be equal to the maximum, leading to a large current error.

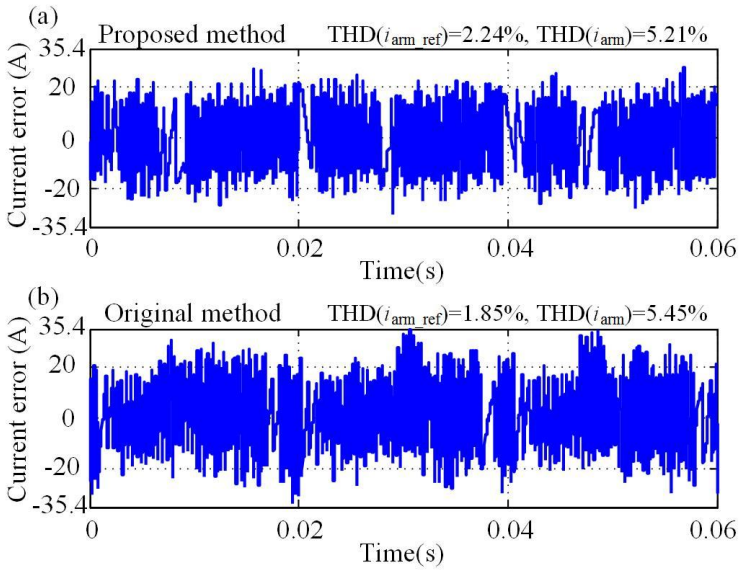

Figure 7.11: Current error comparison between the proposed method and the original method

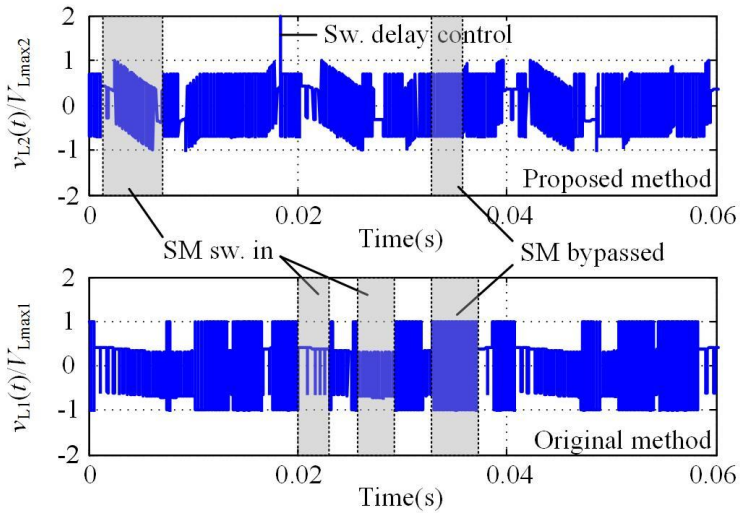

Figure 7.12: Inductor voltage comparison between the proposed method and the original method

7.4 Experiment Verification

A prototype test platform is built to verify the validity and accurarcy of the compensated model assisted SM testing scheme. Parameters in the experiment are listed in Table 7.6. Both the FB converter and the dc power supply are the same as the ones used in Chapter 6. According to the components selection in Chapter 7.2, the dc power supply is set to 100 V and the coupling inductance equals 10 mH. Note the actual inductance is chosen to be twice of the minimum value given by (7.16) (L_{min}=5 mH) in order to limit the large current error introduced by the auxiliary SM switch-delay control. Figure 7.13 shows a picture of the new SM board. Both the RC deadband circuit and the gate driver are integrated on the board to enhance the anti-interference ability and improve the switching performance. Details of the RC deadband circuit and gate driver design can be found in Chapter 6.5. Both the prototype SM and the auxiliary SM have two IXYS IXA37IF1200HJ IGBTs mounted on the back of the PCB board. The current measurement board is the same as the one used in Chapter 6 with -70 A to 70 A measurement range. The voltage measurement boards are based on the LEM LV 25-P voltage transducer. The primary side resistor is 40 kΩ (10 W) and the measurement range is from -560 V to 560 V.

Figure 7.14 shows a picture of the prototype and auxiliary SMs mounted on a test board. Figure 7.15 shows the prototype test platform assembled and installed in a protective enclosure. Figure 7.16 shows an oscilloscope snapshot of the experiment results. From top to bottom are the waveforms for the SM capacitor voltages (blue – prototype SM and red – auxiliary SM), the generated ‘arm current’ in yellow and the prototype SM switching sequence in green. The time average voltages for both SM capacitors are measured to be around 400 V. The dc offset can be clearly seen in the ‘arm current’ generated by hysteresis switching.

Item	Type	Parameters
Dc power supply	Magna-Power Electronics	Rated: 600 V_{max}; 20 A; Set at 100 V
FB converter	SEMIKRON SK35GD126ET	Rated: 1200 V; IGBT 32 A, diode 23 A at 80 °C
Coupling inductor	Hammond Manufacturing	Rated: 10 mH; 20 A_{dc}
SM rated dc voltage		400 V
Prototype SM capacotor	EPCOS B25620-B1427-A101	Rated: 420 μF; 1100 V_{dc}; Actual: 373 μF
Auxiliary SM capacitor	WIMA DCP6-I0-6780-E000	Rated: 780 μF; 600 V_{dc}; Actual: 759 μF
SM power module	Two IXYS IXA37IF1200HJ	Rated: 1200 V; IGBT 37 A, diode 25 A at 80 °C
Interface	dSpace DS1103	f_s=20 kHz
Voltage transducer	LV 25-P	-560 V to 560 V
Current transducer	LA 55-P	-70 A to +70 A

Table 7.6: Parameters for experiment

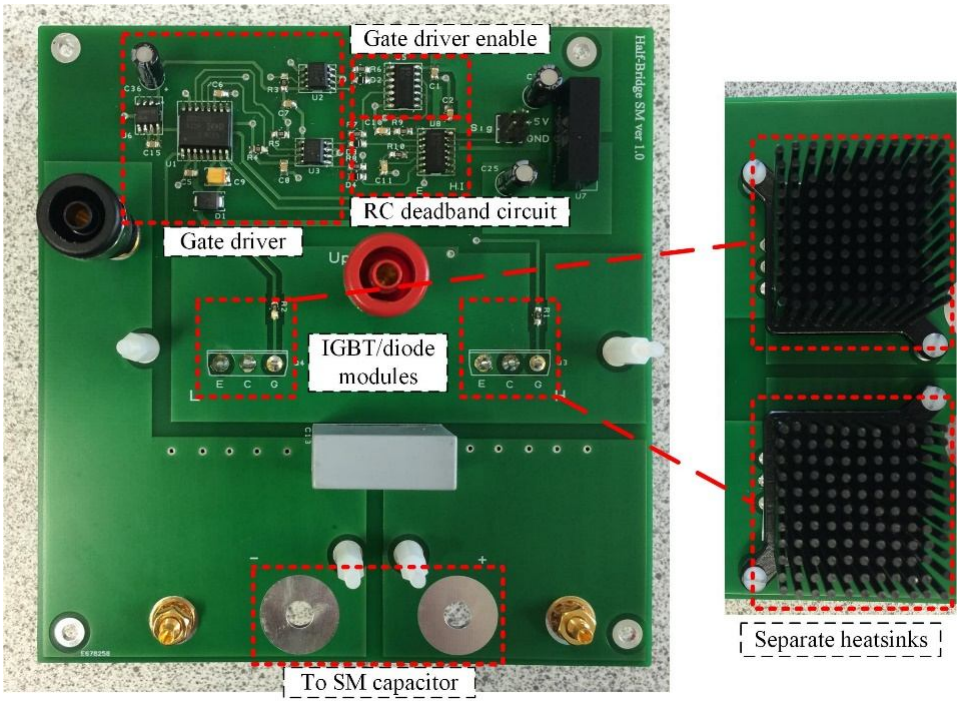

Figure 7.13: SM board (2nd version) with onboard gate driver and RC deadband

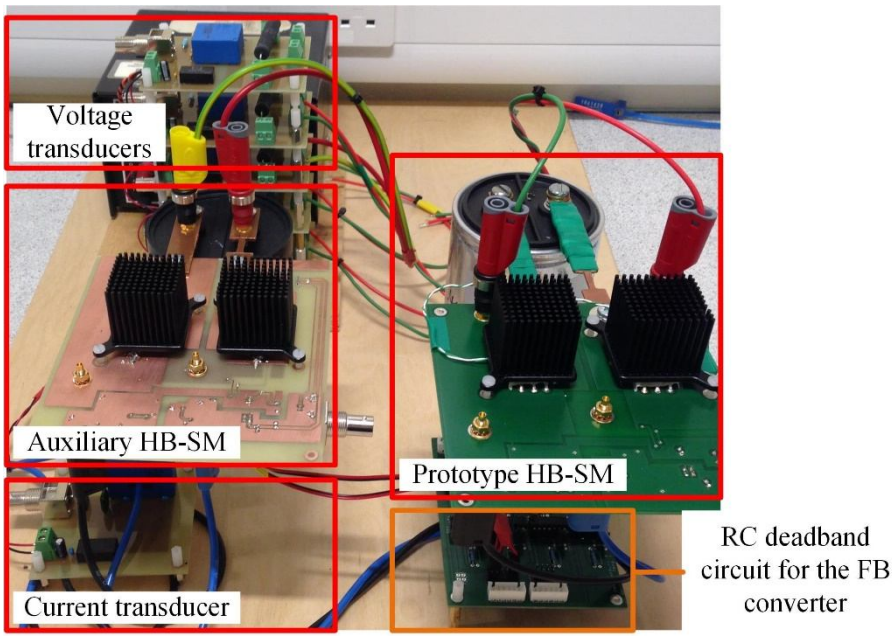

Figure 7.14: Prototype and auxiliary SMs mounted on a test board

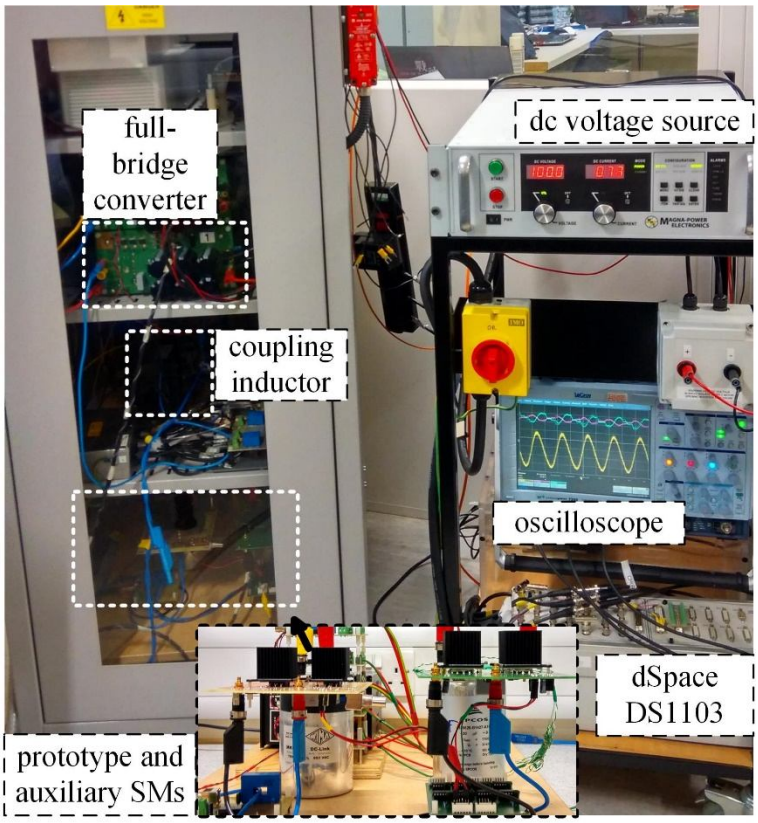

Figure 7.15: Prototype test platform installed in a protective enclosure

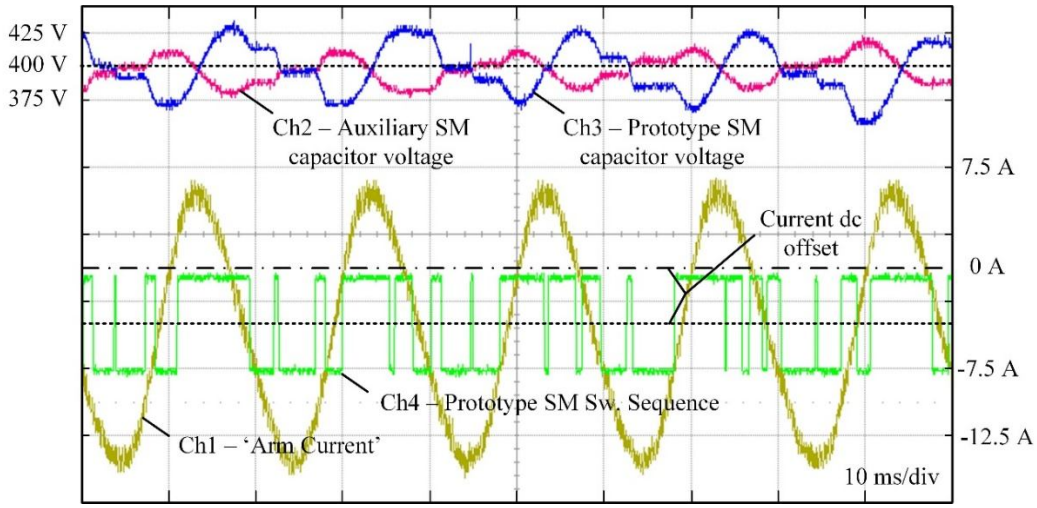

Figure 7.16: Experiment results recorded by the oscilloscope. Horizontal Axis: 10 ms/div. Ch1-'arm current': 5 A/div, -0.5 div offset (yellow). Ch2-auxiliary SM capacitor voltage: 50 V/div, -5.5 div offset (red). Ch3-prototype SM capacitor voltage: 50 V/div, -5.5 div offset (blue). Ch4-prototype SM switching sequence (green)

In order to show the performance of the test platform, Figure 7.17 compares the experimental results to the complete model simulation. Figure 7.17(b) shows the current flowing into the prototype SM tightly tracks the given reference from the computer simulation. The two zoomed views give the details of the actual 'arm current' achieved by the hysteresis switching. Owing to the excellent current tracking performance as well as accurate switching of the prototype SM, its capacitor voltage in the experiment also tightly tracks the reference given by the complete model simulation as in Figure 7.17(a). As both the voltage and current of the prototype SM perfectly agree with the simulation results of a complete system, the other output characteristics of the SM, including electro-thermal, electro-mechanical and electromagnetic characteristics would be representative of the SM installed in a complete MMC. Figure 7.17(c) shows the actual injected current by the prototype SM capacitor voltage regulator. As in the steady state, K_i (=0.01 A/V·s) is set large with very small K_p (=0.002 A/V) to filter out high frequency noises, the injected current is nearly dc with a magnitude around -130 mA, which is less than 1% of the peak 'arm current'.

Current tracking errors are shown in Figure 7.17(d) and (e). In all cases, the current errors are controlled to be within the allowable ±1.4 A region. As shown in the zoomed view in Figure 7.17(e), when the switch-delay is not active, the current error steps are always less than the designed 0.93 A. When the switch-delay is being used, the current error step is measured to be 1.7A. Owing to the control method given in Table II, the current error in such a case is still kept in the allowable region.

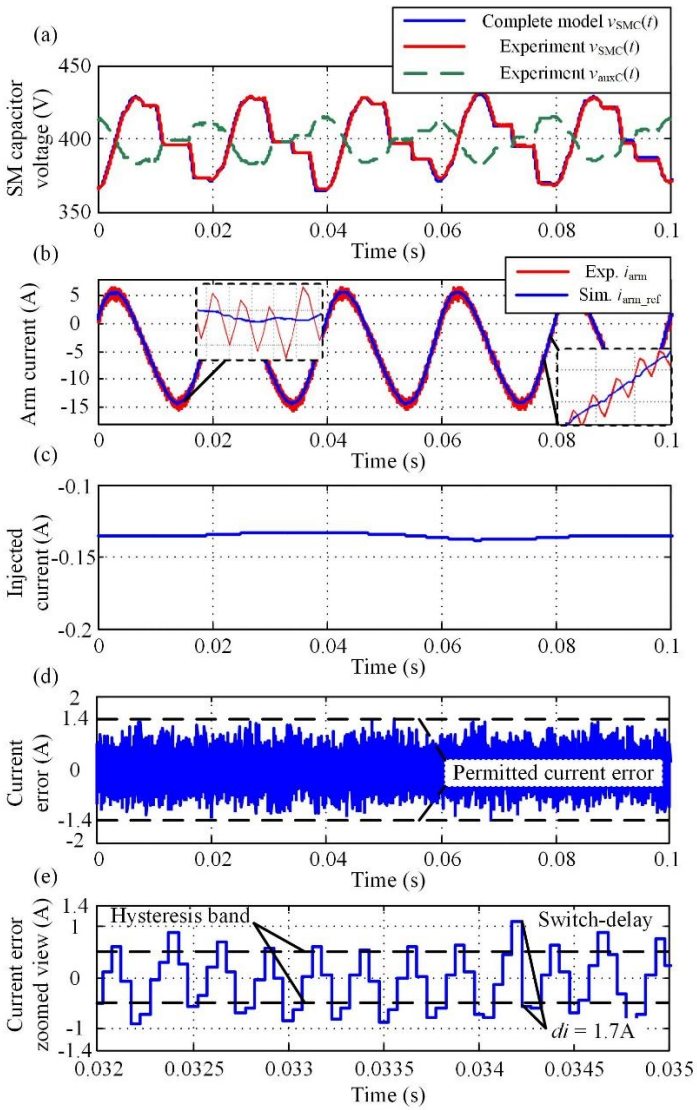

Figure 7.17: Comparison between experiment and complete model simulation: (a) SM capacitor voltages; (b) 'arm current'; (c) injected current; (d) current error; and (e) zoomed view of the current error

Figure 7.18 gives the fast Fourier transform (FFT) analysis of the current error. The high order harmonics mainly distribute around 3.7 kHz due to the hysteresis switching. As shown in the zoomed view, the error at dc can be explained by the injected current that is around -130 mA in the experiment. The error at the fundamental frequency 50 Hz is around 80 mA. The current error at 100 Hz is for the harmonic circulating current component in the 'arm current'. The amplitudes of the above errors are small when compared with the peak 'arm current'. However, if those errors are not acceptable in certain applications, methods such as narrower permitted current error band, faster sampling frequency and/or variable hysteresis band could be adopted.

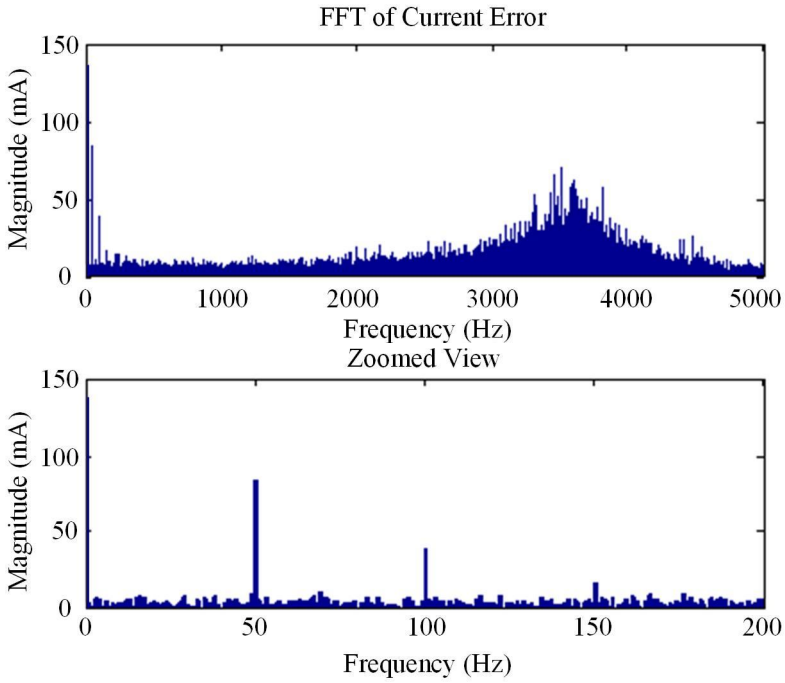

Figure 7.18: Top: FFT of the current error; bottom: zoomed view

7.5 Summary

A compensated model assisted SM testing scheme for the MMC is proposed in this chapter. This testing scheme uses an auxiliary SM to compensate the dc component in the prototype SM output voltage aiming at increasing the testing capability of the original testing method. As a result, the required coupling inductance and dc supply voltage can be largely reduced when compared with the original method to test the same SM. In addition, with the same test platform, the proposed method is able to offer much higher voltage testing capability with even better current tracking accuracy. The proposed testing method can be easily applied to the test platform design for the original method with one additional SM, which can be the same as the prototype. A new switch-delay controller is proposed to independently control the auxiliary SM capacitor voltage. The energizing and discharging of both prototype and auxiliary SM capacitors can be achieved without additional auxiliary circuits. Both simulations and experiments have shown the validity and accuracy of the proposed testing method.

8 A COMPACT MMC SM STRUCTURE WITH REDUCED CAPACITOR USING THE STACKED SWITCHED CAPACITOR ARCHITECTURE

MMCs are being actively developed for the grid connection of offshore wind or tidal farms. In order to reduce the construction and maintenance costs of the offshore converter platform, it is desirable to reduce the weight and volume of the converter system. In each MMC SM of current designs, the reservoir capacitor usually accounts for over 50% of the total volume and 80% of weight. This chapter presents a new design concept and control principle for a SM using the stacked switched capacitor (SSC) architecture. Practical considerations for a high-voltage high-power system are presented in this chapter, leading to the design of a

21-level, 40 kV (pole-to-pole dc), 19.1 MW, grid-connected SSC based MMC system, which is demonstrated experimentally on a scaled down 400 V, 12.3 A_{peak} laboratory prototype SM using the SM test bench presented in Chapter 7. It is shown that with the proposed SSC-SM, the total volume of capacitors in each SM can be reduced by more than 40% without significantly increasing the power loss.

8.1 Introduction

HVDC projects with VSCs, especially MMCs are being actively developed for offshore wind or tidal power collection and onwards transmission. Given the difficulties of constructing and maintaining an infrastructure in a harsh environment, it is important to keep the weight and size as low as possible. In the current designs of an MMC SM, the reservoir capacitor needs to absorb low order harmonics and hence accounts for over 50% of the total size and 80% of weight. For most time, the energy buffering capability of the capacitor is not well utilized. The SM capacitor needs to be large enough (capacitance) to constrain the voltage ripple, while have sufficient ripple current capability to avoid overheating. As described in Chapter 3, MPPF capacitors are commonly used in MMC SMs due to their excellent stability and high ripple current capability. It is found in [86] that when the capacitor is selected by the capacitance to satisfy the voltage ripple requirement, the ripple current capability of the selected MPPF capacitor can be twice or three times higher than needed. As a result, there is an opportunity to improve the utilization of MPPF capacitors in the MMC.

Very limited research has targeted the size reduction of the bulk SM capacitors. Increasing switching frequency is not effective in MMC SMs with HB or FB topologies, where a majority of the energy that needs to be buffered by the SM capacitor is caused by the imbalanced power between the ac and dc sides at low frequencies. A few methods were

developed [101, 135] to reshape the circulating currents within converter arms so that part of the imbalanced power can circulate at higher frequencies, resulting in lower capacitor voltage ripple. However, such methods can increase the peak arm current and thus lead to higher losses as well as increased current rating of semiconductor devices [98].

Recently proposed stacked switched capacitor (SSC) energy buffer architecture has been demonstrated to be effective in low-voltage low-power ac-dc applications for buffer-capacitor size reduction [136-138]. This chapter proposes a new MMC SM structure utilizing the SSC concept to take place of the bulk single capacitor in the original HB-SM. In an SSC based SM (SSC-SM), the SM dc bus voltage is achieved by combining several series-connected capacitors. The overall volume of all capacitors is much smaller than the original capacitor. The voltage of each capacitor can fluctuate in a wider range towards specification limits. The increased voltage ripples in different capacitors are compensated through appropriate switching strategy, to stabilize the SM dc bus voltage. With this technique, the energy density of an SSC-SM can be doubled with only 7% higher power loss at the rated power. Moreover, when the converter operates below half of the rated power for majority of the time, the SSC-SM operation reduces to a conventional SM. The additional energy losses can be further reduced.

The rest of the chapter is organized as follows. Chapter 8.2 briefly reviews the energy characteristics of MPPF capacitors. The concept of the SSC architecture is introduced in Chapter 8.3. Chapter 8.4 presents the control of the proposed SSC-SM structure. The design of a 21-level, 40 kV (pole-to-pole dc), 19.1 MW, grid-connected MMC system with SSC-SMs is presented in Chapter 8.5 together with simulation results. In Chapter 8.6, the capacity of the system is scaled down to 21-level, 8 kV (pole-to-pole dc), 92 kW for experiment. A 400 V, 12.3 A prototype SSC-SM is tested in the laboratory. In Chapter 8.7, a partial operating mode will be introduced that the SSC-SM can operate similar to a

conventional HB-SM when the converter power is low. Both simulation and experiment results for the partial operating mode are given. A discussion on the additional losses will be provided in Chapter 8.8. Chapter 8.9 concludes the chapter.

8.2 MPPF Capacitors

The SM capacitor requires large capacitance in order to buffer the imbalanced power (at low frequencies) between the ac and dc sides and ensure that the SM dc bus voltage ripple not to be excessive. Another design constraint is that it has to offer sufficient ripple current capability. The size of the SM capacitor is usually constrained by the voltage ripple, and the capacitor ripple current capability is underutilized [86].

MPPF capacitors are commonly used in MMC applications for the following reasons: (1) their characteristics are very stable over entire temperature and voltage ranges; (2) the ESR is very low at low frequencies (<1 kHz) and (3) the self-healing capability leads to satisfactory lifetime [77, 86]. Figure 3.4 shows the energy density (J/litre) versus the rated dc voltage of 240 commercial metalized film capacitors. Below 400 V, polyester film is usually used as the dielectric for lower cost, but leading to very low energy density. Above 450 V, MPPF is used and the energy density increases with the rated voltage until about 1000 V where the maximum energy density is reached (approx. 350 J/litre). The relationship between the energy density and rated voltage is useful in energy buffer design [139].

The operational principle of the proposed SSC-SM is to allow large voltage ripple on the main energy buffering capacitor, while using additional small capacitors with lower rated voltages and smaller volumes to compensate the ripple. Since larger voltage ripple on each capacitor is allowed, capacitors with smaller capacitance can be used, yielding smaller overall capacitor size and higher device utilization ratio.

8.3 Review of Stacked Switched Capacitor (SSC) Architecture

Figure 8.1 shows the general architecture of the SSC energy buffer [83], composed of series-connected backbone and supporting blocks. Each block contains one or several parallel-connected branches of switched capacitors. The capacitors are of a type that can be charged and discharged over a wide voltage range (e.g. MPPF capacitors). The switches enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer output port (v_{bus}). This design enables the voltage ripple of each individual capacitor to vary. The voltage ripple at the buffer output port is still within a narrow range through appropriate reconfiguration of the switches to select the most suitable capacitor pair in series.

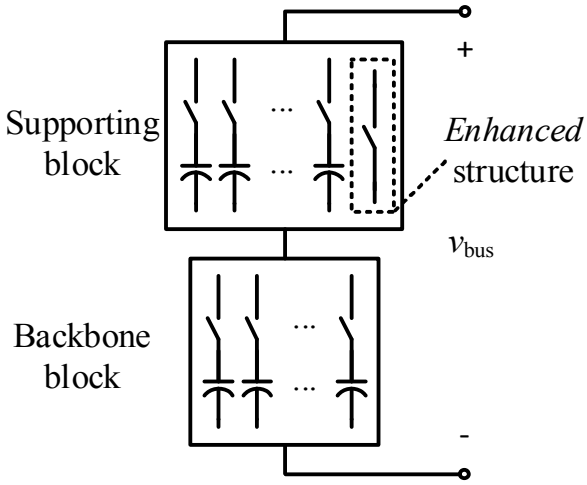

Figure 8.1: Typical structure of the SSC energy buffer

As shown in Figure 8.2, there are multiple embodiments of the SSC energy buffer [83], which can be named according to the structure, e.g. *n-m enhanced/original unipolar/bipolar* SSC energy buffer. *n-m* indicates the number of capacitor branches in the backbone and supporting blocks. *n* is usually selected between 1 or 2 while *m* can be large [83, 137, 138]. When compared with the *original* structure [Figure 8.2(a)], the only change in the *enhanced*

structure [Figure 8.2(b)] is an additional capacitor-free branch in the supporting block. By doing that, the backbone capacitor can be directly connected to the buffer output port without a supporting capacitor connected in series. According to [137, 138], the *enhanced* structure usually has higher energy density and round-trip efficiency than the *original* with the same *n-m* setting. With additional route-changing switches, as shown in Figure 8.2(c), the *bipolar* structure allows charging/discharging of supporting capacitors regardless of the current direction in the energy buffer. As a result, *bipolar* SSC designs usually have higher energy density at the costs of higher complexity and losses than the *unipolar* option [83].

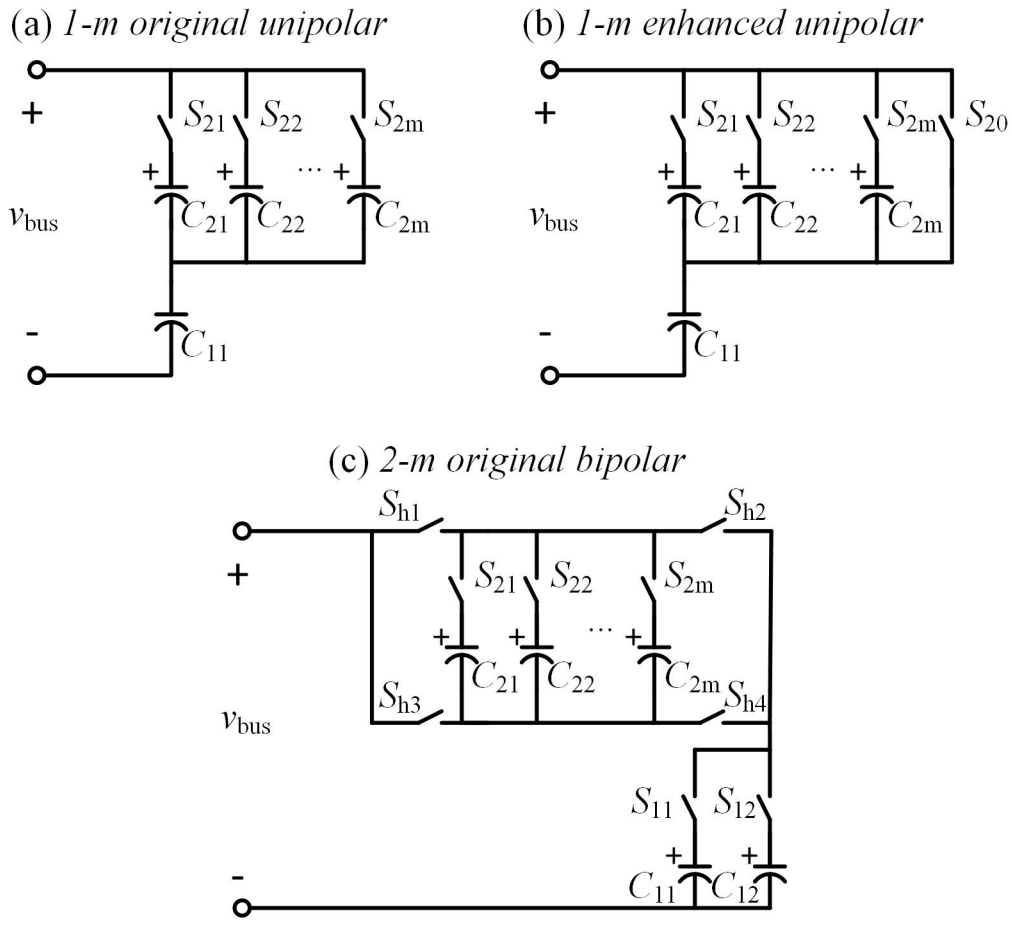

Figure 8.2: Circuit diagrams of different SSC energy buffers

The selection of the SSC architecture is a trade-off between the energy density and circuitry complexity as well as system efficiency. In high power applications where efficiency is usually the priority, the number of additional switches, especially the series connected ones must be minimized. As a result, the *1-2 enhanced unipolar* SSC architecture is selected as the topology for investigation in this chapter.

8.4 The Proposed SSC-SM: Structure, Control and Component Requirements

8.4.1 Structure of the proposed SSC-SM

Figure 8.3 compares the circuit diagram of the proposed SSC-SM against the original HB-SM. The lower switch S_L stays unchanged. S_{U1}, S_{U2_1} together with S_{U3_1} can be regarded as replacing the original upper switch S_U. The rest is the *1-2 enhanced unipolar* SSC energy buffer. There are one backbone capacitor (C_0), two supporting capacitors (C_1 and C_2) and a capacitor-free branch (S_{U3_1} and S_{U3_2}). In the rest of the chapter, the *SM dc bus voltage* (V_{bus}) refers to the total voltage of the backbone capacitor C_0 and the active supporting capacitor (C_1 or C_2 or none) that is to be/being switched in. The two additional switches (S_{U2_2} and S_{U3_2}) are connected with S_{U2_1} and S_{U3_1} in a back-to-back manner to prevent parallel connection of C_1, C_2 and the capacitor-free branch. For the reasons to become clear later the switches only slightly increase power losses and some of them are of low voltage ratings. Through advanced packaging, it is possible to integrate all switches into a single customized module. With innovative chip arrangement such as three-dimensional (3-D) packaging, the volume and weight of the new power module will be comparable with the HB design [140-142]. Hence, the increased number of semiconductors is expected to be acceptable.

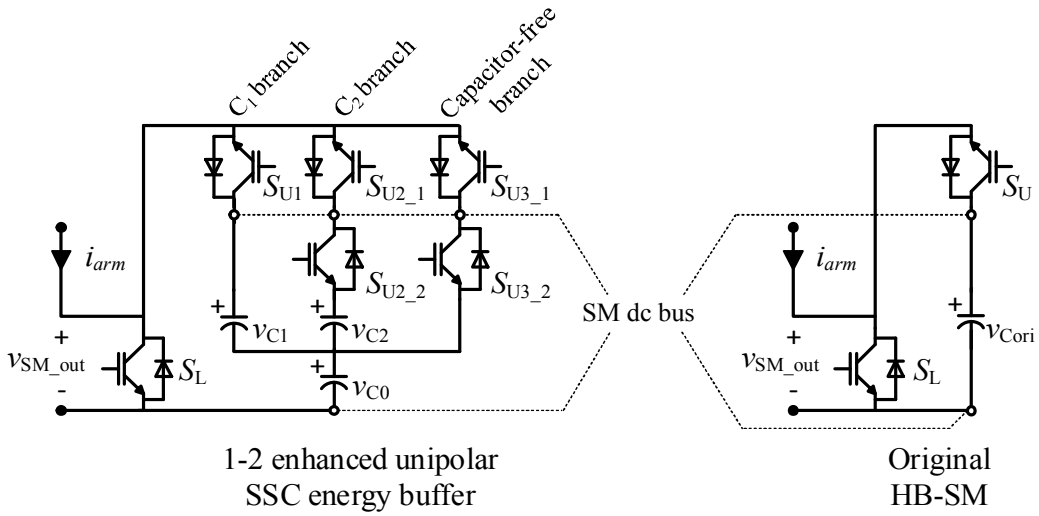

Figure 8.3: Circuit diagrams of SSC-SM and HB-SM

The rated voltage of C_0 is selected to be the same as C_{ori} but with half capacitance. Both C_1 and C_2 have the same capacitance as C_0. The rated voltages of C_1 and C_2 are much lower and both depend on the permitted voltage ripple of the SM dc bus. In the following analysis, the SM dc bus voltage ripple is assumed to be symmetrical about the average, and the p.u. value, $V_{\text{ripplep.u}}$ (peak-to-peak), is based on the SM rated dc voltage $V_{\text{SM\_dc}}$ (the MMC rated dc bus voltage V_{dc} divided by the total number of SMs in one arm N). Rated voltages of C_0, C_1 and C_2 are chosen to be $(1+½V_{\text{ripplep.u.}})V_{\text{SM\_dc}}$, $3/2V_{\text{ripplep.u.}}V_{\text{SM\_dc}}$, and $V_{\text{ripplep.u.}}V_{\text{SM\_dc}}$ respectively as to be detailed in Figure 8.5. The capacitor rated energy storage is calculated as $½CV^2$ where C is the rated capacitance and V the capacitor rated voltage. The total rated energy storage of three capacitors in an SSC-SM is

$$E_{\text{SSC-SM}} = \frac{1}{2}\frac{C_{\text{ori}}}{2}\left\{\left(1+\frac{1}{2}V_{\text{ripplep.u.}}\right)^2+\left(\frac{3}{2}V_{\text{ripplep.u.}}\right)^2+V_{\text{ripplep.u.}}^2\right\}V_{\text{SM\_dc}}^2. \qquad (8.1)$$

The rated energy storage of the capacitor in the original HB-SM is

$$E_{\text{HB-SM}} = \frac{1}{2}C_{\text{ori}}\left(1+\frac{1}{2}V_{\text{ripplep.u.}}\right)^2 V_{\text{SM\_dc}}^2. \qquad (8.2)$$

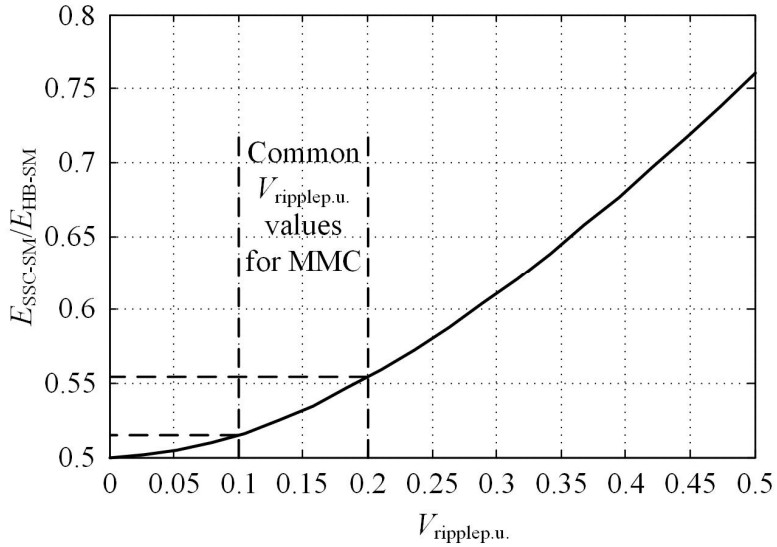

Figure 8.4: Rated energy storage comparison: the ratio between the total rated energy storage of all capacitors in one SSC-SM over that in one HB-SM versus permitted voltage ripple in p.u. (peak-to-peak)

Figure 8.4 plotted the ratio between (1) and (2) for different values of $V_{ripplep.u.}$. The total rated energy storage in one SSC-SM is always lower than that in one HB-SM with $V_{ripplep.u.}$ below 0.5. In addition, more benefits can be gained from the SSC structure with smaller permitted voltage ripple. The reduction of the total rated energy storage is about 45% when $V_{ripplep.u.}$ equals 0.2. Note that with the same capacitor energy density, Figure 8.4 also shows the potential capacitor volume reduction when using the SSC architecture.

8.4.2 Operating principle and switching strategy

When the converter operates at or close to the rated power, the SSC-SM will have all three supporting branches being active, which is referred to as *full operating mode*. In order to reduce the additional power losses, the SSC-SM can also operate with only two or even one supporting branch when the converter power is lower. This is referred to as *partial operating mode*. This section will detail the full operating mode for rated and reduced power operation. The partial operating model will be presented at the end of the chapter. Controlled system

pre-charging is possible as long as gate drivers are available.

Figure 8.5 sketches the waveforms of an SSC-SM at rated power when the SM capacitor is always in the arm circuit. The current through the SSC energy buffer equals the arm current $i_{arm}(t)$. For simplicity, charging and discharging currents are both assumed to be constant with identical amplitudes. Hence in each fundamental cycle there are symmetrical charging and discharging processes. Switching strategies for both processes can be divided into three phases similar to that discussed in [138]:

1) Phase 1 – charging C_0 and C_1: when the energy buffer is to be charged, C_1 branch is activated (and all the other supporting branches are OFF). Detailed switching states are shown in Table 8.1. C_0 and C_1 are charged in series during this period, and C_2 is floating. When the SM dc bus voltage, V_{bus}, reaches its upper limit V_{SM_dcmax}, i.e. $(1+V_{ripplep.u.}/2)V_{SM\_dc}$, v_{C1} becomes $(3/2)V_{ripplep.u.}V_{SM\_dc}$. Then C_1 branch is turned OFF and C_2 branch is turned ON. v_{C2} adds to v_{C0} and the SM dc bus voltage drops back to the lower limit V_{SM_dcmin}, i.e. $(1-V_{ripplep.u.}/2)V_{SM\_dc}$.

2) Phase 2 – charging C_0 and C_2: during this period, C_2 branch is ON. C_0 and C_2 are charged in series until the SM dc bus voltage reaches V_{SM_dcmax} again. At this time v_{C0} becomes $(1-V_{ripplep.u.}/2)V_{SM\_dc}$, and v_{C2} increases to $V_{ripplep.u.}V_{SM\_dc}$. Then C_2 branch is turned OFF, and capacitor-free branch is turned ON. The SM dc bus voltage equals the voltage of C_0.

3) Phase 3 – charging C_0 only: during this period, only the capacitor-free branch is ON. C_0 is charged until the SM dc bus voltage reaches V_{SM_dcmax}.

At this time, all capacitors have reached their maximum and the discharging process will begin which is simply the reverse of the charging process.

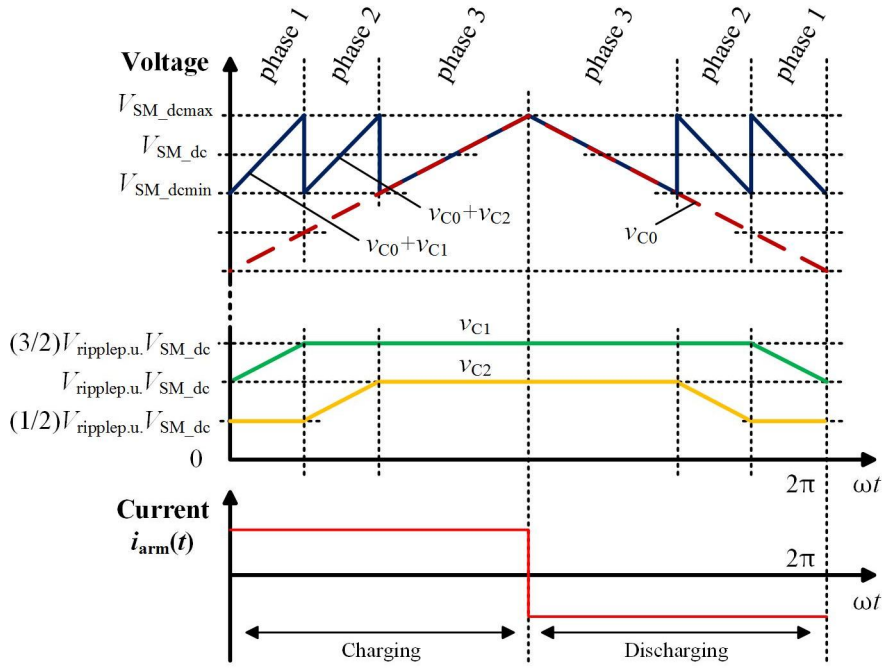

Figure 8.5: Typical operating waveforms of a *1-2 enhanced unipolar* energy buffer based SSC-SM operateing at rated power when the SM is always switched into the arm circuit with constant charging and discharging currents

Figure 8.6 sketches operation waveforms when the SM capacitor is constantly inserted or bypassed in an MMC arm. The current passing through the SSC energy buffer (solid red line) equals the arm current (dashed red line) when the SM capacitor is switched in, which will contain a dc offset corresponding to the active power exchange between the ac and dc sides of the converter. The 2nd order harmonic circulating current component is usually eliminated to avoid extra losses [13]. Hence, only the fundamental component and the dc component are included in the arm current waveform.

Referring to Figure 8.6, the switching strategy between different supporting branches is the same as in Figure 8.5 where the next supporting branch will be turned ON every time when the upper limit of the SM dc bus voltage is met in the charging process or when the lower limit is met in the discharging process. The total voltage of the currently active

capacitor(s), i.e. (v_{C1}+v_{C0}), (v_{C2}+v_{C0}) or v_{C0}, is used for control as shown in Figure 8.7. The saw-tooth like waveform in Figure 8.6 sketches the SM output voltage v_{SM_out} that will drop to near 0 when the SM is bypassed, during which the current passing through the energy buffer equals zero and all capacitor voltages remain constant. The SM-bypass mode is special in MMC applications. Although the SM may be bypassed for arbitrary periods of time in a line frequency cycle, the overall energy charging and discharging the capacitor are balanced by the MMC system-level controller. As a result, the control strategy of the SSC-SM is still effective for all conditions because the capacitors are charged and discharged periodically.

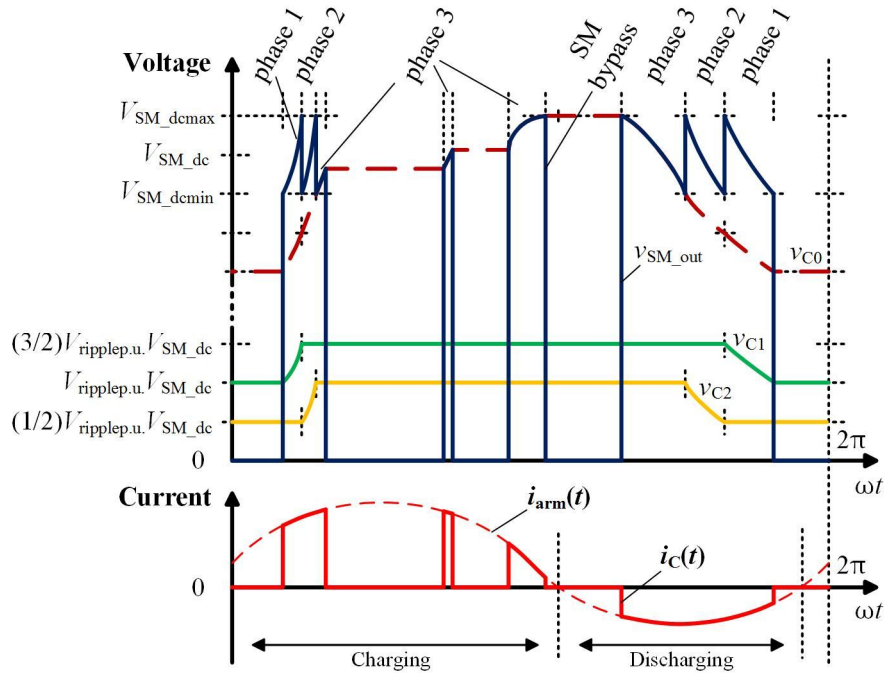

Figure 8.6: Typical operating waveforms of a *1-2 enhanced unipolar* energy buffer based SSC-SM operating at rated power when the SM is being switched as installed in an MMC system with actual sinusoidal arm current containing a dc offset

Figure 8.7 is the control diagram of an SSC-SM in full operating mode. One advantage of the SSC-SM approach is that its control is localized and does not affect the system-level

(MMC) control. Voltages of the three capacitors, C_0, C_1 and C_2, the arm current i_{arm}, as well as the permitted voltage ripple $V_{ripplep.u.}$ are required for controlling the SM. Usually the current sensor for i_{arm} is already installed for SM capacitor voltage balancing control. Moreover, the current-sensorless control method of the SSC energy buffer [136] can be adopted when necessary.

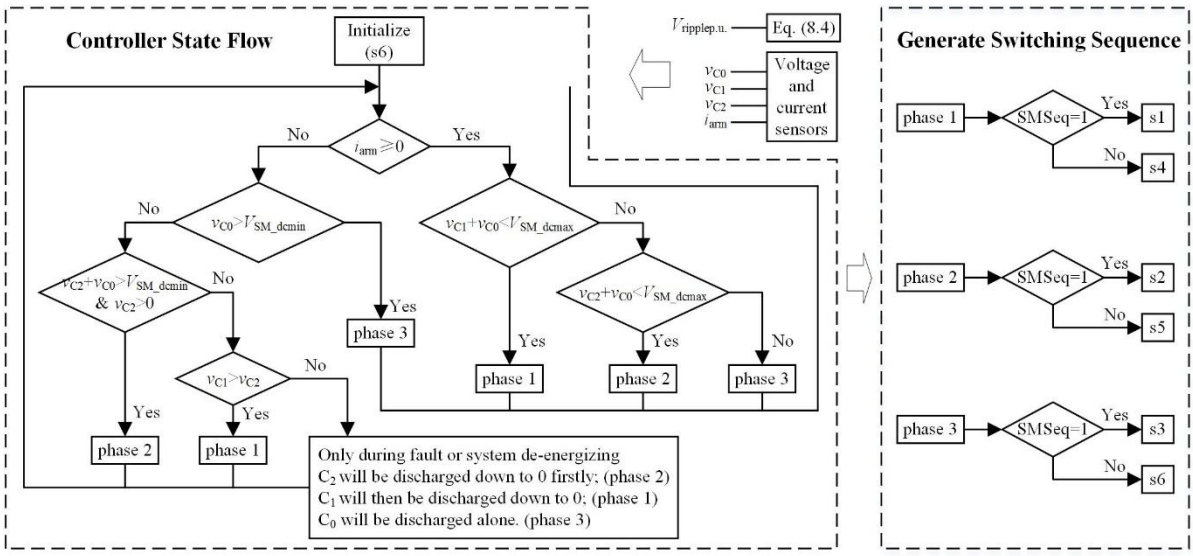

Figure 8.7: SM-level control diagram of the SSC-SM (full operating mode)

s1 to s6 in Figure 8.7 are the gating signals for the switches as listed in Table 8.1. In normal operation when the SM is switched into the arm circuit, the switching strategies are shown in the third column marked as s1, s2 and s3 for phases 1, 2 and 3 respectively. In addition, the switching strategies to bypass the SM are listed in the second column marked as s4, s5 and s6 for the three operating phases.

In additional to the forth column in Table 8.1, Figure 8.8 sketches the switching strategies especially during deadbands. In high-voltage higher-power applications, a deadband with a duration of a few microseconds is usually added before the turn-ON command in order to avoid shorting the dc bus capacitor. d and d^* represent two types of deadbands.

States	SM bypassed						SM switched-in						Deadband					
	S_L	S_{U1}	S_{U2_1}	S_{U2_2}	S_{U3_1}	S_{U3_2}	S_L	S_{U1}	S_{U2_1}	S_{U2_2}	S_{U3_1}	S_{U3_2}	S_L	S_{U1}	S_{U2_1}	S_{U2_2}	S_{U3_1}	S_{U3_2}
phase 1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
$i_{arm} \geq 0$	$v_{SM\_out} = 0$ (s4)						$v_{SM\_out} = v_{C1} + v_{C0}$ (s1)						$v_{SM\_out} = v_{C1} + v_{C0}$					
$i_{arm} < 0$													$v_{SM\_out} = 0$					
phase 2	1	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0
$i_{arm} \geq 0$	$v_{SM\_out} = 0$ (s5)						$v_{SM\_out} = v_{C2} + v_{C0}$ (s2)						$v_{SM\_out} = v_{C2} + v_{C0}$					
$i_{arm} < 0$													$v_{SM\_out} = 0$					
phase 3	1	0	0	1	0	1	0	0	0	1	1	1	0	0	0	1	0	1
$i_{arm} \geq 0$	$v_{SM\_out} = 0$ (s6)						$v_{SM\_out} = v_{C0}$ (s3)						$v_{SM\_out} = v_{C0}$					
$i_{arm} < 0$													$v_{SM\_out} = 0$					

Table 8.1: Switching strategy and SM output voltage

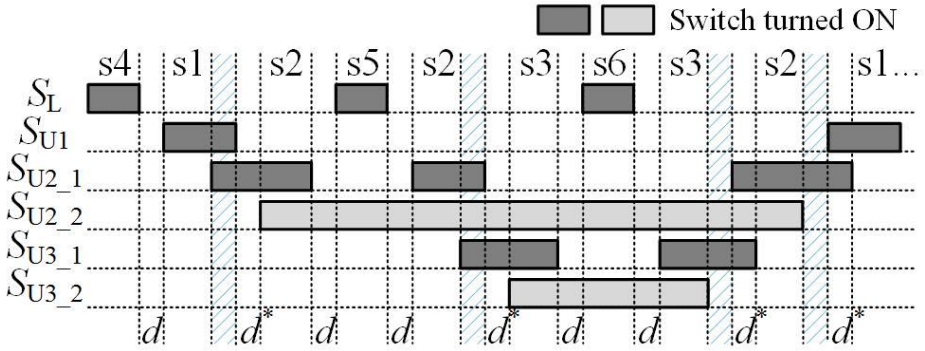

Figure 8.8: Deadband strategies for power switches

d represents the deadband between the lower switch S_L and the upper main switches – S_{U1}, S_{U2_1} and S_{U3_1} – when the SM is switched in or out of the arm circuit (only the capacitor charging process is shown in Figure 8.8). When the SSC-SM is bypassed (s5 and s6 in Table 8.1), other than S_L, S_{U2_2} is still ON in s5 and both S_{U2_2} and S_{U3_2} are ON in s6. Similar case can be found in s3. The reason for this action is to ensure that the SM output voltage is always within the permitted range [0, V_{SM_dcmax}] during deadbands d, especially when the current flows into the SM. As a result, the voltage that needs to be blocked by S_L will never exceed V_{SM_dcmax}, and thus no higher voltage blocking capability is required for S_L in the SSC-SM.

Deadbands marked as *d** are added in between the switching of supporting branches (S_{U1} & S_{U2_2} and S_{U2_1} & S_{U3_2}) to prevent fault discharging of supporting capacitors. In addition, a short overlap time (the hatched blue areas usually with a length of a few microseconds) is added to the two upper main switches being switched to reduce switching losses. In such a case, zero-voltage-switching (ZVS) or near ZVS is achieved. Since the switching losses of IGBT/diode modules are proportional to the blocking voltage [143], the switching losses are kept low. As an example, when i_{arm} is negative and the SSC energy buffer is switched from phase 3 (s3) back to phase 2 (s2), S_{U3_2} is turned OFF immediately. After S_{U3_2} is OFF, the current continues to flow through the diode of S_{U3_2} and the IGBT of S_{U3_1}. After a short overlap time, S_{U2_1} is turned ON and C_2 will start to discharge through S_{U2_1} and S_{U2_2} while the capacitor-free branch will automatically block due to V_{C2}. The voltage on S_{U3_1} is always close to zero. The voltage on S_{U2_1} is only V_{C2} before it is turned ON. Thus, the turn-OFF loss of S_{U3_1} is negligible and the turn-ON loss of S_{U2_1} is only 20%-30% of the case when the switch is switched at SM rated dc voltage. The switching losses of the back-to-back connected switches S_{U2_2} and S_{U3_2} are always low due to the very low voltages they block.

Table 8.2 lists the required voltage blocking capabilities for all power switches. With the proposed deadband strategy, the required voltage blocking capability of S_L in the SSC-SM stays the same as in the HB-SM: V_{SM_dcmax}. S_{U1} and S_{U2_1} need to have slightly higher voltage blocking capabilities than the S_U in the HB-SM. When S_L is conducting, both S_{U1} and S_{U2_1} need to withstand the total voltage of the backbone and one supporting capacitor. Note that $V_{ripple.u.}$ is usually very small (around 15%). As a result, in implementation, the voltage-blocking requirements of S_{U1} and S_{U2_1} are comparable to S_U in the HB-SM. Note that at all switching instants the actual switching voltages for S_{U1} and S_{U2_1} will not be higher than V_{SM_dcmax}, yielding similar switching losses. S_{U3_1} needs to withstand the peak voltage of v_{C0}, i.e. V_{SM_dcmax}. The back-to-back connected switches S_{U2_2} and S_{U3_2} are added to prevent

unwanted discharging of supporting capacitors and thus they only require relatively low voltage blocking capabilities equal to the maximum voltage of the supporting capacitors.

Switching states	**Maximum voltage on power switches**					
S_L-S_{U1}-S_{U2_1}-S_{U2_2}-S_{U3_1}-S_{U3_2}	vs_{UL}	vs_{U1}	vs_{U2_1}	vs_{U2_2}	vs_{U3_1}	vs_{U3_2}
0-0-0-0-0-0 ($i_{arm} \geq 0$) & 0-1-0-0-0-0	v_{C1}+v_{C0} (phase 1)	0[a]	0	v_{C1}-v_{C2}	0	v_{C1}
0-0-0-0-0-0 ($i_{arm} < 0$) & 1-0-0-0-0-0	0	v_{C1}+v_{C0} (phase 1)	v_{C2}+v_{C0} (phase 1)	0	v_{C0}	0
0-0-0-1-0-0 ($i_{arm} \geq 0$) & 0-0-1-1-0-0	v_{C2}+v_{C0} (phase 2)	v_{C1}-v_{C2}	0	0	0	v_{C2}
0-0-0-1-0-0 ($i_{arm} < 0$) & 1-0-0-1-0-0	0	v_{C1}+v_{C0} (phase 2)	v_{C2}+v_{C0} (phase 2)	0	v_{C0}	0
0-0-0-1-0-1 ($i_{arm} \geq 0$) & 0-0-0-1-1-1	v_{C0} (phase 3)	v_{C1}	v_{C2}	0	0	0
0-0-0-1-0-1 ($i_{arm} < 0$) & 1-0-0-1-0-1	0	v_{C1}+v_{C0} (phase 3)	v_{C2}+v_{C0} (phase 3)	0	v_{C0}	0

[a]0-voltage indicates that the switch is conducting neglecting the on-state voltage drop.

Table 8.2: Voltage capability requirement for power switches

8.4.3 Reduced power operation

In a conventional HB-SM based MMC, when the converter operates at lower than the rated power, the width of the voltage ripple will reduce accordingly. The voltage ripple is found to be proportional to the ac side line current I_s (rms) for a given operating point (m, φ) [86]:

$$V_{\text{ripplep.u.}} = \frac{2\sqrt{2}NI_s}{\omega V_{dc} C_{ori}} f_{\text{ripple}}(m,\varphi), \tag{8.3}$$

where m is the modulation index, V_{dc} the converter pole-to-pole dc bus voltage, φ the power factor angle at ac output, ω the fundamental angular frequency. (8.3) is a simplified equation to estimate the SM capacitor voltage ripple with good accuracy. If higher precision of the estimation is required, (4.27a) or (4.32) in Chapter 4 can be used. Values of $f_{\text{ripple}}(m, \varphi)$ with respect to m and φ are plotted in Figure 8.9 [86]. In an SSC-SM, in order to balance the amplitudes all the voltage ripples introduced by switching the supporting branches and ease the circulating current suppression control, the permitted voltage ripple (sent to the controller

in Figure 8.7) is adjusted in real-time according to the converter's operating point by

$$V_{\text{ripplep.u.}} = \frac{I_{\text{s}} f_{\text{ripple}}(m,\varphi)}{I_{\text{s\_r}} f_{\text{ripple\_r}}(m,\varphi)} V_{\text{ripplep.u.\_r}}, \tag{8.4}$$

where symbols with subscript '_r' stand for rated values while those without are for real-time variables.

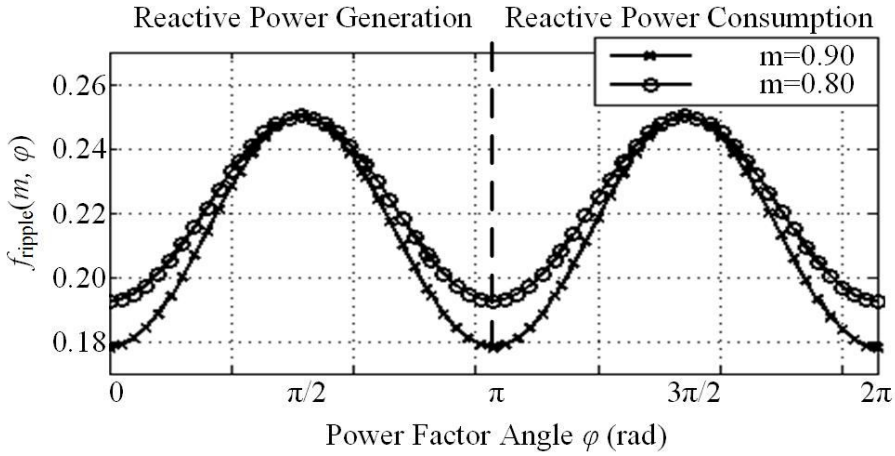

Figure 8.9: Voltage ripple function $f_{\text{ripple}}(m, \varphi)$ extracted from [86]

8.5 Simulation Validation of the SSC-SM based MMC

A grid-connected SSC-SM based MMC system is modelled in Matlab/Simulink to assist the design of a prototype SM. Control algorithms of the new converter system include the amended outer loop current and inner circulating current suppression controllers to suppress the additional harmonics introduced by switching the supporting branches in SSC-SMs. Performance of the SSC-SM based MMC is evaluated in both steady state and transients. Finally, power losses are compared with a HB-SM based design.

8.5.1 System design

Figure 8.10 shows the circuit diagram of a 21-level MMC with the SSC-SM as in the dashed box. The converter is connected to a ±20 kV dc-link and a 23 kV (line-to-line rms), 50 Hz ac

grid busbar through a three-phase transformer. The arm inductor is 16.2 mH. All p.u. values are based on the rated ac side voltage and current. There are 20 SMs in each arm with SM rated dc voltage V_{SM_dc}=2000 V. The converter is designed to invert or rectify 19.1 MW active power with a modulation index m=0.9. The ac side power is measured at the converter output to exclude the coupling transformer effect. Table 8.3 summarizes the system parameters. With the allowable 0.15p.u. peak-to-peak voltage ripple at rated power ($V_{ripplep.u.\_r}$), the minimum required capacitance for one HB-SM is derived to be 2.6 mF [86] with 2150 V_{dc} rated voltage. For the SSC-SM, the capacitance of backbone or a supporting capacitor (C_0, C_1 or C_2) is half of this i.e. 1.3 mF.

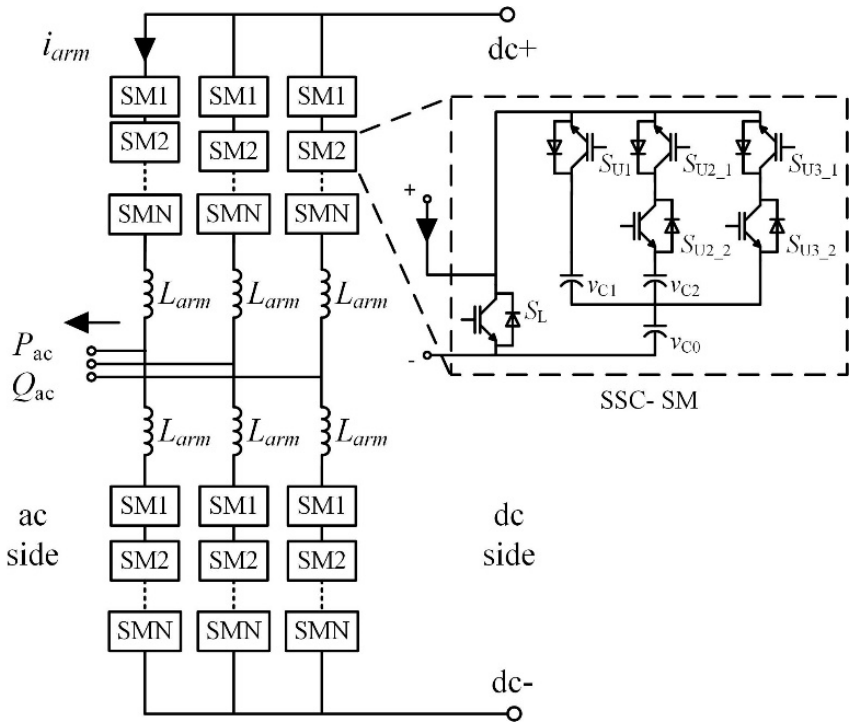

Figure 8.10: Circuit diagram of an MMC system based on the proposed SSC-SM

Item	Parameters
Dc bus voltage	40 kV (pole-to-pole)
Grid voltage	23 kV line-to-line (rms), 50Hz
V_{nominal} at output point	18 kV phase to neutral
Rated line current	500 A_{rms}
Rated capacity	19.1 MW (PF=1)
Transformer inductance	0.1p.u.
Number of SMs	20 per arm
Arm inductance	16.2 mH
SM rated dc bus voltage	2000 V
$V_{\text{ripplep.u.\_r}}$	0.15 peak-to-peak

Table 8.3: System parameters for simulation

No.	Brand	Capaci-tance (C mF)	Max. voltage (V)	Rated voltage (V_r V)	Rated energy storage ($0.5CV_r^2$)	Energy density (J/Litre)	Total volume (Litre)	Relative est. volume with C_{ori}	Ripple current (A)
Original HB-SM									
C_{ori}	IXYS	5×0.52	2150	2200	6.30 kJ	294	21.42	100%	600
SSC based HB-SM									
C_0	IXYS	2.5×0.52	2150	2200	3.15 kJ	294	10.71	50%	300
C_1	TDK	1.3×1.0	450	450	0.13 kJ	119	1.11	5.2%	176
C_2		1.3×1.0	300	450	0.13 kJ	119	1.11	5.2%	176

Table 8.4: Capacitor selection for HB-SM and SSC-SM

Table 8.4 compares the selection of capacitors for both HB-SM and SSC-SM. Five 520 μF, 2200 V_{dc} capacitors from IXYS each with 120 A_{rms} ripple current capability [144] are selected for an HB-SM while two and half (assuming possible in a customized design in the future) of the same are chosen as the backbone capacitor in an SSC-SM. Both supporting capacitors use the 1000 μF, 450 V_{dc} capacitor from TDK each with 135 A_{rms} ripple current capability [145]. In order to offer the 1.3 mF capacitance, parameters including the capacitance, volume and ripple current capability are scaled. The total volume of the capacitor in one HB-SM is 21.42 litres while that in one SSC-SM is 12.93 litres, which is

only 60% of one HB-SM.

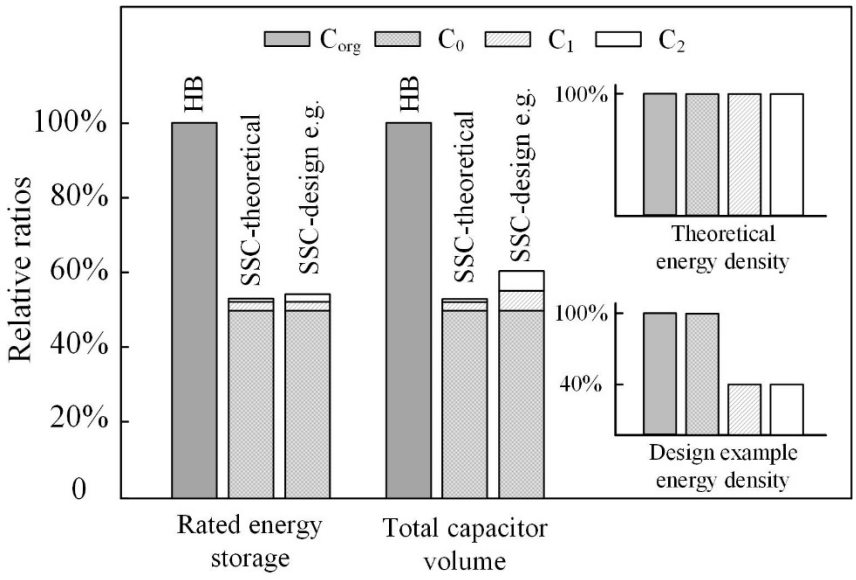

Figure 8.11: Comparison of the rated energy storage and total capacitor volume between the HB-SM and SSC-SM including both theoretical and actual values for the design example. The rated energy storage is the overall ½CV^2 of all the capacitors

Figure 8.11 further compares the rated energy storage and the total capacitor volume between the HB-SM and SSC-SM for the design example. In all cases, values of the HB-SM are treated as 100% while the values of the SSC-SM are converted to a ratio based on the corresponding HB-SM value. In theoretical calculation, the rated capacitor voltage of both the HB-SM and SSC-SM are set to the maximum in normal operation (C_{ori}, C_0: 2150 V; C_1: 450 V; C_2: 300 V), and the same energy density is assumed for all capacitors. When calculating for the design example, the capacitance, rated capacitor voltage and energy density are based on the chosen products as listed in Table 8.4. Due to the lower energy density of the two supporting capacitors, the actual total capacitor volume of the SSC-SM is higher than the theoretical calculation. Nonetheless, in this example, the total capacitor volume in an SSC-SM is still only 60% of one HB-SM. The above analysis and Figure 3.4 show that the effect of SM capacitor reduction (volume) using the SSC architecture depends

on the energy density of the supporting capacitors. If their energy density were close to that of the backbone capacitor, the total capacitor volume in an SSC-SM will be close to the theoretical calculation. Therefore, SMs with higher rated voltages will benefit more from the SSC architecture.

Table 8.5 lists the choices of power switches for the HB-SM and SSC-SM. The 3.3 kV, 1 kA IGBT/diode module from Infineon [146] is chosen for the HB-SM (S_L and S_U), and the same modules are to be used for the high voltage ones in the SSC-SM (S_L, S_{U1}, S_{U2_1} and S_{U3_1}). Two 650 V, 450 A IGBTs/diodes also from Infineon [147] are chosen for the low voltage switches (S_{U2_2} and S_{U3_2}). These could all be packed in the same customized module without significantly increasing the volume and weight from the HB-SM power module. Table 8.5 presents the ratio between the maximum blocking voltage and the rated collector-emitter voltage V_{CES} for each device. If larger safety margin is required, devices rated at 4.5 kV may be used. The rated continuous current I_C for all devices is about twice the peak arm current to ensure safety.

No.	**Power switch**	**Rated** V_{CES}	**Rated** I_C	**Max. blocking voltage** (V_{max})	V_{max}/V_{CES}
Original HB-SM					
S_L, S_U	Infineon FZ1000R33HE3	3300 V	1000 A	2150 V	65%
SSC based HB-SM					
S_L	Infineon FZ1000R33HE3	3300 V	1000 A	2150 V	65%
S_{U1}				2600 V	79%
S_{U2_1}				2450 V	74%
S_{U3_1}				2150 V	65%
S_{U2_2}	2 Infineon FF450R07ME4	650 V	450 A ×2	450 V	69%
S_{U3_2}				450 V	69%

Table 8.5: Power switch comparison between the HB-SM and SSC-SM

8.5.2 System control

The system-level control of the SSC-SM based MMC is similar to the one with HB-SMs as introduced in Chapter 2 and in [19, 39]. Figure 8.12 shows the control block diagram. The outer power controller converts the power references to current references (I_{d_ref} and I_{q_ref}) for the inner current controller. The inner loop is based on the *dq* frame [42] that generates the required converter output voltages. In the SSC-SM based MMC, due to switching the supporting branches, additional harmonics are found in the converter ac outputs. Thus, another *dq* based controller is added to eliminate the dominant 5th harmonic. 4th order harmonic is also found in the circulating currents between converter arms. In addition to the circulating current suppressing controller (CCSC) operating at twice line-frequency [19], a similar controller is added to eliminate the 4th harmonic.

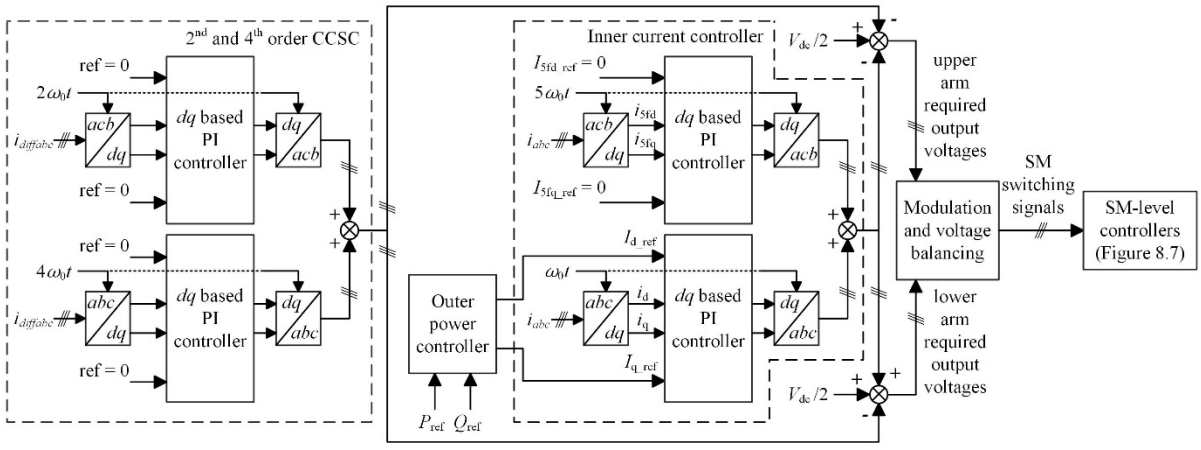

Figure 8.12: System-level control diagram of the SSC-SM based MMC system

Control signals generated by the inner current controllers and CCSCs are used to determine the required arm voltages. The acquired signals are then sent to the modulation block [19] to decide the number of SMs to be switched-in for each arm. The SM capacitor voltage balancing control will then help to find the exact SMs to be inserted. The signals sent

to the voltage balancing controller are only the backbone capacitor voltages, yielding a fully-independent SM control strategy. The supporting capacitor voltages are controlled and balanced locally with the SM-level controller embedded in each SM.

8.5.3 Simulation results: steady state

Figure 8.13 gives the ac output currents and voltages of the SSC-SM based MMC when inverting 19.1 MW active power at PF=1. Harmonic analysis shows a slight increase of THD compared with the HB-SM based converter outputs. The THD of output current and voltage are increased from 0.6% and 4.28% to 0.78% and 5.56% respectively. Additional harmonic distortions are caused by switching the supporting branches. Advanced MMC control strategies can be implemented to cancel the voltage ripple of different SSC-SMs if necessary.

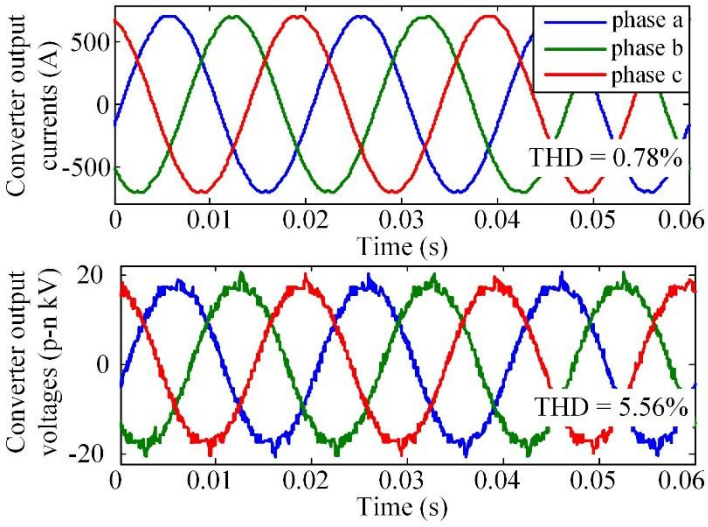

Figure 8.13: Converter ac output current (top) and voltage (bottom) waveforms of the SSC-SM based MMC in normal operation

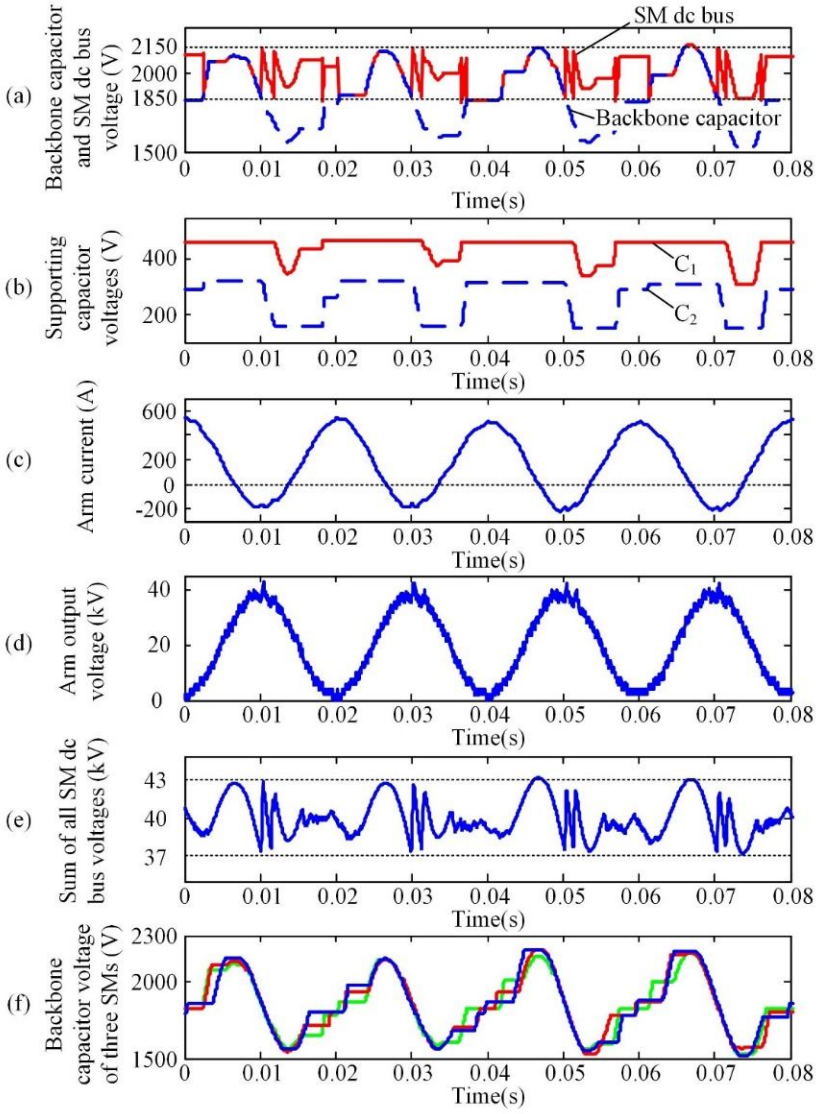

Figure 8.14: Steady state operation waveforms: (a) backbone capacitor and SM dc bus voltage of one SM in the upper arm in phase *a*; (b) supporting capacitor voltages in the same SM; (c) arm current; (d) arm output voltage; (e) sum of all SM dc bus voltages in the arm and (f) backbone capacitor voltages of three SMs in the arm

Figure 8.14 shows the voltages and currents in the upper arm of phase *a* in the SSC-SM based MMC. Figure 8.14(a) shows a SM backbone capacitor voltage in dashed blue. With half the capacitance of a HB-SM capacitor, its voltage ripple (approx. 600 V) is twice of the permitted voltage ripple of the SM dc bus (300 V or 0.15 p.u. p-p). Through switching the

supporting branches, the SM dc bus voltage is maintained within the allowable range at all times [solid red line in Figure 8.14(a)]. Figure 8.14(b) sketches the supporting capacitor voltages in the same SM. v_{C1} (in red) varies between 300 V and 450 V while v_{C2} (in blue) varies between 150 V and 300 V. All voltage waveforms in Figure 8.14(a) and (b) agree with the expected in Figure 8.6. Note that in both HB-SM and SSC-SM based MMCs, depending on the SM capacitor voltage balancing algorithm, the switching sequence of a SM may be different from cycle to cycle, i.e. the bypass time of a SM may vary. The capacitor voltage in the same SM may vary from cycle to cycle. In addition, due to low switching frequency, there are small derivations between the SM capacitor voltages in the same arm [Figure 8.14(f)]. That is why the waveforms in Figure 8.14(a) and (b) are slightly different from the expected. Similar effects are found in a HB-SM based MMC and this has no impact on the overall system performance because these variations are not reflected in the ac outputs. The arm current is shown in Figure 8.14(c). With 2nd and 4th order CCSCs, the harmonic circulating currents are negligible leaving only the 50 Hz and dc offset. Figure 8.14(d) shows the arm output voltage. When the arm voltage is high, majority of the SMs are switched into the arm string, two voltage spikes can be found in each cycle due to simultaneously switching the supporting branches. The additional *dq* frame (4th and 5th order) based PI controllers in the inner current controller and the CCSC have helped to limit the impacts of the voltage spikes on the converter ac outputs. If higher quality is required, faster controllers such as predictive control can be applied. Figure 8.14(e) shows the sum of all SM dc bus voltages in the arm. The ripple of this voltage is within the permitted band (0.15p.u. p-p). Figure 8.14(f) gives three backbone capacitor voltages in the arm, which are well balanced. The capacitor ripple currents in C_0, C_1 and C_2 are measured to be 138 A, 40 A and 75 A (rms) respectively, which are much lower than their limits.

Figure 8.15 compares the average loss power of one SM in HB-SM or SSC-SM based

MMC system, at four operating points: 1) inverting, 2) rectifying 19.1 MW active power, 3) generating or 4) consuming 19.1 MVAr reactive power at the converter ac output. For loss analysis, (6.7) and (6.8) are used to calculate the conduction losses of both IGBT and diode, the switch-ON and switch-OFF losses of IGBT and the diode reverse recovery loss respectively. When calculates the losses for the parallel connected 650 V power modules, the conducting current is divided by two and then double the derived losses. Table 6.6 and 6.7 list the parameters of the selected power modules for conduction and switching losses calculation respectively. All data are extracted from the datasheets [146, 147] by a curve-fitting method. The junction temperature is chosen as 125ºC for all cases to provide a certain safety margin.

Device\Parameter	V_{0j} / V	r_j / Ω
IGBT - 3.3 kV	1.3642	1.6642e-3
Diode - 3.3 kV	1.2587	1.5333e-3
IGBT - 650 V	0.7567	2.0811e-3
Diode - 650 V	0.9213	1.3639e-3

Table 8.6: Voltage offset and ON-state resistance coefficients of the power module (125℃)

Energy\Parameter	a_p	b_p	c_p
[a]E_{on} - 3.3 kV / mJ	6.4935e-5	1.3948	223.6364
[a]E_{off} - 3.3 kV / mJ	1.7857e-4	1.1539	105.4545
[a]E_{rec} - 3.3 kV / mJ	-4.1304e-4	1.2635	244.8696
[b]E_{on} - 650 V / mJ	-2.8986e-6	0.0114	0.2826
[b]E_{off} - 650 V / mJ	3.0918e-5	0.0376	5.4783
[b]E_{rec} - 650 V / mJ	-1.4726e-5	0.0219	1.9819

[a]FZ1000R33HE3 V_{CE_ref} = 1800 V; [b]FF450R07ME4 V_{CE_ref} = 300 V.

Table 8.7: Coefficients in the switching energy polynomial of the power module (125℃)

Figure 8.15 shows that the average loss power of one SSC-SM are slightly higher than that of one HB-SM in rated power operation with an increment of 7% to 15%. Power losses of the lower switch S_L are similar because of the similar modulation and voltage balancing

controllers applied in both systems. The total loss of the three upper main switches (S_{U1}, S_{U2_1} and S_{U3_1}) in the SSC-SM is close to the upper switch total loss in the HB-SM (S_U). It shows that the additional switching losses introduced by switching the supporting branches are insignificant owing to the low-voltage switching presented in Chapter 8.4.2. For all four operating points, power losses of the two low voltage switches (S_{U2_2} and S_{U3_2}) contribute to most of the additional losses. Note that conduction losses dominate in S_{U2_2} and S_{U3_2}.

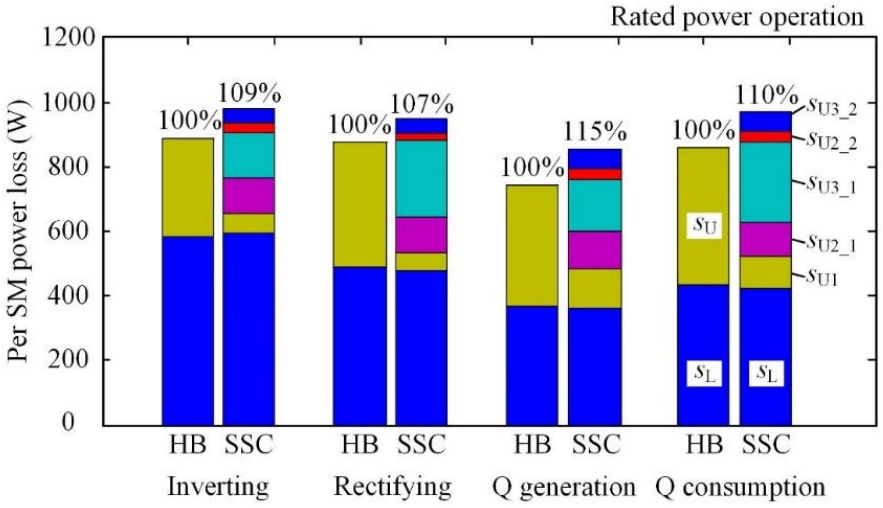

Figure 8.15: Power losses comparison between one HB-SM and one SSC-SM operating at inverting, rectifying, reactive power (Q) generation or consumption

8.5.4 Simulation results: power reversal

In order to show the transient performance of an SSC-SM based MMC, Figure 8.16 presents the system response during active power reversal. The converter was rectifying 19.1 MW active power with unity power factor, and it suddenly switched to inverting the same amount of power. Figure 8.16(a) to (d) give the converter outputs as well as the arm current and voltage of the upper arm in phase *a*. The system has very fast response and reaches steady state shortly after the load change.

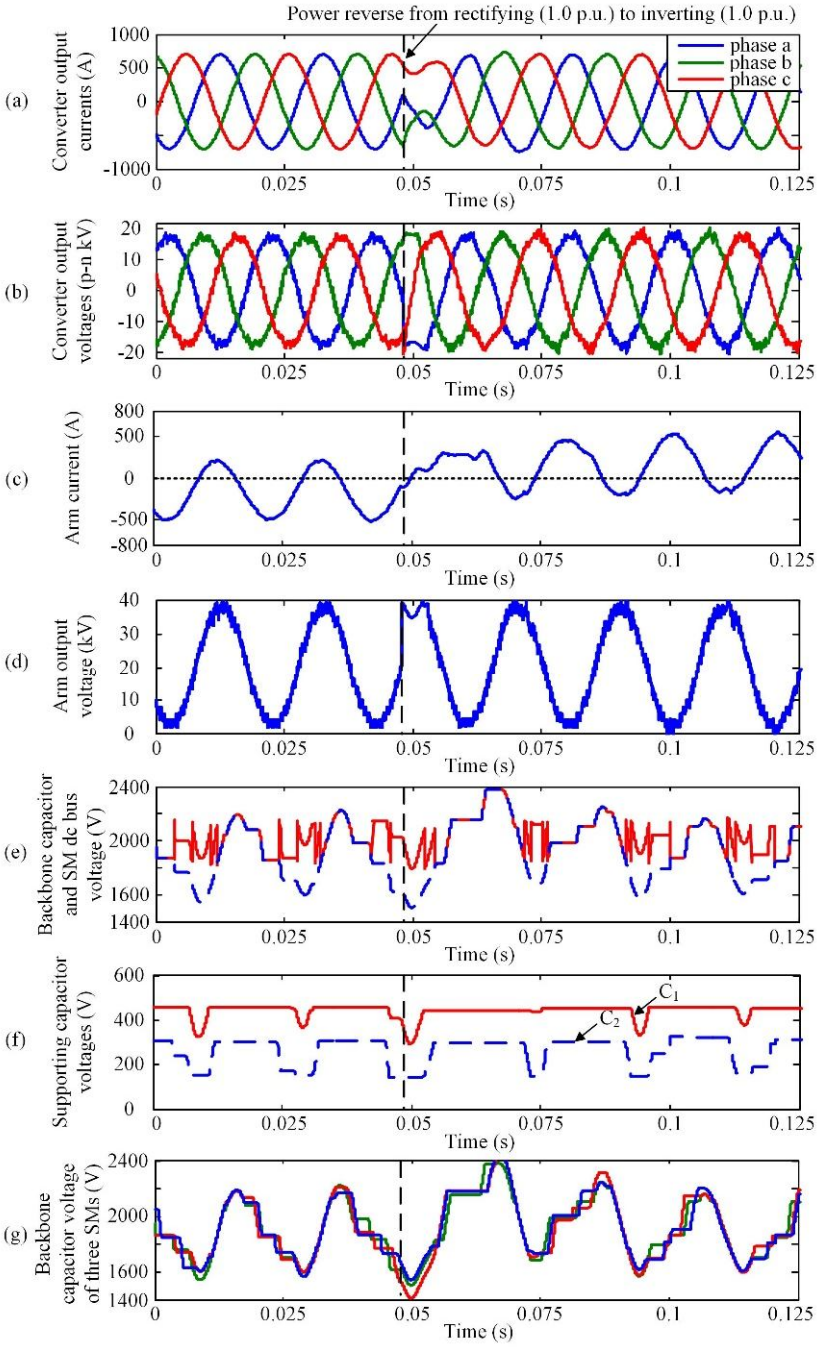

Figure 8.16: Waveforms during active power reversal: (a) and (b) ac output currents and voltages; (c) arm current; (d) arm output voltage; (e) backbone capacitor and SM dc bus voltage of one SM; (f) supporting capacitor voltages and (g) backbone capacitor voltages of three SMs in the arm

During the transient, the SM dc voltage [solid red line in Figure 8.16(e)] and both supporting capacitors are well controlled [Figure 8.16(f)]; in the meantime, all backbone capacitor voltages in the arm [Figure 8.16(g)] are balanced. Note that the backbone capacitor voltages exceed the rated limit after the power reversal but only last for one cycle. This short period of overvoltage is believed to have neglected impacts on the capacitor lifetime and this phenomenon happens in a conventional HB-SM based MMC during fast power reversal as well.

8.6 Experimental Validation

In the last section, computer simulation helps to show the validity of the system-level control of the SSC-SM based MMC and its performance under both steady state and transient conditions. This section will show the validity of the SM-level control and the low-voltage switching strategy through experiment. The capacity of the design example is scaled down for experiment validation. A prototype SSC-SM is built and tested in the laboratory using the compensated model assisted SM testing scheme presented in Chapter 7.

8.6.1 Experimental test platform and prototype SSC-SM

A prototype SSC-SM with reduced capacity is built and tested experimentally to verify the SM-level control and the low-voltage switching strategy. Rated capacity of the 21-level SSC-SM based MMC system is scaled down to 92 kW (PF=1) with 8 kV pole-to-pole dc and 4.4 kV line-to-line rms ac side voltages. The rated ac current is 12 A_{rms}. With 20 SMs in each arm, the SM rated dc voltage is 400 V. Due to the lower rated current limited by the test platform, the permitted SM dc bus voltage ripple is 0.12p.u. peak-to-peak. The compensated model assisted SM testing scheme presented in Chapter 7 is used to test the prototype SSC-SM.

To limit the SM dc bus voltage ripple within 0.12p.u. p-p, the required capacitance for one HB-SM is calculated to be 400 μF [86]. Hence, the capacitance of all backbone and supporting capacitors in the SSC-SM is 200 μF. According to Figure 8.5, the maximum capacitor voltage of the backbone capacitor is 424 V and of the supporting capacitors C_1 and C_2 are 72 V and 48 V respectively. Hence, a 200 μF 450 V_{dc} MPPF capacitor from VISHAY is selected as the backbone capacitor. The supporting capacitor C_1 is made up of three parallel-connected 68 μF 100 V_{dc} capacitors from AVX while C_2 is made up of two parallel-connected 110 μF 75 V_{dc} capacitors also from AVX. In the experiment, capacitors with rated voltages higher than demanded are chosen for safety reasons. Six IGBT/diode modules from ON Semiconductor are used. Detailed parameters in the experiment are listed in Table 8.8.

Item	Parameters
Dc bus voltage	8 kV (pole-to-pole)
Grid voltage	4.4 kV line-to-line (rms), 50Hz
Rated ac current	12 A rms
Rated capacity	92 kW (PF = 1)
Transformer inductance	0.1p.u.
Arm inductance	108 mH
Number of SMs	20 per arm
SM rated dc bus voltage	400 V
Peak arm current	12.3 A
$V_{\text{ripplep.u.\_r}}$	0.12p.u. peak-peak
Backbone capacitor C_0	200 μF 450 V_{dc} MKP1848720454Y5 (VISHAY)
Supporting capacitor C_1	3 × 68 μF 100 V_{dc} FFB54E0686K (AVX)
Supporting capacitor C_2	2 × 110 μF 75 V_{dc} FFB54D0117K (AVX)
IGBT/diode module	6 × NGTB40N120FLWG (ON Semiconductor) Rated: 1.2 kV; (IGBT & diode) 40 A at 100 °C
Interface	PC + dSpace DS1103
Auxiliary SM	Same as the one used in Chapter 7
Coupling inductor	Hammond Manufacturing; Rated: 10 mH; 20 A_{dc}

Table 8.8: Experiment platform parameters

Figure 8.17 shows the prototype SSC-SM with all backbone and supporting capacitors mounted on the top side of the PCB and IGBT/diode modules on the back. Three snubber capacitors (220 nF, 1000 V) are added to reduce the voltage and current spikes caused by the switching of power switches. In a design of a full-scale SSC-SM for high-voltage high-power applications, the relative volume of the snubber capacitor is expected to be much smaller than the backbone and supporting capacitors.

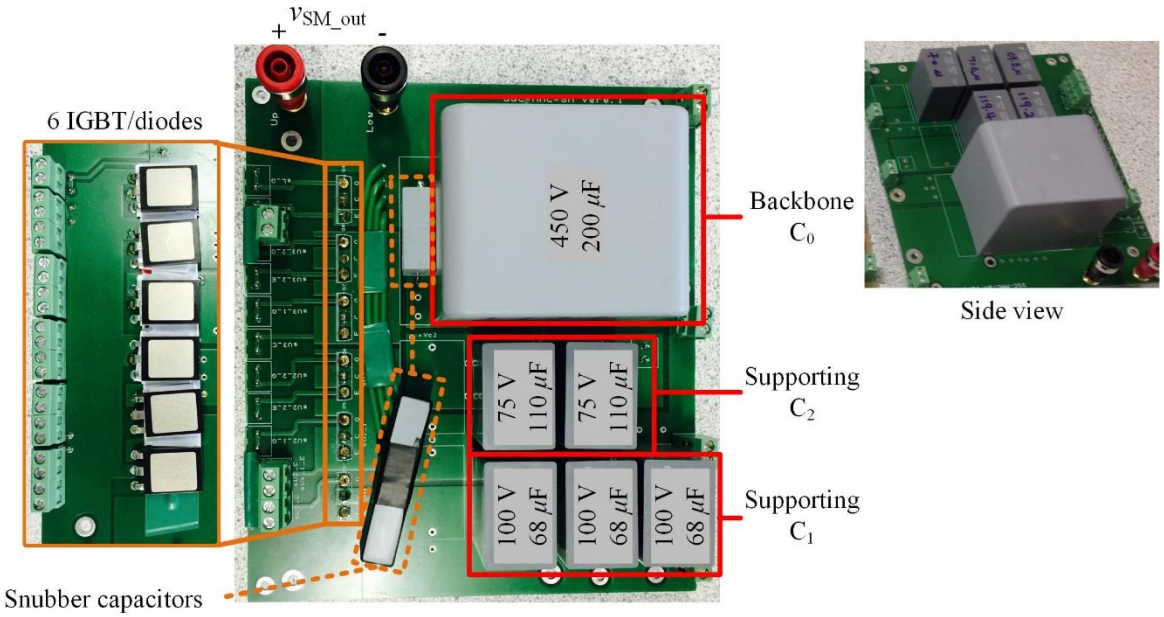

Figure 8.17: A picture of the 400 V, 12.3 A_{peak} prototype SSC-SM

Similar to Figure 8.11, Figure 8.18 compares the rated energy storage and the total capacitor volume of the prototype SSC-SM against a HB design. Due to the relatively low rated voltage, the two supporting capacitors have low energy density: 13.1 J/litre (C_1) and 11.9 J/litre (C_2) respectively, which are less than 17% of the backbone capacitor energy density (77.4 J/litre). It is the reason that the total volume of both supporting capacitors is aound half of the backbone capacitor in Figure 8.17. It shows again that SMs with higher rated voltages will benefit more from the SSC architecture if film capacitors were used for both the backbone and supporting capacitors. In SMs with lower rated voltages, as the case

of the prototype, other types of capacitors, such as ceramic, with higher energy densities may be chosen.

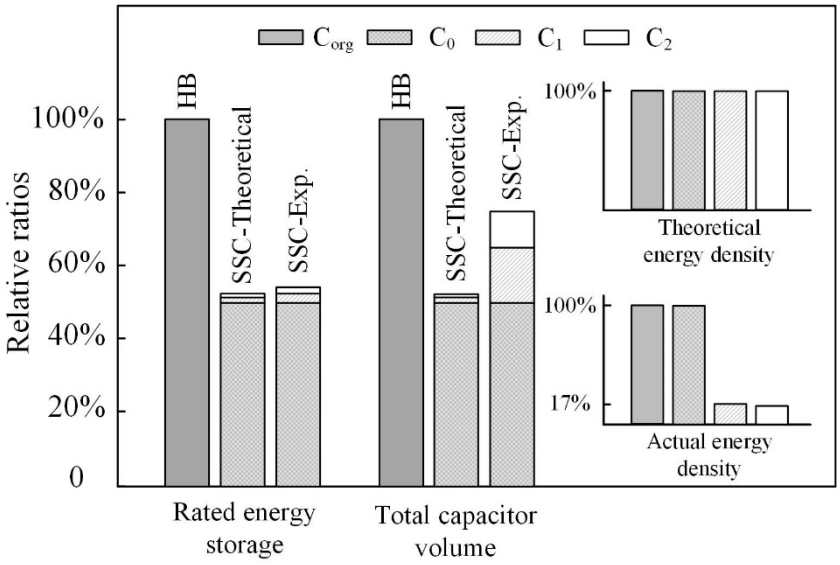

Figure 8.18: Comparison of the rated energy storage and total capacitor volume between the HB-SM and SSC-SM including both theoretical and actual values for the "scaled down" prototype

Figure 8.19 shows a schematic circuit diagram of the test platform using the compensated model assisted SM testing scheme. Signals of the arm current and switching sequence of one SM (only indicates whether the SM is switched-in or bypassed while the gate signals are generated by the SM-level controller during the experiment) are recorded in computer simulation and used to run the test platform. The test platform uses a FB converter and a coupling inductor to synthesize the required arm current with current hysteresis control while sending the switching sequence into the SM under test. The FB converter, the coupling inductor (10 mH, 20 A_{dc}) and the auxiliary SM are the same ones adopted in Chapter 7. The dc supply voltage is set to 120 V. Detailed parameter selection for the test platform can refer to Chapter 7.2.

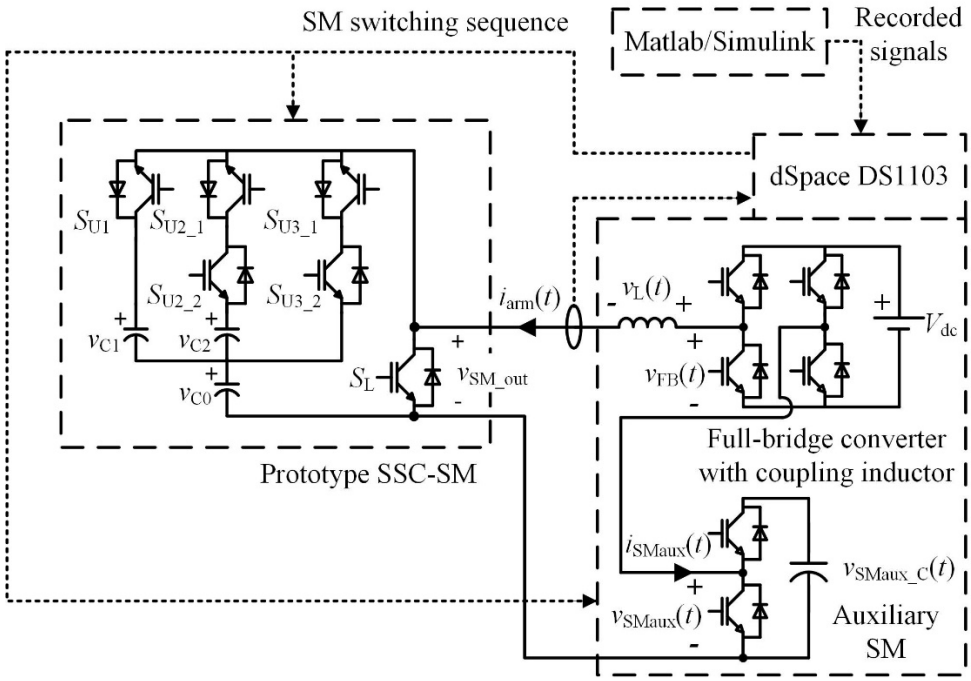

Figure 8.19: Schematic circuit diagram of the test platform using the compensated model assisted SM testing scheme

During the experiment, the backbone and supporting capacitor voltages as well as the 'arm current' are measured and sent to the dSpace DS1103. The SM-level controller runs in the dSpace platform generating the corresponding switching sequences for all six switchses according to the control diagram shown in Figure 8.7. The switching sequences are then sent to the RC switch-ON delay board as shown in Figure 8.20 to add a deadband with a duration of around 6 μs (R=1 kΩ, C=6.8 nF) to avoid shorting the capacitors. Details of the switching strategies during deadbands can be found in Table 8.1 and details of the RC switch-ON delay board are presented in Chapter 6.5. As marked by the hatched blue areas in Figure 8.8, in order to achieve the low-voltage switching to reduce switching losses, a short overlap time is added to the two upper main switches being switched. The duration of the overlap time can be similar to the deadband (a few microseconds). In the experiment, it is set to the shortest control cycle of the dSpace platform (ΔT=50 μs).

Figure 8.21 shows a top view of the test platform. The prototype SSC-SM is in the bottom right corner. As shown in Figure 8.3, the three upper switches (S_{U1}, S_{U2_1} and S_{U3_1}) and the two back-to-back connected switches (S_{U2_2} and S_{U3_2}) have a floating emitter channel. Hence, all six IGBT/diode modules are separately driven by six isolated gate drivers that can operate up to 1.2 kV. In the experimental prototype, the gate drivers have relatively large volume when compared with the SSC-SM itself. In a design of a full-scale SSC-SM for high-voltage high-power applications, through customized design the relative volume of the gate driver and control board is expected to be much smaller. Finally, Figure 8.22 shows the prototype test platform assembled in a protective enclosure.

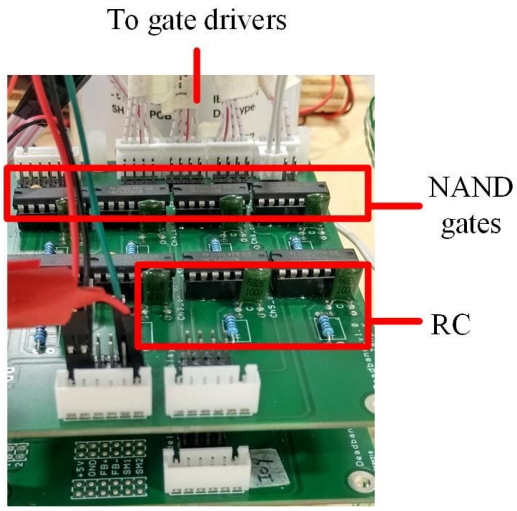

Figure 8.20: RC deadband board

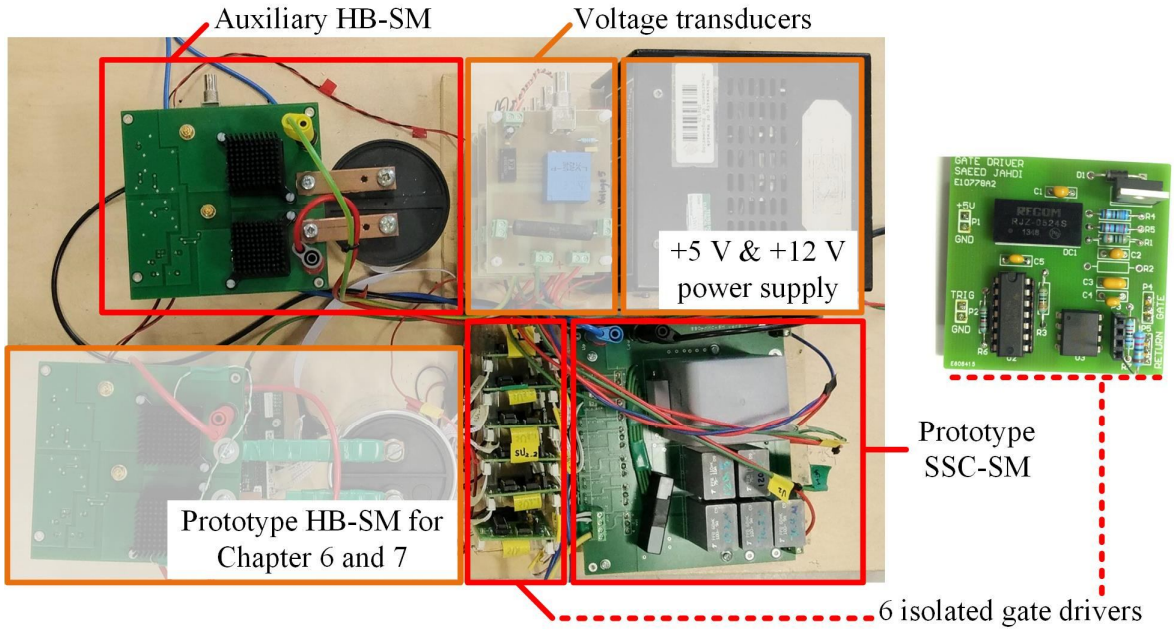

Figure 8.21: Top view of the test platform

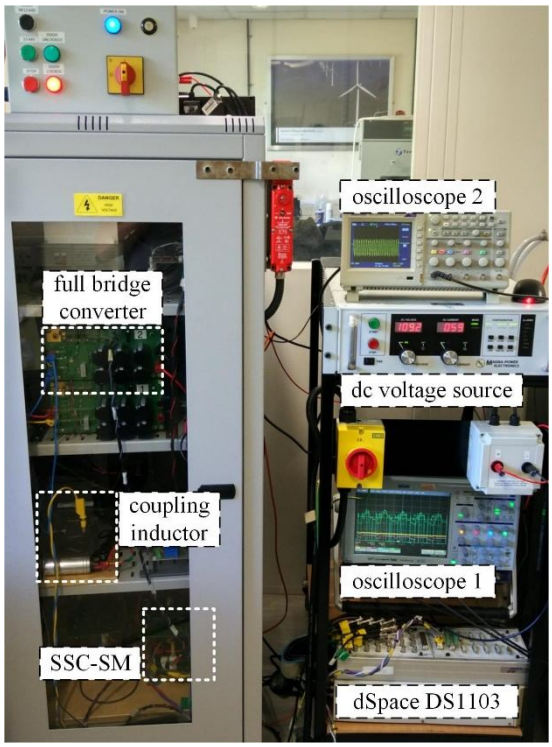

Figure 8.22: Prototype SSC-SM test platform installed in a protective enclosure

8.6.2 Experiment results

Figure 8.23 to Figure 8.26 give a set of oscilloscope snapshots during the test in rated power operation. SM output voltage (green), voltages of the backbone capacitor C_0 (red) and supporting capacitors C_1 (yellow) and C_2 (blue) are shown in Figure 8.23. All waveforms well agree with the theoretical analysis as depicted in Figure 8.6. The saw-tooth like waveform in green is the SM output voltage that is always controlled within the permitted range 0.12p.u. p-p (376 V to 424 V) when the SM is switched into the arm circuit. When the SM is bypassed, the SM output voltage will drop to near zero. The backbone capacitor voltage v_{C0} fluctuates at twice the range of the SM dc bus voltage. When v_{C0} is less than the minimum SM dc bus voltage (376 V), one supporting capacitor C_1 or C_2 will be switched in to compensate the gap and satisfy the voltage ripple requirement. The maximum voltage of C_1 is measured to be 72 V and that of C_2 is 48 V, both agreeing with the design calculations.

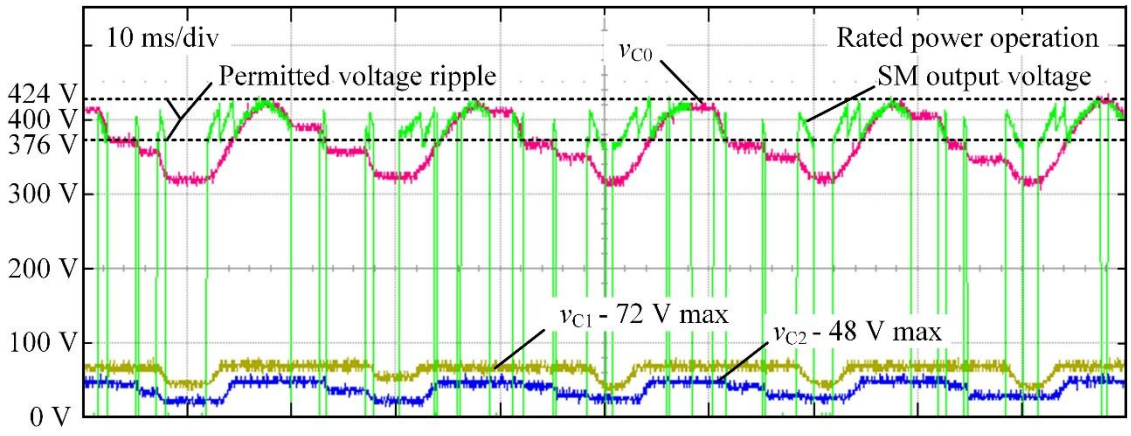

Figure 8.23: Experiment results (overall). Horizontal Axis: 10 ms/div. v_{C1}: 100 V/div, -2 div offset (yellow). v_{C2}: 100 V/div, -2 div offset (blue). v_{C0}: 100 V/div, -2 div offset (red). SM output voltage: 100 V/div, -2 div offset (green)

Figure 8.24 to Figure 8.26 show the validity of the low-voltage switching strategy given in Table 8.1 and Figure 8.8. In Figure 8.24, the collector-emitter voltage of S_{U1} is measured under rated power operation (in red). Again, the saw-tooth like waveform in green is the SM

output voltage; the upper square waveform in blue at the bottom is the gate signal for S_{U1} and the lower square waveform in yellow indicates the SM being switched-in or bypassed. As shown in Table 8.2, the voltage to be blocked by S_{U1} is the highest and is the sum of v_{C1} and v_{C0}. If both capacitors are fully charged, $v_{CE}(S_{U1})$ will be 496 V (72 V+424 V) while the maximum experimental measurements is 500 V. The highest switching voltage for S_{U1} is always less than the maximum SM dc bus voltage as marked by (A). In other words, no higher switching losses will be caused in S_{U1} when compared with the S_U in a HB-SM. During switching the supporting branches, with the proposed low-voltage switching strategy as shown in Figure 8.8, the switching voltage of S_{U1} is always the maximum voltage difference between v_{C1} and v_{C2} or (48 V=72 V–24 V) as marked by (B). Note that the SM output voltage shown by the saw-tooth like waveform is also the collector-emitter voltage of the lower switch S_L. With the proposed switching strategy as listed in Table 8.1, the voltage on S_L is ensured to be within the maximum SM dc bus voltage at all times.

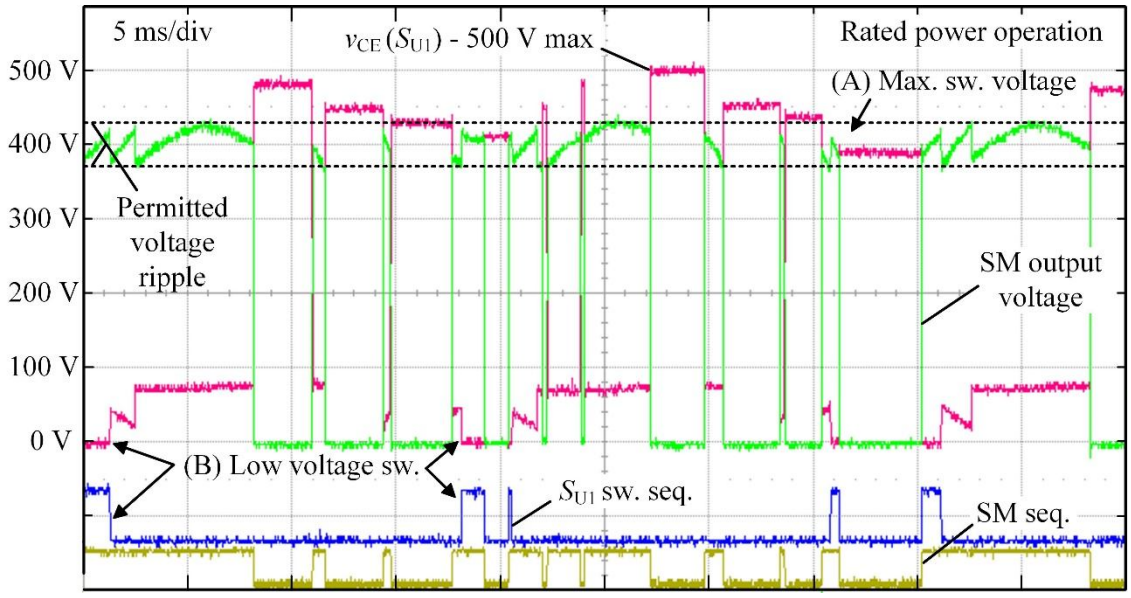

Figure 8.24: Experiment results (S_{U1}). Horizontal Axis: 5 ms/div. SM switching sequence (yellow). S_{U1} switching sequence (blue). $v_{CE}(S_{U1})$: 100 V/div, -2 div offset (red). SM output voltage: 100 V/div, -2 div offset (green)

Figure 8.25 shows the collector-emitter voltage of S_{U2_1} under rated power operation (in red) together with its switching sequence (upper square waveform in blue). Similar to S_{U1}, S_{U2_1} also needs to block the total voltage of two capacitors, C_2 and C_0. The maximum voltage is 472 V (48 V+424 V) as verified in the experiment (475 V max.). The maximum switching voltage for S_{U2_1}, as marked by (A) is also within the maximum SM dc bus voltage. Different from S_{U1}, S_{U2_1} will not only switch at low voltage but even zero voltage during the switching between supporting branches. When the SSC energy buffer switches between phase 1 and phase 2 as marked by (C), the switching voltage of S_{U2_1} is zero ignoring the ON-state voltage. In another case when the energy buffer switches between phase 2 and phase 3 as marked by (B), the switching voltage of S_{U2_1} is the maximum of C_2 or 48 V. Again, all experiment measurements well agree with the analysis.

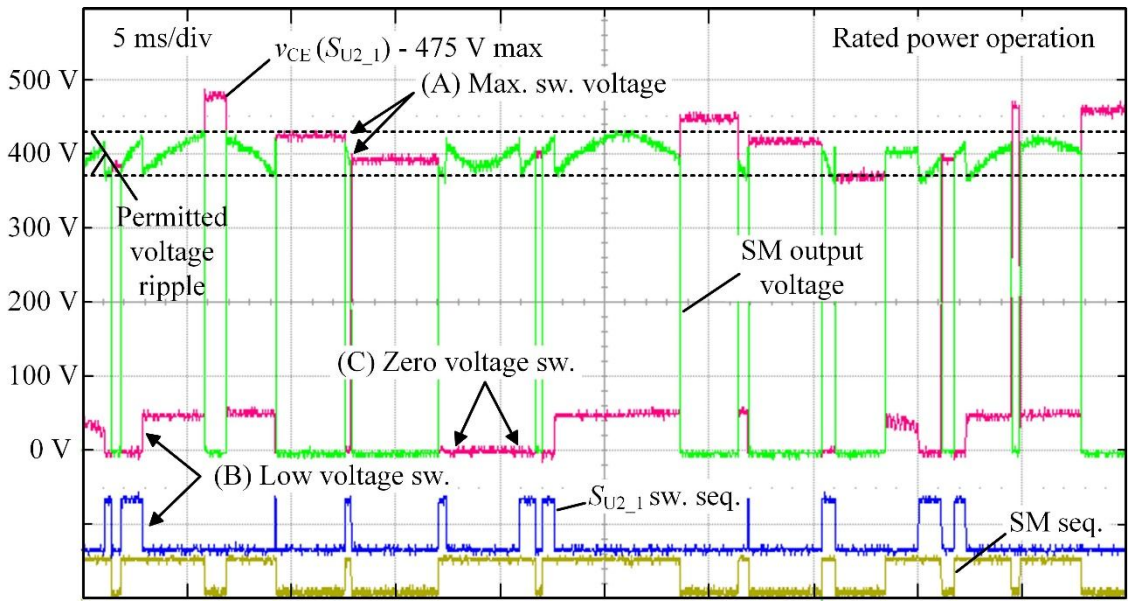

Figure 8.25: Experiment results (S_{U2_1}). Horizontal Axis: 5 ms/div. SM switching sequence (yellow). S_{U2_1} switching sequence (blue). V_{CE}(S_{U2_1}): 100 V/div, -2 div offset (red). SM output voltage: 100 V/div, -2 div offset (green)

Finally, the voltage of S_{U3_1} is shown in Figure 8.26 in red with its switching sequence in blue. Different from S_{U1} and S_{U2_1}, S_{U3_1} only needs to block the voltage of the backbone capacitor C_0. Hence, the maximum value of $v_{CE}(S_{U3\_1})$ is measured to be the maximum SM dc bus voltage as marked by (A). During switching the supporting branches, with the proposed low-voltage switching strategy, the switching voltages of S_{U3_1} are always measured to be close to zero as marked by (B). The small voltage fluctuations while S_{U3_1} is turned OFF are due to the parasitic inductance in the board indicating the demand of optimized circuit or packaging design.

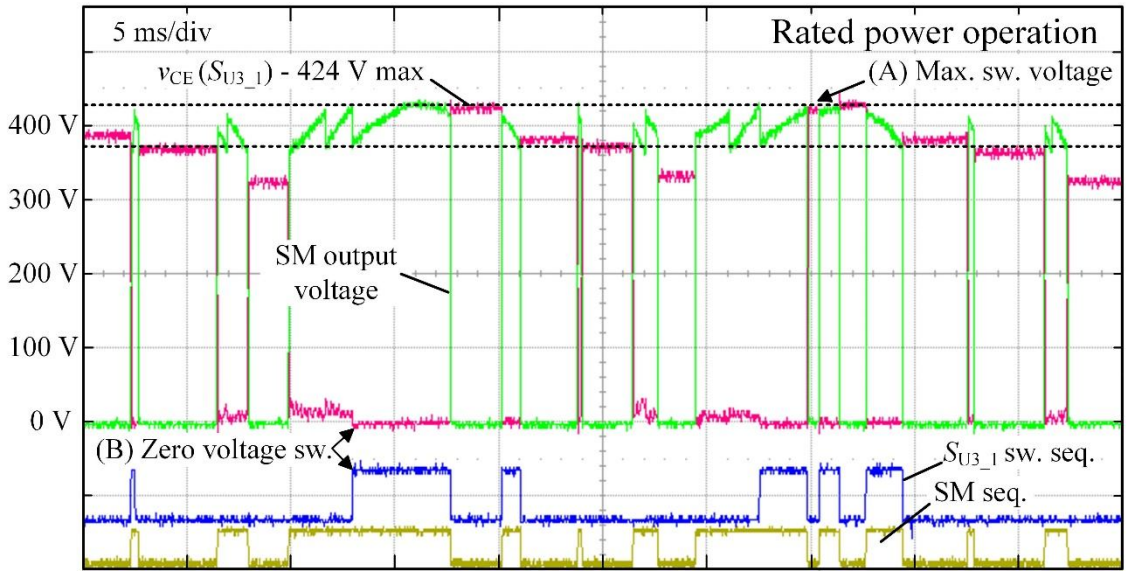

Figure 8.26: Experiment results (S_{U3_1}). Horizontal Axis: 5 ms/div. SM switching sequence (yellow). S_{U3_1} switching sequence (blue). $v_{CE}(S_{U3\_1})$: 100 V/div, -2 div offset (red). SM output voltage: 100 V/div, -2 div offset (green)

8.7 Extended Study: Partial Operating Mode

As shown in Figure 8.27 and 8.28, due to the intermittency of wind or wave resources, the power output of offshore wind or wave farm seldom reaches the rated capacity. For around 60% of the time, the output power of the wind farm shown in Figure 8.27 operates at less than half of the rated capacity. The figure for the wave farm shown in Figure 8.28 is even close to 90%. In such cases, the operating power of the offshore converter for renewable power collection will be much lower than the rated capacity as well. As a result, the SM dc bus voltage ripple will be much smaller than the permitted range. In order to reduce the additional losses due to switching the supporting branches, the SSC-SM can operate with only two or even one supporting branch. As a result, the SM dc bus voltage ripple will increase but will be still within the permitted range.

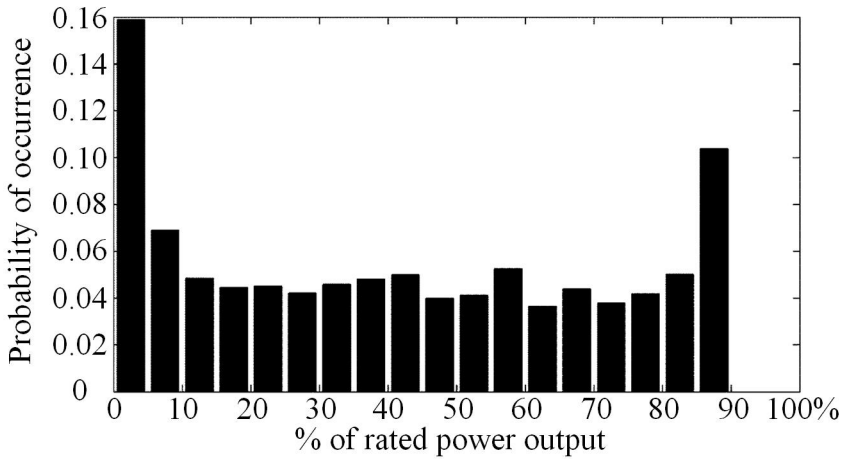

Figure 8.27: Annual histogram of rated power output states of an offshore wind farm at buoy 46030 [148]

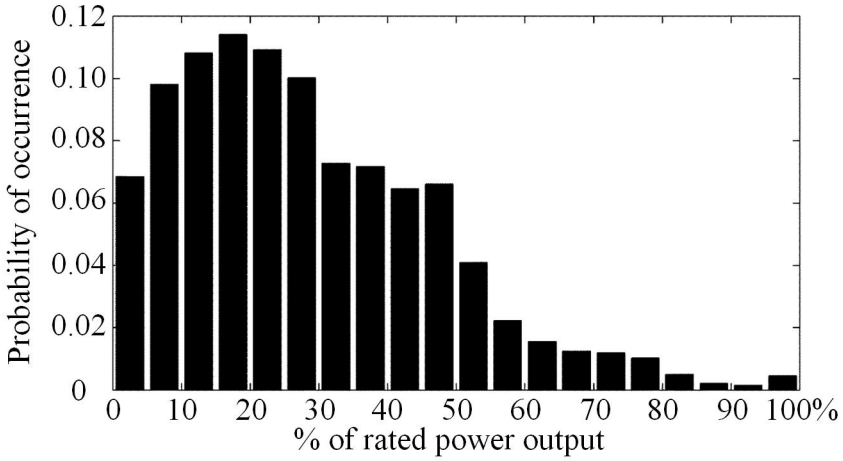

Figure 8.28: Annual histogram of rated power output states of a wave farm at buoy 46030 [148]

8.7.1 Partial operating mode: control strategy

Table 8.9 offers one possible control strategy to combine the partial operating mode with the full operating mode. $V_{\text{ripplep.u.}}$ is the estimated SM dc bus voltage ripple using (8.4) in real time. The corresponding converter active power P is shown in the second column, which is compared with its rated value P_{r}. As shown in Figure 8.9 and (8.3), the SM dc bus voltage ripple depends on not only the converting power but also the operating point (m, φ). For simplicity, in the 2nd to 4th column in Table 8.9, only the active power is considered and the reactive power is assumed zero. When $V_{\text{ripplep.u.}}$ is larger than 75% of $V_{\text{ripplep.u._r}}$, all three branches are used and the energy buffer operates in the full operating mode with waveforms shown in Figure 8.6. When $V_{\text{ripplep.u.}}$ is 50% to 75% of $V_{\text{ripplep.u._r}}$, the energy buffer will operate between phase 2 and phase 3. In such a case, due to the absence of C_1 branch, the rated power of the converter system drops to 75% of the nominal value, assuming C_1, C_2 and C_0 all equal to half of C_{ori}. Hence, $V_{\text{ripplep.u.}}$ sent to the controller will be scaled up by a factor of (1/0.75). When $V_{\text{ripplep.u.}}$ is less than 50% of $V_{\text{ripplep.u._r}}$, the backbone capacitor will be switched in at all times. $V_{\text{ripplep.u.}}$ will be further scaled up by a factor of (1/0.5). In such a

case, there is no switching between supporting capacitors and the SSC-SM operates similar to a conventional HB-SM. When $V_{\text{ripplep.u.}}$ further reduces to less than 25% of $V_{\text{ripplep.u.\_r}}$, the SSC-SM can operate with phase 1 only. By doing that, the additional conduction loss can be eliminated due to the absence of the back-to-back connected switch in the C_1 branch. In all cases, the SM dc bus voltage ripple is within the permitted range $V_{\text{ripplep.u.\_r}}$. As shown in the 3rd and 4th column in the table, for 36% and 50.4% of the time in offshore wind and wave power integration, the transmitted power is less than 25% of the rated value. In such a case, the SSC-SM based MMC would operate similar to a conventional MMC without additional power losses. Note the power levels for the mode-switching are derived when all the back-bone and supporting capacitors have the same capacitance. In practice, their capacitance values can be optimized in a way that the converter system could operate as a conventional MMC in most of the time and only when the power goes higher than a certain value, the converter will turn to the SSC-mode at the expenses of slightly higher power losses.

$V_{\text{ripplep.u.}}$ / $V_{\text{ripplep.u.\_r}}$[a]	P/P_r[b]	% Time wind Figure 8.28	% Time wave Figure 8.29	C_1 branch	C_2 branch	Cap-free branch	$V_{\text{ripplep.u.}}$ to controller
> 0.75	> 75%	20.7%	2.3%	Enable	Enable	Enable	(8.4)
≤ 0.75	≤ 75%	21.1%	10%	Disable	Enable	Enable	(8.4)/0.75
≤ 0.50	≤ 50%	22.2%	37.3%	Disable	Disable	Enable	(8.4)/0.50
≤ 0.25	≤ 25%	36%	50.4%	Enable	Disable	Disable	(8.4)/0.25

([a]Defined in (8.4); [b]$P_{(r)}$ is converter (rated) active power, reactive power is assumed zero in this example)

Table 8.9: Partial operating mode strategy of the SSC-SM energy buffer

8.7.2 Partial operating mode: simulation results

The partial operating mode is integrated into the controller of the 21-level SSC-SM based MMC simulation model presented in Chapter 8.5. Figure 8.29 gives the voltage waveforms of an SSC-SM when the active power of the converter (P_{ac}) drops from the rated -19.1 MW

(rectifying) to 0.3p.u. (-5.73 MW) and then gradually increases back to the rated power. The reactive power (Q_{ac}) is kept at 0. This is to imitate the behavior of an offshore converter designed for renewable power collection during load changes. At 0.04 s, when the power drops to 0.3p.u., the estimated voltage ripple derived by (8.4) also drops to 30% of $V_{ripplep.u.\_r}$. Both C_1 and C_2 branches are deactivated [Figure 8.29 (c)] leaving only the backbone capacitor C_0 directly connected to the SM dc bus through the capacitor free branch. In such a case, the SSC-SM operates in the same way as a HB-SM [Figure 8.29(b)]. At 0.16 s, the power rises to 0.6p.u. (-11.5 MW). According to (8.4) and Table 8.9, the backbone capacitor alone can no longer limit the SM dc bus voltage ripple within the allowable range. C_2 branch is activated while C_1 branch is still idle [Figure 8.29(c)]. In such a case, in each fundamental cycle, there are only three ripples in the SM dc bus voltage [solid red line in the dashed box in Figure 8.29(b)] instead of five as in the rated power operation. At 0.25 s, the converter goes back to rated power with all three supporting branches being used.

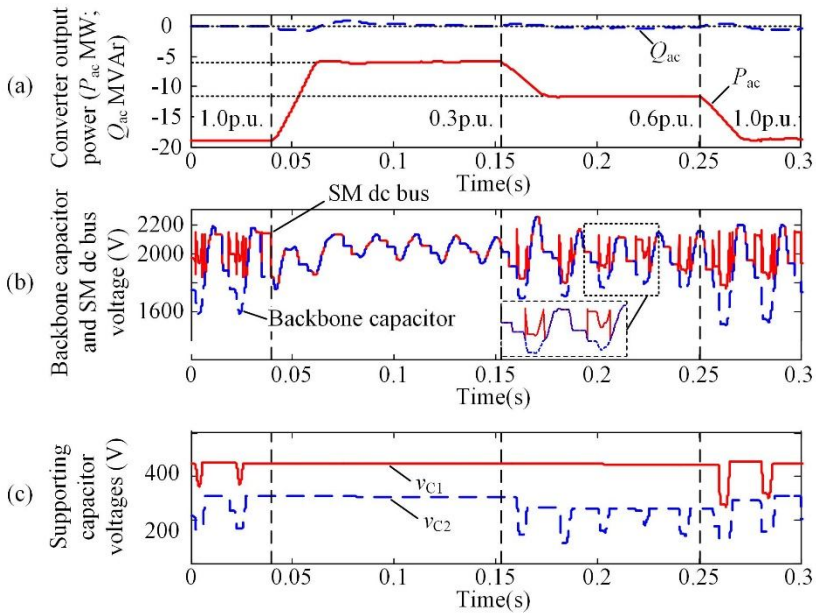

Figure 8.29: Simulation waveforms in partial operating mode: (a) converter output power; (b) backbone capacitor voltage (in dashed blue) and SM dc bus voltage (in solid red); (c) supporting capacitor voltages (solid red for v_{C1} and dashed blue for v_{C2})

8.7.3 Partial operating mode: experiment results

The partial operating mode is also integrated into the controller of the prototype SSC-SM to verify the controller design through experiment. Figure 8.30 shows the voltage and current waveforms of the prototype SSC-SM during load changes: the 'arm current' increases from 0.3p.u. to 0.6p.u., and finally to 0.8p.u. When the 'arm current' is less than 50% of the rated value, according to Table 8.9, the backbone capacitor C_0 alone can limit the SM dc bus voltage within the permitted range. Hence, both supporting capacitors are bypassed [Figure 8.30(c)] leaving only C_0 in operation [Figure 8.30(a) and (b)]. At 0.15 s, when the 'arm current' goes higher than 0.5p.u., C_2 is put into operation while C_1 is still idle as shown in Figure 8.30(c). In such a case, C_1 will be automatically charged to the maximum voltage of C_2 and then stay constant. As can be seen in the zoomed view (a2) in Figure 8.30(a), the SM dc bus voltage has three ripples in a fundamental cycle T due to the switching between C_2 and the capacitor-free branch. When the 'arm current' increases to higher 75% of the rated value, all three supporting branches are in use. As shown in Figure 8.30(c), both C_1 and C_2 are activated and the SM dc bus voltage is still controlled to be within the permitted region [Figure 8.30(a)]. The maximum voltages of C_1 and C_2 are controlled according to the real-time permitted voltage ripple derived in (8.4) to be 57.6 V (0.8×72 V) and 38.4 V (0.8×48 V) respectively. All experimental measurements well agree with the calculations.

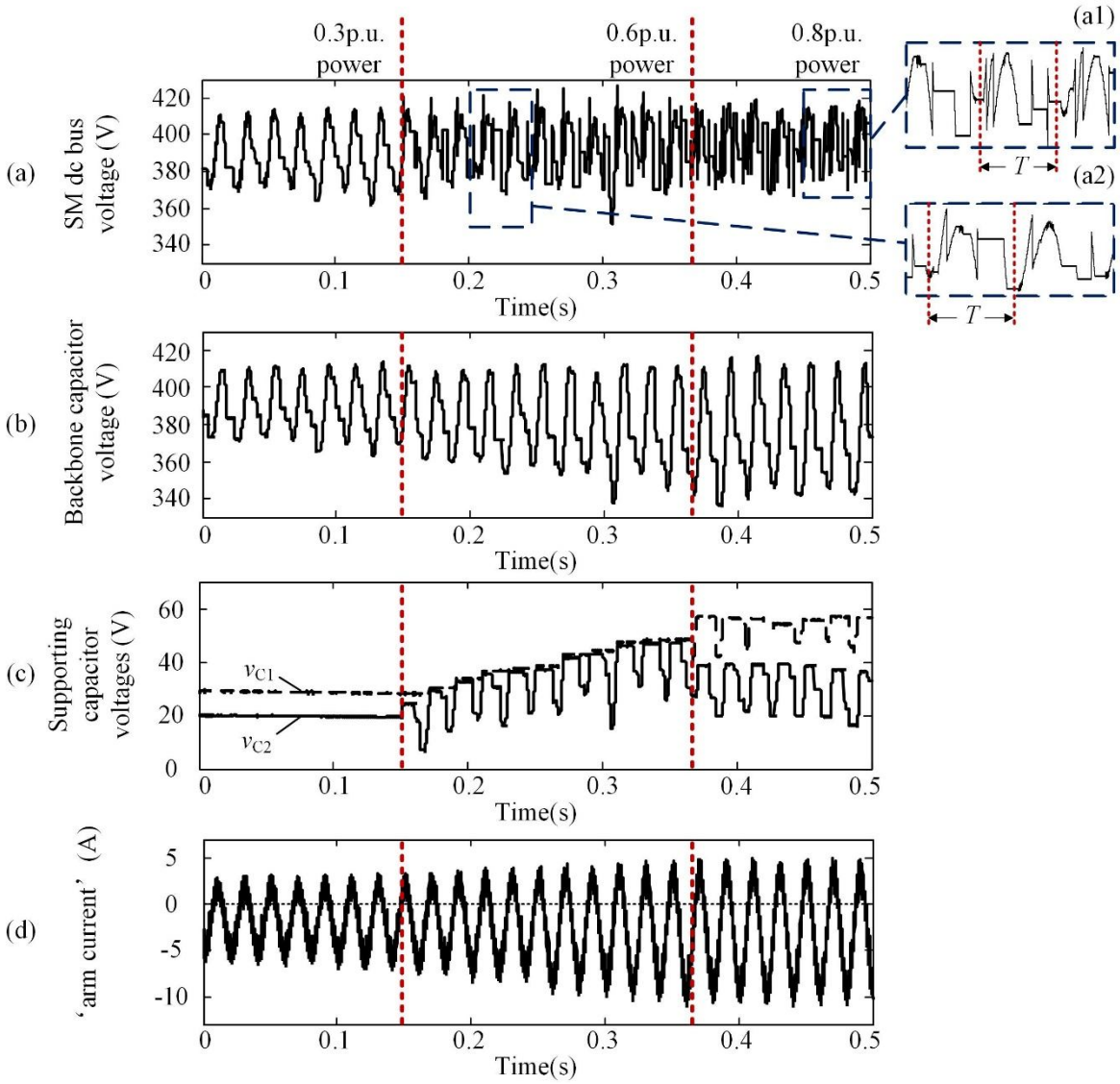

Figure 8.30: Experiment waveforms of the prototype SM during load changes: (a) SM dc bus voltage; (b) backbone capacitor voltage; (c) supporting capacitor voltages and (d) 'arm current' generated by the FB converter

8.8 Discussion on Power Loss

As shown in the loss simulation (Figure 8.15), an SSC-SM based MMC will increase the power loss by 7% in the rectifier mode, which is of interest for an offshore wind or tidal power collection system. From the economics point of view, the impacts of the additional losses can be evaluated as follows. Firstly, the total semiconductor device losses of a HB-SM based MMC (ac/dc or dc/ac) account for about 0.56% of the rated power. If the converter operates at the rated power all the year (8760 hours), the additional losses (7%) in terms of electricity sales are estimated to be £155 per MW converter capacity, assuming an average electricity wholesale price in UK of £45/MWh [149, 150]. If the service life of the converter system is 25 years, the total cost due to the additional energy loss is £3.88k/MW. According to [151], the capital costs of the converter equipment (VSC based) are usually £160k/MW. It can be shown that if the cost of all SM capacitors accounts for more than 6% of the total capital cost, the MMC system based on SSC-SM will be preferable than the HB-SM based system. Moreover, due to the intermittency of wind or tidal resources, the offshore converter seldom operates at its rated capacity. Both Figure 8.28 and 8.29 indicate a very low capacity factor for offshore applications. The total cost due to the additional energy loss can be as low as £1k/MW for the entire service lifetime (25 years) with 25% capacity factor, making the SSC-SM based system even more attractive. Furthermore, the above has not considered the fact that the offshore platform will cost much more than the converter itself [152]. A cheaper offshore platform can be adopted due to the lighter and more compact SSC-SMs. Moreover, the partial operating mode can help to reduce the additional power losses. Finally, the power losses of semiconductor devices will be much lower and no longer a major problem in the future due to developments such as SiC for high voltage applications.

8.9 Summary

This chapter proposes a compact SM topology for the MMC based on *1-2 enhanced unipolar* SSC energy buffer architecture. The physical volume of all capacitors in one proposed SSC-SM is only 60% of the one in an original HB-SM with 2000 V SM rated dc voltage and 0.15p.u. p-p voltage ripple. Computer simulation shows the performance of the SSC-SM based MMC system in both steady state and transient, which are very close to the HB-SM based system. Modulation algorithm, capacitor voltage balancing and sorting controllers of the HB-SM based system can be used with only slight modifications. The switching of the supporting branches is controlled locally within each SM. The major disadvantage of the SSC-SM based system is the increase of losses by 7% to 15% at rated power operation. Nevertheless, when the converter operates at less than 50% of the rated power, the SSC-SM almost reduces to a HB-SM. This feature will be beneficial to applications with stringent footprint and weight requirements, such as offshore converters for wind or wave power integration. In such a case, the converter will operate as a HB-SM based MMC system in most of the time and only when the power goes higher than a certain value, the converter will turn to the SSC-mode at the expenses of slightly higher power losses. In this sense, SSC can be used as an effective way to address the unusual, extreme conditions in operation. Experiments on a prototype SSC-SM verify the validity of the design as well as the effectiveness of the SM-level controller and the low-voltage switching strategy.

9 CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

The focus of this thesis lies in the SM dimensioning, testing method and topology innovation of the MMC for its applications including offshore renewable power collection and onwards transmission.

In Chapter 3, properties and characteristics of electrolytic capacitors, ceramic capacitors and film capacitors are reviewed and compared. Although electrolytic capacitors have very high energy density, they are being phased out in modern power electronics due to their short lifetime, high ESR, low ripple current capability and high explosion rate. Different ceramic capacitors have different properties depending on the dielectric. In the future, ceramic capacitors could very well be the game changers in high-voltage high-power applications. However, due to their small capacitance (<100 μF), and most importantly, due to their high ESR at low frequencies, ceramic capacitors do not make for a suitable option for MMC SMs

with low switching frequencies. On the other hand, one type of film capacitors, the MPPF capacitors, is found to be suitable for MMC SMs due to their long lifetime, low ESR at low frequencies, high ripple current capability and stable property over a wide variety of temperature and voltage ranges. Their energy density can be up to 350 J/litre when their rated voltage is higher than 1000 V. For MPPF capacitors with lower rated voltages, the energy density will be lower. MPPF capacitors will usually have 100 mA/μF to 400 mA/μF ripple current capability; however, the ripple current capability for some designs can be as low as 10 mA/μF. The understanding of the energy density and ripple current capability properties will be helpful in capacitor selection and system design. Ageing mechanisms of MPPF capacitors are also reviewed in this chapter. The study shows that the maximum capacitor voltage, capacitor voltage ripple and current ripple stress during design must be taken into consideration.

In Chapter 4, a novel SM capacitor selection method is presented. An analytical model of SM capacitor voltage ripple is developed. Based on the model, the required SM capacitance can be derived to satisfy three voltage requirements: the maximum capacitor voltage, the capacitor voltage ripple and the SM voltage capability requirements. The first two requirements are to ensure safe operation of the capacitor while the last is to ensure that there is always enough voltage storage in the converter arms for output. Short of arm voltage will lead to distorted output waveforms and cause disturbances. Hence, the SM voltage capability requirement must be addressed, especially when the converter is designed to absorb lagging reactive power from the grid. The effect of arm inductor is considered in the design. A quick and accurate way to estimate the capacitor ripple current stress is also presented. A few design curves are generated to give a comprehensive understanding of how the operating point of the converter and different design variables will affect the capacitance demands and capacitor ripple current stress. Fast manual calculations are achievable with the simplified

equations and design curves.

As a conclusion of Chapter 5, the 50/3 Hz ac is a promising candidate for offshore power transmission with distances from 100 km to 250 km. The major advantage is the possibility of building a multiterminal offshore network with mature ac circuit breakers and transformers. The major problem is the larger and heavier low-frequency transformers. In addition, the B2B MMC is found to be a good option for frequency conversion between 50/3 Hz and 50 Hz ac. It has excellent ac fault ride-through capability, but the major problem is the larger and heavier SM capacitors in the 50/3 Hz side of the converter due to the low operating frequency. This type of converter will greatly benefit from SM capacitor reduction techniques.

In Chapter 6 and Chapter 7, two model assisted SM testing schemes are presented. With the proposed methods, the prototype SM can be thoroughly tested without a complete MMC. Different from the published testing methods, in the proposed testing schemes, both the SM switching sequence and the 'arm current' can be faithfully achieved simultaneously. The 'arm current' could contain not only the fundamental frequency component but also the dc offset and the harmonic circulating current components. The uncompensated testing scheme presented in Chapter 6 uses fewer devices, and has simpler control and faster transient dynamics. The compensated testing scheme presented in Chapter 7 requires much lower dc supply voltage, smaller coupling inductance, and provides higher current tracking accuracy in steady state. The two testing methods can be used collaboratively in different development stages of a prototype SM. It is believed that the proposed testing schemes can effectively shorten the development cycle of a prototype SM and largely reduce the research costs.

In Chapter 8, a compact SM topology for MMCs based on *1-2 enhanced unipolar* SSC energy buffer architecture is presented. The physical volume of all capacitors in one proposed SSC-SM is only 60% of the one in an original HB-SM with 2000 V SM rated dc

voltage and 0.15p.u. peak-to-peak voltage ripple. The major disadvantage of the SSC-SM based MMC is the increase of losses by 7% to 15% at rated power operation. However, when the converter operates at less than 50% of the rated power, the SSC-SM almost reduces to a HB-SM. This feature will be beneficial to applications with stringent footprint and weight requirements, such as offshore converters for wind or wave power integration. In such a case, the converter will operate as a HB-SM based MMC system in most of the time and only when the power goes higher than a certain value, the converter will turn to the SSC-mode at the expenses of slightly higher power losses. In this sense, SSC can be used as an effective way to address the unusual, extreme conditions in operations.

9.2 Future Work

Firstly, the SM capacitor selection method proposed in this thesis only considers one certain case with assumptions that all harmonic circulating currents are eliminated and the arm voltage only contains fundamental frequency component. It will be beneficial to generate more sets of design curves to include the effects of the harmonic circulating currents and third order harmonic voltage injection using the proposed method. Those design curves will be helpful for researchers and engineers to have a clear understanding of how the above factors will affect the capacitor demands and how they will limit the operating region of the converter.

In addition, the analytical model of SM capacitor voltage ripple for capacitor selection is derived using a time-average model. An important feature of the MMC is, however, its low switching frequency indicating that some important details may be left out in the time-average model. It will be valuable to perform an analysis on the impacts of the switching actions on the capacitance demand functions as well as the ripple current stress function.

After that, the thesis evaluates the 50/3 Hz ac for offshore power transmission. The

reason for choosing the 50/3 Hz as the operating frequency is its popularity in European traction systems. As the operating frequency reduces, the transmission distance will further increase, but will also lead to larger and heavier coupling transformers and passive components in the frequency converter. A detailed study can be carried out to look for an optimized operating frequency considering not only the transmission distance and capacity but also the costs of the transformer, the offshore platform, the frequency converter, etc.

Then, a high-level design of a B2B MMC for the frequency conversion is presented. The study found that the conventional HB-SM based MMC is not likely to be a suitable option for applications with very low operating frequencies. Otherwise, its SM capacitors will be excessively large. The compact SM structure based on SSC architecture proposed in Chapter 8 can be a solution. Other available converter topologies shall be considered as well such as the modular matrix converter. A detailed comparison between different technologies is required including loss analysis for high-power applications. Besides, dynamic control of the B2B MMC is worth further study as well. Due to the absence of a long dc link, control of one side of the B2B MMC can base on the operating status of the other side instead of the dc bus measurements. Feedforward and predictive control algorithms may help to increase the control dynamics.

In Chapter 6 and Chapter 7, two model assisted SM testing schemes are presented. However, due to the lack of a powerful real-time simulator, the two prototype test platforms are based on the offline testing scheme. If such a real-time simulator is available, it will be valuable to build a test platform based on the online testing scheme. Testing tasks such as investigating the SM's responses during converter load changes and under fault conditions can be performed so long as the desired 'arm current' can be generated by the current source. Another direction to improve the SM testing scheme is to investigate advanced current control techniques to reduce the current tracking error. In addition, it will be valuable to

estimate the current tracking error in order to develop an error compensation method.

Finally, a compact MMC SM structure based on the SSC architecture is proposed. Note that this structure is only based on one embodiment of the SSC architecture. It will be valuable to look into other embodiments such as *n-m enhanced bipolar* structure to achieve much higher energy density for applications with very stringent footprint and weight requirements, such as motor drives for electric vehicles or wind power generators. In addition, in order to reduce the impacts of the additional power switches, it will be beneficial to integrate all semiconductor switches into a single customized module using innovative chip arrangements and advanced packaging techniques. Finally, the switching between supporting branches in SSC-SMs will lead to additional harmonic distortions in converter ac outputs. Advanced MMC control strategies, such as predictive control, can be implemented to cancel the additional voltage ripple and achieve smoother arm voltage outputs.

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