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Physics-Based Modelling and Experimental Characterisation of Parasitic Turn-On in IGBTs

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Keywords

«IGBT Parasitic Turn-On Modelling», «Temperature Dependent», «Shoot-through Current», «Voltage Source Converter», and «Miller Capacitor».

Abstract

As power electronic engineers increase the switching speed of voltage source converters for the purpose of higher power density, the *dI/dt* and *dV/dt* across the power semiconductors increases as well. A well-known adverse consequence of high *dV/dt* is parasitic turn-on of the power device in the same phase leg as the device being triggered. This causes a short circuit with high shoot-through current, high instantaneous power dissipation and possibly device degradation and destruction. It is critical for converter designers to be able to accurately predict this phenomenon through diagnostic and predictive modelling. In this paper, a physics-based device and circuit model is presented together with experimental results on parasitic turn-on of IGBTs in voltage source converters. Because the model is physics based, it produces more accurate results compared with compact circuit models like SPICE and other circuit models that use lumped parameters. The discharge of the Miller capacitance is simulated as a voltage dependent depletion capacitance and an oxide capacitance as opposed to a lumped capacitor. The model presented accurately simulates IGBT tail currents, PiN diode reverse recovery and the non-linear miller capacitance all of which cannot be solved by lumped parameter compact models. This is due to the fact that the IGBT current in the model is calculated using the Fourier series based re-construction of the ambipolar diffusion equation and the miller capacitances are calculated using fundamental device physics equations. This paper presents a physics-based device and circuit model for parasitic turn-on in silicon IGBTs by numerically modelling the minority carrier distribution profile in the drift region. The model is able to accurately replicate the transient waveforms by avoiding the use of lumped parameters normally used in compact models.

Nomenclature

C_{FB1}	Top IGBT feedback capacitance (F)	T_0	Room temperature (K)
C_{FB2}	Bottom IGBT feedback capacitance (F)	V_{CE1}	Top IGBT collector-emitter voltage (V)
I_{C1}	Top collector current (A)	V'_{CE1}	Top IGBT observed collector voltage (V)
I_{C2}	Bottom IGBT collector current (A)	V_{CE2}	Bottom IGBT collector-emitter voltage (V)

I'_{C1}	Top IGBT observed current (A)	V'_{CE2}	Bottom IGBT observed collector voltage (V)
I'_{C2}	Bottom IGBT observed current (A)	V_{DC}	DC link or supply voltage (V)
I_{G1}	Top IGBT gate current (A)	V_{GE1}	Top IGBT gate-emitter voltage (V)
I_{G2}	Bottom IGBT gate current (A)	V_{GE2}	Bottom IGBT gate-emitter voltage (V)
I'_{G1}	Top IGBT internal gate current (A)	V'_{GE1}	Top IGBT observed gate voltage (V)
I'_{G2}	Bottom IGBT internal gate current (A)	V'_{GE2}	Bottom IGBT observed gate voltage (V)
I_{RL}	Load current (A)	V_{gg1}	Top IGBT gate drive voltage (V)
K_p	MOSFET device transconductance (AV^{-2})	V_{gg2}	Bottom IGBT gate drive voltage (V)
K_{p0}	MOSFET device transconductance at room temperature (AV^{-2})	$V_{L_{s1}}$	Top IGBT stray inductance voltage (V)
L_{e1}	Top IGBT Kelvin emitter inductance (H)	$V_{L_{s2}}$	Bottom IGBT stray inductance voltage (V)
L_{e2}	Bottom IGBT Kelvin emitter inductance (H)	V_{RL}	Load voltage (V)
L_{G1}	Top IGBT gate stray inductance (H)	V_{th}	Threshold voltage (V)
L_{G2}	Bottom IGBT gate stray inductance (H)	V_{th0}	Threshold voltage at room temperature (V)
L_{s1}	Top IGBT stray inductance (H)	μ_n	Electron mobility ($cm^2V^{-1}s^{-1}$)
L_{s2}	Bottom IGBT stray inductance (H)	μ_{n0}	Low-field (maximum) electron mobility ($cm^2V^{-1}s^{-1}$)
R_{FB1}	Top IGBT feedback resistance (Ω)	μ_p	Hole mobility ($cm^2V^{-1}s^{-1}$)
R_{FB2}	Bottom IGBT feedback resistance (Ω)	μ_{p0}	Low-field (maximum) hole mobility ($cm^2V^{-1}s^{-1}$)
R_{G1}	Top IGBT gate resistance (Ω)	τ_{HL}	High-level carrier lifetime (s)
R_{G2}	Bottom IGBT gate resistance (Ω)	τ_{HL0}	High-level carrier lifetime at room temperature (s)
R_L	Load resistance (Ω)	τ_{lim}	Differentiator limiting time constant (s)
T	Temperature (K)		

I. Introduction

The drive to increase the power density in voltage source converters is enabled by higher switching frequencies for which higher switching speeds are necessary. The result of this is high *dI/dt* and *dV/dt* transients which cause undesirable effects like EMI and parasitic turn-on induced short circuits. The latter effect is the short circuiting of a phase leg due to unintentional turn-on of a power switching device that is acting under the influence of the complementing device in the same phase leg. In any power converter, the power devices in the same phase leg should never be switched on simultaneously however, if one device is switched rapidly with high *dV/dt*, the other device in the same phase leg can turn on as a result of the Miller capacitance discharge current which flows the gate drive circuit and initiates unintentional turn-on [1, 2]. This causes a high surge current capable of destroying the device that is being parasitically turned-on since a high voltage appears across the device, thereby resulting in very high instantaneous power dissipation. As the switching frequency is increased, the power dissipation related to this phenomenon increases significantly thereby increasing the operating temperature and reducing reliability.

Modeling parasitic turn-on in silicon IGBT and PiN diode circuits is important for diagnostic reliability evaluation. It is important for power electronics engineers to be able to predict the surge current as a function of the switching rates of the power devices. Compact based circuit models for IGBTs based on lumped parameters are not capable of accurately predicting the voltage and current waveforms under shoot-through conditions. This is because compact models use lumped capacitors to represent the Miller capacitance which is limited in the sense that the magnitude of the capacitance cannot vary with the voltage across the device. In a real device, the Miller capacitance is the series combination of an oxide capacitance and a depletion capacitance, hence, varies with voltage through the depletion width in the semiconductor. Other effects that cannot be captured by SPICE based compact models include the IGBT tail currents and PiN diode reverse recovery, both of which rely on the accurate calculation of stored charge in the drift region through the solution of the ambipolar diffusion equation. In this paper, the parasitic turn-on of an IGBT in a 2 level voltage source converter is modelled. The IGBT model is physics based and the drift-diffusion equations are solved with the continuity equations. The minority carrier distribution profile in the charge storage region responsible for the IGBT turn-off current transient is calculated using the Fourier series reconstruction of the ambipolar diffusion equation. Section II of the paper describes the IGBT model, section III describes

the circuit model, section IV describes the model discussion and results while section V concludes the paper.

II. IGBT Model Development

Multiple publications have detailed how the minority carrier distribution profile in the drift region of bipolar devices can be modelled using the Fourier series construction of Ambipolar Diffusion Equation (ADE) [3-16]. The IGBT model is developed based on the drift and diffusion equations of carriers and takes the displacement current into account. The minority carriers stored in the drift region of the IGBT is reconstructed using the Fourier series reconstruction of ADE. The model takes conductivity modulation, Schockley-Read-Hall recombination, Auger recombination, carrier-carrier scattering, depletion layers behavior and local lifetime into account. Hence, it provides more details about the charge stored in the drift region which consequently provides details of the switching transient and can more accurately model the *dV/dt* across the device during the IGBT turn-on. Moreover, the Miller capacitance in the model is nonlinear and is based on the behavior of the device rather than having a lumped value that some circuit simulators such as SPICE use. The voltage drop across the IGBT in the drift region is calculated based on the concentration of carriers in the drift region and the background doping of the device. Two dimensional solution to the ADE is required to achieve matching between the simulation and experiments during turn-on of the IGBT. Two dimensional ADE is:

$$D\left(\frac{\partial^2 p}{\partial y^2}+\frac{\partial^2 p}{\partial x^2}\right)=\frac{p}{\tau}+\frac{\partial p}{\partial t} \tag{1}$$

The Fourier series solution to the two dimensional ADE can be written using two frequencies, m and n, which comes from the sinusoidal terms in two dimensions. In this equation, W is the boundary in x direction from the P-emitter towards the P-well and MOS region (width of the device) and L is the boundary in y direction from the mid-point of the P-well to the middle of the region under the gate.

$$p(x,y,t)=\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}p_{mn}(t)\cos\left(\frac{m\pi x}{W}\right)\cos\left(\frac{n\pi y}{L}\right) \tag{2}$$

For $m>0,\ n>0$:

$$\frac{4D}{W}\left[\left.\frac{\partial p}{\partial x}\right|_{WP}-\left.\frac{\partial p}{\partial x}\right|_{WT}\right](-1)^m\sin(n\pi\beta)=\frac{dp_{mn}}{dt}+p_{mn}\left[\frac{1}{\tau}+D\pi^2\left(\frac{m^2}{W^2}+\frac{n^2}{L^2}\right)\right]-\frac{2}{W}\frac{dW}{dt}\left[\frac{p_{mn}}{4}+\sum_{\substack{i=1\\ i\neq m}}^{\infty}\frac{i^2}{i^2-m^2}p_{in}(-1)^{i+m}\right] \tag{3}$$

For $m=0,\ n>0$:

$$\frac{2D}{W}\left[\left.\frac{\partial p}{\partial x}\right|_{WP}-\left.\frac{\partial p}{\partial x}\right|_{WT}\right]\frac{\sin(n\pi\beta)}{n\pi}=\frac{dp_{0n}}{dt}+p_{0n}\left[\frac{1}{\tau}+\frac{D\pi^2 n^2}{L^2}\right]-\sum_{i=1}^{\infty}\frac{p_{in}}{W}\frac{dW}{dt}(-1)^i \tag{4}$$

For $m=0,\ n=0$:

$$\frac{D}{W}\left[\beta\left.\frac{\partial p}{\partial x}\right|_{WP}+(1-\beta)\left.\frac{\partial p}{\partial x}\right|_{WT}-\left.\frac{\partial p}{\partial x}\right|_{0}\right]=\frac{dp_{0n}}{dt}+\frac{p_{0n}}{\tau}-\sum_{i=1}^{\infty}\frac{p_{i0}}{W}\frac{dW}{dt}(-1)^i \tag{5}$$

Fig. 1 shows the reconstruction of the ambipolar diffusion equation in the drift region of an IGBT at different instances of time during the turning-off of the IGBT. As can be seen, the charge is depleted and recombined in the drift region and the depletion region is shaped as the device switches off.

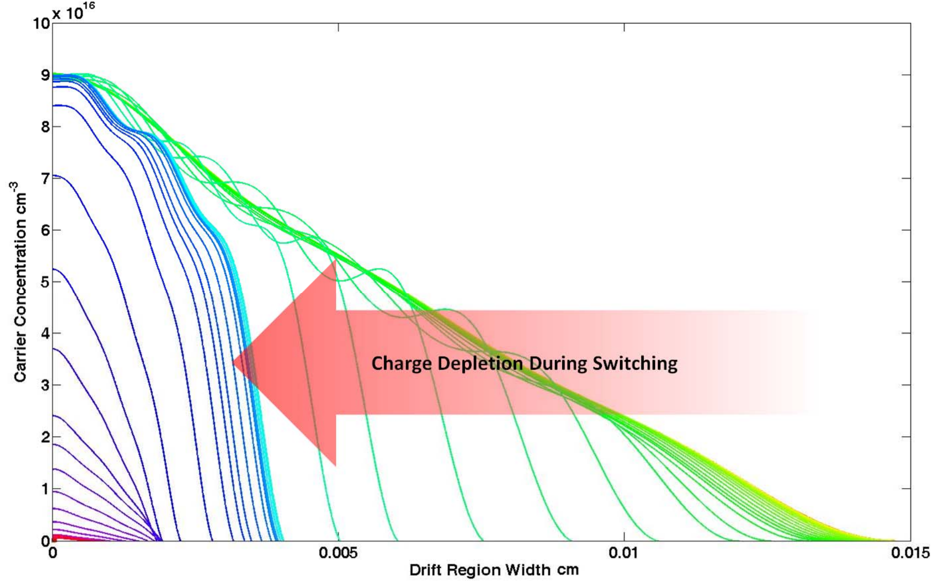


Fig. 1: Simulation results showing the reconstruction of the ambipolar diffusion equation in the drift region of an IGBT during the switch-off of the device and the formation of the depletion region during the switching.

III. Half Bridge Model Development

Fig. 2 shows diagram of a half-bridge circuit including all the parasitic inductances and gate resistors. This circuit is used in the test rig to capture the waveforms of the IGBT when the parasitic turn-on phenomenon occurs in the bottom IGBT. By applying Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) at the nodes and loops of the circuit diagram below, equations 6-21 can be obtained.

In the diagram above, the feedback capacitors and resistors (C_{FB1}, C_{FB2}, R_{FB1} and R_{FB2}) may be used to improve model convergence. The stray inductance is lumped into L_{s1} and L_{s2} for the top and second IGBTs respectively. The gate resistors and Inductors are R_{G1}, R_{G2}, L_{G1}, L_{G2} respectively for IGBT 1 and IGBT 2. The load resistance is R_L and is 1 kΩ in the experiments.

In addition, L_{e1} and L_{e2} are the Kelvin emitter inductances for two IGBTs. V'_{GE} and V'_{CE} are the observed IGBT voltages. In equations 18-21, the differentials of the currents I_{C1}, I_{C2}, I_{G1}, and I_{G2} are used that are taken from the inputs to the integrators used to calculate I_{C1}, I_{C2}, I_{G1}, and I_{G2}. The differential limiting time constant τ_{lim} is set to 10^{-12} s.

$$I_{G1} = I'_{G1} + (V_{CE1} - V_{GE1})\left(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}}\right)\left(\frac{1}{1+s\tau_{lim}}\right) \tag{6}$$

$$I_{G2} = I'_{G2} + (V_{CE2} - V_{GE2})\left(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}}\right)\left(\frac{1}{1+s\tau_{lim}}\right) \tag{7}$$

$$I'_{G1} = \frac{1}{L_{G1}} \int (V_{gg1} - I'_{G1}R_{G1} - V'_{GE1})\, dt \tag{8}$$

$$I'_{G2} = \frac{1}{L_{G2}} \int (V_{gg2} - I'_{G2}R_{G2} - V'_{GE2})\, dt \tag{9}$$

$$I_{C1} = I'_{C1} - (V_{CE1} - V_{GE1})\left(\frac{sC_{FB1}R_{FB1}}{1+sC_{FB1}R_{FB1}}\right)\left(\frac{1}{1+s\tau_{lim}}\right) \tag{10}$$

$$I_{C2} = I'_{C2} - (V_{CE2} - V_{GE2})\left(\frac{sC_{FB2}R_{FB2}}{1+sC_{FB2}R_{FB2}}\right)\left(\frac{1}{1+s\tau_{lim}}\right) \tag{11}$$

$$V_{L_{s2}} = V_{RL} - V'_{CE2} \tag{12}$$

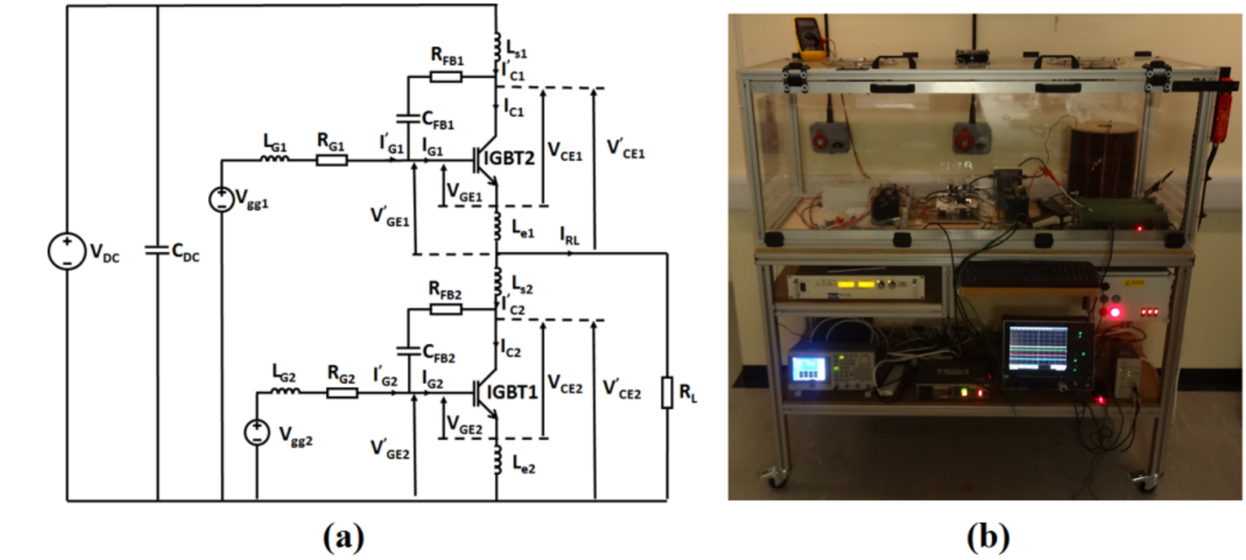
$$I'_{C2} = \frac{1}{L_{s2}} \int V_{L_{s2}} dt = \frac{1}{L_{s2}} \int (V_{RL} - V'_{CE2}) dt \quad (13)$$

$$V_{L_{s1}} = V_{DC} - V'_{CE1} - V_{RL} \quad (14)$$

$$I'_{C1} = \frac{1}{L_{s1}} \int V_{L_{s1}} dt = \frac{1}{L_{s1}} \int (V_{DC} - V'_{CE1} - V_{RL}) dt \quad (15)$$

$$I_{RL} = I_{C1} + I_{G1} - I'_{C2} \quad (16)$$

$$V_{RL} = I_{RL} . R_L \quad (17)$$



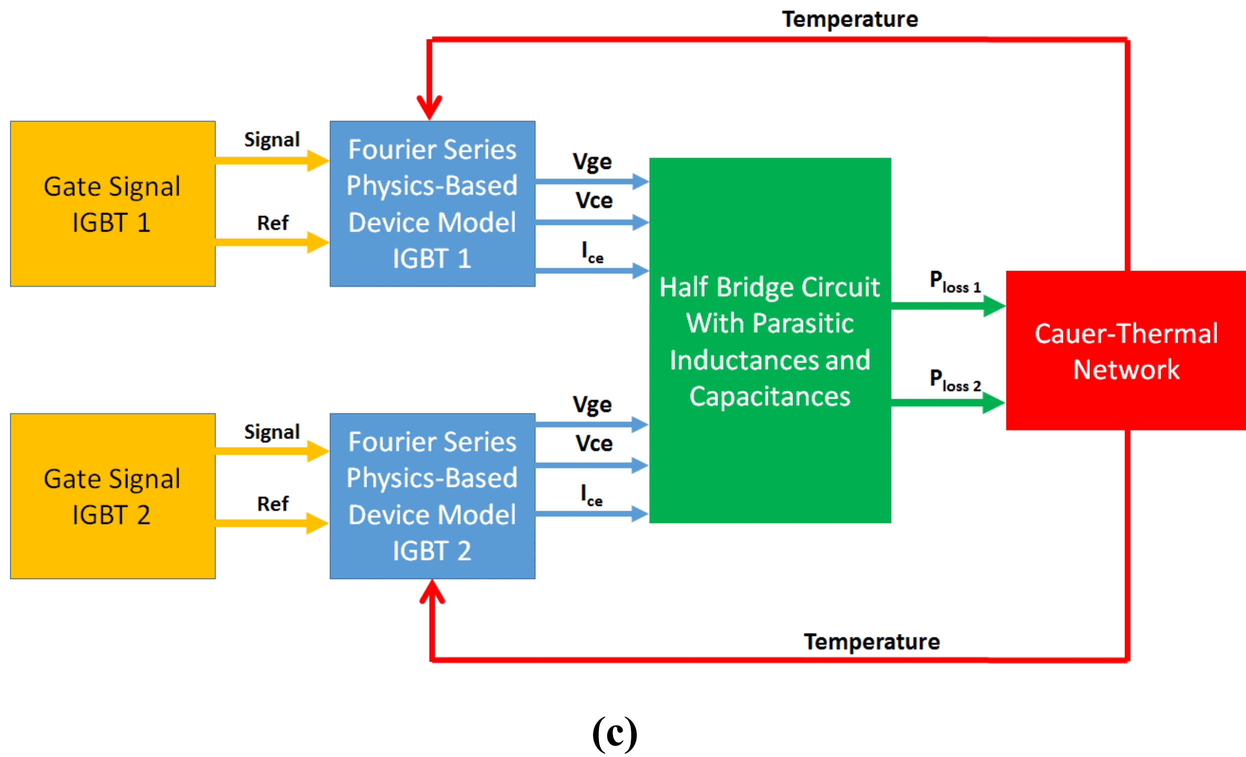


Fig. 2: Schematic of a half bridge in a voltage source inverter (a) and the experimental setup for the parasitic turn-on test (b) block diagram of the model (c).

$$V'_{CE2} = V_{CE2} + L_{e2}(I_{C2} + I_{G2})\left(\frac{1}{1+s\tau_{lim}}\right) \tag{18}$$

$$V'_{CE1} = V_{CE1} + L_{e1}(I_{C1} + I_{G1})\left(\frac{1}{1+s\tau_{lim}}\right) \tag{19}$$

$$V'_{GE2} = V_{GE2} + L_{e2}(I_{C2} + I_{G2})\left(\frac{1}{1+s\tau_{lim}}\right) \tag{20}$$

$$V'_{GE1} = V_{GE1} + L_{e1}(I_{C1} + I_{G1})\left(\frac{1}{1+s\tau_{lim}}\right) \tag{21}$$

IV. Results and Discussion

The results of the experimental measurements of the shoot-through current are shown in Fig. 3(a) whereas Fig. 3(b) shows the results of the model. With respect to Fig. 2, the high side IGBT is switched on intentionally whereas the low side IGBT is the device that is unintentionally turned on. Hence, R_{G1} is the gate resistance of the IGBT that is deliberately switched whereas R_{G2} is the gate resistance of the low side IGBT that is parasitically turned on. In Fig. 3(a), the shoot-through current is shown for 2 different gate resistances (R_{G2}) on the low side IGBT. The results show good matching between the measurements and the models. Fig. 4(a) shows the measured collector-emitter voltage across the low side IGBT that is parasitically turned-on whereas Fig. 4(b) shows the modelled V_{CE} characteristics. It can be seen in both the experimental measurements and the model that there are 2 slopes in the V_{CE} transient i.e. dV_{CE}/dt is initially high and then reduces. The characteristics are accurately captured by the model. Fig. 5(a) and Fig. 5(b) shows V_{GE} transients of the IGBT under parasitic turn-on. The Miller capacitance C_{gc} is that of the two dimensional depletion layer between the gate and N^- plasma region underneath the gate. Basically, this capacitor is the series connection of the oxide capacitance C_{ox} and the depletion layer capacitance between the gate oxide and charge storage region. This capacitance is calculated using equations (22-24) as below:

$$C_{gc} = Aa_iC'_{ox}\left(1 + \frac{W'_{dg}}{l_m}\left[\frac{1}{\frac{C'_{ox}W_{dg}}{\varepsilon}+1} - 1\right]\right) \tag{22}$$

$$W'_{dg} = \begin{cases} W_{dg} & if\ W_{dg} \le l_m \\ l_m & otherwise \end{cases} \tag{23}$$

$$W_{dg} = \sqrt{\frac{2\varepsilon(V_{d2}-V_{ge})}{qN_B}} \tag{24}$$

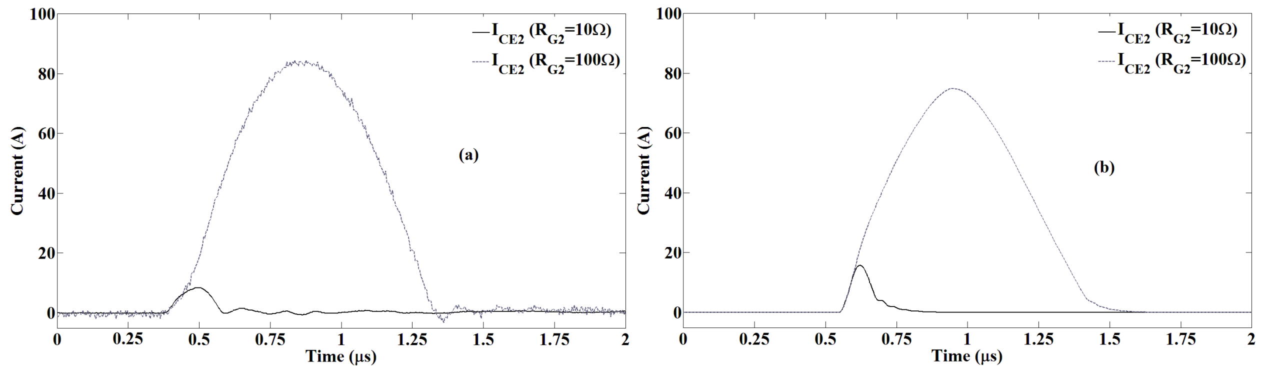


Fig. 3: Experimental results showing parasitic turn-on current waveform of the bottom switch that is constantly off for two different gate resistances of 10 and 100 Ω (a) and the simulation results under the same conditions (b).

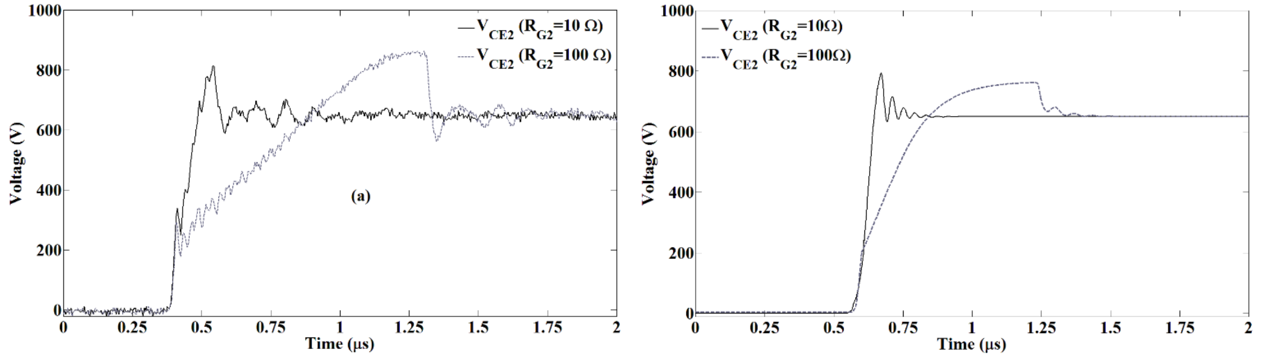


Fig. 4: Experimental results showing parasitic turn-on collector-emitter waveform of the bottom switch that is constantly off for two different gate resistances of 10 and 100 Ω (a) and the simulation results under the same conditions (b).

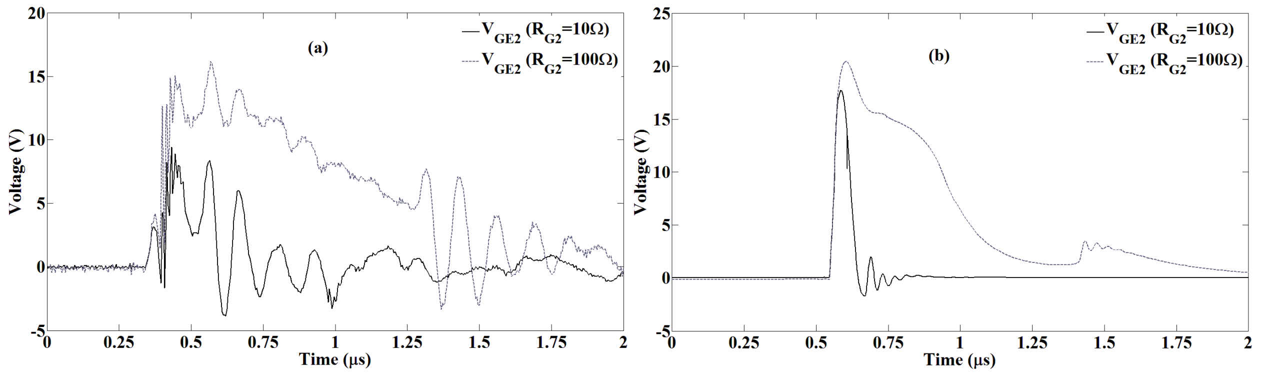


Fig. 5: Experimental results showing parasitic turn-on gate-emitter waveform of the bottom switch that is constantly off for two different gate resistances of 10 and 100 Ω (a) and the simulation results under the same conditions (b).

In this equation, C'_{ox} is the IGBT oxide capacitance per unit area (Fcm^{-2}), A is the die area (cm^2), a_i is the ratio of Intercell area to active device area, ε is the permittivity of silicon (Fcm^{-1}), N_B is the base doping of the drift region, lm is the IGBT Intercell half-width (μm). V_{dg} determines the width of the gate depletion. The sharp decrease in capacitance happens when V_{dg} exceeds zero. This capacitance decrease determines the onset of the main rise in V_{CE}. The decrease in the collector-gate current cannot completely sustain the negative gate current, so the gate-emitter capacitor starts to discharge again the consequently, V_{ge} drops slightly. This happens with a slight decrease in the MOS current and hence, the electron current into the drift region falls. This gives a steep negative current density gradient at the end of the plasma region and a faster rate of depletion layer expansion which consequently brings about a faster dV_{ce}/dt.

As can be seen, this capacitance changes overtime, is nonlinear and depends on the depletion width between the gate oxide and charge storage region. Hence, this model is able to accurately replicate the transient waveforms by avoiding the use of lumped parameters normally used in compact models thereby resulting in a more detailed transient curve. The two slopes appearing in the voltage waveform during the turn-on is as a result of this capacitor. Fig. 6 illustrates the effect of the miller capacitance on the two slopes of V_{ce} during the cross talk. Fig. 7 shows the effect of gate oxide on the slopes of the emitter-collector voltage during the cross talk. It can be seen from the measurements in Fig. 4 that the V_{CE} transient has two distinct slopes with dV_{CE}/dt being initially high and later reducing. The model is able to reproduce this transient accurately, as opposed to lumped parameter spiced-based model that use a constant Miller capacitance. The two slopes are due to the sudden reduction of the total Miller capacitance as the voltage dependent depletion capacitance starts to decrease as the depletion width expands due to the rising collector voltage. So the initially high dV_{CE}/dt, is due to a series combination of the oxide capacitance and the depletion capacitance whereas the lower dV_{CE}/dt is due to a reduction in the depletion capacitance.

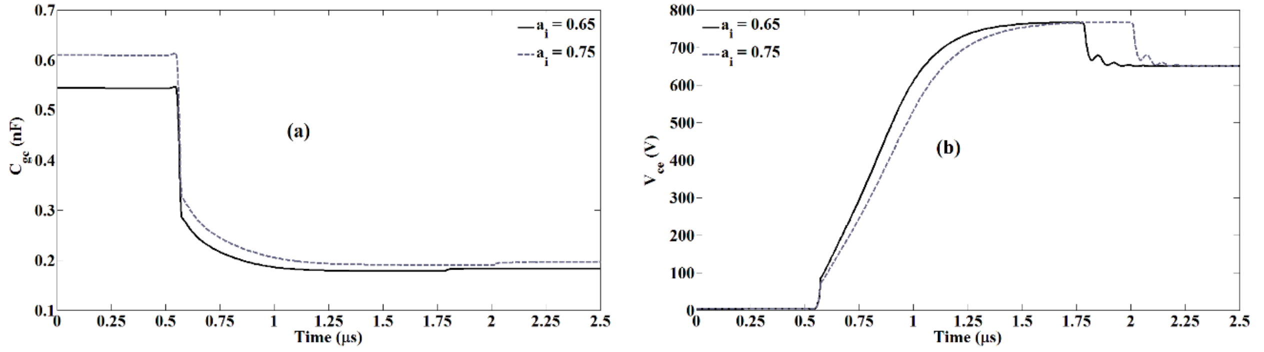


Fig. 6: Simulation result showing (a) time dependent gate-collector capacitance for two different values of ratio of Intercell area and active die area (a_i) (b) collector-emitter voltage slope change for two different values of ratio of Intercell area and active die area.

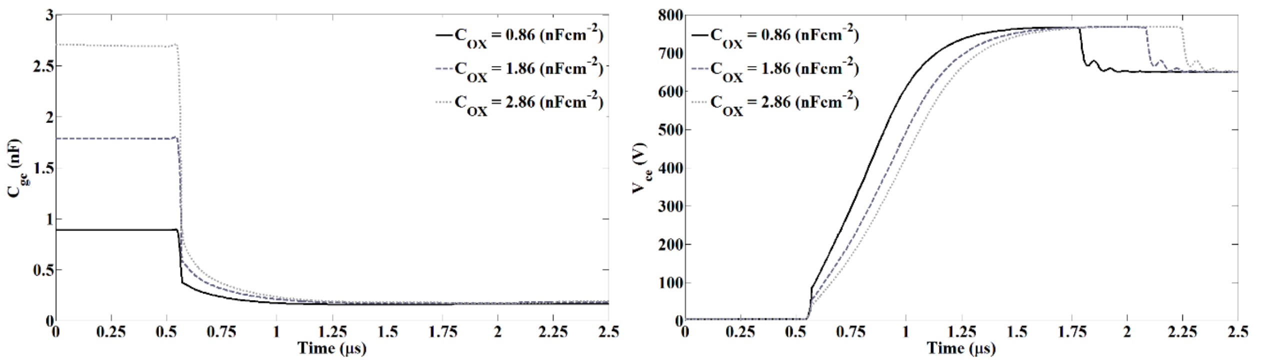


Fig. 7: Simulation result showing (a) time dependent gate-collector capacitance for three different values of C_{ox} (b) collector-emitter voltage slope change for three different values of C_{ox}.

V. Conclusion

An accurate physics based model for parasitic turn-on of an IGBT has been presented together with experimental measurements. The results show that the modelled shoot-through current, collector-emitter voltage and gate-emitter voltage transients replicate the experimental measurements with good precision. The presented model uses a physics-based approach for modelling the Miller capacitance which accurately predicts current and voltage transients as opposed to compact models that use lumped parameters that remain invariant with voltage. The circuit models where developed using KCL and KVL equations and the device models were developed using a Fourier series based solution to the ambipolar diffusion equation.

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