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Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules

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***Abstract*—The temperature and *dV/dt* dependence of crosstalk has been analyzed for Si-IGBT and SiC-MOSFET power-modules. Due to smaller Miller capacitance resulting from a smaller die-area, the SiC-module exhibits smaller shoot-through currents compared with similarly rated Si-IGBTs in spite of switching with a higher *dV/dt* and a lower threshold-voltage. However, due to high voltage overshoots and ringing from the SiC-Schottky diode, SiC modules often exhibit higher shoot-through energy density and cause voltage oscillations in the DC-link. Measurements show that the shoot-through current exhibits a positive temperature coefficient for both technologies the magnitude of which is higher for the Si-IGBT i.e. the shoot-through current and energy shows better temperature stability in the SiC-power-module. The effectiveness of common techniques of mitigating shoot-through, including bipolar gate drives, multiple gate resistance switching paths as well as external gate-source and snubber capacitors have been evaluated for both technologies at different temperatures and switching rates. The results show that solutions are less effective for SiC-MOSFETs because of lower threshold voltages and smaller margins for negative gate bias on the SiC-MOSFET gate. Models for evaluating the parasitic voltage have also been developed for diagnostic and predictive purposes. These results are important for converter designers seeking to use SiC technology.**

***Index Terms*—Crosstalk, Silicon Carbide, Temperature, IGBT, SiC MOSFET**

I. INTRODUCTION

CROSSTALK is an important factor that must be evaluated when using power semiconductor devices in converters. Crosstalk has also been referred to as parasitic turn-on, false turn-on, self-turn-on, etc. [1] Crosstalk occurs when a device is unintentionally switched on as a result of the intentional switching of the device in the same phase leg. This unwanted turn-on can impose serious reliability concerns since it can result in semi-short-circuits with high currents flowing through the power devices thereby resulting in high thermal losses and unnecessary electro-thermal stresses on the device wire-bounds and die [2]. Crosstalk normally happens in synchronous DC-DC converters or in three-phase DC-AC inverters where the devices are intended to turn on with appropriate dead-times allocated between the switching edges [3], [4]. As one device is turned on, the *dV/dt* imposed on the complimenting device in the same phase leg causes the Miller capacitance to discharge a current into the gate resistance which causes a voltage drop capable of triggering the device if it is greater than its threshold voltage [5]. The main contributors to crosstalk are the magnitude of the Miller capacitance and its ratio compared with the input capacitance of the device, the gate resistance connected to the device (which includes the internal gate resistance of the module), the switching rate, the threshold voltage of the device and its operating temperature. Equation 1 shows the parasitic gate-source (V_{GS} for MOSFET) or gate-emitter (V_{GE} for Si-IGBT) voltage as a function of the gate resistance (R_G), Miller capacitance (C_{GD}) and turn-on *dV/dt*.

$$V_{GS} = R_G C_{GD} \frac{\mathrm{d}V_{DS}}{\mathrm{d}t} \left(1 - e^{\frac{-t}{R_G(C_{GD} + C_{GS})}} \right) \quad (1)$$

Figure 1 shows an example of a parasitic (unintended) gate voltage across a SiC MOSFET during turn-on and turn-off of a complementing device.

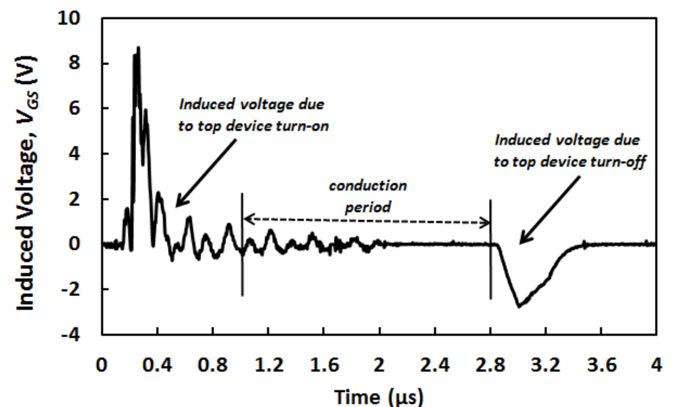

Fig. 1. Measured parasitic gate voltage across a Si-IGBT switched with a *dV/dt* of up to 10 *kV/µs*.

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The positive spike in V_{GS} during turn-on and the negative spike during turn-off is due to the polarity of the Miller capacitance charge and discharge current. The mechanism is explained in [6]. To mitigate this problem, techniques like negative gate bias and multiple resistive paths for turn-on/turn-off have been developed. This paper aims to evaluate the problem of crosstalk as well as the effectiveness of the solutions for SiC MOSFETs compared with silicon IGBTs [7]. The desire to maximize power density by increasing the switching frequency gives SiC an advantage, however, crosstalk is expected to cause problems since the shoot-through energy is proportional to the switching rate [8]. SiC MOSFETs have lower threshold voltages and switch with higher *dV/dt* both of which should contribute to higher shoot-through currents. However, the Miller capacitance in SiC MOSFETs is significantly smaller than that in silicon IGBTs because of its smaller die area [9]. The temperature coefficients of the threshold voltages in both technologies will also be critical for the crosstalk performance at higher temperatures. Furthermore, the impact of oscillations in the SiC Schottky diode [10] on the DC link voltage and the shoot-through energy also needs further characterization. This paper presents a comprehensive analysis of crosstalk in both technologies. Section II presents a modeling approach for predicting crosstalk, Section III will provide details of the experimental measurements performed and analyze the switching rate (*dV/dt*) and temperature dependence of crosstalk. Section IV study the effectiveness of applicable mitigation techniques while Section V concludes the paper.

II. Crosstalk Models

To develop a diagnostic tool for the prediction of the crosstalk, several modeling approaches are considered, all of which are based on the capacitive divider in the device.

- The first modeling approach is described in [11] by using the maximum possible voltage at turn-ON as V_m of the device, along with time instance it occurs as T_m in Equation 1. This approach is the simplest method of modeling and does not consider the parasitic elements in the circuit. Also it does not consider the changes in the *dV/dt* of the circuit. Hence despite being straightforward, it lacks accuracy. An example of this method is shown in Figure 2. This method results in the following expression:

$$V_{GS} = R_G C_{GD} \frac{V_m}{T_m} \left(1 - e^{\dfrac{-t}{R_G (C_{GD} + C_{GS})}} \right) \quad (2)$$

- The second approach is to use the *dV/dt* measured from the transient of the device to estimate the induced gate voltage. This method is more accurate as it considers the dynamic changes of the *dV/dt* in the circuit and also indirectly considers the impact of parasitic elements in the circuit. However, using this method requires having the voltage transient measurements of the circuit requires some initial characterisations. An example of this method is shown in Figure 3.

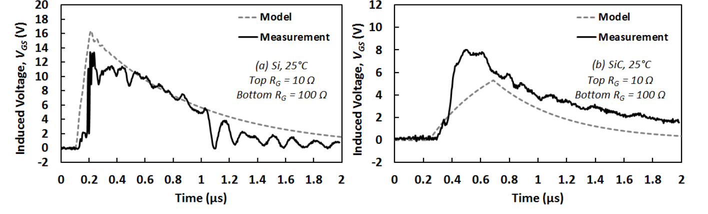

Fig. 2. Modeled and measured induced V_{GS} using method one for (a) Si-IGBT and (b) SiC-MOSFET with top R_G = 10 Ω and bottom R_G = 100 Ω.

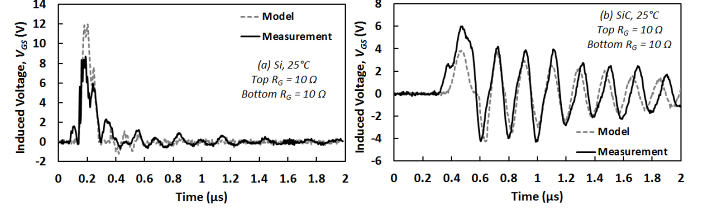

Fig. 3. Modeled and measured induced V_{GS} using method one for (a) Si-IGBT and (b) SiC-MOSFET with both top and bottom R_G = 10 Ω.

- The third method, which is common, uses simulation software such as PLECS or SPICE to model the characteristics of the device in a circuit emulator. This method is capable of providing the characteristics of the induced gate voltage as a function of the parasitic circuit components (inductances and capacitances) and is user friendly. However, the temperature dependency of the shoot-through current is not modelled accurately because the temperature coefficient of the threshold voltage and on-state resistance is not properly accounted for. An example of this method is shown in Figure 4.

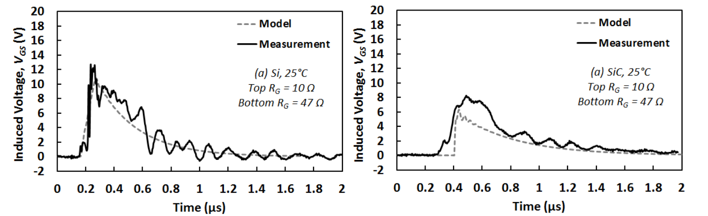

Fig. 4. Modeled and measured induced V_{GS} using method one for (a) Si-IGBT and (b) SiC-MOSFET with top R_G = 10 Ω and bottom R_G = 47 Ω.

- The last method is the method proposed here. The parasitic voltage is modeled by developing a transfer function of the equivalent circuit shown in Figure 5. In this figure, the power device that is intentionally switched is modeled as an ideal switch however with a finite *dV/dt* that falls on the low side power device causing it to be parasitically triggered. In this case, first the equations for the V_{GS} are developed. This is done by using the Kirchhoff law in the circuit. Then, having the numerator and denominators of the transfer function, and by using the *dV/dt* of the intentionally switched device as an input to the transfer function, the induced voltage can be calculated. Details of this method is described next.

The circuit shown in Figure 5 includes the parasitic capacitances of the device, the stray inductances as well

as the parasitic resistances and inductances resulting from the circuit layout. These parasitic elements are critical for accounting the possible oscillations in the parasitic voltage transient characteristics [12]. Hence, the model developed can be used to predict the possibility of crosstalk, if a voltage above the threshold voltage of the device is induced on the gate. The model can be used to predict the severity of the shoot-through current (to a certain extent) by comparing the level of the V_{GG} with V_{TH}. The average values for the parasitic elements are used for the development of the model [13], and are applicable when devices are switched with no mitigation technique applied. These are shown in Table II.

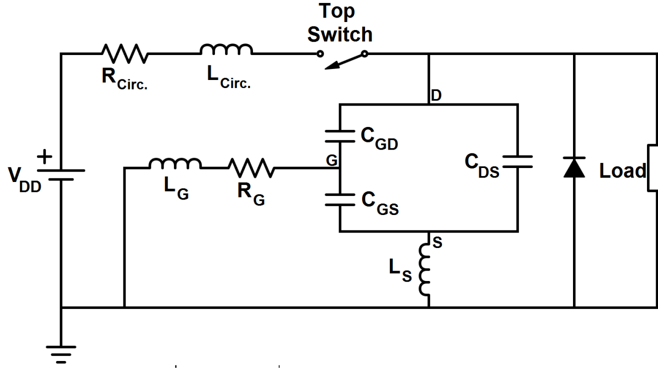

Fig. 5. Equivalent circuit schematic for developing parasitic voltage model for the bottom power device with the top device as an ideal switch.

TABLE I
MODEL PARAMETERS AND VALUES

C_{GD} (Si-IGBT)	≈ 0.15 nF
C_{GS} (Si-IGBT)	≈ 7.2 nF
C_{GD} (SiC-MOSFET)	≈ 0.08 nF
C_{GS} (SiC-MOSFET)	≈ 10 nF
L_S	≈ 5 nH
L_G	≈ 5 nH
$L_{Circ.}$	≈ 100 nH
$R_{Circ.}$	≈ 1 Ω
V_{DD}	650 Volts

Applying KCL at the gate, source and drain terminals of the circuit in Figure 5 will yield 3 equations as shown in 3- 5.

$$\frac{V_G}{R_G + sL_G} + (V_G - V_S)sC_{GS} + (V_G - V_D)sC_{GD} = 0 \quad (3)$$

$$(V_S - V_G)sC_{GS} + \frac{V_S}{sL_S} + (V_S - V_D)sC_{DS} = 0 \quad (4)$$

$$(V_D - V_G)sC_{GD} + (V_D - V_S)sC_{DS} + \frac{V_D - V_{DD}}{R_{Cr} + sL_{Cr}} = 0 \quad (5)$$

Solving the equations above for the gate-source voltage will yield the transfer function shown in 6 as:

$$V_G = \frac{N_4 s^4 + N_3 s^3 + N_2 s^2 + N_1 s}{D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + 1} \quad (6)$$

where the numerators are given by:

$$N_4 = L_G L_S V_{DD} \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$
$$N_3 = L_S R_G V_{DD} \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$
$$N_2 = C_{GD} L_G V_{DD}$$
$$N_1 = C_{GD} R_G V_{DD}$$

And the denominators are given by:

$$D_4 = (L_{Cr}L_G + L_{Cr}L_S + L_S L_G) \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$
$$D_3 = (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS}) \times (L_{Cr}R_G + L_G R_{Cr} + L_S R_{Cr} + L_S R_G)$$
$$D_2 = L_{CR}(C_{DS} + C_{GD}) + L_G(C_{GS} + C_{GD}) + L_S \times (C_{DS} + C_{GS}) + R_{Cr}R_G \times (C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})$$
$$D_1 = R_{Cr} \times (C_{DS} + C_{GD}) + R_G \times (C_{GS} + C_{GD})$$

The *dV/dt* of the intentionally switched device is used as an input to the model. The values of the capacitances used in the model are obtained from the datasheets as shown in section III and the inductances are measured directly from the test rig. The results of the model are shown together with experimental measurements in Figure 6(a) and 6(b) for a silicon IGBT and SiC MOSFET half-bridge power module respectively switched with a gate resistance of 10 Ω and a *dV/dt* of up to 10 *kV/μs*. Figure 6(c) and 6(d) show the results of the model with experimental measurements with a higher bottom side gate resistance of 47 Ω but with the same switching *dV/dt*. The ringing in the gate characteristics of the SiC module is modulated by the parasitic inductances and the switching rates. It can be seen from Figure 6 that the model is able to replicate experimental measurements with good accuracy.

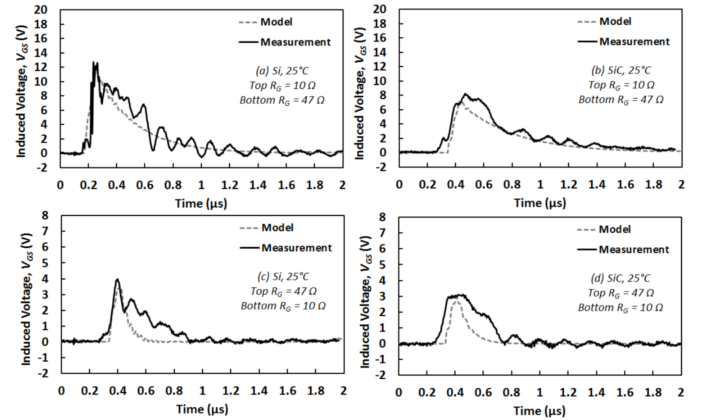

Fig. 6. Modeled and measured parasitic gate voltage transients for Si-IGBT and SiC-MOSFET with (a,b) top bottom R_G = 10 Ω and bottom R_G = 47 Ω and in (c,d) top R_G = 47 Ω and bottom R_G = 10 Ω.

III. EXPERIMENTAL MEASUREMENTS

To evaluate the temperature and switching rate dependence of crosstalk in silicon IGBT and SiC MOSFET power modules, a dedicated test rig has been developed and equipped with a hot plate as well as temperature

control and measurement equipment. Since crosstalk entails short-circuiting a high voltage power supply, extra protection has been applied to the test rig. In this section, first the details of the set-up is presented, then the analysis of the switching rate dependence of the crosstalk is discussed. This is done by changing the range of R_G on both top and bottom device to vary the applied *dV/dt* and the induced voltage. The rate at which the output voltage rises/falls (dV_{DS}/dt for MOSFETs and dV_{CE}/dt for IGBTs) depends on the rate at which the Miller capacitance is charged/discharged through the gate resistance. Hence, *dV/dt* is inversely related to $R_G C_{GD}$ [14] through the Miller capacitance's dependence on the output voltage i.e. the Miller capacitance is partially comprised of a depletion capacitance whose value depends on depletion widths modulated by the output voltage. Therefore the value of R_G directly impacts the *dV/dt* and *dI/dt* rates [15]. The temperature dependence of crosstalk is also analyzed by mounting the modules of a thermal plate and ranging the temperature from room temperature to 120 °C. It should be noted that the SiC module has used 5 dies per device in parallel, each die with an area of 16.6 mm^2, resulting in a total die are of approximately 83 mm^2 (0.83 cm^2), whereas the Silicon module is a single die per device with a die area of approximately 105 mm^2 (1.05 cm^2). Given that the modules are of the same power rating, this shows that the SiC module has a higher power density. In the next sections, this information has been used to estimate the shoot-through energy per die area of the devices for a comparable evaluation.

A. Set Up

The schematic of the test rig is shown in Figure 7. The applied voltage is 650 Volts and the load is a 1 kΩ resistor with a 1 kW power rating connected in parallel to the bottom device. The top device is switched while the bottom device is monitored for induced switching. The DC link capacitors have a total capacitance of 320 μF with a voltage rating of 1.2 kV. The silicon IGBT half bridge module is DM2G100SH12AE with a Miller capacitance (C_{GD}) of 0.15 nF and the SiC half bridge module is CAS100H12AM1 with a Miller capacitance of 0.08 nF. The threshold voltage of the silicon IGBTs range from 5 to 8 V, whereas in the SiC MOSFET it ranges around 2 V. The gate signal is generated by Agilent AFG3022C controller while the waveforms are captured by LeCroy 104MXs-B digital oscilloscope. The current and voltages waveforms are also captured via calibrated current clamped (Tektronix TCP303 15 MHz) and differential high voltage probes (Rapid GDP-100 100 MHz) as shown in Figure 8. The temperatures are ranged from room temperature to 120 °C while the switching rate is controlled by a range of R_G from 10 to 100 Ω. This range of R_G is intentionally chosen wide because, as will be analysed in the next sections, the shoot-through current increase with the applied *dV/dt* on the bottom device, the Miller capacitance of the bottom device and the gate resistance on the bottom device. The peak parasitic gate voltage is given by $R_G.C_{GD}.dV_{DS}/dt$, hence, an increase in any one of the parameters will affect the shoot-through current in a similar way. While further increase of the *dV/dt* or changing the device's Miller capacitance has not been an option, to investigate the performance of the device and also the effectiveness of the mitigation techniques in higher shoot-through currents, the bottom-side R_G has been increased from 10 to 100 Ω to replicate these situations [16]. The design of the gate driver PCB's is also shown in Figure 9.

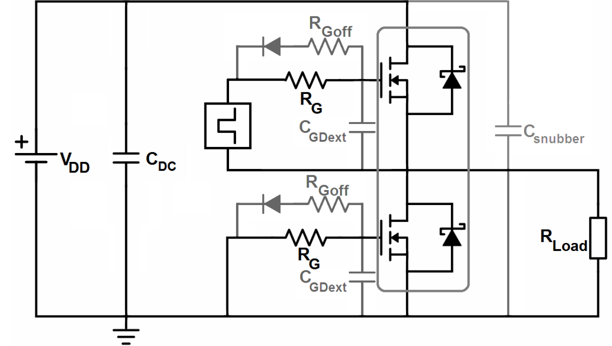

Fig. 7. Schematic of the measurement circuit.

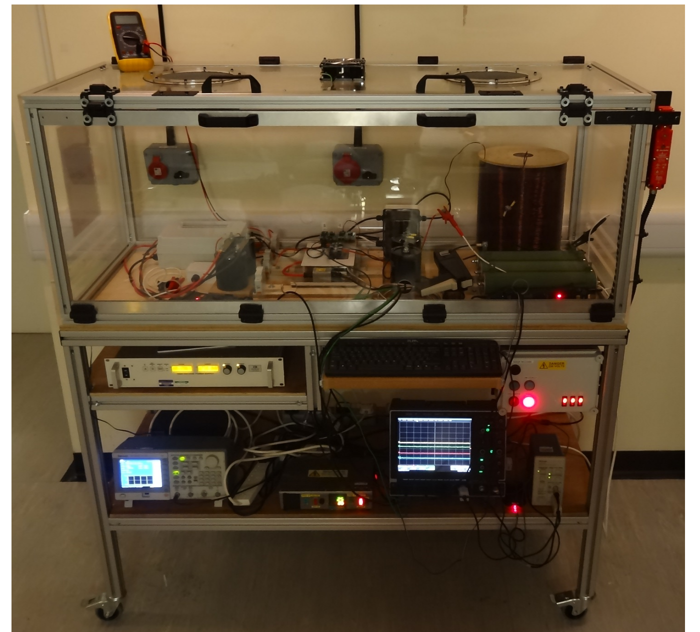

Fig. 8. Measurement Test rig set-up.

B. Switching Rate Dependence

Figure 10 shows the results of the measurements for the switching rate dependence of the crosstalk where the *dV/dt* is modulated by a single gate resistance on the top side device which is intentionally switched and the parasitic voltage is measured on the bottom device by the connection of a range of gate resistances. Figure 10(a) shows the induced gate voltage on the bottom device in the silicon IGBT module while the top device is switching with a high *dV/dt* modulated by a gate resistance of 10 Ω. Figure 10(b) shows the corresponding shoot-through current. It can be seen from these two figures that increasing the bottom side R_G at a constant dV_{DS}/dt

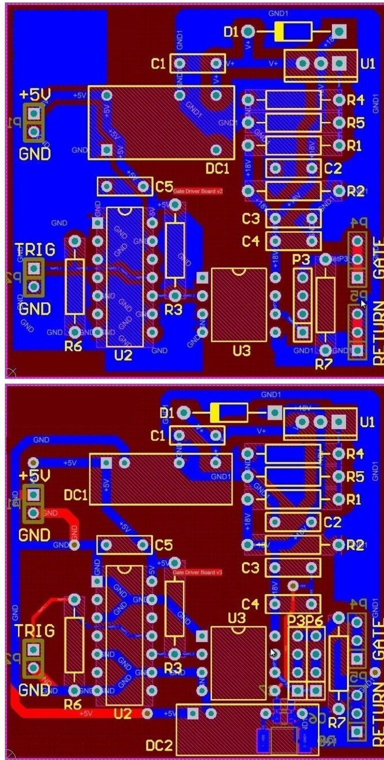

Fig. 9. The PCB design schematic of the gate drivers; top: Unipolar Driver, bottom: Bipolar Driver with extra gate resistance slots for two resistive paths.

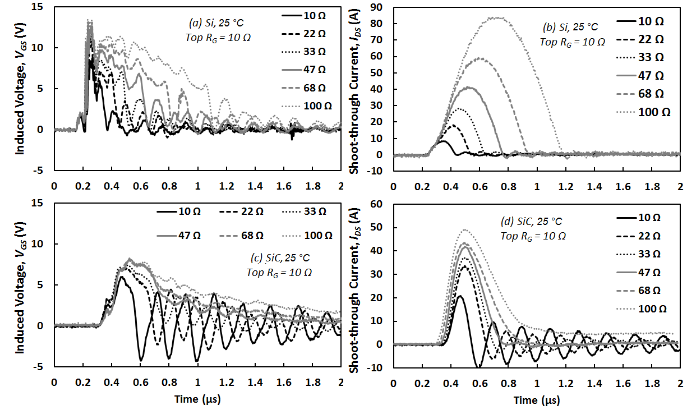

Fig. 10. (a). The induced parasitic turn-on voltage on the gate of the Si-IGBT power module at different gate resistances with a constant turn-on *dV/dt*. (b). The corresponding shoot-through current through the Si-IGBTs at different gate resistances. (c,d) The same figures for SiC device.

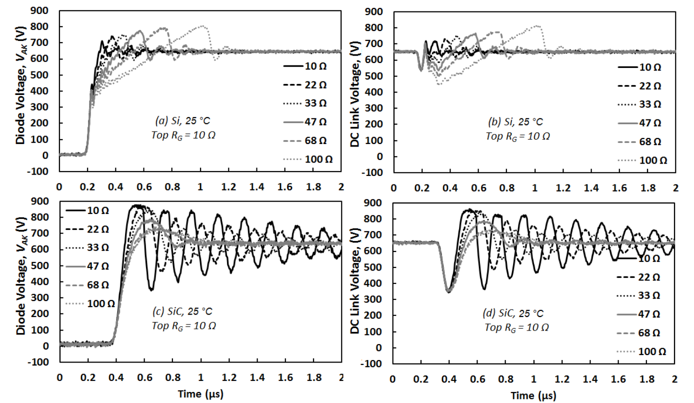

Fig. 11. Bottom diode and DC link voltage with measurements at 650 volts and 25 °C, (a,b) Si-IGBT (c,d) SiC-MOSFET.

causes a corresponding increase in the induced voltage turn-on duration although the peak is relatively the same at about 13 V which is well above the threshold voltage of 5 V. Figure 10(c) shows the induced parasitic voltage on the bottom side SiC MOSFET while Figure 10(d) shows the corresponding shoot-through current. For the SiC MOSFET power module, oscillations occur in the gate characteristic due to the ringing in the bottom side V_{DS} characteristics which feedback to the gate drive through the Miller capacitance. The ringing, which is due to RLC resonance, has an oscillation frequency that is proportional to the switching *dV/dt*. It can be seen from Figure 10 that the peak shoot-through current is approximately 70% higher for the Si-IGBT power module compared to the SiC power module. This is due to the 10 times higher Miller capacitance in the Si-IGBT which according to 1 will cause a higher parasitic gate voltage.

The impact of shoot-through on the DC link voltage and the diode voltage is shown in Figure 11. Figure 11(a) shows the voltage measured across the bottom side Si-IGBT/PiN diode for the different gate resistances while Figure 11(b) shows the measured DC-link voltage during the short circuit. Figure 11(c) shows the measured voltage across the bottom side SiC-MOSFET/Schottky diode while Figure 11(d) shows the corresponding DC link voltage. It is seen that the SiC device exhibits ringing which is connected to the ringing in the gate characteristics and shoot-through currents in Figure 10(c) and 10(d). The significance of ringing is exacerbated by higher *dV/dt* as was expected.

Figure 12(a) shows the shoot-through energy density for the Si-IGBT power module for a matrix of gate resistances ranging from 10 Ω to 100 Ω while Figure 12(b) shows the same for the SiC-MOSFET. The best combination to achieve the smallest shoot-through energy density is to switch the devices on more slowly than switching the devices off. The shoot-through energy density is higher for the SiC power module because of the diode turn-off voltage overshoot.

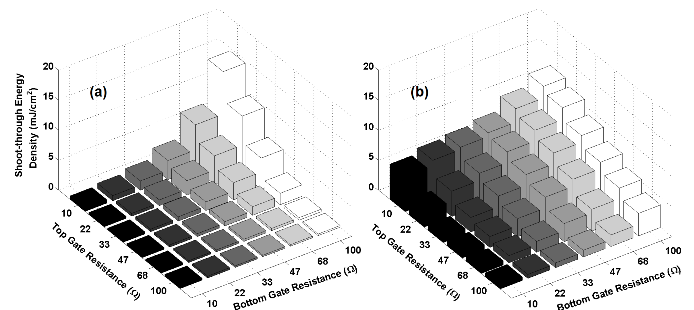

Fig. 12. (a). The shoot-through energy density for different combinations of gate resistances in the Si-IGBT power module (b). The shoot through energy density for the SiC power module.

C. Temperature Dependence

The temperature dependence of the shoot-through current and energy has also been investigated experimentally for both technologies. Figure 13(a,c) shows the parasitic induced voltage on the gate of the Si-IGBT at different temperatures and Figure 13(b,d) shows the corresponding shoot-through current at different temperatures. As can be seen in Figure 13(a), the parasitic voltage characteristics are temperature invariant whereas in Figure 13(b), the peak shoot-through current can be seen to increase by 60% (80 A to 130 A) as the temperature is increased from room temperature to 120 °C. Figure 13(c) shows the induced parasitic voltage in the SiC power module whereas Figure 13(d) shows the corresponding shoot-through currents. The shoot-through currents in the SiC power module are smaller and show more temperature stability compared to the Si-IGBT module. For the same temperature range, the peak shoot-through current in the SiC power module increases from 40 A to 60 A. Figure 14 shows the bottom side diode voltage and its consequent DC link voltage for both silicon and SiC power modules where both devices are connected to low R_G, resulting in high switching rates. It is seen that they are nearly temperature invariant at high switching rates. The reason is explained in [**?**], [17], [18].

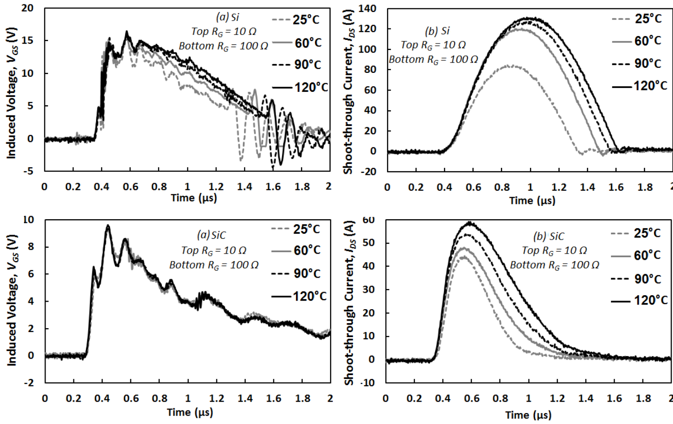

Fig. 13. (a). The induced parasitic turn-on voltage on the gate of the Si-IGBT power module at different temperatures with constant turn-on/off *dV/dt*. (top R_G = 10 Ω, bottom R_G = 100 Ω) (b). The corresponding shoot-through current through the Si-IGBTs at different temperatures. (c,d) The same figures for SiC device.

The shoot-through switching energy density is shown in Figure 15 as a function of temperature for the 2 technologies with different bottom side gate resistances. The SiC module shows better temperature stability because the negative temperature coefficient of the threshold voltage is lower in SiC compared to silicon. Due to the wider bandgap in SiC, the rate of threshold voltage decrease with temperature is lower because the thermal energy needed to increase the intrinsic carrier concentration by generating carriers is higher.

Crosstalk can be investigated by different approaches. The direct approach is to evaluate it through shoot-through current in the device. This shoot-through current can cause, for example, the circuit protection to activate. However the amplitude of the current is not a sufficient method for

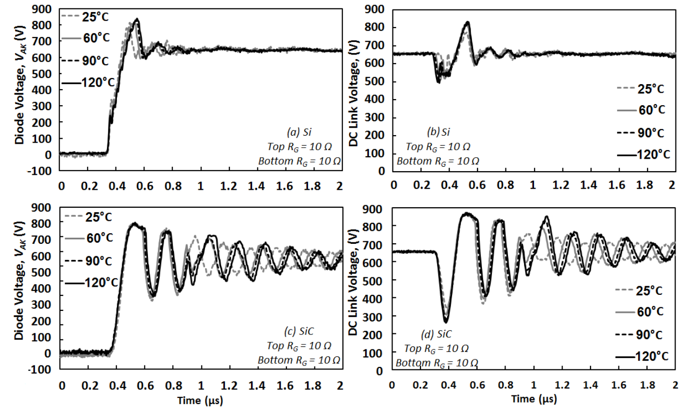

Fig. 14. The impact of temperature on the diode and DC link voltage at high switching rates (both top/bottom devices are connected to R_G = 10 Ω) (a,b) silicon devices (c,d) SiC devices showing invariance with temperature at high switching rates.

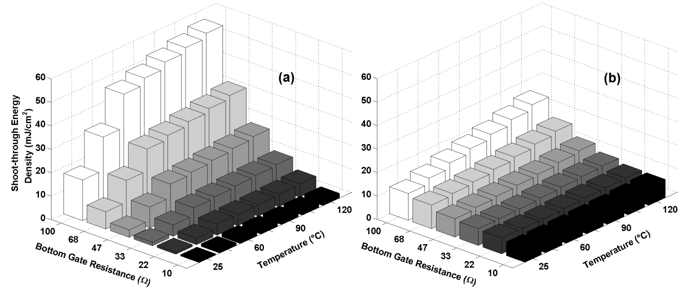

Fig. 15. The shoot-through energy density at different temperatures and bottom side gate resistances in (a) the Si-IGBT power module (b). the SiC-MOSFET power module.

understating the consequences of crosstalk, since the duration of the shoot-through current is also a critical parameter. Hence, the shoot-through charge which incorporates both the peak amplitude and the transient duration should be used to understand the severity of the consequences. Also the shoot-through energy density, as a result of the dissipated power during crosstalk resulting from simultaneous voltage/current per die should be analyzed, since reliability issues and device failures are often caused by the excessive heat generated within the device junction. Therefore the shoot-through current measured at each temperature for each technology has been integrated over time to get the shoot-through charge. The shoot-through charge increases approximately linearly with temperature as a result of the corresponding decrease in the threshold voltage. That rate of change of shoot-through charge with temperature has been calculated so as to evaluate the temperature dependence for both technologies. Figure 16 shows a comparison of the shoot-through charge (integrated shoot-through current over time) temperature coefficient for both technologies where it can be seen that the SiC MOSFET module is more temperature invariant. Figure 17 shows the corresponding shoot-through energies. It can clearly be seen that the SiC module exhibits better temperature stability compared to the Si-IGBT module. A typical example of result of this shoot-through energy is shown in Figure 18.

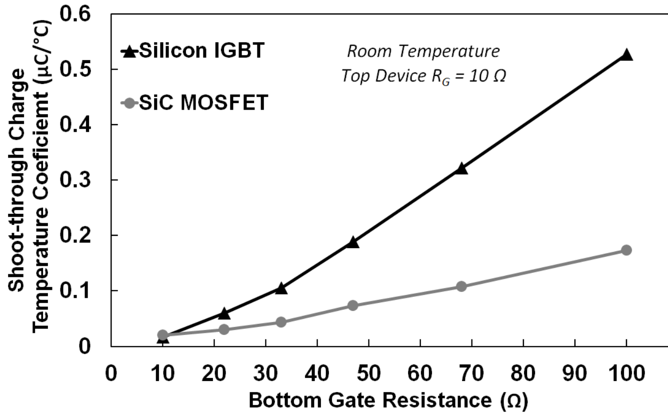

Fig. 16. Shoot-through charge temperature coefficient (μC/°C) as a function of the bottom-side gate resistances, showing that the silicon IGBT device is more temperature variant compared with its SiC counterpart.

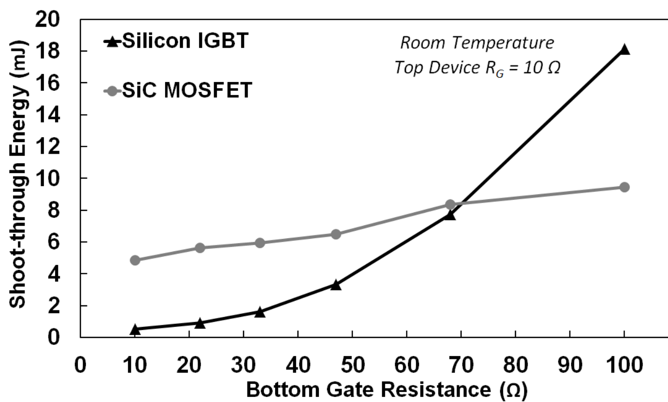

Fig. 17. Shoot-through energy of Silicon device compared with its SiC counterpart, showing that the shoot-through energy of the silicon device is more dependent on change of switching rate compared with SiC device.

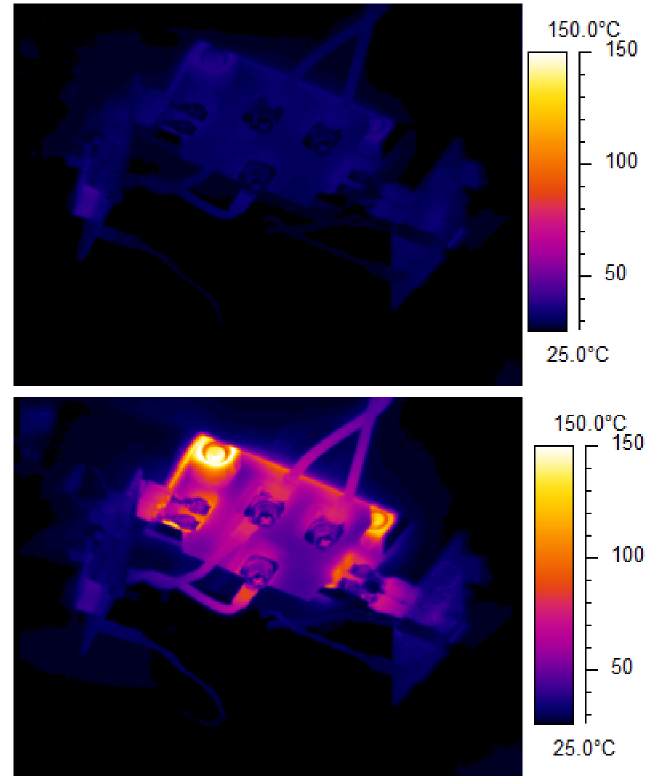

Fig. 18. Thermal camera image of the SiC MOSFET module switching at 8 kHz with low R_G of (top) 10 Ω and (bottom) 100 Ω with high side device switched with 10 Ω, showing a typical example of temperature rise as a result of continues occurrence of crosstalk in less than 8 minutes.

IV. Evaluation of Crosstalk Mitigation Techniques on Si-IGBT and SiC-MOSFET Modules

To mitigate the induced parasitic voltage and its subsequent consequences, including the shoot-through current and the DC link voltage ripple, several correction techniques can be employed [19]–[21]. However not all these techniques are applicable for all cases. The correction techniques to be analyzed for effectiveness include (i) the use of a bipolar gate driver instead of a unipolar driver (negative voltage offset) (ii) using two different gate resistors for turn-on and turn-off (iii) using an external gate-source capacitor and (iv) using a DC link snubber capacitor. Other correction techniques include the use of the Miller clamp which is not suitable for SiC power modules [21]. Several publications proposed advanced gate drive techniques to mitigate the crosstalk. However the aim of this paper is to compare the basic techniques applied to the basic gate drivers.

A. Negative offset Gate Bias from Bipolar Gate Drives

The basic idea behind the negative gate bias is to increase the margin required for current flow from the threshold voltage V_{TH} to the sum of the negative gate bias and the threshold voltage (V_{GB}+V_{TH}). However, this requires gate driver circuits capable of providing negative bias (bipolar gate drivers) which are more complicated and expensive compared to unipolar gate drivers. Furthermore, subjecting SiC power MOSFETs to negative stress across the gate oxide is a reliability concern since threshold voltage shift can cause the devices to become normally on. In this paper, the effectiveness of this correction technique is evaluated for both technologies. The negative bias voltage applied to both devices is equally set as -5 Volts and the same unipolar and bipolar drives are used in both cases to provide a fair comparison. This voltage is chosen as it is the maximum negative gate voltage that SiC device can withstand during continues operation based on the device datasheet. Figure 19(a) shows the induced parasitic voltage on the bottom side Si-IGBT for both unipolar and bipolar gate drives whereas Figure 19(b) shows the shoot-through current. Similar plots are shown for the SiC module in Figure 19(c) and Figure 19(d). It can be seen that the induced voltage is suppressed and the peak shoot-through current is significantly reduced (from 80 A to 5 A) for the Si-IGBT module whereas for the SiC module, the peak shoot-through current is reduced from 45 A to 20 A. Hence, while the bipolar gate drive solves the problem for the Si-IGBT module, it does not completely solve it for the SiC module. This is thought to be due to the higher *dV/dt* coupled with lower threshold voltage of the SiC module.

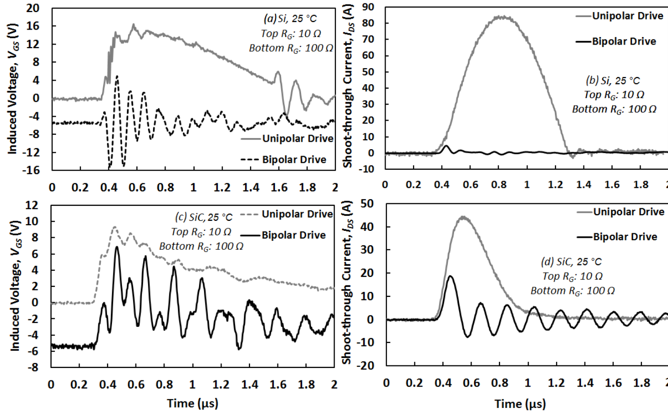

Fig. 19. Measurements in 25 °C with a R_G = 10 Ω (top), R_G = 100 Ω (bottom) (a). Impact of the bipolar driver on the biasing the induced voltage on Si-IGBT (b). Impact of the biased induced voltage on the shoot-through current on Si-IGBT (c). The same figures for SiC device.

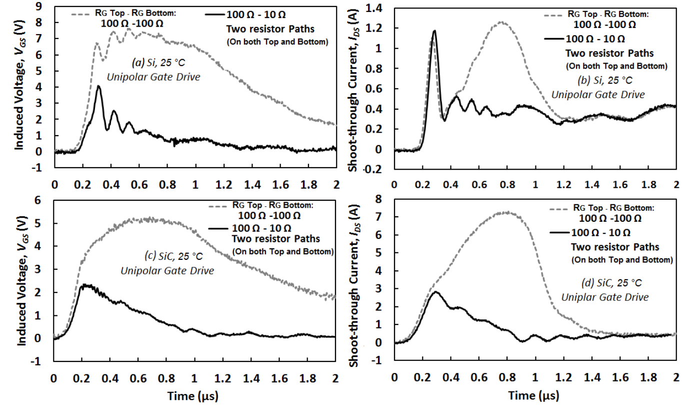

Fig. 21. Measurements in 25 °C with a unipolar driver (a). Impact of the two resistive paths technique on the induced voltage on Si-IGBT (b). Impact of the two resistive paths technique on the shoot-through current of Si-IGBT (c,d) The same figures for the SiC device.

B. Use of two resistive paths for turn-on and turn-off

The basic concept behind this technique is using two different resistive paths for the turn-on (R_{GON}) and turn-off (R_{GOFF}) as shown in Figure 7. The result of applying this is shown in Figure 20. As can be seen, the turn-on and turn-off rates are controlled by the different resistances. A lower parasitic voltage is induced by using a diode to ensure that the capacitive Miller current flows through the lower R_{GOFF}. Looking at Figure 21(a) and (b) for Si-IGBT and Figure 21(c) and (d) for SiC module, it is seen that this technique has significantly lowered the shoot-through current.

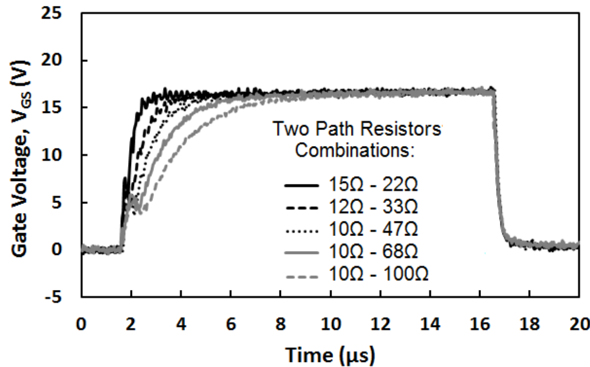

Fig. 20. The gate signal for two resistive paths technique. As seen the turn-on is done by different rates, while the turn-OFF is consistently fast.

C. External C_{GS}

An external gate-source capacitance can be used to reduce the induced voltage as it will consume part of the current through the Miller capacitance, resulting in lower currents flowing through the gate resistance, causing lower induced voltage. This method also causes a lower *dV/dt* on top device turn-on as the external capacitance also consumes part of the gate current and therefore slows down the device. As a result, it is not preferable in SiC-MOSFETs where the switching rate is aimed to high values. Looking at Figure 22(a) and (b) for the Si-IGBT and (c) and (d) for the SiC-MOSFET, it is seen that connecting a 10 nF external source-gate capacitance has reduced the induced voltage and shoot-through current by a small degree and the impact is relatively low compared with other correction techniques examined. Increasing the external C_{GS} causes lower *dV/dt* and higher switching energies and therefore is not recommended.

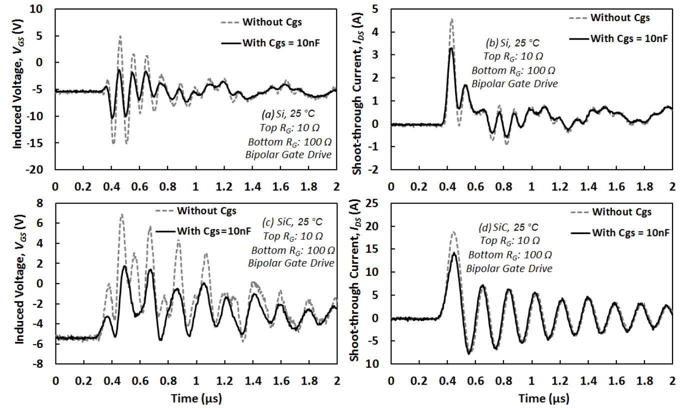

Fig. 22. Measurements in 25 °C with a bipolar driver (a). Impact of external C_{GS} on the induced voltage on Si-IGBT (b). Impact of external C_{GS} on the shoot-through current on Si-IGBT (c,d) The same figures for the SiC device.

D. Snubber Capacitor

The shoot-through current causes a significant voltage dip on the DC link which destabilizes the voltage on the DC link capacitors. Stabilizing the DC link voltage using a snubber capacitor on the half bridge module can reduce the high frequency ringing in the shoot-through current, resulting in less oscillation in the induced voltage. This in turn will reduce the shoot-through switching energy as well. As seen in Figure 23, the snubber capacitor (here with a value of 100 nF) has stabilized the DC link and consequently, the overshoot in the voltage of the silicon modules diode. The snubber capacitor is particularly effective for the SiC power module since as seen in Figure 14(c) and (d), the oscillation

on the DC link voltage of the SiC power module is significant. Figure 23(c) and (d) shows that the snubber capacitor filters out the oscillations and stabilizes the DC link as well as the bottom side SiC MOSFET/Schottky diode voltage. This also stabilizes the induced parasitic voltage as well as the shoot-through current as seen in Figure 24.

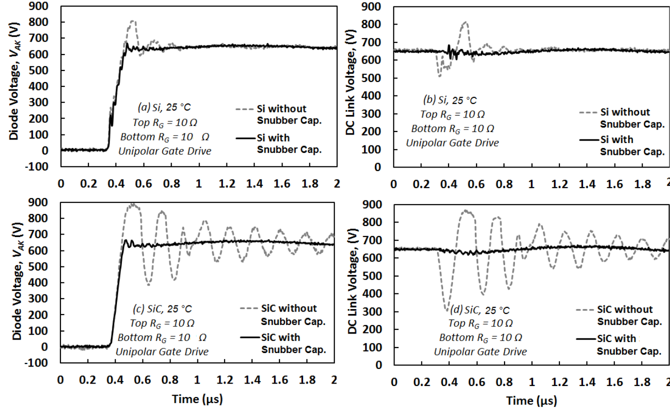

Fig. 23. The impact of the snubber capacitor on the voltage dip and oscillations on the bottom diode voltage and DC link in silicon and SiC.

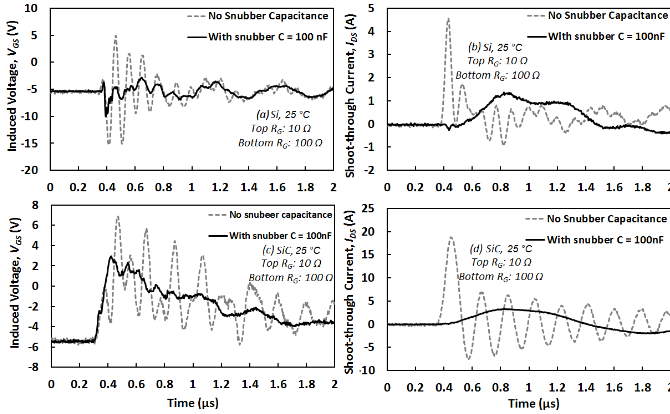

Fig. 24. Measurements in 25 °C with a bipolar driver (a). Impact of the snubber capacitor on the induced voltage fluctuations on Si-IGBT (b). Impact of the snubber capacitor on shoot-through current of Si-IGBT (c,d) The same figures for the SiC device.

To provide a comprehensive and comparative analysis on the effectiveness of the correction techniques, Figure 25 to 28 have been produced. Figure 25 shows the effectiveness of using a (a) unipolar gate driver compared with the (b) bipolar driver for two bottom side gate resistances (10 Ω and 100 Ω) while the top switch is switched at a high rate with R_G of 10 Ω. It is seen here that although the Si-IGBT module has a higher shoot-through charge compared with the SiC MOSFET module at bottom side R_G = 100 Ω and it is lower at bottom side R_G = 10 Ω. It can also be seen that the shoot-through charge of the SiC MOSFET module is less dependent on R_G as is expected due to its lower Miller capacitance. By applying a bipolar gate driver as seen in Figure 25(b), the shoot-through charge is reduced in both devices; however, the effectiveness of the Bipolar gate drive is less in the SiC MOSFET module as a result of its lower threshold voltage and higher *dV/dt*. As can be seen from Figure 25(b), the shoot-through charge for both R_G cases is minimal in the Si-IGBT module with Bipolar gate drive compared with the SiC MOSFET module. This is shown in terms of charge reduction percentage for R_G = 10 Ω.

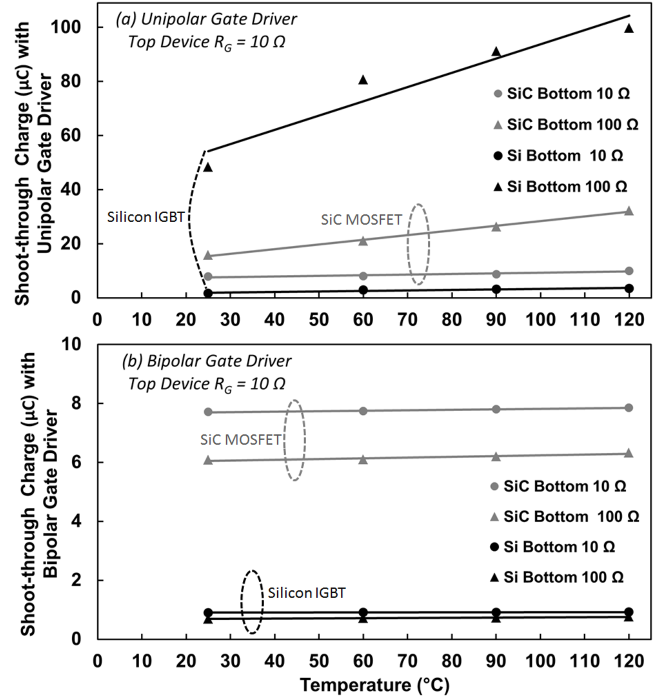

Fig. 25. Shoot-through charge of different R_G on bottom device, with (a) Unipolar and (b) Bipolar Gate drivers in Silicon and SiC devices.

Figure 26 shows the percentage reduction of shoot-through charge from the use of the bipolar gate drive for both technologies i.e. a measure of its effectiveness.

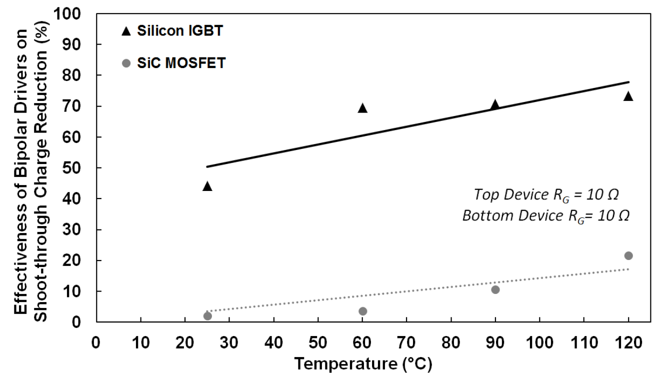

Fig. 26. Percentage reduction of shoot-through charge in both silicon and SiC device with R_G = 10 Ω showing that using a bipolar driver has a better impact on silicon IGBT device than the SiC device.

It can be seen from this figure that reduction of charge in Si-IGBT module is higher than the SiC MOSFET module. This can be seen by comparing Figure 19(b) and 19(d). Figure 27 and Figure 28 show the results of all correction techniques applied to each device technology at 25 °C and 120 °C using the shoot-through energy density as the indicator. As was explained in the previous sections, to provide a fair

comparison the shoot-through is represented by the energy density (mJ/cm^2) instead of energy (mJ). As can be seen from Figure 25, although the Si-IGBT module initially exhibits a higher shoot-through charge, using a Bipolar gate drive is more effective in reducing the shoot-through charge and energy. In Figure 27 and 28, it can be seen that applying a snubber capacitor does not have a considerable impact on reduction of the shoot-through energy density, although as it was seen previously, the use of the snubber capacitor mainly in the SiC MOSFET module is required for preventing ringing/oscillations in the turn-on of the bottom device. As these Figures show, the use of two resistive paths results in a very significant reduction of the shoot-through energy density and has the same effectiveness as a the use of a Bipolar gate drive in the Si-IGBT module. However, for the SiC MOSFET module, both techniques together the use of a snubber across the DC link is required.

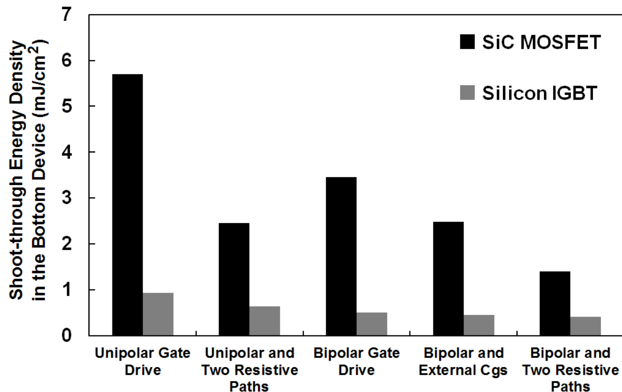

Fig. 27. Shoot-through energy density as a result of crosstalk in bottom device in 25 °C with R_G = 10 Ω (or its equivalent) in top and bottom devices.

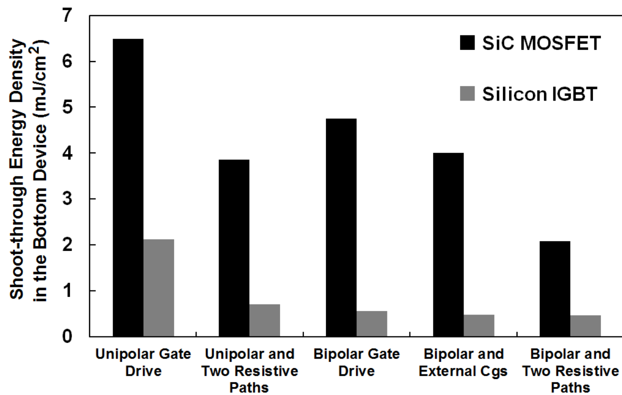

Fig. 28. Shoot-through energy density as a result of crosstalk in bottom device in 120 °C with R_G = 10 Ω (or its equivalent) in top and bottom devices.

V. Conclusion

Crosstalk has been modeled and experimentally characterized for SiC MOSFET and Si-IGBT power modules. It has been experimentally demonstrated that SiC devices normally have a lower shoot-through charge although often exhibit higher shoot-through energy. The lower shoot-through charge is due to a considerably smaller Miller capacitance in SiC MOSFETs compared with Si-IGBTs in spite of switching with higher *dV/dt* and having a lower threshold voltage. However, the higher shoot-through energy in SiC MOSFET modules is due to the ringing in the Schottky diode turn-off transient resulting in oscillations in the DC link voltage. It has also been demonstrated that the shoot-through charge in Si-IGBT module has a higher temperature coefficient for all conditions, meaning that it is more sensitive to ambient temperature rise. The temperature coefficient of the shoot-through charge in SiC is lower as a result of the lower threshold voltage temperature coefficient resulting from the wide-bandgap characteristics. Various correction techniques have been examined to mitigate the problem. For the Si-IGBT modules, the traditional solutions of negative gate bias and/or 2 resistive paths are sufficient in mitigating the problem. However, for the SiC MOSFET modules, the bipolar gate driver is not sufficient to completely solve the crosstalk problem since the threshold voltage of SiC devices is low and the *dV/dt* remains high. Furthermore, negative bias rating of the SiC MOSFET is lower than that of Si-IGBTs, hence, the margins for negative bias are smaller. It has also been shown that the presence of the snubber capacitor is required to damp the high frequency oscillations in the DC link resulting from diode ringing, in the case of SiC devices. Therefore, for the Si-IGBT modules, the bipolar gate driver with a negative bias value of at least five Volts should suffice to mitigate the possibility of shoot-through, whereas for SiC devices, due to the restrictions over the negative bias gate voltage, the two resistive path method in conjunction with the bipolar gate driver and the snubber capacitor are recommended.

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