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Robustness and Balancing of Parallel Connected Power Devices: SiC vs. CoolMOS

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***Abstract*—Differences in the thermal and electrical switching time constants between parallel connected devices cause imbalances in the power and temperature distribution thereby reducing module robustness. In this paper, the impact of electro-thermal variations (gate and thermal resistance) between parallel connected devices on module robustness is investigated for 900V-CoolMOS and 1.2kV-SiC MOSFETs under clamped inductive switching (CIS) and unclamped inductive switching (UIS). Under CIS, the difference in the steady-state junction temperature (ΔT_J) and switching energy (ΔE_{SW}) between the parallel connected devices for a given difference in the gate and thermal resistance (ΔR_G & ΔR_{TH}) is used as the metric for determining robustness to electrothermal variations i.e. how well the devices maintain uniform temperature in-spite of switching with different rates and thermal resistances. Under UIS conditions, the change in the maximum avalanche current/energy prior to device failure as a function of the ΔT_J and ΔR_G between the parallel connected devices is used as the metric. Under both CIS and UIS, SiC devices show better performance with minimal negative response to electrothermal variations between the parallel connected devices. Finite element models have also been performed showing the dynamics of BJT latch-up during UIS for the different technologies.**

***Index Terms*—CoolMOS, IGBTs, Silicon Carbide MOSFETs, Unclamped inductive switching**

I. Introduction

The ability of power semiconductor devices to share current and temperature in parallel is a very important feature because parallel connected devices are often required to deliver higher current ratings [1-7]. Although solder fatigue and wire-bond damage are the dominant failure mechanisms in power modules [8-14], it is nevertheless important to study the impact of possible electrothermal variations between parallel connected devices on the overall robustness of the power module. Differences in the electrical and thermal parameters of the individual devices can trigger other failure mechanisms [15, 16]. If parallel connected power devices are subject to different load currents, they will undergo different thermal cycles and hence, different degrees of thermo-mechanical fatigue from stress cycling due to CTE mismatch. This means the thermal resistance will degrade at different rates and the devices will thus operate at different junction temperatures. Hence, while thermo-mechanical fatigue may degrade the health of the module, the single event failure mechanism may be electrothermal overloading from the degraded safe-operating-area. Although devices may begin the application mission profile with minimal variation between the electrothermal parameters, over the course of operation in the field, this variation may increase due to the position dependency of the device or application related field fails. Electrothermal variations between parallel connected devices can also accelerate short circuit failure since the current is not shared equally between the parallel devices. The short circuit performance of SiC power devices have been studied in [17-19] hence, this paper does not focus on the short circuit performance.

Under normal operation in clamped inductive switching (CIS) conditions, the positive temperature coefficient of the on-state resistance of power MOSFETs makes them ideal for parallel operation since temperature limits the current [4, 20]. In unclamped inductive switching (UIS), it is the temperature coefficient of the breakdown voltage that regulates the current and temperature distribution between parallel connected devices [21-24]. CoolMOS devices use the principle of super-junctions to deliver low conduction losses by using alternate p and n columns in the voltage blocking drift layer [25-27]. CoolMOS competes with SiC in the sub 1200 V application space. In high current applications where several die are required in parallel, the ability of the devices to share current and temperature equally is important [28, 29]. How the current and temperature balancing capabilities of CoolMOS devices under CIS and UIS compare with SiC power MOSFETs is not known.

This paper studies the impact of variation in electrothermal parameters between parallel connected devices for the different technologies. The two principal parameters under investigation in this paper are electrical switching rates and the thermal

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resistance. Variations in the electrical switching time are set by the gate resistances which determine the *dI/dt* while variation in the thermal resistance is emulated by setting different initial junction temperatures between the parallel devices. Section II describes the experimental set-up used in this paper. Section III shows the results obtained from clamped inductive switching measurements. Section IV presents results from the unclamped inductive switching measurements. Section V presents finite element simulations supporting the experimental results while Section VI concludes the paper.

II. Experimental Set Up

The circuit diagram and picture of the experimental test rig is shown in Figure 1 and Figure 2 respectively. The parallel connected Devices under Test (DUTs) are driven by separate gate drives, a common 470 µF DC link capacitance, the same free-wheeling diodes and a DC power supply. Although the gate drivers are separate, they are identical circuits driven from the same signal generator and have thus been synchronized. Proper current/temperature sharing between the devices under identical conditions have been guaranteed before electrothermal variations are introduced. Hence, under repetitive clamped inductive switching, the case temperatures of 2 parallel connected devices identically driven by the 2 gate drives were within 1 °C of each other. The switching energies were also measured under identical conditions, and it was confirmed that the devices are identical in switching characteristics and the separate gate drivers have not introduced variations between the parallel devices. The SiC power MOSFETs are 1.2kV/10A devices from CREE with datasheet reference C2M0280120D while the CoolMOS devices are from Infineon and rated at 900V/15A with datasheet reference IPW90R340C3. Differences in the electrical response between parallel connected devices are set by ensuring $R_{G1} \neq R_{G2}$ and in the case of thermal response, $T_{J1} \neq T_{J2}$.

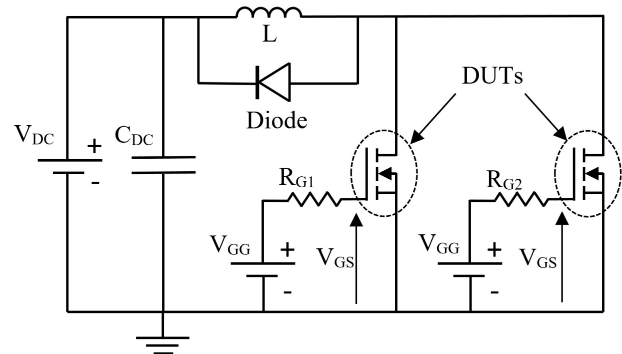

Fig. 1. Circuit schematic for the experimental set-up.

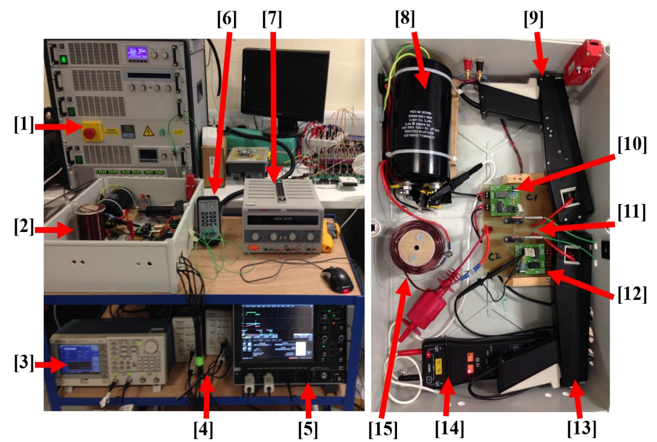

Fig. 2. This shows the picture of the experimental set-up with [1] Power Supply. [2] Test Chamber. [3] Function Generator. [4] Current probe Amplifier. [5] Oscilloscope. [6] Thermometer. [7] DC power supply for heater. [8] DC capacitor. [9] and [13] Current Probes. [10] and [12] Gate Drives. [11] DUTs. [14] Voltage probe. [15] Inductor.

III. Clamped Inductive Switching Measurements

A. The Impact of Switching Rate Mismatch

Figure 3(a) shows the turn-on current transient waveforms for the parallel connected SiC MOSFETs driven with different gate resistances while Figure 3(b) shows the same characteristics for the CoolMOS device. The drain voltage during switching is 300 V. It can be seen from Figure 3(a) and Figure 3(b) that the device with the smaller gate resistance switches faster thereby conducting more of the load current compared to the slower switching device. However, the difference between the currents in both devices is higher for the CoolMOS device compared to the SiC device in spite of the fact that the parallel pairs are driven with the same variations in switching speed. Figure 4(a) shows the measured turn-off characteristics for the parallel connected SiC MOSFETs switched with different rates while Figure 4(b) shows similar characteristics for the parallel CoolMOS devices. It can be seen in Figure 4, that contrary to Figure 3, the slower switching device conducts the bulk of the turn-off current because the entirety of the load current is diverted to it after the faster switching device is turned-off. Hence, at turn on, the faster switching devices experience higher power losses compared to the slower switching devices and at turn off, the converse is true.

The measured switching energy is calculated by integrating the dissipated power ($I_{DS} \cdot V_{DS}$) over the duration of the switching transients at turn-on and turn-off. Figure 5 shows the measured turn-on switching energy for the parallel connected SiC MOSFETs switched with different variations in switching rates i.e. $R_{G2} - R_{G1}$ where R_{G2} is the gate resistance of DUT2 and R_{G1} is the gate resistance of DUT1. The switching rate of DUT1 is held constant with a gate resistance R_{G1}=10 Ω while the switching rate of DUT2 is varied over a wide range of resistances. Figure 6 shows similar characteristics for the CoolMOS devices where the switching energies have been measured for each of the parallel DUTs switched at different rates. It is clear from Figure 5 and Figure 6 that not only do the SiC MOSFETs have smaller switching losses than the CoolMOS device but that the devices can cope with imbalances in the switching rates better. The maximum change in switching energies between the parallel connected DUTs is 40% higher for the CoolMOS devices under the same variation in switching

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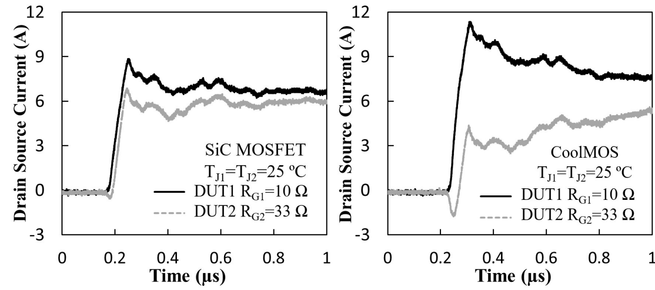

Fig. 3. (a) Turn-on current waveforms for parallel connected SiC MOSFETs with different switching rates. (b) Similar characteristics for the CoolMOS device.

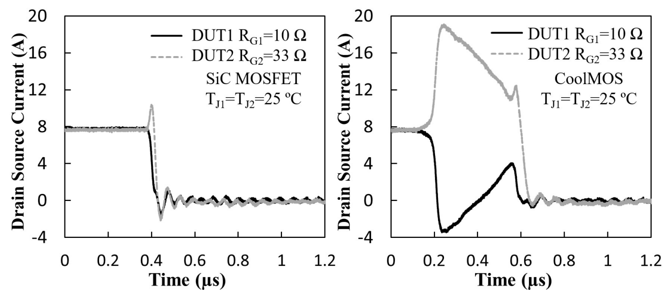

Fig. 4. (a) Turn-off current waveforms for parallel connected SiC MOSFETs with different switching rates. (b) Similar characteristics for the CoolMOS device.

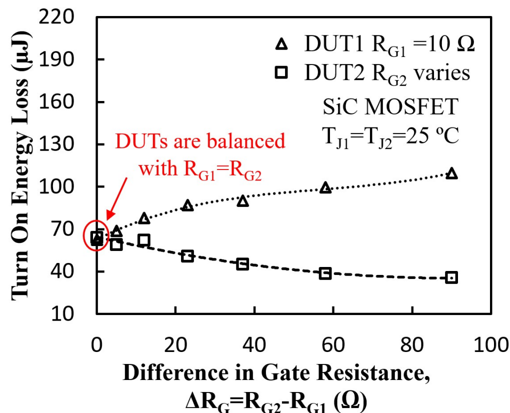

Fig. 5. The measured turn-on switching energies of the parallel connected SiC MOSFET as a function of the difference in gate resistance.

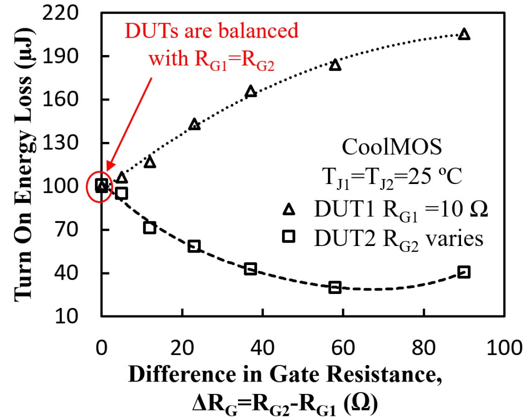

Fig. 6. The measured turn-on switching energies of the parallel connected CoolMOS devices as a function of the difference in gate resistance.

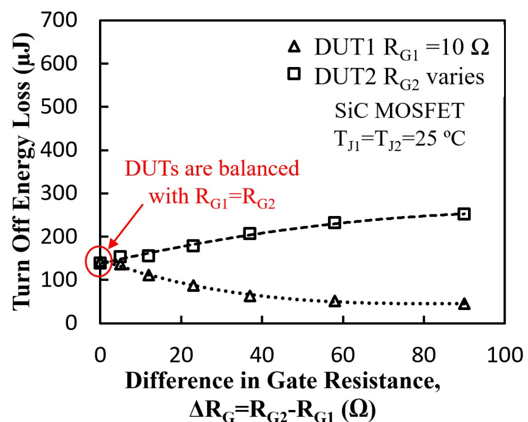

Fig. 7. The measured turn-off switching energies of the parallel connected SiC MOSFET as a function of the difference in gate resistance.

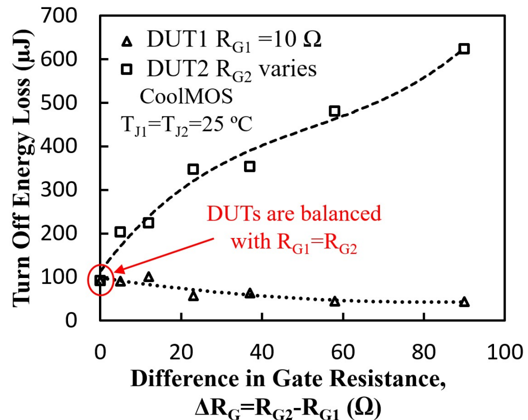

Fig. 8. The measured turn-off switching energies of the parallel connected CoolMOS devices as a function of the difference in gate resistance.

rates i.e. $\Delta R_G = R_{G2}-R_{G1}$. It can also be seen that this variation in switching energy (ΔE_{SW}) increases with the difference in switching rate (ΔR_G) for the CoolMOS while it is relatively more stable for the SiC devices i.e. $\Delta E_{SW}/\Delta R_G$ is higher for the CoolMOS than for the SiC device.

Figure 7 shows the measured turn-off switching energy for the parallel connected SiC MOSFETs while Figure 8 shows that of the CoolMOS devices. Unlike the turn-on characteristics shown in Figure 5 and Figure 6, the slower switching DUT exhibits higher switching energy. This is due to the current overshoots in the slower switching device during turn-off as shown in Figure 4. It can also be seen from Figure 7 and Figure 8 that ΔE_{SW} at a given ΔR_G is smaller for SiC compared to the CoolMOS device. This correlates well with Figure 4, where the current overshoot in the slower switching CoolMOS device is much higher than that in the SiC MOSFET.

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The case temperatures have also been measured for each of the parallel DUTs so as to ascertain how the variation in switching rates (ΔR_G) impacts the respective junction/case temperatures of the individual DUTs. Due to the smaller die size in SiC MOSFETs, the junction-to-case thermal resistance for the SiC MOSFET is 1.8 °C/W while that of the CoolMOS device is 0.6 °C/W. Figure 9(a) shows the measured case temperature rise for the parallel connected SiC MOSFETs with repetitive switching at a frequency of 2 kHz with DUT1 switched at 10 Ω and DUT2 switched at 33 Ω. Figure 9(b) shows similar characteristics for the CoolMOS devices.

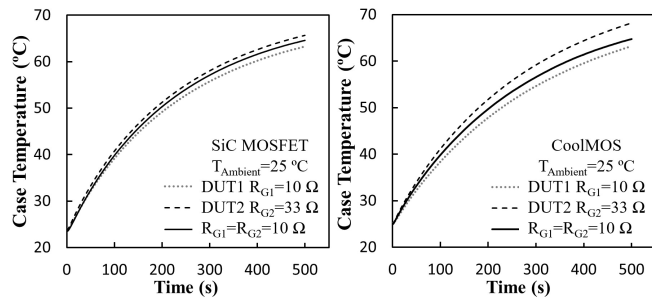

Fig. 9. (a) The measured case temperature rise for the parallel connected SiC MOSFETs switched with R_G of DUT1 and DUT2 as 10 Ω and 33 Ω respectively. (b) Similar measurements for the CoolMOS device.

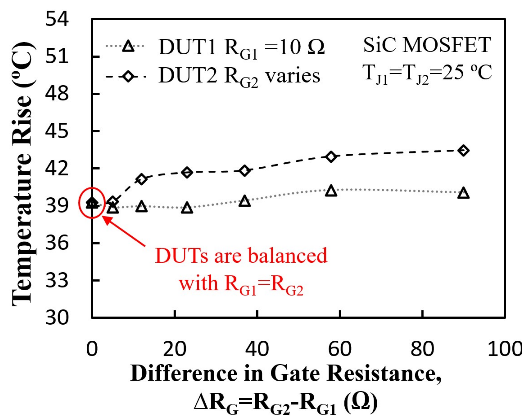

Fig. 10. The measured case temperature rise for the parallel connected SiC MOSFETs switched at different rates.

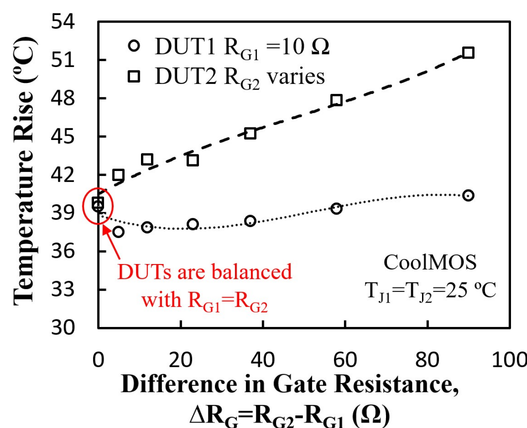

Fig. 11. The measured case temperature rise for the parallel connected CoolMOS devices switched at different rates.

It can be seen in Figure 9 that the variation in the case temperature between the parallel connected DUTs is higher for the CoolMOS device than for the SiC MOSFETs. Figure 10 shows the measured steady state case temperatures for the parallel connected SiC MOSFETs repetitively switched at 2 kHz with different magnitudes of ΔR_G=R_{G2}-R_{G1}. Figure 11 shows the same plot for the CoolMOS device. By comparing Figure 10 and Figure 11, it can be seen that the SiC MOSFETs show less temperature variation (ΔT_J) between the respective DUTs compared with the CoolMOS devices. Hence, the impact of mismatch in the switching rate of the parallel connected devices results in less temperature mismatch for the SiC MOSFETs compared with the CoolMOS devices. The smaller die sizes and less temperature sensitive electrical parameters in SiC mean that variations in temperature and switching rate between the parallel connected DUTs result in less mismatch in switching energy and dissipated power.

B. *Impact of Initial Junction Temperature Mismatch*

Similar measurements have been performed for parallel connected devices, however, with different initial junction temperatures. The initial junction temperatures are set by electric hot-plates connected to the base of the device. Since the system is at steady-state, it can be assumed that the case temperature is equal to the junction temperature. Figure 12(a) shows the turn-on current for the parallel connected SiC MOSFETs with different junction temperatures set by the heaters. Again, V_{DS}=300 V. Figure 12(b) shows a similar plot for the CoolMOS devices. Figure 12 shows that the hotter device takes less current as expected because of the positive temperature coefficient of the on-state resistance and the current divider rule which stipulates that the more current flows through the more conductive device. By comparing the SiC and CoolMOS characteristics it can be seen that the steady state current mismatch is less for the SiC device compared with the CoolMOS device. This is due to the fact that SiC is more temperature resilient since its wide bandgap ensures that thermally generated carriers for any given temperature are smaller compared to those in silicon devices.

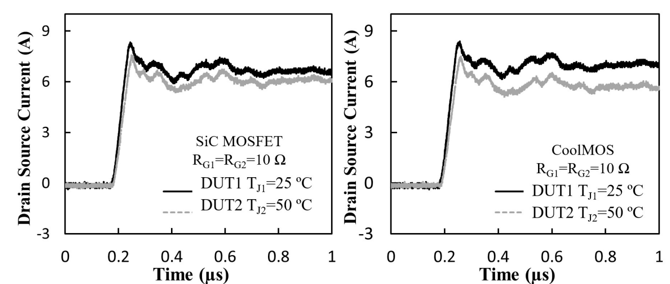

Fig. 12. (a) The measured turn-on current for the parallel connected SiC MOSFETs driven at 2 different junction temperatures. (b) Similar measurements for the CoolMOS device.

Figure 13 shows the measured turn-on energy of the parallel connected SiC MOSFETs with different magnitudes of initial

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junction temperature mismatch between the DUTs i.e. DUTs set at different $\Delta T_J = T_{J2} - T_{J1}$ where T_{J2} is the junction temperature of DUT2 and T_{J1} is the junction temperature of DUT1. In Figure 13, the junction temperature of DUT1 is held constant at 25 °C while the junction temperature of DUT2 is varied over a wide temperature range. Figure 14 shows similar characteristics for the CoolMOS device. It can be seen from Figure 13 and Figure 14 that the turn-on energy of the device at the higher junction temperature is lower. This is expected in MOSFETs because the turn-on dI_{DS}/dt increases with temperature as a result of the negative temperature coefficient of the MOSFET threshold voltage. It can also be seen by comparing Figure 13 with Figure 14 that the difference in turn-on energy loss (ΔE_{SW}) between the parallel connected DUTs is smaller in SiC and remains more stable as ΔT_J is increased. Hence, it is demonstrated that parallel connected SiC MOSFETs perform better than CoolMOS devices under both temperature and switching rate imbalances. As can be seen from the CoolMOS measurements in Figure 14, increasing the temperature difference (ΔT_J) between the parallel DUTs results in much higher switching energy variation (ΔE_{SW}) compared with the SiC MOSFETs.

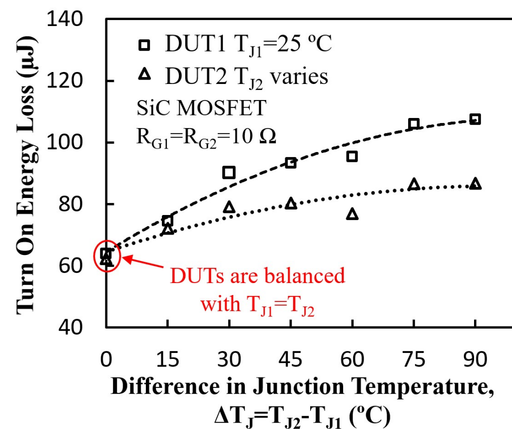

Fig. 13. Measured turn-on switching energy for the parallel connected SiC MOSFETs with the DUTs set at different junction temperatures.

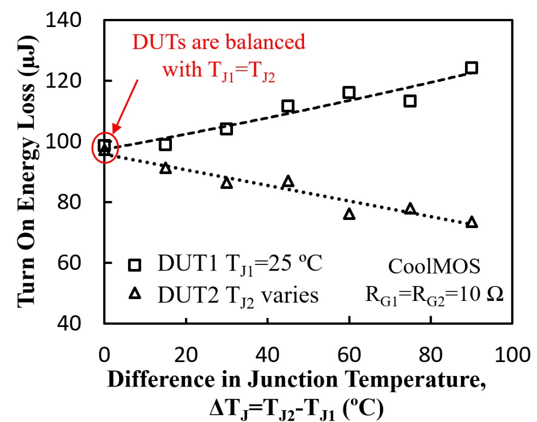

Fig. 14. Measured turn-on switching energy for the parallel connected CoolMOS devices with the DUTs set at different junction temperatures.

IV. Unclamped Inductive Switching Measurements

Under unclamped inductive switching (UIS), the device conducts current in avalanche mode. Avalanche mode conduction occurs when the electric field across the device exceeds the critical field, thereby causing carriers to accelerate, collide with atoms and generate additional electron-hole pairs if the collision energy exceeds the bandgap of the semiconductor. UIS measurements have also been performed on the parallel connected DUTs with mismatch in both the switching rate and initial junction temperatures. The goal was to determine the impact of mismatch between the parallel connected DUTs on the overall electrothermal robustness of the parallel pair. In UIS, the free-wheeling diode in parallel with the inductor is removed so that the inductor forces current through the parallel DUTs as they turn-off. The measurement set-up for UIS can be seen in [30, 31]. The size of the inductor determines the avalanche duration. As the parallel connected DUTs are forced into UIS, they will share current according to their breakdown voltages i.e. the device with the smaller breakdown voltage goes into avalanche. During UIS, the V_{DS} rises to the breakdown voltage of the device. The initial conditions of the DUTs will impact the avalanche breakdown characteristics. The failure mode from UIS is parasitic BJT latch-up within the device which results from hole currents in the body causing a voltage drop between the source and p-body [32, 33]. Within a single device, non-uniformities between parallel conducting FET cells accelerates BJT latch-up. This is likewise the case between parallel conducting devices.

Figure 15(a) shows the avalanche current characteristics for each of the parallel connected SiC MOSFETs conducting current under UIS with different gate resistances. The supply voltage for the UIS measurements is 50 V. In Figure 15(a), DUT1 is driven by a 10 Ω gate resistance while DUT2 is driven by a 33 Ω gate resistance. Figure 15(b) shows similar characteristics for the parallel connected CoolMOS devices driven with the same combination of mismatched gate resistances. It can be seen from both figures that the slower switching device fails under UIS. This is due to the fact that the slower switching DUT is still partially conducting at the time the avalanche current starts flowing. As a result the bulk of the avalanche current is forced through the slower switching DUT.

Figure 16(a) shows the avalanche current characteristics for each of the parallel connected SiC MOSFETs conducting current under UIS with different initial junction temperatures. The junction temperature of DUT1 is set at 25 °C while that of DUT2 is set at 50 °C. Figure 16(b) shows the results of similar measurements performed on the CoolMOS devices. It can be seen from both plots in Figure 16 that the DUT with the initially lower temperature fails under UIS while that with the higher junction temperature does not. This results from the positive temperature coefficient of the breakdown voltage which means that the DUT with the higher initial junction temperature will have a higher breakdown voltage. This is due to increased

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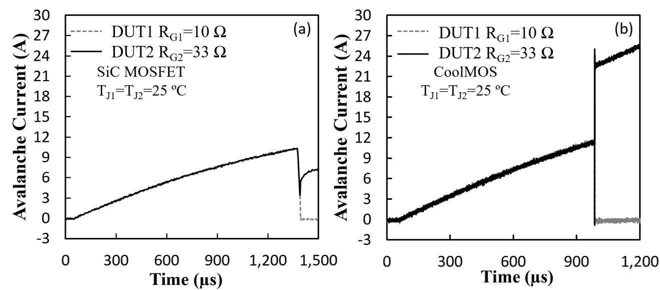

Fig. 15. (a) Avalanche current characteristics for the parallel connected SiC MOSFETs with different R_G. (b) Similar characteristics for CoolMOS.

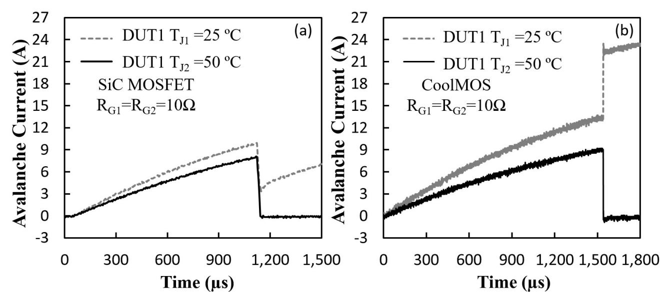

Fig. 16. (a) Avalanche current characteristics for the parallel connected SiC MOSFETs with different T_J. (b) Similar characteristics for CoolMOS.

phonon scattering reducing the carrier mean-free-path thereby delaying the on-set of sustained impact ionization that is necessary for avalanche mode conduction. Hence, the cooler DUT has a lower breakdown voltage and conducts all of the avalanche current which triggers the parasitic BJT and results in device failure. It can be seen from Figure 16 that the difference in the peak avalanche current between the parallel connected DUTs is higher for the CoolMOS than for the SiC MOSFET. This is due to the lower temperature coefficient of the on-state current in SiC compared to the CoolMOS device, hence, the imbalance in peak avalanche current between the parallel connected DUTs is lower in SiC than in CoolMOS.

The maximum avalanche current that the parallel connected DUTs are able to safely conduct (without thermal runaway) with a given mismatch in temperature and switching rate (ΔT_J and ΔR_G) has been determined for different avalanche durations and for each device technology. This was done by increasing the duration of the gate pulse which in turn increases the current through the inductor and the peak avalanche current during UIS. It is known that the peak avalanche current that the DUTs can withstand without failure reduces as the avalanche duration increases since the total avalanche energy dissipated by the DUT is approximately equal to the energy stored in the inductor i.e. $0.5 \cdot LI^2$. Hence, as a larger inductor is used (avalanche duration is increased), the peak current that the DUTs can safely conduct reduces and vice versa [31, 34]. It is expected that introducing mismatch (ΔT_J and ΔR_G) in the parallel connected DUTs will reduce the total peak avalanche current and energy sustainable by the parallel connected DUTs so the goal in these measurements is to quantify the reduction for the respective device technologies.

Figure 17 shows the peak avalanche energy sustained by the parallel connected SiC MOSFETs driven with different ΔR_G combinations. The UIS measurements have been performed with 3 different inductors which are used to set the avalanche duration. Figure 18 shows the same measurements performed on the CoolMOS devices. For both technologies, it is clear that increasing the switching rate mismatch (ΔR_G) reduces the total avalanche energy the parallel combination can withstand. This is for reasons explained in Figure 15 and Figure 16. However, what is also noticeable in Figure 17 and Figure 18 is that the rate at which the peak energy decreases with increasing ΔR_G is much higher for CoolMOS than for SiC. In other words, the parallel SiC MOSFETs are more avalanche rugged with increasing switching rate mismatch (ΔR_G) than the CoolMOS devices.

Figure 19 shows the peak avalanche energy sustained by the parallel connected SiC MOSFETs driven with different ΔT_J combinations. Figure 20 shows similar measurements for the CoolMOS devices. Similar to variations in the switching rate, the parallel connected SiC MOSFET perform better under temperature imbalance. Although the peak avalanche energy

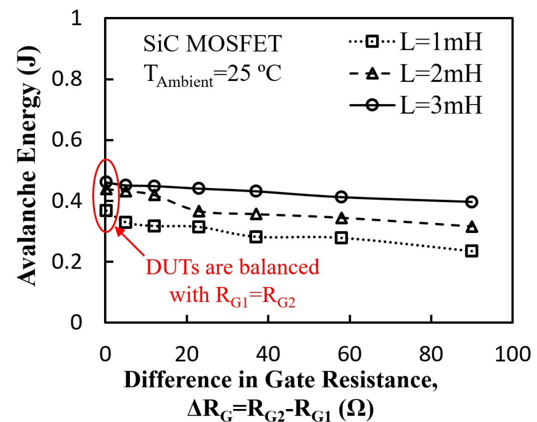

Fig. 17. Peak avalanche energy in the parallel connected SiC MOSFETs for different ΔR_G before failure under UIS.

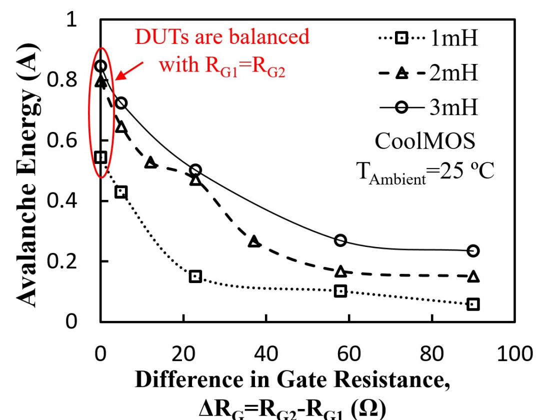

Fig. 18. Peak avalanche current in the parallel connected CoolMOS devices for different ΔR_G before failure under UIS.

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reduces with increasing temperature mismatch (ΔT_J) between the parallel connected DUTs, the reduction is quite small for the SiC MOSFETs compared with CoolMOS devices.

Figure 21 shows the comparison of the percentage change in the measured peak avalanche energy (E_{AV}) for different ΔR_G in the parallel SiC and CoolMOS devices. It can be seen that the percentage change in the maximum avalanche energy is significantly smaller in the SiC MOSFETs than in the CoolMOS device. Figure 22 shows a similar plot, but with temperature variation between the parallel DUTs. Similar to the switching rate variation, the parallel connected SiC MOSFETs exhibit smaller variation in the avalanche characteristics.

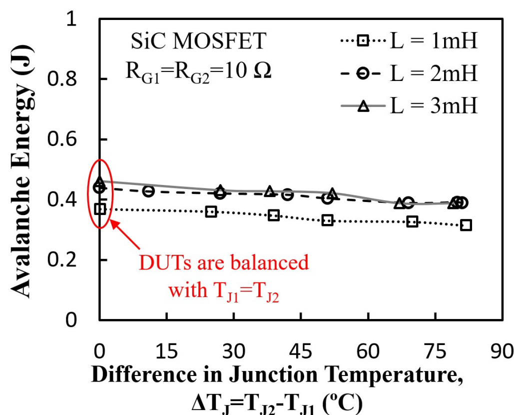

Fig. 19. Peak avalanche current in the parallel connected SiC MOSFETs for different ΔT_J before failure under UIS. 7

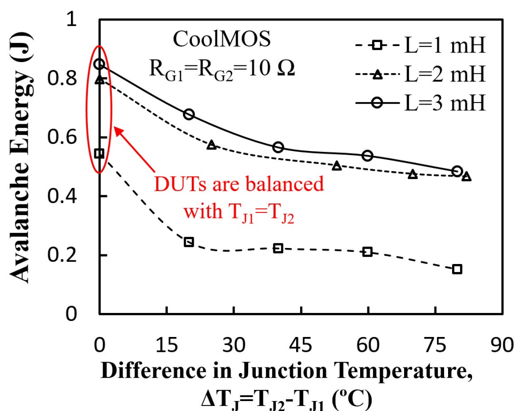

Fig. 20. Peak avalanche current in the parallel connected CoolMOS devices for different ΔT_J before failure under UIS.

Figure 23 shows the percentage change in the switching energy as a function of the variation in the switching rate (ΔR_G). The SiC MOSFETs perform better than the CoolMOS since the variation in the switching energy is less for a given magnitude of ΔR_G between the parallel connected DUTs. A similar plot is shown in Figure 24 for parallel connected devices set at different junction temperatures. Again, the percentage change in

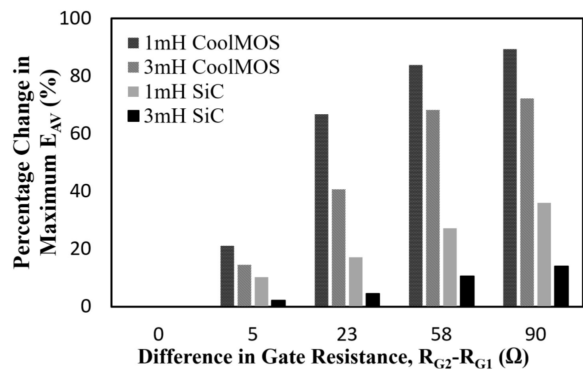

Fig. 21. Percentage change in the peak avalanche energy (E_{AV}) as a function of the switching rate difference between the parallel DUTs

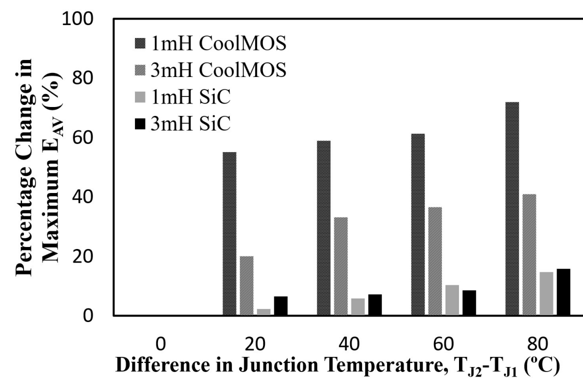

Fig. 22. Percentage change in the peak avalanche energy (E_{AV}) as a function of the temperature difference between the parallel DUTs

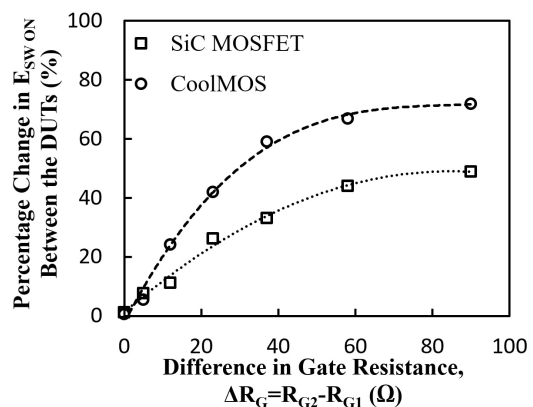

Fig. 23. Percentage change in the turn-on switching energy (E_{SW}) as a function of the switching rate difference (ΔR_G) between the parallel DUTs.

the switching energy for a given ΔT_J is smaller for the SiC MOSFETs than for the CoolMOS devices.

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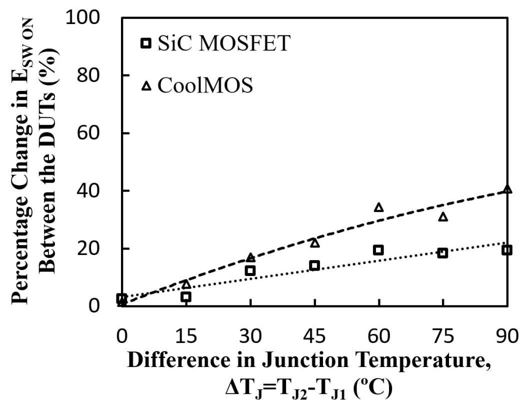

Fig. 24. Percentage change in the turn-on switching energy (E_{SW}) as a function of the junction temperature difference (ΔT_J) between the parallel DUTs.

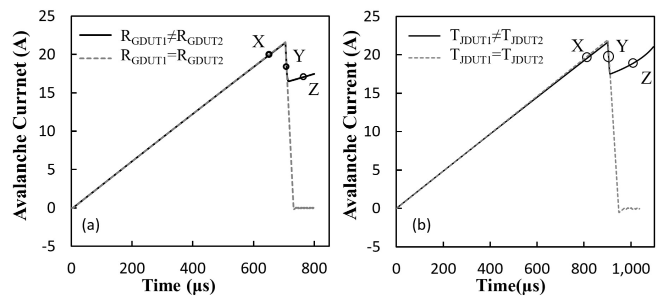

Fig. 25. (a)Simulated avalanche characteristics showing latch-up in parallel connected DUTs with $R_{G1}=R_{G2}$ and $R_{G1}\neq R_{G2}$. (b) Similar characteristics with $T_{J1}=T_{J2}$ and $T_{J1}\neq T_{J2}$.

V. FINITE ELEMENT SIMULATIONS

Finite element simulations have been performed in order to replicate the experimental measurements so as to understand the failure modes of parallel connected devices under UIS. The device simulations were done in SILVACO and the circuit simulations were performed using the mixed mode circuit application to solve the transient and steady-state circuit equations. The FET cells were simulated in parallel for both the SiC MOSFET and CoolMOS devices. The source n-type doping in the SiC MOSFET was set at 1×10^{19} cm^{-3} and the p-body doping was 5×10^{17} cm^{-3}. The doping of the deep p-body implant was set at 1×10^{19} cm^{-3}. The drift layer thickness was set at 7 µm and the doping was set at 1×10^{16} cm^{-3}. The channel length was set at 1.9 µm and the cell area was 1.5 mm^2. The concentration dependent mobility model was used and the heat capacity and thermal conductivity were set as temperature dependent. In the case of the CoolMOS the p-pillar and n-drift region doping was balanced at 1×10^{15} cm^{-3} to have the maximum breakdown voltage. Similar source and drain doping was used in the CoolMOS simulations. The oxide thickness for both devices was set at 50 nm. The lattice heating application package was activated to include electrothermal effects together with the appropriate impact ionization and temperature dependent mobility models.

Figure 25(a) shows the typical avalanche current characteristics for 2 parallel connected DUTs with equal and non-equal gate resistances. It can be seen that BJT latch-up occurs in the devices with $R_{G1}\neq R_{G2}$ while it does not occur in the devices with $R_{G1}=R_{G2}$. Figure 25(b) shows similar avalanche current characteristics, however with the parallel connected DUTs set at different initial junction temperatures. Again, the device with $T_{J1}=T_{J2}$ does not undergo BJT latch-up while the device with $T_{J1}\neq T_{J2}$ does. Two-dimensional current density contour plots have been extracted from the simulator at various points in time during the UIS characteristics. These have been labelled in Figure 25 as points X, Y and Z. The goal of these current density plots is to understand the internal current distribution within the devices during UIS for SiC MOSFETs and CoolMOS devices.

Figure 26 shows the 2-D current density contour plots of the parallel connected SiC MOSFETs at point X during the normal on-state conduction period of the UIS characteristics. It can be seen from Figure 26 that both DUTs conduct current normally prior to the on-set of avalanche. Figure 27 shows the 2-D current density contour plots at point Y (avalanche mode) for the parallel connected DUTs. It can be seen that the DUT with R_G=10 Ω conducts the avalanche current through the deep p-body that constitutes the internal body diode of the device. This region is usually doped with a high p+ concentration to ensure that the body is adequately shorted to the source in order to pre-empt the triggering of the parasitic BJT. However, it is evident from the current density contour plots of the DUT with R_G=33 Ω, that there is significant lateral current through the lightly doped p-body under the channel. This is due to the lower breakdown voltage since the slower switching device is not completely turned-off when the faster switching device abruptly diverts the current away i.e. at the instant when turn-off is initiated, the slower switching device has a lower breakdown voltage because it is not fully turned off.

Figure 28 shows the 2D current density contour plots for both DUTs at point Z corresponding to Figure 25(a), where it can be seen that the DUT with R_G=10 Ω does not conduct any current whereas that with R_G=33 Ω is in full BJT latch-up i.e. the current flows through the npn BJT. This is in agreement with the experimental measurements shown in Figure 15(a).

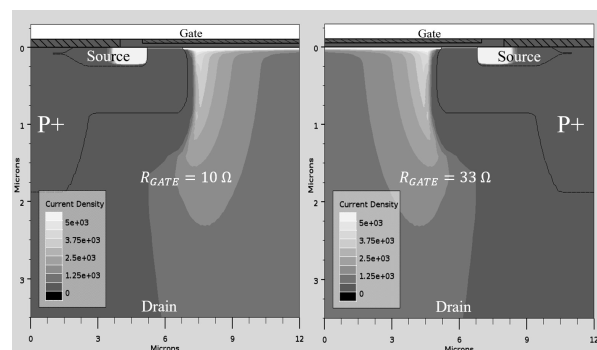

Fig. 26. 2D current density plots for parallel connected SiC with different gate resistances under UIS. This corresponds to point X in Fig. 25(a) where the DUTs are under normal conduction mode.

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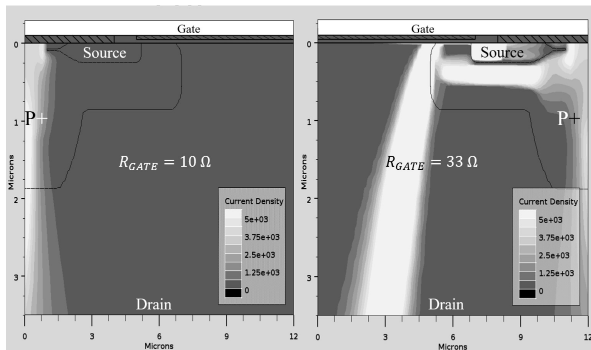

Fig. 27. 2D current density plots for parallel connected SiC with different gate resistances under UIS. This corresponds to point Y in Fig. 25(a) where the DUTs are under avalanche mode conduction.

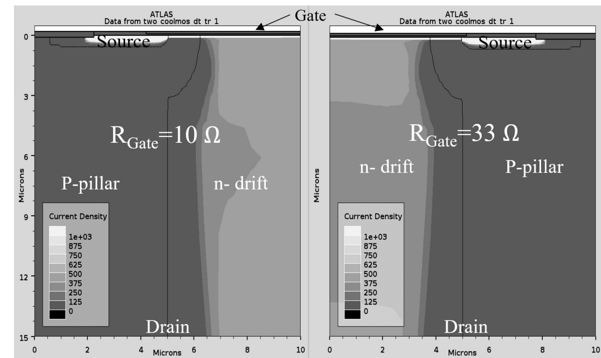

Fig. 29. 2D current density plots for parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point X in Fig. 16(a) where the DUTs are under normal conduction mode.

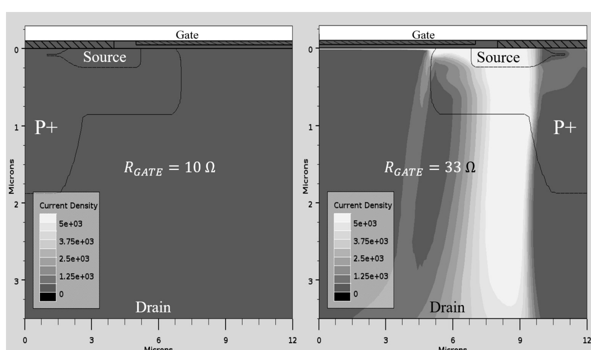

Fig. 28. 2D current density plots for parallel connected SiC with different gate resistances under UIS. This corresponds to point Z in Fig. 25(a) where the slower switching DUT fails under BJT latch-up.

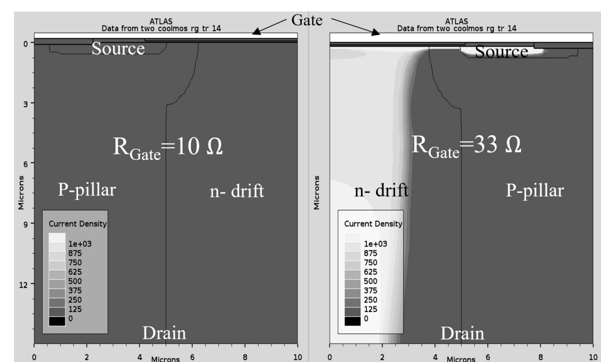

Fig. 30. 2D current density plots for parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point Y in Fig. 16(a) where the DUTs are in avalanche mode conduction.

Similar characteristics are shown for the CoolMOS devices where Figure 29 shows the 2D current density contour plots at point X (conduction mode), Figure 30 shows the 2D plots at point Y (avalanche mode) and Figure 31 at point Z (BJT latch-up). The CoolMOS devices exhibit different latch-up characteristics than the SiC MOSFETs. By comparing Figure 31 to Figure 28, it can be seen that under BJT latch-up, the CoolMOS device exhibits more lateral currents due to presence of the p-pillar in the drift region.

Figure 32 shows the 2D current density contour plots for the parallel SiC MOSFETs with different junction temperatures under UIS at point Z (in Figure 25(b)) where the devices are in latch-up. Figure 33 shows similar characteristics for the CoolMOS device. Similar to the experimental measurements in Figure 11, the DUTs with the lower junction temperature (T_J=25 °C) undergoes BJT latch-up due to its lower breakdown voltage. This was confirmed by electric field plots showing higher fields in the device with the higher junction temperature. It can be seen that the avalanche current in the CoolMOS device has a significant lateral component while that in the SiC MOSFET is mostly vertical. The wider bandgap means that the temperature coefficient of the impact ionization rate in SiC is smaller compared to that in the silicon CoolMOS device Hence, variations in the junction temperature between the parallel DUTs cause less of a variation in the breakdown voltage in the SiC devices, therefore, the total avalanche energy sustainable by the parallel pair is less affected by variations in the initial junction temperature.

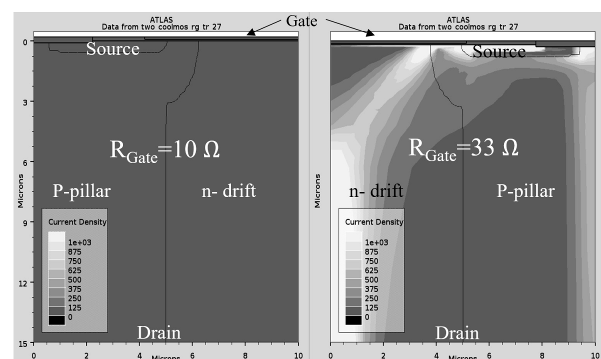

Fig. 31. 2D current density plots for parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point Z in Fig. 16(a) where the slower switching DUT fails under BJT latch-up.

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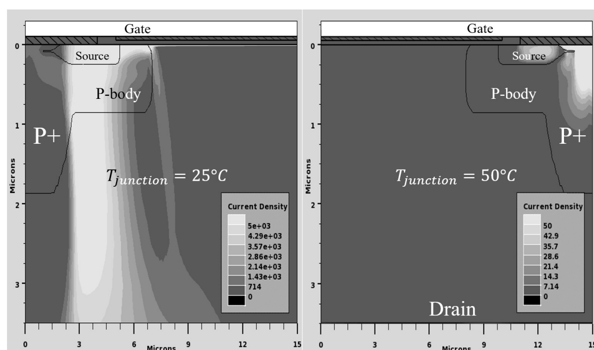

Fig. 32. 2D current density plots for parallel connected SiC MOSFETs with different junction temperatures under UIS. Here, the cooler DUT fails in BJT latch-up.

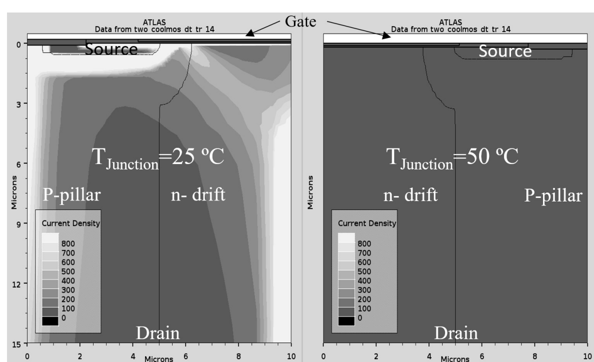

Fig. 33. 2D current density plots for parallel connected CoolMOS with different junction temperatures under UIS. Here, the cooler DUT fails in BJT latch-up.

VI. CONCLUSIONS

In conclusion, it has been demonstrated that parallel connected SiC MOSFETs are more resilient to electrothermal imbalance than CoolMOS devices under both clamped and unclamped inductive switching. Given the same variations in switching rates and thermal resistance (junction temperature), SiC MOSFETs will exhibit less variations in the switching energy, steady state operating temperatures, maximum avalanche energy and output characteristics. This is due to lower switching losses (due to smaller parasitic capacitances) and less temperature sensitive electrical parameters.

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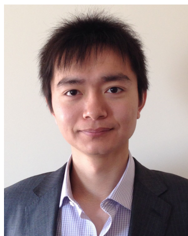

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