The Effect of Electrothermal Non-Uniformities on Parallel Connected SiC Power Devices under Unclamped and Clamped Inductive Switching

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***Abstract*—Non-uniformities in the electrothermal characteristics of parallel connected devices reduce overall reliability since power isn't equally dissipated between the devices. Furthermore, a non-uniform rate of operational degradation induces electrothermal variations thereby accelerating the development of failure. This paper uses simulations and experiments to quantitatively and qualitatively investigate the impact of electrothermal variations on the reliability of parallel connected power devices under unclamped inductive switching (UIS) conditions. This is especially pertinent to SiC where small die areas mean devices are often connected in parallel for higher current capability. Measurements and simulations show that increasing the variation in the initial junction temperatures and switching rates between parallel connected devices under UIS reduces the total sustainable avalanche current by 10%. It is seen that the device with the lower junction temperature and lower switching rate fails. The measurements also show that the maximum sustainable avalanche energy for a given variation in junction temperature and switching rate increases with the avalanche duration, meaning that the effect of electro-thermal variation is more critical with high power (high current & low inductor) UIS pulses compared with high energy (low current & high inductance) pulses. These results are important for condition monitoring and reliability analysis.**

***Index Terms*—Parasitic Bipolar Latch-up, SiC Power MOSFETs, Unclamped Inductive Switching**

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I. Introduction

POWER modules are usually comprised of a number of dies connected in parallel for the purpose of delivering higher current ratings. Likewise, power devices are comprised of several cells internally connected in parallel thereby sharing common terminals and delivering the rated current of the device. Process variations mean that the electrical and thermal parameters of the switching device may not always be exactly uniform. This can be true of separate discrete power devices as well as the internal FET cells of a single power device. Since commercial semiconductor fabrication processes are often designed to tightly limit the variation in the electrical parameters across the wafer from which the devices are derived, there are limits to the variation of these electrical parameters e.g. breakdown voltage, on-state resistance, threshold voltage etc. However, operational degradation of the devices does not usually occur at the same rate. Devices connected in parallel may begin the operational mission profile with almost identical thermal and electrical parameters, however, over time, may develop variations resulting from non-uniform rates of degradation. For instance, the thermal resistances of the power devices typically increase as a result of solder joint degradation due to thermo-mechanical stresses arising from coefficient of thermal expansion (CTE) mismatch between the die and the substrate [1-4]. Depending on the position of the device on the heat-sink, this effect of mechanical degradation may not occur at the same rate. Parallel connected devices with different degrees of solder joint delamination will have different thermal resistances and therefore different electro-thermal properties arising from different junction temperatures. Another source of possible variation is the electrical switching time constant, which is determined by the gate resistance and internal capacitances. Over the operating life of the power device, thermo-mechanical stresses from temperature and power cycles mean that the gate resistance is likely to increase as a result of wire-bond mechanical degradation [2, 5]. If this degradation occurs at a non-uniform rate between parallel connected devices, then a situation can arise whereby parallel connected devices have significantly different gate resistances and therefore switch at different rates. Although less likely, the gate capacitance can increase as a result if higher interface and fixed oxide charges from the adjacent channel. This can cause variation in the electrical switching time constant between the parallel connected devices. This problem is all the more pertinent to

SiC power devices where small die areas mean several devices are often required to meet defined current ratings. Furthermore, during operation at higher switching frequencies, which is seen to be the unique advantage of SiC unipolar devices, variations in electrothermal switching characteristics constitute more of a reliability concern.

It is well understood that the failure mode of power devices under unclamped inductive switching (UIS) are of 2 categories which are (i) parasitic bipolar latch-up for UIS pulses with high currents and low durations [6-8] and (ii) intrinsic temperature limitations for lower current pulses over a long avalanche duration [7, 9, 10]. The wider bandgap, higher critical electric field and higher thermal conductivity of SiC means that the devices are more robust under UIS compared to similarly rated technologies as has already been demonstrated in [9, 11-16]. However, the impact of electro-thermal variations in parallel connected devices under UIS has yet to be determined. Furthermore, how these electro-thermal variations impact the overall reliability of parallel connected devices for high power avalanche pulses with short durations compared to smaller power avalanche pulses over longer avalanche durations is interesting to consider.

This paper uses experimental measurements and simulations of parallel connected SiC power devices to understand the impact of electro-thermal variation on module reliability. The impact of variations in the junction temperature and gate resistance between parallel connected SiC MOSFETs on overall avalanche ruggedness is analyzed using a dedicated test rig and a finite element solver. Section II presents the experimental set-up used to investigate the problem of how electrothermal variation in parallel connected devices affects overall reliability under UIS. Section III introduces the finite element models of the parallel connected devices where the internal physics of device failure under UIS is assessed. Section IV discusses clamped inductive switching while section V concludes the paper.

II. EXPERIMENTAL MEASUREMENTS AND OBSERVATIONS

Fig.1(a) shows the circuit schematic of the experimental set-up used for the investigations while Fig. 1(b) shows a photograph of the set-up comprising of the power supply, DC link capacitor, inductor, gate drivers, measurement instrumentation and the 2 parallel devices under test (DUTs). The devices under investigation are 1.2kV/10A CREE SiC MOSFETs with datasheet reference C2M0280120D. The avalanche current is determined by the duration of the gate pulse which charges the inductor. The turn-on and turn-off gate voltages were set as 18 V and 0 V respectively. The negative temperature coefficient of the threshold voltage means that the V_{TH} reduces as the temperature increases. However, for the temperature range that will be examined in this paper (between 25 and 110 °C), the threshold voltage reduction is not sufficient to affect avalanche current sharing between the parallel connected DUTs since the avalanche duration will be much longer than the turn-off time. According to the temperature dependency of the threshold voltage presented on the datasheet of the device, the maximum difference in threshold voltage between the parallel connected devices will be limited to 0.5 V corresponding to a temperature difference of 85°C between the DUTs. Fig. 1(c) shows typical avalanche characteristics for a 1.2 kV SiC MOSFET under UIS. In Fig. 1(c), the current ramp up phase can be seen while the gate voltage is on. It can also be seen that the drain-source voltage rises abruptly to the breakdown voltage as the gate voltage is turned off and the device conducts in avalanche.

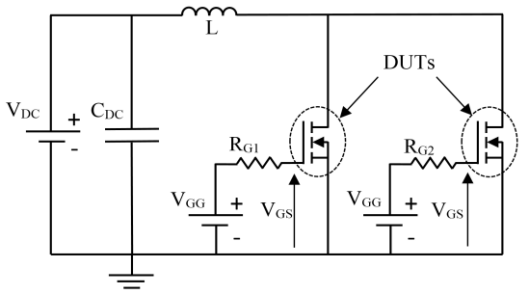

Fig. 1(a). Circuit schematic for the experimental set-up.

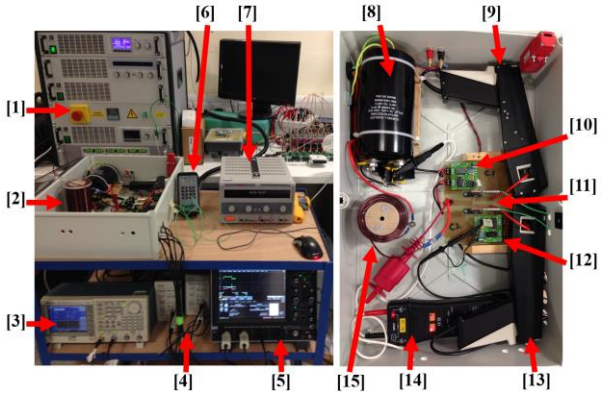

Fig. 1(b). The picture of the experimental set-up with [1] Power Supply. [2] Test Chamber. [3] Function Generator. [4] Current Probe Amplifier. [5] Oscilloscope. [6] Thermometer. [7] DC Power Supply for Heater. [8] DC Capacitor. [9] and [13] Current Probes. [10] and [12] Gate Drives. [11] DUTs. [14] Voltage Probe. [15] Inductor.

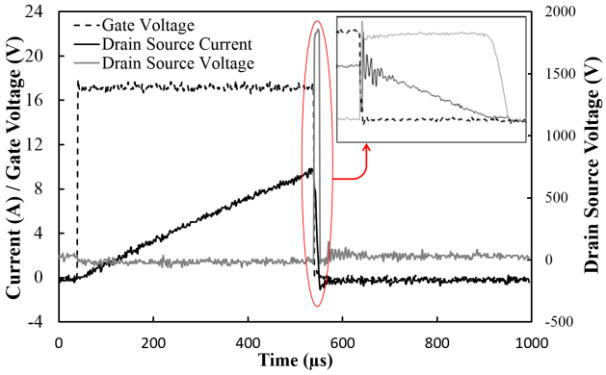

Fig. 1(c). Typical avalanche characteristics showing the gate voltage, drain voltage and drain-source current during the charging and avalanche conduction phases.

UIS pulses can come in the form of higher avalanche current with a short avalanche duration (using a small inductor) or a smaller avalanche current dissipated through the

DUT over a longer avalanche duration (using a larger inductor). The failure mode triggered by large peak avalanche currents is parasitic BJT latch-up which is ultimately induced by current crowding due to electro-thermal non-uniformity between the internal FET cells of the device [15-17]. The failure mode triggered by long avalanche durations is a maximum temperature limitation set by the material properties of the semiconductor. Fig. 2(a) shows how the maximum avalanche current sustainable by the DUT before failure under UIS is determined by progressively increasing the peak avalanche current through the duration of the charging gate pulse. Fig. 2(b) shows the peak avalanche current characteristics of the SiC MOSFET that has failed under UIS for 2 different avalanche durations. It can be seen that the peak avalanche current sustainable by the device decreases with increasing avalanche duration i.e. when a larger inductor is used, a smaller peak current is needed to destroy the device. Fig. 2(c) shows pictures of de-capsulated 1.2kV/24A and 1.2kV/10A SiC power MOSFETs that have failed under UIS with the burn marks due to thermal runaway showing. The de-capsulation was done destructively using mechanical force while ensuring that the process did not alter the die surface. The burn marks occur just underneath the source wire-bonds where high current densities are likely to occur due to the proximity of the source wires. Fig. 2(d) shows the measured maximum sustainable energy successfully dissipated by the DUT prior to failure under UIS for different avalanche durations and temperatures. It can be seen that higher avalanche energies can be dissipated by the device if it comes in the form of lower peak avalanche currents over longer durations [16, 18].

It can also be observed from Fig. 2(d) that increasing the ambient temperature of the UIS experiment decreases the overall sustainable energy as expected. In the next phase of the experiments, the impact of electro-thermal variations in parallel connected devices on the maximum sustainable avalanche energies sustainable without failure will be investigated. Specifically, the impact of different initial junction temperatures (which result from different thermal resistances) and the impact of different switching rates set by different gate resistances will be investigated.

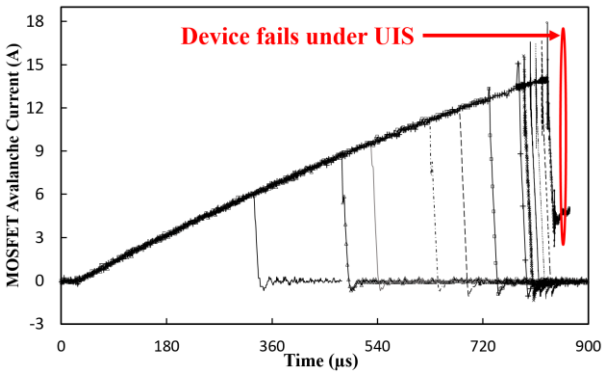

Fig. 2(a). UIS measurements of a 1.2kV/10A SiC MOSFET drain-source currents during the inductor charging and avalanche phases with different gate pulse durations.

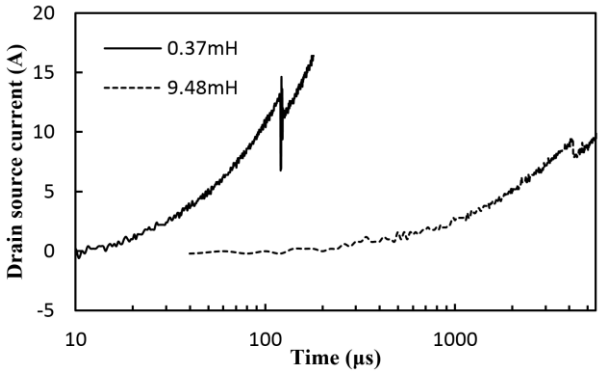

Fig. 2(b). The peak avalanche current characteristics of a SiC MOSFET for 2 different inductor sizes.

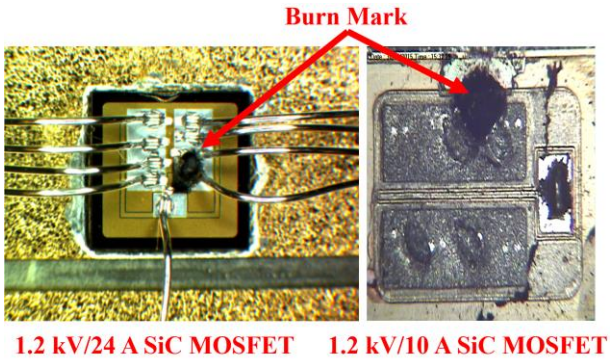

Fig. 2(c). Picture of the de-capsulated SiC MOSFETs showing burn mark resulting from failure under UIS.

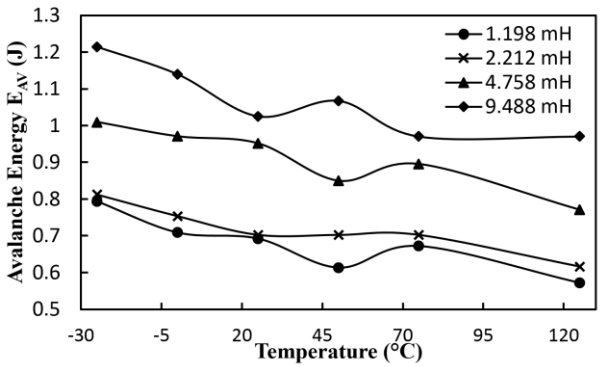

Fig. 2(d). The measured maximum sustainable avalanche energy before failure under UIS for different inductors as a function of temperatures. The device tested was a 1.2kV/24A SiC power MOSFET.

A. Impact of Temperature Difference between the DUTs on Avalanche Ruggedness

The junction temperature of the DUT is determined by using an electric hot-plate shown in Fig. 1(b) which is set individually for each DUT. Fig. 3(a) shows the experimental measurements performed with DUT1 and DUT2 with initial junction temperatures of 25 ^{0}C and 50 ^{0}C respectively where it can be seen that DUT1 fails under UIS induced latch-up while DUT2 does not. These measurements were repeated to ensure statistical integrity of the analysis. The reason for this is twofold. First, the DUT with the lower junction temperature conducts more current during the inductor charging phase which is due to lower on-state resistance [19]. This can be seen in Fig. 3(a) where the DUT with the lower junction

temperature has a higher current slope (dI_{DS}/dt) because of the lower on-state resistance. Secondly, the higher junction temperature in DUT2 means the device has a higher breakdown voltage. Breakdown voltage increases with temperature as a result of the reduced carrier mean free path from increased phonon scattering delaying the on-set of impact ionization. Hence, the bulk of the avalanche current flows through DUT1 because it has a lower breakdown voltage thereby resulting in failure under UIS in DUT1. The measurement was repeated for a range of temperature differences between the DUTs and it was seen that the DUT with the lower junction temperature always failed. Fig. 3(b) shows the peak avalanche current successfully dissipated as a function of the temperature difference between DUT1 and DUT2. These measurements have been performed with 3 different avalanche durations which have been set by 3 different inductors (1, 2 and 3 mH). It can be seen from Fig. 3(b) that the peak avalanche current sustainable by the device decreases as the avalanche duration (inductor) increases as expected. It can also be seen that the maximum combined avalanche currents of both DUTs marginally reduce as the temperature difference between the DUTs increases. This is due to increased current crowding in the lower temperature DUT as the temperature difference rises. Fig. 3(c) shows the maximum measured avalanche energy successfully dissipated by the DUTs before failure under UIS for the 3 avalanche durations. It can be seen from Fig. 3(c) that the energy is higher when the avalanche duration is increased since the DUTs sustain the highest avalanche energies for the case of the 3 mH inductor. This implies that the mismatch in junction temperature is more detrimental to the overall avalanche ruggedness of the parallel connected devices when the UIS event occurs with high current and low inductance.

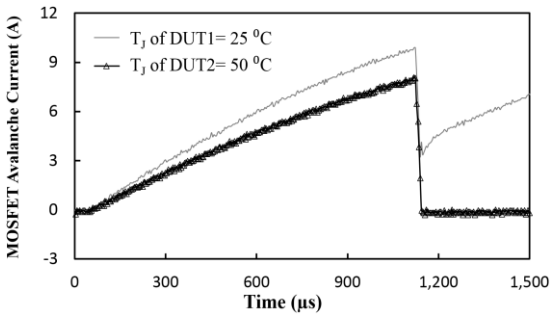

Fig. 3(a). The measured inductor charging and avalanche characteristics for the DUTs with different initial junction temperatures.

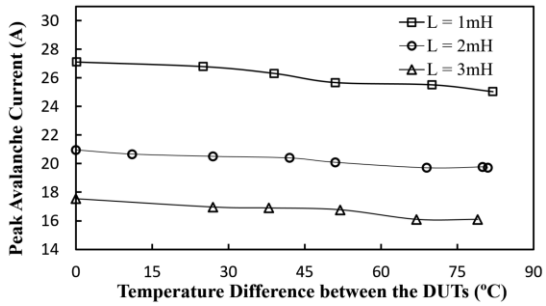

Fig. 3(b). The measured peak avalanche currents conducted by the DUTs as a function of the temperature difference between the DUTs for 3 avalanche durations (inductance sizes).

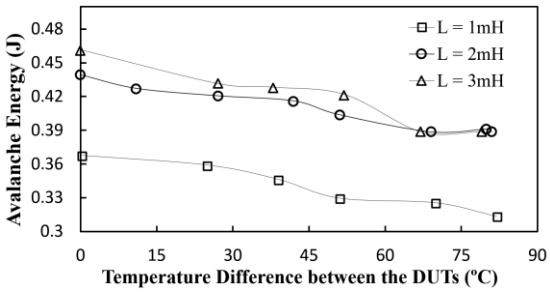

Fig. 3 (c). The measured avalanche energy successfully dissipated by the combined DUTs as a function of the temperature difference between the DUTs for 3 avalanche durations (inductor sizes).

This is expected since failure under UIS is triggered by current crowding which is aggravated by higher current densities.

B. Impact of Variation in Switching Rates between the DUTs on Avalanche Ruggedness

The switching rate of the DUTs is set by simply changing the gate resistances. Fig. 4(a) shows the measurement results for the UIS experiments with DUT1 switched with a smaller gate resistance than DUT2. It can be seen that DUT2, which is the slower switching device, fails while DUT1 does not. The test has been repeated for different combination of gate resistances and on all occasions the slower switching device fails under UIS while the faster switching device does not. The reason for this, as subsequent finite element models will show, is that the slower switching device is more conductive during UIS since there is a residual channel due to the slower turn-off transient. Since the DUT with the larger gate resistance (lower dI_{DS}/dt) switches off more slowly, the channel is more conductive, thereby exacerbating current crowding within the device. Fig. 4(b) shows the peak combined avalanche current for both DUTs (before the failure of either under UIS) as a function of the difference between the gate resistances between the DUTs. The measurements in Fig. 4(b) have been performed for 3 different avalanche durations i.e. 3 different inductors namely 1, 2 and 3 mH. It can be seen from Fig. 4(b) that the peak combined avalanche current of both DUTs before failure decreases as the difference between the gate resistances of DUT1 and DUT2 increases. This is expected since further increment in the difference between the switching rates of the DUTs will exacerbate current crowding in the slower switching DUT. Fig. 4(c) shows the measured maximum avalanche energy successfully dissipated in both DUTs as a function of the difference between the gate resistances (and dI_{DS}/dt) in the DUTs. Again, the measurements have been performed with different inductors (1, 2 and 3 mH) to investigate the impact of avalanche duration on the reliability of the DUTs switching with different rates. It can be seen from Fig. 4(c) that the avalanche energy sustainable by the combined DUTs increases with the avalanche duration for a given mismatch in the switching rate. In other words, differences in the switching rates of parallel connected DUTs degrades the overall avalanche ruggedness of the device faster for high current low inductance UIS pulses compared with low current high inductance UIS pulses. Hence, similar to the case of variation of junction temperatures between the DUTs, the effect is exacerbated by higher current densities.

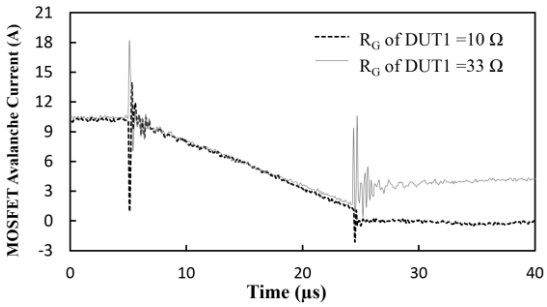

Fig. 4(a). The measured inductor charging and avalanche characteristics is shown for the parallel connected DUTs with different switching rates.

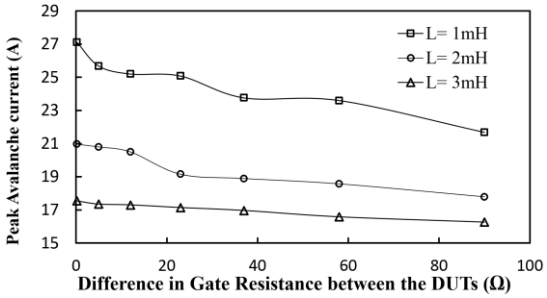

Fig. 4(b). The measured peak combined avalanche currents conducted by the DUTs as a function of the switching rate difference between the DUTs for 3 avalanche durations (inductance sizes).

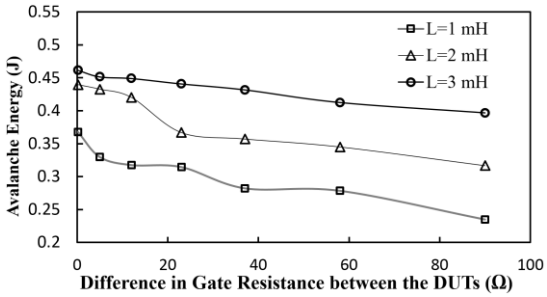

Fig. 4(c). The measured avalanche energy safely dissipated by the combined DUTs as a function of the switching rate difference between the DUTs for 3 avalanche durations (inductor sizes).

III. Finite Element Simulations

The circuit shown in Fig. 1(a) has been simulated in ATLAS from SILVACO using the mixed mode circuit application to solve the switching transients with the finite element model. The finite element models have been performed on SiC power MOSFETs under avalanche mode conduction so as to gain a deeper insight into the physics of device failure with 2 parallel devices. The model included lattice-heating and impact ionization together with the continuity/Poisson equations for carrier transport. The drift layer doping and thickness was optimized to achieve the desired breakdown voltage in SiC. To correctly model the on-state current, Shockley-Read-Hall (SRH) recombination was used together with concentration dependent mobility for the electrons in the MOSFET channel. A p-body doping of 1×10^{18} cm^{-3} was used in combination with a 1×10^{19} cm^{-3} p+ doping for the body diode shorting the source to the body. The source and drain regions were degenerately doped with n+ and an oxide thickness of 50 nm was used for the gate dielectric. The thickness and doping of the voltage blocking drift layer in the device was set to achieve a breakdown voltage of 1.5 kV. A drain current density of 60 A/cm^2 was achieved in the simulation based on the simulated active area. Firstly, electro-thermally identical MOSFFETs have been simulated in order to understand the internal physics of the device under ideal conditions. The results are shown in Fig. 5(a) where the inductor charging and avalanche characteristics of the device are shown. Fig. 5(b) shows the 2-dimensional current density contour plots of the identical devices at point A corresponding to Fig. 5(a). At this point, the MOSFETs conduct normally through the channel under drift-diffusion mechanisms. It can be seen that the highest current densities occur in the source, channel and drain regions of the device as expected. Fig. 5(c) shows the 2-dimensional current density contour plots of the identical devices at point B corresponding to Fig. 5(a). At this point, the devices have been switched off and the inductor dissipates the current stored in its magnetic field through the devices which are conducting in avalanche.

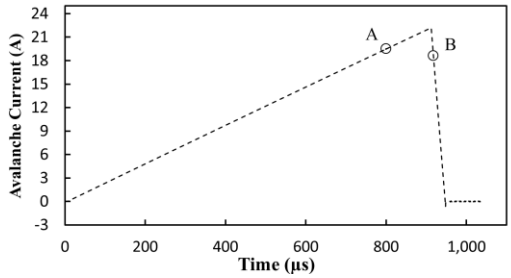

Fig. 5(a). The modeled avalanche current characteristics of 2 parallel connected DUTs with identical electro-thermal parameters under UIS.

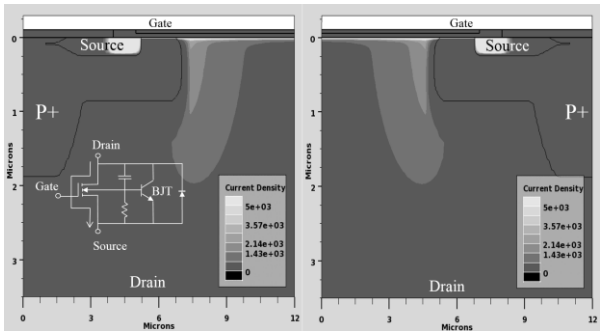

Fig. 5(b). The modeled 2D current density contour plots of the parallel connected DUTs at point A corresponding to Fig. 5(a).

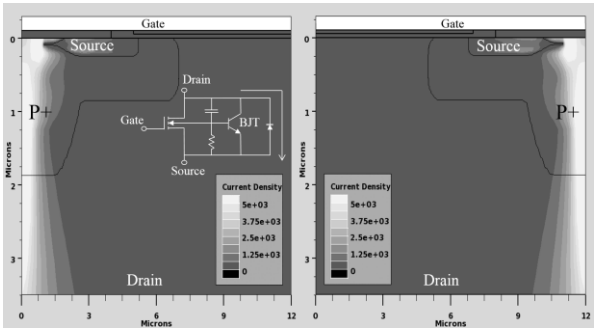

Fig. 5(c). The modeled 2D current density contour plots of the parallel connected DUTs at point B corresponding to Fig. 5(a).

It can be seen from the current density contour plots in Fig. 5(c) that the peak avalanche flowing through the device is not

through the channel but through the reverse biased body diode comprised of the deep P+ body and the drain. This is how a power device reliably conducts current through the body diode and not through the internal npn BJT. Subsequent 2D current density plots obtained from the simulator for devices that have failed under UIS will show high current densities through the npn BJT thereby indicating latch-up.

A. Finite Element Simulations of the Impact of Different Junction Temperatures

Similar to the experiments, the impact of different initial junction temperatures has been investigated. The results are shown in Fig. 6(a), where the transient UIS characteristics are shown for devices with the same and with different initial junction temperatures. It can be seen from Fig. 6(a) that the devices with $T_{J1}=T_{J2}$ pass the test while those with $T_{J1}\neq T_{J2}$ fail. Fig. 6(b) to 6(e) show the 2D current density contour plots in the device corresponding to points W to Z respectively in Fig. 6 (a). Fig. 6(b) shows the 2D plot at point W when both channels are conducting normally. On closer inspection, it can be seen that the lower temperature device on the LHS has a slightly higher current density because the reduced on-state resistance. Fig. 6(c) shows the current density plot corresponding to point X where it can be seen that both devices go safely into avalanche by conducting the current through the body diode. Fig. 6(d) corresponds to the point Y in Fig. 6(a) where the DUT with the lower junction temperature is going into thermal runaway due to BJT latch-up. It can be seen that the current is moving away from the antiparallel body diode towards the intrinsic npn BJT. At this point, the current through the antiparallel body diode of the device simulated with the higher junction temperature is diminishing because the device simulated with the lower junction temperature is taking all of the current. Fig. 6(e) shows the lower temperature device on the LHS in full BJT latch-up while the higher temperature device stops taking any current. These plots fully explain and agree with the experimental measurements shown in Fig. 3. The breakdown voltage of the simulated device shows a positive temperature coefficient. Since avalanche current always flows through the device with the smallest breakdown voltage, the bulk of the avalanche current flows through the device simulated with the lower junction temperature. Using the simulations, it was also confirmed that increasing the difference between the junction temperatures of the parallel connected devices reduces the total avalanche current the devices can sustain without the cooler device initiating BJT latch-up.

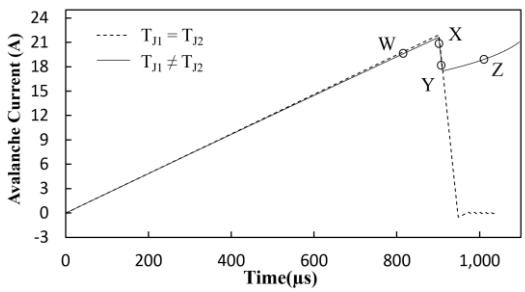

Fig. 6(a). The modeled UIS characteristics of 2 parallel connected DUTs at identical and different initial junction temperatures.

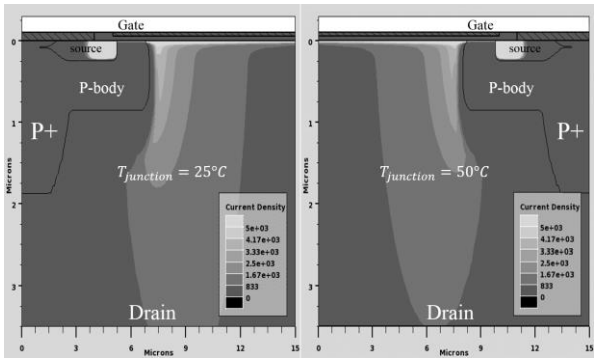

Fig. 6(b). The 2D current density contour plots for devices with different initial junction temperatures at point W corresponding to Fig. 6(a).

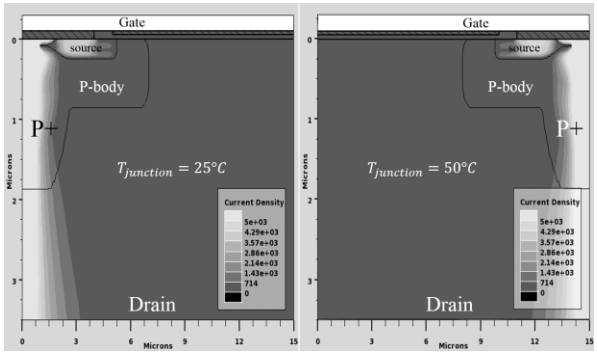

Fig. 6(c). The 2D current density contour plots for devices with different initial junction temperatures at point X corresponding to Fig. 6(a).

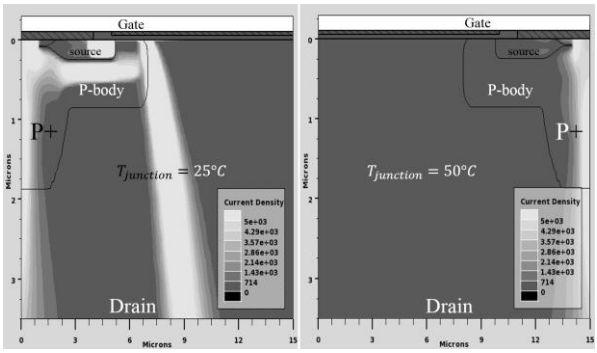

Fig. 6(d). The 2D current density contour plots for devices with different initial junction temperatures at point Y corresponding to Fig. 6(a).

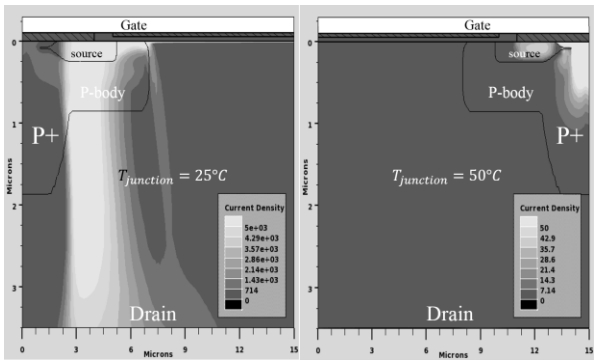

Fig. 6(e). The 2D current density contour plots for devices with different initial junction temperatures at point Z corresponding to Fig. 6(a).

B. Finite Element Simulations of the Impact of Different Switching Rates

Similar simulations have been performed to investigate the impact of different switching rates on parallel connected DUTs under UIS. Fig. 7(a) shows the simulated UIS characteristics for parallel connected SiC MOSFETs switched at different rates with different gate resistances. It can be seen in Fig. 7(a) that similar to the experimental measurements presented earlier, the devices simulated with R_{G1}=R_{G2} successfully dissipate the avalanche current while the devices with R_{G1}≠R_{G2} undergo thermal runaway during UIS. Fig. 7(b) shows the 2-D current density contour plots in the simulated devices at point X where it can be seen that both devices conduct current normally. The devices share the current equally during the steady state since differences in the switching time will cause differences only during switching transients. Fig. 7(c) shows the 2-D current density contour plots of the simulated devices at point Y during avalanche mode conduction after the devices have been switched off. It can be seen in Fig. 7(c) that the slower switching device exhibits a considerably high current density through the npn BJT as well as through the body diode. Because the device switches slower, the channel is still conductive at the point that the avalanche current starts to flow, hence, the significant current density through the p-body under the source. The faster switching device with the lower gate resistance conducts the avalanche current normally through the antiparallel body diode. Fig. 7(d) shows the 2-D current density contour plots at point Z corresponding to Fig. 7(a) where full BJT latch-up is evident in the slower switching device (on the RHS) with the higher gate resistance. The faster switching device does not conduct any current since thermal runaway in the slower switching device has diverted the entire avalanche current away. These simulations correspond to and very well explain the experimental measurements presented in Fig. 4 where the slower switching device failed during the UIS test.

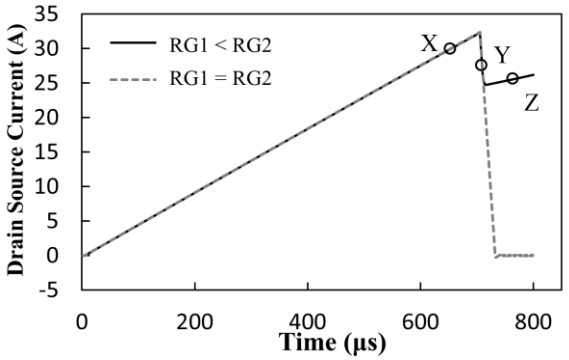

Fig. 7(a). Modeled UIS characteristics of 2 parallel connected DUTs at the same and different switching rates.

IV. CLAMPED INDUCTIVE SWITCHING MEASUREMENTS

Most power electronic converters operate under clamped inductive switching conditions where a high side anti-parallel diode exists for reverse conducting capability. Hence, the impact of electro-thermal variations on the operating conditions of the devices has been studied with the devices switching repetitively at high frequencies under clamped conditions. The switching frequency is set at 2 KHz with a duty cycle of 10%. The experimental test rig presented in Fig. 1(a) was used, with the only modification being the inclusion of a reverse conducting 1.2 kV SiC Schottky diode in parallel with the inductor for free-wheeling the current. The case temperatures were measured under steady-state conditions for each of the parallel connected devices. Differences in switching rates were set by using different gate resistances, while differences in the thermal resistance were set by using different heat sinks. Fig. 8(a) shows the turn-on waveforms of the individual DUTs, with DUT1 and DUT2 switched with R_G=10 Ω and R_G=33 Ω respectively. Fig. 8(b) shows the turn-

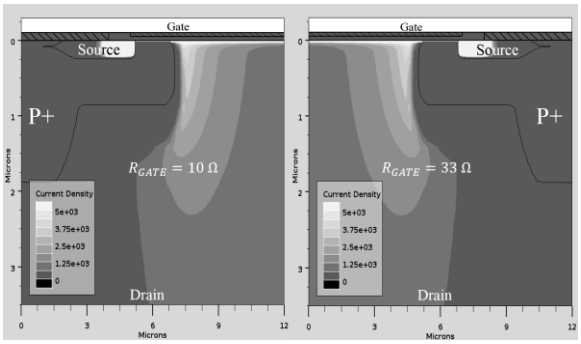

Fig. 7(b). Modeled 2D current density contour plots for the parallel connected devices with different switching rates at point X corresponding to Fig. 7(a).

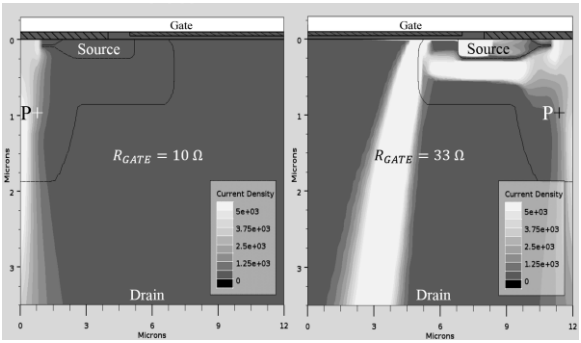

Fig. 7(c). Modeled 2D current density contour plots for the parallel connected devices with different switching rates at point Y corresponding to Fig. 7(a).

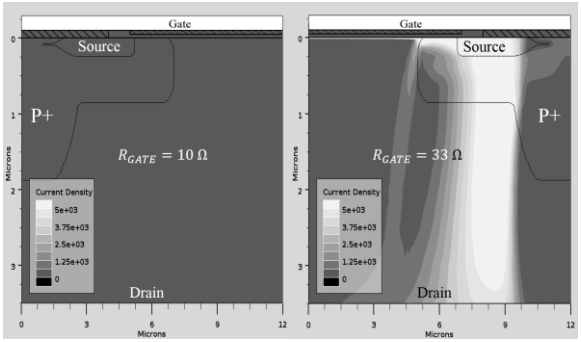

Fig. 7(d). Modeled 2D current density contour plots for the parallel connected devices with different switching rates at point Z corresponding to Fig. 7(a).

off waveforms. It can be seen from Fig. 8(b), that there is significant current overshoot in the slower switching device which results from the current initially flowing through the faster switching device being diverted to the former subsequent to the faster turn-off of the latter. These high current spikes contribute to higher steady-state temperature rise in the slower switching device.

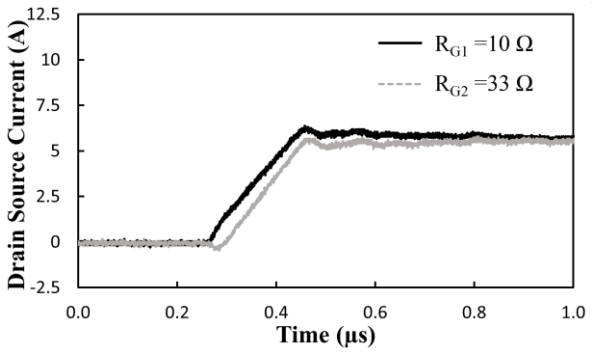

Fig. 8(a). Measured drain-source current turn-on transients for parallel connected DUTs under clamped inductive switching.

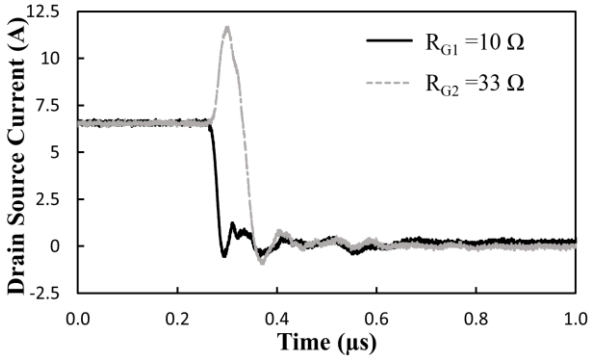

Fig. 8(b). Measured drain-source current turn-off transients for parallel connected DUTs under clamped inductive switching.

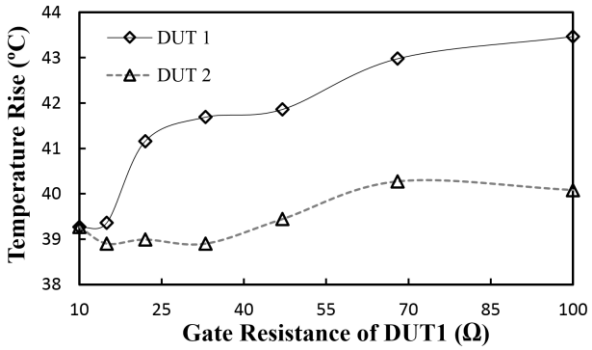

Fig. 9. The measured junction temperatures of the parallel connected DUTs under clamped inductive switching with different switching rates. The R_G of DUT2 is held constant at 10 Ω and R_G of DUT1 is varied.

Fig. 9 shows the measured steady state case temperature rise of both DUTs while switching with the gate resistance of DUT2 held constant at 10 Ω and the gate resistance of DUT1 varied. It can be seen from Fig. 9 that mismatch in the switching rate causes a significant temperature variation between the devices due to the slower switching device experiencing significant current overshoots during turn-off.

V. CONCLUSION

In this paper, both experimental measurements and simulations have been used to reach the following conclusions about parallel connected SiC MOSFETs conducting under avalanche mode conditions in UIS

i) SiC MOSFETs can dissipate higher avalanche energies in the form of lower peak avalanche currents over longer avalanche durations compared to higher peak avalanche currents over shorter durations

ii) Differences in the initial junction temperature reduce the overall maximum avalanche energy the combined devices can conduct without failure in either device. A junction temperature difference of 85°C between the DUTs causes the maximum sustainable avalanche current to reduce by 10% while a gate resistance difference of 90 Ω causes the maximum sustainable avalanche current to reduce by 14%.

iii) The device with the lower initial junction temperature fails under UIS while the device with the higher initial junction temperature does not. This is primarily due to the positive temperature coefficient of the breakdown voltage.

iv) The device switching with the higher gate resistance (lower d_{IDS}/dt) fails because the channel is more conductive during UIS compared to the device switching with the lower gate resistance (higher d_{IDS}/dt).

v) The impact of different junction temperatures and switching rates on the overall avalanche ruggedness of the parallel connected devices is less effective when the avalanche energy is dissipated in the form of a lower peak current over a longer avalanche duration.

vi) Under clamped inductive switching conditions, the slower switching device operates at a higher junction temperature.

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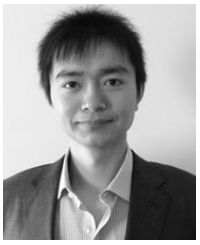

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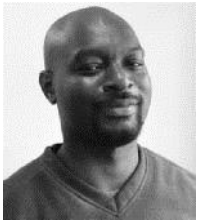

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