Strategies for the Improvement of Critical Infrastructure Resilience to Electromagnetic attacks

European Commission Grant Agreement FP7-SEC-2011-285257

SEVENTH FRAMEWORK PROGRAMME

IEMI Detection Systems:
A low cost IEMI detector

J F Dawson, L Dawson, I D Flintoft, L Rebers,
Michael Camp, Juergen Schmitz, Markus Jung

EMC Europe 2015, Dresden
Workshop 26, Paper 6a

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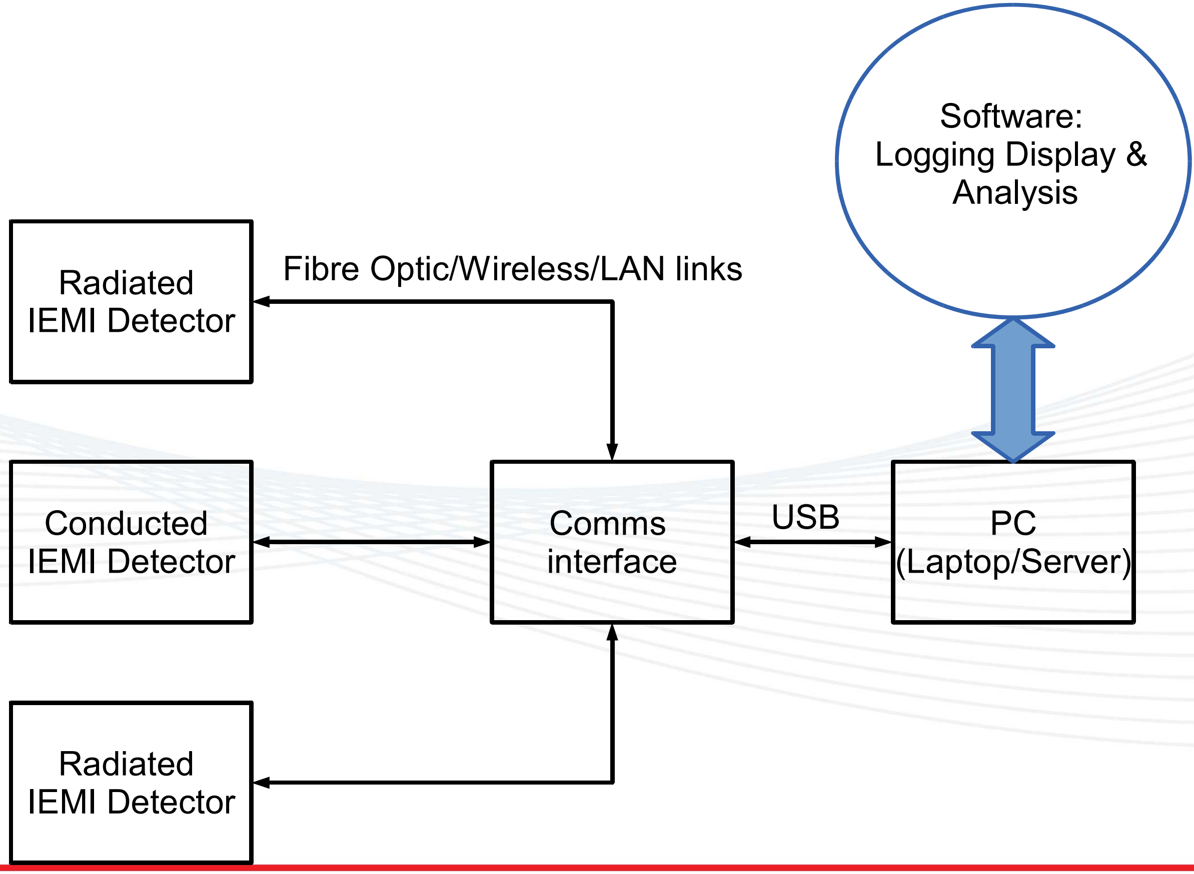
System Concept



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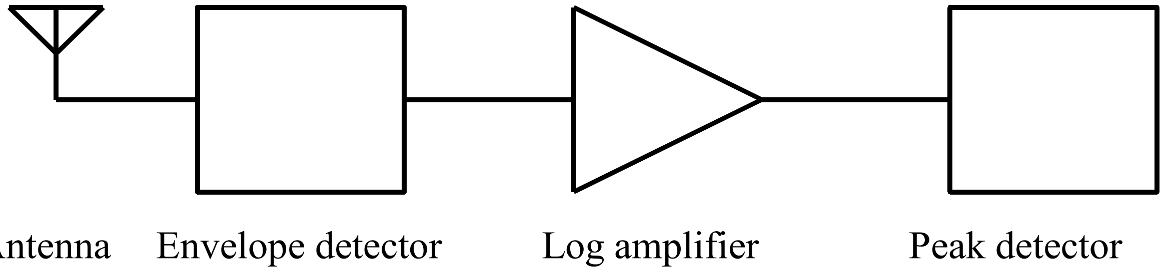
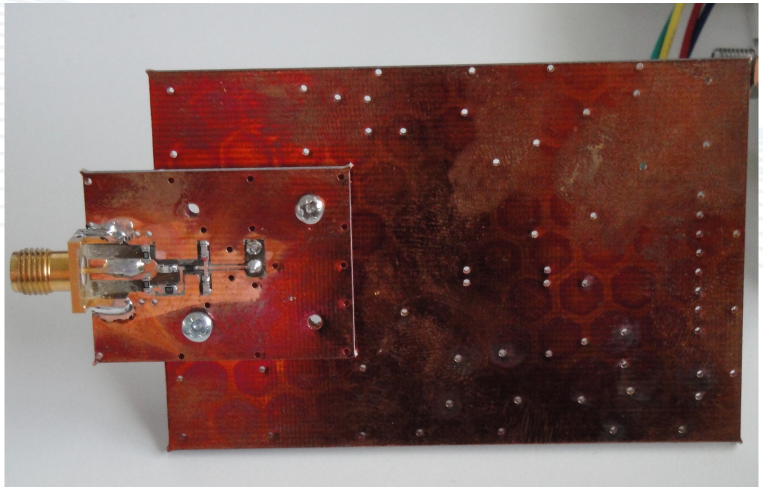
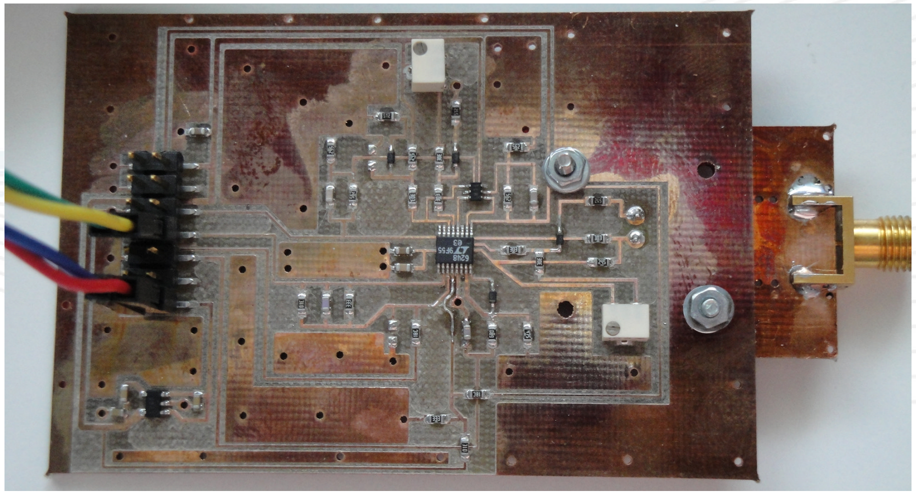
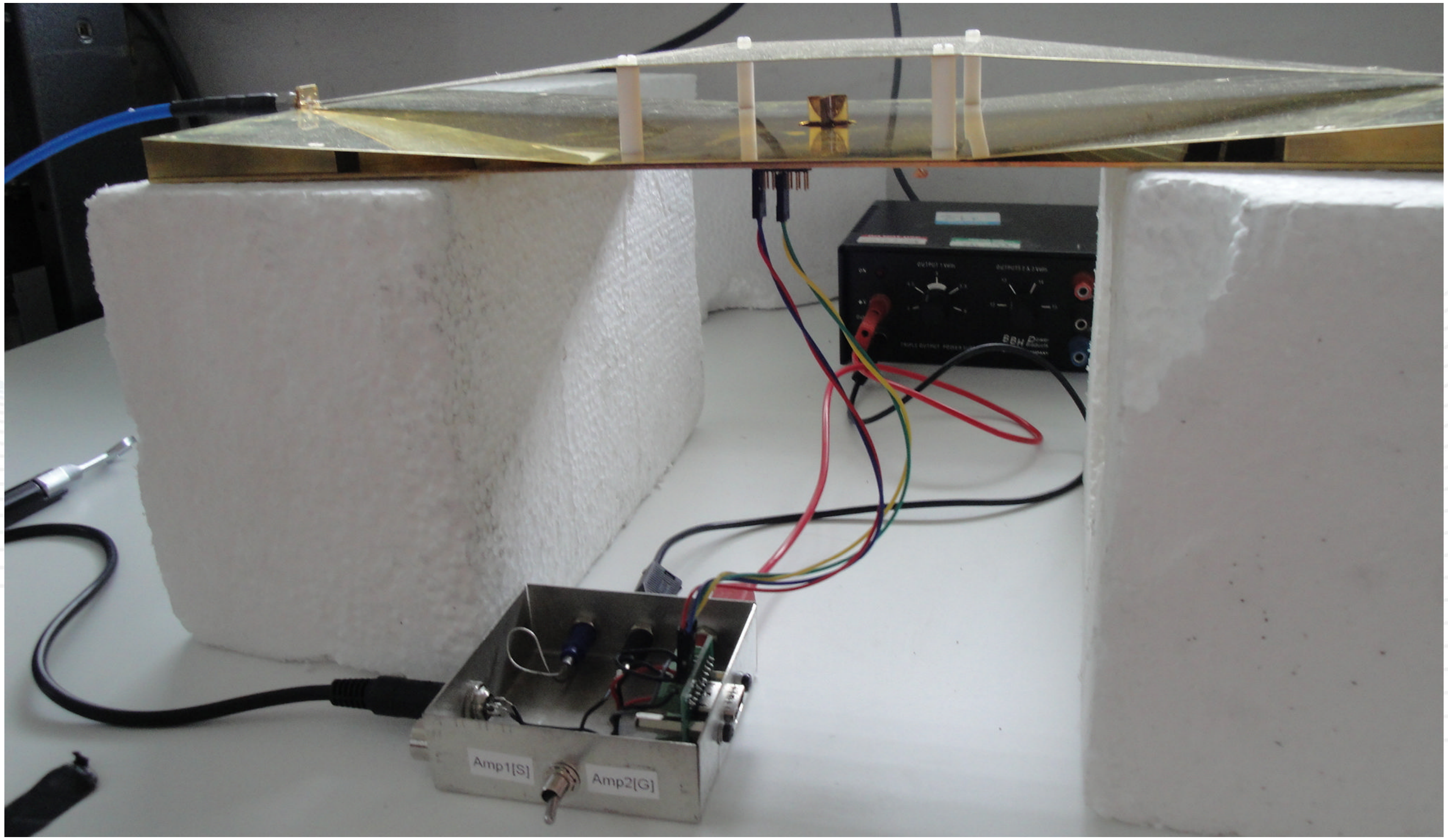
Radiated IEMI Sensor



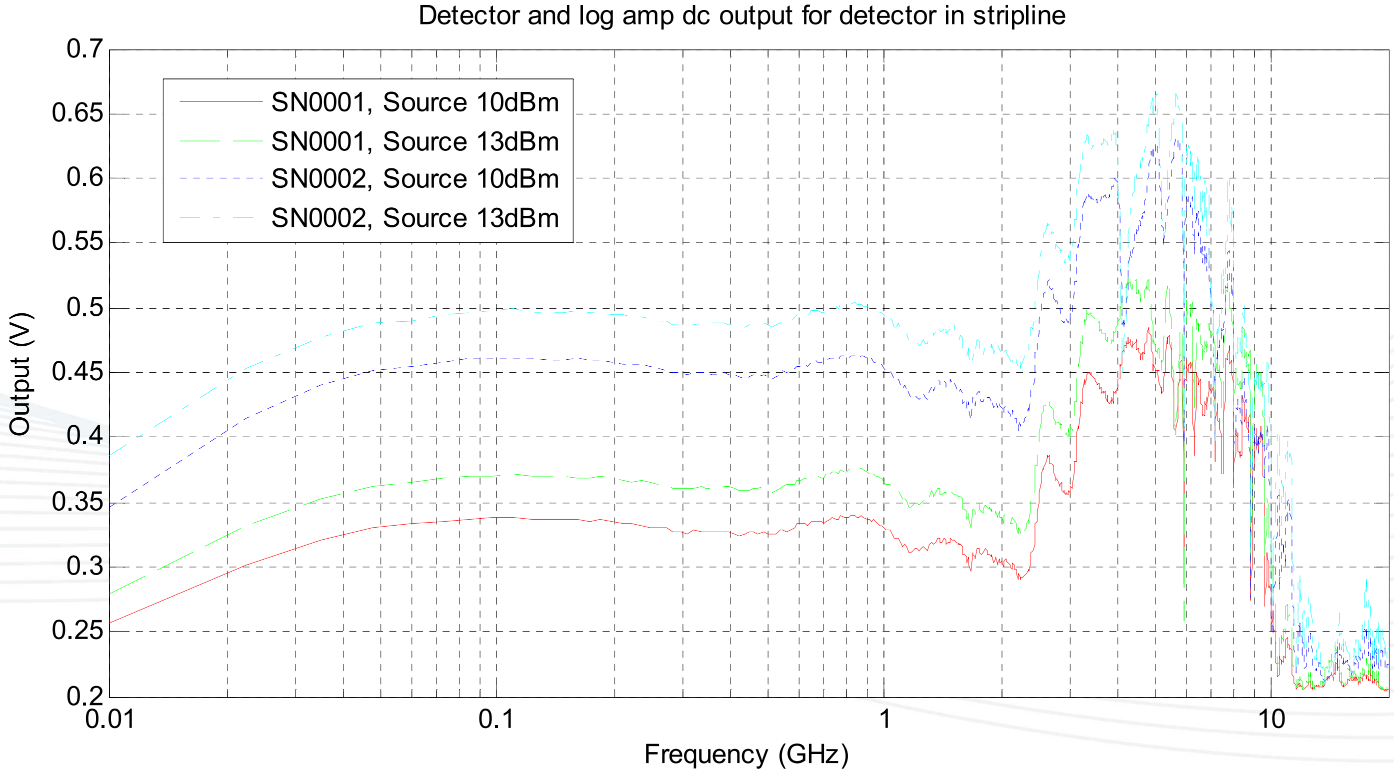




Sensor in 25mm Stripline



Sensor Frequency Response



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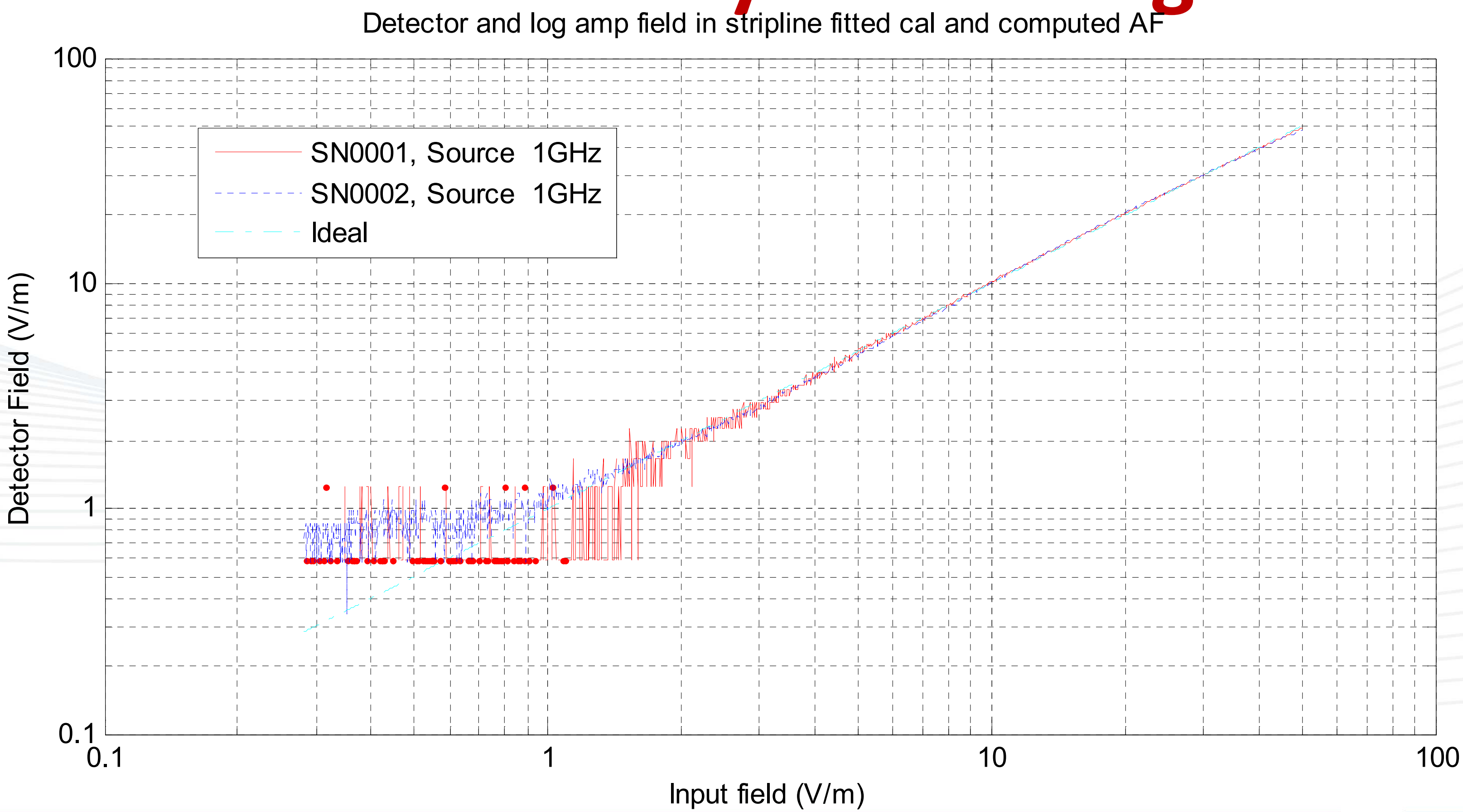
Sensor CW Dynamic range



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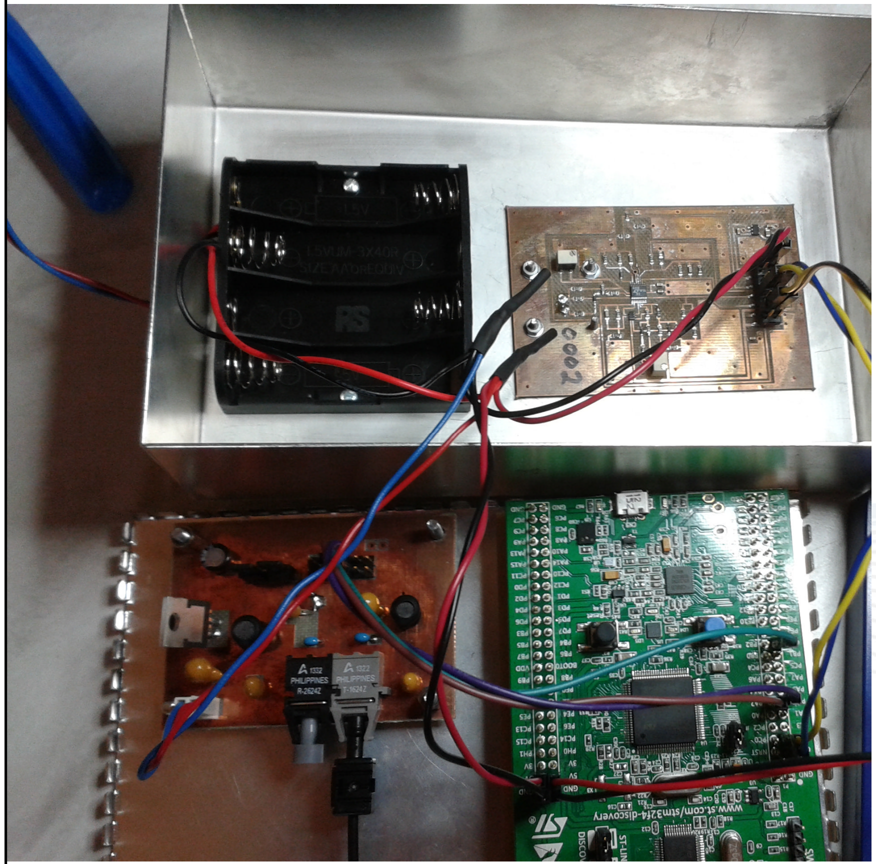
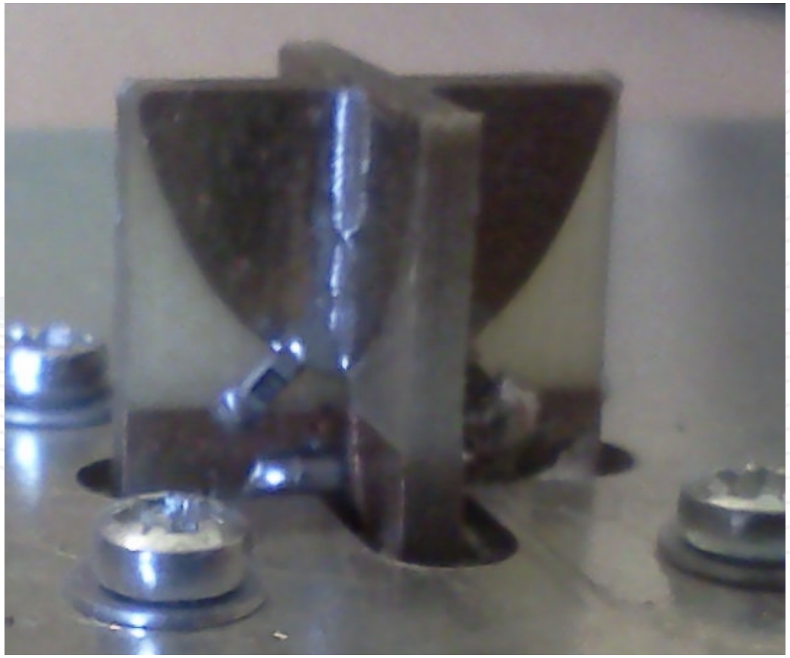
Detector Assembly



Prototype detector, microcontroller, optical link, and batteries in shielded enclosure

Antenna close up



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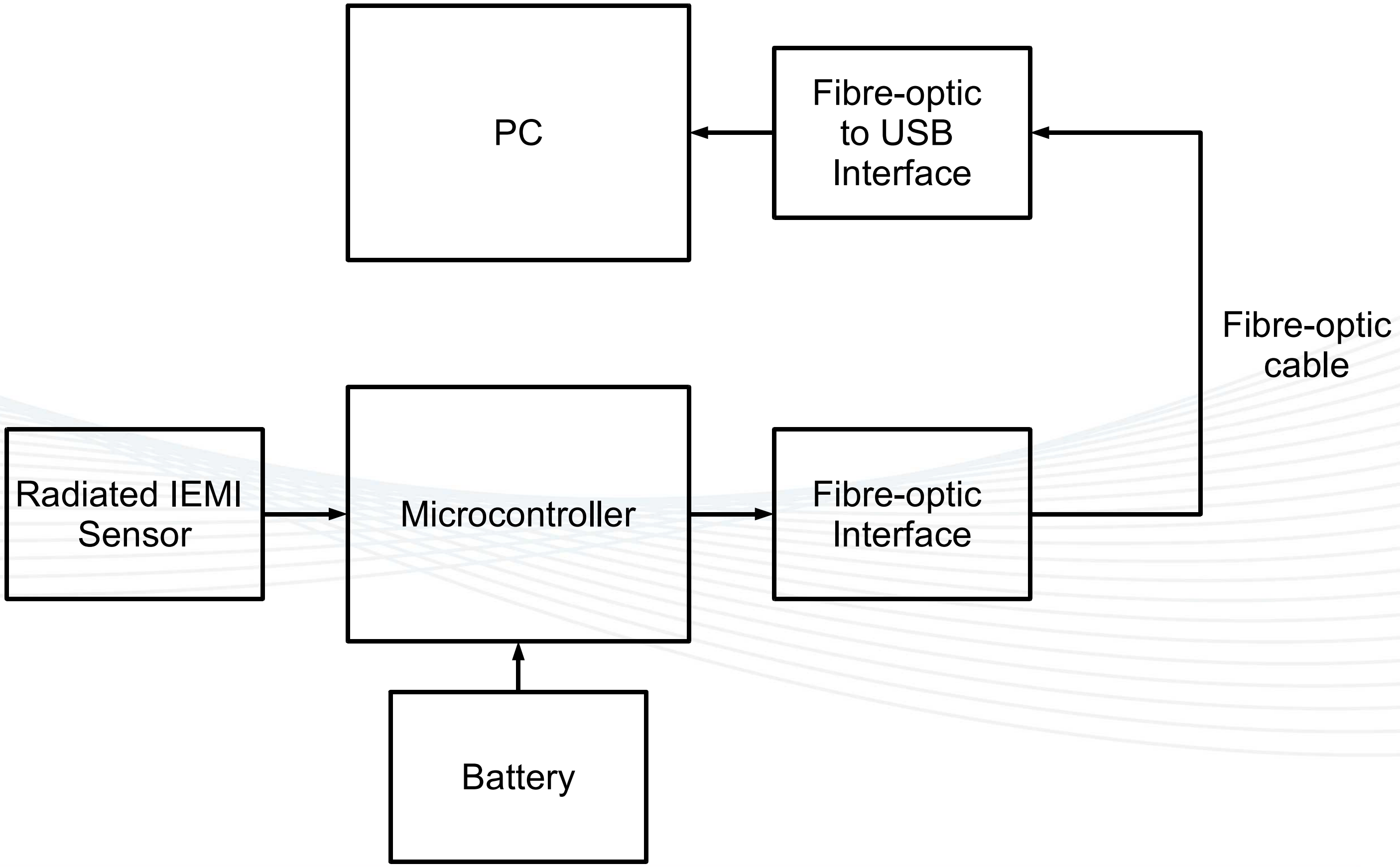
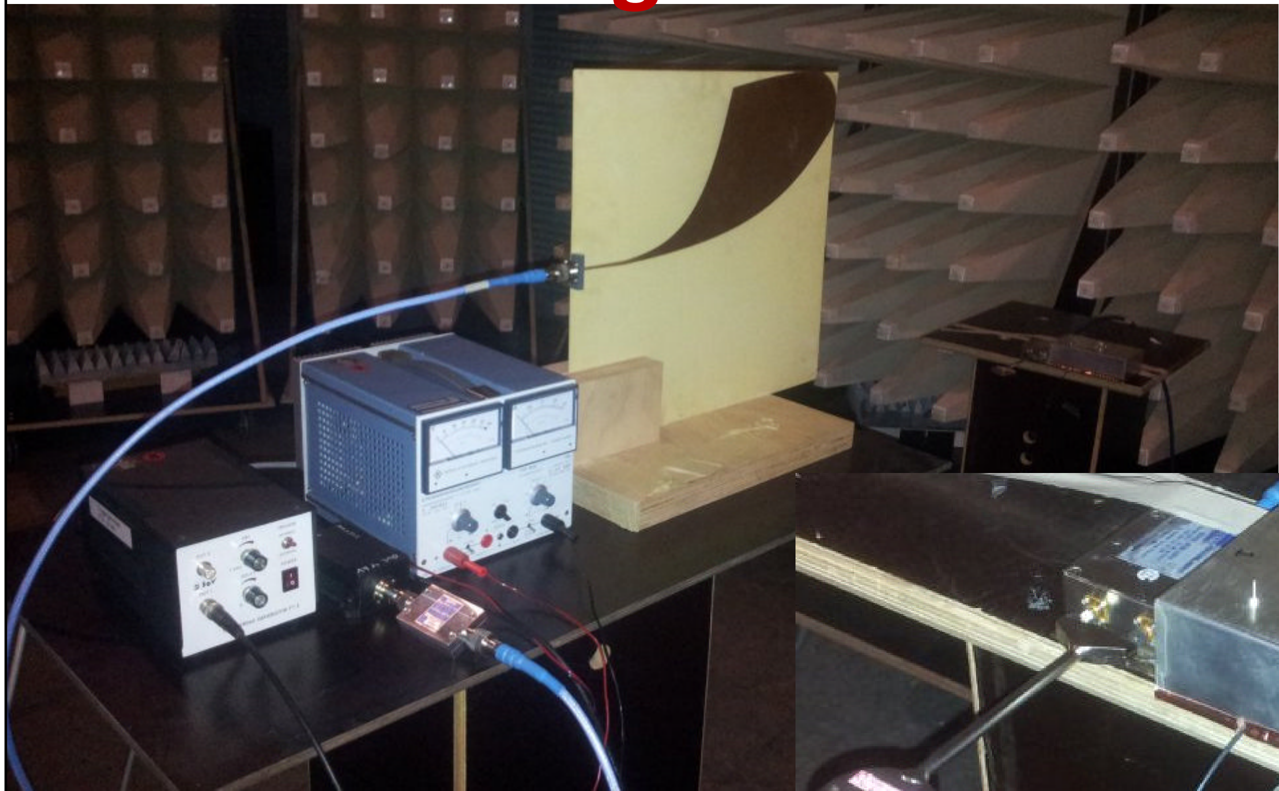
High Field Tests at RMW



High Field Tests



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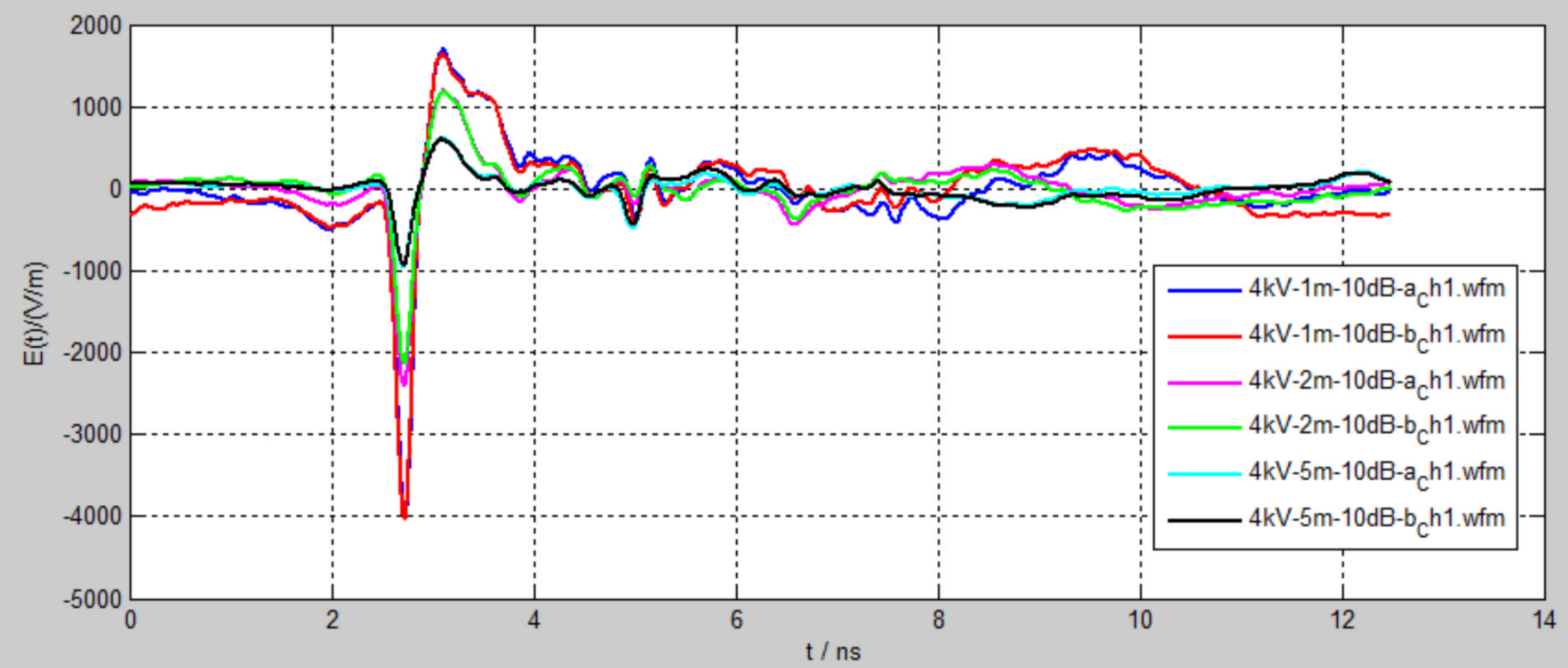
Integrated D-dot probe output



Tests at Rheinmetall from double exponential pulse generator

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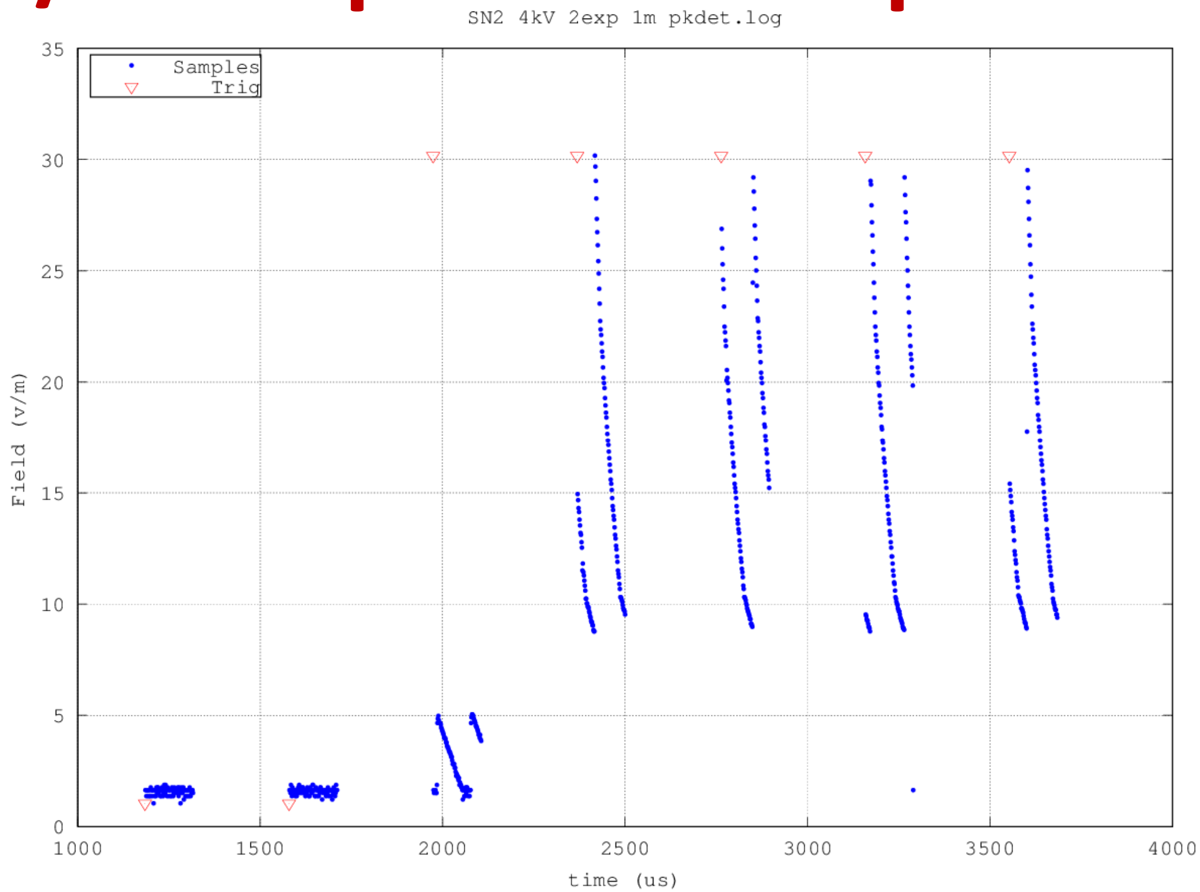
4kV/m 250ps double Exponential



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Low cost detector Status

- Useable Radiated detector up to 6~GHz
- Frequency response flat to 2GHz
  - Sensitive 2V/m to > 4kV/m
- Partial response to short pulses
  - Sensitive 200V/m to > 4kV/m for 250ps pulse
- Potential for low power operation
  - could be solar powered
- A conducted IEMI detector has also been designed using the same hardware

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SEVENTH FRAMEWORK PROGRAMME

IEMI Detection Systems:

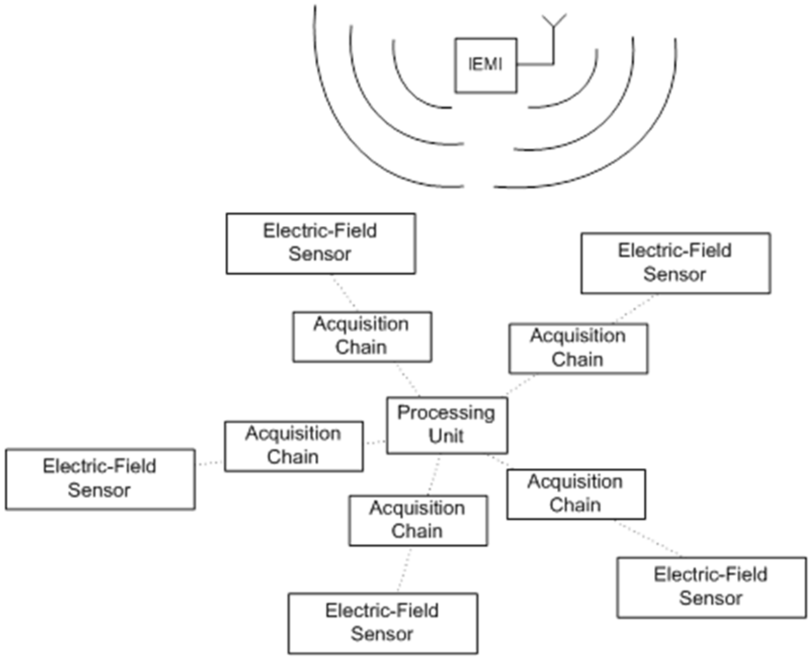
A system for sensing, localization and identification of IEMI attacks

Werner Hirschi, Mirjana Stojilović, Marcos Rubenstein, Benjamin Menssen, Heyno Garbe

EMC Europe 2015, Dresden
Workshop 26, Paper 6b

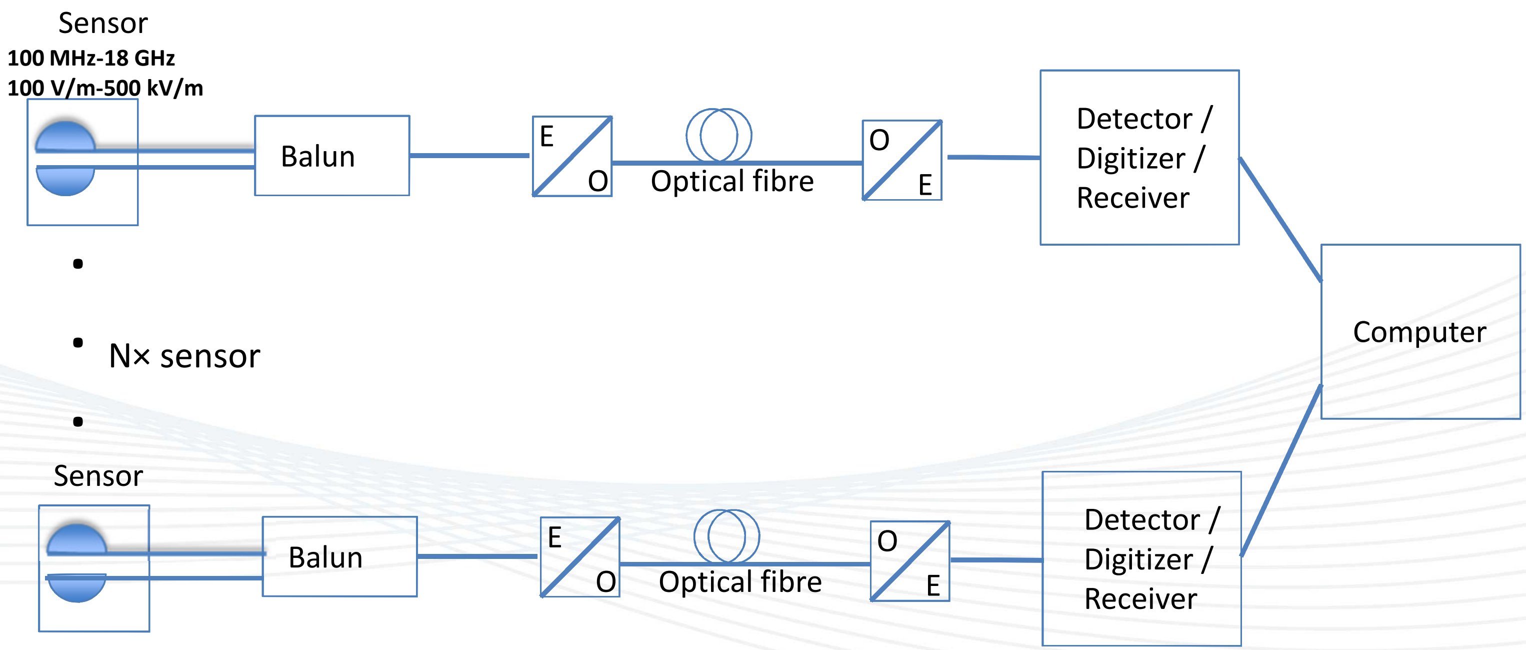
Overall Architecture

- Localization by the time difference of arrival method
- Identification of IEMI sources by analysis of the received waveforms



Overall architecture for identification and localization system for IEMI sources

Ideal architecture



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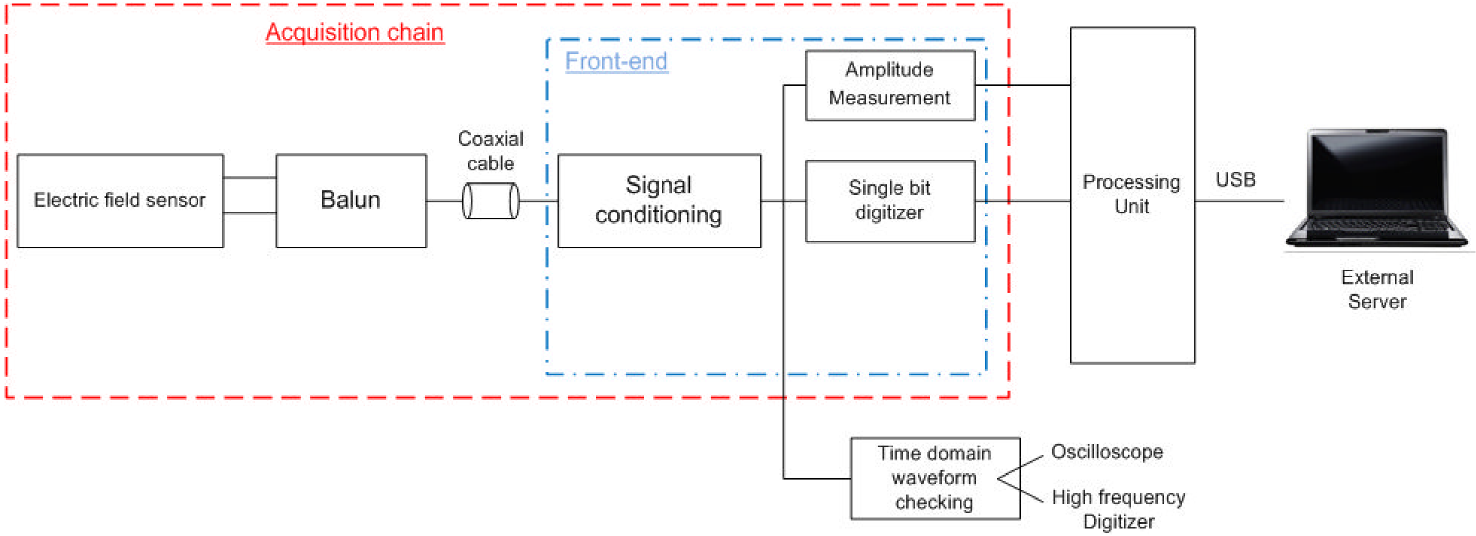
Block Diagram for one sensor

- Electric-field sensor
- Signal Conditioning
- Amplitude Measurement
- Single bit digitizer
- Time domain waveform checking
- Processing unit
- External server

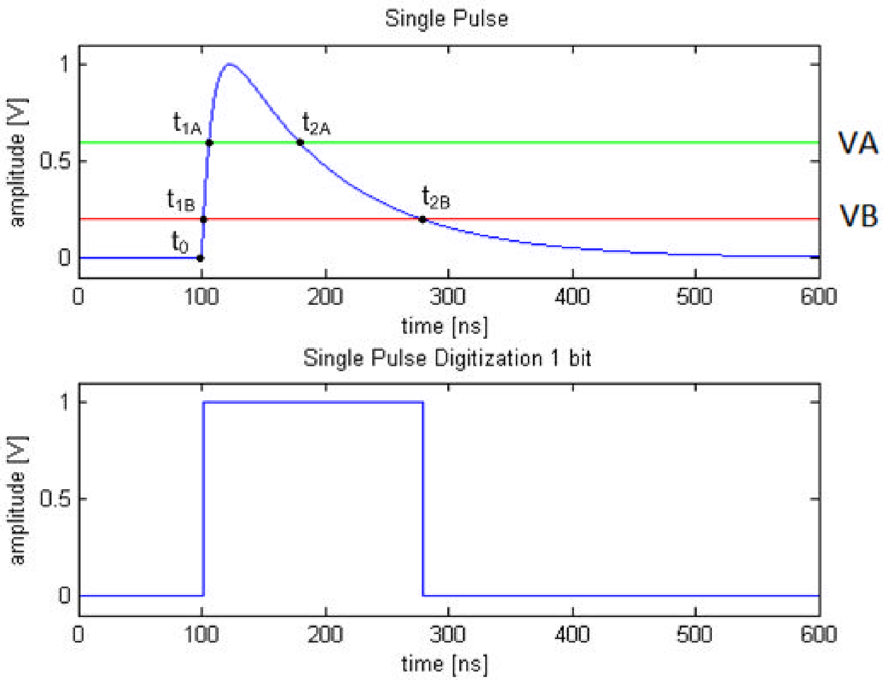


Block diagram for one sensor

Estimations of waveform parameters

Single pulse double exponential

- Estimating time constants
  - From timing two threshold crossings we can obtain the two time constants



$$V_A \cong V_0 e^{-t'_{2A}/\tau_1} \qquad V_B \cong V_0 e^{-t'_{2B}/\tau_1}$$

$$V_A / V_B \cong e^{(-t'_{2A} + t'_{2B})/\tau_1}$$

$$\tau_1 \cong (t'_{2B} - t'_{2A}) / \ln(V_A / V_B)$$

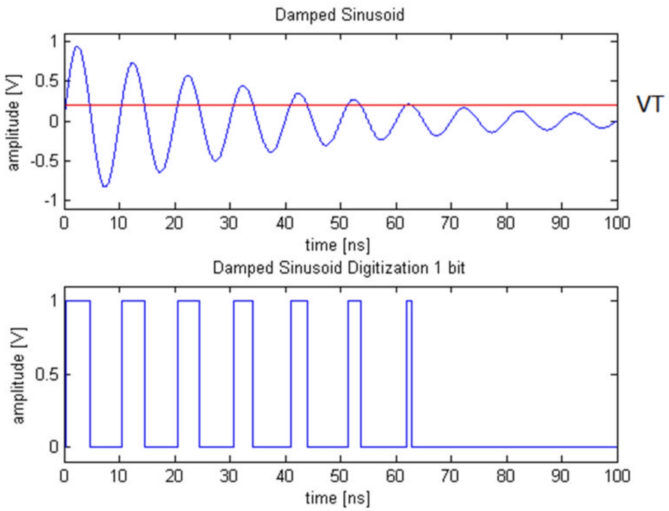
$$V_0 \cong \frac{V_A}{e^{-t'_{2A} \ln\left(\frac{V_A}{V_B}\right) \Big/ (t'_{2B} - t'_{2A})}}$$

$$\tau_2 = -t'_{1A} / \ln\left(e^{-t'_{1A}/\tau_1} - V_A / V_0\right)$$

Estimations of waveform parameters

Damped sinusoid

- Estimating decay time constant and fundamental frequency



Damped sinusoid

$$t_{Start,m} = m/f$$

$$t_{End,m} = (2m-1)/2f$$

$$e^{-t/\tau} \geq V_T$$

$$t \leq -\tau \ln(V_T)$$

$$\frac{2m-1}{2f} \leq -\tau \ln(V_T)$$

$$\tau \geq -\frac{2m-1}{2f \ln(V_T)}$$

$$x(t) = \sin(2\pi f t) e^{-t/\tau}$$

$$\sin(2\pi f t) e^{-t/\tau} = V_T$$

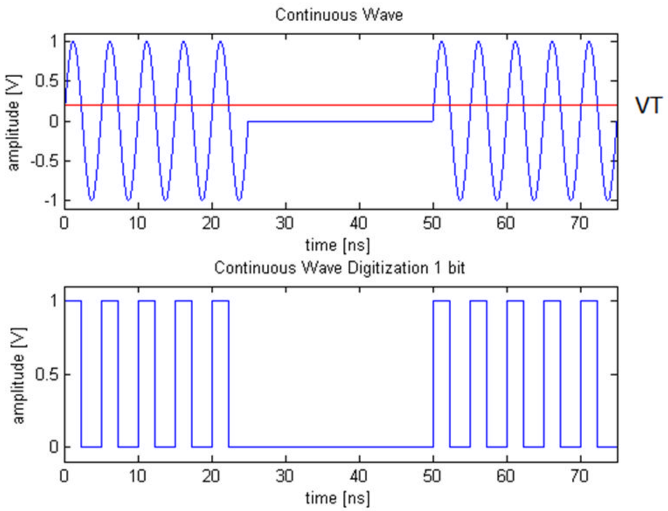
$$f = \frac{n-1}{2\Delta t} \quad \text{if} \quad n > 1$$

$$f \approx \frac{p-1}{2\Delta t_{n,V_T \neq 0}}$$

Estimations of waveform parameters

Continuous wave

- Estimating fundamental frequency



Continuous Wave

$$\Delta t_n = \frac{(n-1)\pi}{2\pi f}$$ If n is odd

$$\Delta t_n = \frac{\pi - 2\arcsin(V_T) + (n-2)\pi}{2\pi f}$$ If n is even

$$f = \frac{n-1}{2\Delta t_n}$$ If n is odd

$$f = \frac{\pi - 2\arcsin(V_T) + (n-2)\pi}{2\pi \Delta t_n}$$ If n is even

Specifications of the demonstrator

- System able to accept large dynamic in amplitude & frequency
  - Amplitude dynamic range : min 100 V/m; max 20 kV/m
  - Frequency dynamic range : a few hundred Hz -> 1 GHz
- Amplitude measurement with fast transition and rise time in case of the pulse signal
  - lowest rise time = 300 ps
  - lowest duration 50% = 1 ns

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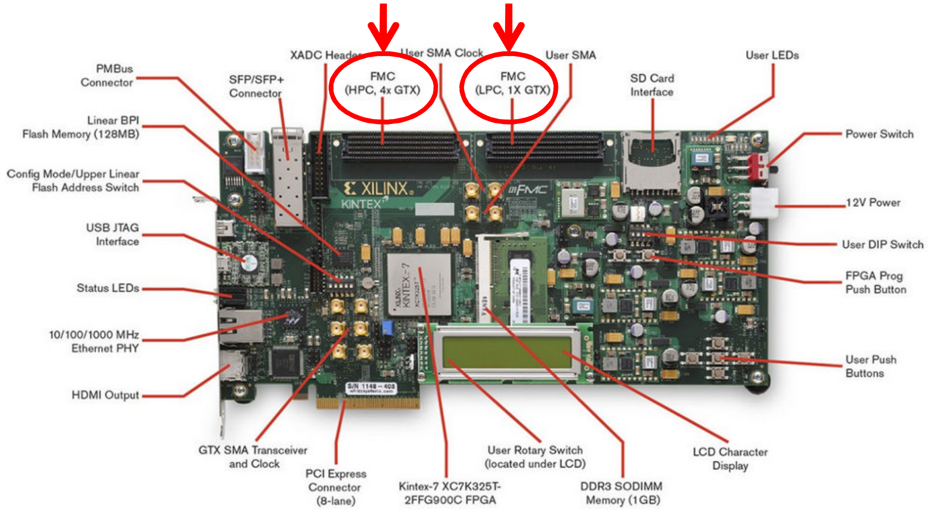
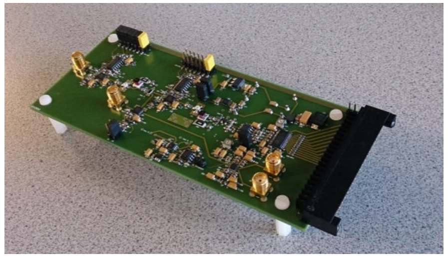
KC705 Evaluation Board for the Kintex-7 FPGA

- Main reason for the choice

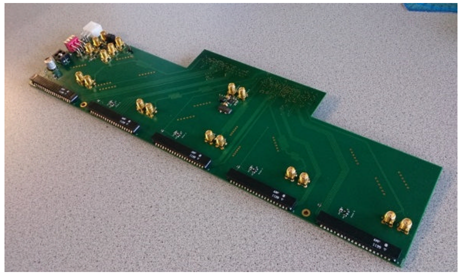


- High-performance transceivers capable of up to 12.5 Gb/s; the demonstrator of the Structures project runs at 8 Gb/s
- Extremely cheap multi channel high speed digitizing system

System assembly

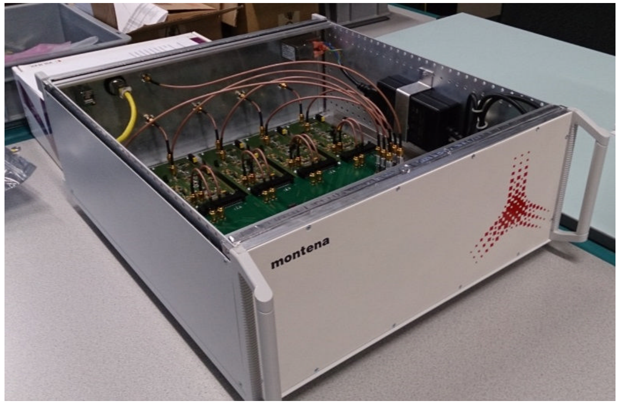


Sensor board



Interface Board

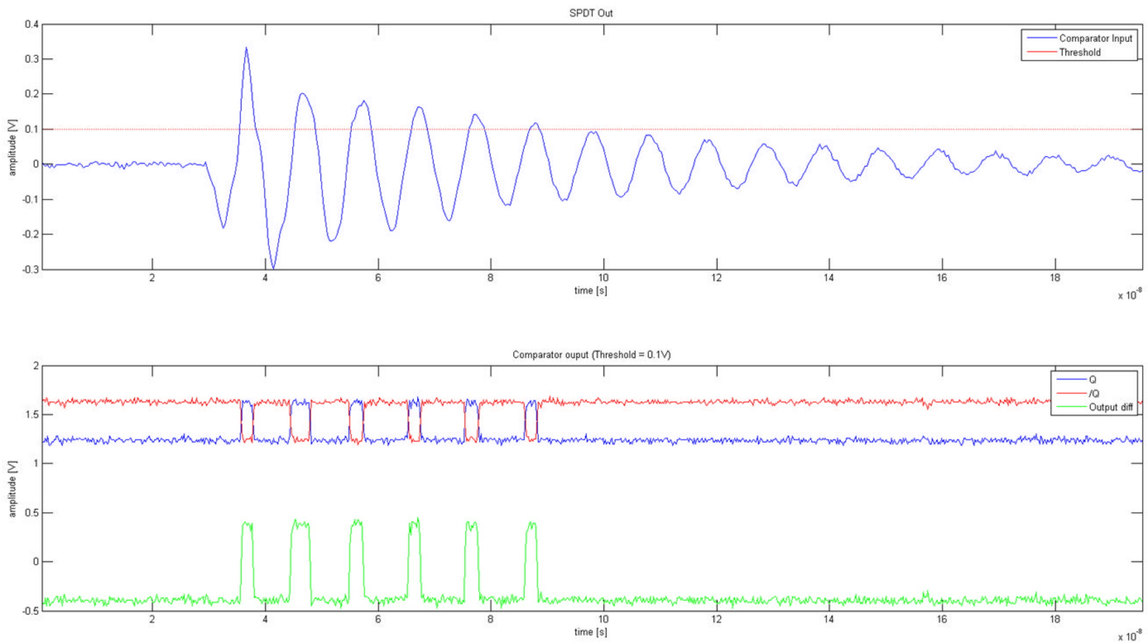
FPGA



Integrated equipment

Hardware results & measurement

- Comparator measurement



Comparator result (Damped Sinus 100MHz)

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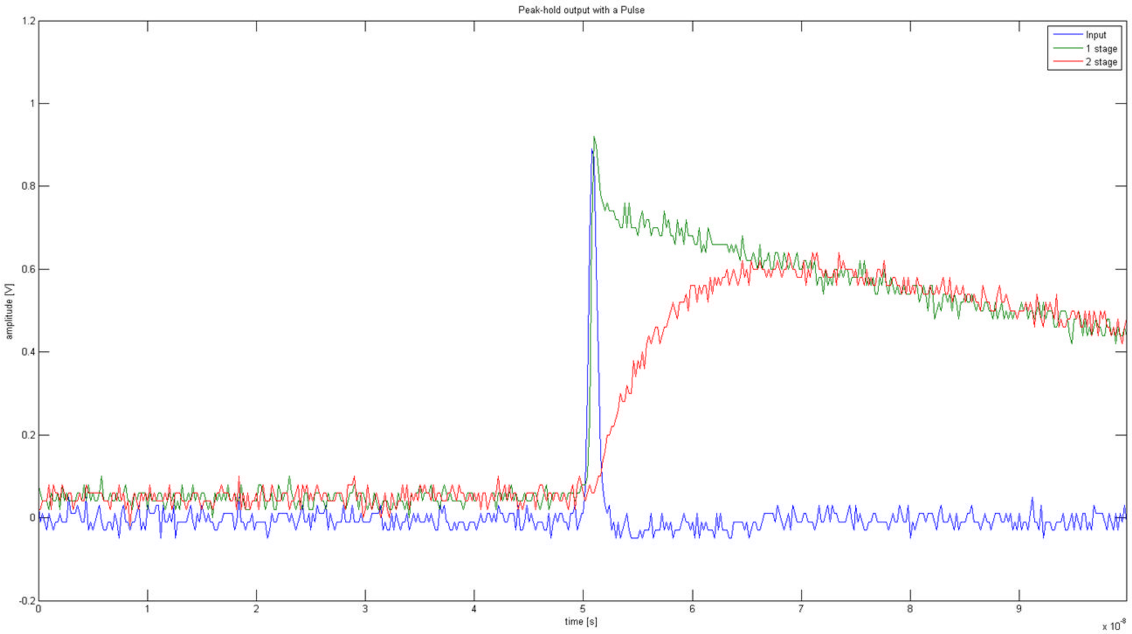
Hardware results & measurement

- Peak-hold measurement



Peak-hold with pulse signal

Algorithm: Localization

Time Difference of Arrival (TDoA)

- Calculating the time difference between the received signals at the different sensor locations using the cross correlation algorithm
- 5 sensors are used of which one is considered as reference
- Using 5 sensors, the set of equations can be linearized
- Solving the source location by linear algebra methods

Localization and identification system Status

- Prototype detection and identification system demonstrated

