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Innovative Approaches for AlGaN/GaN-based Technology

By

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Abstract

Gallium Nitride (GaN) has been proven to be a very suitable material for advanced power electronics on account of its outstanding material properties. Today, researchers are exploring GaN-based high electron mobility transistors (HEMTs) for conventional as well as high-end solutions in the range of 600 – 1200 V. However, thermal and power density limitations have impeded the achievement of the peak operational capability of AlGaN/GaN HEMTs. GaN-on-Diamond technology has proven to be a feasible solution to reduce thermal resistance and increase power density of AlGaN/GaN HEMTs for RF applications. The work presented in this thesis is focused on the realisation of high-voltage GaN-on-Diamond power semiconductor devices. This goal was achieved through extensive numerical simulations applied to device design, fabrication, and characterisation. The fabricated devices include conventional AlGaN/GaN HEMT design in circular and linear form with and without field plate engineering. The circular GaN-on-Diamond HEMTs with gate width of ~ 430 μm, gate length of 3 μm, gate-to-drain separation of 17 μm and source field plate length of 3 μm have shown breakdown voltage of ~ 1.1 kV.

In this work a new concept of normally-off optically-controlled AlGaN/GaN-based power semiconductor device is proposed. A simulation study has been carried out in order to explore the DC characteristics, switching characteristics, breakdown voltage, and current gain of these novel devices. The typical structure comprises a 20 nm of undoped $Al_{0.23}Ga_{0.77}N$ barrier layer, a 1.1 μm undoped-GaN buffer layer and a p-doped region (to locally deplete the electron channel and ensure a normally-off operation). The simulation study shows that the gain and the breakdown voltage of the device are highly dependent on the depth of the p-doped region. At a particular depth of the p-doped region of 500 nm the gain of the device is 970 (at light intensity of 7 W/cm^2) and the breakdown voltage is ~ 350 V. The rise and fall times of the device is found to be 0.4 μsec and 0.3 μsec respectively. The simulation results show a significant potential of the proposed structure for high-frequency and high-power applications.

Acknowledgements

First of all, I must express my sincere gratitude to my supervisor, Professor Shankar Madathil, who gave me the chance to be a part of this exciting area of research, and whose valuable support, guidance and encouragement have been vital during the course of my study.

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I also want to thank Element Six for providing GaN-on-Diamond epi-wafers for this work.

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Chapter 1

Introduction

The semiconductor industry has been dominated by Silicon (Si) since 1959, when the metal-oxide-semiconductor field-effect-transistor (MOSFET) was invented. Si's dominant position can be mainly attributed to low cost and the simplicity of growth of a high-quality native oxide on its surface, which facilitated the development of complementary metal-oxide-semiconductor (CMOS) process that revolutionised the digital world we currently live in. Although Si has been the traditional choice of material in the power semiconductor industry, it is a narrow band gap semiconductor (band gap energy, E_G = 1.1 eV) and that limits its power handling capability. Hence the search for potential replacements with superior properties continues. The new wide band gap materials which are being extensively investigated include gallium nitride (GaN), silicon carbide (SiC), and diamond.

Since the realisation of the first GaN based transistors in the early to mid-1990's [1] they have been widely studied and developed for high-voltage power switching as well as for high-frequency high-power applications. GaN has a wide band gap (E_G = 3.44 eV) which translates into ability to sustain high electric fields without material breakdown. Among the other wide band gap materials (SiC and diamond), GaN is particularly attractive on account of its ability to create heterojunctions with materials of wider band gap such as aluminium nitride (AlN) (E_G = 6.2 eV) or aluminium gallium nitride ($Al_{0.26}Ga_{0.74}N$) (E_G = 4.09 eV). At the interface of this heterojunction, the formation of a highly dense electron channel or a 2-dimensional-electron-gas (2DEG) with high mobility naturally occurs, due to high polarisation inside the semiconductors. The abilities of GaN to form 2DEG and support high electric fields can be used to create devices which are able to provide or handle high output power and can be operated up to 450 GHz for power amplifier applications or as power switches respectively. It is expected that GaN based power semiconductor devices with power densities of about 10 times greater than that of gallium arsenide (GaAs) [2] will prevail over traditional semiconductors (such as GaAs and Si) in high end applications. GaN substrates are expected to have a market

size of almost $4 billion in 2020 [3]. Fig. 1.1 shows a prediction of the positioning of the current and future device technologies [4]. According to Fig. 1.1, wide band gap devices are primarily positioned for high-end applications and GaN devices are currently targeted for medium voltage applications (in the 200 – 600 V). GaN devices also play a significant role in the optoelectronic sector, particularly as light emitting diodes (LEDs). Fig. 1.2 shows a GaN-on-diamond wafer manufactured by Element Six [5], one of the fabricated devices during this research as well as commercially available devices and examples of targeted applications for GaN-based technology.

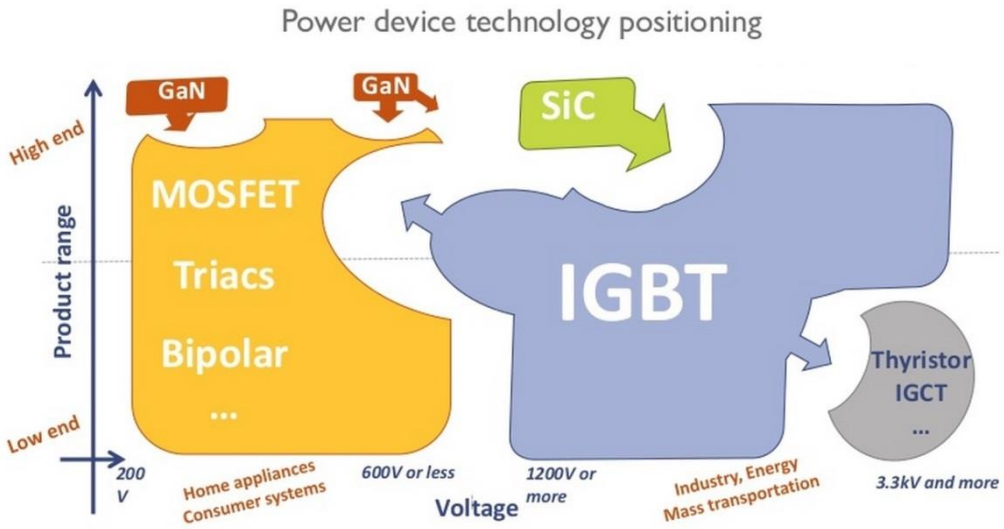


Figure 1.1: Power device technology positioning with respect on voltage range [4].

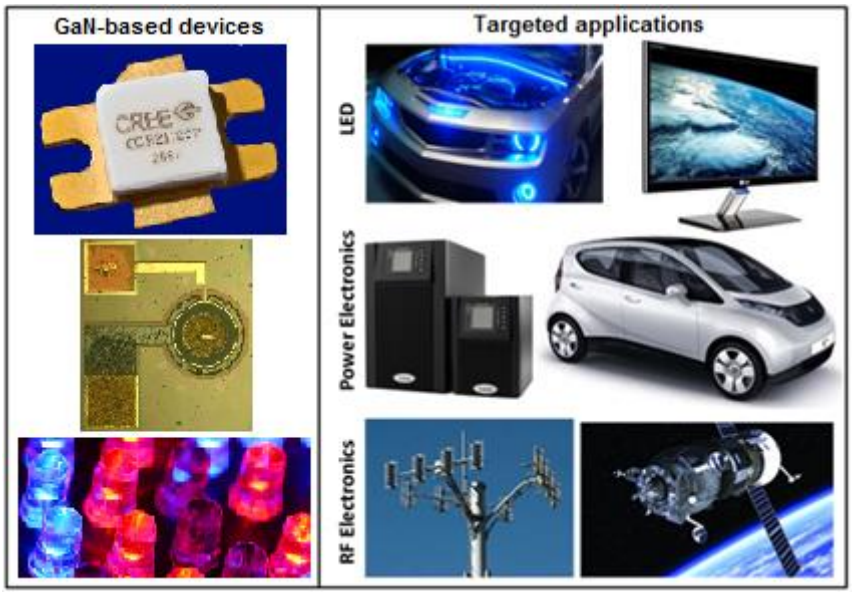


Figure 1.2: GaN-on-Diamond and targeted applications.

1.1 Material Properties and Figures of Merit

The outstanding properties of GaN are very appealing for power electronic applications. The comparison between GaN and Si (which has been the main player in the field for almost forty years) can provide a clear understanding of why GaN is so attractive to the electronics industry. The properties of GaN include [6, 7, 8]:

- Wide band gap (E_G = 3.4 eV for GaN compared to E_G = 1.1 eV for Si)
- High critical electric field (~ 330 V/μm for GaN compared to 30 V/μm for Si)
- High saturation velocity and electron mobility (2.5 x 10^7 cm/s and 900 – 2000 cm^2/V·s for GaN compared to 1.0 x 10^7 cm/s and 1350 cm^2/V·s for Si, respectively).

These superior properties of GaN translate into the following potential benefits of GaN based devices compared to those fabricated using Si:

1. Better voltage blocking capability. Since the critical electric field of GaN is ~ 300 V/μm then theoretically a bias voltage of 300 V could be applied across a region with a spacing of 1 μm before avalanche breakdown is initiated in the material. However, this theoretical limit for a given drift length has not been demonstrated yet in lateral GaN devices, as it's primarily governed by the overall electric field profile in the device, under blocking conditions.
2. Lower on -state losses. The specific on-state resistance of GaN devices is expected to be lower by more than two orders of magnitude compared to Si based devices, while sustaining the same blocking voltage of 1000 V [101], thereby significantly enhancing the efficiency of the devices.
3. Faster switching frequencies resulting in circuits using GaN HEMTs requiring smaller capacitors and inductors and so reducing overall size and cost.
4. Ability to work at higher temperatures with lower losses due to wider bandgap and hence significantly lower intrinsic carrier concentration. By operating at temperatures beyond 300 °C [9, 10] GaN-based devices can reduce the necessity of cooling systems and large heat sinks, however it

was also reported that the RF operational lifetime can be reduced due to thermal activated degradation at 300 °C (10^4 hours) [116].

Table 1.1 shows the key material parameters of semiconductors for power switching applications: E_G – bandgap energy of material, ε – relative dielectric constant, E_C – critical breakdown field, κ – thermal conductivity, μ_n – mobility of electrons, and ν_{sat} – saturated electron velocity.

Table 1.1: Properties of most commonly used semiconductors for high frequency and high power electronic applications [6].

Parameter	Si	GaN	4H-SiC	Diamond	GaAs
E_G (eV)	1.1	3.4	3.3	5.5	1.42
ε	11.8	9	10	5.5	13.1
E_C (MV/cm)	0.3	3.3	3.0	5.6	0.4
κ (W/cm·K)	1.5	1.3	4.5	20	0.43
μ_n ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	1350	900 (Bulk) 2000 (2DEG)	700	1900	8500
ν_{sat} (10^7 cm/s)	1.0	2.5	2.0	2.7	1.0
Band type	I	D	I	I	D

In order to make an accurate and practical comparison between materials shown in Table 1.1, figures of merit (FOM) can be used. FOMs are derived purely considering certain key material properties and can be used as benchmarks to directly compare different materials in the context of specific electrical characteristics. There are four FOMs (Table 1.2) that have been most frequently used in the field of power electronics to compare semiconductor materials and are as mentioned below:

1. Johnson's power handling figure of merit (JFOM) brings together the saturated drift velocity and the critical electric field of the material. The JFOM provides an indication of the power handling capability of a device at high frequencies. The JFOM of GaN is 760 times greater than that of Si (the larger number shows its superiority) [6].
2. Baliga's conduction losses figure of merit (BFOM) brings together the relative permittivity, mobility and the critical electric field of the material and

serves as an indicator of conduction losses in a device. The BFOM of GaN is 650 times higher than that of Si [6].

3. Baliga's high frequency figure of merit (BHFFOM) is based on mobility of the carriers and the critical electric field of the material and serves as an indicator of switching losses of a power device. The BHFFOM of GaN is 77.8 times higher than that of Si [6].
4. Keyes's thermal performance figure of merit (KFOM) brings together thermal conductivity, the saturated drift velocity, and the relative permittivity of the material and provides an indication of thermal performance of power devices. The KFOM of GaN is 1.6 times higher than that of Si [6].

Table 1.2: Figures of merit of frequently used semiconductors for high frequency and high power electronic applications [6].

FOM	Si	GaN	4H-SiC	Diamond	GaAs
Johnson $(E_C \cdot \nu_{sat}/\pi)^2$	1	760	180	2540	7.1
Baliga $\varepsilon \cdot \mu \cdot E_c^3$	1	650	130	4110	15.6
Baliga HF $\mu \cdot E_c^2$	1	77.8	22.9	470	10.8
Keyes $\kappa(\nu_{sat}/\varepsilon)^{1/2}$	1	1.6	4.61	32.1	0.45

1.2 AlGaN/GaN HEMT. Structure and band diagram

High electron mobility transistors (HEMTs) are the most common lateral gallium nitride based electronic devices. They form the primary building blocks for a number of high power applications such as power amplifiers and power switches [8]. GaN based HEMTs are the type of devices used in this work therefore their structure and properties will be described in this section.

Fig. 1.3 shows a cross-sectional schematic of a typical GaN HEMT. The most common ways to grow the material structure are molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD). As it was indicated in Table 1.1, the mobility of electrons in bulk GaN is ~ 900 cm^2/ V·s. By growing semiconductor with a wider bandgap (so called barrier layer) on top of bulk GaN, a heterojunction with quantum well could be formed. Electrons confined into this

quantum well represent a 2-dimensional-electron-gas (2DEG), and their mobility can be up to 2000 cm^2/ V·s [11]. $Al_xGa_{1-x}N$ acts as the barrier layer that typically has a thickness of about 20 – 30 nm. X in $Al_xGa_{1-x}N$ is the percentage of Al in the alloy also referred to as the mole fraction and is usually in the range of 20 – 30%. AlN has also attracted some attention as barrier on account of high electron density in the 2DEG (up to ~ $2x10^{13}$ cm^{-2} can be achieved with only 3 nm of barrier layer [12]), however the potential of AlN has been limited by a number of problems such as high Ohmic contact resistances, high leakage currents and surface sensitivity [13].

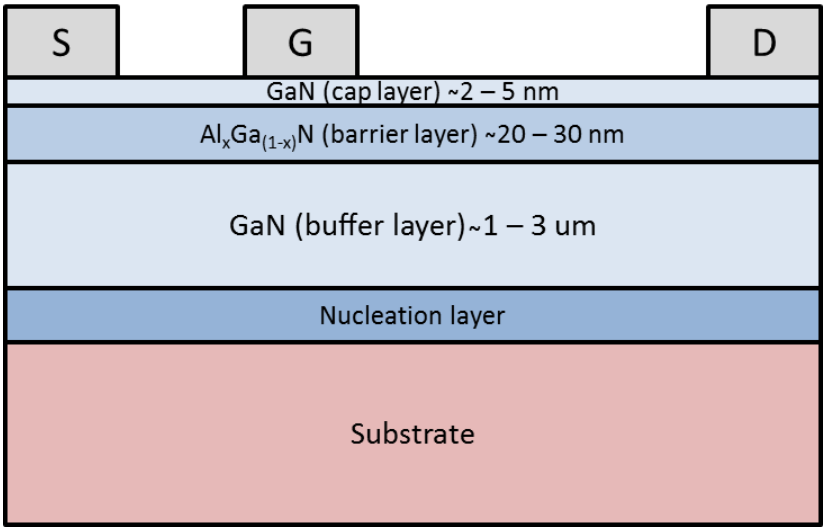


Figure 1.3: Illustration of the cross-sectional schematic of a typical GaN-based HEMT.

As shown in Fig. 1.3, GaN-based HEMTs are usually grown on a thick substrate of foreign material because of the high cost and difficulty of obtaining native GaN substrates. Sapphire, Si, or SiC are the most common choices for the substrate. In order to reduce lattice mismatch and difference in the thermal expansion coefficients between the GaN epilayers and the foreign substrate an intermediate/nucleation layer (or layers) is usually introduced. For instance, if sapphire substrate is used for GaN growth then the two step growth method could be used to achieve crack-free GaN epitaxial films [117]. Firstly, a thin AlN nucleation layer is deposited at low temperature (500 – 600 °C) and then GaN deposited at higher temperature (1000 °C). Due to increased temperature, the polycrystalline nano-islands will be formed in AlN layer which acts as the nucleation layer for GaN growth. If SiC substrate is used for epitaxial growth, then a thin layer of AlN (nucleation layer) is usually grown on top of it in order to decrease the lattice

mismatch and stress between GaN buffer layer and foreign substrate material. In case of Si substrates, an AlN nucleation layer is often grown to avoid the diffusion of Ga into Si substrate which is usually followed by several GaN/AlN superlattices. These superlattices are introduced to create an additional compressive stress in order to counterbalance the tensile strain present in nitrides deposited on silicon.

In order to increase the effective Schottky barrier height and reduce gate leakage current a thin GaN cap layer is usually grown on top of the AlGaN barrier layer [14, 15]. The top GaN layer is also deposited to reduce oxidation of the surface of AlGaN layer and to improve the formation of electrical contacts [118].

The structure shown in Fig. 1.3 requires no impurity doping since piezoelectric and spontaneous polarisation of the AlGaN/GaN heterostructure provide so-called polarization doping that forms an electron channel of very high concentration and mobility. AlGaN/GaN HEMT is typically a three terminal device with a Schottky Gate contact, an ohmic Drain contact and an ohmic Source contact.

Fig. 1.4 illustrates the conduction band diagram of an AlGaN/GaN heterojunction, where GaN with its narrower band gap is shown on the right side and AlGaN with its comparatively wider band gap on the left. A conduction band offset ΔE_C, which is formed at AlGaN/GaN heterointerface because of the difference in the conduction band energies, leads to formation of a triangular quantum well. This quantum well attracts the electrons (because of preferable lower energy) which form the 2DEG.

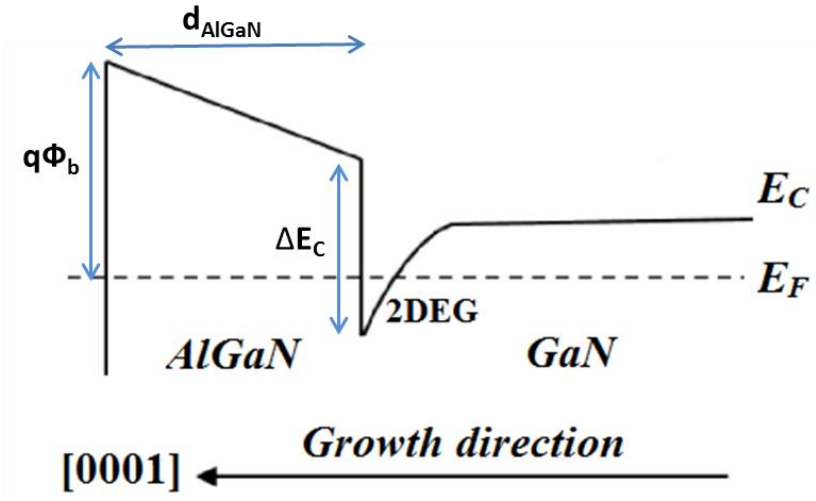


Figure 1.4: Schematic illustration of conduction band diagram of an AlGaN/GaN heterojunction.

1.3 GaN devices for high power applications

Power semiconductor devices (PSDs) are the basis of the power electronics, where Si has been the dominant player for decades. First power MOSFETs on silicon began appearing in 1976 and became a better alternative to the bipolar junction transistors (BJT). These devices had better power handling capability, higher switching speed and larger current gain than BJTs. Power MOSFETs started to populate our lives by many different applications such as early computer's power supplies, DC-DC converters, fluorescent lights, motor drives, etc. [16].

Despite that Si has reached its theoretical limits, research on design and fabrication of Si devices is still going on, primarily due to low cost of the material. However, the theoretical limits of Si devices include a breakdown field of only 30 V/μm; Si also suffers from high on-state resistance which leads to high conduction losses. Thus, it is evident that much more efficient power devices based on alternative superior semiconductor materials would be very desirable.

GaN based HEMTs have proved that they are legitimate candidates for high frequency high power applications. The great potential of these devices is mainly based on high switching speeds, lower specific on-state resistance, and high breakdown voltages [17]. Therefore, it is obvious that research into design and fabrication of effective GaN based devices is of current importance.

The critical electric field of GaN is ~ 300 V/μm which means that a bias voltage of around 300 V could be applied to contacts on GaN with a spacing of only 1 μm before material breakdown would occur (assuming uniform distribution of the electric field between the contacts). However, this is not the case for AlGaN/GaN HEMT which has three electrodes (as shown in Fig. 1.3). For such a device when high drain voltage is applied, the electric field starts crowding at the drain end of the gate. This crowding of electric field can exceed the critical electric field of the semiconductor and lead to premature breakdown. This issue is one of the main challenges in the development of high power AlGaN/GaN HEMTs for power electronics as well as for microwave power amplifier applications.

1.4 Aims of the research

Power density is one of the main figures of merit used to evaluate the progress of power electronics. Diamond is the most thermally conductive material found in nature, which makes diamond substrates very appealing choice to address the heat spreading issues and for the development of AlGaN/GaN HEMTs for high power density applications. This work is focused on realisation of high voltage GaN-on-Diamond power devices. Another, focus of this research is the introduction of the new concept of the normally-off optically-controlled AlGaN/GaN-based power semiconductor device. The goals of this research could be summarised as follows:

1. Numerical simulations of AlGaN/GaN HEMTs in order to get an insight on the operation and dependence of key electrical characteristics on geometrical parameters of the device architecture.
2. Device design and optimisation for realising high voltage devices (> 1000 V), process-flow development, device fabrication followed by extensive electrical characterisation.
3. Novel design of optically-controlled enhancement-mode GaN power semiconductor devices using detailed numerical simulations.

1.5 Thesis structure

As mentioned in the previous section, this thesis will primarily concentrate on the realisation of high-voltage GaN-on-Diamond power semiconductor devices by means of simulation, device design and optimisation, process-flow development, device fabrication, and comprehensive electrical characterisation. This thesis will also focus on the development of optically-controlled enhancement-mode GaN power semiconductor devices using physically-based simulation. Other aspects which can affect performance of GaN devices such as material structure, growth and substrates, metal contacts, surface passivation will be also referred and briefly discussed.

The structure of this thesis is as follows:

Chapter 1 provides an introduction.

Chapter 2 will provide an overview of the unique material properties of GaN and describe in detail the formation of the 2DEG in an AlGaN/GaN heterostructure, which followed by the description of the operation principle of AlGaN/GaN HEMTs and main challenges.

Chapter 3 will provide the details of the numerical simulation of the AlGaN/GaN HEMTs relevant for this research. The information obtained from the simulation gives insight into the operation of the device, electric field distribution in the device without and with field plates at the moment of material breakdown. Based on these results a new idea of the non-uniform field plate is introduced.

Chapter 4 will outline the device design optimized via simulation, process-flow developed for this work, and device fabrication.

Chapter 5 will provide comprehensive electrical characterisation of the fabricated devices.

Chapter 6 will provide an overview of photoconductive power semiconductor devices and introduce a new concept of the normally-off optically-controlled AlGaN/GaN-based PSD via simulation study.

Chapter 7 will give conclusion of this thesis along with the future work which could be carried out.

Chapter 2

Properties of GaN and AlGaN/GaN heterostructure

2.1 Introduction

This chapter will provide a comprehensive overview of the main physical properties of III-nitrides, AlGaN/GaN heterostructures along with the operating principle of AlGaN/GaN HEMTs. Firstly, the strong polarisation fields which are present in GaN and GaN based heterostructures will be outlined and then followed by a description of the way the 2-dimesional electron gas (2DEG) is formed. Metal contacts, operation principle of AlGaN/GaN HEMTs along with breakdown mechanism will then be covered. To conclude the chapter the growth of III-nitrides and the various substrates most commonly utilized for their growth will be described.

2.2 Physical properties of GaN

III-nitride materials (as well as SiC and diamond) fall into the category of wide band gap semiconductors which also have smaller bond length between their atoms in comparison with GaAs and Si. The small bond length translates into strong bonding energy between the constituent atoms resulting in highly stable and inert materials. Fig. 2.1 shows the correlation between the band gap and bond length energy of different semiconductors. It can be seen that III-nitrides as well as other wide band gap materials (SiC and diamond) are positioned in a different domain in comparison with GaAs and Si.

GaN and other III-nitrides can take different crystal forms: Wurtzite, Zincblende or rock-salt [18, 19]. Wurtzite is the most commonly used structure because it is more stable and easier to grow [18]. The vast majority of GaN based devices are grown on Wurtzite structure and only Wurtzite GaN will be further discussed.

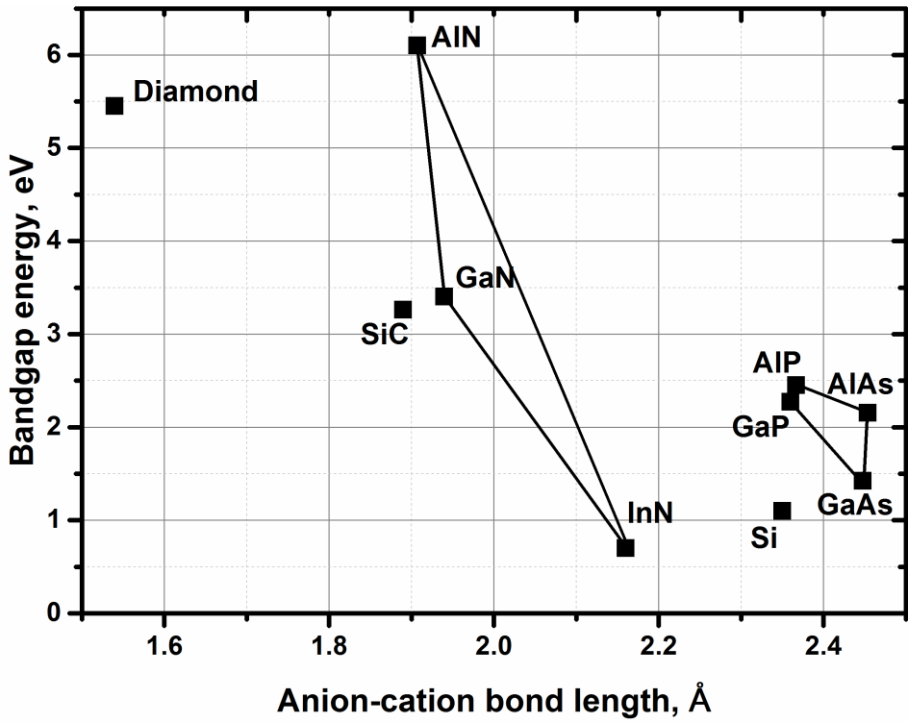


Figure 2.1: Correlation between the anion-cation bond length and band gap energy for most commonly used semiconductor materials [6].

The hexagonal unit cell of Wurtzite structure is defined by two lattice parameters *a* (the edge length of the basal hexagon) and *c* (the height of the hexagonal unit cell), and the internal parameter *u* (anion-cation bond length *b* divided by *c*) as shown in Fig. 2.2 [20]. The Wurtzite structure of GaN (as well as other III-nitrides) lack an inversion plane perpendicular to the *c*-axis, for this reason GaN can exist in two different polarities, Ga-face (grown in the [0001] direction) or N-face (grown in the $[000\bar{1}]$ direction) [11]. The distinction between these two polarities is very important since they have different implications for the polarity of the polarization charge and can affect device processing and performance. In general, the crystal with Ga-polarity is more chemically stable and robust than the one with N-polarity [18]. Due to the hardness of Ga-polar GaN its etching rate is much smaller than the etching rate of N-polar GaN at the same conditions [18]. Even though the devices based on N-polar GaN have been investigated and shown good performance [21], the vast majority of electronics research is focused on Ga-polar GaN. Throughout the course of this work only the Ga-polar materials have been used.

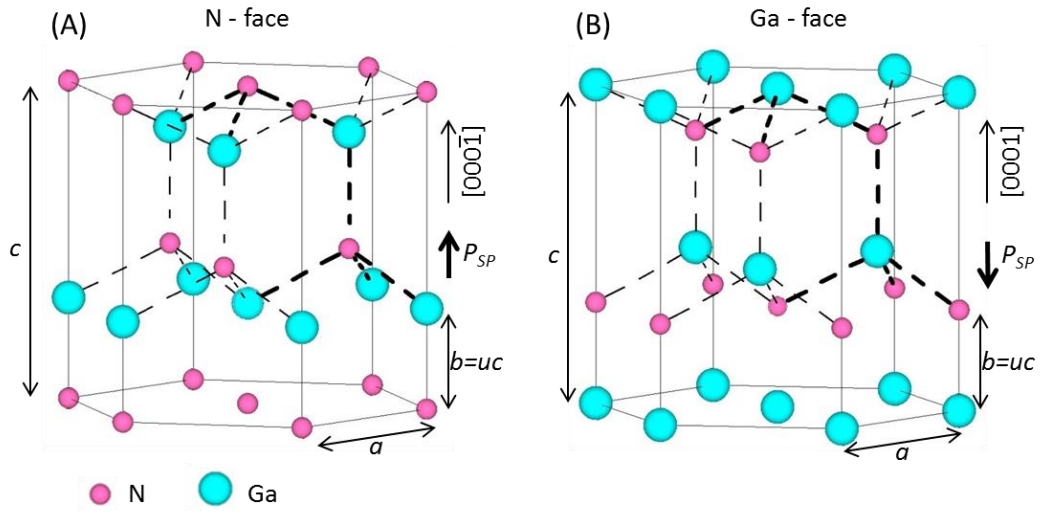


Figure 2.2: Illustration of the hexagonal Wurtzite structure for GaN with (a) N-polar face and (b) Ga-polar face.

2.3 Polarisation in AlGaN/GaN and 2DEG formation

As described in Section 1.3, an electron channel with very high carrier density called a two-dimensional electron gas (2DEG) could be formed at the AlGaN/GaN heterointerface. In order to understand the origin of electrons which form the 2DEG, it is useful to have a closer look at the phenomenon of polarisation in GaN and AlGaN/GaN heterostructures.

2.3.1 Polarisation

All semiconductors with a non-centrosymmetric crystal structure exhibit polarisation-related effects [119].

Spontaneous polarisation occurs in a material when a polarisation dipole exists in each unit cell of the relaxed material in its equilibrium state. In wurtzite structure, this happens both because of a lack inversion symmetry in the crystal and a deflection in lattice parameters *c* and *a* from their ideal ration (i.e., $c/a = (8/3)^{1/2}$). The deflection from the ideal ratio leads to a net displacement between anion and cation placement within the unit cell and creats a dipole [119]. The Wurtzite GaN crystal (as well as AlGaN) can benefit from spontaneous polarisation P_{SP} without application of any external electric fields along the *c*-axis and oriented parallel to the [0001] direction.

Within a bulk crystal, polarisation does not induce a net negative or positive charge since the charge imbalance from each dipole is cancelled by adjacent dipoles. However, there is bound polarisation charge at the interfaces or surfaces of a crystal due to the change in spontaneous polarisation density [119].

Piezoelectricity is an electromechanical phenomenon in which an electric dipole is generated by an external mechanical stress [120]. When a relatively thin AlGaN layer (usually 20 – 30 nm) is grown on top of bulk GaN the mismatch between their lattice structures brings in tensile strain which leads to piezoelectric polarization P_{PE} in the AlGaN barrier layer, while the GaN buffer layer is fully relaxed on account of its relatively high thickness (usually 1 – 3 μm) and hence does not have any piezoelectric polarisation. The piezoelectric polarisation can be defined by [11]:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y), \tag{2.1}$$

where $\varepsilon_z = (c - c_0)/c_0$ is the strain along the c-axis, $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$ is the in-plane strain, a_0 and c_0 are the equilibrium values of the lattice parameters.

The relation between the lattice constants of the hexagonal GaN is given by [11]:

$$\frac{c - c_0}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0}, \tag{2.2}$$

where C_{13} and C_{33} are elastic constants. Using Eqs. (2.1) and (2.2), the amount of the piezoelectric polarisation in the direction of the c-axis can be calculated by [11]:

$$P_{PE} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right), \tag{2.3}$$

It has been shown that $[e_{31} - e_{33}(C_{13}/C_{33})]$ for AlGaN over the whole range of compositions, the piezoelectric polarisation is positive for compressive and negative for tensile strained barriers, respectively [11]. Fig 2.3 shows Ga-polar AlGaN/GaN heterostructure with the indicated directions of the piezoelectric and spontaneous polarization. The spontaneous polarisation P_{SP} of AlGaN is greater than that of GaN because the asymmetry of the crystal increases with Al concentration, which leads to an increase in the values of the polarization constants [22]. The spontaneous

polarisation for AlN and GaN was found to be negative [11], meaning that for Al(Ga)-face heterostructures the spontaneous polarisation is pointing towards the substrate (Fig. 2.3).

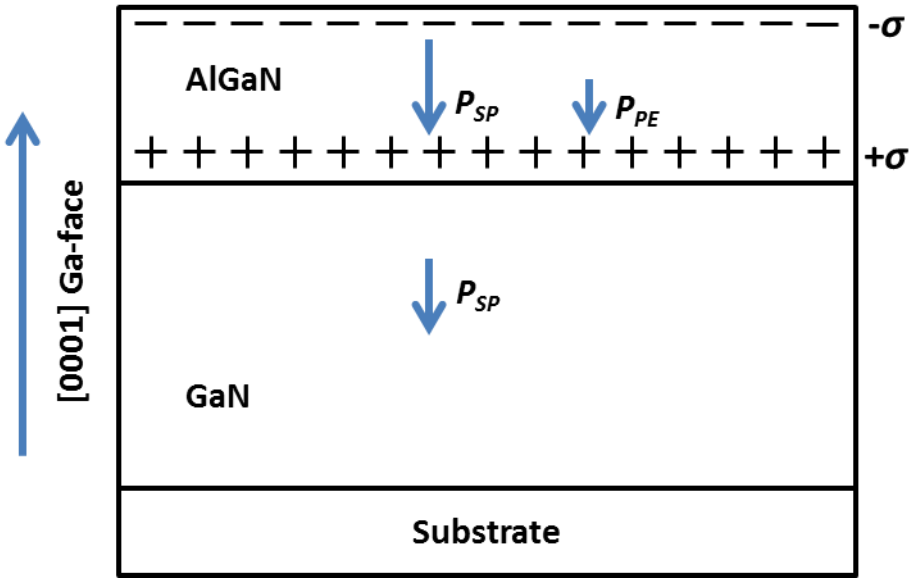


Figure 2.3: Schematic structure of a Ga-face AlGaN/GaN heterostructure with indicated polarization induced charges and directions of piezoelectric and spontaneous polarisation [11].

The linear interpolations between the physical properties of AlN and GaN to calculate the amount of the polarisation induced sheet charge density σ at the AlGaN/GaN interface in dependence of the Al-content *x* of the $Al_XGa_{1-X}N$ are given by [11]:

Lattice constant: $a(x) = (-0.077x + 3.189)\ 10^{-10}$ m,

Elastic constants: $C_{13}(x) = (5x + 103)$ GPa,

$C_{33}(x) = (-32x + 405)$ GPa,

Piezoelectric constants: $e_{31}(x) = (-0.11x - 0.49)$ C/m^2,

$e_{33}(x) = (0.73x + 0.73)$ C/m^2,

Spontaneous polarisation: $P_{SP}(x) = (-0.052x - 0.029)$ C/m^2, (2.4)

As shown in Fig. 2.3, a positive sheet charge is induced at the AlGaN/GaN heterointerface by the resulting polarisation. This positive charge will draw free

negative charge carriers (in order to be compensated) which form the 2DEG with electron concentration n_S. The charge density induced by polarization using Eqs. (2.3) and (2.4) can be calculated by [11]:

$$\begin{aligned}\sigma(x) &= P(Al_xGa_{1-x}N) - P(GaN) = \\ &= P_{SP}(Al_xGa_{1-x}N) + P_{PE}(Al_xGa_{1-x}N) - P_{SP}(GaN) = \\ &= 2\frac{a(0)-a(x)}{a(x)}\left(e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right) + P_{SP}(x) - P_{SP}(0)\end{aligned} \tag{2.5}$$

For the N-face heterostructure, the sign of the polarisation induced sheet charge is negative for the AlGaN/GaN and positive for the GaN/AlGaN interface. For a Ga-face heterostructure, the amount of the sheet charge density remains the same, but the positive sheet charge causing a 2DEG is located at AlGaN/GaN interface [11].

2.3.2 Formation of the 2DEG

As mentioned in previous section, free electrons tend to compensate the positive polarisation induced sheet charge at the AlGaN/GaN interface. The maximum sheet carrier concentration located at these interfaces of the nominally undoped structures is given by [11]:

$$n_S(x) = \frac{+\sigma(x)}{e} - \left(\frac{\varepsilon_0\varepsilon(x)}{de^2}\right)[q\phi_B(x) + E_F(x) - \Delta E_C(x)], \tag{2.6}$$

where $\varepsilon(x)$ is the relative dielectric constant of the $Al_XGa_{1-X}N$ barrier layer, d is the thickness of this layer, $q\phi_B$ is the height of Schottky barrier of the gate electrode, ΔE_C is the offset of the conduction band at the interface of AlGaN/GaN heterostructure, and E_F is the Fermi level (these components could be seen in Fig. 1.4). One of the dominant components of the Eq (2.6) is the polarization induced sheet charge. The Al-content of the AlGaN barrier layer has a direct impact on this charge, so that if the percentage of Al is increased the polarization charge will be increased and therefore the concentration of electrons can be increased [11]. However, if the percentage of Al in the AlGaN barrier layer is more than 0.4, then the 2DEG mobility will be limited by increased structural defect density and a rough surface because of the increased thermal expansion coefficient mismatch and lattice

mismatch between AlGaN and GaN layers [11]. On the other hand, if $x < 0.15$, then the sheet carrier concentration starts to suffer from bad confinement due to decreased conduction band offset. Another important component of the Eq (2.6) is the thickness of the AlGaN barrier layer. So that by increasing the barrier thickness (above the critical thickness t_{CR}) the sheet carrier concentration can be increased, for a given Al-mole fraction. However, if the barrier thickness is too large, then the carrier density will drop due to strain relaxation [23]. For the above reasons, the typical barrier thickness is maintained between 20 – 30 nm with an Al-concentration of 20 – 25 %.

It has to be noted that the given description of the polarisation is for undoped materials and the 2DEG formation is happening without any impurity doping. The benefit of this is that electron mobility is not affected by the presence of ionised impurities.

The formation of 2DEG occurs without application of any external fields which means that large current can flow between source and drain at zero gate bias in AlGaN/GaN HEMTs. In order to switch off the device a negative voltage has to be applied to the gate electrode. Such devices are called normally-on (or depletion mode) transistors in contrast to the normally-off (or enhancement mode) transistors which are switched off at zero gate bias and require a positive (above zero) gate voltage in order to be switched on. Enhancement mode AlGaN/GaN HEMTs are preferred for power electronics since they are fail safe (i.e. in case of a malfunction of the control circuit, there would be no current path between ground and DC supply, whereas with a normally-on device there would be a short circuit between them) and their use can simplify the circuit design [25]. For this reason, normally-off transistors have been extensively studied and developed. The normally-on transistors are commonly used for RF applications.

Chapter 6 will provide a new concept for normally-off optically controlled AlGaN/GaN-based power transistor.

2.4 Metal contacts of the GaN-based HEMTs

GaN-based HEMTs have two types of contact, namely ohmic (source and drain) and Schottky (gate). Ohmic contacts have non-rectifying linear behaviour in

contrast to rectifying, non-linear Schottky contacts. Both Schottky and achieving good ohmic contacts are critical for enhancing device performance, functionality and reliability.

2.4.1 Ohmic contacts

The main purpose of the ohmic contacts is to form a low-resistance junction between metal electrode and semiconductor material in order to maximise the current flow and minimise the on-state resistance of the devices. Typically, to form ohmic contacts for AlGaN/GaN HEMTs, a four-layer metal stack is used which consist of titanium (Ti), aluminium (Al), nickel (Ni) and gold (Au). In this work, the thickness of these metal layers have been 20 nm of Ti, 100 nm of Al, 45 nm of Ni and 55 nm of Au. In order to make the pads of the devices more robust for probing, their additional metallization with Ti/Au (20/480 nm) has been carried out. The metals are deposited by a thermal evaporator and subsequently annealed at 800 °C for 1 min in N_2 ambient (using the Mattson RTA System) in order to get a low resistance contact. Each metal in this 4 layer stack plays a specific role in order to form the final ohmic contact after annealing, and they are as follows:

- **Titanium** ensures mechanical stability as well as good adhesion to the semiconductor material. After annealing, Ti extracts nitrogen N out of the GaN and leads to formation of a TiN interfacial layer. The vacancies left behind after N extraction, create high density of donor states close to the interface which form a tunnel junction. Furthermore, the TiN layer provides thermal stability to the contact [26].
- **Aluminium** reacts with Ti to form Al_3Ti layer which prevents oxidation of Ti. Al also improves the contact resistance by creating N vacancies (donor states beneath contact) after reaction with GaN [26].
- **Nickel** serves as a blocking layer which prevents mutual penetration of the top lying Au layer and the Al layer and formation of the highly resistive alloy known as ‘purple plague’ [27].
- **Gold** improves conductivity of the contact and prevents oxidation.

2.4.2 Schottky gate

In a typical AlGaN/GaN HEMT, the current flow between the ohmic drain and source contacts is controlled using a Schottky metal gate (Fig. 1.3). The Schottky contact is a rectifying junction between metal and semiconductor material. In order to obtain an effective Schottky gate contact the following properties are required:

- Good adhesion of the metal gate to semiconductor material
- High Schottky barrier height in order to reduce the leakage currents
- Mechanical and thermal stability during high-voltage operation

Various kinds of metals such as Ti, Pt, and Ni have been used to form the Schottky gate of AlGaN/GaN HEMTs so as to investigate the performance of the aforementioned attributes [28]. Among them, Ni/Au metallization scheme is now most commonly used to manufacture the Schottky contacts in GaN-HEMTs due to good adhesion properties and high work function of Ni, while the gold layer prevents oxidation and improves conductivity of the contact. The metal stack used in this work consists of 20 nm of Ni and 200 nm of Au. In order to make the pads of the devices more robust for probing, their additional metallization with Ti/Au (20/480 nm) has been carried out.

2.5 AlGaN/GaN HEMTs

This section will provide a detailed explanation of the operating principle of AlGaN/GaN HEMTs.

2.5.1 Operating principle

The main applications of AlGaN/GaN HEMTs are in power switching and high-frequency signal amplification. Fig. 2.4 shows schematic output current-voltage characteristics of an AlGaN/GaN HEMT. The most frequently used configuration to bias a GaN-HEMT is common source (as shown in the inset of Fig. 2.4).

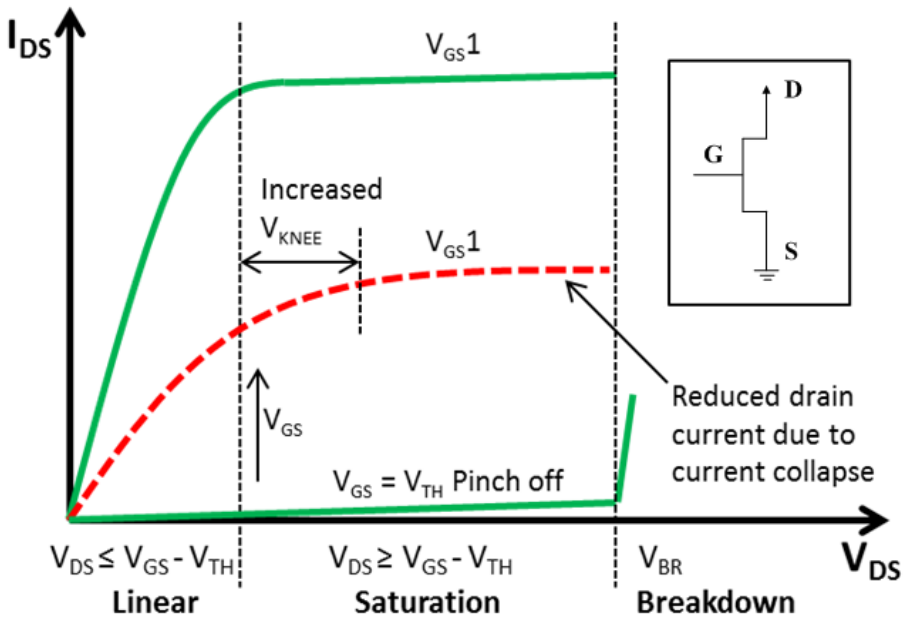


Figure 2.4: Schematic illustration of current-voltage characteristics of a GaN-based HEMT. Inset: common source configuration.

The input electrode is the Schottky gate, the output electrode is the drain whilst the source is the common terminal. The device is controlled by the gate's input signal which can switch the device between on and off-states. A normally-on device requires a negative voltage to be applied to the gate in order to deplete the electron channel and disrupt the current flow. The charge carrier concentration in the channel of GaN-based HEMT with application of gate bias voltage is given by [29]:

$$n_S = \frac{\varepsilon}{q(d+\Delta d)}(V_{GS} - V_{TH}) \tag{2.7}$$

where d is the thickness of the AlGaN layer, ε is the dielectric constant of the AlGaN layer, Δd is the distance from the heterointerface to the location of the 2DEG peak density, V_{TH} is the threshold voltage (i.e. minimum value of negative gate voltage at which the device current will start to flow), and V_{GS} is the gate voltage. When $V_{GS} = V_{TH}$, the Eq. (2.7) will be equal to zero meaning that there are no electrons in the channel and the device is switched off. If $V_{GS} = 0$, then the

channel will be naturally populated with electrons due to polarisation phenomena and the current will flow between the drain and source when a drain bias is applied.

When drain electrode of the GaN-based HEMT is biased at a low voltage (i.e. $V_D < V_{GS} - V_{TH}$), it is said to be operating in a linear region, where the electron velocity in the channel is linearly related to the applied electric field and hence the drain current will linearly increase with this field. The drain current in the linear region of a GaN-based HEMT is given by [30]:

$$I_{DS} = qn_S \upsilon W_G \tag{2.8}$$

where υ is the electron drift velocity in the channel and W_G is the width of the gate. The carrier velocity could be expressed through their mobility and the applied electric field [31]:

$$\upsilon = \mu E \tag{2.9}$$

where μ is the mobility of electrons and E is the electric field applied to the channel. The electron mobility in the channel of a GaN-HEMT could be affected by different scattering mechanism due to imperfections of the semiconductor material [32]. According to Eqs. (2.8) and (2.9), for low drain voltages, i.e. $V_D < V_{GS} - V_{TH}$ the drift velocity of electrons linearly rises with the electric field applied to the channel and so does the drain current. However, if the applied electric field is increased so that the drain voltage is $V_D > V_{GS} - V_{TH}$, then the velocity of the electrons will start to saturate and becomes independent of the applied electric field. The saturation of the electron velocity happens mainly due to scattering of the carriers with the semiconductor lattice.

Once the drain voltage is increased so that $V_D > V_{GS} - V_{TH}$, the longitudinal electric field below the gate (caused by high drain voltage) starts to pinch off the channel at the drain end of the gate. As a result, the amount of carriers allowed to flow in the channel becomes limited and the current becomes independent of any further increase in the drain bias (as shown in Fig. 2.4). This is known as the saturation region of device operation. The drain current in the saturation region of an AlGaN/GaN HEMT is given by [29]:

$$I_{DS} = \frac{\varepsilon W_G \upsilon_{SAT}}{(d + \Delta d)} (V_{GS} - V_{TH}) \tag{2.10}$$

where υ_{SAT} is the electron saturation velocity. Eq. (2.10) assumes that drain current is independent of drain voltage due to the saturated velocities of electrons.

2.5.2 Phenomenon of current collapse

The maximum output power of a GaN-HEMT can be calculated from the device's output I – V characteristics superimposed with the load line (Fig. 2.5) by the following expression [33]:

$$P_{OUT} = I_{DSOUT} V_{DSOUT} = \frac{I_{DSMAX}}{2\sqrt{2}} \frac{(V_{BR} - V_{KNEE})}{2\sqrt{2}} = \frac{I_{DSMAX} (V_{BR} - V_{KNEE})}{8} \tag{2.11}$$

where V_{BR} is the device's breakdown voltage, I_{DSMAX} is the maximum drain current, and V_{KNEE} is the knee voltage (i.e. voltage at which the device operation moves from the linear to saturation region). However, it has been experimentally observed that the power of a GaN-based HEMT is lowered due to the reduction of maximum drain current, known as current collapse [33] (see Fig. 2.5). This reduction of output current is directly related to the existence of the surface and buffer traps which can reduce the amount of carriers available in the channel [34]. The current collapse (also known as dispersion) increases the effective on-state resistance in the channel and hence the knee voltage increases as well.

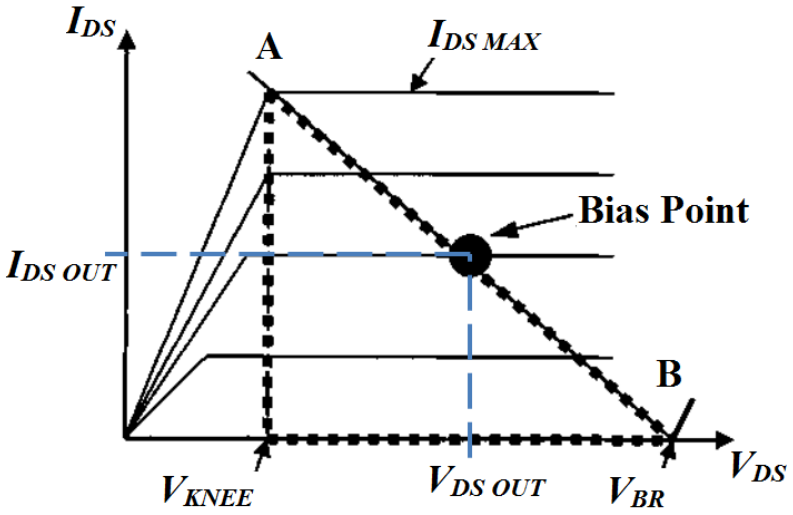


Figure 2.5: Schematic representation of I-V characteristics with a load line drawn to maximize the area of the power triangle shown by dotted lines [33].

The current collapse takes place when the gate contact of the device is biased to negative voltage. The electrons, which may leak from the gate contact when the negative gate bias is applied, are then caught by the empty surface states and buffer traps at the area near the gate (Fig. 2.6, b) [33]. These electrons captured by the surface traps induce so called 'virtual gate' (i.e. the surface with negative potential). This virtual gate acts as a metal gate with an applied negative bias and hence can modulate the depletion region and reduce the amount of charge carriers in the channel, thereby decreasing the drain current of the device. The current collapse is most apparent when the device operates under RF or pulsed conditions, since the device has to be repeatedly switched on and off in a very short time, but the electrons capturing leads to reduced transconductance and thereby resulting in slow transient process. The transient time constants of the trapped electrons are dependent on the energy levels of the surface traps [35].

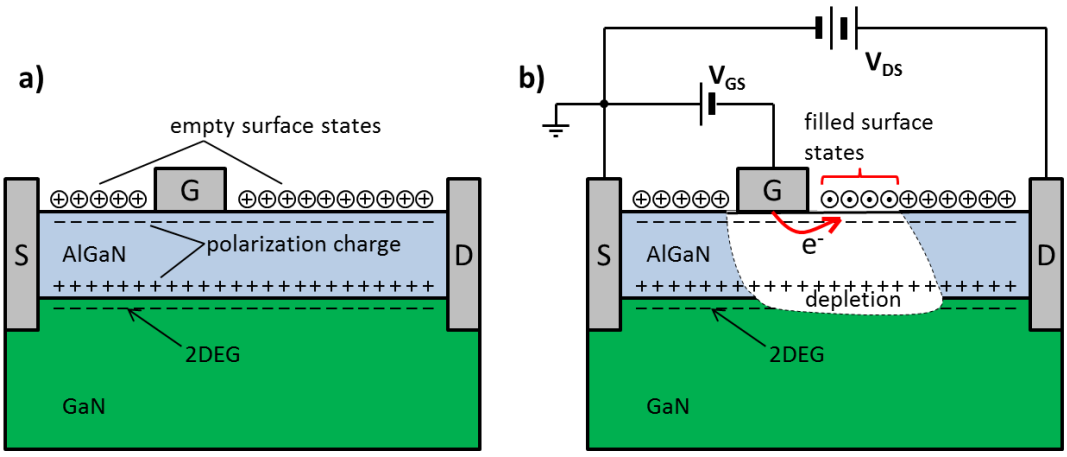


Figure 2.6: Illustration of the current collapse: a) GaN-HEMT with no external field applied; b) a negative voltage is applied to the gate.

The drain current of the device can be recovered to its initial value only if the surface positive charge will be recovered. It has been shown that the surface passivation with silicon nitride averts the creation of the virtual gate by minimising the impact of the surface states. The surface passivation with SiN prevents the current collapse by the following possible mechanisms [33]:

- The passivation buries the surface states, thereby making them unreachable for electrons leaking out of the gate.
- During passivation, Si is incorporated as a shallow donor at the surface of the AlGaN barrier which replaces the surface states.

For power switching devices the current collapse was observed after application of high drain voltage during off-state and strongly depends on the electric field profile [103]. The off-state electric field of a conventional GaN HEMT is strongly peaked at the drain side of the gate. It has been shown, that electrons injected from the gate electrode ($V_{GS} \leq V_{TH}$) under high drain bias can be accelerated by this high electric field and subsequently trapped by surface states and traps/defects in bulk GaN. In order to suppress this phenomenon, application of field plate engineering has been reported [103]. Introduction of field plate mitigates off-state electric field crowding at the drain side of the gate and thereby minimizes the current collapse and enhances the power efficiency [103].

2.6 Gate leakage current and breakdown mechanism

2.6.1 Schottky gate leakage

For a power switching transistor, it is essential to keep the gate leakage at minimum, especially when employed in circuits and systems which require high reliability and negligibly low off-state power consumption. The off-state gate leakage current is measured between the drain and gate. It depends on the strain of the barrier layer, temperature, and the vertical electrical field at the drain-edge of the gate [15, 36, 37, 38]. It has been proposed that the off-state gate leakage current is determined by two dominant mechanisms in a GaN HEMT. The first one is field-emission tunnelling of electrons from the gate electrode to the semiconductor material. This mechanism prevails at low temperatures (125 – 250 K) and becomes substantial at high drain voltage. Another possible mechanism of off-state gate leakage could be associated with threading dislocations within the AlGaN/GaN heterostructure (for temperatures of 250 to 400 K) [39]. In order to suppress the off-state gate leakage, different techniques have been implemented such as passivation of the semiconductor surface with Si_3N_4 [40], or SiO_2 [41], deposition of a GaN cap layer, as well as employing gate insulation layers (MISFETs) [15].

2.6.2 Breakdown in AlGaN/GaN HEMT

The breakdown mechanism in an AlGaN/GaN HEMT is a complex process which doesn't have a cohesive explanation in the literature. Theoretically, for a GaN based device with gate-to-drain drift length of 1 μm, the electrical breakdown will occur when a drain voltage of around 300 V is applied. However, this theoretical limit has not been reached in a three terminal AlGaN/GaN HEMT. The most common doctrine of the breakdown mechanism discussed in the literature is associated with impact ionisation although other breakdown mechanisms such as thermal runaway are suggested [42]. The impact ionisation in AlGaN/GaN HEMTs is initiated by the electrons injected from the gate, and then under the high electric field they gain enough energy to start ionisation of surrounding atoms [43].

When the HEMT is in the off-state, the gate of the device is reverse biased, i.e. $V_{GS} < V_{TH}$ and therefore the 2DEG beneath the gate is completely depleted of electrons. At this condition the channel of the device is highly resistive and there is no current flowing between the drain and source electrodes. So if at this point the drain voltage starts to increase, then the channel will begin to laterally deplete in the drift region between gate and drain electrodes. The electric charge which has been depleted in this portion of the channel will be reflected on the gate [44]. The resulting electric field distribution is such that the field below the gate is highly crowded at the drain side as shown in Fig. 2.7. It has been widely accepted that this electric field crowding at the drain end of the gate leads to electrical degradation/breakdown of AlGaN/GaN HEMTs [44, 45, 46, 47, 48].

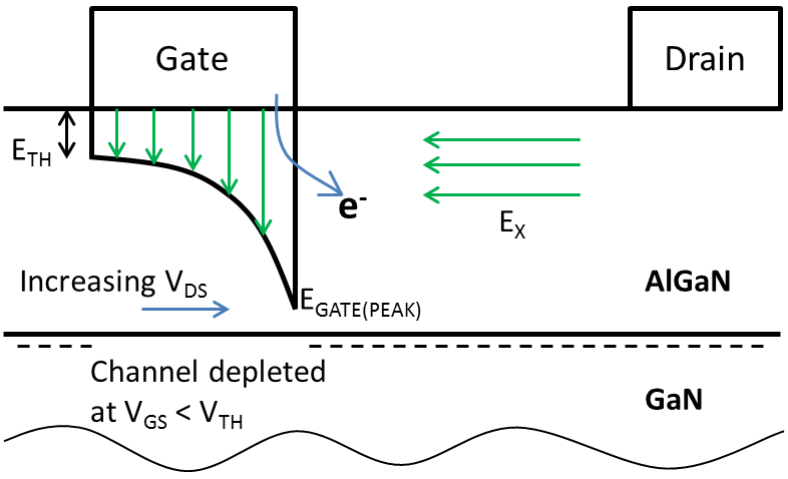


Figure 2.7: Illustration of the simplified electric filed distribution beneath the gate in AlGaN/GaN HEMT.

In several reports [43, 49, 50, 51, 52] the breakdown mechanism in AlGaN/GaN HEMTs is associated with the electrons injection from the gate and their subsequent impact ionisation in the channel. When a positive voltage is applied to the drain of the device under off-state conditions, the electrons will tunnel into the channel from the gate electrode. The gate leakage current arises through thermionic field emission and field-assisted tunnelling [49].

The mechanisms of the breakdown could be summed up in the following:

- Under off-state conditions, electrons are injected from the gate to the channel when a positive voltage is applied to the drain.
- When the voltage applied to the drain is increased to a certain point, the electrons injected into the channel will gain high energies while traveling through high field regions undergo scattering events with bonded electrons in the valence band creating a new electron-hole pair (impact ionisation process). This secondary electron-hole pair can also have a rather high energy. In this case the avalanche effect is triggered and the output current increases instantly.

2.6.3 Electric fields in the depletion region

As mentioned in Section 2.5.2, the electrons injected from the negatively biased gate could be captured by the surface traps and form a virtual gate that can reduce the output drain current of the device. If the gate of the device is biased to pinch-off and the positive drain voltage is applied, then the surface states will be filling up towards the drain. For this reason, the depletion region will laterally extend towards the drain contact. As mentioned in Section 2.3.2, the surface traps are the source of free charge carriers which form the 2DEG. When the traps are occupied with the electrons leaking from the gate, the channel is depleted in order to maintain the neutrality of the system. The resulting electric field in the depletion region includes a vertical polarisation induced field E_P (which depends on the polarisation properties of the material) and a lateral electric field which is given by $E_X = V_{GD} / L_{GD}$ (where L_{GD} is the gate-to-drain drift length) [53]. Then the critical electric field in the depletion region can be defined by [53]:

$$E_C = \sqrt{E_{XC}^2 + E_P^2} \tag{2.12}$$

where E_{XC} is the average breakdown field which is given by [53]:

$$E_{XC} = \frac{V_{BR}}{L_{GD}} \tag{2.13}$$

Since the vertical polarisation field is material dependent, the aspect which can improve the device performance (during the device design) is E_{XC}.

2.7 Substrates for AlGaN/GaN HEMTs

Metal organic chemical vapour deposition (MOCVD) or molecular beam epitaxy (MBE) techniques are used to grow the III-nitrides. Today, the growth of GaN-based epi-structures by MOCVD is the most widely used technique due to the experience and success of the method for development of optoelectronic devices, and relatively high growth rates which are typically about 2 μm/hour. MOCVD growth of GaN is carried out at temperatures ~ 1000 – 1100 °C and involves a chemical reaction of gaseous reactants (trimethylgallium $Ga(CH_3)_3$ and ammonia NH_3) which takes place when they flow above a heated substrate to create a layer of GaN [54]. MBE is the second most frequently used method to grow III-nitrides. MBE growth of GaN is typically carried out in an ultrahigh vacuum at temperatures of about 800 °C and based on reaction of a Ga molecular beam and a nitrogen beam which are directed towards a heated substrate. The advantages of GaN growth by MBE is very precise definition of the interfaces and better flexibility of the interface polarity [54], however these advantages are offered at the cost of decreased growth rates which is typically in the range of 0.5 – 1 μm/hour. III-nitride epilayers are commonly grown on foreign substrates such as SiC, Si, and sapphire on account of the difficulty and high costs and relatively smaller sizes of native GaN substrates.

The choice of the substrate material for device processing is based on the following properties: thermal conductivity, lattice mismatch, coefficient of thermal expansion (CTE), electrical resistivity, thermal boundary resistance and cost. High thermal expansion coefficient and lattice mismatch between the substrate material and GaN results in high density of crystallographic defects, which affect the performance of the device. In order to reduce these mismatches, a nucleation layer is commonly introduced between GaN and substrate, which elevates the thermal boundary resistance and therefore degrades the heat extraction from the device.

Substrates with higher thermal conductivities provide better heat extraction from the channel and thereby improve the device performance. Table 2.1 shows some of the key properties of various substrate materials used for development of AlGaN/GaN HEMTs [55].

Table 2.1: Properties of various substrate materials used for c-plane GaN semiconductors [55]

	Sapphire c-plane	**6H-SiC**	**Si**	**Diamond**	**GaN**
Thermal conductivity, (W/m·K)	35	490	149	>1000	130
Electrical resistivity (Ω·cm)	10^{17}	10^{4}-10^{6}	2.3x10^{4}	10^{13}-10^{16}	10^{6}
Young's modulus (GPa)	325±75	545±155	130	1100	190±110
Lattice mismatch	16%	3.5%	-17%	11%	0%
Thermal expansion coefficient mismatch	34%	25%	56%	73%	0%

Sapphire

Sapphire (Al_2O_3) substrates have been used for epitaxy of GaN since 1969when the first deposition of GaN using hydride vapour-phase epitaxy was achieved by Maruska and Tietjen [56]. Even though, the crystal quality at that time was very poor up to date sapphire remains the substrate for epitaxy of GaN which is commonly used. GaN films can be grown on different sapphire planes – c-plane (0001), a-plane ($01\bar{1}2$), and r-plane ($1\bar{1}02$). The calculated lattice mismatch between the c-plane GaN and the c-plane sapphire is larger than 30%. However, the actual mismatch is smaller (~ 16%) because the small cell of Al atoms on the c-plane sapphire is oriented 30° away from larger sapphire unit cell [18].

GaN grown on the ($11\bar{2}0$) a-plane is (0001) oriented and anisotropically compressed. The in-plane relationship of GaN and sapphire is such that the [$11\bar{2}0$] direction of GaN is aligned with the [0001] direction of sapphire. In this orientation, the bulk positions of both the substrate and the GaN cations lie along the sapphire [0001] direction. The mismatch between the substrate and film is 2% and for the GaN [$1\bar{1}00$] direction parallel to the sapphire [$1\bar{1}00$] is -0.5% [18].

GaN films have also been grown on the r-face ($1\bar{1}02$) of sapphire to achieve smaller lattice mismatch than on the c-plane sapphire. Flms grown on the r-face

assume the $(2\bar{1}\bar{1}0)$ orientation. The lattice mismatch between the $[1\bar{1}01]$ direction of sapphire and [0001] direction of GaN parallel to the sapphire $[1\bar{1}01]$ direction is 1%. In the case when the $[1\bar{1}00]$ direction of GaN is parallel to the sapphire $[11\bar{2}0]$, the lattice mismatch is 16%. Growth on the r-face exhibits ridge-like features that allow relaxation of the mismatch [18].

The lattice mismatch (~16%) between c-plane sapphire and c-plane GaN results in high concentration of dislocations ~10^{10} cm^{-2} which leads to reduction in charge carrier mobility and thereby degrades the device performance [121]. Another limitation of sapphire is that it has a low thermal conductivity (35 W/m·K) and as a result the output saturation current of a GaN-on-sapphire HEMT can be reduced due to self-heating. Even though these drawbacks of sapphire have significantly relegated its use, sapphire substrates are still used for the device processing due their low cost.

Silicon

The (0001) GaN can be grown on the (111) Si substrates. Low cost and the availability of large diameter wafers make Si one of the most attractive choices for GaN epitaxy. Another appealing factor is the possibility of using a standard Si CMOS processing facility for fabrication of GaN devices. The thermal conductivity of Si (149 W/m·K) is higher than that of sapphire and similar to the thermal conductivity of bulk GaN, but still lower than the thermal conductivity of SiC (490 W/m·K). The limitations of Si include large lattice mismatch (17 %) which leads to high dislocation density and thermal expansion coefficient mismatch (56 %) which can result in cracking of GaN-layers during cooling process. These drawbacks impede the growth of GaN-on-Si epistructures of high quality.

Silicon carbide

SiC possesses a number of appealing properties for epitaxy of GaN. First of all, SiC has a similar to GaN wurtzite crystal structure with the smallest lattice mismatch (3.5 %) among the other foreign substrate material used for GaN epitaxy. For this reason, the growth of GaN-on-SiC epi-structures of high quality is easier and requires only a thin AlN nucleation layer which has a lattice mismatch to SiC of less than 1 %. However, the density of misfit dislocation in the GaN layer is still

significant (10^6 – 10^8 cm^{-2}), which can lead to early degradation of the device (reduction of maximum drain current, generation of traps, increase of gate-lag) [102]. Also, SiC has a relatively high thermal conductivity (490 W/m·K) and for this reason SiC substrates are presently the most efficient for extracting the heat from the channel of high power AlGaN/GaN HEMTs. However, degradation (reduction of transconductance and drain current, and an increase of on-state resistance) of AlGaN/GaN HEMTs due to elevated temperature at high drain voltage operation has been reported even on SiC substrates [57], therefore substrates with higher thermal conductivity such as diamond (> 1000 W/m·K) are desirable.

Diamond

Diamond is the most thermally conductive material found in nature. Growth of GaN on crystalline diamond and polycrystalline diamond is inherently difficult due to a large lattice mismatch (~11%) between the two materials which will likely generate mismatch defects and lead to poor crystal quality [122]. Other drawbacks are the large thermal expansion coefficient mismatch (~73%) which could lead to cracking of the GaN-layers and the absence of a fixed epitaxial relationship between the GaN and a polycrystalline diamond substrate making the nucleation of continuous epitaxial GaN layers problematic. Recently it has been shown that the lack of epitaxy and lattice mismatch can be partially overcome by growing GaN on polycrystalline diamond substrate by MOVPE with a low-temperature AlN nucleation layer (dislocation density ~$7x10^9$ cm^{-2}) [122]. The thermal conductivity of diamond is more than three times greater than that of SiC [59], which makes diamond substrates very appealing choice to address the heat spreading issues and for the development of AlGaN/GaN HEMTs for ultra-high power density applications. For this reason, this area of research is gaining more interest and several reports investigating the performance of GaN-on-diamond substrates have been published [58, 59, 60, 61, 62]. It has already been shown through simulation and experimental demonstration that GaN-on-Diamond platform can significantly outperform GaN-on-SiC platform for Radio Frequency (RF) applications by reducing thermal resistance and thereby increasing power density [104, 105, 106]. Fig. 2.8 shows that with GaN-on-Diamond wafers, a nearly threefold improvement in RF power density could be achieved for a given channel temperature when compared to GaN-on-SiC [107]. Therefore, diamond substrates can substantially

increase the power density and reliability of the devices. It should be noted that most of the work which has been accomplished on GaN-on-Diamond to date has been primarily focussed on RF devices. In this work an effort to realise the first high-voltage GaN-on-Diamond power device was undertaken. The GaN-on-Diamond samples (10x10 mm) used in this work were supplied by element six, although there is no specific information on material quality provided by supplier it is expected to be poor since the samples were produced in late 2013.

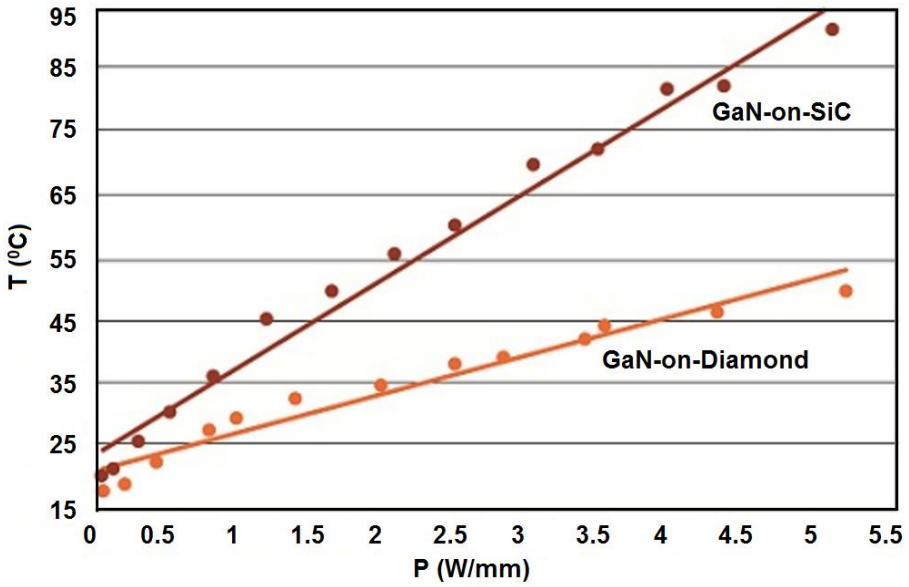


Figure 2.8: Peak channel temperatures of GaN-on-SiC and GaN-on-Diamond HEMTs with gate width of 2x10 µm [107].

2.8 Summary

This chapter provides a summary with material properties of III-nitrides, polarisation and 2DEG formation mechanisms, metal contacts, operation principles of high power AlGaN/GaN HEMTs and with some of the main challenges (current collapse and premature breakdown) associated with their design and fabrication. The substrate choice is discussed. GaN-on-Diamond platform is the most promising technology for high power density applications, therefore these particular wafers will be used in this work. All information gathered in this chapter will be used in consequent realisation of high-voltage GaN-on-Diamond power semiconductor devices.

Chapter 3

Numerical Simulations of AlGaN/GaN HEMTs

3.1 Introduction

The technology for developing Group III-nitride based power semiconductor devices such as AlGaN/GaN HEMTs from the perspective of maturity of a semiconductor technology can be considered to be in a nascent stage. For this reason, a reliable assessment of their performance and a comprehensive understanding of the physical characteristics obtained from experimental work is relatively limited (unlike Silicon (Si) based technologies). Since the physical realisation and undertaking experimental work (design to manufacture) in this area is expensive and time consuming, a reliable and economical method to predict the performance of a device in a short time is essential for GaN device designers. The most common tools used for device design and performance prediction are the physics-based simulators. Although the device simulation is still challenging in the case of GaN devices, it can provide critical insight into the electrical, thermal and optical behaviour of the device under various operational conditions.

This chapter will provide an overview of the physics-based simulations of AlGaN/GaN HEMTs that were carried out during this study. The simulation results aided the actual design of the high voltage devices which were also subsequently fabricated and characterised in detail. An innovative concept employing non-uniform field plate architecture for enabling high voltage AlGaN/GaN HEMTs has also been introduced and described in this chapter. Based on simulation results, the novel structure can substantially enhance the breakdown voltage of the device, compared to conventional devices employing standard uniform field plates.

3.2 Simulation structure of an AlGaN/GaN HEMT

Simulations of AlGaN/GaN HEMTs were carried out using physics-based device simulation software Silvaco “Atlas”. The list of the statements, models, and numerical method used in the script have been summarised in Table 3.1 [63].

Table 3.1: List of models and numerical methods used in the simulation script [63].

Statement:	Description
DOPING TRAP	Designates that the doping concentration will be considered as a density of trap states.
INTTRAP	Actuates trap states at the interface and specifies their energy levels
Models:	
CONSRH	Signifies that model used to describe recombination is Shockley-Read-Hall with concentration dependent lifetimes.
AUGER	Specifies Auger recombination.
FERMIDIRAC	Signifies that Fermi-Dirac carrier statistics being used.
POLARIZATION	Automatically calculates the interface charge induced by piezoelectric and spontaneous polarization
POLAR.SCALE	Sets a scale factor for piezoelectric and spontaneous polarization charges.
CALC.STRAIN	Calculates the strain in the specified region induced by adjacent regions due to lattice mismatch.
ALBRCT.N	Enable the Albrecht mobility model.
GANSAT.N	Signifies that model used for electron mobility is the Nitride Field Dependent.
LAT.TEMP	Includes the lattice temperature model.
Numerical method:	
NEWTON	Signifies that the used solution method is Newton.

The cross-sectional schematic of the simulated GaN HEMT is shown in Fig. 3.1. The epi-layer structure consists of SiN (50 nm), unintentionally doped $Al_{0.26}GaN_{0.73}N$ barrier layer (20 nm) and unintentionally doped GaN buffer layer (800 nm). This epi-structure corresponds to the GaN-on-diamond epi-wafers used for further device processing with some exceptions: adhesion layer (53 nm), substrate (95 μm) and a thin GaN cap layer (2.5 nm) are not included into the structure. The composition of adhesion layer is covered by IP.

One of the most important steps in device simulation is specifying an appropriate mesh. Mesh density should be very fine in the critical regions of the structure (i.e. heterojunctions, interfaces, regions where high electric field is expected) so as to improve the accuracy of the simulation. On the other hand, a mesh with fewer nodes should be used in the less critical regions in order to increase the

numerical efficiency. Fig. 3.2 illustrates a typical mesh used for the simulation of GaN HEMT (Fig. 3.1).

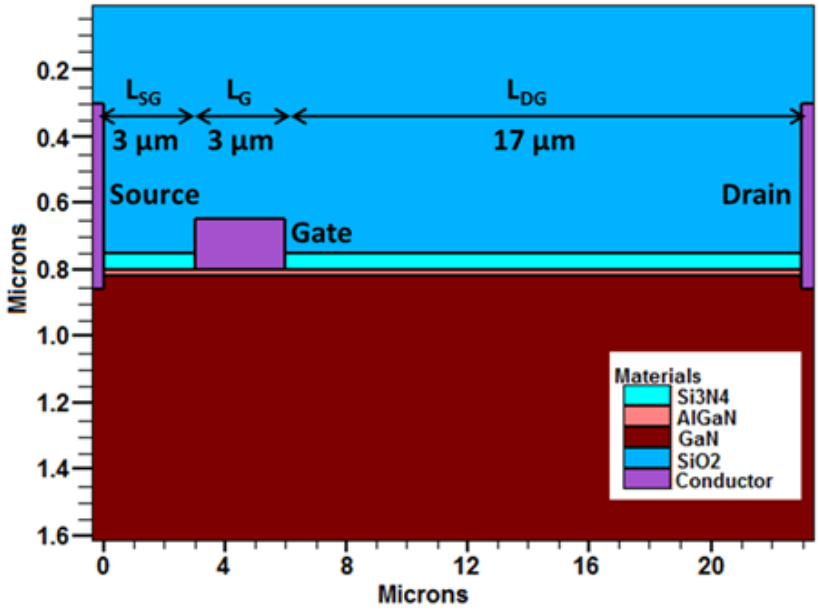


Figure 3.1: Cross-sectional schematic of the simulated AlGaN/GaN HEMT (gate width W_G = 50 µm).

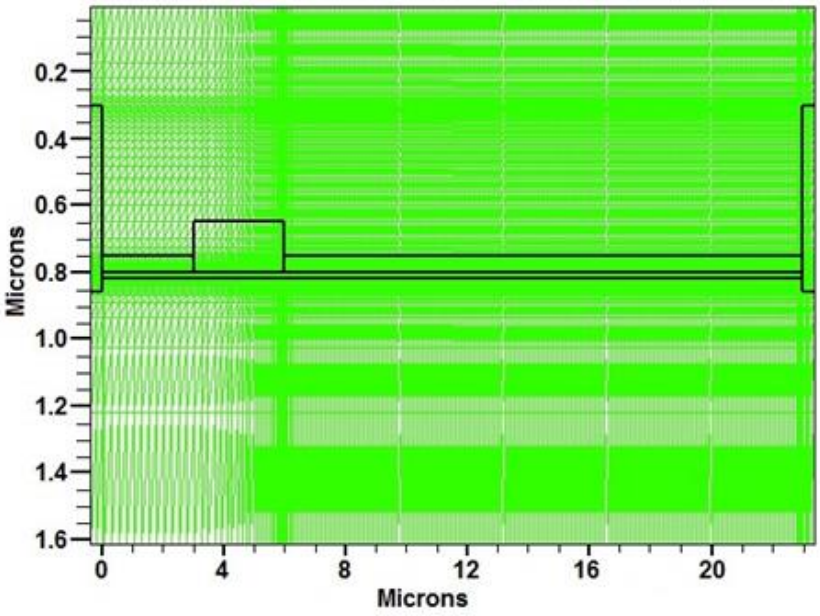


Figure 3.2: Mesh of the simulated structure (see Fig. 3.1).

Fig. 3.3 demonstrates schematics of electron concentration and energy band diagram of the simulated GaN HEMT under thermal equilibrium. The concentration of acceptor and donor traps in AlGaN/GaN layers was set to 5e16 cm^{-3} and 1e17 cm^{-}

^{3} respectively. The conduction band exhibits a triangular quantum well which leads to 2DEG formation with a sheet carrier concentration of ~ 1e13 cm^{2}.

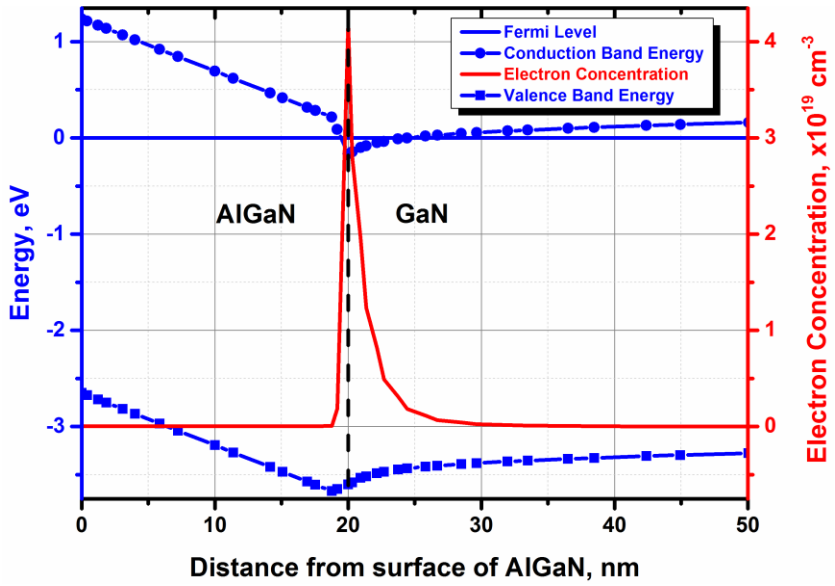


Figure 3.3: Energy band diagram and electron concentration of the simulated AlGaN/GaN HEMT.

3.3 Transfer and output I – V characteristics

Fig. 3.4 shows simulated transfer current-voltage characteristics of the AlGaN/GaN HEMT. The threshold voltage (V_{TH}) is found to be ~ - 3 V and can be controlled by density of acceptor-like traps (i.e. defects in the bulk GaN).

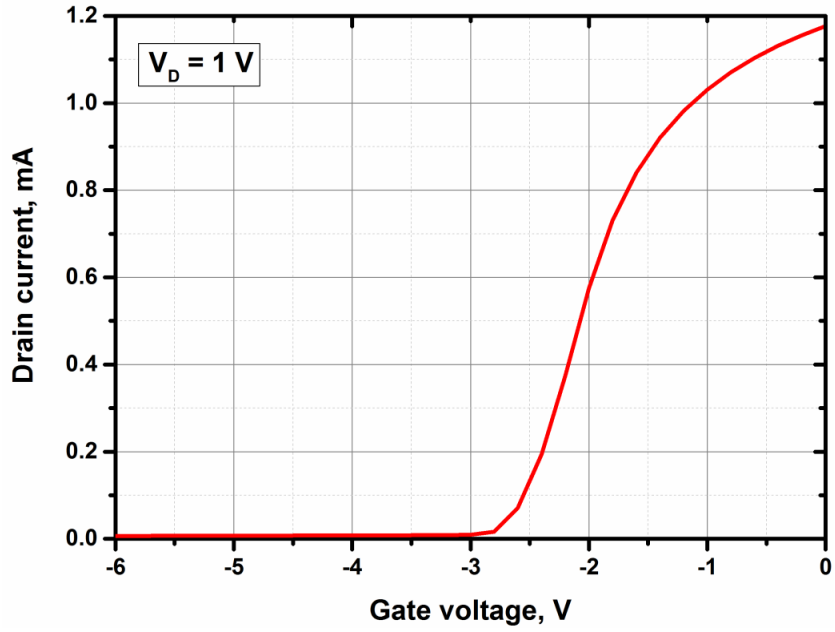


Figure 3.4: Simulated transfer current-voltage characteristic of the GaN-based HEMT (Fig. 3.1)

Output current-voltage characteristics are shown in Fig. 3.5. The calculated specific on-state resistance ($R_{ON}.A$) is found to be ~ 9.5 $m\Omega.cm^2$. Fig. 3.6 illustrates the electron distribution at different gate bias conditions. 2DEG is depleted under the gate electrode when $V_{GS} \leq$ -3 V (Fig. 3.6, a-b), and the channel is formed at V_{GS} > -3 V (Fig. 3.6, c-d).

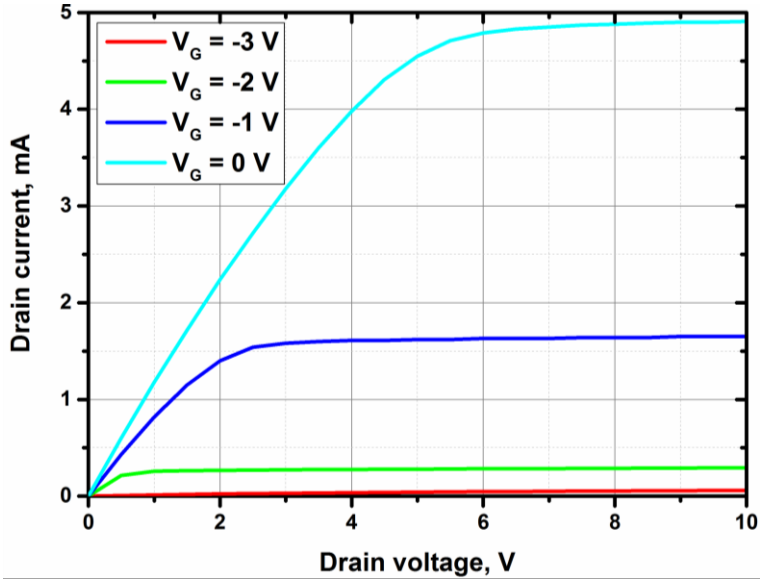


Figure 3.5: Simulated output current-voltage characteristics of the GaN-based HEMT (Fig. 3.1)

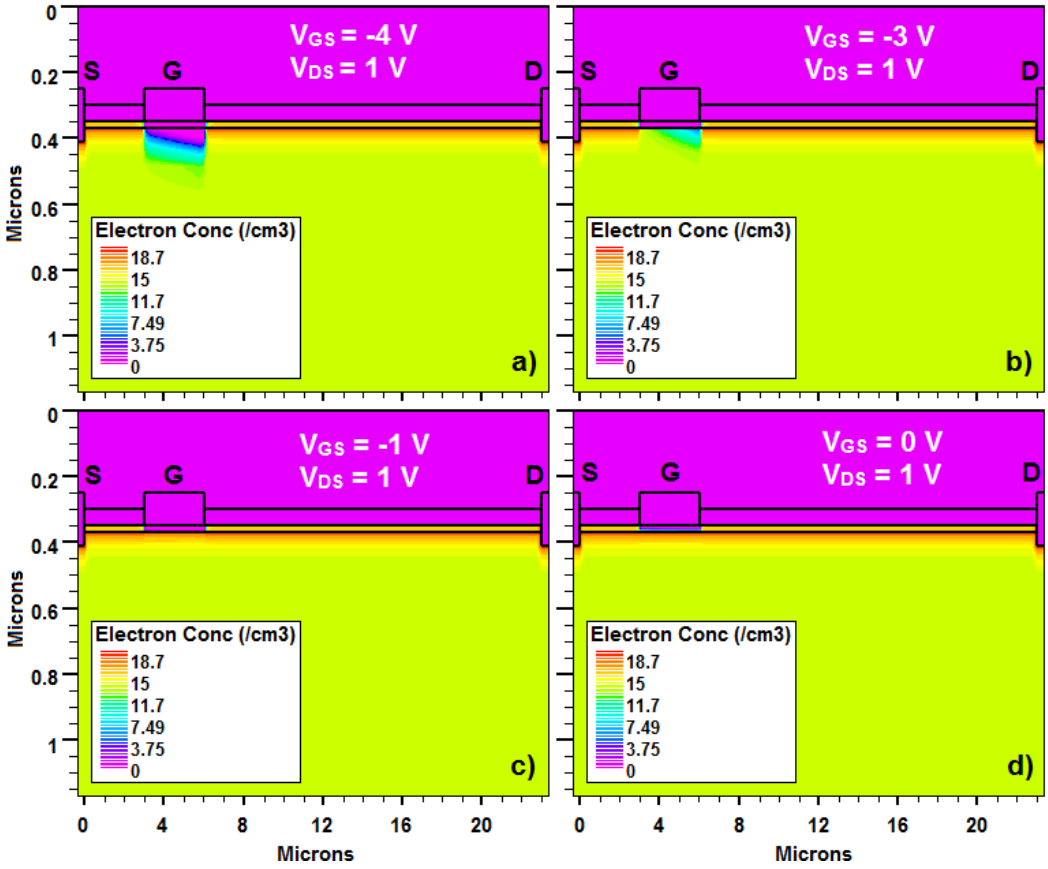


Figure 3.6: Electron concentration schematics of the simulated AlGaN/GaN HEMT at different V_{GS}.

3.4 Breakdown voltage simulation

In Section 2.6.2 it has been shown that the electric field crowding at the drain-side edge of the gate occurs during off-state of a GaN-based HEMT and how this could result in early device breakdown. In this section the simulated distribution of the electric fields for different AlGaN/GaN HEMT structures will be shown. In order to simulate the off-state breakdown of the device **`IMPACT SELB`** model has been used in the simulation script which sets the Selberherr's impact ionization model [63].

3.4.1 AlGaN/GaN HEMT without field plate

The simulated electric field distribution at the moment of the off-state breakdown for an AlGaN/GaN HEMT is shown Fig. 3.7. When the HEMT is in the off-state, the gate of the device is reverse biased, i.e. $V_{GS} < V_{TH}$ and therefore the 2DEG beneath the gate is completely depleted of electrons. At this condition the channel of the device is highly resistive and there is no current flowing between the drain and source electrodes. So if at this point the drain voltage starts to increase, then the channel will begin to laterally deplete in the drift region between gate and drain electrodes. The electric charge which has been depleted in this portion of the channel will be reflected on the gate [44]. The resulting electric field distribution is such that the field below the gate is highly crowded at the drain side as shown in Fig. 3.7.

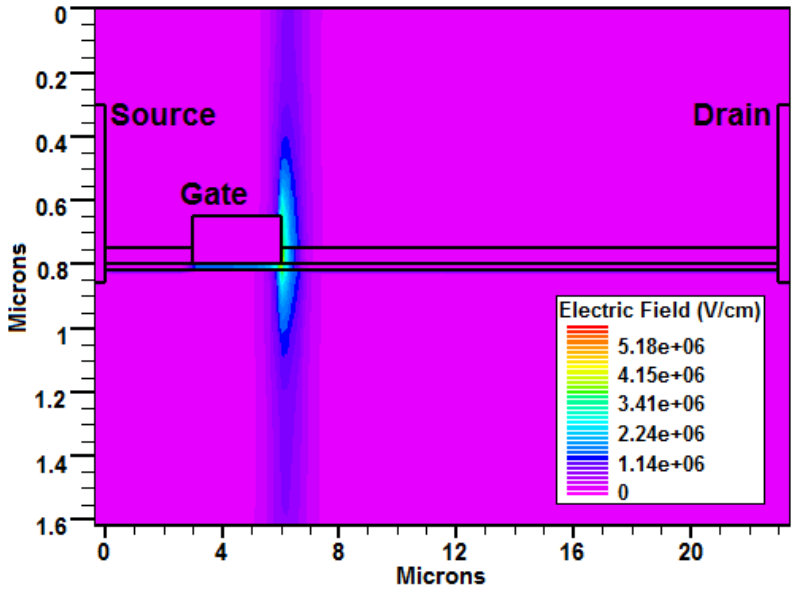


Figure 3.7: Distribution of the electric field at the moment of device breakdown.

Fig. 3.8 shows distribution of the electric field along the electron channel as extracted from the simulations of the AlGaN/GaN HEMT structure (see Fig. 3.7). It is apparent that the electric field is confined within a small range from the drain-side edge of the gate. Therefore, the critical electric field (~ 3 MV/cm) can be reached even for low drain bias which leads to low breakdown voltage. The breakdown voltage (V_{BR}) for this structure is found to be ~ 160 V (Fig. 3.9).

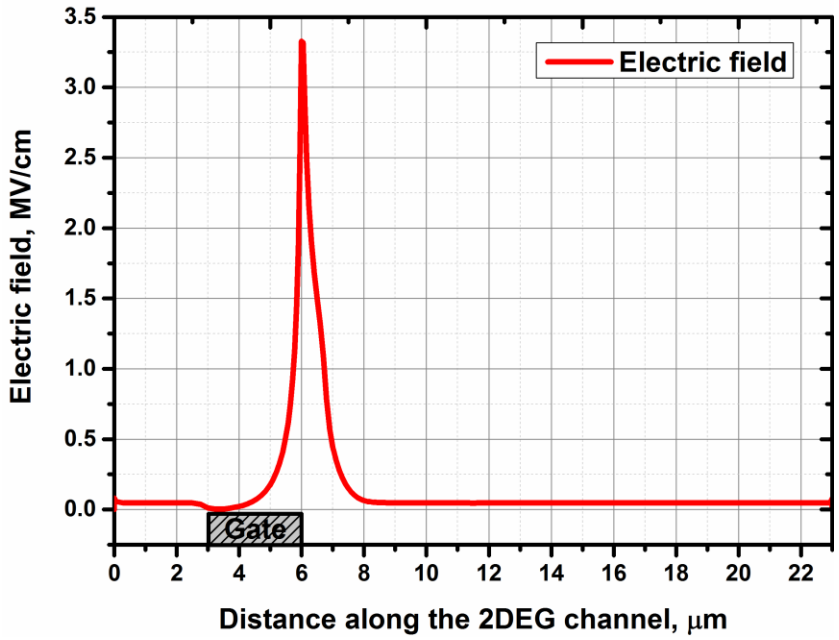


Figure 3.8: Simulated distribution of the electric field along the electron channel of the GaN HEMT on the verge of the device breakdown.

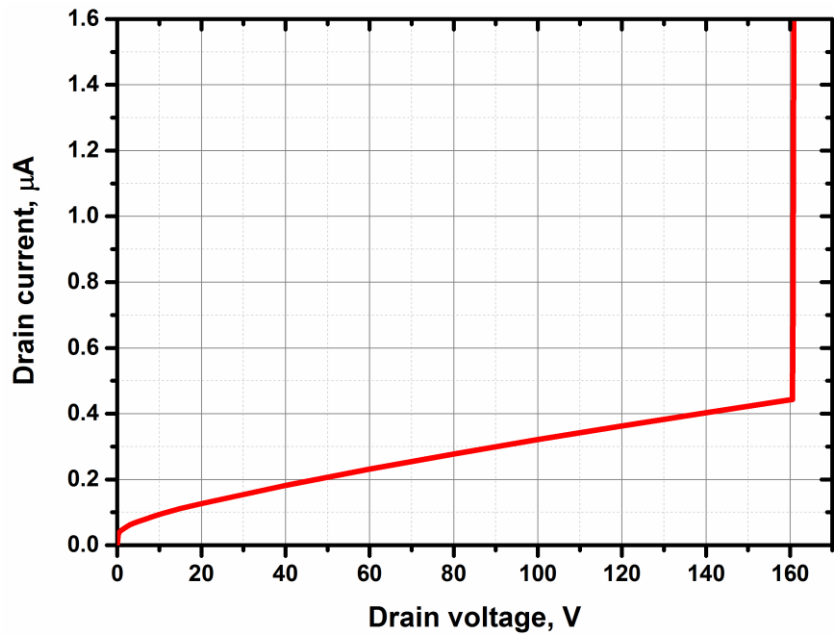


Figure 3.9: Simulated off-state I_D - V_D characteristic.

3.4.2 AlGaN/GaN HEMT with source field plate

Many researchers have used field plates as a tool to enhance breakdown voltage of the devices by decreasing the electric field crowding at the drain-side edge of the gate [64, 110]. The breakdown voltage is due to an avalanche process that usually occurs near the gate edge on the drain side. It is generally accepted that the essence of achieving a high breakdown voltage in a HEMT is to have an increasing depletion width at the surface of the channel from the drain to the Schottky gate [110]. When the field plate is used in a HEMT, the electric field originating from the overlapping portion of field plate contributes to the formation of the depletion region in the passivation and conducting channel layers between the gate and drain. This is equivalent to providing additional trapped charge at the surface of the channel, resulting in a lower electric field peak at the drain-side-edge of the gate [110].

Fig. 3.10 illustrates the simulated electric field distribution at the moment of the off-state breakdown for GaN-based HEMTs with various source field plate (SFP) lengths (L_{FP} = 2, 3, 4, and 11 μm), while the other dimensions of the structure are kept the same as shown in Fig. 3.1. 50 nm of SiN and 450 nm of SiO_2 were used as the dielectrics under the field plate since they provide high dielectric constants (ε_{SiN} = 7.5, ε_{SiO} = 3.9) and high breakdown strength (~ 10 MV/cm for both SiN and SiO_2). Thin SiN layer was used in the simulation in combination with thick SiO_2 layer because it is not recommended to use thick SiN layer due to the risk of cracking during fabrication.

Fig. 3.11 shows the electric field distribution along the electron channel as extracted from the simulation of the device structures with various source field plate lengths (see Fig. 3.10). It is clear that the electric field is better spread along the channel using this architecture and reaches critical electric field at much higher drain voltages when the field plate is included into the structure [64]. Therefore, the breakdown voltage is increased. The breakdown voltage curves for these simulated structures are shown in Fig. 3.12.

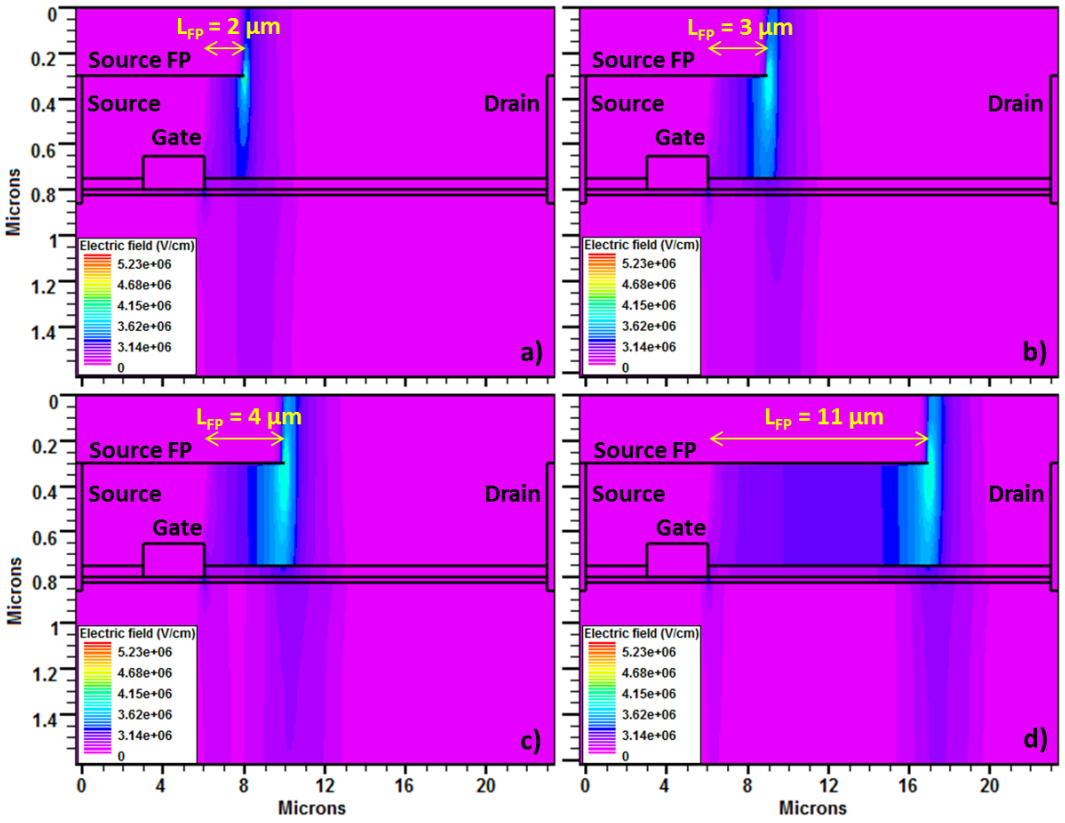


Figure 3.10: Image from Silvaco Atlas showing spreading of the electric field at the moment of breakdown of the devices with SFPs (L_{DG} = 17 µm).

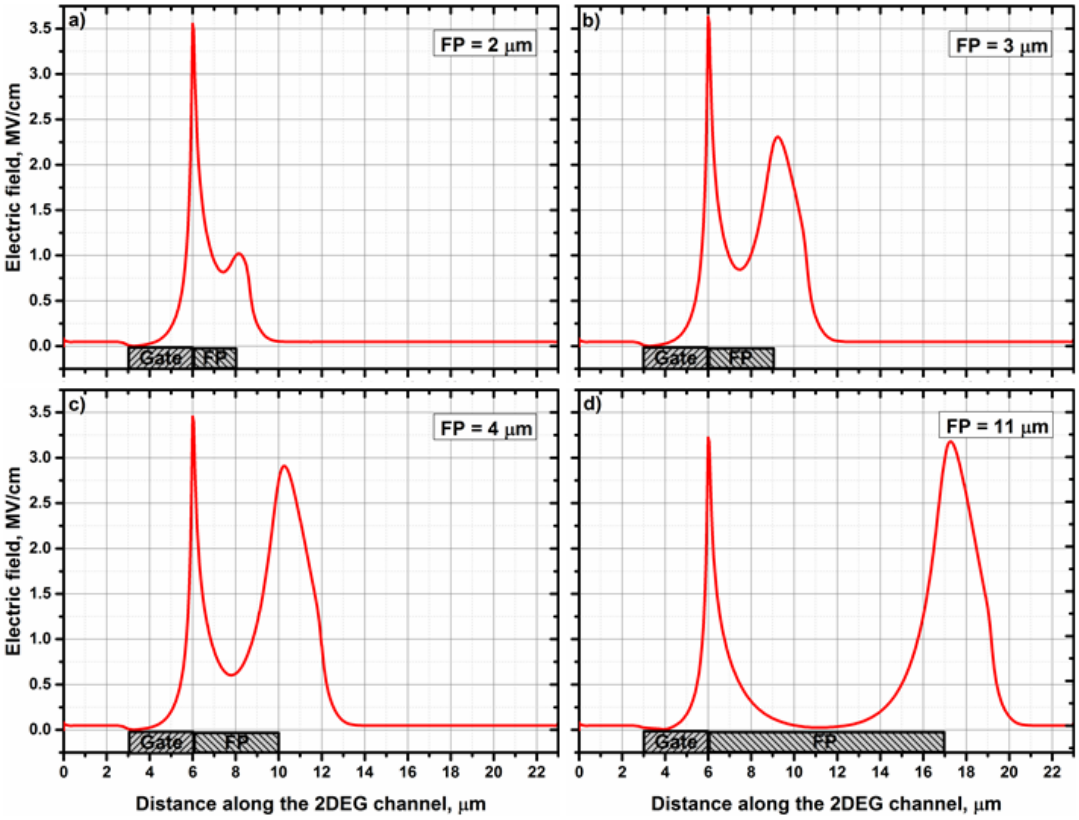


Figure 3.11: Simulated electric field distribution along the channel at the moment of the off-state breakdown of devices with SFPs (L_{DG} = 17 µm).

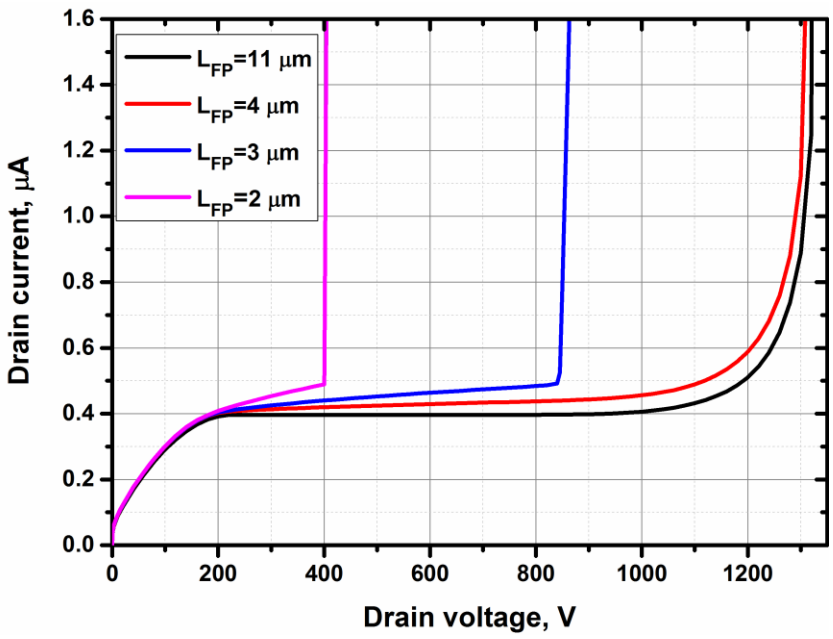


Figure 3.12: Off-state I – V curves for the simulated AlGaN/GaN HEMTs with source field plates.

Fig. 3.13 demonstrates how the breakdown voltage of a GaN-based HEMT (the structure shown in the inset) changes for various lengths of source field plate. It is apparent that the breakdown voltage saturates at a certain length of field plate (L_{FP} = 4 μm). The explanation for this is the fact that the breakdown voltage is the total area of the triangular sections of electric field distribution (see Figs. 3.11, a-d) and the increase in this area saturates as the overlap of the sections reduces with increase in L_{FP} [64].

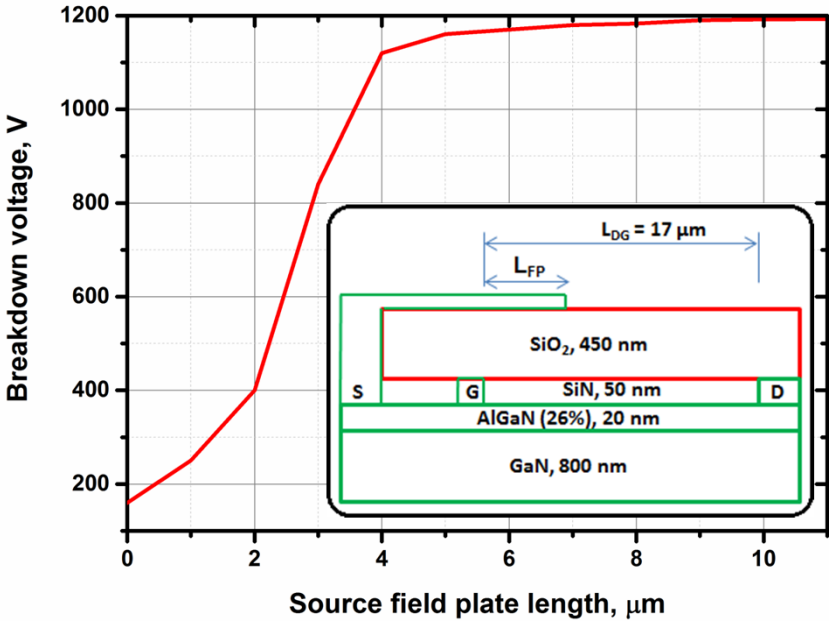


Figure 3.13: Variation of breakdown voltage with respect to length of source field plate (L_{FP}). Inset: simulated device structure.

Fig. 3.14 presents the simulated electric field distribution at the moment of the off-state breakdown for GaN-based HEMTs with source field plate length L_{FP} = 4 µm and various drain-to-gate drift lengths (L_{DG} = 5, 6, 7, and 8 µm), while the other dimensions of the structure are kept the same as shown in Fig. 3.1.

Fig. 3.15 shows the electric field distribution along the electron channel as extracted from the simulations of the device structures with various drain-to-gate drift lengths (see Fig. 3.14). With increase in L_{DG}, the electric field is better spread along the channel and reaches critical electric field at higher drain voltages. The breakdown voltage curves for these simulated structures are shown in Fig. 3.16.

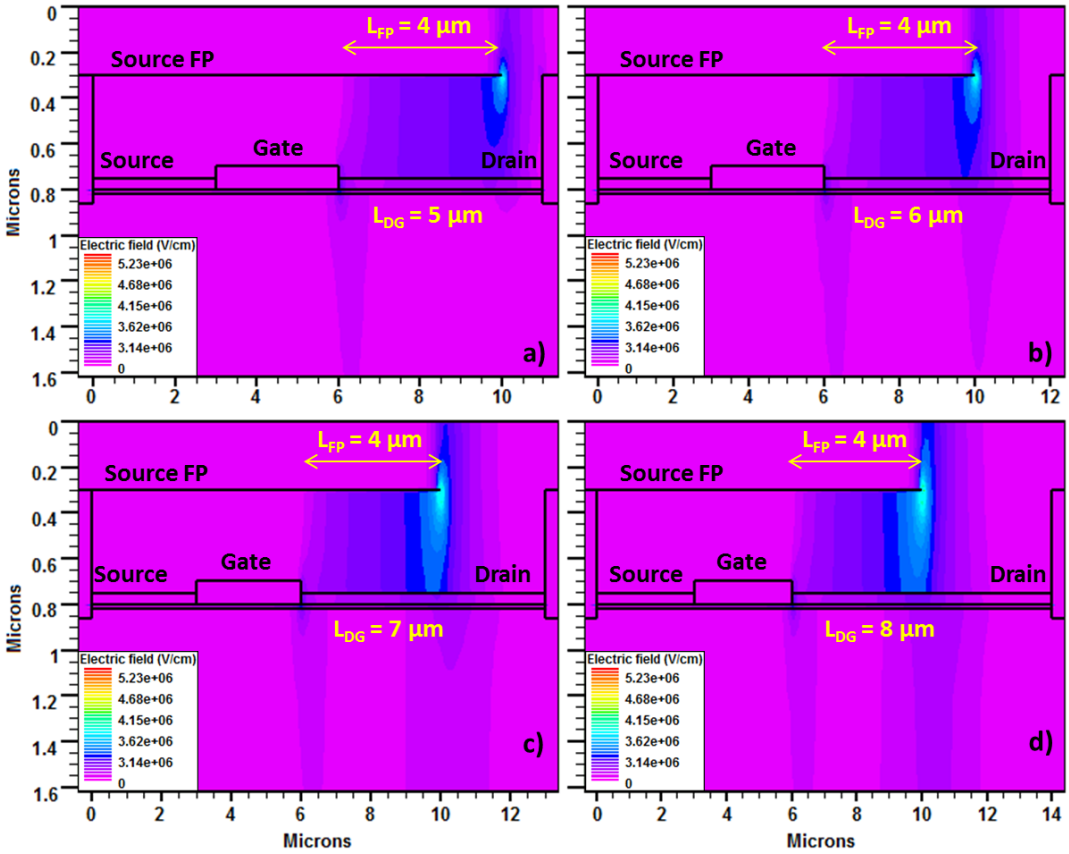


Figure 3.14: Image from Silvaco Atlas showing spreading of the electric field at the moment of breakdown of the devices with different L_{DG}. (L_{FP} = 4 µm).

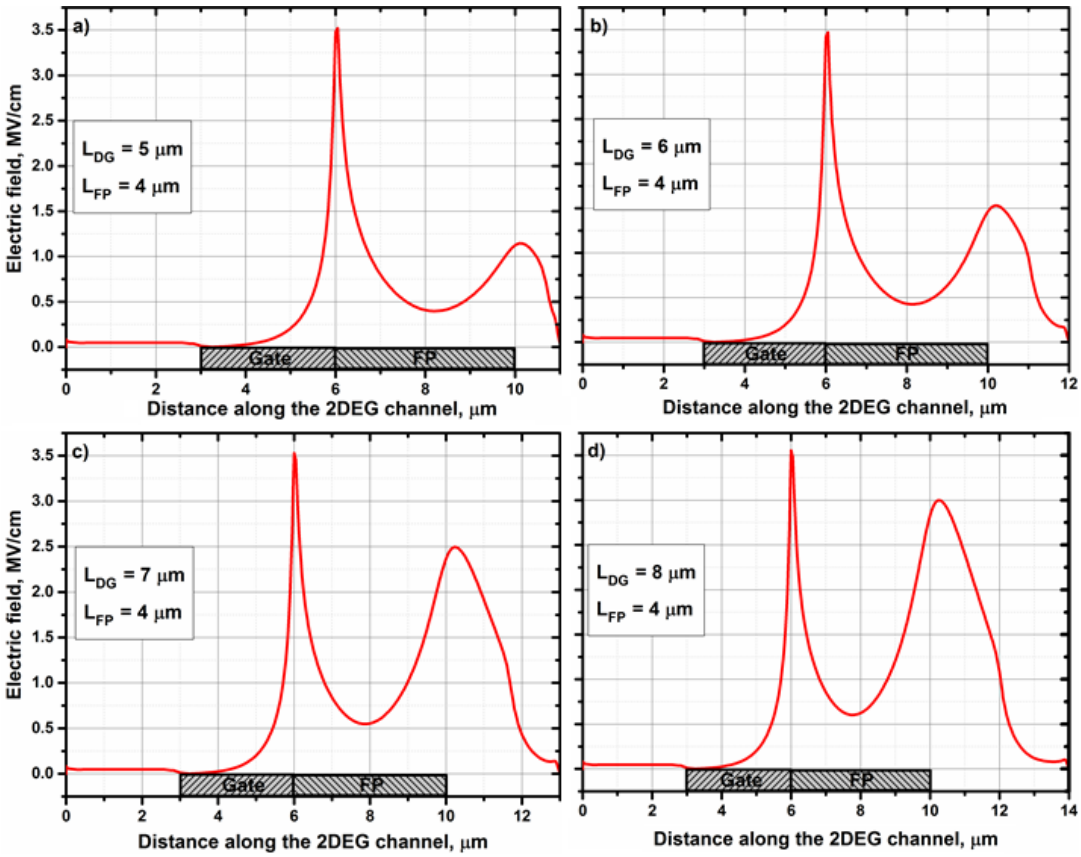


Figure 3.15: Simulated electric field distribution along the channel at the moment of the off-state breakdown of devices with different L_{DG} (L_{FP} = 4 μm).

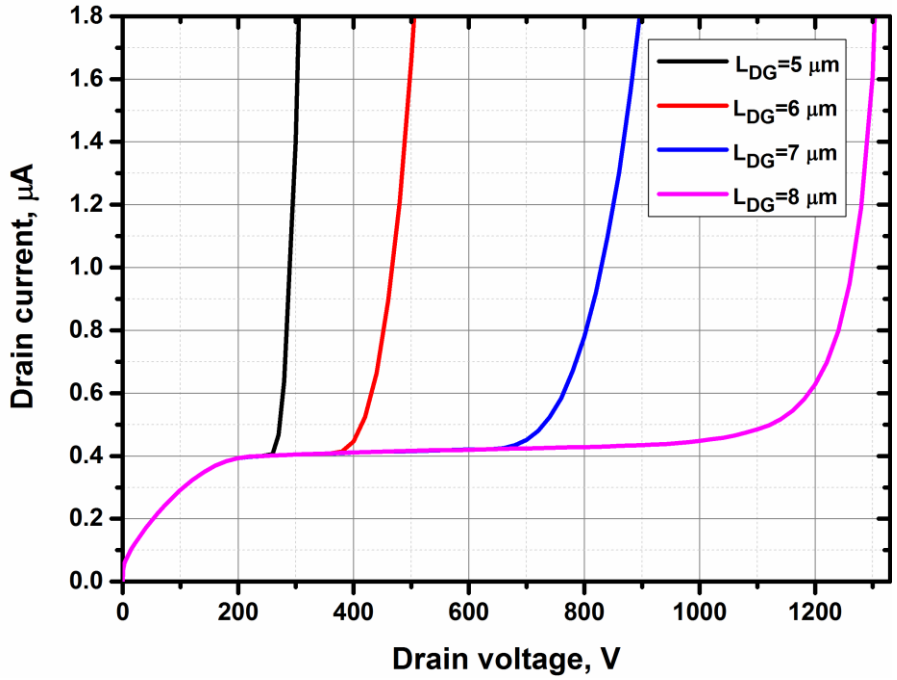


Figure 3.16: Off-state I – V curves for the simulated AlGaN/GaN HEMTs with different L_{DG} (L_{FP} = 4 μm).

Fig. 3.17 reveals how the breakdown voltage of a GaN-based HEMT (the structure shown in the inset) changes with drain-to-gate drift length. It is apparent that the breakdown voltage saturates at L_{DG} = 8 μm (L_{FP} = 4 μm). The saturation of the breakdown voltage can be attributed to the decay of the electric field beyond the edge of the field plate with increase in gate-drain distance [64].

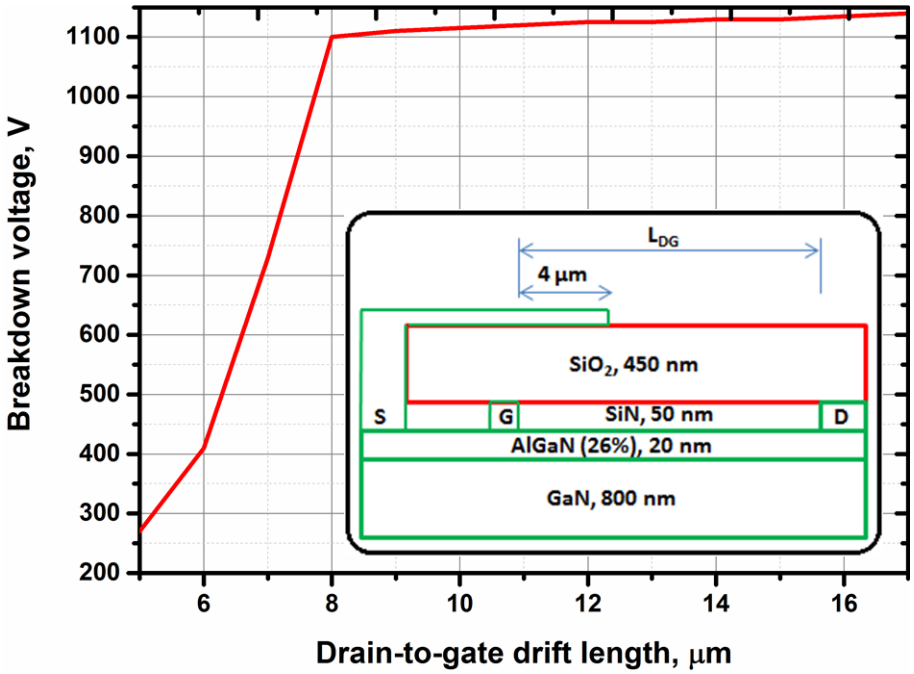


Figure 3.17: Variation of breakdown voltage with respect to drain-to-gate distance. Inset: simulated device structure.

3.4.3 Non-uniform source field plate

From Fig. 3.13 it is clear that after a certain length of source field plate the breakdown voltage saturates and stops improving. In other words, the effectiveness of a conventional field plate is limited. In order to overcome these limitations a new concept of non-uniform source field plate (NUSFP) is introduced in this work. Fig. 3.18 shows novel schematic structure of a GaN-based HEMT with the non-uniform source field plate. As it could be seen, the non-uniform field plate creates several additional metal edges to improve the electric field distribution along the electron channel and hence the breakdown voltage of the device can be enhanced as well.

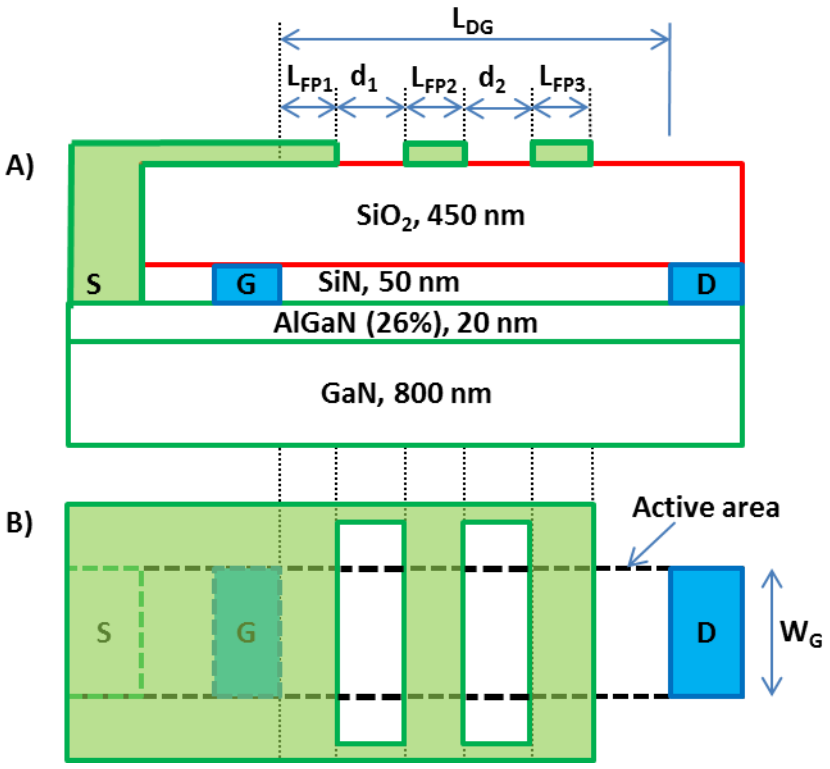


Figure 3.18: A) Schematic illustration of a GaN-based HEMT with non-uniform source field plate; B) view from the top.

Fig. 3.19 demonstrates the simulated electric field distribution at the moment of the off-state breakdown for a device with non-uniform source field plate (L_{FP1} = 3 µm, L_{FP2} = L_{FP3} = 1 µm, d_1 = d_2 = 3 µm, L_{DG} = 17 µm).

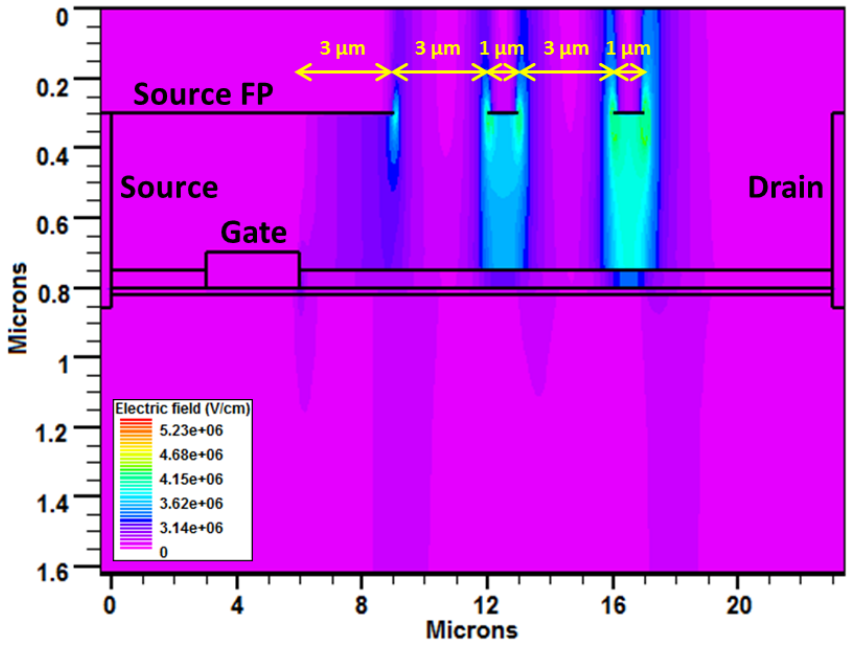


Figure 3.19: Image from Silvaco Atlas showing the electric field distribution at the moment of off-state breakdown of the device with non-uniform source field plate (L_{FP} = 11 µm).

The distribution of electric field along the 2DEG channel at the moment of the off-state breakdown as extracted from the simulations of the device structure with NUSFP with comparison to the device with uniform FP is presented in Fig. 3.20. It is clear that the NUSFP improves distribution of the electric field when compared to conventional uniform field plate. Therefore, the device with non-uniform field plate exhibits higher breakdown voltage.

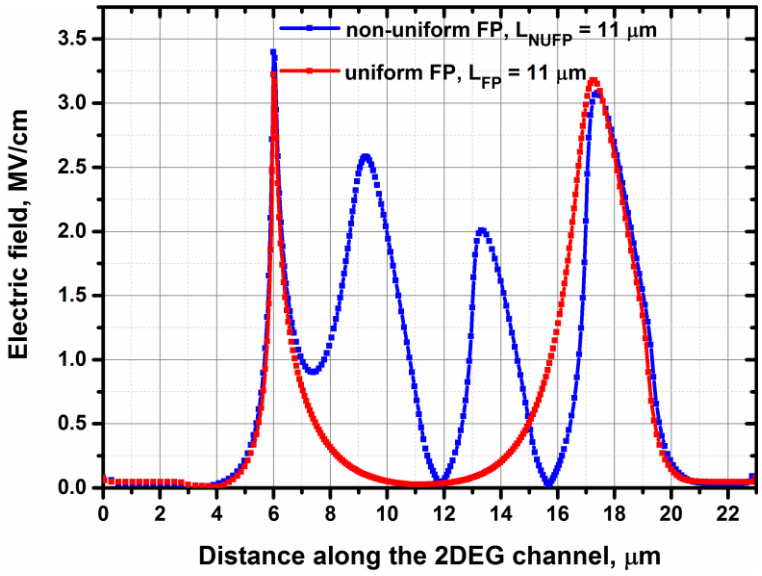


Figure 3.20: Simulated electric field distribution along the channel at the moment of the off-state breakdown of the device with non-uniform source field.

The breakdown voltage for the device structure with NUSFP is found to be V_{BR} ~ 1800 V compared to V_{BR} ~ 1200 V for the structure with uniform field plate of the same length L_{FP} = 11 μm (Fig. 3.21).

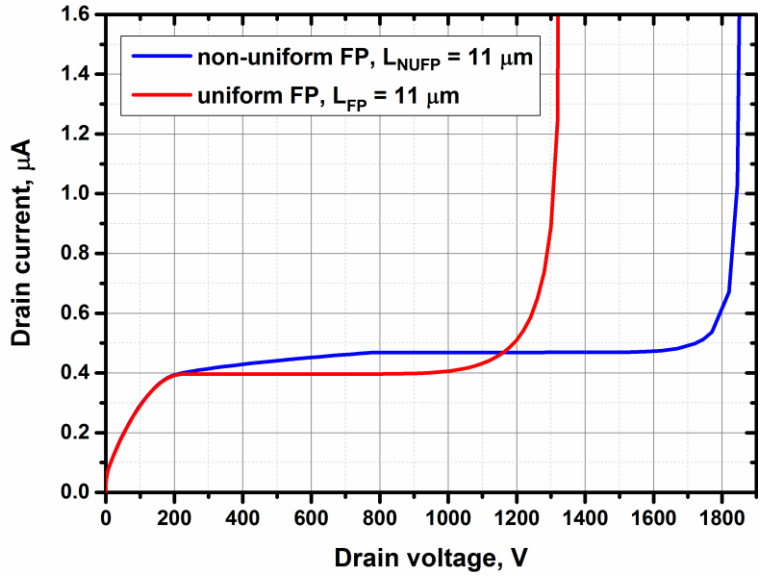


Figure 3.21: Comparison of the off-state I – V characteristics of the GaN HEMTs with non-uniform source field plate and uniform source field plate.

3.5 Conclusions

This chapter has provided an insight on the operating principle, electrical characteristics, and off-state electric field profile along the channel on the verge of breakdown of a typical AlGaN/GaN HEMT by means of physics-based simulation study. The electrical simulation results indicate that the device has threshold voltage of ~ -3 V, specific on-state resistance of ~ 9.5 $m\Omega.cm^2$. The breakdown voltage simulation reveals that the off-state breakdown voltage of the device can be increased with inclusion of source field plate. It has been demonstrated that the breakdown voltage initially increases with FP length and then saturates at L_{FP} = ~ 4 μm (V_{BR} = ~1100 V). In order to overcome this limitation a novel non-uniform field plate structure was proposed. The breakdown voltage of the device with non-uniform FP (L_{FP} = 11 μm) is found to be ~ 1800 V compared to V_{BR} = ~ 1200 V for a device with uniform FP of the same length.

Chapter 4

Device Fabrication of GaN-on-diamond HEMTs

4.1 Introduction

This chapter will describe the mask design and fabrication method of the devices developed during this work. The devices had been designed based on the simulation study described in the previous chapter. The layout schemes adopted for the various devices will be presented initially. Following from that will be a detailed description of the fabrication process-flow developed in this chapter.

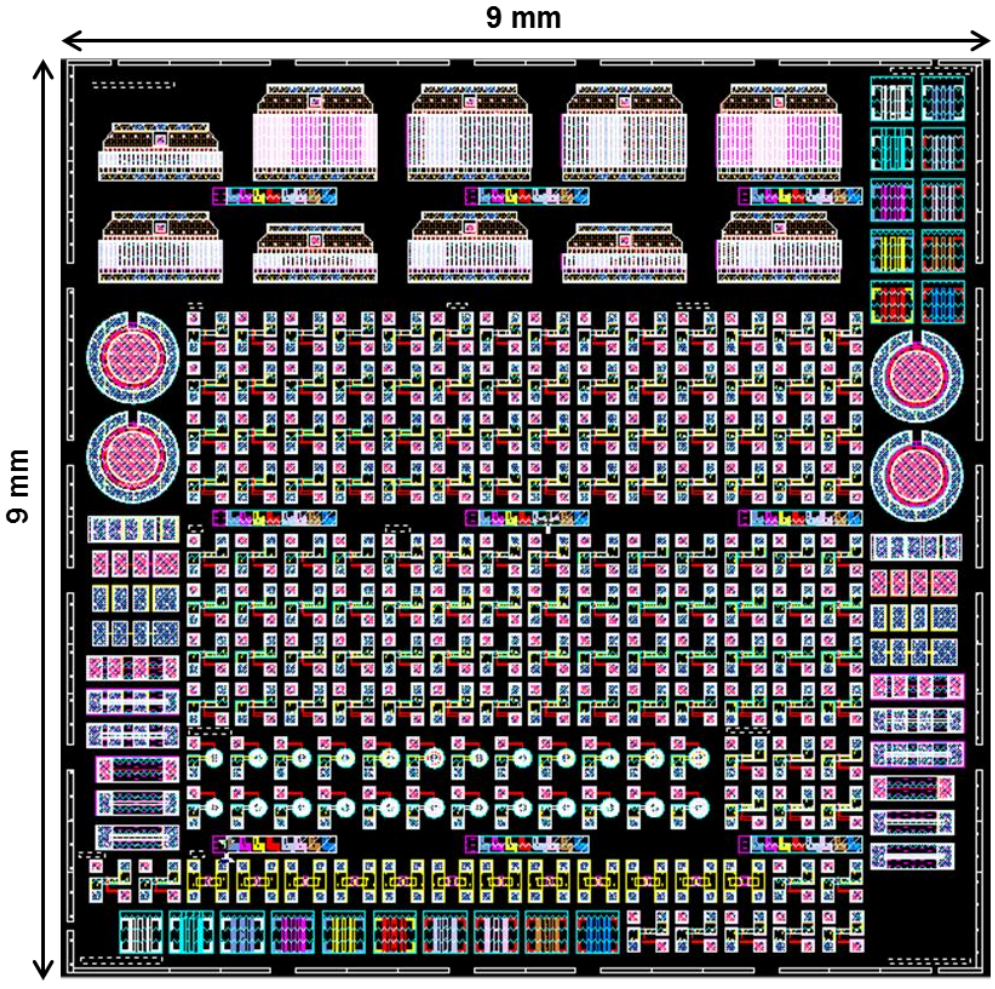


Figure 4.1: Screen shot of the photomask layout.

4.2 Mask Design

Mentor Graphics IC Station software was employed for mask design and the photomasks were fabricated by Compugraphics International Ltd. The fabrication process-flow that was developed required ten photolithography steps (10 masks). Fig. 4.1 shows a snap shot of the photomask that was designed.

Several types of device and process test structures were designed. The list of fabricated devices have been summarised in Table 4.1.

Table 4.1: List of the fabricated GaN-on-Diamond HEMTs.

	Source-to-Gate distance, L_{SG}, µm	Gate length L_G, µm	Gate-to-Drain distance, L_{DG}, µm	Source FP length, L_{SFP}, µm	Drain FP length, L_{DFP}, µm	Gate width, W_G, µm
Liner:						
w/o FP	3	3	5, 7, 9, 11, 13, 17	-	-	50
With source FP	3	3	17	3, 5, 7, 11	-	50
With source and drain FP	3	3	17	3, 5, 7, 11	2.5	50
With non-uniform source FP	3	3	17	3, 5, 7, 11	-	50
With non-uniform source and drain FP	3	3	17	3, 5, 7, 11	2.5	50
Bidirectional:						
w/o FP	3	3	9, 11, 13, 17	-	-	50
With FPs	3	3	13, 17	2	2	50
Circular:						
w/o FP	3	3	5 7 9 11 13 17	-	-	355 367 380 392 405 430
With source FP	3	3	5 7 9 11 13 17	3	-	355 367 380 392 405 430

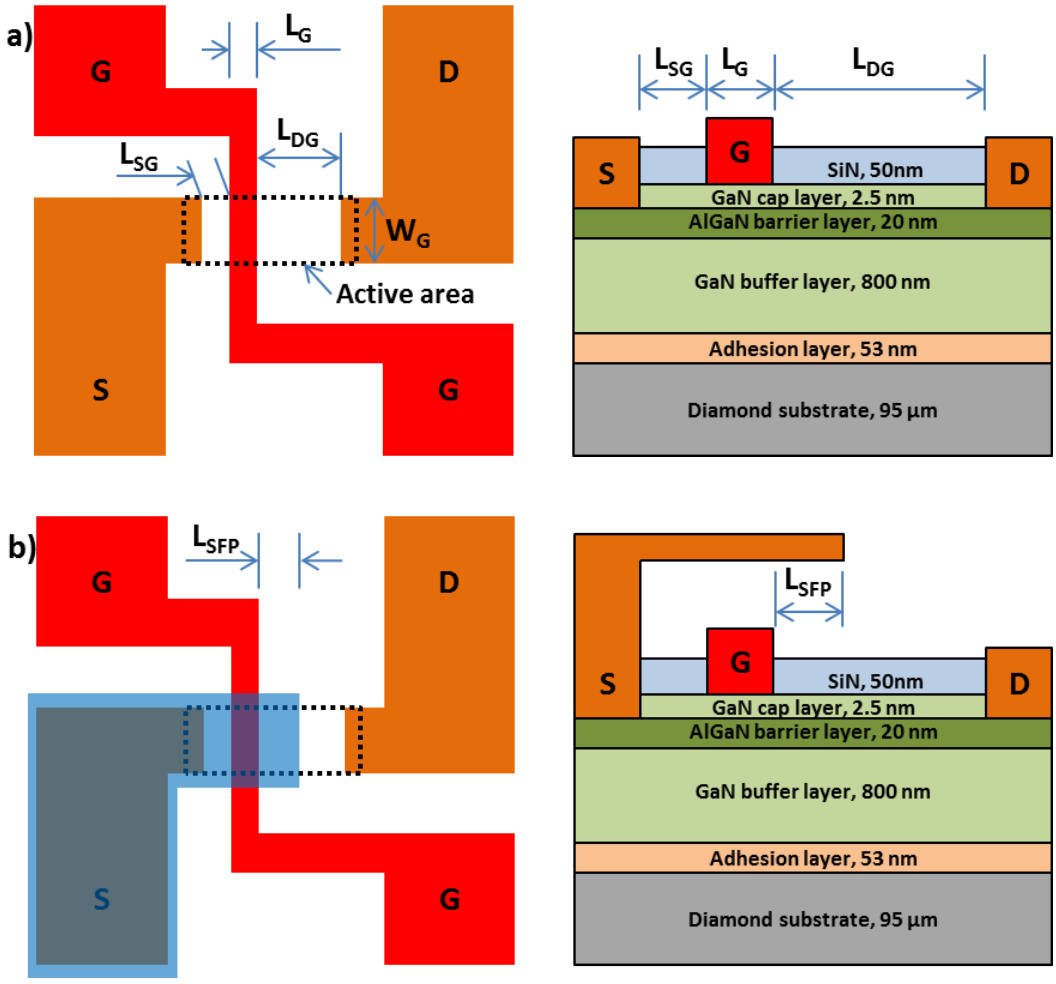
4.2.1 Linear layout devices

Fig. 4.2 shows the layouts and cross-sectional schematics of AlGaN/GaN HEMTs in linear form designed and fabricated in this work. These devices include:

1. Without any field plate (Fig. 4.2, a)
2. With source field plate (Fig. 4.2, b)
3. With source and drain field plates (Fig. 4.2, c)
4. With non-uniform source field plate (Fig. 4.2, d)
5. With non-uniform source field plate and drain field plate (Fig.4.2, e)

All of the designed linear GaN-on-Diamond HEMTs have the gate length L_G of 3 µm, source-to-gate distance L_{SG} of 3 µm, and gate width W_G of 50 µm. Further, devices without field plates have various gate-to-drain drift lengths L_{DG} – 5, 7, 9, 11, 13 and 17 µm. For all other linear HEMTs L_{DG} is 17 µm.

The source field plate (regular and non-uniform) have varied lengths L_{SFP} (L_{NUSFP}) – 3, 5, 7 and 11 µm, while the drain field plate L_{DFP} is fixed to 2.5 µm.



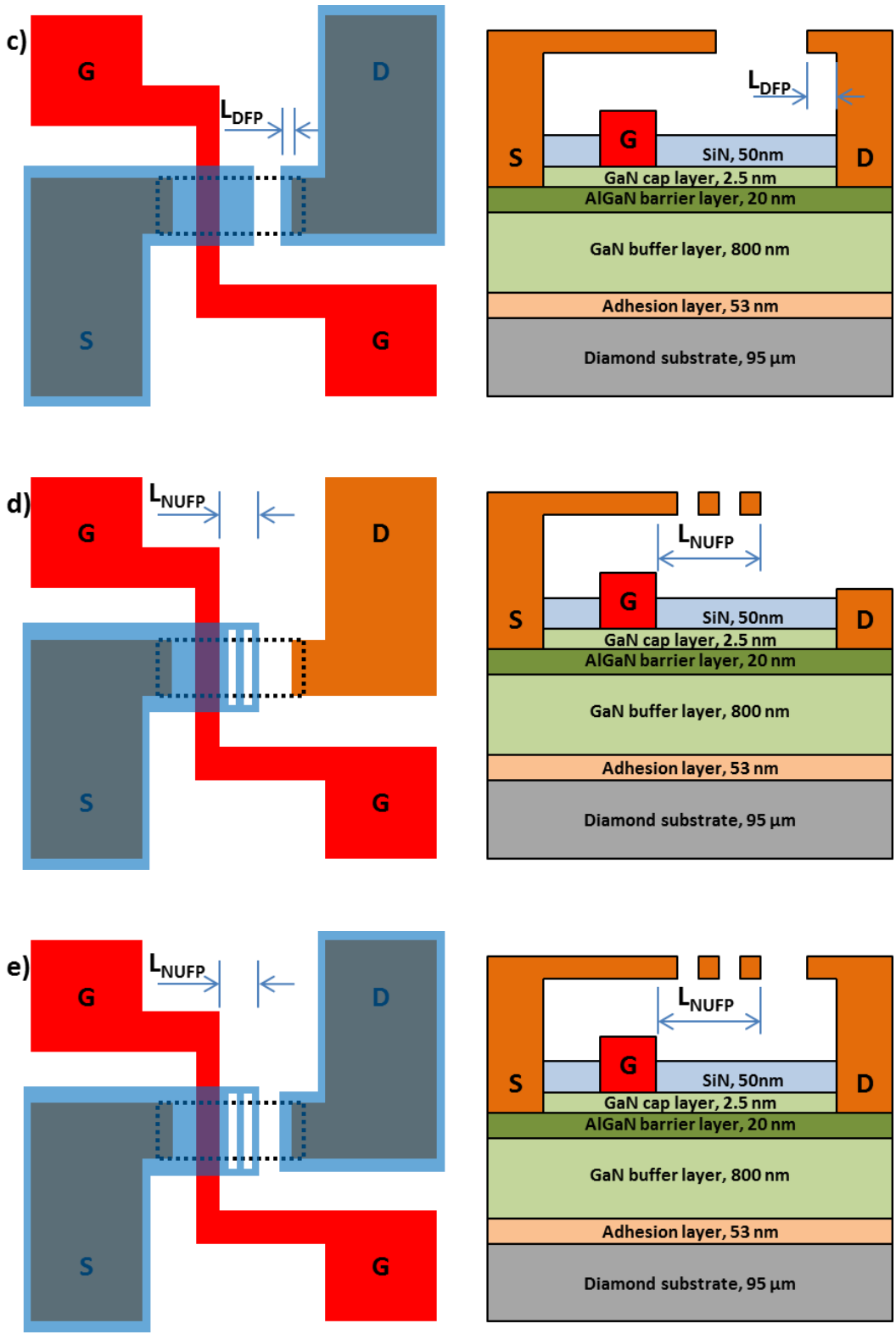


Figure 4.2: Layouts and cross-sectional schematics of linear GaN-based HEMTs: a) without any FP, b) with source FP, c) with source and drain FPs, d) with non-uniform source FP, e) with non-uniform source FP and drain FP.

4.2.2 Linear bidirectional HEMTs

Fig. 4.3 shows the layouts and cross-sectional schematics of linear bidirectional AlGaN/GaN HEMTs designed and fabricated in this work. All of the bidirectional devices have the gate length L_{G1} = L_{G2} = 3 µm, source-to-gate1 L_{SG1} (drain-to-gate2 L_{DG2}) distance of 3 µm, gate width W_{G1} = W_{G2} = 50 µm, and gate1-to-drain L_{DG1} (gate2-to-source L_{SG2}) drift length of 9, 11, 13 or 17 µm. The field plate length L_{FP1} = L_{FP2} = 2 µm.

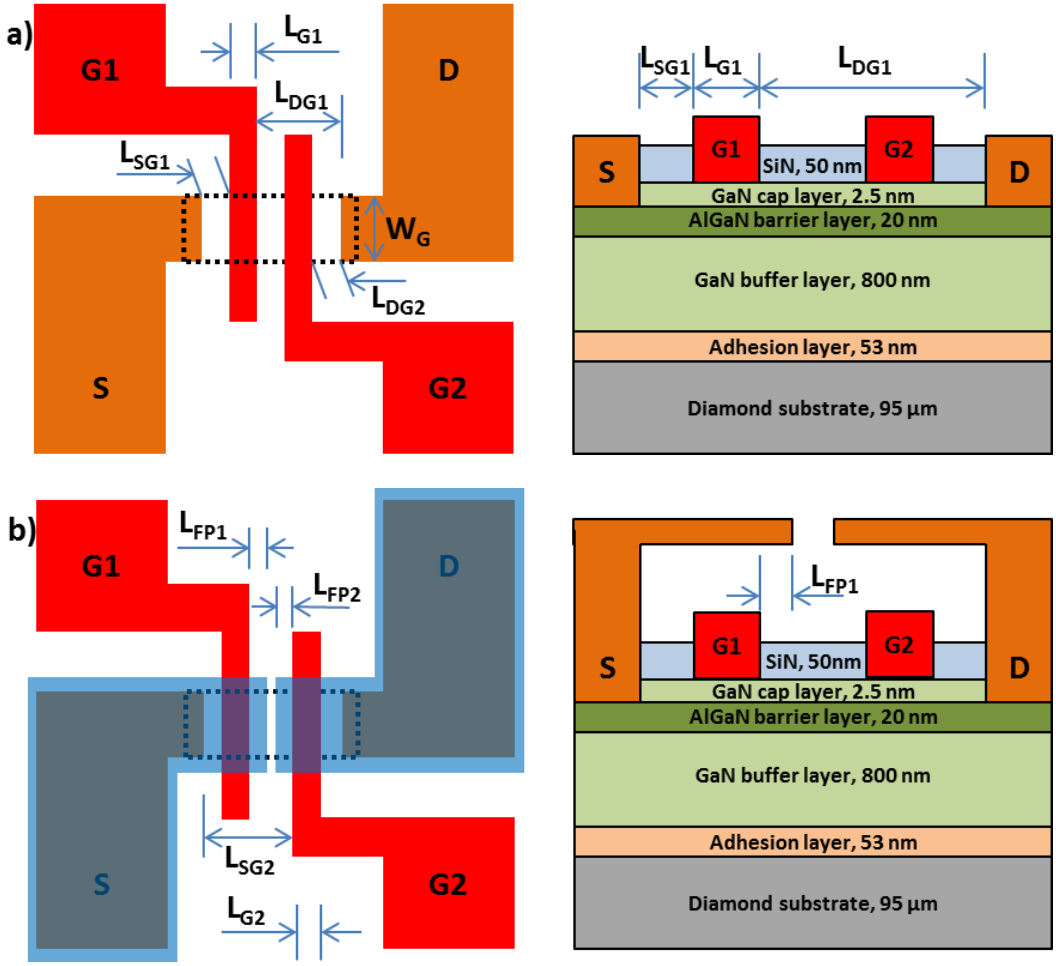


Figure 4.3: Layouts and cross-sectional schematics of bidirectional GaN-based HEMTs: a) without FPs, b) with FPs.

4.2.3 Circular layout devices

One of the advantages of the circular device layout is better electric field distribution. For a linear layout device local crowding of the electric field might happen at the area where gate finger crosses mesa etch region, while for a circular device the electric field distributes uniformly along the gate contact [65, 99].

Moreover, due to its self-enclosed structure, circular device design limits the extra source-to-drain leakage current [66].

Fig. 4.4 shows the layouts and cross-sectional schematics of circular AlGaN/GaN HEMTs designed and fabricated in this work. All of the designed circular GaN-on-Diamond HEMTs have the gate length L_G of 3 µm, source-to-gate distance L_{SG} of 3 µm, and gate-to-drain drift length L_{DG} of 5, 7, 9, 11, 13 or 17 µm. The source field plate length L_{FP} is 3 µm.

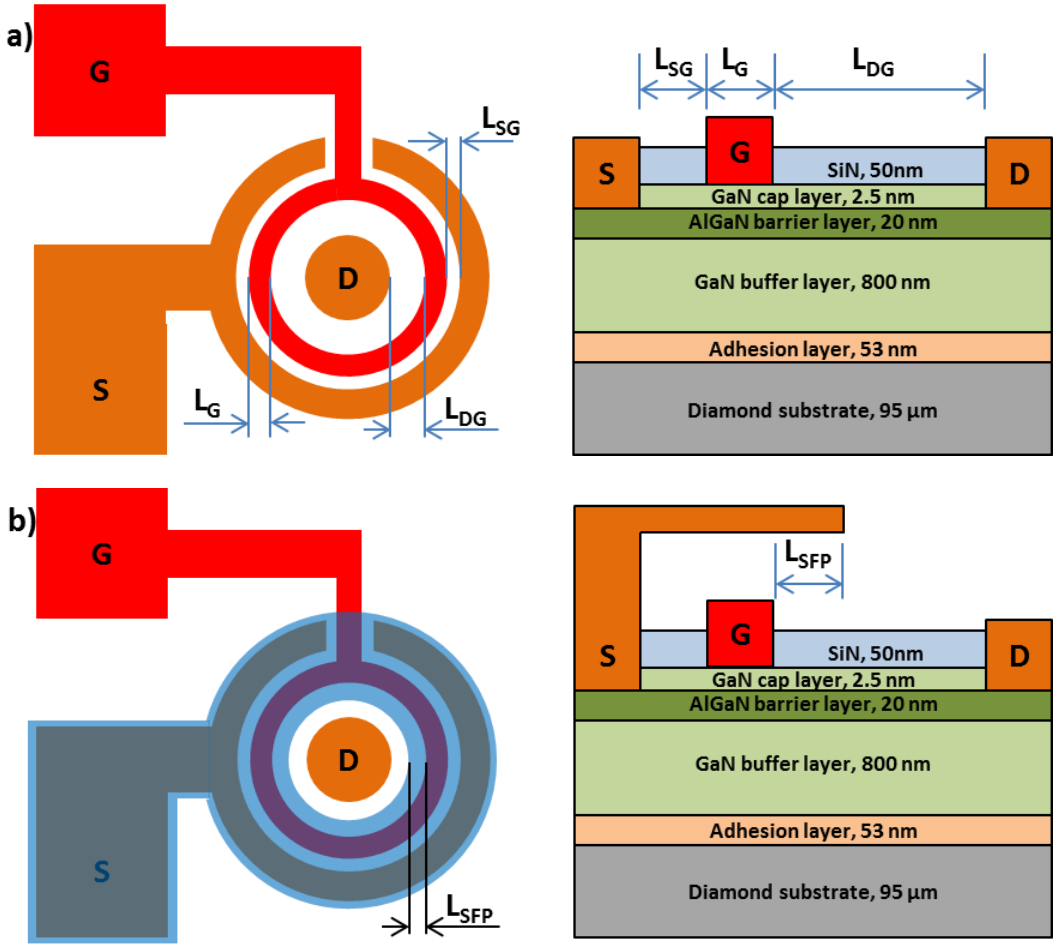


Figure 4.4: Layouts and cross-sectional schematics of circular GaN-based HEMTs: a) without source FP, b) with source FP

4.3 Device fabrication

Device fabrication was undertaken at the National Centre for III-V technologies at Sheffield. The processes required for device fabrication will be described in the following sections.

4.3.1 Structure of the sample

The GaN-on-diamond epi-wafers for this work were supplied by Element Six. The size of the supplied samples is 1 cm x 1 cm. Figs. 4.5 (a)-(b) show the cross-sectional schematic of the epi-layer structure and the top view photograph of the sample respectively.

To prepare the sample for use it has to be chemically cleaned to remove any trace of ionic, organic, and metallic impurities or any other contaminations. The standard 3-stage cleaning process was utilized in this work [100]:

- Immerse in n-butyl acetate;
- Immerse in acetone;
- Immerse in isopropyl alcohol (IPA).

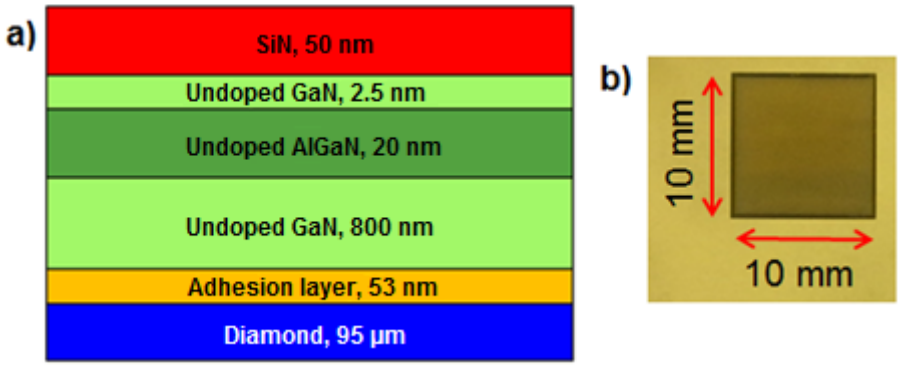


Figure 4.5: a) Epi-layer structure of the GaN-on-diamond sample; b) top view photograph of the epi-wafer

4.3.2 Lithography process

Lithography is the vital part of the device fabrication process that enables transferring of the patterns from the mask to the surface of the semiconductor sample. Photolithography was performed on Karl Suss MJB3 UV400 Mask Aligner MJB3.

In this work, photolithography was performed using the following steps:

1) Chemical cleaning of the sample as outlined in Section 4.3.1.
2) Covering the surface of the sample with a light-sensitive material (photoresist). SPR350 series photoresist was predominantly used in this

work. For a better adhesion of photoresist the sample was treated with hexamethyldisilazane (HDMS) adhesion promoter prior the photoresist application. In cases where the next step after photolithography was metal deposition, prior to SPR350 resist deposition, polymethylglutarimide (PMGI) resist was spun on the surface of the sample for a better metal lift-off. The resist spinner (4000 rpm for 30 sec) was used to coat the sample with resists.

3) Baking the resist after spinning at 100°C for 60 seconds. This step removes all unwanted moisture and improves adhesion of the resist. When the sample was coated with PMGI, it was baked at 180°C for 5 minutes prior to SPR350 application.
4) Exposing the sample through the aligned photomask to the UV light of the mask aligner. The exposure time for SPR350 was optimised as 4.5 seconds.
5) Developing of the photoresist in MF26A developer for 1 minute to wash away any resist that has been exposed. The sample is then rinsed in DI water.
6) O_2 plasma ashing of the sample for 2 minutes in order to remove any residual photoresist.

4.3.3 Processing steps

Overview

Every time the photolithography process is followed either by metal deposition or etch step.

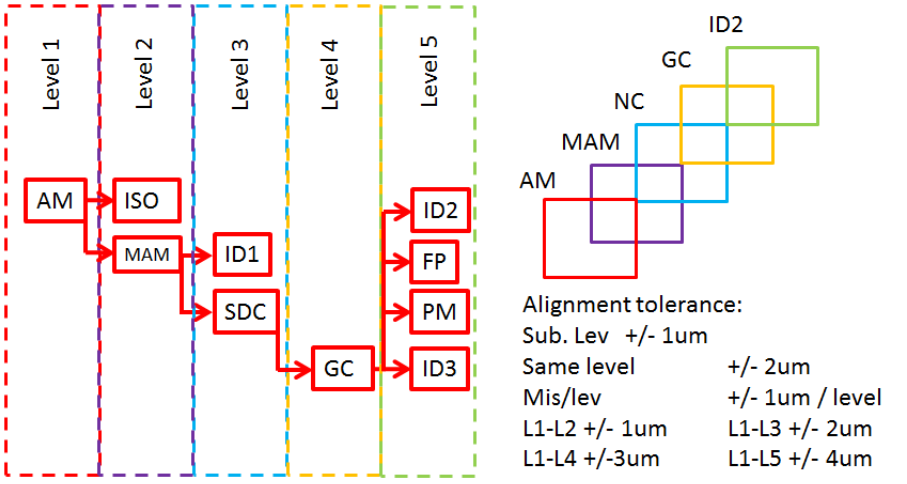
Metal deposition is another essential part of the device fabrication process. Once the lithography process outlined in the previous section is finished the sample can be placed into the metal deposition machine. In this work a thermal evaporator (Edwards Coating System E306A) was used for metal deposition procedures.

Etching is again another crucial aspect of semiconductor device fabrication process. Etching is the process of removal of material which is not covered by hardened photoresist. This process can be done either in liquid (wet etch) or gaseous (dry etch) form. Dry etch is the most preferable choice for GaN due to difficulty of

wet etch [67]. In this work the dry etch processes were completed by using reactive ion etching (RIE) and inductively coupled plasma (ICP) etching. The main difference between RIE and ICP is that the ion energy and ion density of the former can be determined by one RF plasma source while the latter has two independent RF and ICP sources enabling separate control over ion density and ion energy, and providing higher flexibility to the process. Another important issue which has to be mentioned is that no gold is allowed in ICP machine at the facility due to the risk of chamber contamination and therefore in this work the RIE etching was used after metal deposition (metal alignment marks) at step 3. The details of the process steps which were used for this project will be given in the following sections.

Alignment sequence

The developed fabrication process-flow consists of ten photolithography steps (10 masks). The alignment sequence along with alignment tolerance is shown in Fig. 4.6.



1. AM – Alignment mark etch
2. ISO – Mesa isolation etch
3. MAM – Metal alignment mark
4. ID1 – Insulator deposition/patterning
5. SDC – Source/drain contact
6. GC – Gate contact
7. ID2 – Insulator deposition/patterning
8. FP – Field plates metal deposition
9. PM – Pad metallization
10. ID3 - Insulator deposition/patterning

Figure 4.6: Alignment sequence and alignment tolerance.

Mask 1 – Alignment marks etch

The first photomask is simply aligned with the edges of the sample and includes only alignment marks to which the following masks will be aligned. The alignment marks were etched by ICP etching of SiN and III-nitrides (Fig. 4.7). At

first the sample was placed into the ICP machine and the program was set to etch 50 nm of the top SiN layer:

- Gases and flow rates: CHF_3 – 20 sccm and Ar_2 – 30 sccm,
- RF power – 200 W,
- Temperature – 20 °C,
- Pressure of the chamber – 35 mT,
- Etching time – 6.5 min.

Once the etching of SiN has been finished the sample was unloaded and recipe was changed to etch into GaN buffer (~ 250 nm):

- Gases and flow rates: $SiCl_4$ – 1.5 sccm, Cl_2 – 15 sccm, and Ar_2 – 4 sccm,
- RF power – 80 W,
- ICP power – 450 W,
- Temperature – 20 °C,
- Pressure of the chamber – 4 mT.
- Chamber preparation time – 20 min (running the ICP machine with new recipe without the sample). Once the chamber preparation has been finished the sample was placed back into the chamber,
- Etching time – 5 min.

The etching depth and surface profile were checked using Optical Profilometer DEKTAK 150.

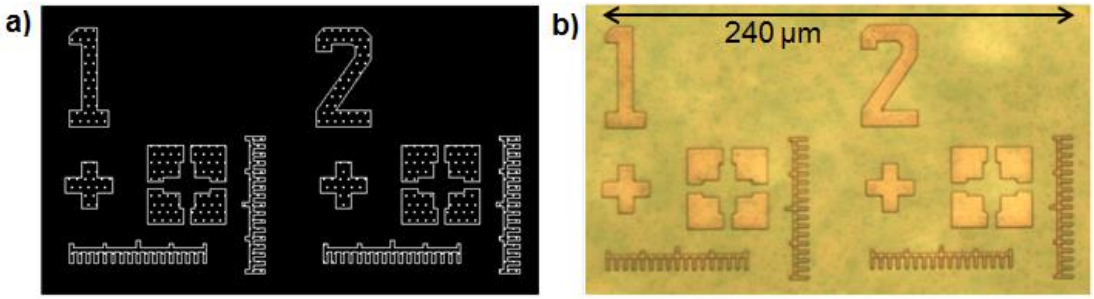


Figure 4.7: Alignment marks for the second and third photomasks: a) layout in IC station; b) processed.

Mask 2 – Mesa isolation etch

Mesa isolation etch is required in order to electrically isolate the individual devices from each other on the sample. For GaN-based HEMTs the mesa isolation could be done by etching into the semi-insulating GaN buffer.

In order to attain better etch control and reduce the surface damage the RF power has to be minimized. However, it is problematic to obtain sustainable striking plasma at low RF power. Two step etching process has been used to overcome this difficulty (etched depth ~ 134 nm):

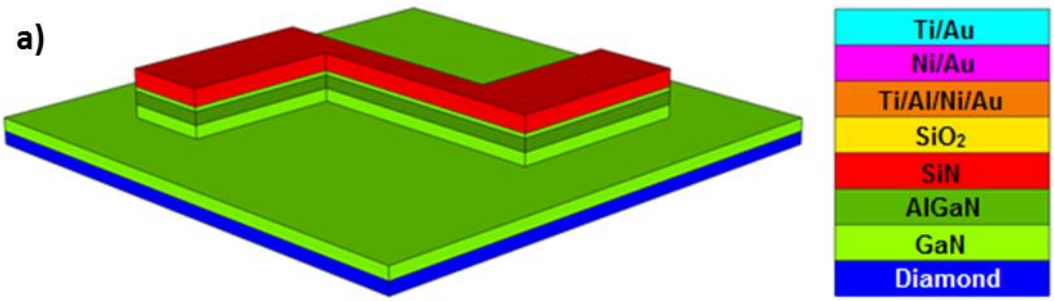
1 step

- Gases and flow rates: $SiCl_4$ – 1.5 sccm, Cl_2 – 15 sccm, and Ar_2 – 4 sccm,
- RF power – 80 W,
- ICP power – 450 W,
- Temperature – 20 °C,
- Pressure of the chamber – 4 mT,
- Time – until the plasma has stabilized (~ 2 – 3 sec)

2 step. Once the plasma has stabilized the RF power was set to:

- RF power – 10 W,
- Etching time – 24.5 min.

The etch depth and surface profile were checked using DEKTAK profilometer. The result of the mesa isolation etch is shown in Fig. 4.8 (adhesion layer between GaN buffer and diamond substrate is not shown).



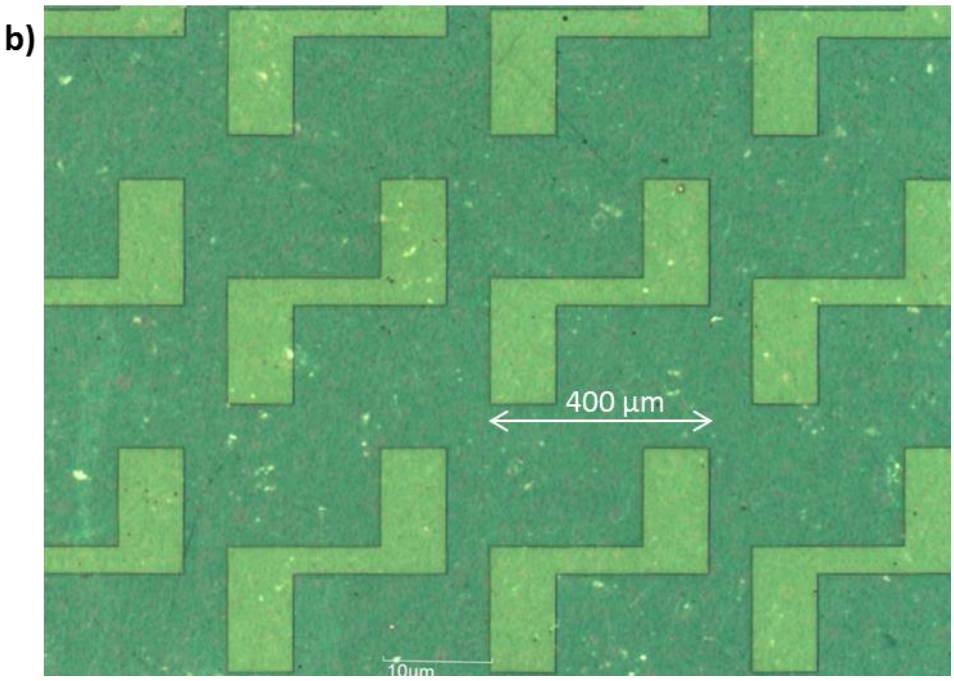
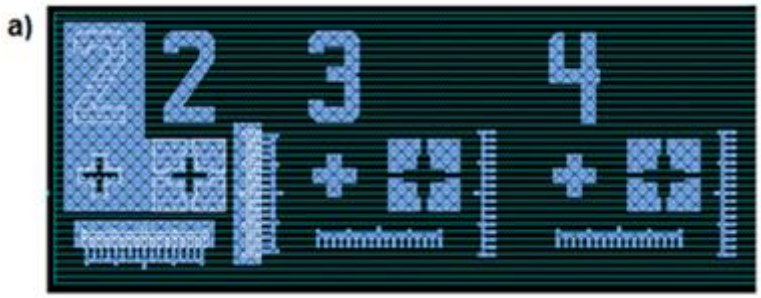


Figure 4.8: Sample morphology after mesa isolation etch step on the example of linear HEMT with uniform source field plate: a) 3D schematic illustration and b) part of actual sample.

Mask 3 – Metal alignment mark

Once the mesa isolation step has been completed, the new alignment marks were formed by thermal evaporation of Ti/Au (20/200 nm) (Fig. 4.9). When the metal deposition process has been finished it is necessary to remove all unwanted metal from the sample (lift-off process). For this purpose the sample is placed in a beaker of acetone which washes away the remaining photoresist and metal deposited on top of it. To remove any residual photoresist the sample is then placed into O2 asher for 2 min.



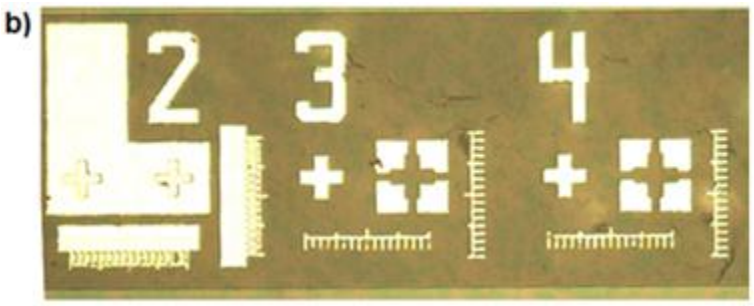


Figure 4.9: Metal alignment marks for the fourth and fifth photomasks: a) layout in IC station; b) processed.

Mask 4 – SiO_2 deposition. SiN and SiO_2 RIE etch

In order to minimize any leakage between pad areas a blanket deposition of SiO_2 was done by plasma enhanced chemical vapour deposition (PECVD) (Fig. 4.10, a). 100 nm of SiO_2 were deposited using PECVD machine, the recipe was set to:

- Gases and flow rates: SiH_4 – 160 sccm, N_2O – 900 sccm, N_2 – 240 sccm,
- RF power – 25 W,
- Temperature: table – 300 °C, wall – 60 °C,
- Pressure of the chamber – 900 mT,
- Deposition time – 2.5 min.

The thickness of the deposited dielectric was checked using V-VASE Ellipsometer.

Since the sample now contained the metal (alignment marks after step 3) it was not allowed to be placed into the ICP machine and the patterning of the SiN and SiO_2 was done by RIE etch. To etch 50 nm of SiN and 100 nm of SiO_2 from the active region of the sample, it was placed in RIE machine and the program was set to:

- Gases and flow rates: CHF_3 – 35 sccm, O_2 – 5 sccm,
- RF power – 100 W,
- Pressure of the chamber – 35 mT,
- Etching time – 7 min.

The etching time was controlled by end-point detection and the etched depth checked by DEKTAK profilometer. The result of this step is schematically illustrated in Fig. 4.10, b. Some of the actual devices after the RIE etching step are shown in Fig. 4.10, c.

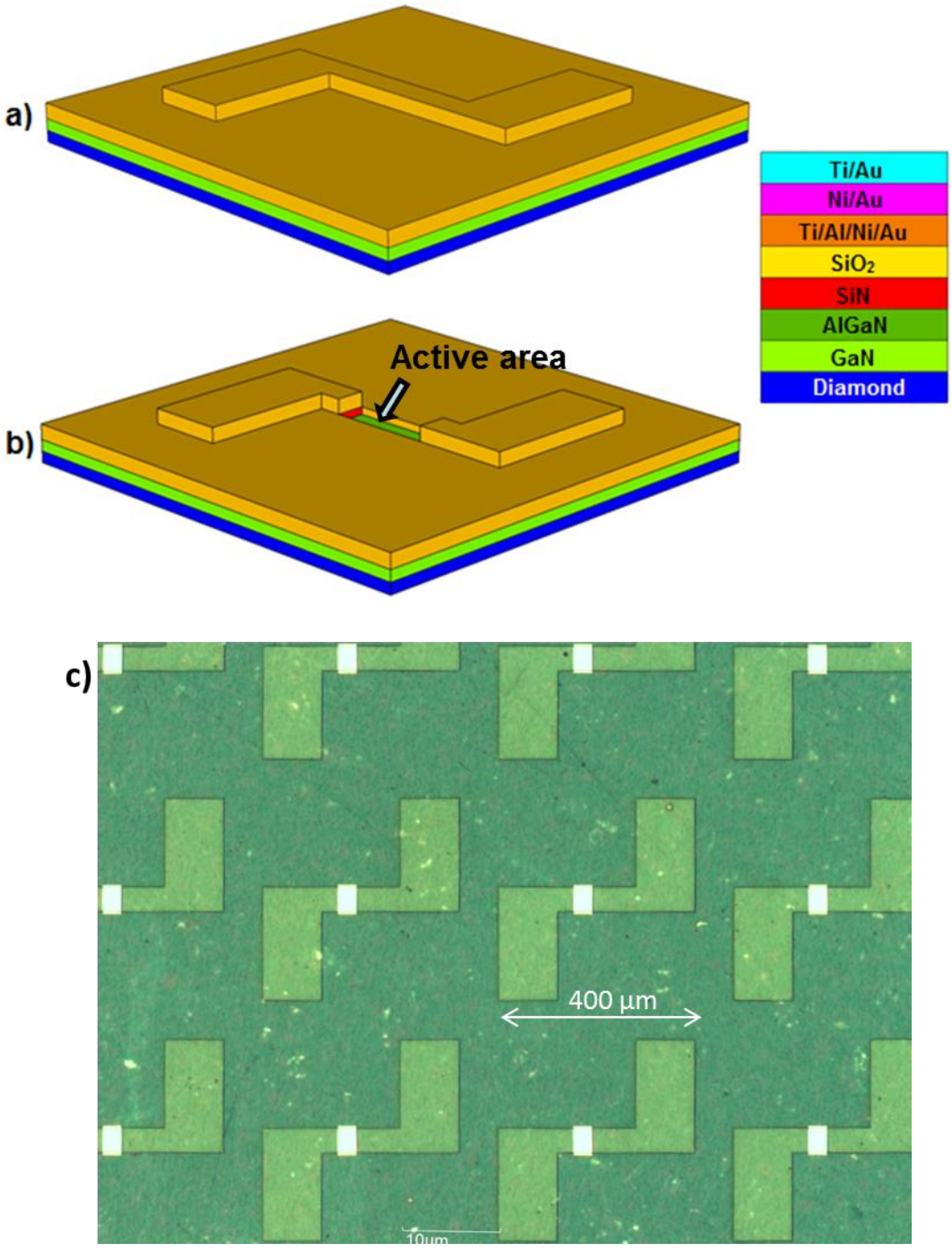


Figure 4.10: Schematics of sample morphology after: a) SiO_2 (100 nm) deposition; b) SiO_2 / SiN etch from the active area; c) actual devices after RIE etching.

Mask 5 – Source and drain contact formation. Annealing

Source and drain electrodes were formed by thermal evaporation of Ti/Al/Ni/Au (20/100/45/55 nm) (Fig. 4.11). In order to make a good Ohmic contact to the semiconductor the drain and source electrodes must be annealed (before gate contact formation). The metal annealing process was completed by rapid thermal annealing (RTA) at 800 °C for 1 minute in N_2 ambient (Fig. 4.11, d).

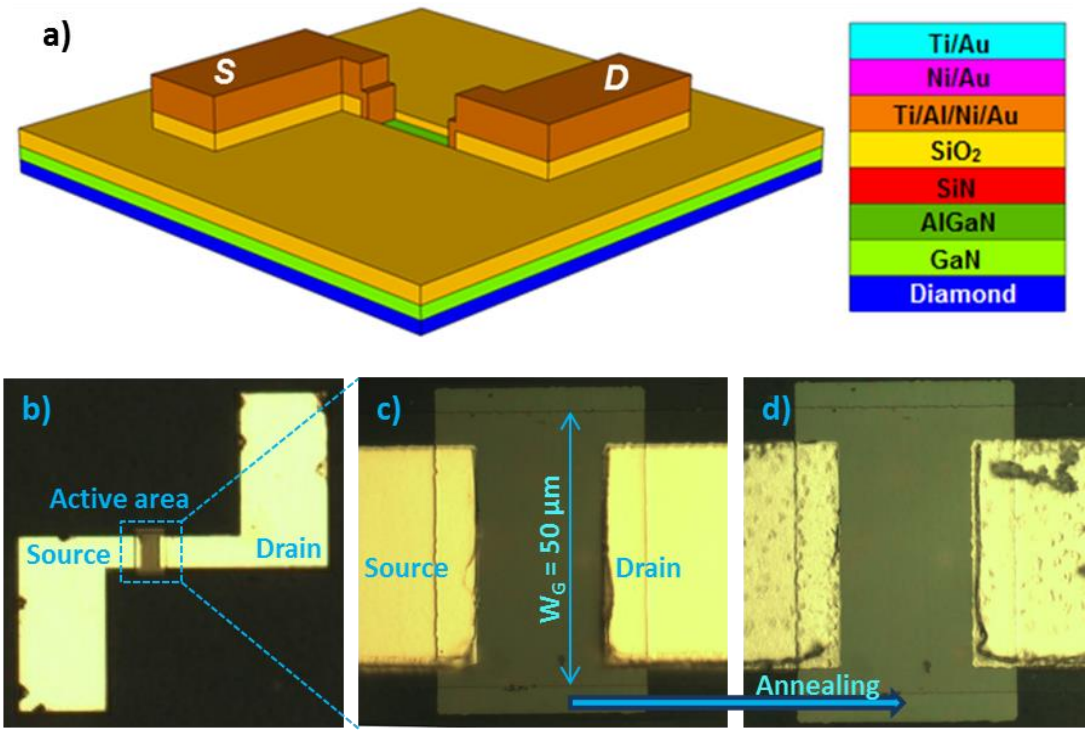


Figure 4.11: Sample after source and drain contacts formation: a) 3D schematics; b) actual device; c) active area before RTA, and d) active area after RTA.

The transmission line model (TLM) is a convenient method for determining the specific contact resistivity ρ_C of Ohmic contact electrodes [109]. Fig. 4.12 shows the typical plot of total contact to contact resistance R_T as a function of distance ℓ along with the equations used for calculations to obtain ρ_C, where W is the contact width, R_C is the contact resistance, L_T is the transfer length, R_{SK} is the sheet resistance of the semiconductor layer directly under the contact, and R_{SH} is the sheet resistance of the semiconductor layer outside the contact region [109]. The TLM pattern (included on the same sample as the devices) is illustrated in Fig. 4.13.

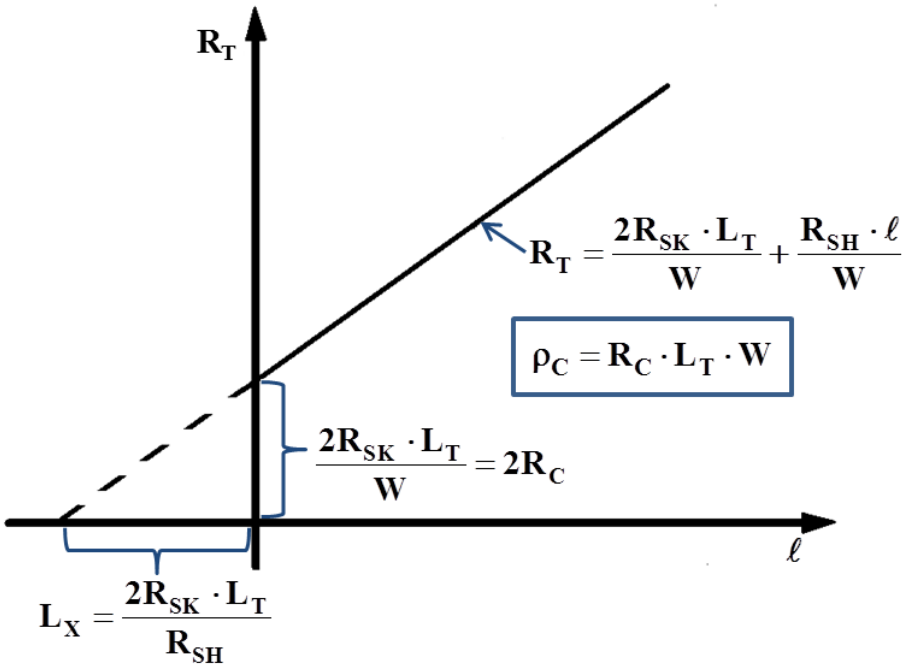


Figure 4.12: Typical plot of total contact to contact resistance as a function of ℓ to obtain specific contact resistivity of Ohmic contact electrodes.

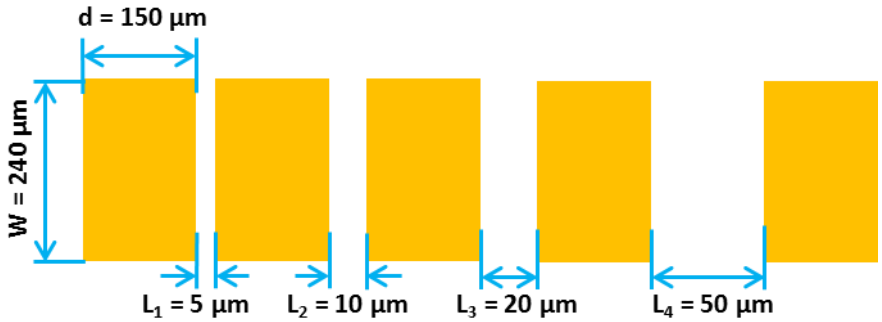


Figure 4.13: TLM pattern used to estimate the ohmic contact parameters.

Fig. 4.14 shows the measured I – V characteristics and calculated resistances between the adjacent contacts of the TLM pattern. Fig. 4.15 demonstrates the plot of total contact-to-contact resistance versus distance between contacts. This graph was used to obtain specific contact resistivity, transfer length, and sheet resistance of 2DEG.

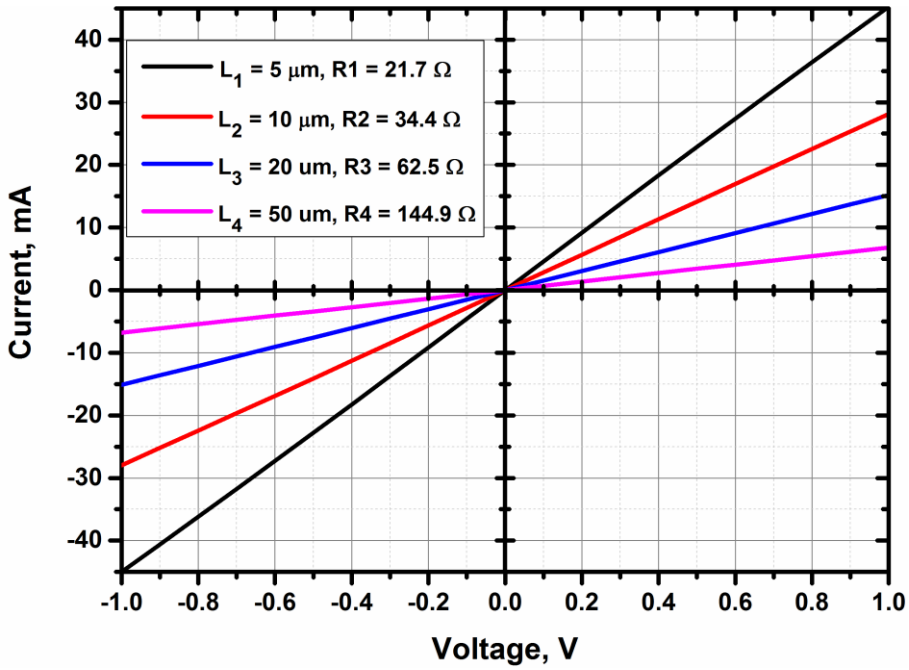


Figure 4.14: I – V characteristics measured between adjacent contacts of TLM pattern.

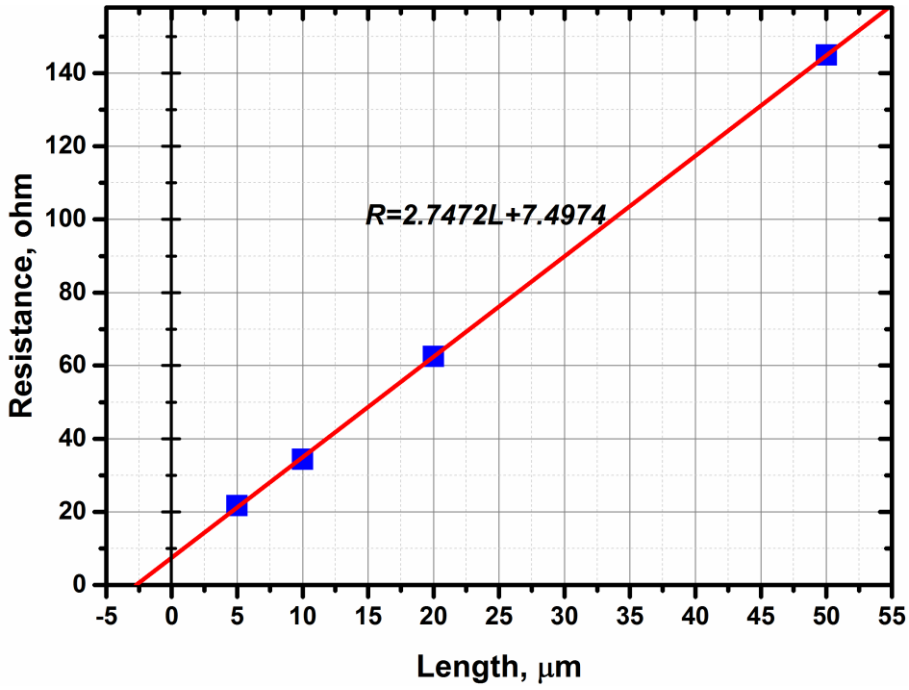


Figure 4.15: Plot of total contact to contact resistance versus distance between contacts.

The specific contact resistivity of Ohmic contact electrodes is found to be ~ 1.2 x 10-5 Ω.cm^2. The sheet resistance of the 2DEG at the AlGaN/GaN interface and transfer length were estimated as 687 Ω/□ and 1.36 μm respectively.

Mask 6 – Gate contact

Once the drain and source contacts were defined, after the corresponding photolithography step, the Schottky gate contact was formed by thermal evaporation of Ni/Au (20/200 nm) and the result is shown in Fig. 4.16.

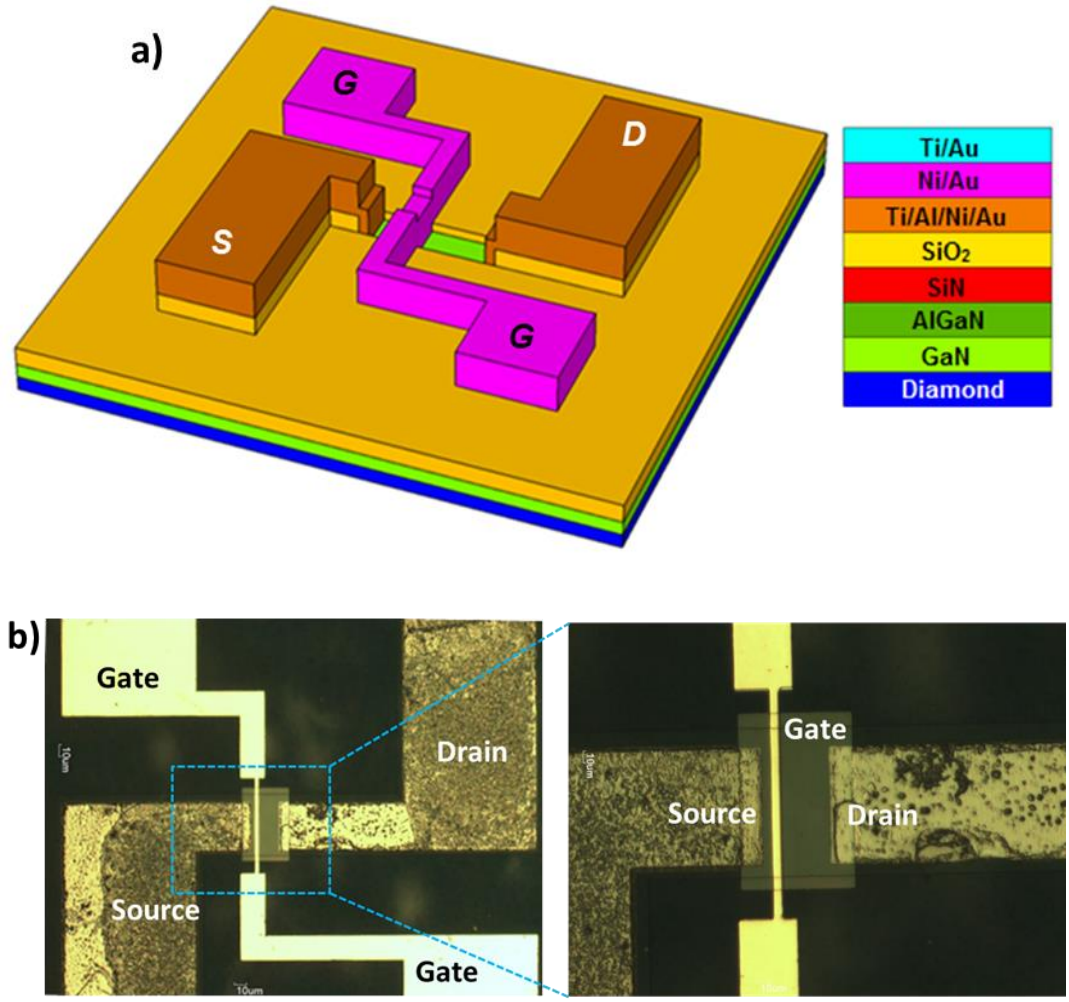


Figure 4.16: Sample after Schottky gate formation: a) 3D schematics. b) Actual device.

After the gate formation initial electrical characteristics of the linear device with L_{DG} = 17 μm were measured and the results are presented in Fig. 4.17. The threshold of the device is found to be V_{TH} ~ -3V and specific on-state resistance (R_{ON}.A) ~ 9.2 mΩ.cm^2.

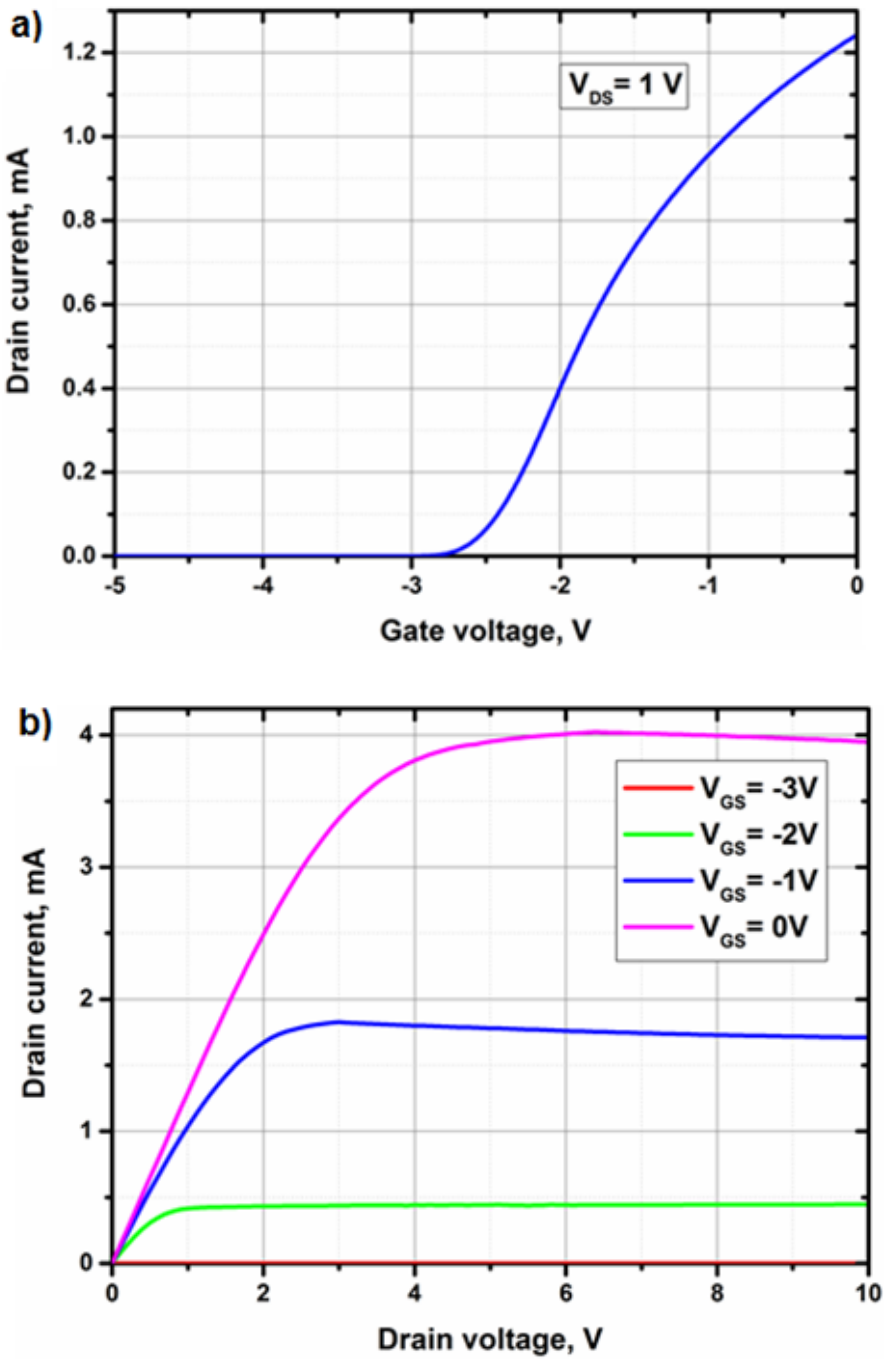


Figure 4.17: Initial transistor characterisation: a) transfer I – V characteristics; b) output I – V characteristics.

Mask 7 – SiN, SiO_2 deposition and patterning

50 nm of SiN and 450 nm of SiO_2 were deposited all over the sample by PECVD (Fig. 4.18). In order to deposit SiN, the program was set to:

- Gases and flow rates: SiH_4 – 100 sccm, NH_3 – 5 sccm, N_2 – 900 sccm,

- RF power – 25 W,
- Temperature: table – 300 °C, wall – 60 °C,
- Pressure of the chamber – 900 mT,
- Deposition time – 5 min.

Once the SiN deposition has been finished the sample was unloaded and the recipe was changed to the one outlined in section Mask 4. In order to prepare the chamber, the PECVD machine was running with a new recipe for 20 minutes without the sample inside. After the chamber preparation the sample was placed in PECVD machine for dielectric deposition for 11 minutes 25 seconds (Fig. 4.18, b).

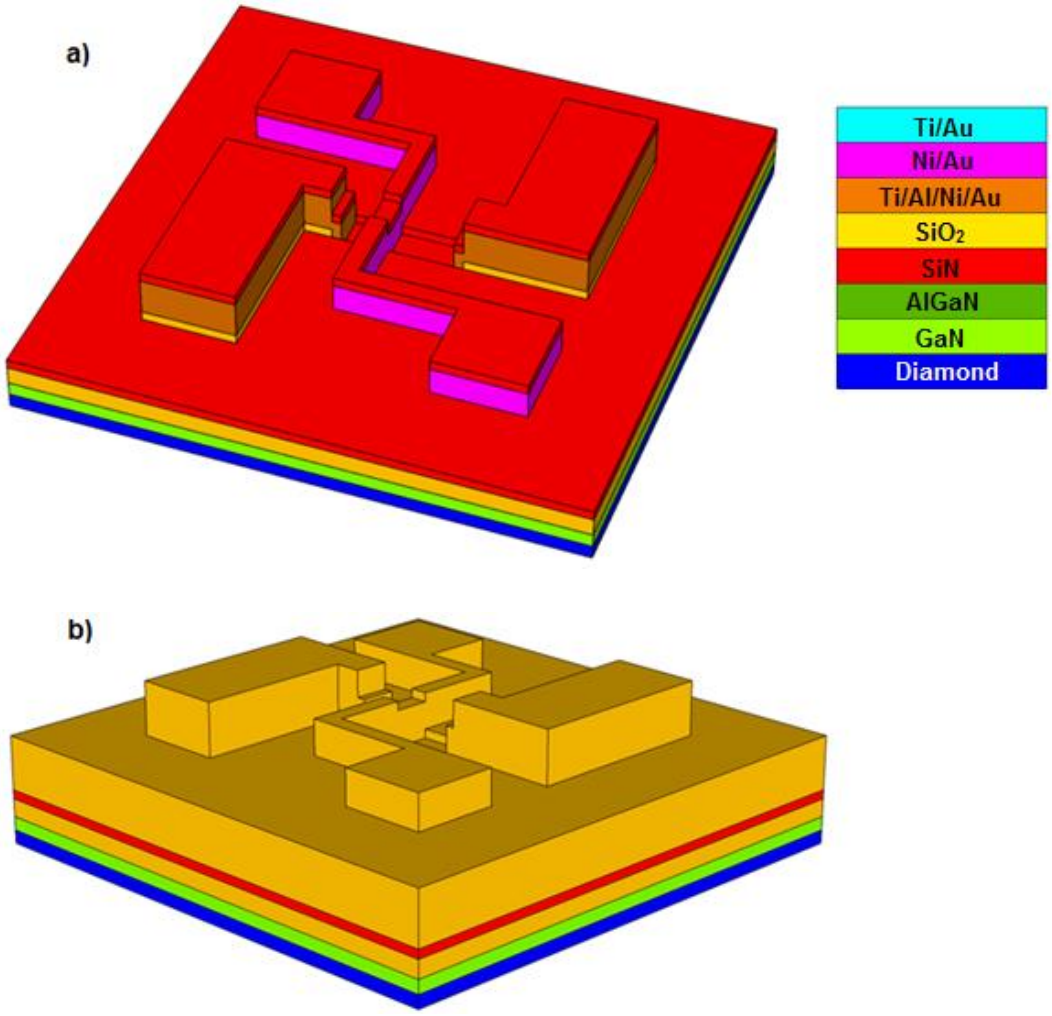


Figure 4.18: Sample after: a) SiN (50 nm) blanket deposition; b) SiO_2 (450 nm) blanket deposition

Once the dielectric deposition and consequent photolithography process have been finished the SiN (50 nm) and SiO_2 (450 nm) were etched from the pad areas by

RIE machine using the same recipes as outlined section Mask 4 (Fig. 4.19). Thicknesses of deposited and etched layers were checked by Ellipsometer and DEKTAK profilometer respectively.

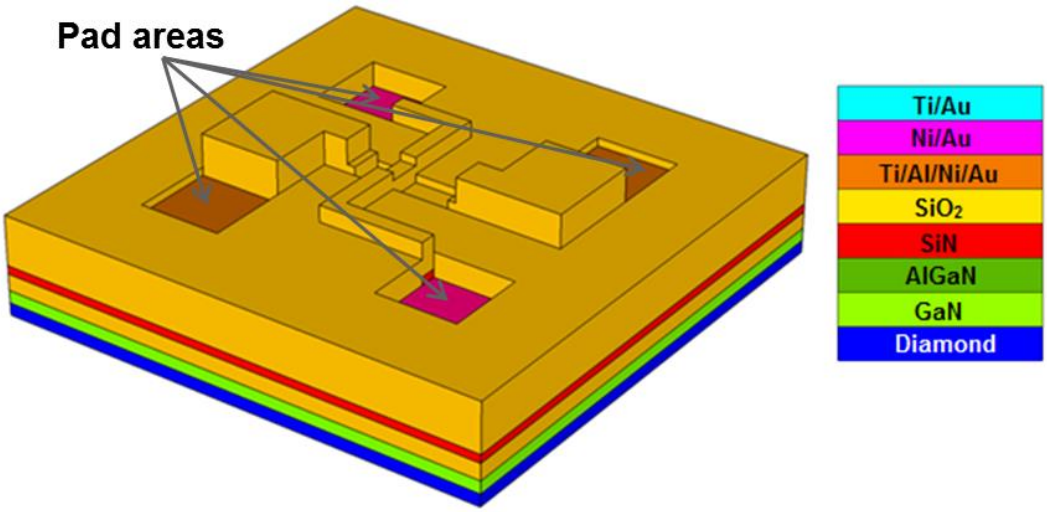


Figure 4.19: Sample after etching SiN / SiO_2 from the pad areas.

Mask 8 – Field plates metal deposition

The field plates were formed by thermal evaporation of Ti/Au (20/480 nm). The result is schematically shown in Fig. 4.20 on the example of GaN-based HEMT in linear form with single uniform source field plate.

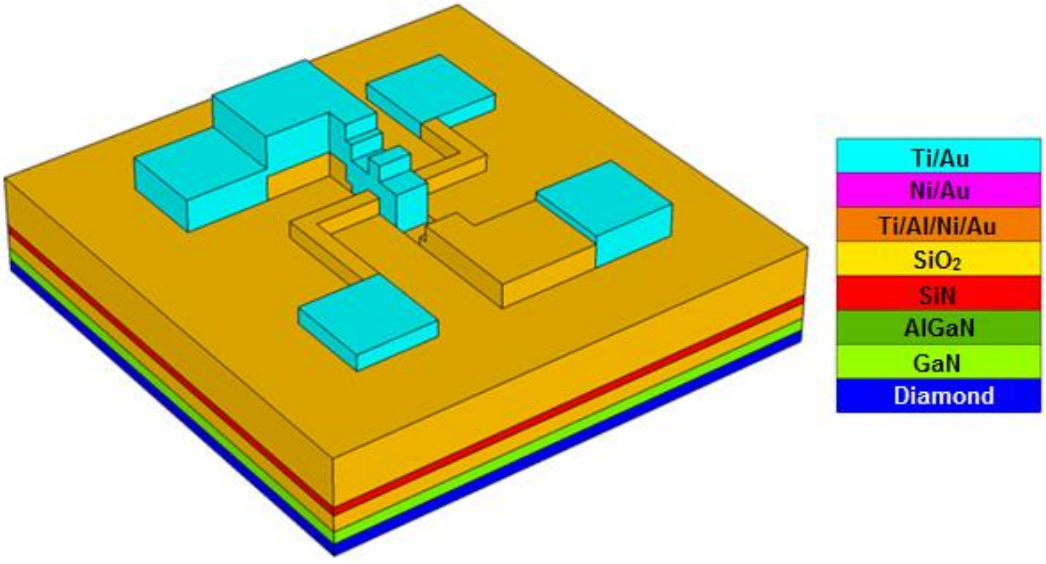


Figure 4.20: Schematic illustration of the sample after field plate formation (on the example of a linear device with single uniform field plate).

Mask 9 –Pad metallization

In order to make the pads of the devices more robust for probing, their additional metallization has been carried out by thermal evaporation of Ti/Au (20/480 nm). Fig. 4.21 shows the schematic illustration of the sample after this step.

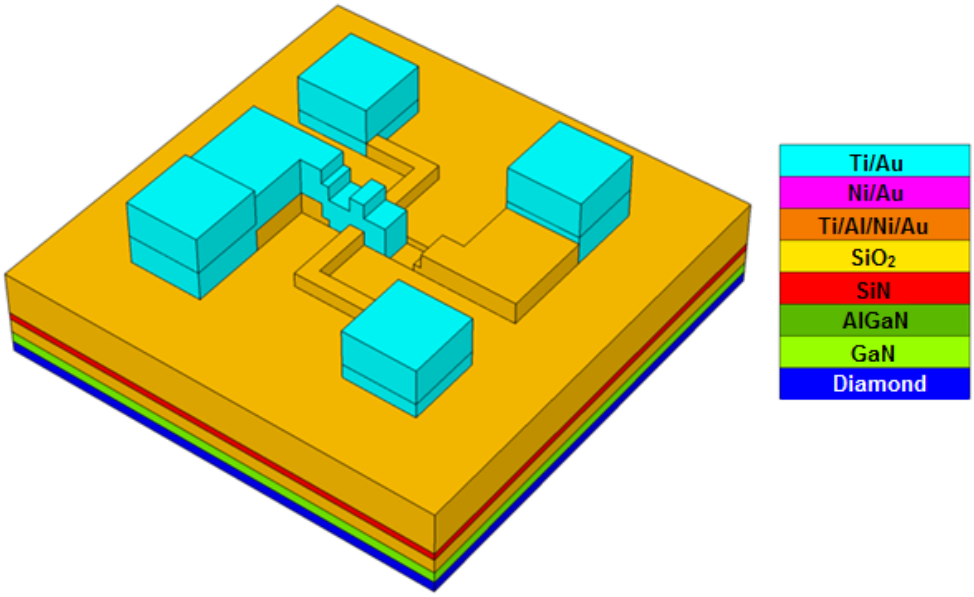
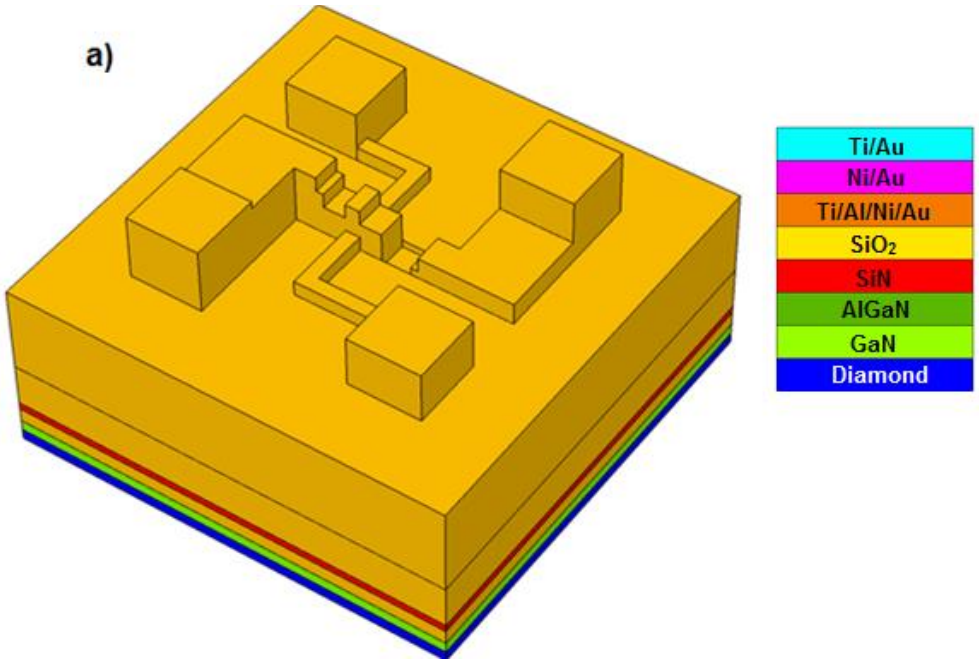


Figure 4.21: Schematic illustration of the sample after additional metallization of the pad areas.

Mask 10 – SiO_2 deposition and patterning

Finally, blanket deposition of a 1000 nm SiO_2 by PECVD (Fig. 4.22, a) and subsequent patterning by RIE etch (Fig. 4.22, b) has been carried out using same recipes as described in previous sections.



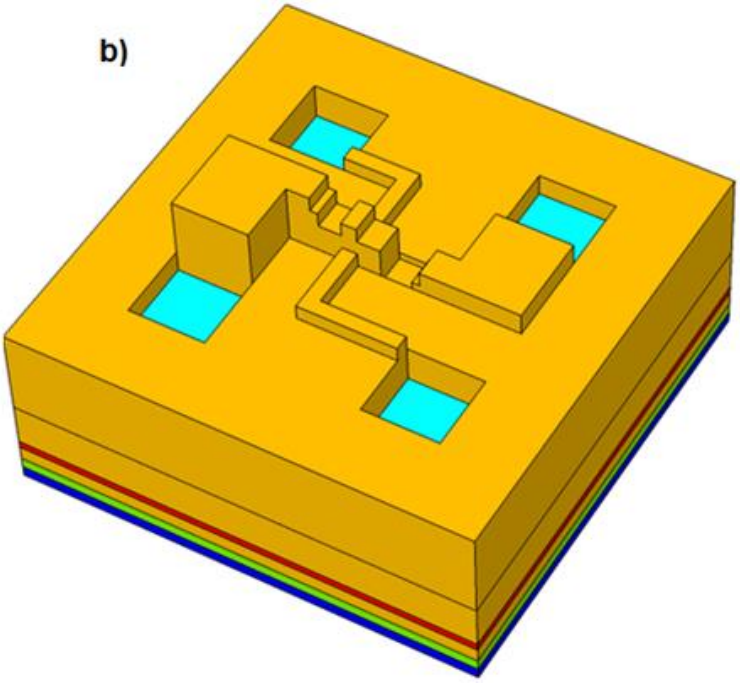


Figure 4.22: Sample after: a) SiO_2 (1000 nm) blanket deposition; b) etching SiO_2 from the pad areas.

4.4 Conclusions

This chapter has provided details on the design and fabrication method of GaN-on-Diamond HEMTs. The device design was based on the data obtained from the simulation. The fabricated devices include conventional GaN-on-Diamond HEMTs in circular and linear form with and without field plates as well as bidirectional transistors. The next chapter will provide the electrical characterisation results of the fabricated devices.

Chapter 5

Electrical Characterisation of GaN-on-Diamond HEMTs

5.1 Introduction

The evolution of advanced power electronic systems is commonly driven by the requirements for lower weight, smaller size, higher reliability, higher efficiency, and lower costs [112]. The most frequently used figure of merit which brings together all these parameters and provides a reliable assessment of the progress of the technology is power density. The power density of power electronic converters has roughly doubled every decade starting from 1970. The present-day technology is already facing the barriers which could limit the power density of power electronic converters in future [112].

AlGaN/GaN high electron mobility transistors (HEMTs) are ideal candidates for use in applications with requirements of high power densities [17]. However, due to poor thermal properties of commonly used starting substrate materials for GaN epitaxial growth (such as Sapphire, Silicon) the usable power densities are limited. In order to attain reliable operation and harness the true performance of GaN devices, improved thermal management is necessary [106]. CVD Diamond with its high room-temperature thermal conductivity that is at least 3 times higher (depends on growth conditions and crystal quality) than good thermally conductive substrates such as Silicon Carbide (SiC) could emerge as the ideal substrate option to address the heat transfer issues and aid the development of power electronics with high reliability and power densities. This area of research is gaining focus and reports evaluating integration of Diamond and GaN for device technologies have been published [60, 113]. It has already been shown through simulation and experimental demonstration that GaN-on-Diamond platform can significantly outperform GaN-on-SiC platform for Radio Frequency (RF) applications by reducing thermal resistance and thereby increasing power density [104, 105, 106]. It should be noted that most of the work which has been accomplished on GaN-on-Diamond to date has been primarily focussed on RF devices, while in this work an effort to realise the first high-voltage GaN-on-Diamond power device was undertaken.

This chapter will present detailed electrical characterisation results of the fabricated GaN-based HEMTs on CVD diamond substrate. The measured electrical characteristics and the simulation results described in Section 3.4 are comparable. Temperature characterisation of 'capacitance – voltage' characteristics will be described in order to provide an insight on the temperature dependence of 2DEG sheet carrier concentration and threshold voltage of the processed devices. Breakdown voltage measurements will also be presented in this chapter. The significant part of the results and discussions presented here has been published in the proceedings of ESSDERC 2015 [111] and the elaborated version of ESSDERC paper has been selected for publication in Solid-State Electronics Journal.

5.2 I – V characterisation

The electrical characteristics of the fabricated devices were measured using Agilent B1500A semiconductor device analyzer. The device was connected to B1500A through probing needles and coaxial cables. As the measurements are sensitive to the presence of light, all measurements have been performed under dark conditions.

5.2.1 Linear GaN-on-Diamond HEMTs without FPs

The top view photograph of the fabricated linear GaN-on-Diamond HEMT without any field plate is shown in Fig. 5.1.

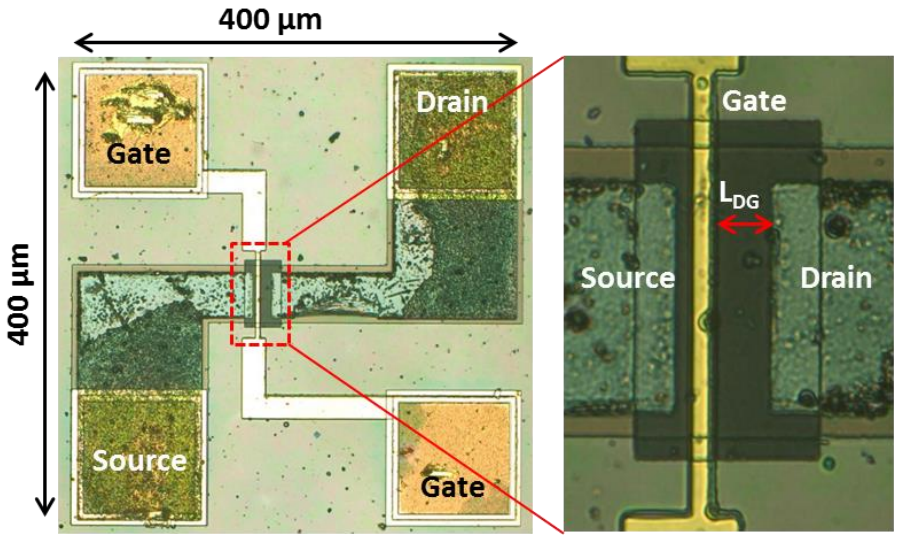


Figure 5.1: Fabricated linear GaN-on-Diamond HEMT (top view photograph).

Fig. 5.2 shows output current-voltage characteristics of the HEMT with gate-to-drain drift length L_{DG} of 17 μm after gate deposition (see Fig. 4.11) and after the completed fabrication. The specific on-state resistance (R_{ON}.A) of the completed device (mask 10) is ~ 8.1 mΩ.cm^2 compared to ~ 9.2 mΩ.cm^2 obtain from electrical characterisation of this device after gate formation step (mask 6).

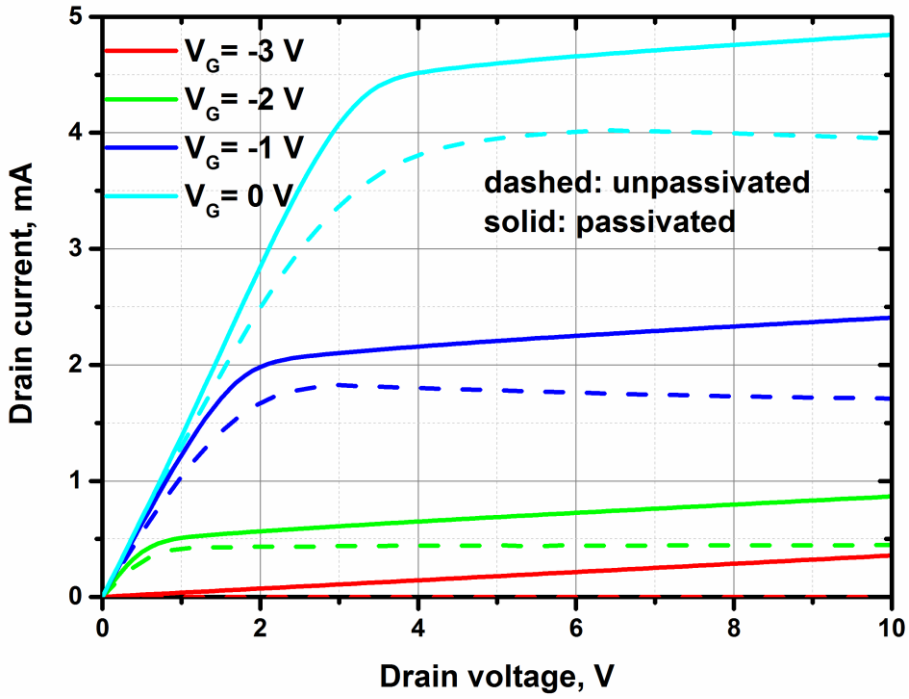


Figure 5.2: Output current-voltage characteristic of the linear GaN-based HEMT with L_{DG} = 17 μm

Although, the maximum drain current has increased (Fig. 5.2) due to surface passivation, the rise in the off-state leakage current is observed (Fig. 5.3). The rise in Drain to Source leakage current could be attributed to increase in sheet carrier concentration due to additional external stress on the AlGaN/GaN epilayers after deposition of thick dielectric layers [68] or due to poor crystal quality of GaN-on-Diamond sample.

Fig. 5.3 shows transfer I-V characteristic of this device (after gate formation step and after completed processing) at drain voltage V_{DS} = 1 V. The magnitude of threshold voltage (V_{TH}) has shifted towards higher values, from ~ - 3 V (step 6) to ~ - 3.17 V (step 10). The threshold voltage shift could also be attributed to increase in sheet carrier concentration.

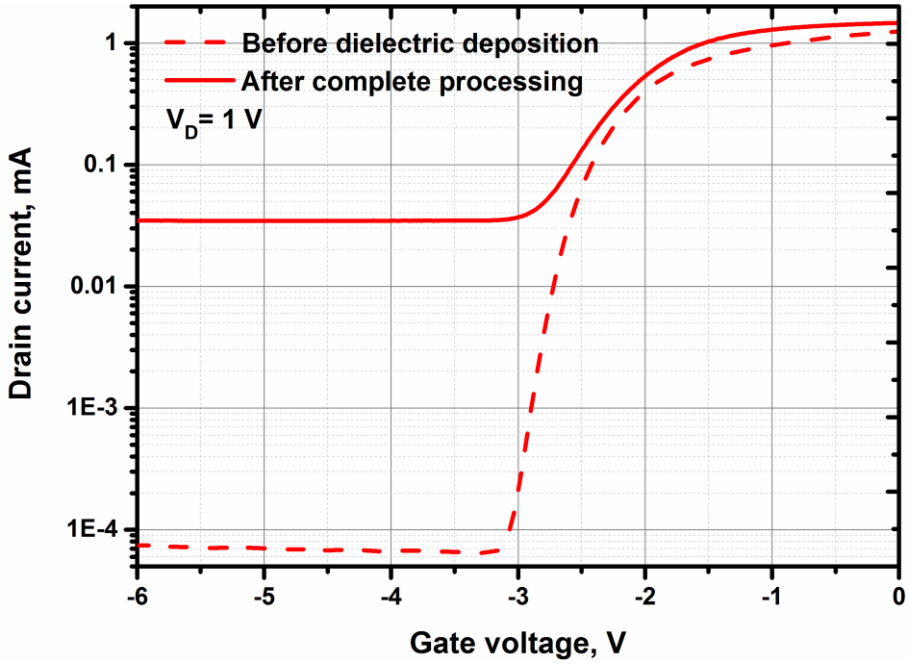


Figure 5.3: Transfer current-voltage characteristic of the linear GaN HEMT with L_{DG} = 17 µm.

5.2.2 Linear GaN-on-Diamond HEMTs with source FP

The photograph of the fabricated linear GaN-on-Diamond transistor with source field plate is shown in fig. 5.4.

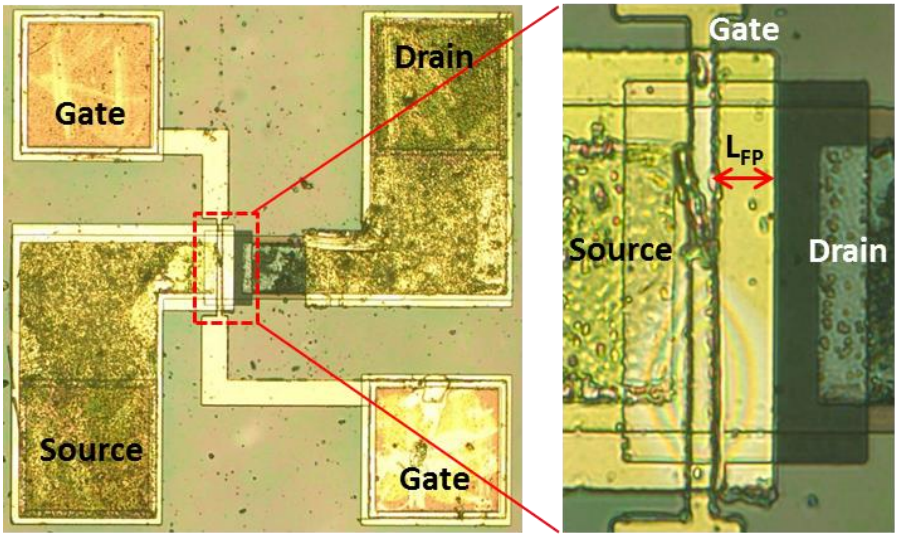


Figure 5.4: Fabricated linear GaN-on-Diamond HEMT with source field plate (top view photograph).

Figs. 5.5 (a)-(b) show output and transfer electrical characteristics of the GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 µm and source

field plate L_{FP} = 11 µm. The threshold voltage (V_{TH}) of the device obtained from transfer characteristic is ~ - 2.9 V. The specific on-state resistance (R_{ON}.A) is ~ 9.7 mΩ.cm^2.

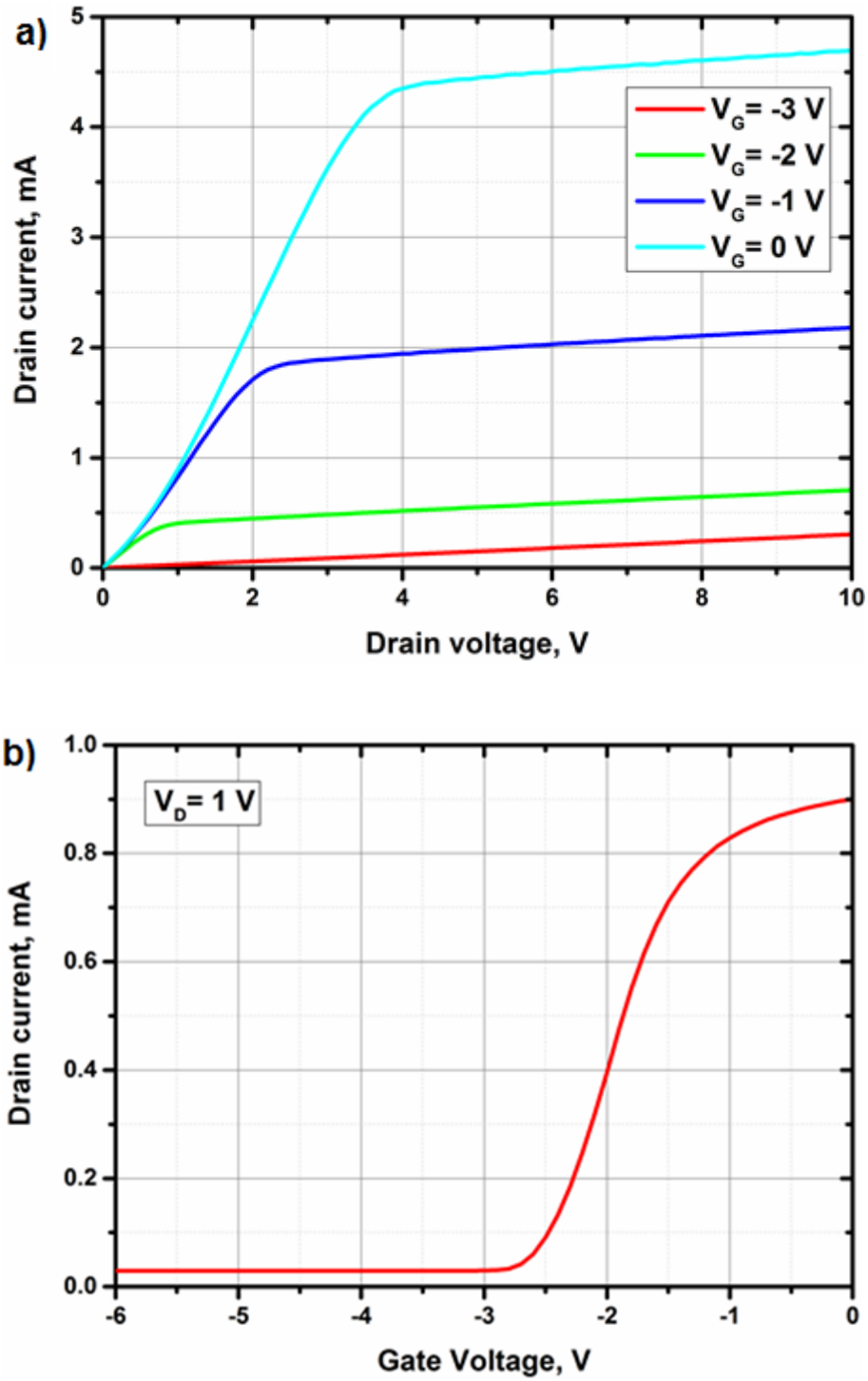


Figure 5.5: Electrical characteristics of the GaN-on-Diamond HEMT with L_{DG} = 17 µm and SFP L_{FP} = 11 µm: a) output I-V; b) transfer I-V

5.2.3 Linear GaN-on-Diamond HEMTs with source and drain FPs

The photograph of the fabricated linear GaN-on-Diamond transistor with source and drain field plates is shown in fig. 5.6.

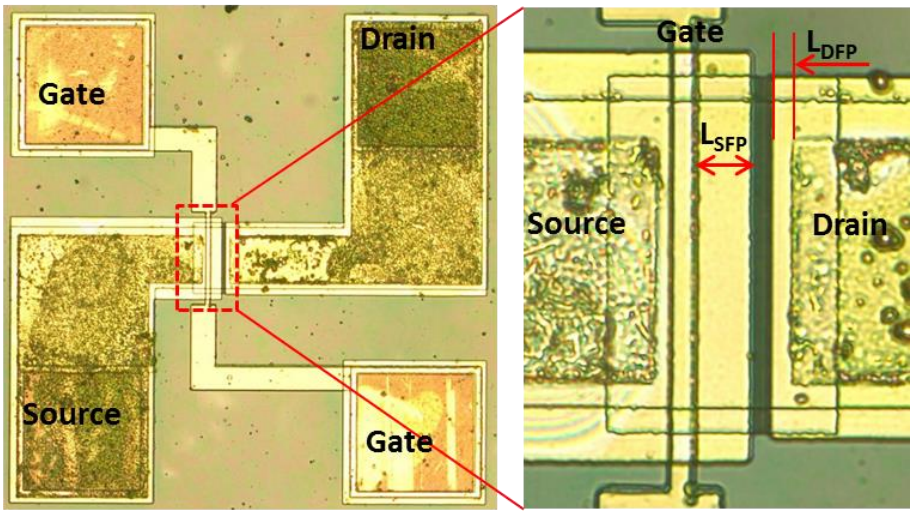
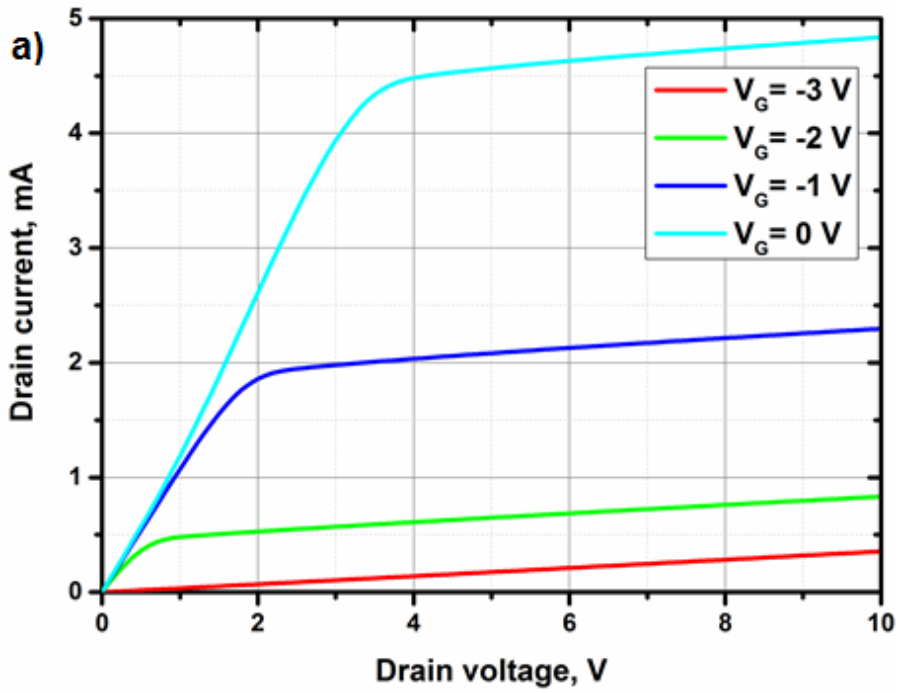


Figure 5.6: Fabricated linear GaN-on-Diamond HEMT with source and drain field plates (top view photograph).

Figs. 5.7 (a)-(b) show output and transfer electrical characteristics of the GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 µm, source field plate L_{SFP} = 11 µm, and drain field plate L_{DFP} = 2.5 µm. The threshold voltage (V_{TH}) of the device obtained from transfer characteristic is ~ - 2.9 V. The specific on-state resistance (R_{ON}.A) is ~ 8.6 mΩ.cm^2.



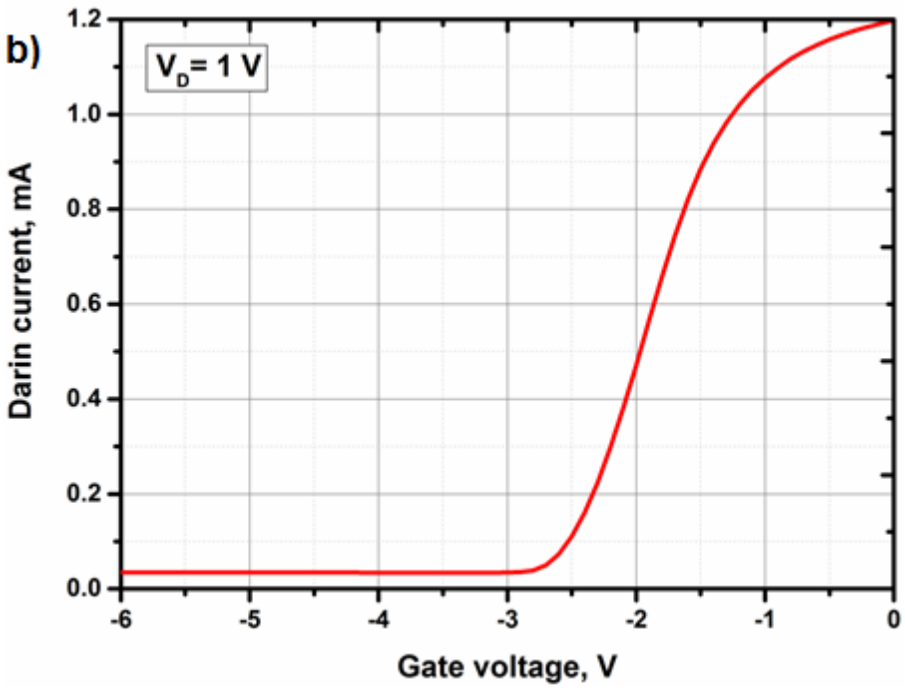


Figure 5.7: I – V characteristics of the device with L_{DG} = 17 µm, source field plate L_{SFP} = 11 µm, and drain field plate L_{DFP} = 2.5 µm: a) output; b) transfer.

5.2.4 Linear GaN-on-Diamond HEMTs with non-uniform SFP

The photograph of the fabricated linear GaN-on-Diamond transistor with non-uniform source field plate is shown in Fig. 5.8.

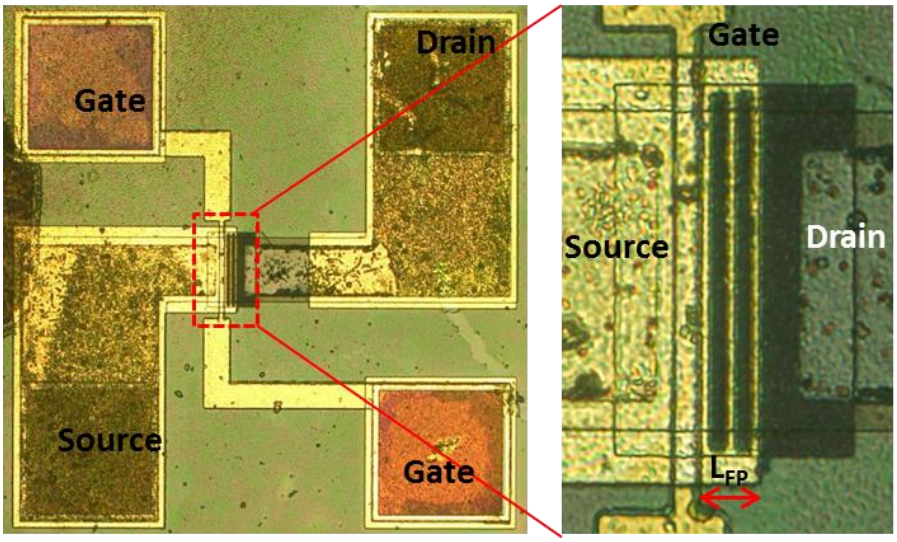


Figure 5.8: Fabricated linear GaN-on-Diamond HEMT with non-uniform source field plate (top view photograph).

Figs. 5.9 (a)-(b) show output and transfer electrical characteristics of the GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 µm and non-uniform source field plate L_{FP} = 11 µm. The threshold voltage (V_{TH}) of the device obtained from transfer characteristic is ~ - 3 V. The specific on-state resistance (R_{ON}.A) is ~ 8.3 mΩ.cm^2.

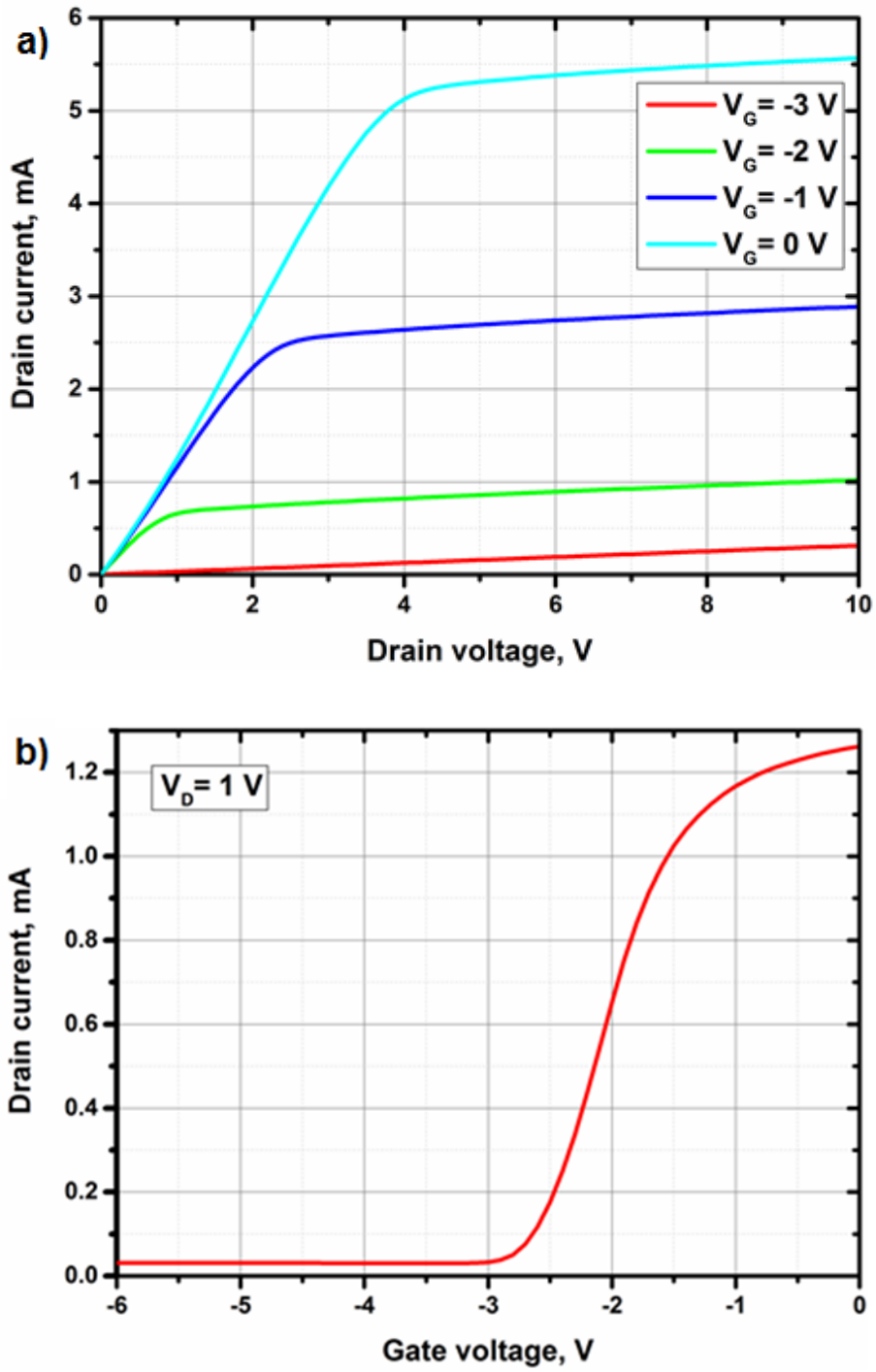


Figure 5.9: I – V characteristics of the device with L_{DG} = 17 µm and non-uniform source field plate L_{FP} = 11 µm: a) output; b) transfer.

5.2.5 Linear GaN-on-Diamond HEMTs with non-uniform source and drain FPs

The photograph of the fabricated linear GaN-on-Diamond transistor with non-uniform source field plate and drain field plate is shown in fig. 5.10.

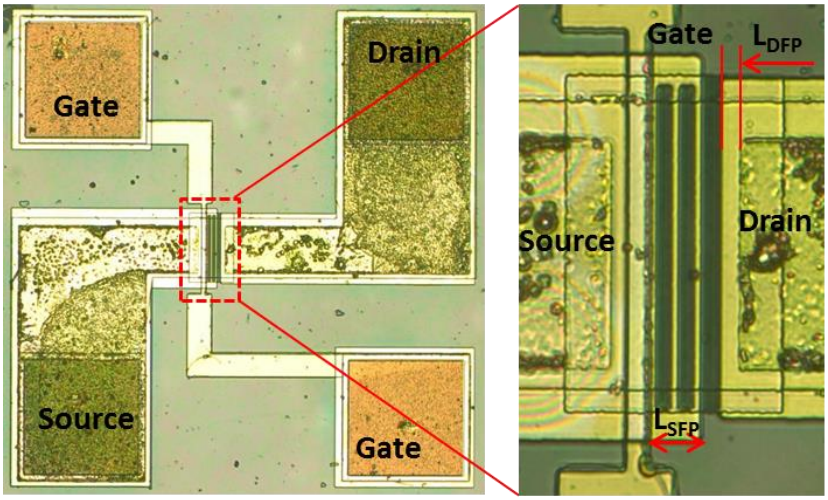
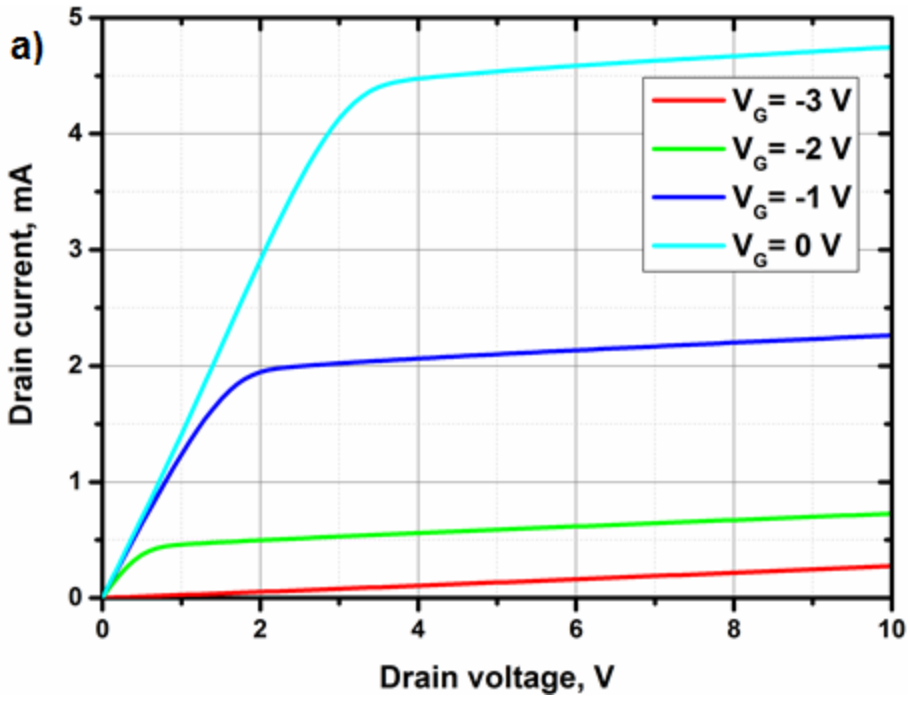


Figure 5.10: Fabricated linear AlGaN/GaN HEMT with non-uniform source field plate and drain field plate (top view photograph).

Figs. 5.11 (a)-(b) show output and transfer electrical characteristics of the GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 µm, non-uniform source field plate L_{SFP} = 11 µm, and drain field plate L_{DFP} = 2.5 µm. The threshold voltage (V_{TH}) of the device obtained from transfer characteristic is ~ - 2.8 V. The specific on-state resistance ($R_{ON}.A$) is ~ 8 mΩ.cm^2.



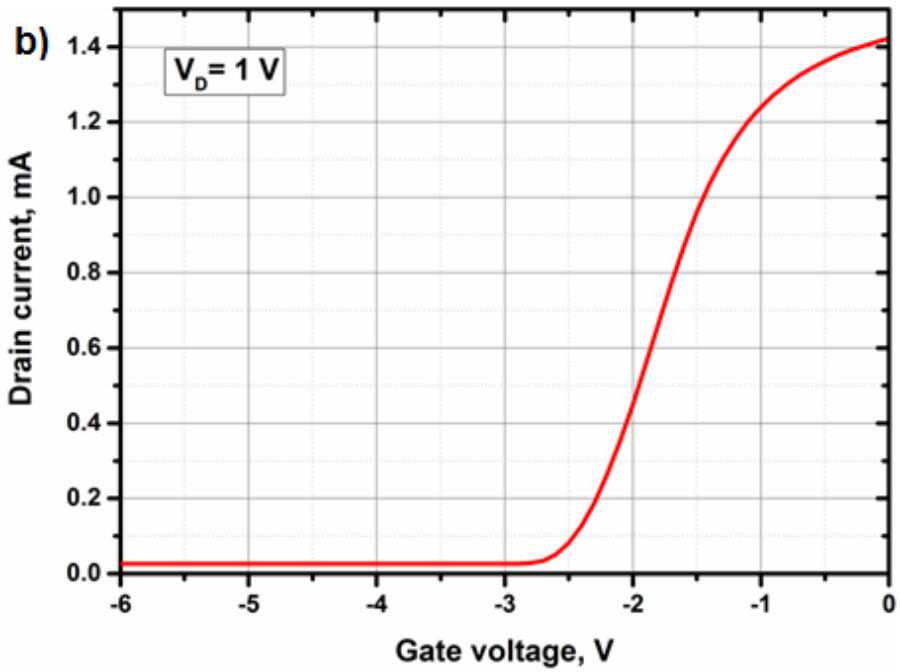


Figure 5.11: I – V characteristics of the device with L_{DG} = 17 µm, non-uniform source field plate L_{SFP} = 11 µm, and drain field plate L_{DFP} = 11 µm: a) output; b) transfer.

Table 5.1 summarises the key electrical results for each of the devices with LDG = 17 µm. All linear devices have threshold voltage of ~ - 3 V and specific on-state resistance in the range of 8 – 10 mΩ.cm^2 which is in good agreement with the simulation results (V_{TH} = ~ -3 V, R_{ON}.A = ~ 9.5 mΩ.cm^2) presented in Section 3.3.

Table 5.1: Key results of electrical characterisation.

Device	**V_{TH}, V**	**R_{ON}.A, mΩ.cm^2**
Linear (W_G = 50 µm):		
w/o FP	-3.17	8.1
With source FP	-2.9	9.7
With source and drain FP	-2.9	8.6
With non-uniform source FP	-3	8.3
With non-uniform source and drain FP	-2.8	8

5.2.6 Bidirectional GaN-on-Diamond HEMTs

The photograph of the fabricated GaN-on-diamond bidirectional transistor is shown in Fig. 5.12.

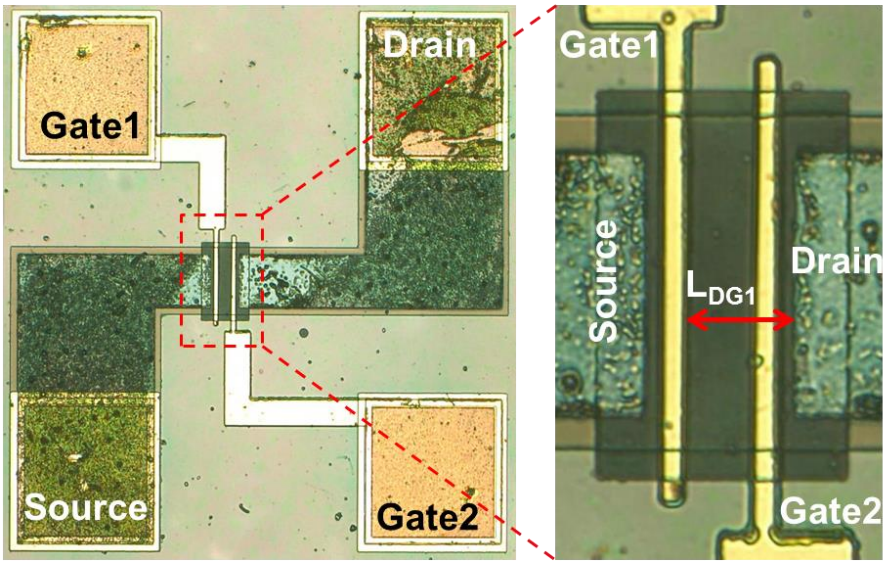


Figure 5.12: Fabricated bidirectional AlGaN/GaN HEMT (top view photograph).

Fig. 5.13 (a) shows typical transfer current-voltage characteristics of the fabricated bidirectional GaN-on-Diamond HEMTs with gate width $W_{G1} = W_{G2} = 50$ μm, drift length $L_{DG1} = L_{SG2} = 17$ μm, and gate length $L_{G1} = L_{G2} = 3$ μm. From the transfer I-V characteristics, it is apparent that the drain current of the device is effectively controlled by Gate-1 (voltage V_{G1S}) in forward direction (current flow from D electrode to S electrode (Fig. 5.12) and by Gate-2 (voltage V_{G2D}) in the reverse direction (current flow from S electrode to D electrode (Fig. 5.12). The measured threshold voltage is found to be around - 3 V. Fig. 5.13 (b) shows output I-V characteristics of the bidirectional HEMT. The device has symmetrical characteristics in the both directions. The specific on-state resistance of the bidirectional HEMT, calculated from the output I-V characteristic is ~ 10 $m\Omega.cm^2$.

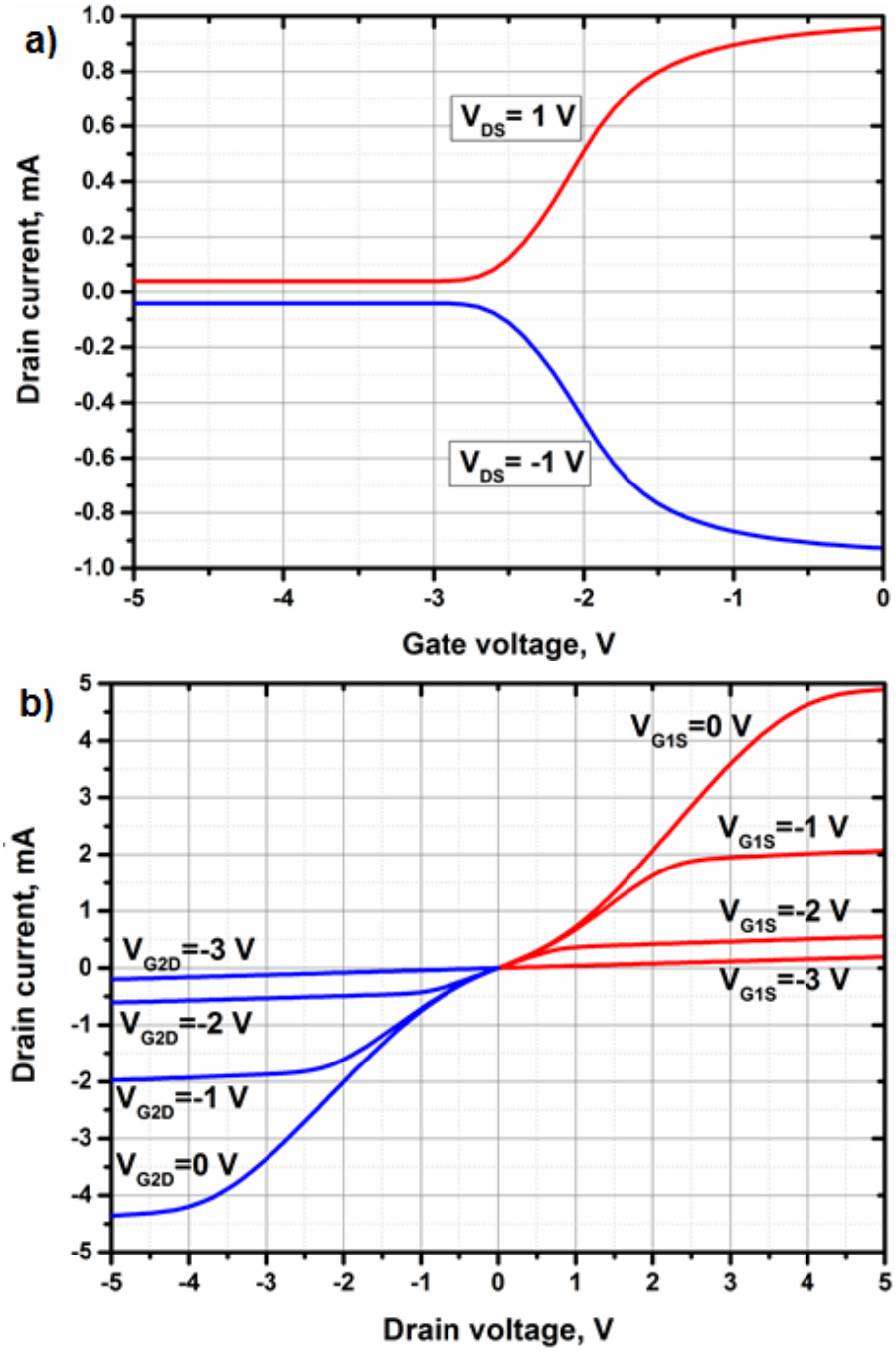


Figure 5.13: Electrical characteristics of the bidirectional HEMT: a) transfer I-V; b) output I-V.

5.2.7 Circular GaN-on-Diamond HEMTs without source FP

The photograph of the fabricated circular GaN-on-diamond transistor without any field plate is shown in fig. 5.14.

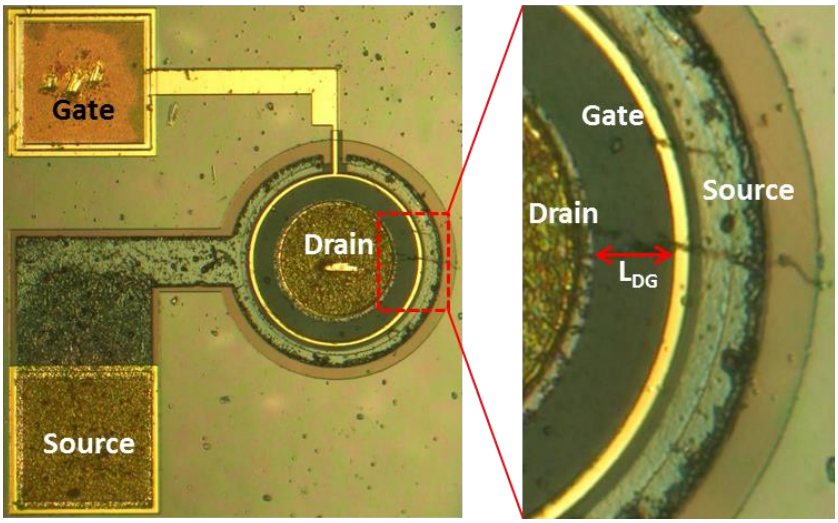
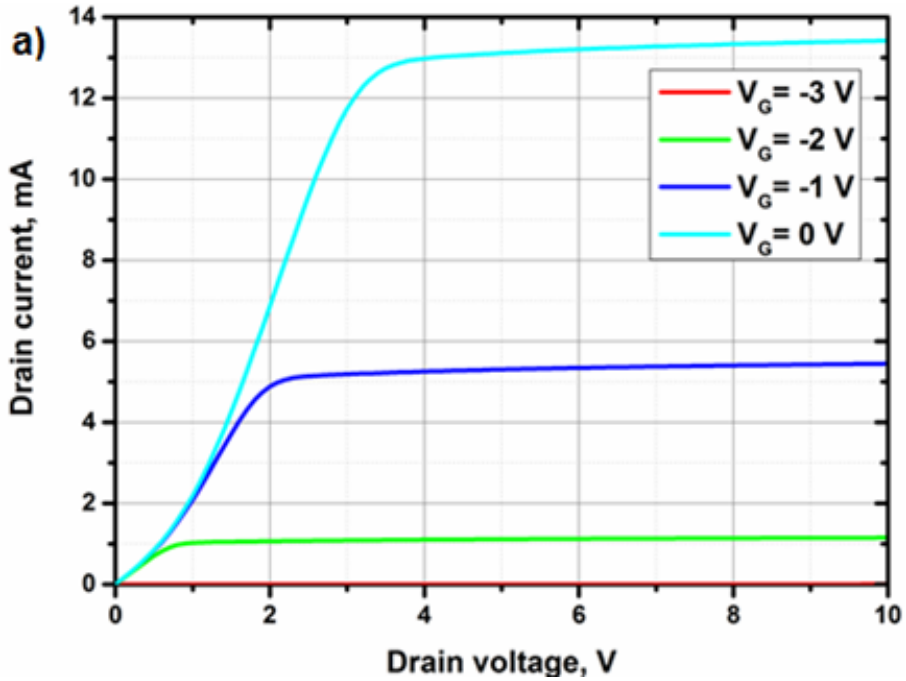


Figure 5.14: Fabricated circular AlGaN/GaN HEMT (top view photograph).

Figs. 5.15 (a)-(b) show output and transfer electrical characteristics of the circular GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 μm. The off-state leakage of the circular devices is at least two orders of magnitude smaller than the leakage of the linear devices due to their self-enclosed structure [66]. The threshold voltage (V_{TH}) of the device obtained from transfer characteristic is ~ - 3.1 V. The specific on-state resistance (R_{ON}.A) is ~ 23.2 mΩ.cm^2. The substantial increase in specific on-state resistance of circular devices compared to linear devices can be attributed to inhomogeneous current distribution due to different device design.



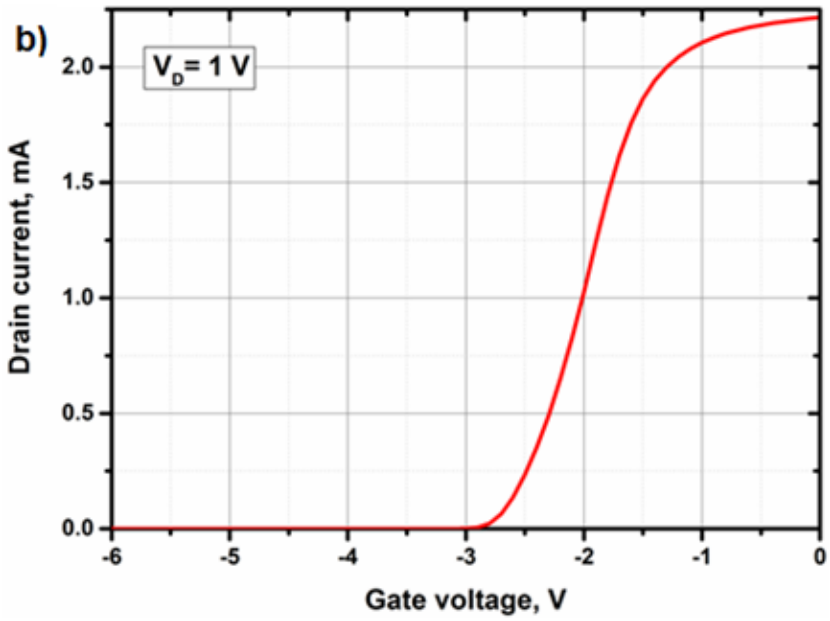


Figure 5.15: I – V characteristics of the circular HEMT with L_{DG} = 17 µm: a) output; b) transfer.

5.2.8 Circular GaN-on-Diamond HEMTs with source FP

The photograph of the fabricated circular GaN-on-diamond transistor with source field plate is shown in fig. 5.16.

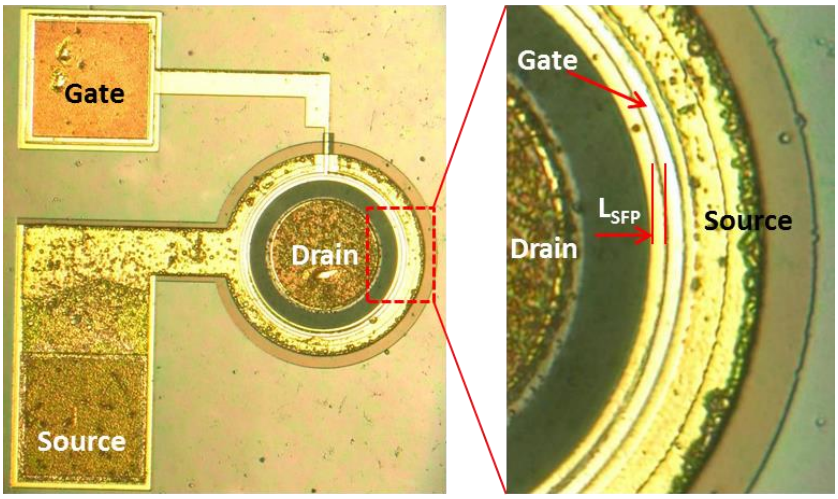


Figure 5.16: Fabricated circular GaN-on-Diamond HEMT with source field plate (top view photograph).

Figs. 5.17 (a)-(b) show output and transfer electrical characteristics of the circular GaN-on-Diamond HEMT with gate-to-drain drift length L_{DG} = 17 µm and source field plate L_{SFP} = 3 µm. The threshold voltage (V_{TH}) of the device obtained

from transfer characteristic is ~ - 3.1 V. The specific on-state resistance (R_{ON}.A) is ~ 21.1 mΩ.cm^2.

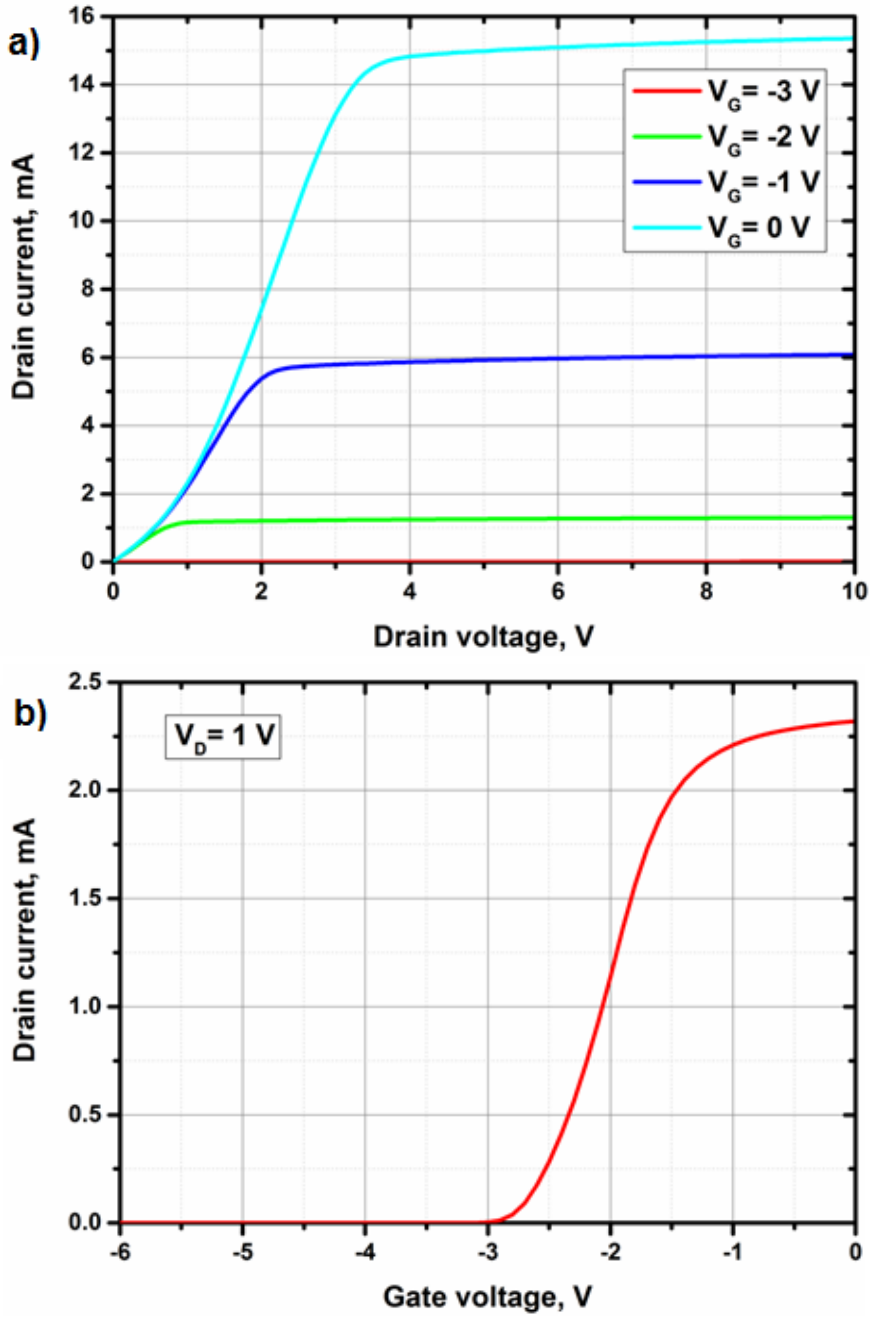


Figure 5.17: I – V characteristics of the circular HEMT with L_{DG} = 17 µm and source field plate L_{SFP} = 3 µm: a) output; b) transfer.

Table 5.2 summarises the key electrical results for each of the devices with L_{DG} = 17 µm. The substantial increase in specific on-state resistance of circular devices can be attributed to inhomogeneous current distribution due to device design.

Table 5.2: Key results of electrical characterisation.

Device	**V_{TH}, V**	**R_{ON}.A, mΩ.cm^2**
Linear (W_G = 50 µm):		
w/o FP	-3.17 V	8.1
With source FP	-2.9	9.7
With source and drain FP	-2.9	8.6
With non-uniform source FP	-3	8.3
With non-uniform source and drain FP	-2.8	8
Bidirectional	-3 in both directions	10.1; 10.6
Circular (W_G = 430 µm):		
w/o FP	-3.1	23.2
With source FP	-3.1	21.1

5.3 Temperature characterisation

Output I – V characteristics

Fig. 5.18 shows output current-voltage characteristics of the linear GaN-on-Diamond HEMT (L_{DG} = 11 µm) measured at various temperatures (from - 80 ^{0}C to 90 ^{0}C). The measurement was performed on a TTP4 cryogenic manipulated-probe station. It is apparent from the graph that as temperature rises the drain current reduces. This could be explained by reduction of carrier mobility due to increased number of collisions at higher temperature [69].

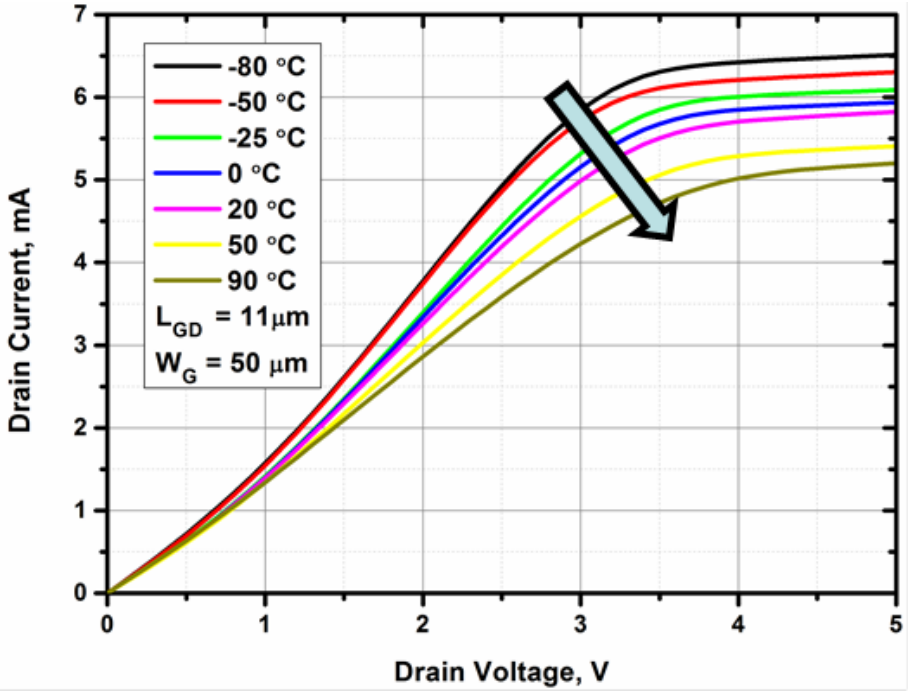


Figure 5.18: Output I-V characteristics of the linear GaN-based HEMT (without field plate) with respect to temperature.

Fig. 5.19 shows the trend of specific on-state resistance (R_{ON}.A) (measured at V_{DS} = 2 V and V_{GS} = 0 V) as well as the drain saturation current I_{DSAT} (at V_{DS} = 4 V and V_{GS} = 0 V) of the device with respect to temperature. A linear trend has been observed for both parameters with a temperature coefficient of ~ 5.85 μΩ.cm^2/ ^{0}C and - 8.62 μA/ ^{0}C for R_{ON}.A and I_{DSAT} respectively. Similar trend has been observed in the literature for GaN-on-Si HEMTs [70]. The increase in R_{ON}.A and decrease in I_{DSAT} at high temperatures can be primarily attributed to the degradation of the 2DEG mobility [70].

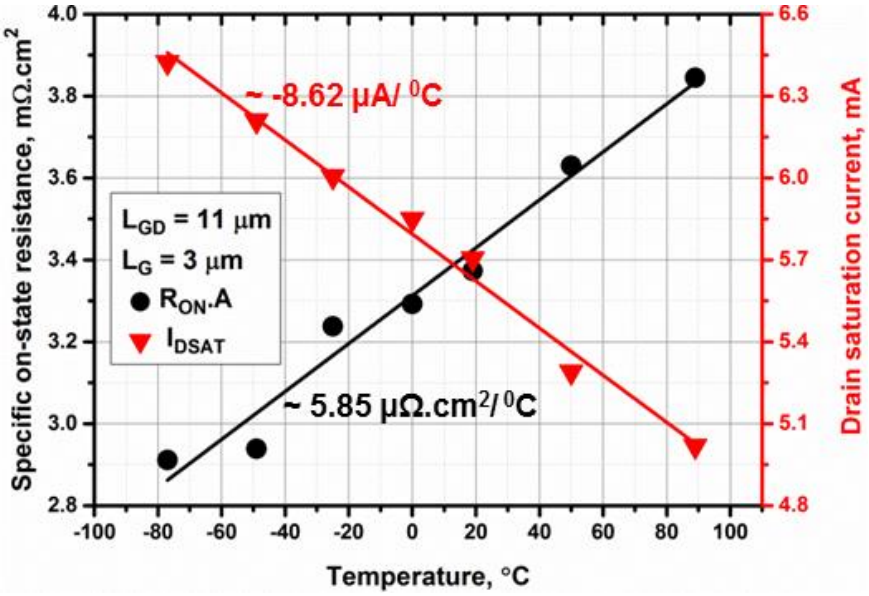


Figure 5.19: Specific on-state resistance (at V_{DS} = 2V and V_{GS} = 0V) and drain saturation current (at V_{DS} = 4V and V_{GS} = 0V) of a conventional AlGaN/GaN HEMT (without field plate) with respect to temperature.

Capacitance – voltage measurements

Small-signal capacitance – voltage (CV) characteristics were measured using Agilent B1505A semiconductor device analyzer with an in-built multi-frequency capacitance measurement unit (MFCMU). Being wafer-level measurements, phase compensation as well as open and short corrections were performed on the setup before proceeding with the actual device measurements. Fig. 5.20 shows CV characteristics of the circular device (L_{DG} = 17 μm) with source field plate (L_{SFP} = 3 μm) measured at 1 MHz and various temperatures (25 ^{0}C – 125 ^{0}C). The source terminal of the device was left floating during this measurement. The depletion of

the 2DEG under the gate starts at drain voltage V_D ~ 3 V corresponding to the threshold voltage V_{TH} ~ - 3 V.

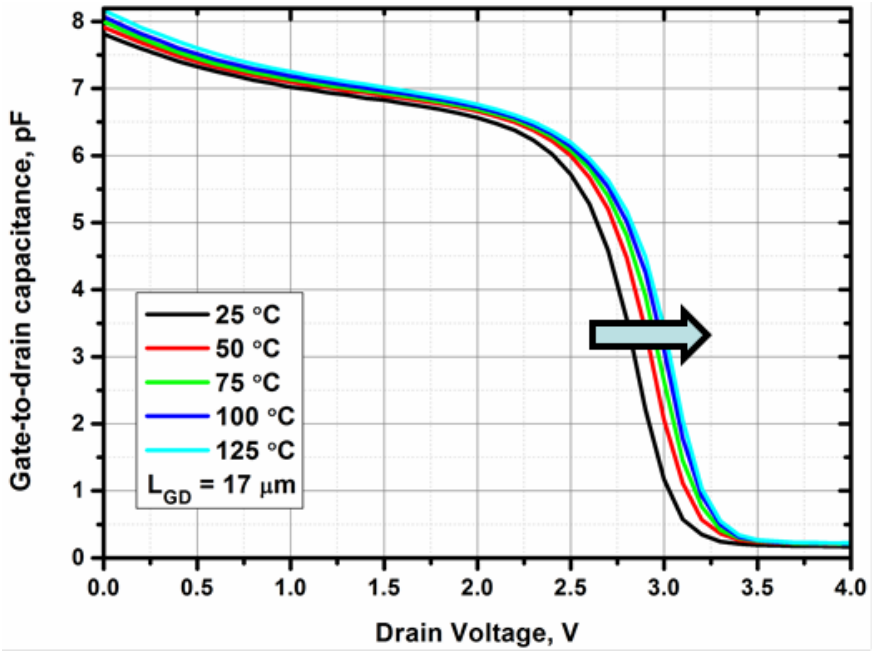


Figure 5.20: Capacitance – voltage characteristics of a high voltage circular AlGaN/GaN HEMT performed at various temperatures.

The apparent carrier density (N_{CV}) as extracted from the CV data is shown in Fig. 5.21. The peak of apparent carrier concentration N_{CV} = 2.3e19 cm^{-3} is observable at a depth of ~ 19 nm which also corresponds to the location of the 2DEG at the AlGaN/GaN heterointerface.

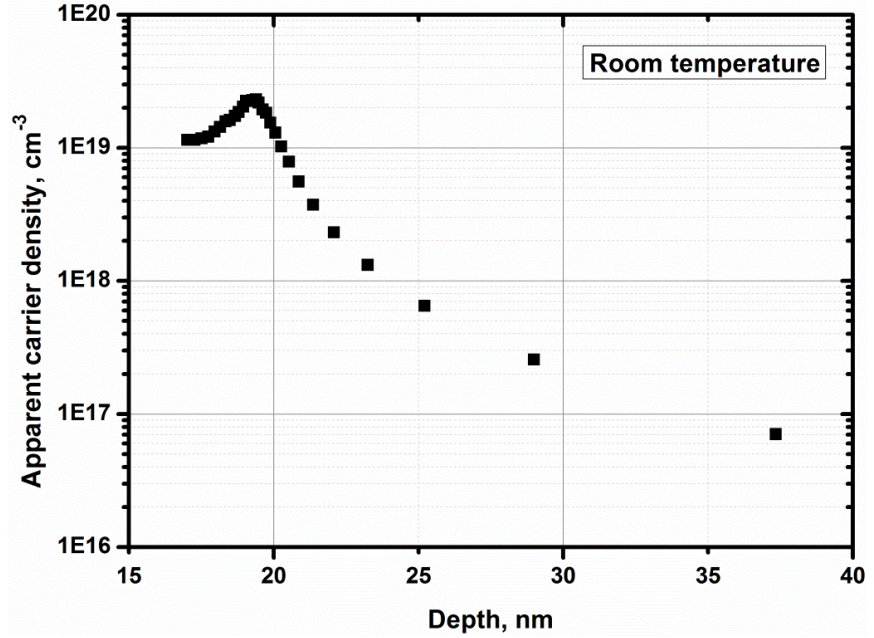


Figure 5.21: Extracted from the CV characteristics, apparent carrier density profile of the circular GaN-on-Diamond HEMT.

Fig. 5.22 shows the trend of V_{TH} as well as apparent carrier concentration with respect to temperature. The capacitance slightly increases when the temperature rises which is leading to the shift of V_{TH} magnitude towards higher values. The temperature coefficients for the sheet carrier concentration and V_{TH} are found to be ~ 7 x 10^9 cm^{-2}/ ^{0}C and - 2.8 mV/ ^{0}C respectively. The increase in the sheet carrier concentration can be attributed to thermally generated carriers in bulk-regions of the heterostructure [114].

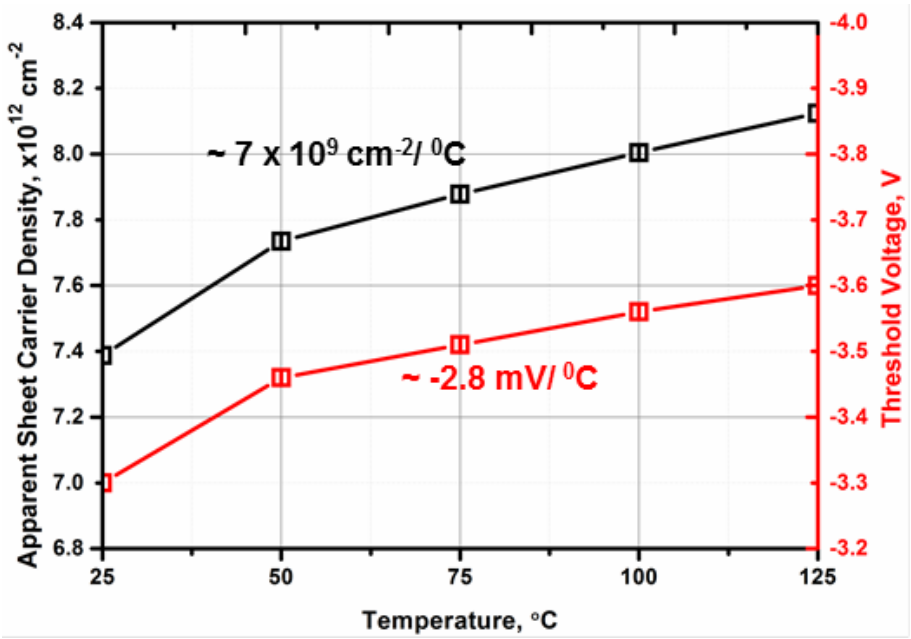


Figure 5.22: Variation of the apparent sheet carrier concentration and threshold voltage with respect to temperature (extracted from the CV measurements).

5.4 Breakdown voltage measurements

Off-state Breakdown Voltage (BV_{DSS}) of the circular devices with and without SFP and with various gate-to-drain separations (L_{GD}) was measured under Fluorinert ambient by using a Sony Tektronix 370 programmable curve tracer and a bench-top power supply. The bench-top power supply was used to bias the gate-to-source voltage (V_{GS}) of the HEMT at - 5V (Threshold Voltage V_{TH} ~ - 3 V). The drain voltage was biased using the curve tracer by sweeping the voltage gradually (pulsed mode) from 0 V to the point of electrical breakdown. A simplified illustration of the setup has been shown in Fig. 5.23.

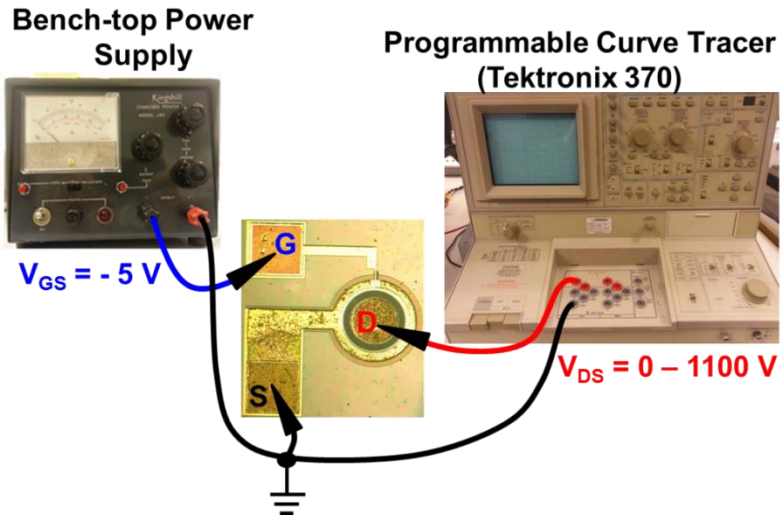


Figure 5.23: Simplified illustration of the setup for breakdown voltage measurements.

Fig. 5.24 depicts the measured breakdown voltage values (destructive) of devices with and without SFP with respect to L_{GD}. The BV_{DSS} of devices without SFP and varying L_{GD} changes only slightly ~ 550 - 600 V, which corresponds to the average breakdown field strength of ~ 0.18 MV/cm. The devices with SFP and L_{GD} = 13 and 17 µm, show considerably higher BV_{DSS} of ~ 800 V and 1100 V respectively. This corresponds to an average breakdown field strength of ~ 0.72 MV/cm, illustrating the enhanced electric field management achieved with the SFP. It has to be noted that the circular devices fabricated in this work even without SFP still show quite high breakdown voltage which is in agreement with other published results for AlGaN/GaN HEMTs on SiC and sapphire substrates with similar circular/square gate design [71, 72]. This could be explained by better electric field distribution due to the circular gate design. For a linear layout device local crowding of the electric field might happen at the area where gate finger crosses mesa etch region, while for a circular device the electric field distributes uniformly along the gate contact [65, 99]. The GaN-on-Diamond epi-wafers used here were manufactured in late 2013 and the crystal quality is quite poor. Devices reported here represented the first-time that a power switching device has been made with GaN-on-Diamond albeit with epitaxy designed for RF applications. The performance shown here is expected to improve with epitaxy that has been better tailored for power electronic applications and improved crystal quality.

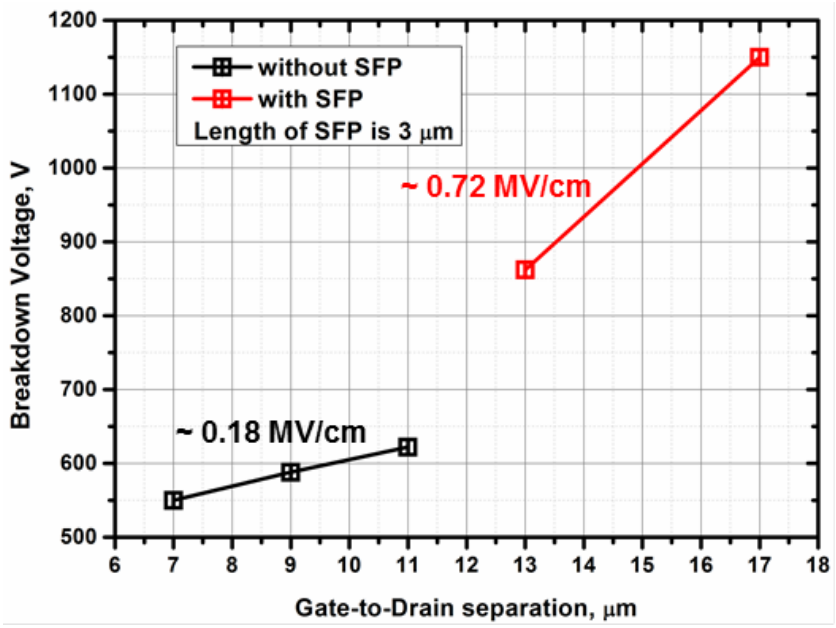


Figure 5.24: Breakdown voltage versus gate-to-drain drift length

Figs. 5.25 (a)-(b) show photographs of the circular HEMTs without and with source field plate after breakdown evaluation. The corresponding breakdown region has been demarcated and the breakdown behaviour is destructive.

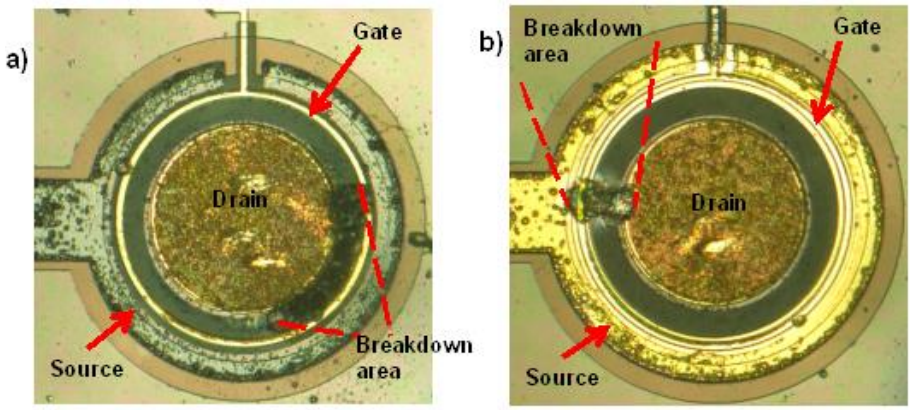


Figure 5.25: Top view photographs of circular HEMTs after breakdown measurements: a) without field plate and L_{DG} = 11 μm; b) with field plate and L_{DG} = 17 μm (V_{BR} ~ 1100 V).

5.5 Conclusions

This chapter provided the detailed electrical characterisation results of AlGaN/GaN HEMTs on CVD Diamond substrate. I-V characterisation results showed that the linear and circular devices have the same threshold voltage of around ~ -3 V. The specific on-state resistance of circular devices (R_{ON}.A= ~ 21 – 23

$m\Omega.cm^2$) is more than two times higher than that of linear devices ($R_{ON}.A$= ~ 8 – 10 $m\Omega.cm^2$) which could be associated with the fabrication process. However, the off-state leakage current of the circular devices is at least two orders of magnitude smaller than the leakage of the linear devices due to their self-enclosed structure. Furthermore, for a linear layout device local crowding of the electric field might happen at the area where gate finger crosses mesa etch region, while for a circular device the electric field distributes uniformly along the gate contact. Therefore, the circular design devices (with improved fabrication process) are better for high voltage applications.

Fabricated circular AlGaN/GaN HEMTs with source field plate length of 3 μm and gate-to-drain separation of 17 μm have demonstrated an off-state breakdown voltage of ~ 1100 V. The systematic measurements of output I-V, transfer I-V, off-state breakdown voltage, capacitance – voltage characteristics and temperature characterisation results provide insights on the device performance and temperature dependence of the heterostructure characteristics. The GaN-on-Diamond epi-wafers used here were manufactured in late 2013. Devices reported here represented the first-time that a power switching device has been made with GaN-on-Diamond albeit with epitaxy designed for RF applications. The performance shown here is expected to improve with epitaxy that has been better tailored for power electronic applications.

Chapter 6

Optically-controlled AlGaN/GaN-based power transistor

6.1 Introduction

Optically controlled power semiconductor devices are promising candidates for high-power high-voltage applications. They provide key advantages over regular electrically controlled devices [73]. Firstly, controlling the power device by optical signal provides complete isolation between high voltage and low-voltage power stages. And secondly, there is no electromagnetic-interference of the control link between power stage and the controller [74]. The earlier studies on optically activated devices have been mainly concentrated on Si and GaAs-based devices. However, devices made from these materials have certain limitations such as breakdown voltage and current density. In comparison, wide direct bandgap GaN possess very attractive properties such as short carrier lifetime, high critical electric field strength and high optical absorption coefficient [75, 76].

This chapter will firstly provide a brief insight into the photogeneration phenomenon and the literature review on the photoconductive device, followed by proposition of a new concept of enhancement mode optically-controlled AlGaN/GaN based power transistor. Part of the discussions and results presented here has been published in the proceedings of ISPS 2014 [115].

6.2 Photogeneration phenomenon and photoconductive devices

The operation of power semiconductor device (PSD) is realised by the controlled motion of charged particles inside it. To operate a PSD we have to interrupt the balance of the charge carrier density. This might be done by external thermal energy (thermionic emission), electrical field (electrical injection), optical beam (optical injection). Photoconductive PSDs are a part of a specific category of electronic semiconductor devices in which the initiation of charge carrier transportation is realised using optical energy [77].

The operating principle of photoconductive PSDs is based on the photogeneration phenomenon. The illustration of this phenomenon is schematically shown in Fig. 6.1. Photogeneration is an action when an electron is excited to the conduction band from the valence band which is caused by an incident photon. Photogeneration can happen only if the energy of the photon hν (ν – light frequency and h – Planck's constant) is higher than the semiconductor's bandgap energy E_g and always occur as electron-hole pairs, because when an electron is excited from the valence band to the conduction band it always leaves behind a hole. These electron-hole pairs take part in current conduction in the device and since they are generated by light incidence, the device is called a photoconductive device [73].

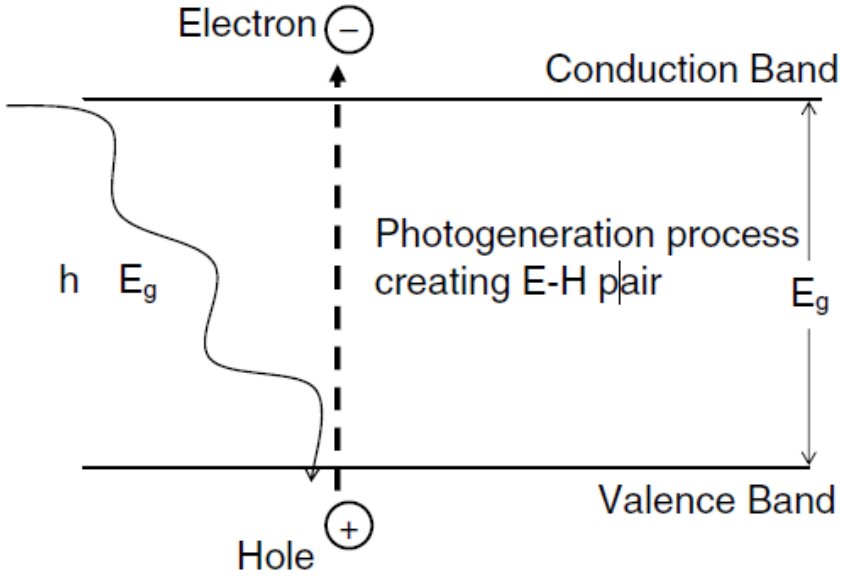


Figure 6.1: Illustration of photogeneration process caused by the incident photon [73].

6.3 Review of photoconductive devices in power electronics

All of the photoconductive or optically triggered devices operate on the photogeneration phenomenon of excess charge carriers which interrupts the equilibrium of the carrier density inside semiconductor and leads to current conduction [77]. Power electronic applications require specific properties from a semiconductor device such as large current handling capacity, high reverse voltage blocking capability, low on-state voltage drop, precise controllability, and low opening and closing delays. Low surface and contact defect densities, low radiation hardness, good thermal stability are other demands for better reliability and for

extreme applications (space and military applications) [78]. In the following sections there is a review of the important optically triggered devices and their pros and cons as a semiconductor switch.

6.3.1 A bulk optically controlled semiconductor switch (BOSS)

The concept of optically controlled bulk switches is based on quenching and excitation of photoconductivity in the semiconductor and has been introduced in [79]. These copper-doped semi-insulating GaAs-based devices are bistable, that is to say they require control signal only to switch them off and on, and they don't need the signal to keep the switch conducting [80]. They also don't have any depletion layers, since the quenching and excitation of photoconductivity happens uniformly in the whole volume of the material. This switch is triggered on by laser light with wavelength $\lambda = 1.06$ μm to produce majority carrier current conduction with high photoconductive gain. Switching the device off can be done at any point of the conduction state by activating another laser with $\lambda = 1.62$ μm which stimulates the quenching of photoconductivity by fast free carrier recombination. Fall and rise times less than 10 nsec and conduction periods greater than 1 μsec are possible with GaAs-based inexpensive switches. Moreover, an arbitrary extension of the conduction time is possible by implementing multiple laser pulses with $\lambda = 1.06$ μm prior to a single conduction-terminating laser pulse.

The main disadvantage of the BOSS is the requirement of two lasers with different wavelengths which increases cost and complexity.

6.3.2 Light triggered thyristor

A thyristor is a bistable, regenerative semiconductor switch which is used mainly for high-voltage direct current transmission systems. A light-triggered thyristor (LTT) is an elegant device for a lot of high power applications, since an LTT does not require most of thyristor level electronic parts which an electrically triggered thyristor (ETT) requires, resulting in more compact system design and higher reliability. Furthermore, the LTT has much better electromagnetic noise immunity and provides electrical isolation due to the nature of triggering signal [81].

Optical triggering of the device is realised by localised illumination of an optical well which is located in the centre and surrounded by amplifying thyristor

and pilot thyristor structure. The generated pairs of electrons and holes driven by anode bias start a current flowing in the lateral direction from the illuminated area. This photocurrent switches on the pilot thyristor which subsequently starts the amplifying thyristor. The amplifying thyristor then drives the gate of the main device. Sometimes, several amplifying thyristors are used in relation to the device's current requirements. Fig. 6.2 illustrates a schematic LTT structure with one optical gate and three amplifying gates [82].

Light triggered thyristors are usually made from III-V compounds such as InP, GaAs, AlGaAs, due to their higher radiation, temperature, and breakdown handling capability in comparison to silicon. Other advantages of these direct bandgap materials are better optical efficiency and possibility of heterostructures [83].

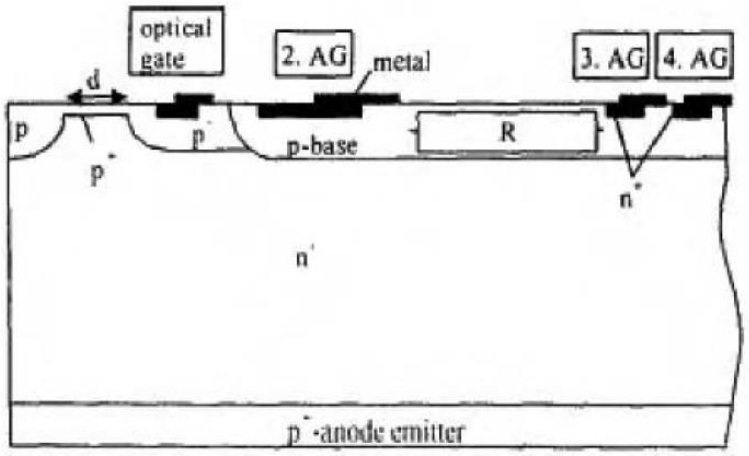


Figure 6.2: Schematic structure of a light triggered thyristor, with an optical gate, an integrated breakover diode, and three amplifying gates [82].

Whereas successful fabrication of LTTs and their use have been shown for pulsed power switching applications [84, 85, 86], there are several problems such as edge breakdown, surface degradation and defects in the base layer which can cause premature breakdown at voltages significantly lower than the ones predicted by theory [86]. Another disadvantage of LTT is the fact that like most power thyristors, they are not suitable for rapid switching.

6.3.3 Light triggered MOSFET

MOSFET as a unipolar device is a good choice for high frequency applications since there isn't any storage delay introduced by minority carriers in unipolar conduction, as happens in the case of thyristor or BJT. Other advantages of MOSFET are good di/dt and dv/dt handling capabilities and a positive temperature coefficient, which leads to easier paralleling of devices when compared to thyristor or BJT, by eliminating the possibility of thermal runway [78].

The optical control of power MOSFETs is rarely studied. There are reports about optical switching of MOSFET [87, 88], but they are mainly focused on low power sensor or optical communication applications. Optically triggered power MOSFET simulation study has been reported in [89]. The structure of the reported device consists of Si DMOS, GaAs photoconductive switch and GaAs photodiode as demonstrated in Fig. 6.3. In order to turn on the device the GaAs-based photodiode is illuminated by optical pulse and photogenerated current starts to flow. This photocurrent charges the capacitance of the gate of the Si-based DMOS over the threshold voltage. In order to turn-off the device another optical pulse illuminates the GaAs-based photoconductive switch to alter its resistance and discharge the DMOS gate capacitance [93].

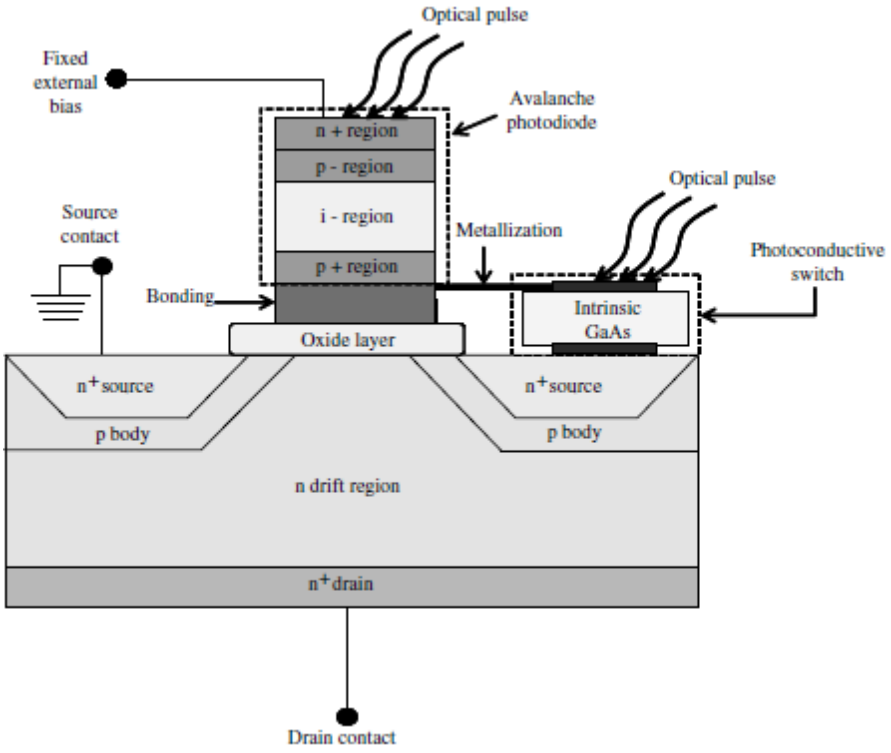


Figure 6.3: Schematic structure of optically activated power MOSFET, illustrating the activating avalanche photodiode, photoconductive switch, and MOSFET [73].

6.3.4 Light triggered IGBT

The IGBT is a bipolar device with higher current and voltage handling capability but lower operation frequency than MOSFET. However, its frequency of operation is much greater in comparison to a power BJT. In other words, IGBT is the device of choice for high current and voltage applications of relatively low frequency. An attempt to realise an optically triggered IGBT has been undertaken in [90] and the proposed device structure is shown in Fig. 6.4, a.

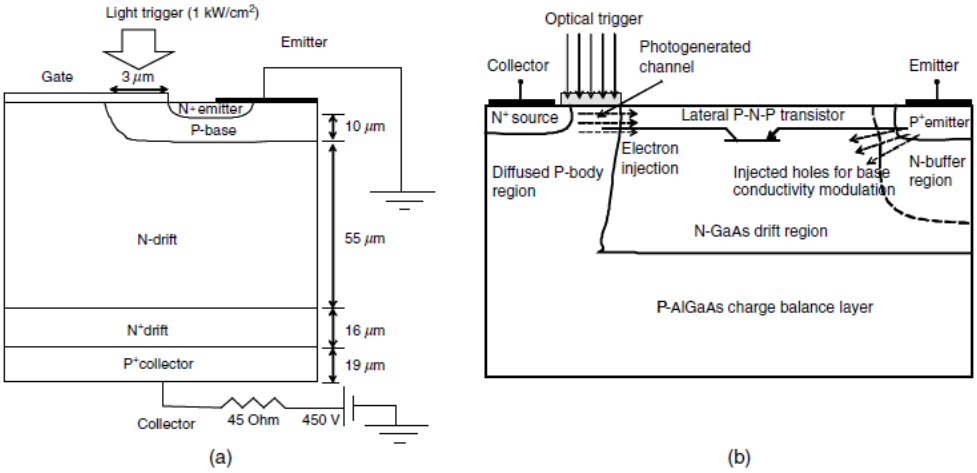


Figure 6.4: Schematic structure of: a) optical IGBT [90]; b) OGBT [91].

GaAs-AlGaAs based optically activated lateral power devices were the result of further research [91]. Fig. 6.4, b shows the optically gated bipolar transistor (OGBT). It exhibits high device gain owing to optical base conductivity modulation. OGBT has better switching times than conventional electrically controlled power bipolar transistors owing to shorter carrier lifetime in GaAs than in silicon.

6.3.5 Optically-triggered GaN-AlN-(4H)SiC vertical PSD

The earlier research on optically triggered devices has concentrated mainly on GaAs and Si-based devices. GaAs and Si are the materials of choice because of the good optical absorption coefficient and direct bandgap of the former and low cost of the latter. However, devices based on these materials have certain limitations such as low current-density and breakdown voltage because of the low thermal conductivity and bandgap of these materials. GaN and SiC are the semiconductor materials with very attractive properties including large bandgap energies, high breakdown fields, and high thermal conductivities. Moreover, the GaN material has short (sub-nanosecond) carrier lifetime and good optical absorption coefficient α (the

values of α at 300 k and 3.42 eV is around 0.8 – 4 × 10^5 cm^{-1}) [76, 92, 123, 124]. Recently an optically triggered thyristor based on SiC material has been proposed. The thyristor structure has been chosen due to its high gain which somewhat offsets the low optical absorption coefficient of SiC thereby preventing the necessity in an expensive high-power short-wavelength laser. Unfortunately, the thyristor structure is not suitable for high frequency applications due to its inefficient turn-off characteristics. Recently, a new optically-activated GaN-AlN-(4H)SiC-based vertical PSD was proposed and the simulation results have been reported in [75]. The structure of the device is shown in Fig. 6.5. In order to benefit from thermal conductivity of SiC and good light absorption of GaN an attempt to synthesize these two materials has been made. So as to decrease the lattice mismatch between SiC and GaN a 1 nm thick AlN-buffer layer is introduced. To turn on or off the device an optical pulse with an intensity of 15 W/cm^2 and a wavelength of 350 nm is used. According to the published results the gain of the device is 190 (which is the ratio between collector current and generated photocurrent). However, the electron mobilities of bulk GaN and SiC are relatively low (~ 900 $cm^2/V{\cdot}s$ and ~ 700 $cm^2/V{\cdot}s$ respectively) which is a significant disadvantage [92, 98]. To push these values up for GaN the good approach is to take the benefit of the two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction. The mobility of 2DEG is commonly around 1200 – 2000 $cm^2/V{\cdot}s$ at room temperature which can be beneficial for both high-power and high-frequency applications [92, 98].

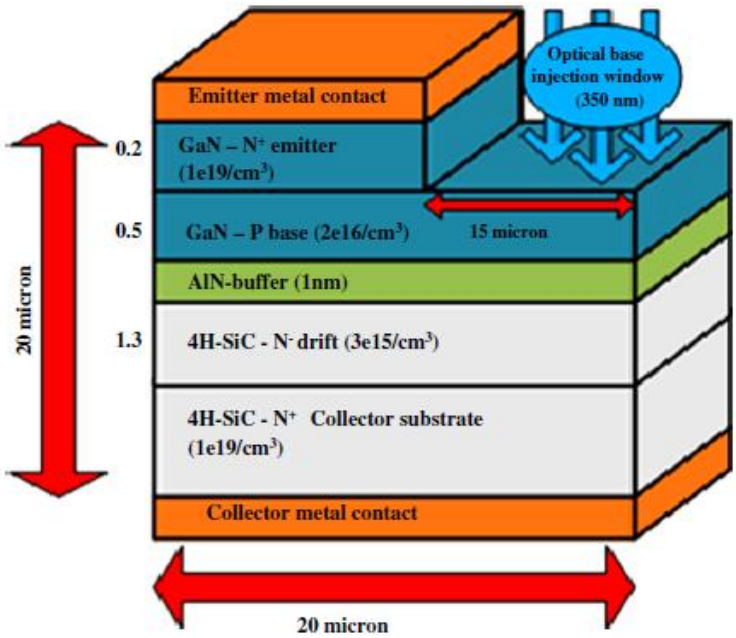


Figure 6.5: Optically triggered GaN-AlN-(4H)SiC vertical PSD [75].

6.3.6 Conclusion of the photoconductive devices review

The optically activated power semiconductor switches in power electronics have their advantages and disadvantages. One of the main advantages is complete isolation between high voltage and low-voltage power stages. Another, that there is no electromagnetic-interference of the control link between power stage and the controller [74]. The main disadvantage is the difficulty to design a high voltage device with small conduction losses and high current gain. The result is that there is no broadly used, commercially available optically-activated (controlled) power semiconductor device for power switching applications.

6.4 The novel optically controlled AlGaN/GaN-based PSD

The optically controlled device should have following properties [94]:

- Fast response speed, particularly lowest possible turn-on delay, and rise time, fast turn-off speed and low turn-off delay;
- Good responsivity to light so that small optical-triggering power can modulate the conductivity by large amount;
- Ability to handle large peak current which may flow through the device during turn-on and turn-off transient (for instance, to charge/discharge the input capacitance of a large current rated PSD);
- Ability to sustain large peak voltage for short time that may result during rapid transients of voltage and current changes in the PSD being coupled though parasitic capacitances.

These desired attributes presume that the material of the device has high optical absorption coefficient or be optically efficient and the device structure should have a high internal gain. Also, rapid response - requires a material with short minority carrier lifetime. GaN is a wide bandgap material with high breakdown field. Moreover, GaN has low carrier lifetime and good optical absorption coefficient [76, 92]. Another, very interesting property of GaN material is the possibility to create heterostructures with materials of wider bandgap such as AlGaN. As a result, a two-dimensional electron gas (2DEG) can be formed at the interface of such heterostructure. The 2DEG mobility is commonly around 1200 – 2000 $cm^2/V{\cdot}s$ at room temperature which can be beneficial for both high-power and high-frequency

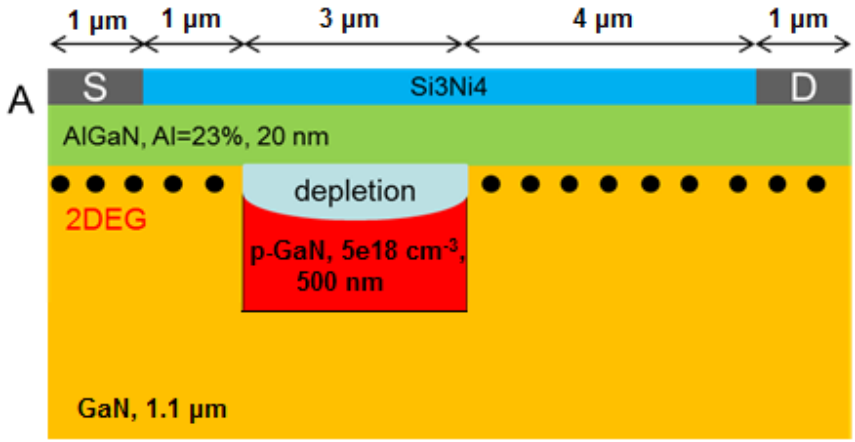
applications [92, 98]. All these properties make the GaN material a great candidate for optically triggered devices.

6.4.1 Device structure and operating principle

Fig. 6.6 shows cross-sectional schematics of the enhancement mode AlGaN/GaN-based optically controlled transistor (OCT). This is a lateral device with drain and source metal electrodes. In order to benefit from 2DEG formation, there is a thin AlGaN barrier layer on top of the GaN buffer layer, which is covered by an anti-reflective SiN coating in order to reduce reflection of light. The key part of the structure is a p-doped GaN region which locally depletes 2DEG channel and makes the device normally-off (Fig. 6.6, a). The main issue associated with the device design is p-GaN region. As in most wide-band-gap nitride and oxide materials, GaN can be easily doped n type but is difficult to dope p type. The insufficient hole concentration in p-type III-nitride compounds still remains one of the obstacles in achieving high-performance semiconductor devices. The low hole concentration in Mg-doped p-type GaN primarily results from [125]:

- The low solubility for Mg;
- The formation of compensating deep defects due to the heavy Mg doping;
- The large acceptor activation energies (~125-215 meV for Mg in GaN).

For these reasons, the hole concentration in uniformly Mg-doped GaN grown by metal organic chemical vapor deposition (MOCVD) method is generally difficult to exceed 1×10^{18} cm^{-3} [125].



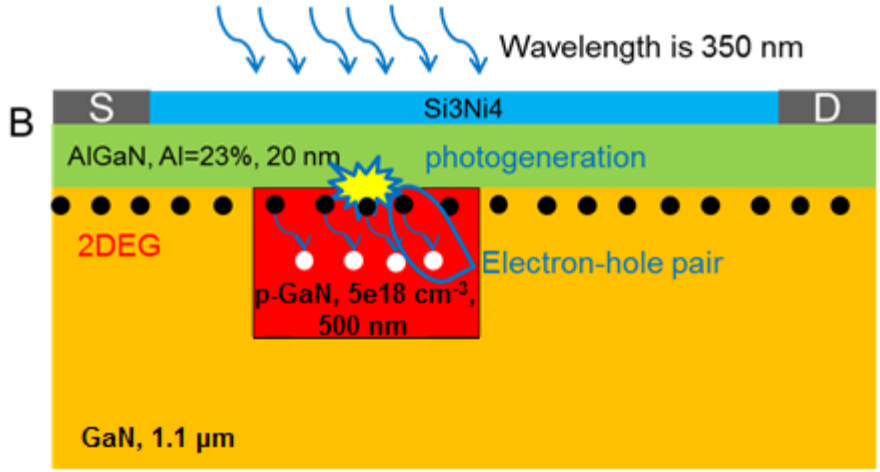


Figure 6.6: Schematic structure of the AlGaN/GaN OCT: a) 2DEG channel depleted by p-doped region; b) electron-hole plasma generation under illumination leads to channel recovery.

The operating principle of the AlGaN/GaN OCT is based on the photogeneration phenomenon [77, 95]. When the triggering light signal falls on the surface of the device it is absorbed in the optical window region, then penetrates through AlGaN barrier layer into the depletion region where it generates electron-hole pairs due to photogeneration phenomenon (Fig. 6.6, b). Further, the generated electrons are shifted towards the drain due to applied voltage and thereby the device shifts to the on-state. The generated holes stay around the p-doped body because their mobility is at least two orders of magnitude smaller than mobility of the electrons. If the light beam is sustained, then the channel resistivity of the device remains low and the device stays in the on-state. When the optical beam is off, the charge carriers start to recombine and the device returns to off-state condition with highly resistive channel.

6.4.2 Simulation results

The simulation of the device was carried out in physics-based two-dimensional numerical simulator package Silvaco ATLAS. LUMINOUS platform was used for the modelling of the optical pulse. The structure used for simulation is shown in Fig. 6.6, a. To switch the device on and off an optical pulse with a wavelength of 350 nm and power intensity of 7 W/cm^2 is incident on the surface of optical window above the p-doped region (Fig. 6.7).

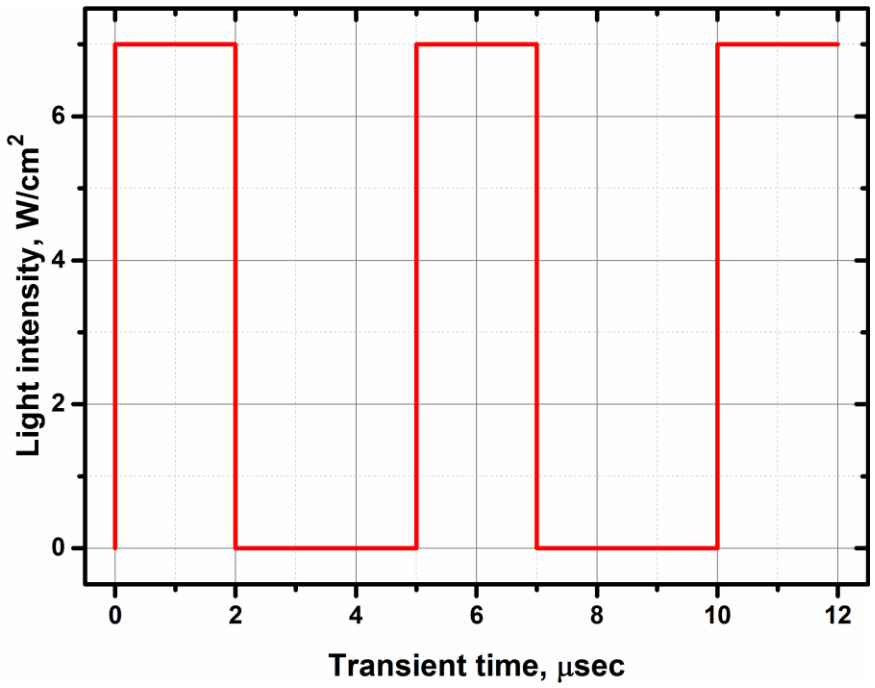


Figure 6.7: Light beam with an intensity of 7 W/cm^2 and a wavelength of 350 nm used to turn the PSD on or off.

Fig. 6.8 shows the photogeneration in the optically-controlled AlGaN/GaN-based transistor. Despite the fact that photogeneration gradually reduces with GaN depth it still has a high value within 500 nm. Fig. 6.9 shows that the photocurrent available in the structure is very high and almost equal to the source photocurrent which is due to the good optical absorption coefficient of GaN [75].

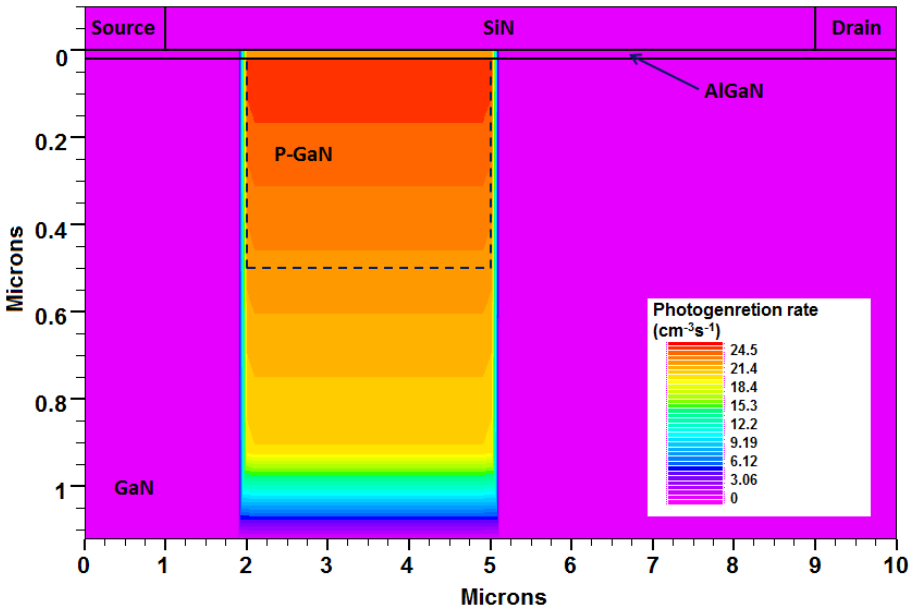


Figure 6.8: Simulated photogeneration rate in optically-controlled AlGaN/GaN-based PSD.

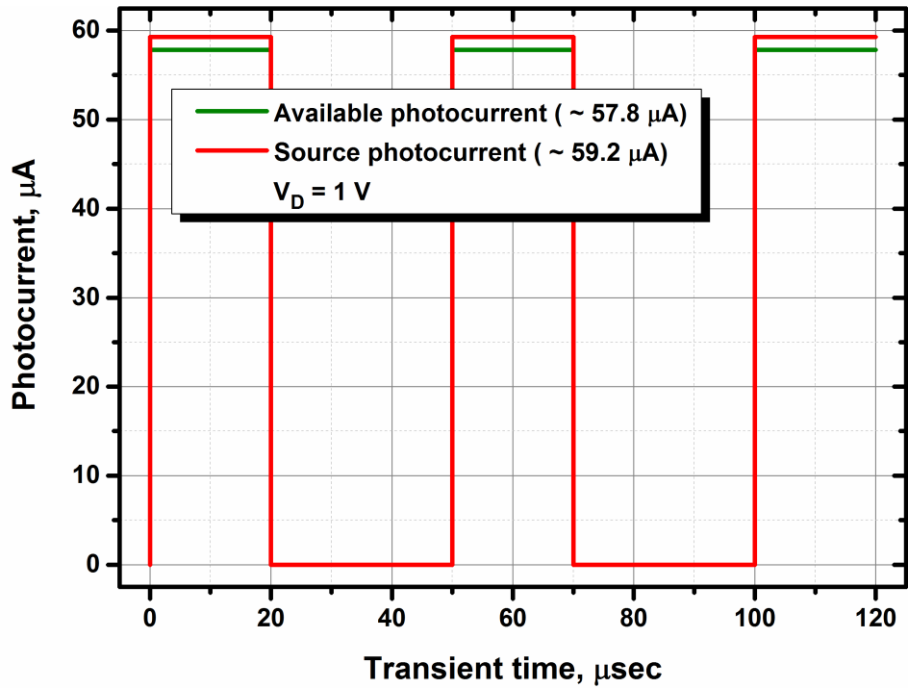
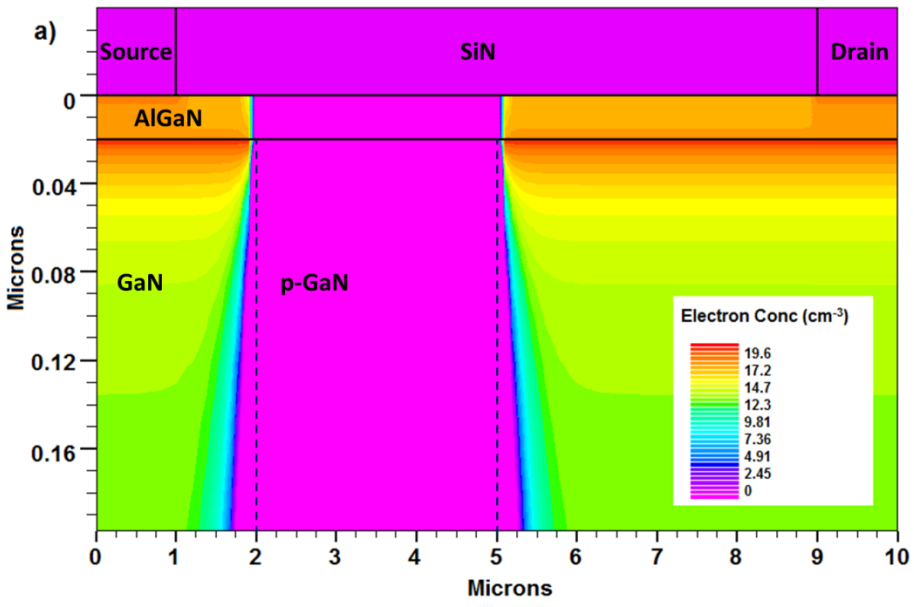


Figure 6.9: Photogenerated current in optically-controlled AlGaN/GaN-based PSD.

Figs. 6.10 (a)-(b) demonstrate electron concentration during off and on periods of the device operation respectively. It can be seen that the 2DEG is completely depleted above the p-doped GaN region (Fig. 6.10, a), and when the light beam is incident on the surface of the device electron-hole pairs are generated and the device goes to the on-state (Fig. 6.10, b).



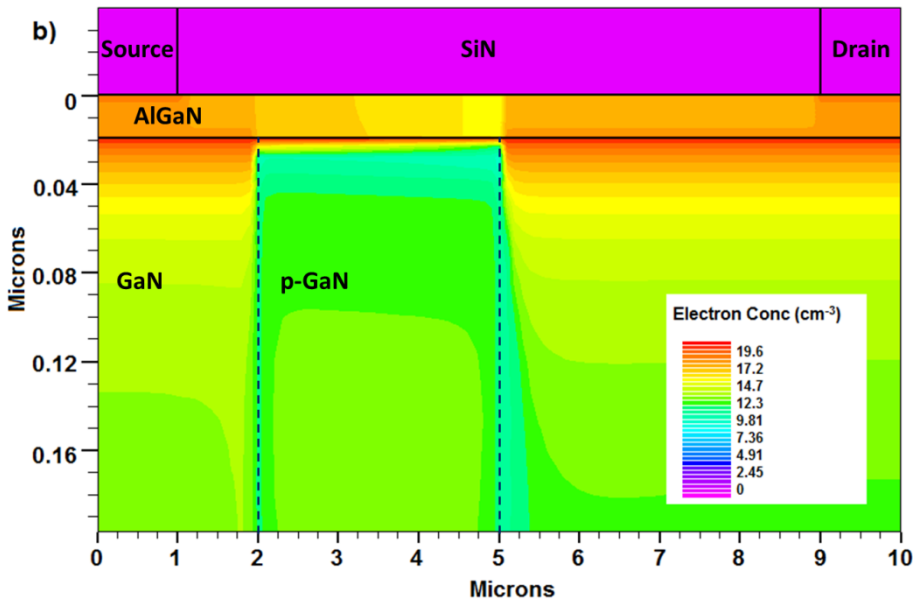


Figure 6.10: Electron concentration during: a) off-state condition; b) on-state condition (application of optical beam).

The simulation reveals that the optically-controlled AlGaN/GaN-based PSD has good switching characteristics with rise and fall times of ~ 0.4 and ~ 0.3 μsec respectively (Fig. 6.11). The device has low fall and rise times because of short carrier lifetime and good optical absorption coefficient of GaN respectively [75].

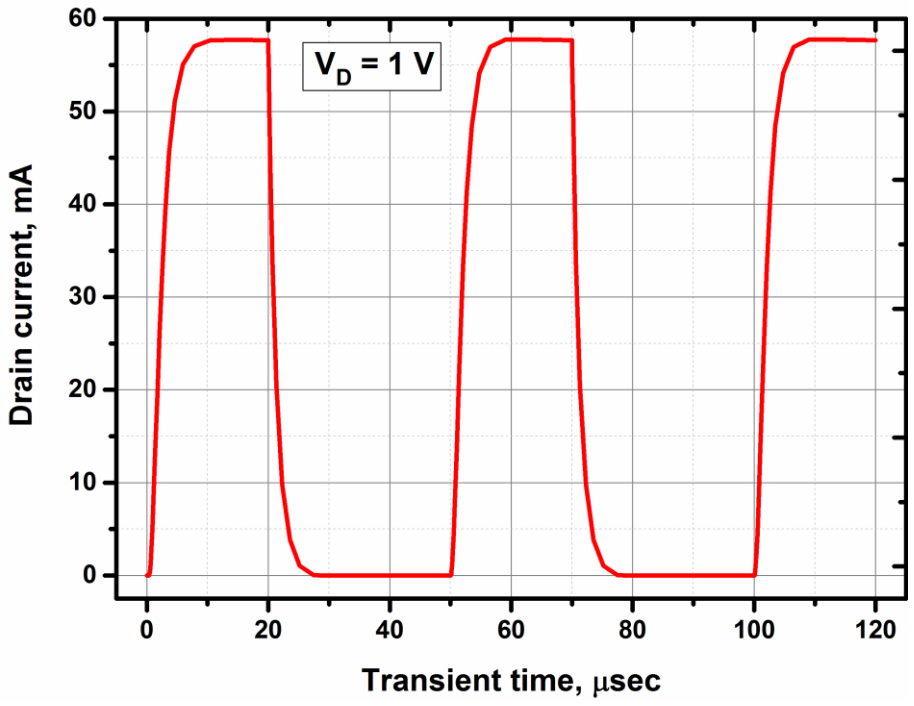


Figure 6.11: Drain current variation with time of optically-controlled AlGaN/GaN-based PSD.

Fig. 6.12 shows drain current – optical intensity characteristic of the device. The threshold optical power of the device is found to be ~ 500 mW/cm^2. Fig. 6.13 demonstrates drain current – drain voltage characteristics with respect to optical intensity.

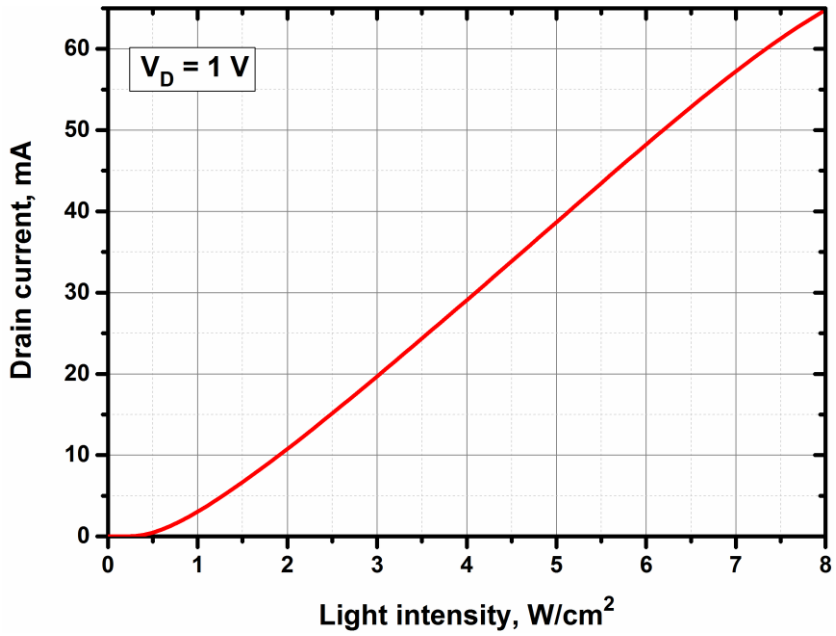


Figure 6.12: Drain current – light intensity characteristic (V_D = 1 V) of the device.

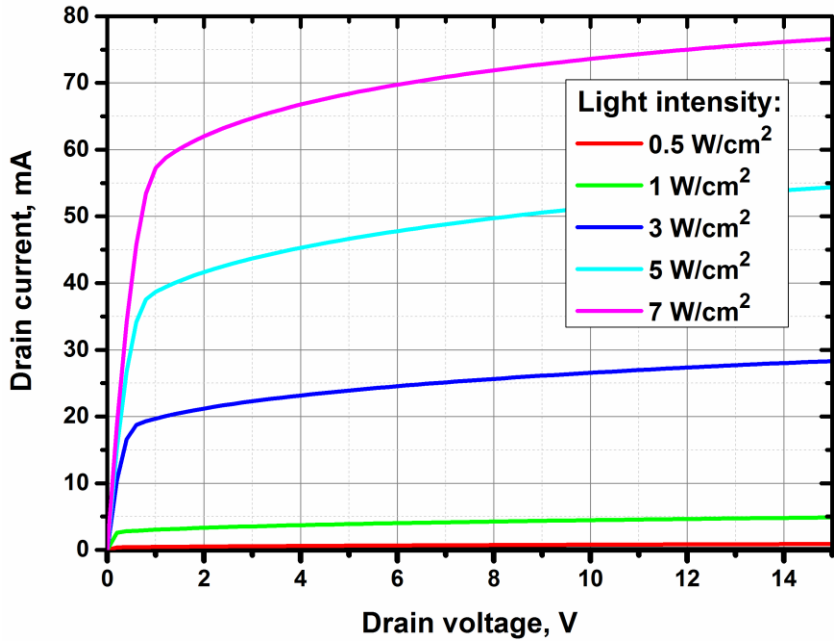


Figure 6.13: I_D - V_D characteristic of the optically-controlled AlGaN/GaN-based PSD.

Fig. 6.14 shows how the gain of the optically-controlled AlGaN/GaN-based PSD varies with intensity of the applied light. The device exhibits maximum current gain of ~ 970 at the light intensity of ~ 7 W/cm^2.

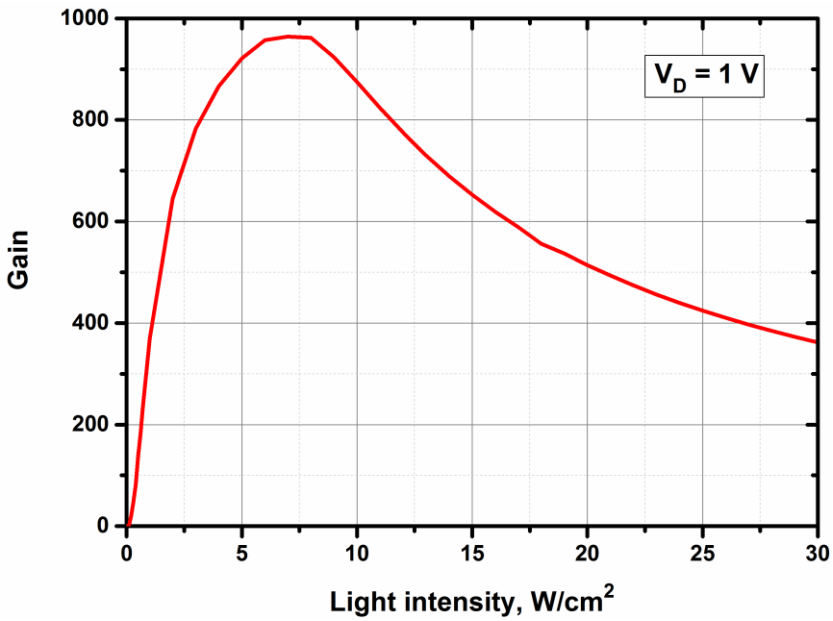
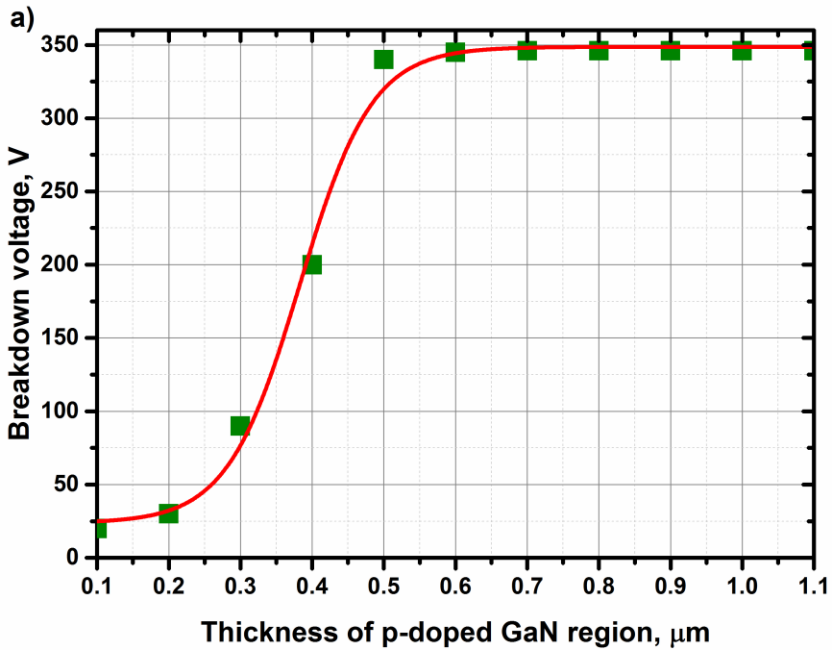


Figure 6.14: Current gain variation with intensity of the applied light beam.

The main element of the design of optically-controlled AlGaN/GaN PSD is the p-doped GaN region, the geometry (i.e. length, thickness) of which is critical for device performance. Figs. 6.15 (a)-(b) show how the breakdown voltage and gain of the device varies with thickness of p-doped GaN region ($t_{P\text{-}GaN}$). The breakdown voltage of the device initially increases and then saturates at $t_{P\text{-}GaN}$ ~ 500 nm, while the gain dramatically decreases with $t_{P\text{-}GaN}$. It can be attributed to the higher resistance of the channel between AlGaN barrier layer and p-doped GaN region with increased $t_{P\text{-}GaN}$ [96].



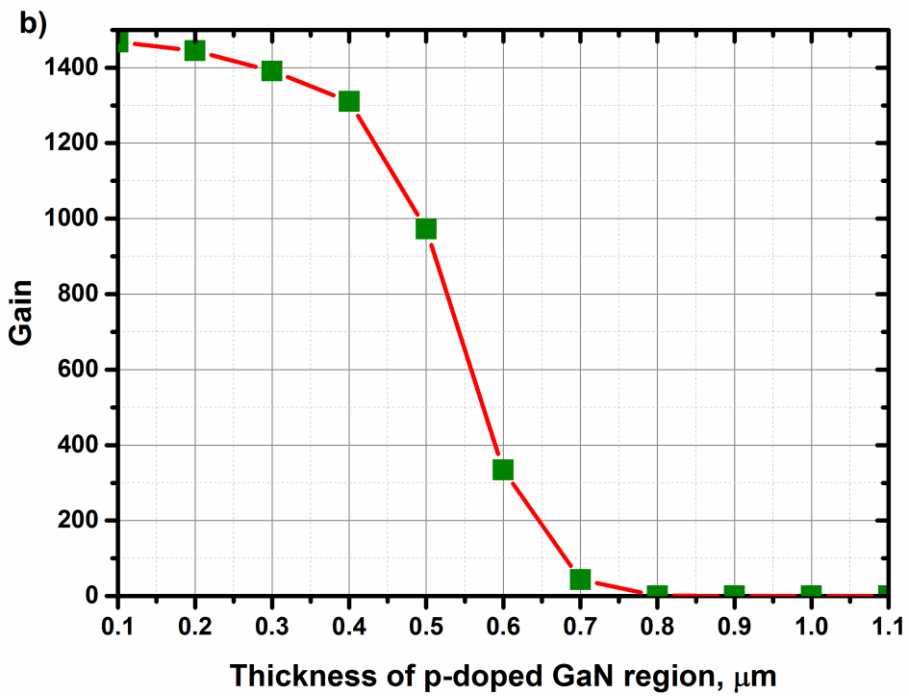
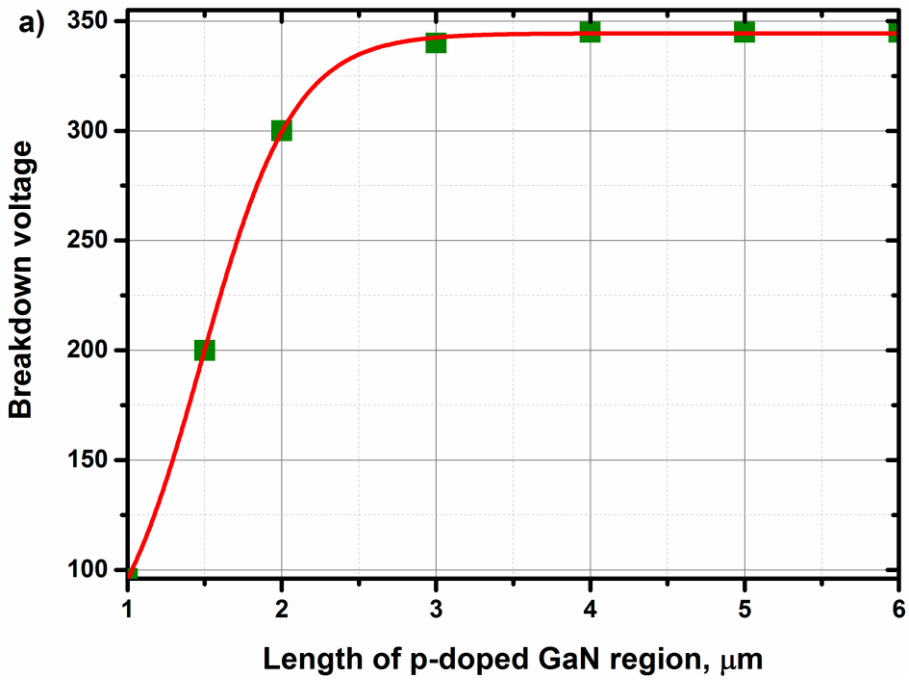


Figure 6.15: (a) Variation of breakdown voltage with thickness of p-doped GaN region; (b) Variation of gain with thickness of p-doped GaN region.

Figs. 6.16 (a)-(b) show how the breakdown voltage and gain of the device varies with length of p-doped GaN region ($L_{P\text{-}GaN}$). The breakdown voltage of the device initially increases and then saturates at $L_{P\text{-}GaN}$ ~ 3 μm, while the gain gradually decreases with $L_{P\text{-}GaN}$. The reduction in gain can be attributed to larger photocurrent due to increase in area which has to be illuminated [96].



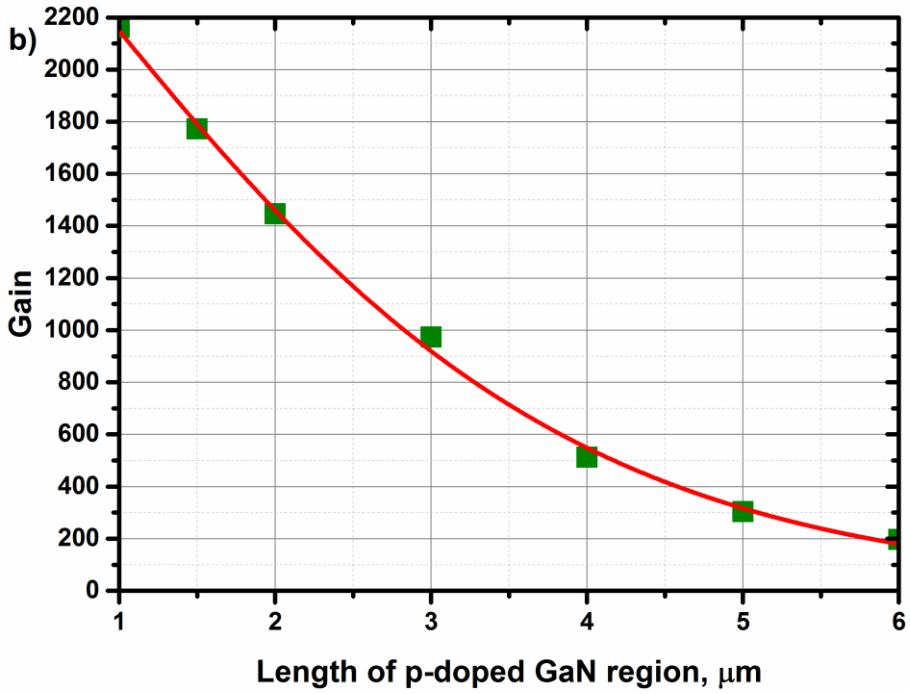


Figure 6.16: (a) Variation of breakdown voltage with length of p-doped GaN region; (b) Variation of gain with length of p-doped GaN region.

6.5 Conclusion

The purpose of this chapter was to present a new idea of the optically-controlled AlGaN/GaN-based power semiconductor device through the simulation study. The typical structure comprises a 20 nm of undoped $Al_{0.23}Ga_{0.77}N$ barrier layer, a 1.1 μm undoped-GaN buffer layer and a p-doped region (to locally deplete the electron channel and ensure a normally-off operation). The simulation study shows that the gain and the breakdown voltage of the device are highly dependent on the depth of the p-doped region. At a particular depth of the p-doped region of 500 nm the gain of the device is 970 (at light intensity of 7 W/cm^2) and the breakdown voltage is ~ 350 V. The rise and fall times of the device is found to be 0.4 μsec and 0.3 μsec respectively. Based on simulation results the device has good switching characteristics and high gain, but the breakdown voltage is not very high. However, the breakdown voltage of the device could be enhanced by implementing Polarization Super Junction concept as shown in [96, 97].

The main challenge in the fabrication of an optically-controlled AlGaN/GaN-based power semiconductor device is the formation of p-GaN region. Current limits

of hole concentration on Mg doping in c-plane GaN is about 1×10^{18} cm^{-3} due to (i) the low solubility for Mg, (ii) the formation of compensating deep defects due to the heavy Mg doping, and (iii) the large acceptor activation energies (~125-215 meV for Mg in GaN). However, the work in order to improve the hole concentration is actively going on and recently hole concentration on Mg-doped p-type GaN of 1.5×10^{18} cm^{-3} has been achieved [125].

In general, the results obtained from the simulation clearly indicate that the optically-controlled AlGaN/GaN-based PSD can be a good candidate for advanced power electronics if the p-type GaN with sufficient hole concentration would be achieved.

Chapter 7

Conclusion and Future work

7.1 Conclusion

The aim of this thesis is to provide new approaches for AlGaN/GaN-based optical and power devices. One of the major demands of the continual development of power electronics is power density, therefore the major focus of this work was on the GaN-on-Diamond technology. All the work which has been done up-to-date on GaN-on-Diamond substrates has been focusing on RF applications. In this work an effort to realise the first high-voltage GaN-on-Diamond power device was undertaken.

The realisation of high-voltage GaN-on-Diamond HEMTs was split into three parts which are: device simulation, device design, device fabrication and electrical characterisation.

The device simulation has provided an insight on the operating principle, electrical characteristics, and off-state electric field profile along the channel on the verge of breakdown of a typical AlGaN/GaN HEMT by means of physics-based simulation study. The electrical simulation results indicate that the device has threshold voltage of ~ -3 V, specific on-state resistance of ~ 9.5 $m\Omega.cm^2$. The breakdown voltage simulation reveals that the off-state breakdown voltage of the device can be increased with inclusion of source field plate. It has been demonstrated that the breakdown voltage initially increases with FP length and then saturates at L_{FP} = ~ 4 μm (V_{BR} = ~1100 V). In order to overcome this limitation a novel non-uniform field plate structure was proposed. The breakdown voltage of the device with non-uniform FP (L_{FP} = 11 μm) is found to be ~ 1800 V compared to V_{BR} = ~ 1200 V for a device with uniform FP of the same length.

The design and fabrication method of GaN-on-Diamond HEMTs was also provided in this thesis. The device design was based on the data obtained from the simulation. The fabricated devices include conventional GaN-on-Diamond HEMTs in circular and linear form with and without field plates as well as bidirectional transistors.

The detailed electrical characterisation results of AlGaN/GaN HEMTs on CVD Diamond substrate are also given. I-V characterisation results showed that the linear and circular devices have the same threshold voltage of around ~ -3 V. The specific on-state resistance of circular devices (R_{ON}.A= ~ 21 – 23 mΩ.cm^2) is more than two times higher that of circular devices (R_{ON}.A= ~ 8 – 10 mΩ.cm^2) which could be associated with the fabrication process. However, the off-state leakage current of the circular devices is at least two orders of magnitude smaller than the leakage of the linear devices due to their self-enclosed structure. Furthermore, for a linear layout device local crowding of the electric field might happen at the area where gate finger crosses mesa etch region, while for a circular device the electric field distributes uniformly along the gate contact. Therefore, the circular device design devices (with improved fabrication process) are better for high voltage applications.

Fabricated circular AlGaN/GaN HEMTs with source field plate length of 3 μm and gate-to-drain separation of 17 μm have demonstrated an off-state breakdown voltage of ~ 1100 V. The systematic measurements of output I-V, transfer I-V, off-state breakdown voltage, capacitance – voltage characteristics and temperature characterisation results provide insights on the device performance and temperature dependence of the heterostructure characteristics. The GaN-on-Diamond epi-wafers used here were manufactured in late 2013. Devices reported here represented the first-time that a power switching device has been made with GaN-on-Diamond albeit with epitaxy designed for RF applications. The performance shown here is expected to improve with epitaxy that has been better tailored for power electronic applications.

Moreover, an innovative approach for an optically-controlled AlGaN/GaN-based power semiconductor device was introduced through simulation study. The typical structure comprises a 20 nm of undoped $Al_{0.23}Ga_{0.77}N$ barrier layer, a 1.1 μm undoped-GaN buffer layer and a p-doped region (to locally deplete the electron channel and ensure a normally-off operation). The simulation study shows that the gain and the breakdown voltage of the device are highly dependent on the depth of the p-doped region. At a particular depth of the p-doped region of 500 nm the gain of the device is 970 (at light intensity of 7 W/cm^2) and the breakdown voltage is ~ 350 V. The rise and fall times of the device is found to be 0.4 μsec and 0.3 μsec

respectively. Based on simulation results the device has good switching characteristics and high gain, but the breakdown voltage is not very high. However, the breakdown voltage of the device could be enhanced by implementing Polarization Super Junction concept as shown in [96, 97].

The main challenge in the fabrication of an optically-controlled AlGaN/GaN-based power semiconductor device is the formation of p-GaN region. Current limits of hole concentration on Mg doping in c-plane GaN is about 1×10^{18} cm^{-3} due to (i) the low solubility for Mg, (ii) the formation of compensating deep defects due to the heavy Mg doping, and (iii) the large acceptor activation energies (~125-215 meV for Mg in GaN). However, the work in order to improve the hole concentration is actively going on and recently hole concentration on Mg-doped p-type GaN of 1.5×10^{18} cm^{-3} has been achieved [125].

In general, the results obtained from the simulation clearly indicate that the optically-controlled AlGaN/GaN-based PSD can be a good candidate for advanced power electronics if the p-type GaN with sufficient hole concentration would be achieved.

7.2 Future work

The work carried out in this thesis can provide the foundation for further investigations. The key areas of future work could be summarised as follows:

a) Investigation of increased buffer leakage current.

Although, it is clear that the buffer leakage current of the fabricated devices in this work was increased after the deposition of thick SiO_2 layer, it is necessary to investigate this issue and find the ways to prevent it. Also the increase in buffer leakage can be associated with the GaN-on-diamond crystal quality. Therefore it is very important to conduct extensive crystal quality tests.

b) Experimental demonstration of HEMTs with non-uniform field plate.

The simulation results have shown that the devices with non-uniform field plate structure can significantly outperform the devices with conventional field plate by increasing breakdown voltage. However, it is essential to prove this concept through experimental tests. As it was shown in Sections 5.2.4 – 5.2.5 the device with

non-uniform field plate were fabricated, but due to high buffer leakage it was not possible to measure the breakdown voltage of these devices. The GaN-on-Diamond epi-wafers used here were manufactured in late 2013 with epitaxy designed for RF applications. Therefore it is important to fabricate devices with epitaxy that has been better tailored for power electronic applications.

c) Thermal characterisation and reliability test

It is very important to investigate the thermal behaviour of the fabricated devices, and measure such parameters as thermal resistance and variation of the channel temperature with respect to power density. Although, our preliminary tests showed that the devices do not suffer from current collapse, the more profound reliability tests are required. The results presented in this work are based on static electrical characterisation of small area device test structures. In order to effectively evaluate dynamic characteristics as well as reliability, it is necessary to scale-up device test structures to large area devices. Also it is important to show dynamic characterisation and detailed reliability comparison with the state-of-the-art GaN-on-Si, GaN-on-SiC devices.

d) Experimental demonstration of optically-controlled AlGaN/GaN-based power transistors.

The simulation study of the proposed new concept of optically-controlled AlGaN/GaN-based PSD has shown that these devices could be very promising for power electronic applications. Therefore, it is essential to continue investigation in this direction via device fabrication and experimental characterisation. The main challenge in the fabrication of an optically-controlled AlGaN/GaN-based power semiconductor device is the formation of p-GaN region. Current limits of hole concentration on Mg doping in c-plane GaN is about 1×10^{18} cm^{-3}. However, the work in order to improve the hole concentration is actively going on and recently hole concentration on Mg-doped p-type GaN of 1.5×10^{18} cm^{-3} has been shown. In order to prove the concept of the optically-controlled AlGaN/GaN-based PSD the device with not optimum parameters (p-GaN region with lower hole concentration) can be fabricated and experimentally characterised.

Appendix – 1: List of Publications

Journal Publications:

- **Baltynov, T.**, Unni, V., and EM Sankara Narayanan. "The World's First High Voltage GaN-on-Diamond Power Semiconductor Devices." *Solid-state electronics*, 2016 (accepted for publication).

Conference Publications:

- **Baltynov, T.**, and EM Sankara Narayanan. "Simulation Study of AlGaN/GaN-based Optically-controlled Power Transistor." in *Proc. ISPS*, Prague, Czech Republic, 2014.
- **Baltynov, T.**, Unni, V., and EM Sankara Narayanan. "Fabrication and Characterization of bidirectional GaN-on-Diamond HEMTs." in *Proc. UKNC*, Sheffield, UK, 2015.
- **Baltynov, T.**, Unni, V., and EM Sankara Narayanan. "The World's First High Voltage GaN-on-Diamond Power Devices." in *Proc. ESSDERC*, Graz, Austria, 2015.

Patent:

- **Baltynov, T.,** and EM Sankara Narayanan. "Optically controlled devices." WIPO Patent Application WO/2016/027100, Feb 25, 2016.

Appendix – 2: List of Figures

Appendix – 3: List of Tables

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