The University Of Sheffield.

Active Control of Voltage Ripples in Power Electronic Converters

By:

Wen-Long Ming

A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

The University of Sheffield

Faculty of Engineering

Department of Automatic Control and Systems Engineering

June 2015

Abstract

Two major challenges, i.e., bulky electrolytic capacitors and isolation transformers, remain as critical obstacles for further improvement on reliability, power density and efficiency of power electronic converters, which are mainly used to reduce low-frequency voltage ripples and high-frequency common-mode voltage ripples, respectively. In order to overcome the two challenges, the most straightforward way is to simply combine existing solutions developed for each of them. However, this would considerably increase system complexity and cost, which should be avoided if possible. In this thesis, these two challenges are innovatively addressed in a holistic way by using active control techniques.

This thesis first focuses on the reduction of low-frequency voltage ripples in conventional half-bridge converters, after adding an actively-controlled neutral leg. As a direct application of this strategy, a single-phase to three-phase conversion is then proposed. After that, a ρ-converter with only four switches is proposed to significantly reduce both low-frequency ripples and high-frequency common-mode ripples in a holistic way. It is found that the total capacitance can be reduced by more than 70 times compared to that in conventional full-bridge converters. As a result, there is no longer a need to use bulky electrolytic capacitors and isolation transformers. Then, the ρ-converter equipped with the synchronverter technology is operated as an inverter for PV applications. Another converter is also proposed for the same purpose but with reduced voltage stress.

In order to further reduce the total capacitance and to reduce the neutral inductor in the ρ-converter, a new type of converter, called the θ-converter, is proposed. Finally, two actively-controlled ripple eliminators are proposed to reduce low-frequency ripples in general DC systems while the aforementioned research is focused on some specific topologies.

Extensive experimental results are presented to validate most of the developed systems while the rest are validated with simulation results.

Acknowledgements

I would like to first express my sincere thanks to my supervisor Prof. Qing-Chang Zhong, who gave me this precious opportunity to do research. His insight into both control and power electronics helped me stand in the forefront of both areas when I started my PhD. He is always available and patient to talk with me on my research and I have really got a lot of insightful guidance, ideas and suggestions from him. More importantly, he is my spiritual mentor, who has taught me how to overcome difficulties and succeed in life. His generous and unreserved sharing has made me become more creative, active and positive. Without him, I cannot finish my PhD so smoothly.

I wish to thank my colleagues in Control and Power Systems (CAPS) Lab. Their friendship, help and encouragement make my life so enjoyable. Here, I would like to mention some of them and they are Dr. Zhen-Yu Ma, Dr. Long Nguyen, Dr. Tomas Hornik, Miss Yu Zeng, Dr. Xin Zhang, Dr. Yao Zhang, Dr. Zhao-Hui Cen, Prof. Xiao-Lin Wang, Dr. George Konstantopoulos and Mr. Shlomo Gadelovits.

Many thanks also go to Dr. Hua-Liang Wei for his generous help during my stay in Sheffield. I would also like to thank all the support staff in the department who gave me lots of support on my research and daily life. Here, I must mention some of them who helped me a lot. They are Alex Price, Matthew Ham, Ian Hammond, Craig Bacon, Jack Powell, Paul Staniforth, Darren Fox, Yuka Pickstock, Rachel Fearon and Liz Woodward.

Finally, I would like to offer my deep thanks to my dear parents Chun-Ling Li and Jun Ming, and my beloved wife Lin Duo. Your endless love, support and encouragement gave me the powerful impetus to move forward.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

1.1.1 Distributed Power Generation Systems

A power grid is a network to generate, transmit and distribute electrical energy, which is finally consumed by local users. Until now, most of the electrical energy still comes from synchronous generators, which are mostly driven by coal or natural gas. Due to the unidirectional power flow operation of the generators, the majority of electrical energy is delivered in an unidirectional way from large power plants to final users. As a result, the energy generated by power plants should be always equal to energy consumed by users and transmission lines, which may lead to stability problem if not satisfied. Most of power plants are built far from cities because of considerations on cooling, noises and power pollutions. In this case, the current power grid is in a centralised structure and hence, supervisory control and monitoring are required to maintain the balance between the generated and consumed energy. The power grid is regarded as the most complex machine in the human history.

Recently, the penetration of renewable energy systems pushes the development of advanced technologies regarding on the integration of renewable systems with the power grid (Zhong and Hornik, 2013b). With distributed renewable energy systems, the power grid is becoming decentralised. In order to address energy and sustainability challenges we are facing nowadays, it is expected that more and more distributed power generation systems (DPGS) based on renewable energy sources will be connected to the public grid, which

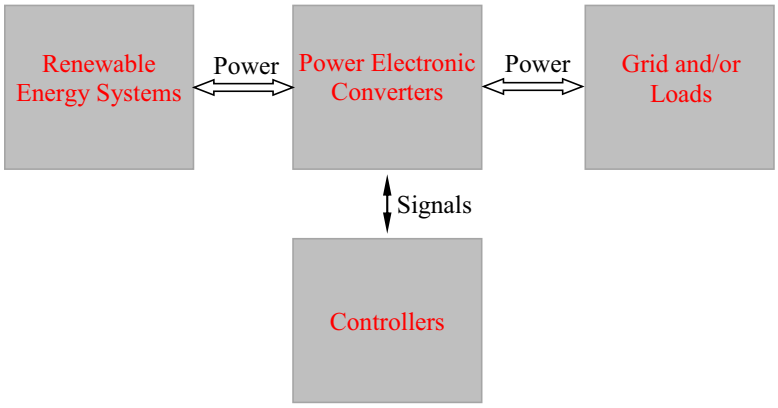


Figure 1.1: Power electronic converters in renewable energy systems.

help to reform the current power grid from a centralised to a decentralised structure. It has been well recognised that decentralised power grid is more reliable, stable and resilient (Boroyevich et al., 2013).

1.1.2 Power Electronic Converters

Most DPGS are finally connected the power grid to take part in the regulation of grid frequency and voltage when the scale of such systems exceeds a certain level. In order to facilitate this connection, power electronic converters (PEC) are often required (see Figure 1.1), which are used to convert electrical energy from one form to another, e.g., from single phase to three phase or from AC to DC. Similar to any other technical systems, PEC are constructed by a number of components that are connected together to achieve some specific functions. Here, the components may include active switches such as IGBTs and MOSFETs and passive components such as inductors and capacitors (Zhong and Hornik, 2013b). There are numerous topologies of PEC for different applications. For example, PEC can be classified into single-phase and three-phase ones, which depend on the number of phases of PEC' inputs and outputs; two-level PEC are preferred for low and medium power applications because of their simple structures but multilevel PEC are often chosen for high power applications.

Apart from topologies of PEC, control strategies are also very important to achieve power conversion. In (Zhong and Hornik, 2013b), a lot of advanced control strategies have been developed to improve the performance of PEC in terms of power quality and

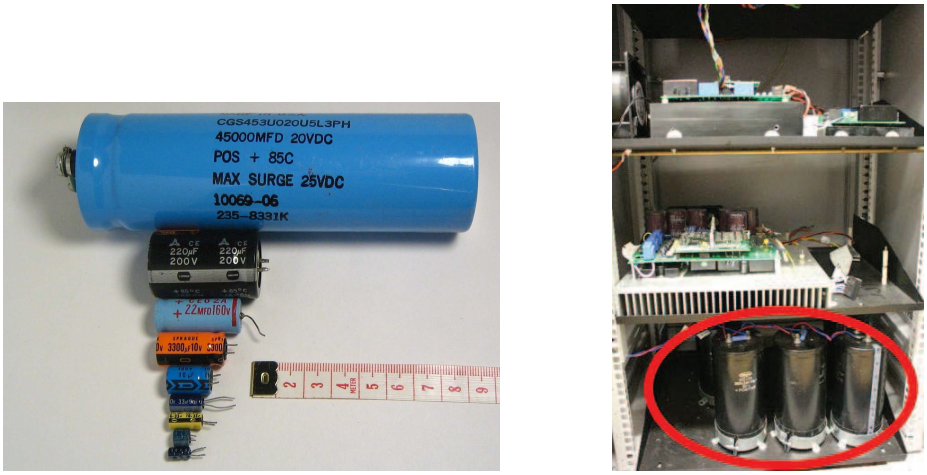
power flow management. Single chip microcontrollers, digital signal processors and field-programmable gate array can be good candidates to construct units to execute control strategies.

1.1.3 Voltage Ripples in PEC

Regardless of specific topologies, there are DC and/or AC sides in PEC, which can be inputs and/or outputs. For example, the input and output sides of a DC/AC rectifier are DC and AC sides, respectively. For bidirectional PEC, both DC and AC sides can be inputs or outputs depending on power flow between the two sides.

At the AC side, there might be second-order, third-order, $\cdots$, switching-frequency and other higher-orders voltage ripples because of on and off operation of active switches. Voltage ripples at the AC side are normally called harmonics. From the view point of loads, it is expected to have high quality AC voltage without noticeable harmonics. For this purpose, a set of small inductors and capacitors are normally used to construct to a first-order LC filter. Of course, other high-orders LC filters can be used but this would inevitably increase system complexity. Another way to limit harmonics is to use advanced control strategies. H^{∞} repetitive voltage and current controllers can be good candidates. Many of such controllers have been presented in (Zhong and Hornik, 2013b).

At the DC side, voltage ripple is often not a major concern because an ideal DC voltage is constant and there is not an issue of phase differences between voltages and currents. However, in applications with PEC, DC voltages are not ideal but have a significant amount of ripple components (Cao et al., 2015). Such ripples often contain fundamental, second-order components and switching-frequency components. For systems powered by batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the life-time of batteries and fuel cells (Wai and Lin, 2010; 2011; Kwon et al., 2009; Zhu et al., 2010). During the charging mode of a battery, an external voltage with large ripples could lead to an immoderate chemical reaction. During the discharging mode, ripple currents drawn from a fuel cell can deteriorate PEC' efficiency significantly and even make PEC unstable (Liu and Lai, 2007). Generally, current ripples should be maintained less than 10% of the rated current for batteries (Wen et al., 2012). DC capacitors are normally used for this purpose. Small capacitors are often enough to limit switching-frequency ripples.



(a) (b)

Figure 1.2: Electrolytic capacitors: (a) of many sizes; (b) in a power inverter system. (Source of (a): http://commons.wikimedia.org/wiki/File:Electrolytic_capacitors.jpg.)

However, bulky capacitors are often needed to smooth low-frequency (fundamental and second-order) ripples. Among different kinds of DC capacitors, only electrolytic capacitors are cost-effective to be used.

For most PEC, AC and DC sides are not directly connected together in order to make sure the successful operation of PEC. In this case, the voltage difference between the two sides is not zero, which may contain low-frequency and/or high-frequency ripples depending on topologies, modulation and control strategies. Normally, this differential voltage is called common-mode (CM) voltage. Due to parasitic capacitors between AC and DC sides, the loop for the CM voltage is closed. If the high-frequency ripple in the CM voltage is high enough, the resulted CM current could be very large. In order to reduce CM currents, galvanic isolation transformers are normally added between DC and AC sides to cut off the closed loop of CM currents.

1.2 Motivations

Driven by the penetration of renewable energy systems, a lot of advanced technologies regarding the integration of renewable systems with the power grid are developed in the last few years (Zhong and Hornik, 2013b). In order to facilitate the interconnection among different types of renewable energy systems and the power grid, PEC are often needed.

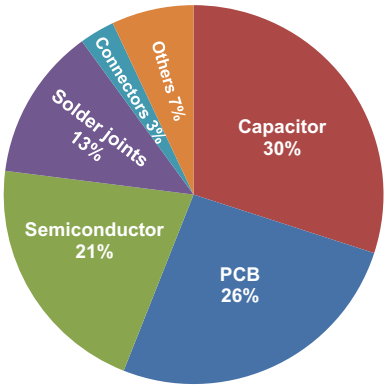


Figure 1.3: Distributions of failure root causes in PEC. (Data sources: (Wolfgang, 2007))

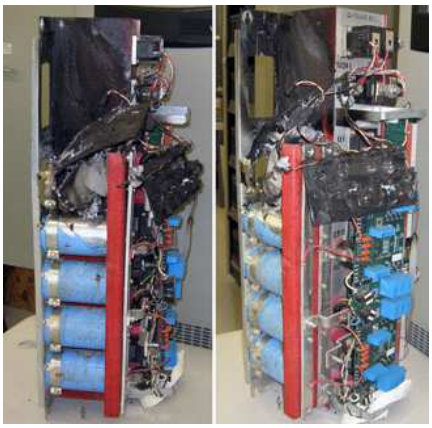


Figure 1.4: A damaged power inverter caused by the degradation of electrolytic capacitors. (Source: http://blog.eecnet.com/eecnetcom/bid/27236/Why-Preventive-Data-Center-Maintenance-is-Important)

Numerous topologies, modulation strategies, and control methods have been proposed to improve power density, efficiency, reliability, and cost of PEC. However, two major challenges remain as critical obstacles for further improvement. The first challenge is the bulky electrolytic capacitors used to reduce low-frequency voltage ripples, which are the most vulnerable components in PEC. The second challenge is the isolation transformer used to reduce high-frequency CM voltage ripples, which reduces system efficiency and causes safety concerns like electric shock.

1.2.1 Challenges of Reducing Low-frequency Voltage Ripples

In order to reduce the ripple current and to smooth the external voltage on batteries and fuel cells, bulky capacitors or ultracapacitors are often connected in parallel with them (Choi

et al., 2006). Large electrolytic capacitors are also often needed to level and smooth the DC-bus voltage of inverters and rectifiers (Wen et al., 2012; Wang et al., 2011; Yao et al., 2012; Zhu et al., shed). For volume-critical and/or weight-critical applications, such as electrical vehicles (Wen et al., 2012) and aircraft power systems (Wang et al., 2011), the volume and weight of electrolytic capacitors could be a serious problem. As shown in Figure 1.2(a), sizes of electrolytic capacitors can be from very small to very large, depending on the their capacitance and voltage ratings. In general, high capacitance and high voltage rating lead to large volume, which should be avoided for the consideration of power density. However, bulky electrolytic capacitors are often required to smooth voltage ripples. As shown in Figure 1.2(b), a power inverter is composed by some control circuits, power switches and bulky electrolytic capacitors. Actually, more than half volume and weight of the inverter are occupied by electrolytic capacitors, which obviously makes the power density of the inverter very low.

What is worse is that electrolytic capacitors, known to have limited lifetime, are one of the most vulnerable components in power electronic systems (Stevens et al., 2002; Krein et al., 2012). As shown in Figure 1.3, almost one third of faults in PEC are caused by degraded electrolytic capacitors (Wolfgang, 2007). Figure 1.4 shows a damaged UPS inverter assembly, the damage was caused by the ageing electrolytic capacitors. This may cause a big disruption in critical loads, which in turn could lead to a huge cost. On the other hand, the presence of large voltage ripples is an essential factor that accelerates the degradation of electrolytic capacitors (Kulkarni et al., 2010; Krein et al., 2012). As a result, in order to enhance the reliability of power electronic systems, it is highly desirable to minimise the usage of electrolytic capacitors and it is very attractive if highly-reliable small capacitors like film capacitors could be used to achieve low-level voltage ripples. However, in applications involving bulky electrolytic capacitors, there often exists a trade off between minimising the required capacitors and reducing voltage ripples. Another design degree of freedom, normally through active control, needs to be introduced to break this deadlock. Along with this idea, a lot of methods have been proposed, which are often based on another actively-controlled energy buffer circuit. In principle, most of ripple energy are diverted from DC-bus capacitors to the active circuit so that DC-bus capacitance is only sized for filtering switching frequency ripples. In this case, it is possible to simultaneously

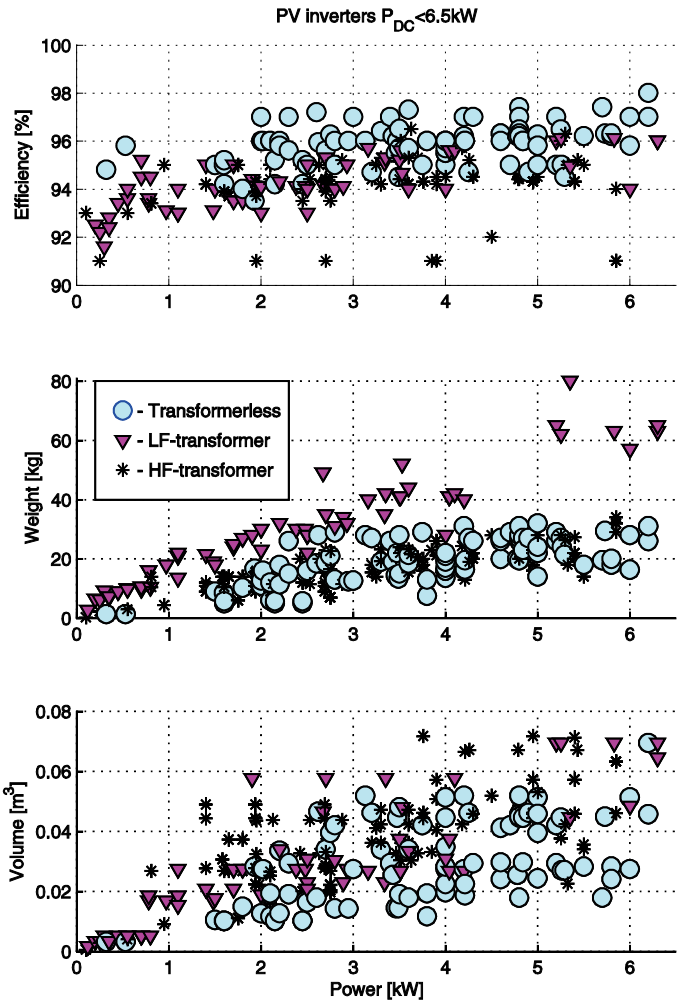


Figure 1.5: A comparison of transfomer-based and transformerless PV inverters in terms of efficiency, weight and volume. (Source: (Kerekes et al., 2011)).

achieve the reduction of voltage ripples and DC-bus capacitance.

1.2.2 Challenges of Reducing High-frequency CM Voltage Ripples

In order to eliminate/reduce CM voltage ripples, galvanic isolation transformers are normally added between the renewable energy systems and the grid. But the adoption of transformers reduces power density and efficiency and increases manufacturing costs.

As demonstrated in (Kerekes et al., 2011), Figure 1.5 shows a comparison of transformer-based and transformerless PV inverters in terms of efficiency, weight and volume. The data used for the comparison are extracted from the database of more than 400 commercial PV inverters (Kerekes et al., 2011). The low-frequency(LF)-transformer-based, high-

frequency(HF)-transformer-based are denoted as 'triangles', 'stars' and 'dots', respectively. It can be found that PV inverters without using isolation transformers always enjoy higher efficiency, lower volume and lower weight, all of which are highly preferred in practice. For example, isolation transformers account for about 3% of system power losses, over 60% of weight, and over 50% of volume in a 6 kW PV inverter. Along with the boost development of renewable energy systems, numerous transformerless PV inverters are developed to reduce the CM voltage without using isolation transformers. Either advanced modulation strategies or topological design techniques are employed for the design of such inverters (Kjaer et al., 2005; Li and Wolfs, 2008; Meneses et al., 2013).

In order to address the aforementioned two issues caused by isolating transformers and bulky capacitors, a possible way is to simply combine the approaches developed to address each issue. For example, both transformers and bulky electrolytic capacitors can be removed if the ripple compensator proposed in (Wang et al., 2011) is applied to the transformerless converter reported in (Gu et al., 2013). However, this kind of combination would make the system complicated and also have high costs due to the increased number of switches and passive components. A better way is to address these two problems together. For example, the midpoints of a split-phase single-phase system at both the DC and AC sides are constructed and connected together in (Breazeale and Ayyanar, 2015) to eliminate the isolating transformer and bulky electrolytic capacitors with six active switches.

In this thesis, the two fundamental challenges are innovatively addressed in a holistic way by completely removing isolation transformers and minimizing the required capacitance via the integration of advanced power electronic and active control techniques. The research in this thesis can be directly applied to different renewable energy systems and it is worth mentioning that most of conclusions resulted from this research can be easily extended to the other systems.

1.2.3 Aims and Objectives

In order to overcome these two challenges, a possible way is to simply combine existing approaches for each of them in the literature. However, this would increase the complexity of the whole system and also lead to high cost due to the increased number of switches and passive components, which should be, of course, avoided. In this thesis, for the first time,

the two fundamental challenges are innovatively addressed in a holistic way by using active control and topological design techniques. The proposed systems in the following chapters are designed to have minimum number of active switches and passive components so that system power density, reliability and efficiency can be improved to the greatest extent.

1.3 Outline of the Thesis

In addition to the Introduction, another 11 chapters are included in this thesis to facilitate the presentation of the proposed holistic way to actively control fundamental, second-order and high-frequency voltage ripples in PEC.

The research is first focused on analysing drawbacks of conventional half-bridge converters in Chapter 2. It is seen that there are large fundamental voltage ripples in DC outputs of the converters. Then, the reduction of such ripples is achieved through adding an actively-controlled neutral leg. Thanks to the neutral leg, the two DC outputs become independent from each other, which makes it possible for the two outputs to interface loads with different voltage requirements.

The work in Chapter 2 lays the foundation for Chapter 3 in which the strategy developed in Chapter 2 is applied to develop a conversion system, which can output independent three phase voltage outputs from a single-phase voltage supply so that balanced or unbalanced, linear or non-linear three-phase loads can be operated. Again, fundamental voltage ripples are removed from DC outputs.

In addition to fundamental-frequency voltage ripples, another low-frequency voltage ripple, i.e., second-order voltage ripple, is considered in Chapter 4. ρ-converters and the corresponding active control strategies are proposed to reduce both of the ripples and total capacitance required at the same time. It has been found in theory and verified in experiments that the required usage of capacitors can be reduced by over 70 times compared to that in conventional full-bridge converter while maintaining the same level of output voltage ripples.

In Chapter 5, the elimination of high-frequency CM voltage ripples without the need of an isolating transformer is investigated via providing a common AC and DC ground for grid-tied converters, following ρ-converters developed in Chapter 4 that reduces low-

frequency voltage ripples. It is seen that high-frequency CM voltage ripples are completely removed and the key to achieve this lies in the active control strategy that decouples the control of the two legs of the ρ-converters.

Most of the research on the ρ-converter in Chapters 4 and 5 is focused on the rectification mode and the corresponding inversion mode is then investigated in Chapter 6. In addition, the synchronverter technology designed for three-phase inverters is extended to a single-phase case to design the controllers of the ρ-converter. As a result, the ρ-converter becomes more grid-friendly because they can now take part in regulations of grid frequency and voltage.

In Chapter 7, an auxiliary capacitor is added to a conventional full-bridge rectifier to provide a path for low-frequency ripple currents and high-frequency CM currents. Compared to the ρ-converter, the proposed rectifier has much lower voltage stress on active switches and higher DC output voltage. All of these merits make the proposed rectifier more suitable for high voltage applications with comparison to the ρ-converter.

In Chapter 8, the aforementioned research on the ρ-converter is moved forward to develop a θ-converter, which further reduces total capacitance required and low-frequency voltage ripples. The location of one capacitor in the ρ-converter is re-located. Compared to conventional converters, the total capacitance required in the θ-converter is reduced by about 172 times, which is more than 2.5 times compared to that of the ρ-converter.

The performance of the θ-converter is further improved, in Chapter 9, through reducing a passive component in the θ-converter, i.e. the neutral inductor. It is analysed and verified by experiments that the current flowing through the neutral inductor can be reduced at least three times and hence, the size of the neutral inductor can be reduced by at least about nine times, which makes the power density of the θ-converter significantly improved.

The previous chapters mainly focus on active control of voltage ripples in specific PEC. On the other hand, the work in Chapters 10 and 11 addresses the control of low-frequency voltage ripples in general DC systems. In Chapter 10, a discontinuous-current-mode (DCM) ripple eliminator, which is a bi-directional buck-boost converter terminated with an auxiliary capacitor, is proposed to reduce low-frequency ripples in DC systems without using bulky capacitors. The concept of ripple eliminators proposed in the Chapter 10 is further developed in Chapter 11 and the ratio of capacitance reduction is quantified

for the first time. Advanced control strategies based on the repetitive control is proposed to one possible implementation of ripple eliminators in continuous-current-mode (CCM). It is found that the proposed CCM ripple eliminator leads to nearly four times improvement of performance than that of the DCM ripple eliminator presented in Chapter 10.

Finally, Chapter 12 concludes the thesis and discusses future work. The presented research in this thesis paves the way to develop PEC in high power density, high reliability and low cost.

1.4 Literature Review

1.4.1 Reduction of Low-frequency Voltage Ripples

In order to reduce low-frequency ripples, the most straightforward approach is to use passive components that can absorb/release low-frequency energies and bulky capacitors are often chosen for this purpose. For such level of capacitors, only electrolytic capacitors are suitable from the view of costs. However, the system performance on power density and reliability would be seriously degraded with such electrolytic capacitors. As a result, it is essential to find out other solutions rather than simply using bulky passive components. During the last few years, a lot of efforts have been paid to develop different active approaches to achieve the reduction of both low-frequency voltage ripples and the required capacitance so that film capacitors can be cost-effective to be used. In general, there are six of them in total.

As shown in Figure 1.6(a), one of the approaches is to inject harmonic currents into the grid current i_g to suppress fluctuations of the input energy by changing control strategies for existing power switches in the system. In (Gu et al., 2009; Wang et al., 2010), it was proposed to inject third harmonic component to the input current so as to reduce DC-bus capacitors in LED drivers. The analysis in these papers is based on the fact that decreased pulsating input power leads to decreased ripple power and capacitor volume on the DC bus, which can be achieved by controlling the input current. In (Lamar et al., 2012), a similar concept was also adopted by distorting the input current to reduce the output capacitor. The essence of injecting harmonic currents or distorting the input current is to obtain a varied duty cycle to control the power switches, which changes the amount of energy delivered to

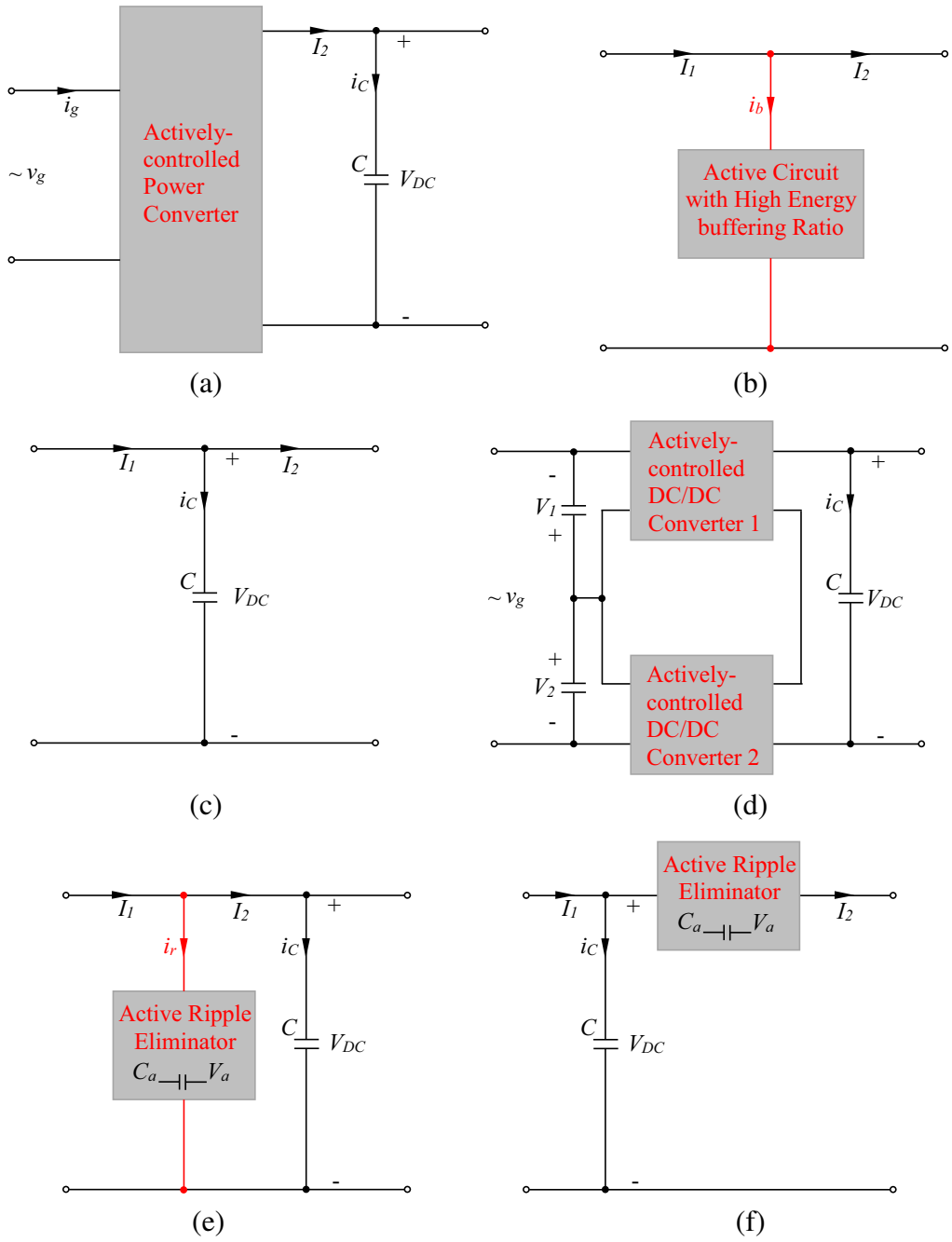


Figure 1.6: Active approaches to reduce low-frequency voltage ripples: (a) through injecting third/fifth harmonics into the grid current i_g; (b) through adding an active circuit with high energy buffering ratio; (c) through synchronising the DC currents I_1 and I_2; (d) through diverting ripples to AC side capacitors C_1 and C_2; (e) through adding a parallel-connected ripple eliminator; (f) through adding a series-connected ripple eliminator.

the load in each fundamental cycle. This approach benefits with no added power components but the disadvantage of this approach is the increased total harmonic distortion (THD) of the input current, which actually should be maintained at a low level.

The second approach is to replace bulky electrolytic capacitors with an active circuit with high energy buffering ratio. Here, the energy buffering ratio is denoted as the ratio of the energy that could be injected and extracted from the DC bus in one cycle respect to the total energy stored in the DC bus. A possible implementation was reported in (Chen et al., 2013), which is constructed based on a switched capacitor circuit. Since only a few film capacitors are needed in the circuit, bulky electrolytic capacitors can be completely removed from the system. The losses of the added circuit can be very low because the switches in the circuit are only operated at line-scale switching frequencies. An enhanced switched capacitor circuit was reported in (Afridi et al., 2014) for the same purpose but with further improved efficiency.

As presented in (Soares de Freitas et al., 2010), the third approach is achieved by synchronising currents before and after DC-bus capacitors, which is very suitable for cases with two converters connected to the DC bus that have specific relationship between their fundamental frequencies. The difference between the two currents, i.e. the current flowing through DC-bus capacitors, can be then reduced so that only small capacitors are required. However, it is obvious this approach is only effective for some specific cases.

The fourth approach is to use buck/boost DC/DC converters to construct two DC voltages across two capacitors that are connected in opposite polarity (Li et al., 2015; Serban, shed; Zhu et al., 2013). The difference of the voltages across the two capacitors is an AC voltage. At the same time, the sum of pulsating energy stored in the two capacitors is equal to system input pulsating energy and hence, no pulsated energy appears on the DC bus. Both DC-bus voltage ripples and required DC-bus capacitance can be significantly reduced.

The fifth approach is to add an active energy storage circuit in parallel with the DC-bus capacitor to bypass the ripple currents originally flowing through the DC-bus capacitor (Wang et al., 2011; Garcia et al., 2003; Zhang et al., 2013b; Krein et al., 2012; Tang et al., 2015; Cao et al., 2015). The strategy proposed in (Cao et al., 2015) is such an example, with a circuit consisting of one capacitor, one inductor and two power switches. It absorbs and releases the ripple energy, respectively, during its two different half cycles. In this case,

most of ripple energy flows through the active circuit rather than DC-bus capacitors. Only very small capacitors are required for filtering switching-frequency ripples on the DC-bus. For the capacitor in the active circuit, it can be with very large voltage ripples because no loads are connected. As a result, it can be very small. In this case, the reduction of DC-bus ripples and total capacitance required can be achieved at the same time.

The sixth approach is based on connecting an active compensator in series with the DC bus line (Wang et al., 2014; Liu et al., 2015). The compensator basically behaves as a voltage source to offset the voltage ripples. Due to the series operation, the voltage stress of the added compensator is reduced. However, the current stress of the compensator is increased because the ripple power for a certain load is fixed. Due to the series connection, lines between the DC sources and loads should be cut off so that the compensator can be connected. However, for some DC systems, this can be a problem because of the widely-distributed sources and/or loads. Note that only the DC voltage after the compensator becomes clean without noticeable low-frequency ripples but the DC voltage before the compensator still suffers from large low-frequency ripples.

1.4.2 Reduction of High-frequency Voltage Ripples

Figure 1.7 illustrates a generic equivalent circuit for analysing CM currents, which consists of a CM voltage source v_{CM}, a filter L and a parasitic capacitor C_p between the DC ground and the AC ground, which is often connected to the earth via the neutral line when an isolating transformer is not used. This closes the loop for the CM current i_{CM} and the CM voltage v_{CM}, which is generated by the switching of power switches and other reasons, appears on the parasitic capacitor C_p. If the switching frequency is high enough, the CM current i_{CM} could be very large even if the parasitic capacitor C_p is relatively small.

In general, the CM current i_{CM} mainly depends on both the behaviour of the CM voltage and the impedance in the path of the CM current. In light of this, there are four main approaches in the literature to reduce CM currents.

The first approach is to add passive components to increase the impedance in the path of the CM current. For example, this can be achieved by increasing the filter L. Filters used for this purpose are called CM filters (Heldwein et al., 2010), which have large inductance to mitigate CM currents. However, due to their large size and heavy weight, the system

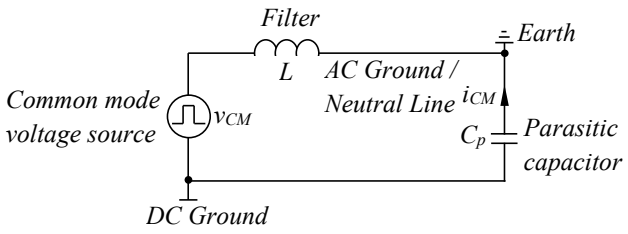


Figure 1.7: Generic equivalent circuit for analysing CM currents.

power density could be reduced. Different from this one, the following approaches are based on active methods.

The second approach is to reduce high-frequency components in the CM voltage v_p across the parasitic capacitor C_p. This can be achieved by reducing high-frequency components in the v_{CM} e.g. changing the modulation strategies (FREDDY TAN et al., 2015; Bae and Kim, 2014) and decoupling AC and DC sides of converters during freewheeling phases (Kerekes et al., 2011; Buticchi et al., 2014; Xiao et al., 2014; Ji et al., 2013). It can also be achieved by putting passive or active components (Barater et al., 2014) in series or in parallel with v_{CM}. Although these methods to reduce v_p can reduce CM currents to some extent, they suffer from reduced voltage utilization ratio (Cavalcanti et al., 2010), reduced ability to process reactive power (Gu et al., 2013) and/or degraded performance caused by parasitic capacitors of switches (Gu et al., 2013).

The third approach is to provide another current path between the AC ground and the DC ground so that most of the CM current flow through this path instead of the parasitic capacitor. For example, this can be achieved by connecting the AC ground to the midpoint of the DC bus, which is normally formed by split capacitors (Xiao and Xie, 2012). This makes the split capacitors in parallel with the parasitic capacitor so that most of the CM current i_{CM} can be bypassed through the split capacitors. Since the split capacitors are normally much larger than the parasitic capacitor C_p, the CM current is reduced. For example, converters based on the half-bridge topology are equipped with split capacitors (Srinivasan and Oruganti, 1998), which have the potential of forming the bypassing current path. For three-phase applications, the three-phase four-wire power converters proposed in (Zhong and Hornik, 2013b; Hornik and Zhong, 2013) also have the bypassing current path so that CM current i_{CM} can be reduced a lot. Another way is to connect the neutral point of the AC side formed by AC capacitors of the LC filters to the split capacitors (Dong et al., 2012a).

In this case, the AC capacitors are in series with the split DC capacitors in the current path, which are in parallel with the parasitic capacitor C_p.

The last approach is to connect the AC ground and the DC ground together so that the CM current i_{CM} is almost completely eliminated. The elimination of CM currents is naturally achieved because the parasitic capacitor is short-circuited without any other efforts, when ignoring the parasitic inductance of the cables. One of such converters is the Karschny inverter (Karschny, 1998). Unfortunately, this inverter suffers from complex structure, increased number of power switches and the need of large capacitors. Another one was proposed in (Gu et al., 2013), where the concept of virtual DC bus is used to enable the direct connection between AC and DC grounds. The virtual DC bus is achieved by adding an extra active switch and an extra DC capacitor into a conventional full-bridge converter. Benefiting from its topological structure, the converter is capable of exchanging both real and reactive power with the power grid. The operation of the two converters are similar to that of conventional full-bridge converters. Moreover, it is also possible to connect the AC and DC grounds together if the midpoints of both AC and DC sides are constructed, as reported in (Breazeale and Ayyanar, 2015).

As reported in (Kerekes et al., 2009), it is possible to have a common AC and DC ground if two series of balanced PV panels are connected to a three-phase inverter with split DC capacitors. The midpoint of the split capacitors is then connected to the grid neutral line. In this case, the CM currents can be almost completely eliminated. However, the upper and lower panels are likely to become unbalanced due to the potential induced degradation (PID) of solar panels (Omron, 2013; Fujita, 2010), even initially designed to be balanced. The unbalanced voltages could lead to the failure of the whole system. From the view of preventing the PID effect, it is better to only keep the upper PV panels. However, it is not straightforward to run the system without the lower PV panels. This is because the split DC capacitors cannot provide the required DC current to make the grid current free from DC components. It is also difficult or even impossible to maintain the voltages across the split capacitors to be balanced without employing a suitable control strategy.

1.5 Summary of Major Contributions

In this thesis, the major research is made to innovatively addresses the two fundamental challenges in a holistic way via using active control techniques, which results in the minimised number of required active switches. Fundamental, second-order voltage ripples and high-frequency CM voltage ripples are significantly reduced so that there is no need to include any bulky electrolytic capacitors and isolation transformers. This breakthrough is expected to pave the way to develop highly compact power converters with the minimum number of switches and passive components. The research conducted in the development of solutions to the two challenges have mainly resulted in the following contributions:

1. Fundamental voltage ripples in DC outputs of single-phase half-bridge rectifiers are significantly reduced through adding an actively controlled neutral leg (Section 2.3) and the corresponding active controller is proposed in Section 2.4, which is the key to enable the reduction of ripples. The required capacitance to achieve the same level of voltage ripples is considerably reduced compared to that in conventional half-bridge rectifiers.

2. A single-phase to independent three-phase conversion system is proposed (Chapter 3). The number of used switches is only eight, which is at least twelve in conventional solutions, and hence, the power density and reliability of the conversion system is improved compared to conventional solutions.

3. With the proposed ρ-converter (Section 4.2), fundamental-frequency, second-order and high-frequency CM voltage ripples are eliminated at the same time. Since only four active switches are needed, the ρ-converter is with the minimum number of switches among all solutions to such converters in the literature. It is theoretically analysed (Section 4.5) and verified by experiments (Section 4.7) that the total capacitance required can be reduced by more than 70 times while both fundamental and second-order voltage ripples are minimised.

4. It is revealed that high-frequency CM voltage ripples can be completely eliminated if the AC and DC grounds of converters are directly connected together (Section 5.2).

The key to facilitate the connection is decoupled active-control strategy of converters, which is discussed in Section 5.3.

5. In order to optimize the performance of the ρ-converter, another converter, i.e., the θ-converter, is proposed to further reduce low-frequency voltage ripples and total capacitance required (Chapter 8) and to reduce another passive component in the converter, i.e., the neutral inductor (Chapter 9). The reduction of these two components are again achieved by using active control techniques. It has been found that the total capacitance required can be reduced by more than 2.5 times (Section 8.5) and the size of the inductor can be reduced by at least 9 times (Section 9.3) compared to those in the ρ-converter.

6. A DCM ripple eliminator is proposed to reduce DC-bus capacitors and low-frequency voltage ripples in general DC systems (Chapter 10). Different from existing solutions, the voltage across the auxiliary capacitor in the eliminator can be either higher or lower than DC-bus voltage, which relaxes the constraints on the system design and also makes it possible to further reduce the auxiliary capacitance via increasing the voltage of the auxiliary capacitor.

7. The concept of the proposed DCM ripple eliminator is further developed and the ratio of capacitance reduction is quantified (Section 11.3). For the first time, it is revealed that the capability of instantly diverting the ripple current away from the DC bus is the key to improve the performance of ripple eliminators (Section 11.5). It is found that CCM ripple eliminators lead to about four times improvement of the performance on the reduction of low-frequency voltage ripples than that of DCM ripple eliminators. As a result, ripple eliminators that can be operated in CCM are preferred in practice.

1.6 List of Publications

Research Monograph

1. Q.-C. Zhong and W.-L. Ming, "Advanced power electronic converters with reduced capacitance, ripples and common-mode voltages," Wiley-IEEE Press, to be published

in 2016.

Academic Journal Papers

2. W.-L. Ming and Q.-C. Zhong, "Current-stress reduction of the neutral inductor in a rectifier with two independent outputs," ***IEEE Trans. Power Electron.***, submitted after a minor resivison.

3. Q.-C. Zhong and W.-L. Ming, "A grid-tied θ-converter with reduced common-mode current, output voltage ripples and total capacitance required," ***IEEE Trans. Power Electron.***, submitted after a major resivison.

4. X. Zhang, Q.-C. Zhong and W.-L. Ming, "Stabilization of a cascaded DC converter system via adding a virtual adaptive parallel impedance to the input of the load converter," ***IEEE Trans. Power Electron.***, vol.31, no.3, pp.1826-1832, Mar.2016.

5. W.-L. Ming, Q.-C. Zhong and X. Zhang, "A single-phase four-switch rectifier with significantly reduced capacitance," ***IEEE Trans. Power Electron.***, vol.31, no.2, pp.1618-1632, Feb.2016.

6. W.-L. Ming and Q.-C. Zhong, "A single-phase rectifier having two independent voltage outputs with reduced fundamental-frequency voltage ripples," ***IEEE Trans. Power Electron.***, vol.30, no.7, pp.3662-3673, Jul.2015.

7. X. Cao, Q.-C. Zhong and W.-L. Ming, "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," ***IEEE Trans. Ind. Electron.***, vol.62, no.4, pp.2224-2235, Apr.2015.

8. Q.-C. Zhong, Z.-Y. Ma, W.-L. Ming and G. Konstantopoulos, "Grid-friendly wind power systems based on the synchronverter technology," ***Energy Conversion and Management***, vol. 89, pp. 719-726, 2015.

9. W.-L. Ming and Q.-C. Zhong, "Reduction of common-mode currents via providing a common AC and DC ground," under review.

10. Q.-C. Zhong, W.-L. Ming, X. Cao and M. Krstic, "Instantaneous diversion of ripple currents to improve the power quality and reduce the usage of electrolytic capacitors in DC systems," under review.

11. Q.-C. Zhong, W.-L. Ming and W.-X. Sheng, "Beijing rectifiers: bridge rectifiers with a capacitor added to reduce common-mode currents, DC-bus voltage ripples and total capacitance required," under review.

12. W.-L. Ming and Q.-C. Zhong, "An improved single-phase θ-converter with reduced inductor current," under review.

13. W.-L. Ming and Q.-C. Zhong, "Diverting harmonic currents to reduce voltage ripples in a dual-buck voltage divider," under review.

14. G. Konstantopoulos, Q.-C. Zhong and W.-L. Ming, "PLL-less nonlinear current-limiting controller for grid-tied inverters: design, stability analysis and operation under grid faults," under review.

15. W.-L. Ming and Q.-C. Zhong, "Transformerless dual-buck rectifiers with two independent outputs and reduced leakage currents," under review.

16. X. Zhang, Q.-C. Zhong and W.-L. Ming, "Stabilization of cascaded DC/DC Converters via adaptive series-virtual-impedance control of the load converter ," under review.

Peer-reviewed Conference Papers

17. X. Zhang, Q.-C. Zhong and W.-L. Ming, "Fast scale instability problem of cascaded Buck conversion system and its phase-shifted-carrier solution," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept.2015.

18. X. Zhang, Q.-C. Zhong and W.-L. Ming, "Stability of DC/DC converter and DC cascaded system with different modulations," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept.2015.

19. X. Zhang, Q.-C. Zhong, W.-L. Ming and X.Ruan, "Stabilization of a cascaded DC system via adding a virtual impedance in parallel with the load converter," *2015 IEEE Int. Symp. Power Electronics for Distributed Generation Systems (PEDG)*, Jun.2015.

20. X. Zhang, Q.-C. Zhong, W.-L. Ming and X.Ruan, "Stabilization of a cascaded DC system via adding a virtual impedance in series with the load converter," *2015 IEEE Int. Symp. Power Electronics for Distributed Generation Systems (PEDG)*, Jun.2015.

21. X. Zhang, Q.-C. Zhong and W.-L. Ming, "Impedance-based local stability criterion for standalone PV-battery hybrid System," *2015 IEEE Int. Symp. Power Electronics for Distributed Generation Systems (PEDG)*, Jun.2015.

22. W.-L. Ming and Q.-C. Zhong, "Synchronverter-based transformerless PV inverters with common AC and DC grounds," *The 40th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Nov.2014.

23. W.-L. Ming Q.-C. Zhong and W.-X. Sheng, "A Single-phase rectifier with a neutral Leg to reduce DC-bus voltage ripples ," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.2734-2738, 14-18, Sept.2014.

24. W.-L. Ming and Q.-C. Zhong, "Single-phase half-bridge rectifiers with extended voltage ranges and reduced voltage ripples," *2014 IEEE Int. Symp. Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1-6, Jun.2014.

25. C. Xin, Q.-C. Zhong and W.-L. Ming, "Analysis and control of ripple eliminators in DC systems," *2014 6th Annual IEEE Green Technologies Conference (GreenTech)*, pp.29, 36, 3-4, Apr.2014.

26. W.-L. Ming and Q.-C. Zhong, "Single-phase voltage-doubler with mismatched capacitors for balanced output voltages and reduced DC-bus voltage ripples," *2013 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.4830-4836, Sept.2013.

27. Q.-C. Zhong, W.-L. Ming and M. Krstic, "A single-phase to three-phase power conversion system with reduced switches and improved output voltages," *2013 IEEE Green Technologies Conference*, pp.386-391, Apr.2013.

28. Q.-C. Zhong, W.-L. Ming and M. Krstic, “Improving the power quality of traction power systems with a single-feeding wire,” *2013 IEEE Green Technologies Conference (GreenTech)*, pp.233-238, Apr.2013.

29. Q.-C. Zhong, W.-L. Ming, C. Xin and M. Krstic, “Reduction of DC-bus voltage ripples and capacitors for single-phase PWM-controlled rectifiers,” *2012 38th Annual Conference on IEEE Industrial Electronics Society (IECON)*, pp.708-713, Oct.2012.

Chapter 2

Half-bridge Rectifiers with Reduced Fundamental-frequency Voltage Ripples

In this chapter, the drawbacks of conventional half-bridge rectifiers are first discussed. It is found that the two voltage outputs of the rectifiers contain large ripples because the currents following through the split capacitors contain significant fundamental-frequency components. Moreover, the two voltage outputs depend on each other and also on system parameters. In order to overcome these drawbacks, an actively controlled neutral leg is added to conventional half-bridge rectifiers. Furthermore, the associated decoupling control strategies are proposed. The rectification leg from the conventional half-bridge rectifier is controlled to maintain the DC-bus voltage and to draw a clean sinusoidal current that is in phase with the supply voltage. The neutral leg is controlled with a PI-repetitive controller to regulate one voltage output and also to provide the current path for any DC and/or fundamental-frequency components. As a result, the two voltage outputs are regulated independently and are robust against system parameters. The output voltage ripples are also reduced and, hence, the required capacitance to achieve the same level of voltage ripples is reduced. Experimental results are provided to validate the performance of the proposed single-phase rectifiers having very low fundamental frequency voltage ripples.

2.1 Introduction

Due to the penetration of renewable energy systems, more and more microgrids are connected to the public power grid via power converters (Zhong and Hornik, 2013b). In both AC

and DC microgrids, AC is always rectified to DC when supplying DC loads and AC/AC conversion often needs DC as an intermediate step. In many circumstances (Zhong and Hornik, 2013b; Machado et al., 2006; Dong et al., 2013a;b), it is quite normal to have single-phase utilities so single-phase rectifiers are very popular (Yao et al., 2012; 2011; Lo et al., 2002; 2007; Wang et al., 2011). A typical application of rectifiers is shown in Figure 2.1, where it is often needed to provide two separate voltage outputs with the presence of a neutral line so that it is possible to power loads at three different voltage levels (Zhang and Gong, 2013). For example, many electronic systems need ± 5 V and/or ± 15 V. Rectifiers based on conventional half-bridge rectifiers, as shown in Figure 2.2, are very attractive because they can provide two voltage outputs at relatively low costs.

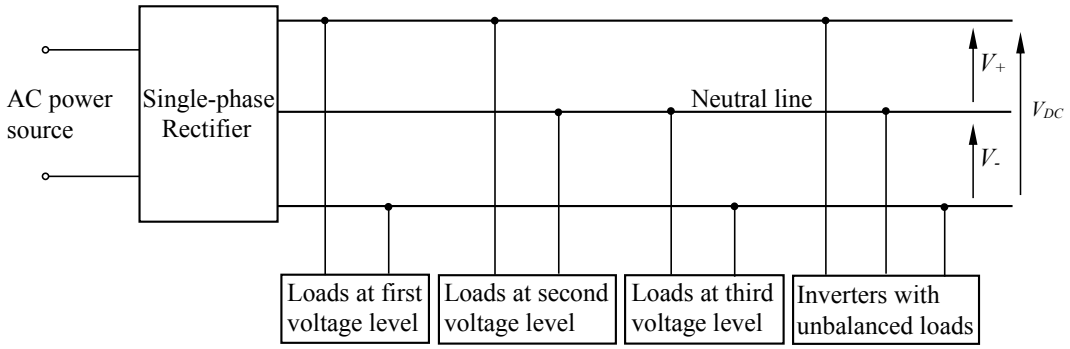


Figure 2.1: Typical application of half-bridge rectifiers.

However, the performance of the half-bridge rectifier could be reduced because of two main drawbacks. First, the two outputs are dependent on each other and also on the system parameters such as loads, capacitors and the source voltage (Srinivasan and Oruganti, 1998; Lo et al., 2002). Because of this, it is hard to obtain two independent voltage outputs, which are expected to be the same or different from each other, according to the requirements of the loads. Moreover, the regulation range of the two outputs is limited by the ratio of the dual loads (R_+ and R_-). To be more precise, when operating with dual loads, the output voltages completely depend on the ratio of the dual loads. What is even worse is that, when operating with only one of the dual loads, the half-bridge rectifier cannot work properly. This is because DC capacitors are incapable of providing any DC currents. Moreover, as the source current is provided by charging and discharging the DC capacitors, the resulting large voltage ripples can be another serious problem and bulky electrolytic capacitors are

often needed to level and smooth the ripples. However, for volume-critical and/or weight-critical systems like electrical vehicles and aircraft power systems, it is preferred to reduce the required bulky capacitors to enhance power density. For systems with batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the lifetime of batteries and fuel cells too (Liu and Lai, 2007; Wai and Lin, 2010; Itoh and Hayashi, 2010).

For the first drawback, there is very few research contributing to obtaining independent voltage outputs. Most of the previous research was focused on balancing the two voltages. Two main approaches have been reported in the literature. One of them is done at the AC side either through injecting a DC component into the AC input current (Lo et al., 2002) or through adding switches in parallel with the AC source (Lo et al., 2007). However, according to the IEEE 1547 standard, the maximum permitted DC bias in the grid current is 0.5% of the rated value. Many other strategies can be found in (Salmon, 1993), most of which also focus on strategies at the AC side. Although the voltage imbalance can be eliminated to some extent, these strategies suffer from low input power factor and/or limited voltage regulation range determined by the ratio of the dual loads. Another approach is done at the DC side through adding balancing circuits, which are put across the DC bus and then connected to the midpoint of the capacitors. In (Zhang and Gong, 2013), a bidirectional buck/boost converter composed of two switches and two inductors was used for this purpose. Due to its topological structure, this strategy also benefits with the resolved shoot-through problem. The circuit studied in (Hornik and Zhong, 2013; Zhong and Hornik, 2013a; Win et al., 2012; Zhang et al., 2013a) is shown to have the capability of balancing two voltages and creating a neutral line but it has not been applied to half-bridge rectifiers.

For the second drawback, it is worth noting that the voltage ripples in a half-bridge rectifier consists of a fundamental component and a second order component (Srinivasan and Oruganti, 1998). The fundamental one is due to the topological structure, which is an unique feature for half-bridge rectifiers. On the other hand, the second order one is caused by the pulsating input power, which is a common feature for all single-phase rectifiers. The mixture of these two components makes the output voltage ripples of conventional half-bridge rectifiers much larger than that of conventional full-bridge rectifiers. How to reduce

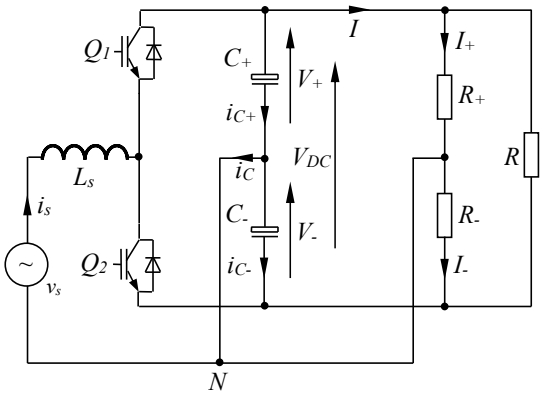


Figure 2.2: Conventional single-phase half-bridge rectifier.

the second-order component of voltage ripples has been extensively studied for different single-phase rectifiers (Wang et al., 2011; 2010; Krein et al., 2012). However, to the best knowledge of the authors, how to eliminate the fundamental component of ripples in half-bridge rectifiers has not been reported in the literature.

In this chapter, the main drawbacks of conventional half-bridge rectifiers are analysed in details at first. After that, the neutral leg used in (Hornik and Zhong, 2013; Zhong and Hornik, 2013a; Hornik and Zhong, 2010; Win et al., 2012; Zhang et al., 2013a) is put across the DC bus, linking to the midpoint of the split capacitors of conventional half-bridge rectifiers, to form a new topology for single-phase rectifiers. With the help of the neutral leg, the two voltage outputs become independent from each other and robust against parameter variations in loads and capacitors. Note that the two voltages can be different or the same, which only depend on the load requirements. What is important is that the difference of the two voltages does not cause any problem to the input current regulation (Srinivasan and Oruganti, 1998) because of the decoupled control strategies adopted. This means the total harmonic distortion (THD) of the input current and the input power factor are not affected by the voltage difference either. The unity power factor can always be achieved as well because the input current can be easily controlled to be in phase with the input voltage. Moreover, in order to obtain two independent bidirectional DC output voltages, more than six active switches are often needed but the proposed topology only needs four active switches, which reduces the cost. This is probably the topology with the minimum number of active switches to form a bi-directional converter with two independent voltage outputs that could supply three loads at the same time. Another benefit of the topology

is that the output voltage ripples can be reduced because the fundamental current component that originally flows through the split capacitors can be diverted and flows through the neutral leg. As a result, the required capacitors become smaller in order to achieve the same level of voltage ripples. Together with the rectification leg from a conventional half-bridge rectifier, the formed rectifier consists of two legs. The control of these two legs are independent, which makes the design of control strategies very flexible. In this chapter, a repetitive controller is designed to regulate the current drawn from the grid so that the DC-bus voltage is maintained and a parallel PI-Repetitive controller is designed for the neutral leg to achieve excellent voltage regulation capability even with different loads and/or different capacitors.

The rest of this chapter is organised as follows. The drawbacks of conventional half-bridge rectifiers are analysed in detail in Section 2.2. In Section 2.3, the topology of the proposed single-phase rectifier is given. After that, operation principles of the rectifier with a neutral leg are discussed in detail. The associated control strategies are developed in Section 2.4, with experimental results presented in Section 2.6. The proposed topology is then compared with a two-stage rectifier that consists of a power factor correction (PFC) converter and two dual-active-bridge (DAB) converters in Section 2.7. Conclusions are made in Section 2.8.

2.2 Drawbacks of Conventional Half-bridge Rectifiers

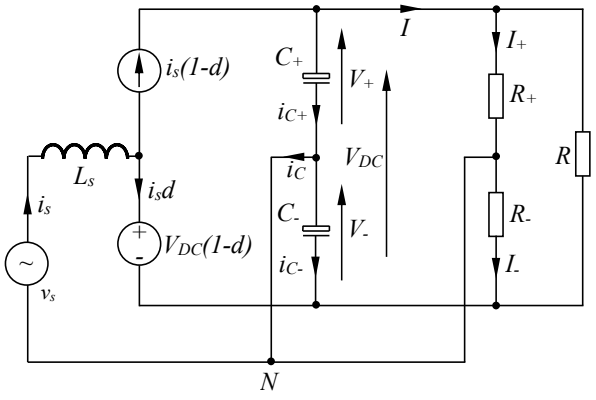


Figure 2.3: Average circuit model of conventional half-bridge rectifier.

2.2.1 Average Circuit Model and Ripple Analysis

Assume that V_+ and V_- are the voltages across the capacitors C_+ and C_-, respectively. Then the DC-bus voltage is

$$V_{DC} = V_+ + V_-. \tag{2.1}$$

Also, assume the source current of the rectifier is regulated to be sinusoidal as

$$i_s = I_s \sin \omega t \tag{2.2}$$

and in phase with the source voltage

$$v_s = V_s \sin \omega t \tag{2.3}$$

where V_s and I_s are the peak values of the input voltage and current, respectively, and ω is the angular line frequency. In this case, the power factor is unity, which is preferred in many applications. The average circuit model can be built as shown in Figure 2.3, according to (Srinivasan and Oruganti, 1998). The switches Q_1 and Q_2 are replaced with a current source $i_s(1-d)$ and a voltage source $V_{DC}(1-d)$, respectively, where d is the duty cycle of Q_2. To the best knowledge of the authors, all the analysis in the literature are based on the assumption that the split capacitors are the same and/or the dual loads are the same (Srinivasan and Oruganti, 1998; Lo et al., 2002; 2007). However, this assumption is hard to meet because the capacitors can easily become different due to their inevitable degradation. Since the loads may be different too, it is desirable that the two voltage outputs can be independent even when different loads are connected (Zhang and Gong, 2013). For this reason, detailed analysis about half-bridge rectifiers with different split capacitors and different loads is carried out in the sequel.

In order to obtain the unity power factor, the two switches are operated complementarily to track the reference source current, which is in phase with the source voltage. As the switching frequency is much higher than the line frequency, the duty cycle of switch Q_2 can be given by

$$d = \frac{V_+}{V_{DC}} - \frac{V_s}{V_{DC}} \sin \omega t \tag{2.4}$$

as demonstrated in (Srinivasan and Oruganti, 1998; Lo et al., 2007). According to the

average circuit model shown in Figure 2.3, the capacitor currents can be calculated as

$$i_{C+} = i_s(1-d) - (\frac{V_+}{R_+} + \frac{V_{DC}}{R}), \tag{2.5}$$

$$i_{C-} = -i_s d - (\frac{V_-}{R_-} + \frac{V_{DC}}{R}). \tag{2.6}$$

After substituting (2.2) and (2.4) into (2.5), there is

$$\begin{aligned} i_{C+} = & \frac{V_- I_s}{V_{DC}} \sin \omega t - \frac{V_s I_s}{2V_{DC}} \cos 2\omega t \\ & + \frac{V_s I_s}{2V_{DC}} - (\frac{V_+}{R_+} + \frac{V_{DC}}{R}). \end{aligned} \tag{2.7}$$

This can be re-written as

$$\begin{aligned} i_{C+} = & \frac{V_- I_s}{V_{DC}} \sin \omega t - \frac{V_s I_s}{2V_{DC}} \cos 2\omega t \\ & + \frac{V_-}{V_{DC}} (\frac{V_-}{R_-} - \frac{V_+}{R_+}), \end{aligned} \tag{2.8}$$

after taking into account the following power balance between the AC side and the DC side when ignoring the losses:

$$\frac{V_s I_s}{2} = \frac{V_+^2}{R_+} + \frac{V_-^2}{R_-} + \frac{V_{DC}^2}{R}. \tag{2.9}$$

Similarly, i_{C-} can be obtained as

$$\begin{aligned} i_{C-} = & -\frac{V_+ I_s}{V_{DC}} \sin \omega t - \frac{V_s I_s}{2V_{DC}} \cos 2\omega t \\ & + \frac{V_+}{V_{DC}} (\frac{V_+}{R_+} - \frac{V_-}{R_-}). \end{aligned} \tag{2.10}$$

It is clear that there are a fundamental-frequency component, a second harmonic component and a DC component in both currents. Because these are currents flowing through capacitors, the DC components have to be zero; see the next subsection for more details. The second harmonic component is a common feature existing in all single-phase rectifiers, which is caused by the pulsating input power (Wang et al., 2011; Yao et al., 2012; Krein et al., 2012). However, the fundamental component is unique for half-bridge rectifiers. After integrating the current i_{C+} and i_{C-}, it can be obviously seen that the peak-peak fundamental-frequency voltage ripples over C_+ and C_- are $\frac{V_- I_s}{\omega C_+ V_{DC}}$ and $\frac{V_+ I_s}{\omega C_- V_{DC}}$, respect-

ively, which are at least four times of the second harmonic ripples because $\frac{V_- I_s}{\omega C_+ V_{DC}} > 4\frac{V_s I_s}{4\omega C_+ V_{DC}}$ and $\frac{V_+ I_s}{\omega C_- V_{DC}} > 4\frac{V_s I_s}{4\omega C_- V_{DC}}$. The voltage ripples can be very large if C_+ and C_- are small and hence it is important and desirable to make sure that no fundamental component exists in the current. The ripple ratio of the fundamental component is $\frac{V_- C_-}{V_+ C_+}$ and the ripple ratio of the second harmonic component is $\frac{C_-}{C_+}$.

2.2.2 Operational Limit Caused by Loads

According to (2.8) and (2.10), there is a DC component in both currents. However, it is well known that no DC current can flow through capacitors and thus, the DC components $\frac{V_-}{V_{DC}}(\frac{V_-}{R_-} - \frac{V_+}{R_+})$ and $\frac{V_+}{V_{DC}}(\frac{V_+}{R_+} - \frac{V_-}{R_-})$ must be equal to 0, which means the following condition

$$\frac{V_+}{R_+} = \frac{V_-}{R_-} \tag{2.11}$$

must be satisfied. Hence, the voltages of the capacitors must be in proportion to the ratio of the dual loads, i.e. $\frac{V_+}{V_-} = \frac{R_+}{R_-}$, in the same way as a voltage divider. Since $V_+ + V_- = V_{DC}$, the voltages can be found as

$$\begin{aligned} V_+ &= \frac{V_{DC}\frac{R_+}{R_-}}{1+\frac{R_+}{R_-}}, \\ V_- &= \frac{V_{DC}}{1+\frac{R_+}{R_-}}. \end{aligned}$$

Also, V_+ and V_- should be larger than V_s in order to ensure the normal operation of the rectifier. As a result, the load ratio $\frac{R_+}{R_-}$ needs to satisfy the following condition

$$\frac{1}{\frac{V_{DC}}{V_s} - 1} < \frac{R_+}{R_-} < \frac{V_{DC}}{V_s} - 1, \tag{2.12}$$

where $\frac{V_{DC}}{V_s}$ is the voltage boost ratio. This characterises the operational limit of the rectifier, as shown in Figure 2.4. For a given voltage boost ratio, the load ratio can only be chosen within the sector shaded by the red lines. This may considerably limit the application of half-bridge rectifiers.

If only a single load R is connected, then $R_+ = R_- = +\infty$. The condition (2.11) can be naturally satisfied because $\frac{V_+}{R_+} = \frac{V_-}{R_-} \equiv 0$. In this case, the rectifier can be operated for any

load R.

If only one of the dual loads R_+ and R_- is connected, then one of $\frac{V_+}{R_+}$ and $\frac{V_-}{R_-}$ is equal to 0 but the other one is not. As a result, the condition $\frac{V_+}{R_+} = \frac{V_-}{R_-}$ cannot be satisfied. This means that the conventional half-bridge rectifier cannot work with only one of the dual loads connected.

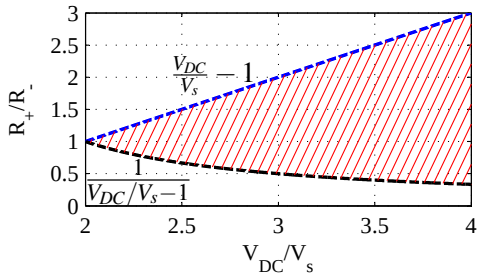


Figure 2.4: The operation limit determined by the load ratio $\frac{R_+}{R_-}$ and the voltage boost factor $\frac{V_{DC}}{V_s}$.

2.3 The Proposed Single-phase Rectifier

2.3.1 Topology

After a careful consideration of the above analysis, it can be found that the current i_C is the key to solve all the problems. First, if i_C is not required to provide DC components, then there is no operational limit caused by loads. Secondly, if i_C is free from providing the fundamental ripple current, then the fundamental voltage ripples can be completely eliminated. Thirdly, if i_C can be regulated (without introducing any DC or harmonics to the source current), then the two voltage outputs can be controlled independently. Hence, another design freedom should be introduced to enable the regulation of i_C. For this purpose, a current branch is designed by adding the neutral leg proposed in (Zhong and Hornik, 2013b; Hornik and Zhong, 2013) to the conventional half-bridge rectifier in this chapter. The formed topology is composed of a rectification leg and a neutral leg as shown in Figure 2.5. The rectification leg inherits the topology and functions from conventional half-bridge rectifiers. The neutral leg is formed by two switches Q_3 and Q_4, an inductor and two split capacitors. The introduction of the neutral leg breaks the constraint on i_C and solves the

drawbacks mentioned before.

It is worth noting that the two legs can be controlled independently. The rectification leg can be controlled to regulate the DC bus voltage, which should be the sum of the two independent voltage outputs, and to draw a sinusoidal current that is in phase with the source voltage. This is quite matured now so the emphasis of this chapter is to control the neutral leg so that the two voltages can be independent, with reduced ripples at the fundamental frequency.

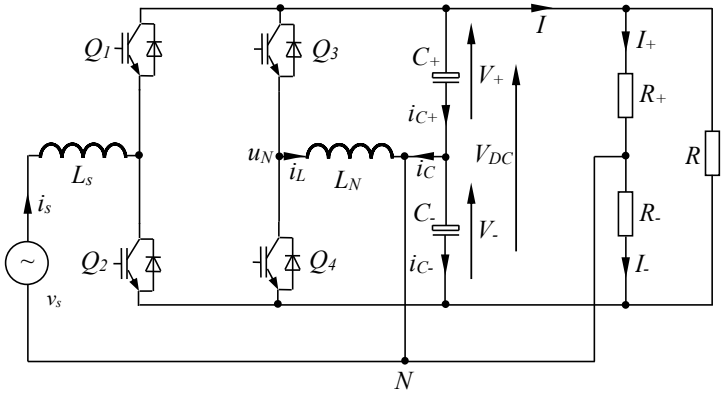


Figure 2.5: The proposed single-phase rectifier with a neutral leg.

2.3.2 Model of the Neutral Leg

The mid-point (or average) of the DC bus is

$$V_{ave} = \frac{V_+ - V_-}{2}. \tag{2.13}$$

According to the Kirchhoff's law, there is

$$u_N = L_N \frac{di_L}{dt} + R_N i_L \tag{2.14}$$

where R_N is the equivalent series resistance of the inductor. Define the currents flowing through the split capacitors are i_{C+} and i_{C-}, respectively. Then,

$$i_C = i_{C+} - i_{C-} \tag{2.15}$$

with

$$i_{C+} = C_+ \frac{dV_+}{dt} \tag{2.16}$$

$$i_{C-} = C_- \frac{dV_-}{dt} \tag{2.17}$$

As a result, the dynamic equation of the DC-bus voltage is

$$\begin{aligned} \frac{dV_{DC}}{dt} &= \frac{dV_+}{dt} + \frac{dV_-}{dt} \\ &= \frac{1}{C_+} i_{C+} + \frac{1}{C_-} i_{C-} \\ &= (\frac{1}{C_+} + \frac{1}{C_-}) i_{C+} - \frac{1}{C_-} i_C \end{aligned} \tag{2.18}$$

from which there is

$$i_{C+} = \frac{\frac{dV_{DC}}{dt} + \frac{1}{C_-} i_C}{\frac{1}{C_+} + \frac{1}{C_-}} \tag{2.19}$$

Hence, (2.16) can be re-written as

$$\begin{aligned} \frac{dV_+}{dt} &= \frac{1}{C_+} \frac{\frac{dV_{DC}}{dt} + \frac{1}{C_-} i_C}{\frac{1}{C_+} + \frac{1}{C_-}} \\ &= \frac{C_-}{C_+ + C_-} \frac{dV_{DC}}{dt} + \frac{1}{C_+ + C_-} i_C \end{aligned} \tag{2.20}$$

Since $V_{DC} = V_+ + V_-$, there is

$$\begin{aligned} \frac{dV_-}{dt} &= \frac{dV_{DC}}{dt} - \frac{dV_+}{dt} \\ &= \frac{C_+}{C_+ + C_-} \frac{dV_{DC}}{dt} - \frac{1}{C_+ + C_-} i_C \end{aligned} \tag{2.21}$$

Assume that the switching frequency is f_s and the switching period is $T_s = 1/f_s$. Define

$$q = \begin{cases} 1 & \text{when } Q_3 \text{ is on and } Q_4 \text{ is off,} \\ -1 & \text{when } Q_4 \text{ is on and } Q_3 \text{ is off.} \end{cases}$$

Then, the corresponding voltage u_N, together with its given q, can be shown in Figure 2.6.

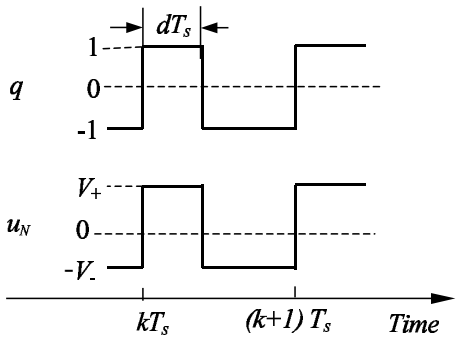


Figure 2.6: Signals q and u_N (Zhong and Hornik, 2013b).

Denote the average of q over a switching period by p. Then $p \in [-1,1]$ and the duty cycle for Q_3 is

$$d = \frac{1+p}{2}.$$

The average of u_N over a switching period (assuming that V_+ and V_- are constant within a switching period) is approximately

$$u_N = dV_+ - (1-d)V_- = \frac{p}{2}V_{DC} + V_{ave}. \tag{2.22}$$

Combining (2.14), (2.20), (2.21) and (2.22), the model of the neutral leg is shown in Figure 2.7, where $V_0 = \frac{C_-}{C_+ + C_-}V_{DC}$ plays the role of an external disturbance and p is the control variable.

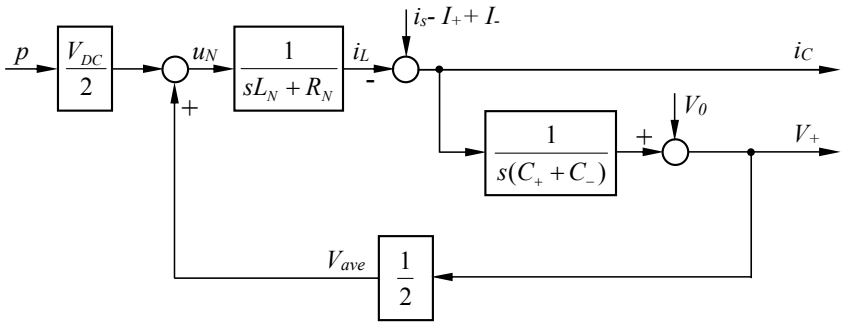


Figure 2.7: Model of the neutral leg.

2.3.3 Advantages

2.3.3.1 Removal of the operational limit on loads

The neutral leg provides the path for the source current i_s and the imbalanced current of the dual loads R_+ and R_-. According to the Kirchhoff's law, there is

$$i_L = i_s - i_C - I_+ + I_-. \tag{2.23}$$

If i_C is maintained around 0, then the imbalanced current $I_+ - I_-$ will be provided by the neutral leg but not by the split capacitors any more. The above-mentioned operational limit can then be naturally removed. The regulation of the i_C can be done through controlling the control variable p as indicated from the model of the neutral leg in Figure 2.7. As a result, the proposed rectifier can work properly no matter what kind of combinations of loads are connected.

2.3.3.2 Reduced voltage ripples

From (2.23), it can be seen that the return source current is provided by the neutral leg, but not by the split capacitors. Hence, the fundamental component of the voltage ripples on the split capacitors can be completely eliminated and the voltage ripples on V_+ and V_- can be reduced.

2.3.3.3 Provision of independent voltage outputs

Assume the references of the two independent DC outputs are V_+^* and V_-^*, respectively, which could be the same or different as long as both of them are higher than the peak value of the source voltage. This is to ensure the boost operation of the rectifier. The DC-bus voltage V_{DC} can then be maintained to be the sum of the two independent outputs by controlling the rectification leg. In other words, the reference for the DC-bus voltage should be set as

$$V_{DC}^* = V_+^* + V_-^*. \tag{2.24}$$

According to the model of the neutral leg shown in Figure 2.7, the DC output V_+ can be regulated via changing control variable p. Then

$$V_+ = V_+^* \tag{2.25}$$

in the steady state, which also means

$$V_- = V_-^*.$$

Hence, both outputs can be controlled independently.

It is worth mentioning that controlling $i_C = 0$ does not necessarily lead to $V_+ = V_+^*$ because the integrator $\frac{1}{s(C_+ + C_-)}$ (as shown in Figure 2.7) may cause the deviation of V_+ from its reference. As a result, when designing the controller for the neutral leg, the regulation of both the current and the voltage should be taken into consideration.

One question that arises naturally is that whether the different voltages V_+ and V_- would cause problems to the input current regulation. As stated previously, the rectification leg and the neutral leg are independently controlled and, as a result, the regulation of the input current only depends on the rectification leg instead of both legs. Indeed, according to (2.4), the maximum and minimum duty cycles of the two switches in the rectification leg are

$$\begin{aligned} d_{max} &= \frac{1}{V_{DC}}(V_+ + V_s) \\ d_{min} &= \frac{1}{V_{DC}}(V_+ - V_s). \end{aligned}$$

Hence, $d_{min} > 0$ and $d_{max} < 1$ can be achieved for any combinations of V_+ and V_- that are higher than V_s and the regulation of the input current is not affected by the difference between V_+ and V_-. The only effect of the voltage difference is that the DC offset of the voltage $V_{DC}(1-d)$ across the switch Q_2, which is the same as V_-, is shifted from the midpoint of the DC bus but this does not cause any problem. To make it easy to understand, the regulation of the input current is concerned about the DC-bus voltage V_{DC} and it does not matter how this is split between V_+ and V_-, which is achieved by the neutral-leg controller. Because the rectification leg is independently controlled, the input power factor and the

THD of the input current can be regulated as usual and are not affected by the difference between V_+ and V_-. Similarly, the effect of any possible DC component in the input voltage is equivalent to the voltage difference between the voltages across the two capacitors and hence is limited.

2.4 Control Design

2.4.1 Control of the Rectification Leg

As analysed before, one of the main functions for the rectification leg is to regulate the DC-bus voltage. For this purpose, the two DC voltage outputs should be measured for feedback. The sum of them constitute the DC-bus voltage, which contains two parts: a constant component and a ripple component. The constant component should be equal to its reference value $V_+^* + V_-^*$ and the ripple one is normally smoothed by DC-bus capacitors or active energy storage circuits (Wang et al., 2011; Zhang et al., 2013b; Wang et al., 2012). The constant component should be extracted from the DC-bus voltage for the feedback. Otherwise, the ripple component is introduced into the control loop, which reduces the performance and hence should be avoided. Here, the hold filter

$$H(s) = \frac{1 - e^{-Ts/2}}{Ts/2},$$

where T is the fundamental period of the supply, is used to remove the ripple component because the major ripple component is at the second harmonic frequency. A PI controller can then be used to maintain the DC-bus voltage as shown in Figure 2.8(a).

In addition to the DC-bus voltage regulation, the rectification leg is also responsible to make sure that the source current i_s is clean and in phase with the source voltage v_s. This reduces the power pollution to the source caused by the rectifier. Considering the power balance at the AC and DC sides, the output of the PI voltage controller is set as the peak amplitude of the reference of i_s. Apart from this amplitude information, the phase information of the source voltage is also needed to form the reference source current. This can be realised in many ways, e.g. with phase-lock loops (da Silva et al., 2010; Rodriguez et al., 2007), sinusoid-locked loops (Zhong and Hornik, 2013b) or sinusoidal tracking algorithms

(STA) (Ziarani and Konrad, 2004). Here, the STA proposed in (Ziarani and Konrad, 2004) is adopted. With the peak amplitude provided by the PI controller and phase information extracted using the STA, the reference source current i_s^* is then formed. What is left now is to design a current controller so that the current i_s tracks its reference.

Many current controllers, such as hysteresis controllers (Tilli and Tonielli, 1998) that have a variable switching frequency and repetitive controllers (Hornik and Zhong, 2011a) that have a fixed switching frequency, can be applied to track the current reference i_s^*. Because of the excellent harmonic rejection performance, the repetitive controller shown in Figure 2.9 is used, where $i_e = i_s^* - i_s$ is the current tracking error. The output of the repetitive controller is sent to a PWM generator to generate the PWM signals for the switches Q_1 and Q_2. The repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where τ_d is a delay term. The poles of the $C(s)$ are the solutions of the transcendental equation

$$\frac{\omega_i}{s+\omega_i} = e^{-\tau_d s},$$

which has infinitely many roots s_k, $k \in \mathbb{Z}$. The Lambert W function, whose history and properties are presented in (Corless et al., 1996), is used to solve this equation. The real part and the imaginary part of the poles s_k are

$$\begin{aligned} \mathrm{Re}\, s_k &\approx \frac{1}{\tau_d} \ln \frac{\tau_d \omega_i}{\sqrt{(\tau_d \omega_i)^2 + (2k\pi)^2}} = \frac{1}{\tau_d} \ln(1 + (\frac{2k\pi}{\tau_d \omega_i})^2) \\ \mathrm{Im}\, s_k &\approx \frac{2k\pi - \tan^{-1} \frac{2k\pi}{\tau_d \omega_i}}{\tau_d} \approx \frac{2k\pi}{\tau_d}(1 - \frac{1}{\tau_d \omega_i}). \end{aligned}$$

It is found that these poles are very close to the imaginary axis. In order to allocate the poles close to the harmonic frequencies, ideally, it is expected that $s_k = j\frac{2\pi}{\tau}k$ where τ is the system fundamental period. In this case, τ_d needs to satisfy

$$\tau_d^2 = \tau_d \tau - \frac{1}{\omega_i}\tau,$$

solutions of which are

$$\tau_d = \frac{1 \pm \sqrt{1 - \frac{4}{\omega_i \tau}}}{2} \tau. \tag{2.26}$$

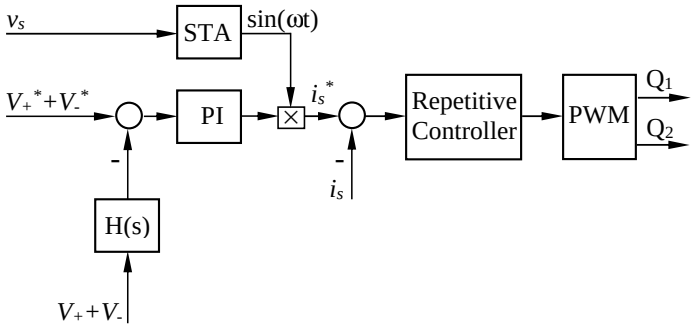
The reasonable positive solution corresponds to the plus sign in (2.26), which leads to a good recommendation for τ_d as

$$\tau_d \approx \frac{1 + 1 - \frac{2}{\omega_i \tau}}{2} \tau = \tau - \frac{1}{\omega_i}.$$

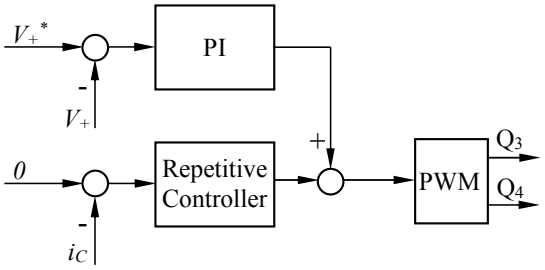
Here,

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\mathrm{s}$$

where $\omega_i = 2550$, $\tau = 0.02\,\mathrm{s}$.



(a)



(b)

Figure 2.8: Controller: (a) for the rectification leg; (b) for the neutral leg.

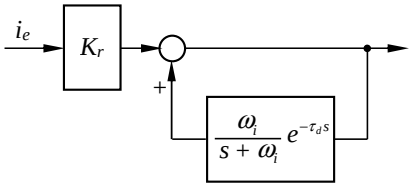


Figure 2.9: Repetitive current controller.

2.4.2 Control of the Neutral Leg

As discussed previously, one of the main tasks of the neutral leg is to maintain the current i_C close to zero. For this purpose, the current i_C should be measured as a feedback to form a current controller. Again, the repetitive controller used in the controller of the rectification leg is adopted here, as shown in Figure 2.8(b), to improve the tracking performance. The current i_C is sent to the repetitive controller as an error signal after being subtracted from its reference, which is zero in this case. If $i_C \approx 0$, then $i_L = i_s - I_+ + I_-$ is satisfied. As a result, the function of the neutral leg, providing the return source current and the imbalanced current, is achieved.

However, as can be analysed from the model of the neutral leg, V_+ could be other values than V_+^* even when $i_c = 0$ because of the existence of the integrator $\frac{1}{s(C_+ + C_-)}$. As a result, another loop is required in order to independently control the two voltage outputs. Because the rectification leg is controlled to maintain the DC-bus voltage at $V_+^* + V_-^*$, it is only necessary to control V_+ to be V_+^*. This can be achieved by using a PI controller. Naturally, $V_- = V_-^*$ can be achieved at the same time. Because this control loop only works at the DC component and the controller that regulates the current i_C only works at non-DC signals, these two controllers can be put into parallel, as done in (Hornik and Zhong, 2013; Zhong and Hornik, 2013b), by adding the output of the PI voltage controller and the output of the current controller together. The sum is then sent to a PWM block to generate drive signals for Q_3 and Q_4. The resulting controller for the neutral leg is shown in Figure 2.8(b).

Table 2.1: Parameters of the system

Parameters	Values
Supply voltage (RMS)	110 V
Line frequency	50 Hz
L_s	2.2 mH
L_N	2.2 mH
C_+	1120 μF
C_-	560 μF
R	1470 Ω
R_+	470 Ω
R_-	1000 Ω

2.5 Simulation Results

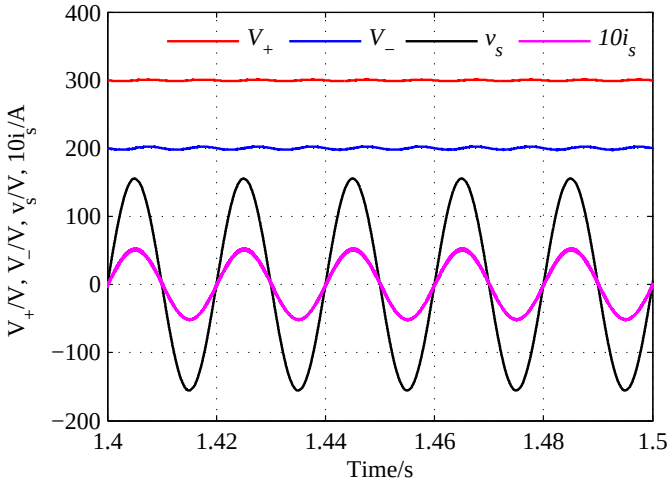


Figure 2.10: Simulation results with three loads when $V_+^* = 300$ V and $V_-^* = 200$ V.

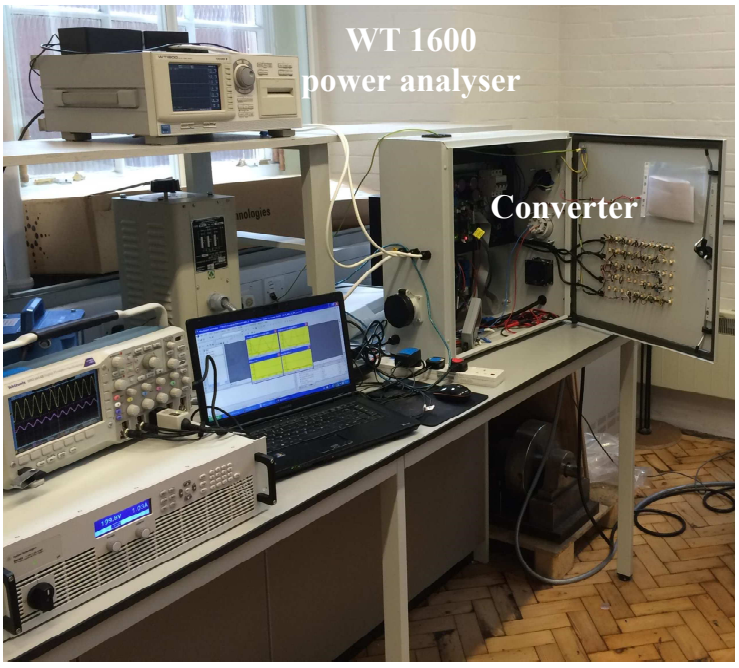
In order to verify the systems performance, a simulation system of the proposed converter was built in PLECS. The system parameters used for the simulation are summarised in Table 2.1. In order to demonstrate the independence of the two DC voltage outputs, the three DC loads and split capacitors were chosen to be different on purpose. The coefficients of the PI controller for the DC-bus voltage were chosen by trial-and-error to be $K_P = 0.05$, $K_I = 2$ and the gain of the repetitive controller for the source current i_s was selected as $K_r = 5$. In addition, the parameters of the parallel PI voltage and repetitive current controller were selected as $K_P = 0.1$, $K_I = 3$ and $K_r = 5$, respectively.

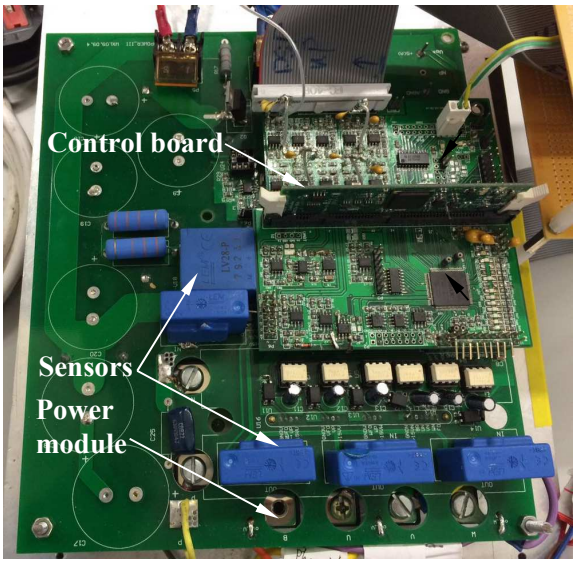
The simulation results with three loads when $V_+^* = 300$ V and $V_-^* = 200$ V are shown in

Figure 2.10. Clearly, the two DC voltages V_+ and V_- are well regulated at their references. Importantly, the grid current i_s is controlled to be clean and be in phase with the source voltage v_s, which is not affected by different voltage levels of the V_+ and V_-.

2.6 Experimental Results

As shown in Figure 2.11, the proposed single-phase rectifier was built up in the lab. An intelligent power module (IPM) was used to construct the topology of the rectifier and a TMS320F28335 DSP control board was used to control the IPM. In addition, voltage and current sensors (see Figure 2.11(b)) were adopted to measure voltages and currents that are used for control. The main system parameters are the same as the ones given in Table 2.1.





(b)

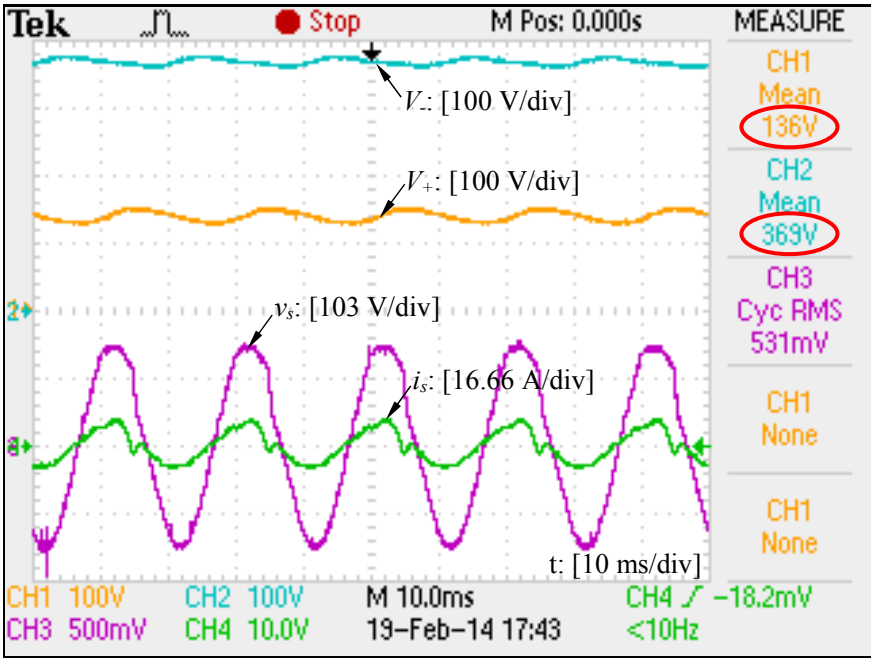
Figure 2.11: Photos of the experimental kit: (a) general structure and (b) control and power boards.

2.6.1 Steady-state Performance

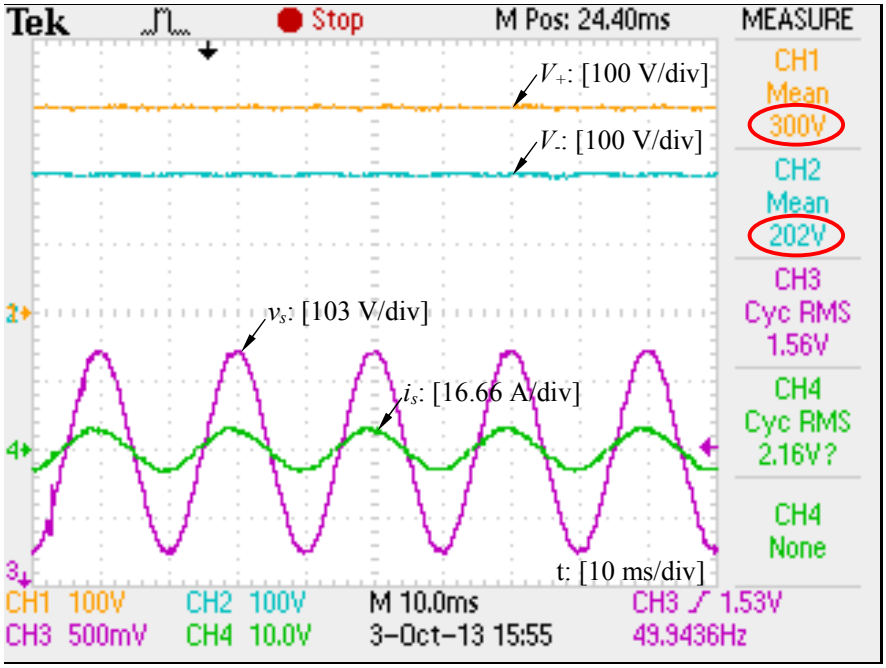
2.6.1.1 With three loads $R_+ = 470\ \Omega$, $R_- = 1000\ \Omega$ and $R = 1470\ \Omega$

In this case, both the conventional half-bridge rectifier and the proposed rectifier work but the performances are completely different. The references of the output voltages are set to $V_+^* = 300$ V and $V_-^* = 200$ V. For the conventional half-bridge rectifier, the results are shown in the (a) and (c) of Figure 2.12. Although the DC-bus voltage is around its reference[1], the source current is not sinusoidal. Although $V_+^* > V_-^*$, there was $V_+ < V_-$ in experiments because the two DC voltage outputs are determined by the loads R_+ and R_- and the voltages are not regulated.

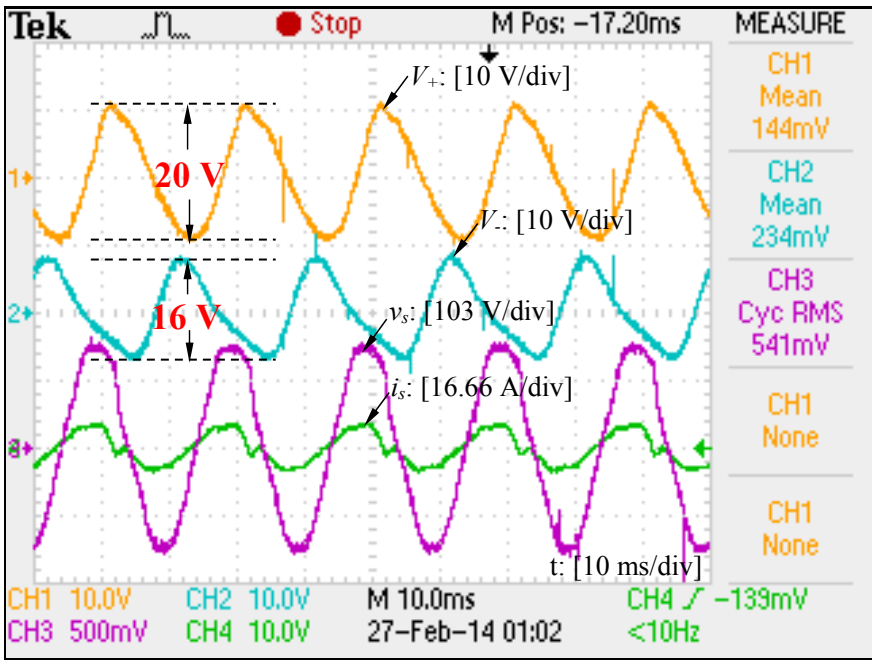
[1]Note that the tolerance of the resistors and the errors in the sensors etc. have caused some errors in the readings in the figures.


Tek
Stop
M Pos: 0.000s
MEASURE
CH1
Mean
136V
CH2
Mean
369V
CH3
Cyc RMS
531mV
CH1
None
CH1
None
V_-: [100 V/div]
V_+: [100 V/div]
v_s: [103 V/div]
i_s: [16.66 A/div]
t: [10 ms/div]
CH1 100V
CH2 100V
M 10.0ms
CH4 ⁄ −18.2mV
CH3 500mV
CH4 10.0V
19-Feb-14 17:43
<10Hz

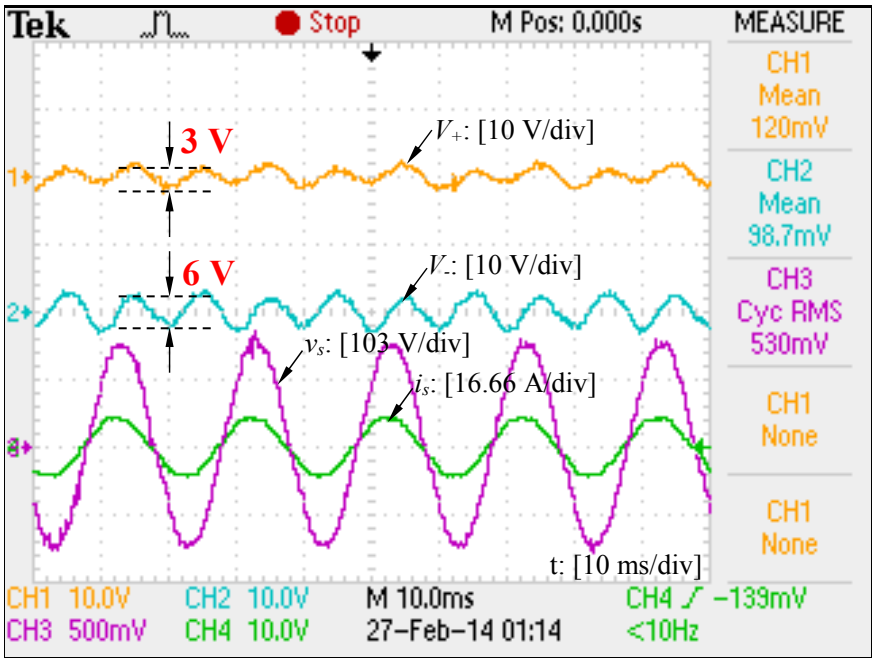
(a)


Tek
Stop
M Pos: 24.40ms
MEASURE
CH1
Mean
300V
CH2
Mean
202V
CH3
Cyc RMS
1.56V
CH4
Cyc RMS
2.16V?
CH4
None
V_+: [100 V/div]
V_-: [100 V/div]
v_s: [103 V/div]
i_s: [16.66 A/div]
t: [10 ms/div]
CH1 100V
CH2 100V
M 10.0ms
CH3 ⁄ 1.53V
CH3 500mV
CH4 10.0V
3-Oct-13 15:55
49.9436Hz

(b)



(c)



(d)

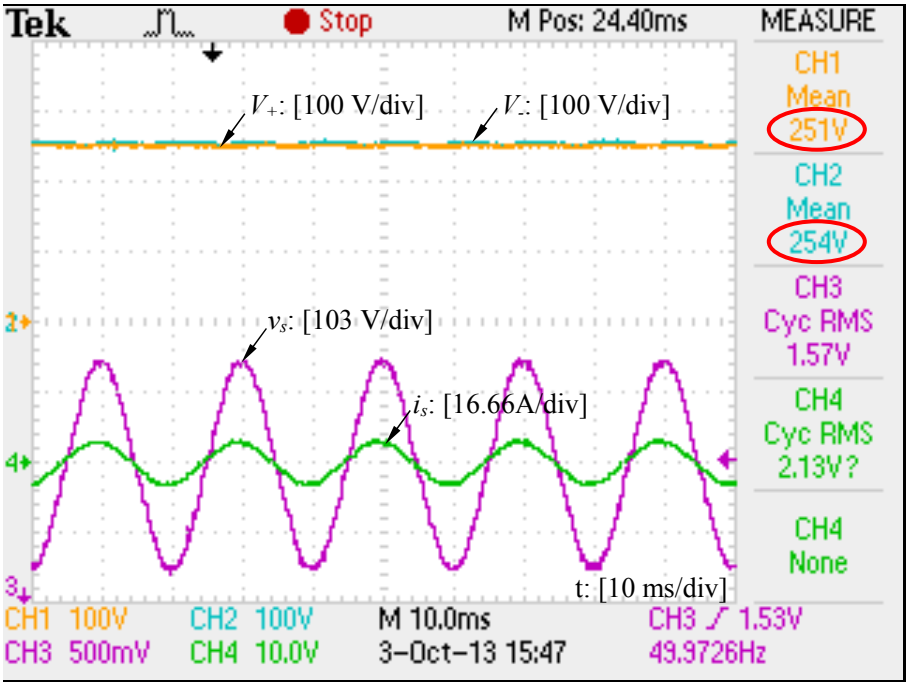
Figure 2.12: Steady-state performance with three loads ($V_+^* = 300$ V and $V_-^* = 200$ V): (a) and (c) the conventional half-bridge rectifier (without the neutral leg); (b) and (d) the proposed rectifier (with the neutral leg).

There are noticeable ripples on both voltage outputs, at the fundamental frequency. For the proposed rectifier, the results are shown in the (b) and (d) of Figure 2.12. The source

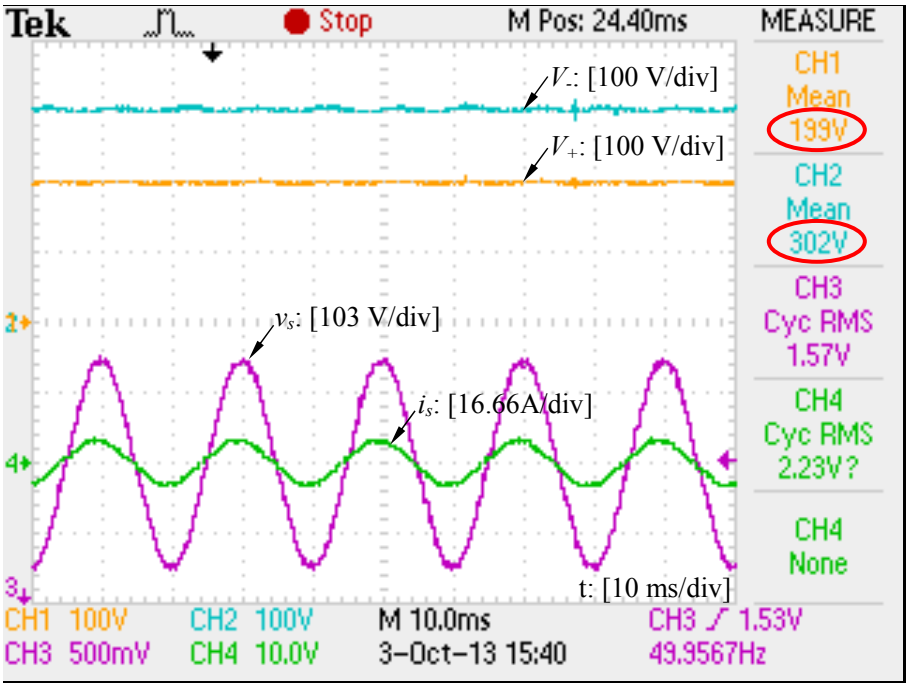
current is now sinusoidal; the two DC voltage outputs are independently well controlled to be 300 V and 200 V (producing a well-controlled DC bus voltage around 500 V); the ripples on both voltage outputs are much smaller and no fundamental-frequency component is seen. It is worth mentioning that the experimental result shown in Figure 2.12(b) has very similar result as the one shown in Figure 2.10, which verifies the accuracy of the simulations used to predict system performance.

In order to further compare the ripples of the two cases, the voltage waveforms are zoomed and shown in Figure 2.12(c) and (d), respectively. From the view of the frequency, it can be clearly seen that the major component of the ripples is at 50 Hz for the case of the conventional half-bridge rectifier and 100 Hz for the case of the proposed rectifier. This is because all the 50 Hz ripples have been diverted from the capacitors by the neutral leg. From the view of the amplitude, the output voltage ripples of conventional half-bridge rectifier are 20 V and 16 V, respectively. According to (2.8) and (2.10), the theoretical ratio of the ripple amplitudes are $\frac{V_- C_-}{V_+ C_+} \approx 1.32$, which is approximately equal to the observed value $\frac{20\,\mathrm{V}}{16\,\mathrm{V}} = 1.25$. As a result, the obtained experimental results are consistent with the theoretical analysis. After starting the neutral leg, the ripple amplitude values are dropped from 20V and 16 V to 3 V and 6 V, respectively, as shown in Figure 2.12(d). The ratio then becomes $\frac{3\,\mathrm{V}}{6\,\mathrm{V}} = 0.5$, which is the same as the theoretical value $\frac{C_-}{C_+} = 0.5$. Note that in the proposed rectifier, the ripple ratio is no longer dependent on the two output voltages but only on the capacitors. In order to clearly show the ripple reduction performance, the voltage V_+ is taken as an example to extract its 50 Hz and 100 Hz ripples from the recorded experimental data with notch filters tuned at 50 Hz and 100 Hz, respectively. For the conventional half-bridge rectifier, the peak-peak values of 50 Hz and 100 Hz ripples are 18 V and 2.3 V, respectively. After starting the neutral leg, the peak-peak value of the 50 Hz ripple is significantly reduced to 0.2 V while the 100 Hz ripple remains more or less the same (because this is not the focus of the chapter and no extra effort is taken to deal with the 100 Hz ripples).

In order to further demonstrate the capability of independently regulating the two output voltages, two other experiments were carried out for different voltage references $V_+^* = 250$ V and $V_-^* = 250$ V and $V_+^* = 200$ V and $V_-^* = 300$ V, respectively. The results are shown in Figure 2.13. The two output voltages were controlled independently very well.

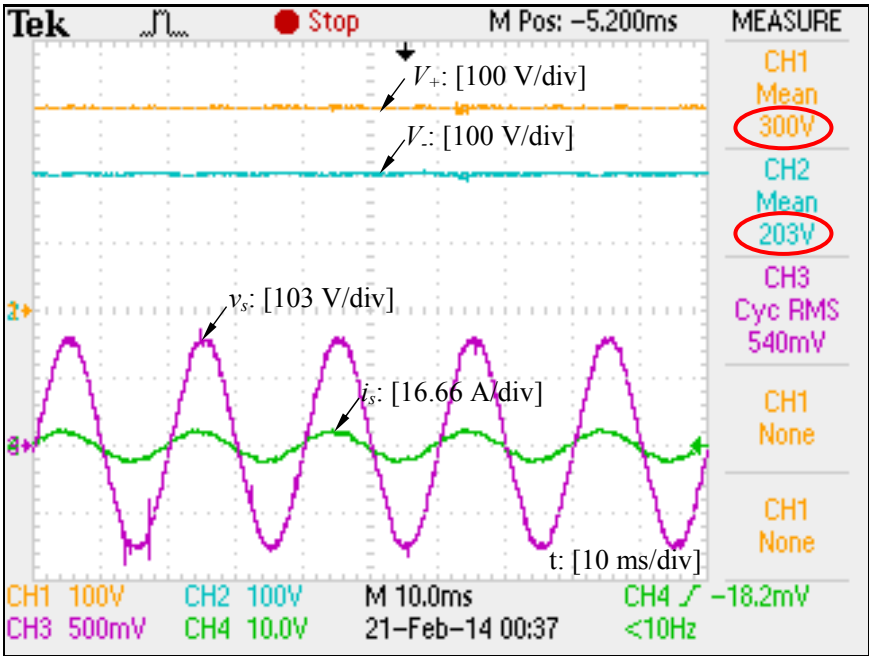


(a)

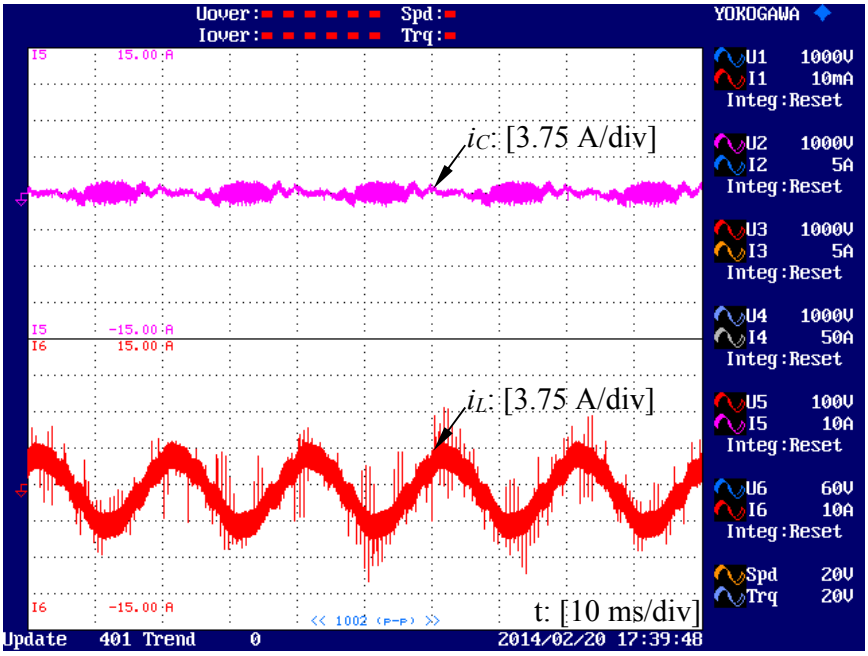


(b)

Figure 2.13: Steady-state performance with three loads: (a) $V_+^* = 250$ V and $V_-^* = 250$ V; (b) $V_+^* = 200$ V and $V_-^* = 300$ V.



(a)



(b)

Figure 2.14: Steady-state performance with only one load $R_+ = 470\ \Omega$ ($V_+^* = 300$ V and $V_-^* = 200$ V): (a) Output voltages, source current and voltage; (b) Neutral current i_C and auxiliary inductor current i_L.

2.6.1.2 With only one load $R_+ = 470\ \Omega$

Another experiment was done to test the proposed rectifier when operated with extremely different loads. Only one of the dual load $R_+ = 470\ \Omega$ was connected. Note that the conventional half-bridge rectifier does not work in this case so no experimental results can be shown. For the proposed rectifier, the results are shown in Figure 2.14(a). The output voltages and the source current are regulated very well, without any problem. Moreover, the neutral current was also well maintained around 0 as shown in Figure 2.14(b), where the inductor current i_L is also shown. It contains a DC component. According to the analysis in Section 2.3, the inductor current i_L should include a DC bias in this case to offset the current difference between the dual loads R_+ and R_-. Theoretically, the current difference should be

$$\frac{V_+^*}{R_+} - \frac{V_-^*}{R_-} = \frac{300}{470} = 0.6383\,\text{A},$$

which is very close to the bias current 0.64 A observed from Figure 2.14(b).

2.6.1.3 Input power factor and input current THD

For all the above cases with the same/different loads and/or voltage references, the THD of the input current is about 4.3% and the input power factor is about 0.99, according to the recorded data from experiments. This verifies that the regulation of the input current is not affected by the voltage difference between V_+ and V_-. Note that the experimental system is not optimised for power quality purposes because it is not the focus of this chapter. The synchronisation unit STA, the hold filter $H(s)$ and the PI controller in the rectification-leg controller shown in Figure 2.8(a) could all bring harmonic components into the reference input current. Moreover, the input filter, which is not optimised either, plays an important role in the power quality as well. Hence, the THD of 4.3% for the input current is already very good. It could be improved if the above factors are taken into consideration.

2.6.2 Transient Performance

In order to evaluate the transient performance, three cases are given here as shown in Figures 2.15-2.17. The first two were conducted with the voltage references $V_+^* = 300$ V and $V_-^* = 200$ V. For the third one, the DC voltage references were changed from $V_+^* = 300$ V

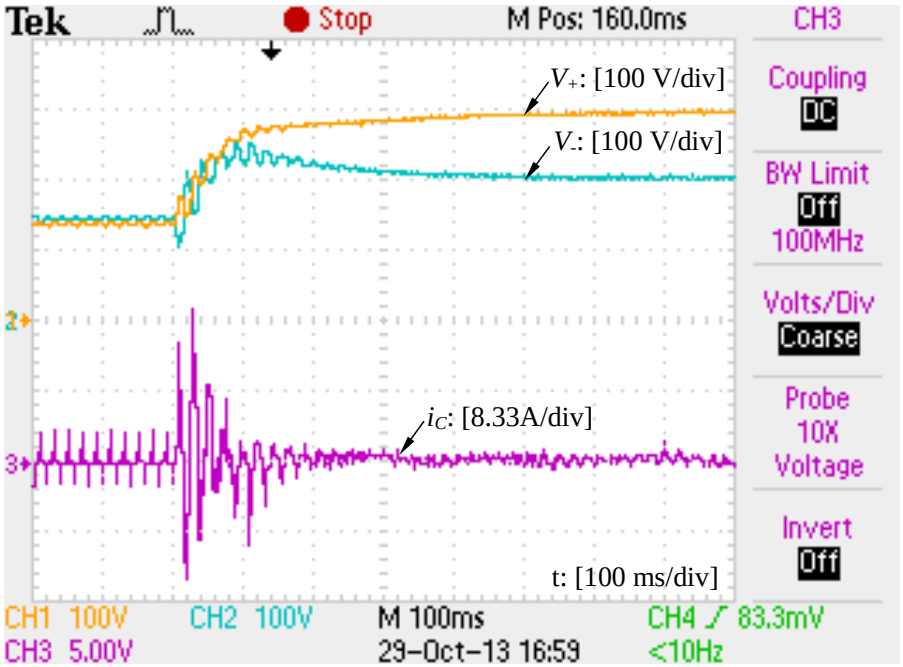


Figure 2.15: Start-up: DC outputs V_+ and V_- and neutral current i_C.

and $V_-^* = 200$ V to $V_+^* = 200$ V and $V_-^* = 300$ V as a step change.

2.6.2.1 Start-up

In the first case, the controllers for the rectification leg and the neutral leg were initially not in function. As a result, the system was operated as a diode bridge rectifier and therefore, the source current is extremely distorted. Also, the DC outputs were clamped at around 150 V, which is the peak value of the source voltage. Note that the two voltages are slightly different because of the different loads and capacitors. After the controllers were activated, the two voltage outputs quickly increased from 150 V to the reference values of 300 V and 200 V, respectively, as shown in Figure 2.15. The neutral current i_C was regulated and settled down to nearly 0. This transient response took about 400 ms, which can be reduced if the allowable maximum neutral current is increased (for the current system it is designed to be 16.66 A).

2.6.2.2 Load change

The second case was with a load change and the result is shown in Figure 2.16. All the three loads R, R_+ and R_- were initially connected and then two of them, R and R_-, were

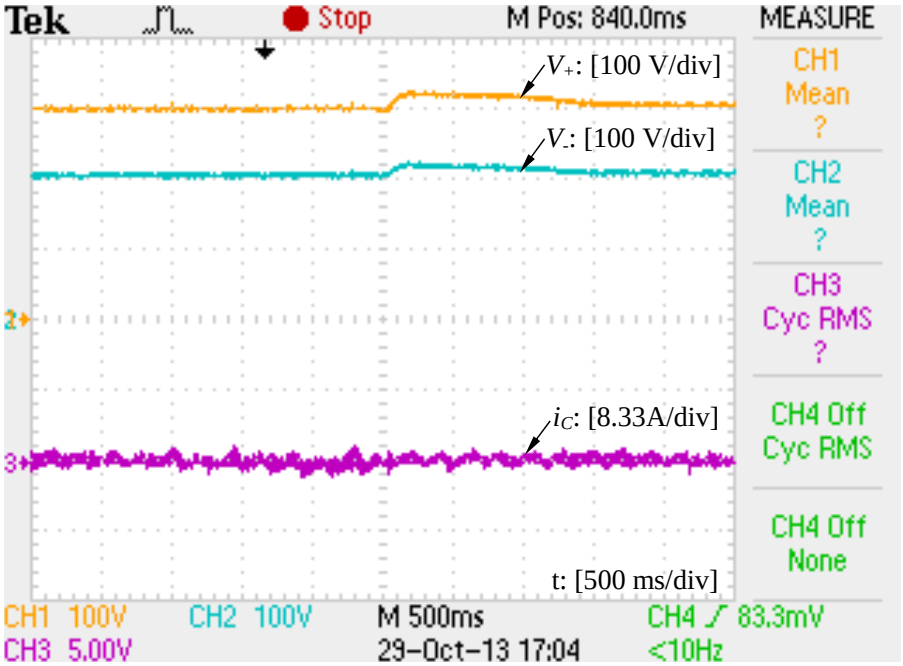


Figure 2.16: Load change: DC outputs V_+ and V_- and neutral current i_C.

suddenly cut off from the system. Due to this change, the DC outputs slightly increased and then went back to the references without any spikes. The neutral current i_C was always maintained around 0.

2.6.2.3 Change of voltage references

The last case was the change of the voltage references and the results are shown in Figure 2.17. It can be seen that the voltages are smoothly regulated to their new references from previous ones. Again, the neutral current is always around 0 without any noticeable changes. The response time in the last two cases can be shortened by increasing the allowable maximum neutral current.

2.7 Comparison with a Solution

It is not easy to identify a suitable topology for comparison because of the functions integrated in the proposed topology. After careful comparison of different topologies, the topology shown in Figure 2.18 is adopted for comparison. It is able to provide two isolated DC output voltages in an independent way and adopts the DAB DC/DC converter (Qin and

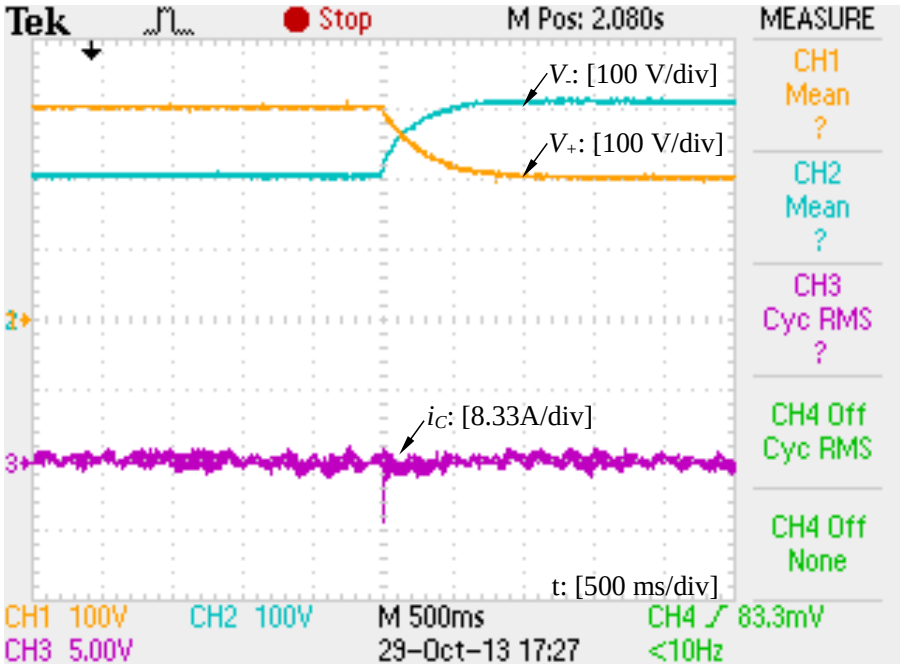


Figure 2.17: Transient response when voltage references were changed from $V_+^* = 300$ V and $V_-^* = 200$ V to $V_+^* = 200$ V and $V_-^* = 300$ V: DC outputs V_+ and V_- and neutral current i_C.

Kimball, 2014; 2012; Kan et al., 2014) cascaded with a front-end PFC converter, which are all very popular topologies. It is possible to connect a third load to the DC bus of the PFC so the system is able to supply three loads at the same time, which is the same as the proposed topology. The DAB converters use only two active switches in order to reduce the losses and the PFC rectifier only uses one switch so this system is not bi-directional but the proposed topology is bidirectional. In order to make this topology bidirectional, several more active switches need to be added, which will reduce the efficiency. Hence, the system shown in Figure 2.18 is a good candidate for comparison apart from the lack of bidirectional capability. The same parameters for the loads, capacitors, active switches and diodes etc. are adopted for both systems. It is obvious that the cost of the DAB system is much higher than that of the proposed system for the same capacity, due to the extra high-frequency transformer, the increased number of active switches (five more) and diodes (nine more), and the extra DC-bus capacitor C. If this system is made bidirectional, the cost is going to increase further. Moreover, the DAB system is much more complicated and the reliability is lower because of the increased component count.

In order to compare their efficiency, both the DAB system and the proposed system were

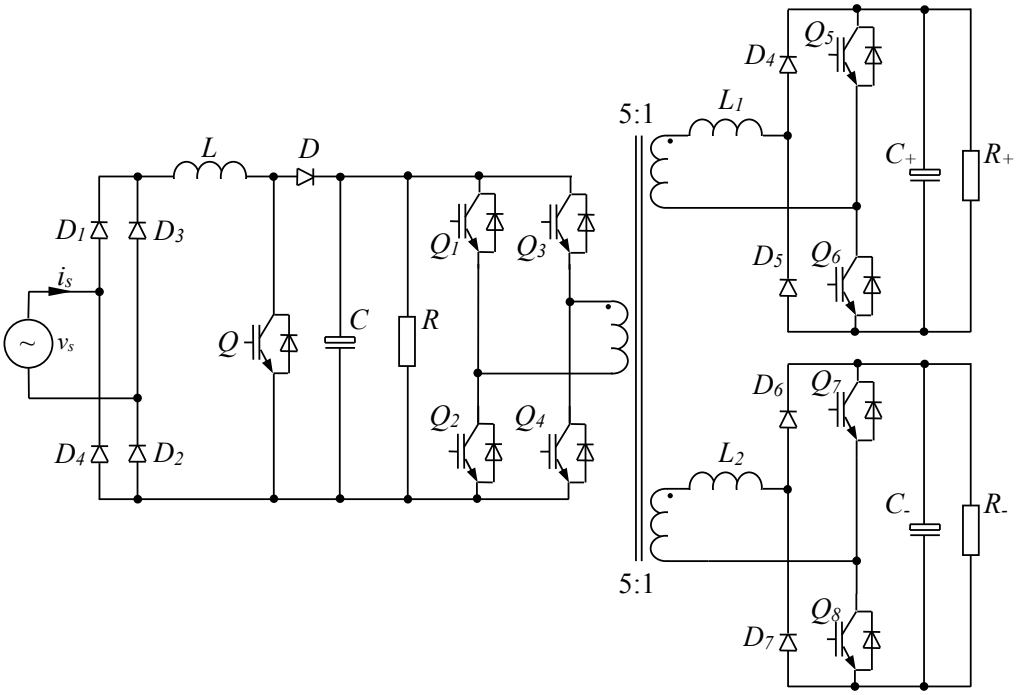


Figure 2.18: The DAB system used for comparison.

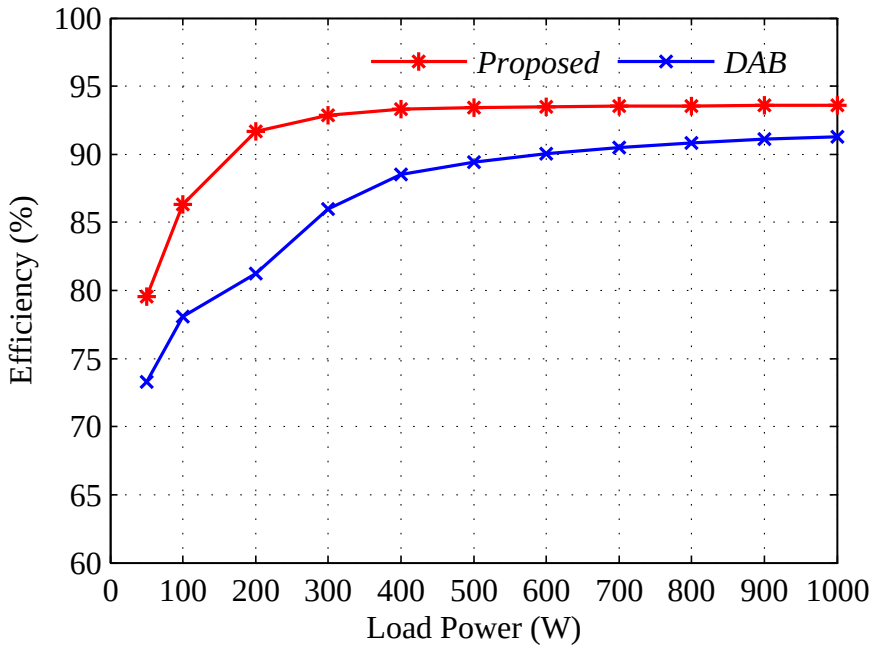


Figure 2.19: Efficiency comparison.

simulated with PLECS, which is able to accurately calculate power losses. The simulations were done with the same parameters for switches and diodes used in both systems. The obtained efficiency curves are shown in Figure 2.19. It is clear that the proposed system has higher efficiency compared to the DAB system. This is expected because of the number of switches in the proposed topology is much less than that in the DAB system.

As to the complexity of the control, it is similar for both systems. The control of the rectification leg has a similar level of complexity to the control of the PFC, both with a current regulator, and the control of the neutral leg has a similar level of complexity to the control of the two DAB converters.

Apart from the above aspects, it is also worth highlighting the important role of the neutral line provided by the proposed topology. For applications like microgrids, a neutral line is necessary if inverters need to supply unbalanced loads and is also needed if both positive and negative voltages are required by loads.

To sum up, as compared to the DAB system, the proposed system has better performance, lower costs and higher efficiency. To be fair, the DC outputs of the DAB system can be higher or lower than the DC-bus voltage but the DC outputs of the proposed system have to be lower than the DC-bus voltage. Hence, the advantage of the proposed topology is obvious.

2.8 Summary

In this chapter, a single-phase rectifier has been proposed as a unified solution to address the two main drawbacks of conventional half-bridge rectifiers. The proposed rectifier consists of a rectification leg and a neutral leg. The main functions of the rectification leg are to draw a clean current that is in phase with the source voltage and to generate a stable DC-bus voltage. On the other hand, thanks to the neutral leg, the two voltage outputs are independent with each other and are robust against with system parameters. In other words, the proposed rectifier has the capability of coping with different loads and different capacitors. Moreover, the ripples of the output voltages are reduced because the fundamental ripple current is diverted from the capacitors by the neutral leg. Although the capacitors used for experiments are not optimised, it is obvious that the capacitors can be reduced if the level

of the voltage ripples is same. Experimental results have demonstrated the capability of the proposed rectifier. Moreover, the comparison with a typical solution that adopts the popular DAB DC/DC converter cascaded with a front-end PFC converter has shown that the proposed topology offers better performance, lower cost, higher reliability and higher efficiency.

Chapter 3

Applications in Single-phase to Independent Three-phase Conversion

As an application of half-bridge rectifiers proposed in Chapter 2, a conversion system is proposed in this chapter, which can generate independent three phases from a single-phase power supply so that balanced or unbalanced, linear or non-linear three-phase loads can be operated. Again, fundamental-frequency voltage ripples are removed from DC outputs as the case in the rectifiers presented in Chapter 2. It can be used in places, e.g., rural areas, where only a single-phase power supply is available. The converter consists of four legs: i) one rectifier leg to generate a DC-bus voltage; ii) two phase legs to generate two independent phases to form balanced three-phase voltages together with the single-phase power supply and iii) one neutral leg to generate a neutral point, which is common to the single-phase supply and the two phases generated. Decoupled control strategies are developed to make sure that i) the current drawn from the single-phase supply is sinusoidal and in phase with the supply voltage, ii) the generated phase voltages contain low voltage harmonics even when the load is non-linear and iii) the neutral point is maintained stable. Simulation results are provided to verify the performance of the system.

3.1 Introduction

In some remote areas, it is quite normal to only have a single-phase power supply even though three-phase distribution systems are very common. This is particularly the case in rural areas (Cipriano dos Santos et al., 2011). But some electric appliances, e.g., air

conditioners and motors above a certain power level, require three-phase voltages. Hence, a device that converts a single-phase supply to balanced three-phase voltages is often needed. This converter is expected to have the capability of powering single-phase and/or three-phase, balanced or unbalanced, linear or non-linear loads and drawing a clean current that is in phase with the supply voltage.

Normally, this conversion process involves in an uncontrolled rectifier bridge cascaded with a three-phase full-bridge inverter via a DC bus as shown in Figure 3.1(a), which are widely adopted in motor drives (Bose, 2001). This topology causes high current harmonics and low input power factor to the supply. Moreover, the power can only unidirectionally flow from the supply to the motor. The current harmonics and low input power factor can be improved by adding a boost converter between the rectifier and the inverter (Singh and Singh, 2010) , as shown in Figure 3.1(b). Figure 3.1(c) shows another popular topology consisting of a controlled single-phase full-bridge rectifier with a three-phase full-bridge inverter (Bose, 2001; Kwak and Toliyat, 2005). Although it is able to provide a clean grid current that is in phase with the grid voltage as well as high quality output voltage, it requires ten switches to process the full power. For economic and reliable operation, it is better to reduce the number of switches. One of the rectifier legs can be replaced with a split DC link to reduce the number of switches (Lee and Kim, 2007; Singh and Singh, 2010), as shown in Figure 3.1(d). However, it has some drawbacks, such as high output voltage distortion and large DC-bus capacitors (Blaabjerg et al., 1997; Lee and Kim, 2007). For these conventional topologies, the full load power needs to be processed by the converter, which increases the cost of the converter.

An interesting topology, as shown in Figure 3.2, was proposed in (Machado et al., 2006) along the line where only partial load power needs to be processed. It takes advantage of the supply voltage as the line-to-line voltage and generates another line to form a balanced three-phase voltages. The three-phase converter in this topology acts as an active power filter to provide the reactive and harmonic currents required by the loads so that the supply current is clean and in phase with the supply voltage. Note that the generated line voltage depends on the load power. Another drawback is that no neutral line is available for unbalanced loads. Recently, a topology with a single-phase to three-phase universal active power filter, as shown in Figure 3.3, has been proposed in (Cipriano dos Santos et al.,

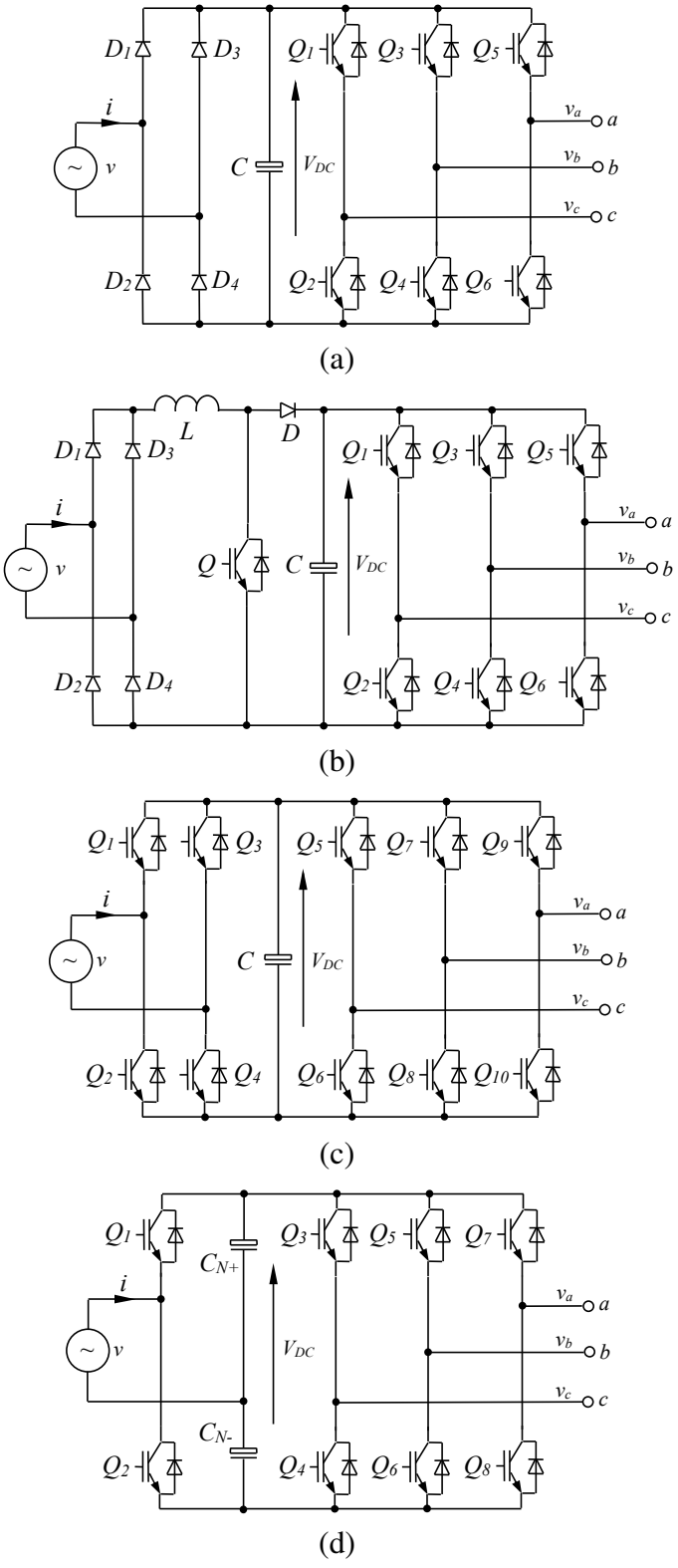


Figure 3.1: Conventional topologies

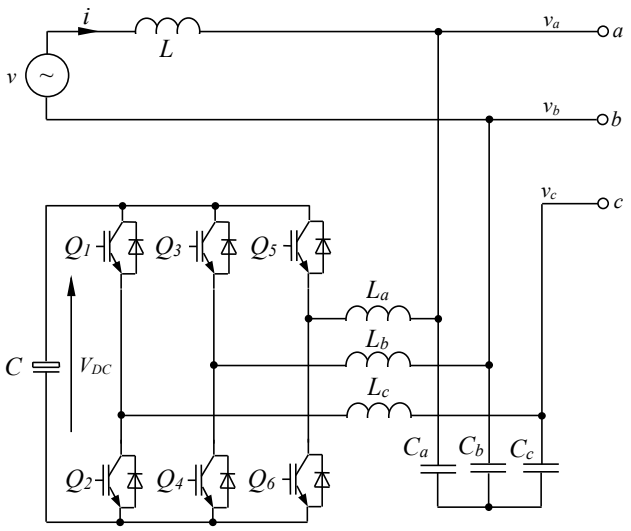


Figure 3.2: A line-interactive single-phase to three-phase converter proposed in (Machado et al., 2006)

2011). A controlled full-bridge rectifier with four switches and a transformer are added to the topology shown in Figure 3.2. The generated phase voltages are balanced and have the same voltage level as the supply voltage but a transformer is needed and no neutral line is available for the operation of unbalanced three-phase loads. Moreover, for these two topologies, there may be significant amount of harmonics in the output voltage as well since no strategies are designed to obtain high power quality under high power non-linear loads.

In this chapter, a new topology is proposed and the corresponding control strategies are developed. The proposed topology consists of a neutral leg, a rectifier leg and two phase legs, with the total of eight power semiconductor switches. The rectifier leg injects power into the DC bus to maintain a stable DC bus voltage and also maintains the current drawn from the supply to be clean and in phase with the supply voltage. The two phase legs generate two independent phase voltages, which together with the supply voltage form balanced three-phase voltages. The neutral leg is controlled to provide a stable neutral point which is shared by the supply voltage and the two phase voltages generated. This facilitates independent control of the rectifier leg and the phase legs. The provided three-phase voltages have the same phase voltage level as the supply voltage and hence no transformer is needed for loads with rated voltage same as the supply voltage. The loads of Phase *a* are directly fed by the supply and the loads of the other two phases are fed by the converter, which saves cost. Because of the provision of a neutral line, both balanced and unbalanced loads

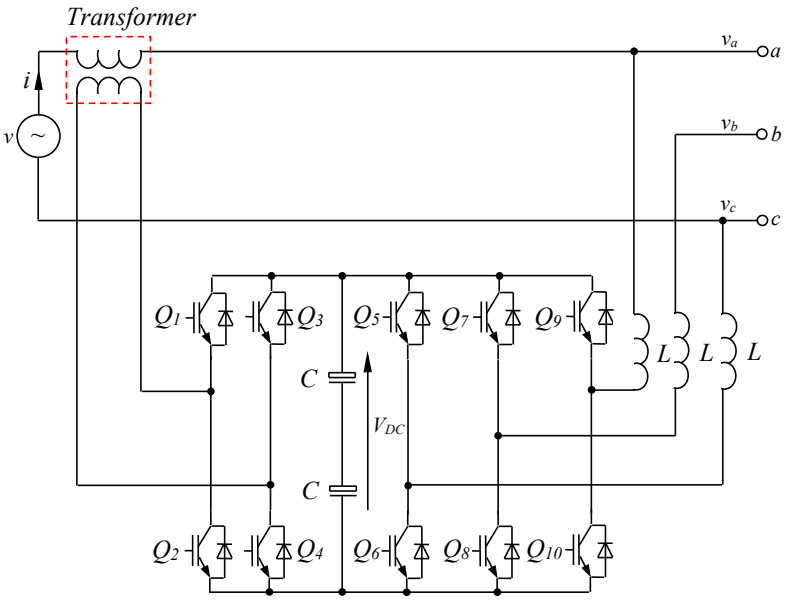


Figure 3.3: The topology with a universal active power filter proposed in (Cipriano dos Santos et al., 2011)

can be connected to the three-phase voltages provided.

Compared to the traditional full bridge converter with ten switches, two switches are saved. Moreover, when three-phase balanced loads are connected, only two thirds of the power flows through the converter, which reduces the power rating of the converter and also decreases the ripples of the DC-bus voltage. In order to obtain high-quality output voltage even when non-linear loads are supplied, a voltage controller proposed in (Zhong et al., 2012a) are used to change the output impedance of the inverter at harmonic frequencies to improve the voltage THD.

Although the proposed strategy is mainly for applications at the supply frequency, it can be applied to applications where a variable frequency is needed. In this case, the three-phase balanced load that requires a variable frequency should be connected to phase points b and c and the neutral point N, with appropriate strategies to generate the voltages; see e.g. (Lee and Kim, 2007; Hoang et al., 2011).

The rest of the chapter is organised as follows. In Section 3.2, the topology to convert a single-phase supply to independent three phases is proposed and described. The associated control strategies are developed in Section 3.3 and simulation results are presented in Section 3.4, with summary made in Section 3.5.

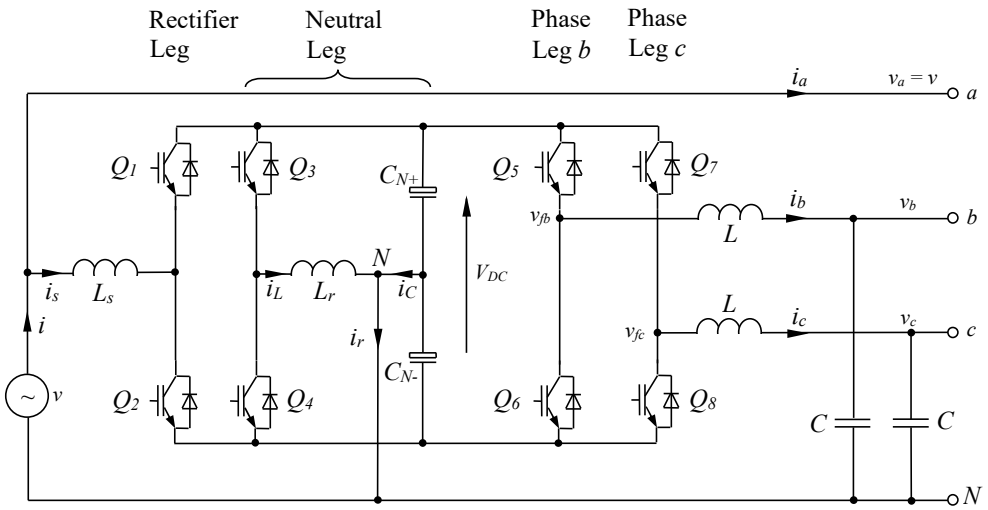


Figure 3.4: The proposed single-phase to three-phase converter

3.2 The Proposed Single-phase to Three-phase Converter

3.2.1 The Proposed Topology

The proposed scheme for single-phase to three-phase conversion with a neutral line is shown in Figure 3.4. It consists of a neutral leg, a rectifier leg and two phase legs. The neutral leg, taking the topology in (Zhong et al., 2006), consists of two switches, one inductor and two split DC-bus capacitors. It is controlled to maintain the neutral point close to the mid-point of the DC bus, which is common to the single-phase supply and to the two phases generated. The provision of a neutral point makes the three-phase voltages independent so that unbalanced loads can be operated and the operation of one phase does not affect others. The rectifier leg, together with the neutral leg, form a rectifier and the two phase legs, together with the neutral leg, form two single-phase inverters to generate two phase voltages that are $\pm\frac{2\pi}{3}$ displaced from the single-phase supply. The rectifier leg is to provide a compensation current so that the current drawn from the supply is clean and in phase with the voltage, to pass the power for the other two phases and to maintain a stable DC-bus voltage. It runs as a boost converter so that the DC-bus voltage can be maintained at a value needed by the two phase legs without a transformer. The two phase legs generate two independent phase voltages which, together with the single-phase supply, form independent balanced three phase voltages. An LC filter is connected to each phase leg to filter out the harmonics caused by the switching. It is worth noting that the provided three-phase

voltages have the same level as the single-phase supply voltage and, hence, there is no need to use transformers for loads rated at the supply voltage level, which is normally the case.

With this topology, the load of Phase a is fed directly by the single-phase supply and the loads of Phases b and c are supplied by the converter. Hence, the converter does not process the full power, which reduces the cost. If balanced loads are connected, only two thirds of the power is provided by the converter. If no loads are connected to Phases b and c, then the converter runs as an active power filter and a reactive power compensator for Phase a so that the current drawn from the grid is clean and in phase with the supply voltage. Another important property of the topology is that the rectifier leg, the neutral leg and the phase legs can be controlled independently, which offers considerable freedom in designing the controller. In principle, any control strategies developed for reactive power compensation and active power filters can be applied to the rectifier leg. Any control strategies developed for neutral legs can be applied to the neutral leg and any control strategies developed for inverters can be applied to the phase legs.

3.2.2 Basic Analysis

Assume that the single-phase supply voltage v is

$$\dot{V} = V\angle 0,$$

where V is its RMS value, and that the generated two phase voltages together with the supply voltage form balanced three-phase voltages to supply three-phase linear loads with the load angle (lagging) of θ, θ_b and θ_c, respectively. Moreover, assume that the power loss in the converter is negligible. Then the (real) power supplied is equal to the (real) power consumed by the load, i.e.,

$$\begin{aligned} VI &= VI_a\cos\theta + V_bI_b\cos\theta_b + V_cI_c\cos\theta_c, \\ &= VI_a\cos\theta + VI_b\cos\theta_b + VI_c\cos\theta_c \end{aligned}$$

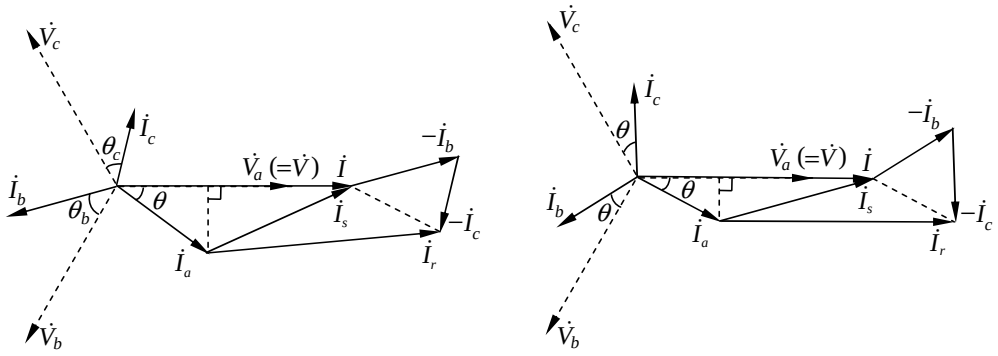


Figure 3.5: Phasor diagram of the system: (a) with linear unbalanced three-phase loads, (b) with linear balanced three-phase loads.

where I_a, I_b and I_c are the RMS values of the three-phase load currents. Hence, the RMS value of the current drawn from the supply is

$$I = I_a \cos\theta + I_b \cos\theta_b + I_c \cos\theta_c.$$

If the loads are balanced, i.e. when $\theta = \theta_b = \theta_c$ and $I_a = I_b = I_c$, then the supply current is

$$I = 3I_a \cos\theta.$$

According to the Kirchhoff's current law, there are

$$i_s = i - i_a, \tag{3.1}$$

and

$$i_r = i - i_a - i_b - i_c = i_s - i_b - i_c. \tag{3.2}$$

As a result, the phasor diagram of the system can be obtained as shown in Figure 3.5, where the cases with linear balanced and unbalanced three-phase loads are illustrated. The current I_s is

$$I_s = \sqrt{I^2 + I_a^2 - 2I_a I\cos\theta}.$$

When the loads are linear and balanced, there are

$$I_s = \sqrt{I_a^2 + (3I_a\cos\theta)^2 - 6I_a^2\cos^2\theta} = \sqrt{1+3\cos^2\theta}\,I_a,$$

and $i_r = i$, which means

$$I_r = I = 3I_a \cos\theta.$$

Hence,

$$I_s \leq 2I_a \quad \text{and} \quad I_r \leq 3I_a.$$

These can be applied to determine the current ratings of the switches of the rectifier leg and the neutral leg.

3.3 Controller Design

As mentioned before, the controller of the four legs can be decoupled and designed independently. The main function of the controller for the rectifier leg is to draw a clean sinusoidal current that is in phase with the supply voltage and to maintain a constant DC bus, which automatically transfers power to the two phases. This is quite similar to the function of a combined active power filter and reactive power compensator. The main function of the controller for the neutral leg is to make the voltage of the common point of the split capacitors with respect to the mid-point of the DC bus stable and close to zero and to provide a return current path for the rectifier leg and the phase legs. As a result, the common point of the split capacitors can be used as the neutral point N that is common to the supply and the two phases generated, which is vital to the operation of the system. The main function of the controller for the phase legs is to convert the DC bus voltage into two phase voltages with low harmonics to form balanced three phase voltages together with the single-phase supply.

3.3.1 Synchronisation Unit

In order to make sure that the current drawn from the supply is in phase with the supply voltage and also that the generated phase voltages are able to form balanced three-phase voltages together with the supply voltage, a synchronisation unit is needed to provide the phase information of the supply. This can be obtained from many ways, e.g. with phase-locked loops (PLL) (da Silva et al., 2010; Rodriguez et al., 2007) or sinusoidal tracking algorithms (STA) (Ziarani and Konrad, 2004), as shown in Figure 3.6(a). Once the phase

information of the supply ωt is obtained, the phase information of the generated voltages can be obtained via adding $\pm\frac{2\pi}{3}$ to it. The unit also needs to provide the RMS value of the supply voltage to be used as the reference RMS value for the generated phase voltages. In this chapter, the STA proposed in (Ziarani and Konrad, 2004) is adopted in the synchronisation unit shown in Figure 3.6(a).

3.3.2 Control of the Rectifier Leg

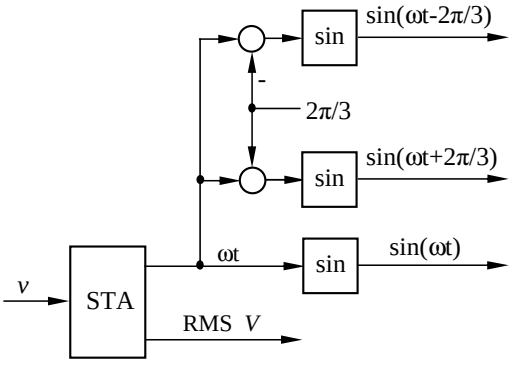
As mentioned before, an important function of the rectifier leg is to inject the right amount of current to maintain a stable DC-bus voltage. This can be achieved by introducing a PI controller, as shown in Figure 3.6(b). Because there are ripples in the DC-bus voltage at the doubled supply frequency, a low-pass filter, e.g. the hold filter

$$H(s) = \frac{1 - e^{-Ts/2}}{Ts/2},$$

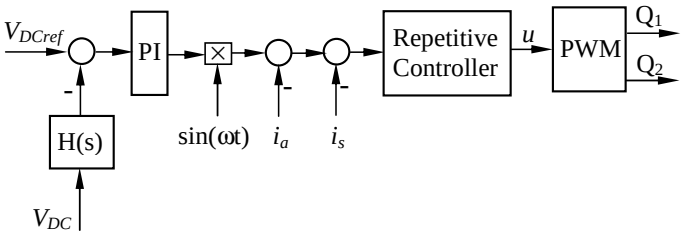
where T is the fundamental period of the supply, can be adopted to remove the ripples of V_{DC} for feedback.

The output of the PI controller actually plays the role of the reference peak amplitude of the current drawn from the supply. The reference current drawn from the supply is then obtained via multiplying it with the phase signal $\sin \omega t$ of the supply voltage provided by the synchronisation unit shown in Figure 3.6(a). This makes sure that no reactive power is drawn from the supply. The reference current of i_s for the rectifier leg is then obtained from subtracting i_a from the reference current drawn from the supply. As a result, all the harmonic current components in i_a are automatically diverted into the reference current of i_s and no extra effort is needed to suppress the current harmonics in the supply current. What is left is to design a current controller so that the current i_s tracks the reference current.

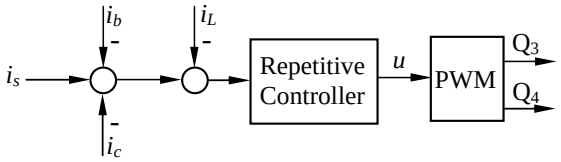
Many current controllers, e.g., hysteresis controllers (Tilli and Tonielli, 1998) that have a variable switching frequency and repetitive controllers (Hornik and Zhong, 2011a) that have a fixed switching frequency, can be applied to track the reference current of i_s. In this chapter, a repetitive controller shown in Figure 3.7 is adopted, where i_e is the current error



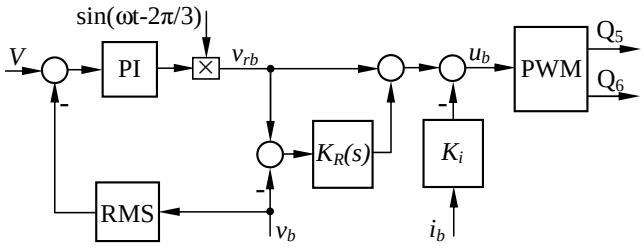
(a) Synchronisation unit



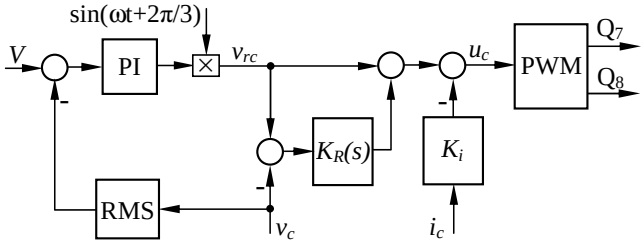
(b) Controller for the rectifier leg



(c) Controller for the neutral leg



(d) Controller for Phase Leg *b*



(e) Controller for Phase Leg *c*

Figure 3.6: The proposed control strategy

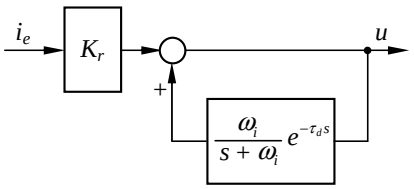


Figure 3.7: Repetitive current controller.

signal. The controller consists of a proportional controller K_r and an internal model:

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where K_r and τ_d are designed based on the analysis in (Hornik and Zhong, 2011a; Weiss and Hafele, 1999) as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0199sec,$$
$$K_r = \omega_i L_r,$$

in which L_r is the neutral line inductor and $\omega_i = 10000$, $\tau = 0.02sec$.

For this purpose, the current i_s is measured for feedback. Since both the supply voltage and the supply current $i = i_a + i_s$ are available, a power meter can be easily embedded into the system for metering purposes.

3.3.3 Control of the Neutral Leg

The neutral leg included in Figure 3.4 is composed of switches Q_3 and Q_4, one inductor L_r and two split DC-bus capacitors. This topology has been the target of several papers; see e.g. (Zhong et al., 2006) for its detailed modelling and control. It is the combination of a split DC link and a neutral leg with the advantage of being controlled separately (Zhong et al., 2006). Assume the voltages across the capacitors C_{N+} and C_{N-} with respect to the neutral point N are V_{N+} and V_{N-}, respectively. Then the DC-bus voltage is

$$V_{DC} = V_{N+} - V_{N-} \tag{3.3}$$

and the voltage of the neutral point N with respect to the mid-point of the DC bus, which is the reference point common to the supply voltage and the phase voltages generated, is

$$V_{ave} = V_{N+} - \frac{V_{DC}}{2} = \frac{V_{N+} + V_{N-}}{2}. \tag{3.4}$$

The main task of the neutral-leg controller is to maintain the voltage V_{ave} close to zero via controlling Q_3 and Q_4. At the same time, it provides a return current path for the rectifier leg and the phase legs. If the switches are controlled so that $i_L \approx i_r$ and $i_C \approx 0$, then almost no current flows through the split DC-bus capacitors. As a result, the voltage V_{ave} is stable and close to 0.

According to (3.2), the current i_r is $i_s - i_b - i_c$. If this is applied as the reference current for the inductor L_r, then the current i_C can be controlled to be nearly 0 via operating the switches Q_3 and Q_4. Hence, the control of the neutral leg is also a current-tracking problem.

Here, the inductor current i_L is measured for feedback and a repetitive controller is applied so that it is able to track the reference inductor current $i_s - i_b - i_c$, as shown in Figure 3.6(c).

3.3.4 Control of the Phase Legs

Since a neutral point that is closed to the mid-point of the DC bus is available, each phase leg could take the form of a half bridge connected with an LC filter, as shown in Figure 3.4. This topology has been widely studied, e.g. in (Liang et al., 2009; Srikanthan and Mishra, 2010). One important aspect here is that the phase of the voltage generated should be synchronised with the supply voltage with Phase b lagging the supply voltage by $\frac{2\pi}{3}$ and Phase c leading the supply voltage by $\frac{2\pi}{3}$. This requires the phase shift at the fundamental frequency caused by the LC filter to be small. The second important aspect is that the output voltage should contain low voltage harmonics even when the load is non-linear. There are many control strategies available for this; see e.g. (Weiss et al., 2004) for repetitive control-based strategy. The third important aspect is that the RMS value of the generated voltage should be the same as that of the single-phase supply voltage.

3.3.4.1 Generation of a clean voltage with the right phase

In order to address the first and second aspects, the simple and effective strategy proposed in (Zhong et al., 2012a) can be adopted. As shown in Figure 3.6(d) or Figure 3.6(e), it consists of a current feedback loop to force the output impedance of the phase to be resistive and a voltage loop to track the reference phase voltage v_{rb} or v_{rc}, respectively. The voltage loop is able to reduce the output impedance at harmonic frequencies, which is able to reduce the harmonic components of the output voltage.

Take Phase b as an example. The following hold for the voltage loop and the current loop:

$$u_b = v_{rb} - K_i i_b + K_R(s)(v_{rb} - v_b)$$

and

$$u_{fb} = sLi_b + v_b.$$

Since the switches are operated so that the average of u_{fb} during a switching period is the same as u_b, there is

$$v_{rb} - K_i i_b + K_R(s)(v_{rb} - v_b) = sLi_b + v_b.$$

That is,

$$v_b = v_{rb} - Z_o(s) i_b,$$

where the output impedance $Z_o(s)$ is

$$Z_o(s) = \frac{sL + K_i}{1 + K_R(s)}.$$

When there is no load, the output voltage v_b is the same as the reference voltage

$$v_{rb} = \sqrt{2}V \sin(\omega t - \frac{2\pi}{3})$$

and, similarly, the output voltage v_c is the same as the reference voltage

$$v_{rc} = \sqrt{2}V \sin(\omega t + \frac{2\pi}{3}).$$

There is no any phase shift or voltage drop.

If there is a load, then the voltage changes slightly because of the load effect. The smaller the output impedance, the smaller the voltage change. In particular, this is true for the harmonic voltage components. In order to improve the THD of the output voltage, the output impedance at harmonic frequencies should be small. This can be done via selecting appropriate $K_R(s)$. If the real part of $K_R(s)$ is positive, then the THD of the phase voltage can be reduced. The block $K_R(s)$ can be chosen to have high gains to obtain a small output impedance at harmonic frequencies. There are many ways to design K_R. One of them is to use the resonant harmonic compensator (Castilla et al., 2009; Shen et al., 2010)

$$K_R(s) = \sum_{h=3,5,\cdots} \frac{2\xi\omega s}{s^2 + 2\xi h\omega s + (hw)^2} \times K_h$$

of which the gain at frequency hw is K_h with zero phases for $1 + K_R(s)$ with $\xi = 0.01$ that is to be used in simulations later. It is almost one everywhere apart from the harmonic frequencies. This means the output impedance can be tuned to be different values at different harmonic frequencies to improve the THD. For most cases, the coefficients K_h should be between 1 and 20 with a larger value for lower harmonics but a smaller value for higher harmonics.

3.3.4.2 Regulation of the RMS value of the generated phase voltage

In order to address the third aspect, another loop is added to regulate the RMS value of the phase voltages generated, as shown in Figure 3.6(d) or Figure 3.6(e). The controller takes the form of a simple PI controller, with the RMS value of the phase voltage generated as feedback. This makes sure that all the three-phase voltages have the same RMS value even when loaded. The output of the PI controller plays the role of the peak amplitude of the reference phase voltage, which is multiplied with the phase information $\sin(\omega t - \frac{2\pi}{3})$ or $\sin(\omega t + \frac{2\pi}{3})$ provided by the synchronisation unit shown in Figure 3.6(a) to form the reference phase voltage v_{rb} or v_{rc}.

3.4 Simulation Results

Simulations were carried out in MATLAB/Simulink to verify the proposed topology and control methods. The solver used was ode23tb with a maximum step size of 1μs. Different

Table 3.1: Parameters of the system

Parameters	Values
Supply voltage	220 V
L_s and L_r	$1.5\,mH$
L	$1\,mH$
C	$20\,\mu F$
C_{N+} and C_{N-}	$4000\,\mu F$
Initial DC-bus voltage	$600\,V$
DC-bus voltage	$800\,V$

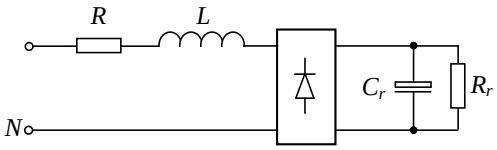


Figure 3.8: Model of non-linear loads

simulations with linear balanced loads and non-linear unbalanced loads were carried out. The model of non-linear loads is shown in Figure 3.8 and the other parameters of the system are given in Table 3.1. The switching frequency of the repetitive controllers is 10 kHz. The K_h are 10 for the fundamental and 20, 10, 5 and 5, respectively, for the 3rd, 5th, 7th and 9th harmonics. $K_i = 4$, the parameters of the PI controller for the DC-bus voltage are $K_P = 0.8$, $K_I = 10$ and the parameters of the PI controller for the RMS phase voltages are $K_P = 16$, $K_I = 248$. $K_r = \omega_i L_N = 15$ for the repetitive current controller.

3.4.1 With Linear Balanced Three-phase Loads

In this simulation, the three-phase loads were linear and balanced, consisting of a resistor of $5\,\Omega$ in series with an inductor of 10 mH for each phase. The simulation was started at 0s with the rectifier leg and the neutral leg turned on at 0.04s and the phase legs turned on at 0.12 s, respectively. The simulation results are shown in Figure 3.9.

When started, the supply current was not in phase with the supply voltage. After the rectifier leg and the neutral leg were turned on, the supply current became in phase with the supply voltage, as shown in Figure 3.9(a). Moreover, the amplitude of the grid current was reduced because only the real power (of Phase a) was drawn from the supply. The DC-bus voltage was regulated to be around 800 V and the neutral point was maintained stable. The

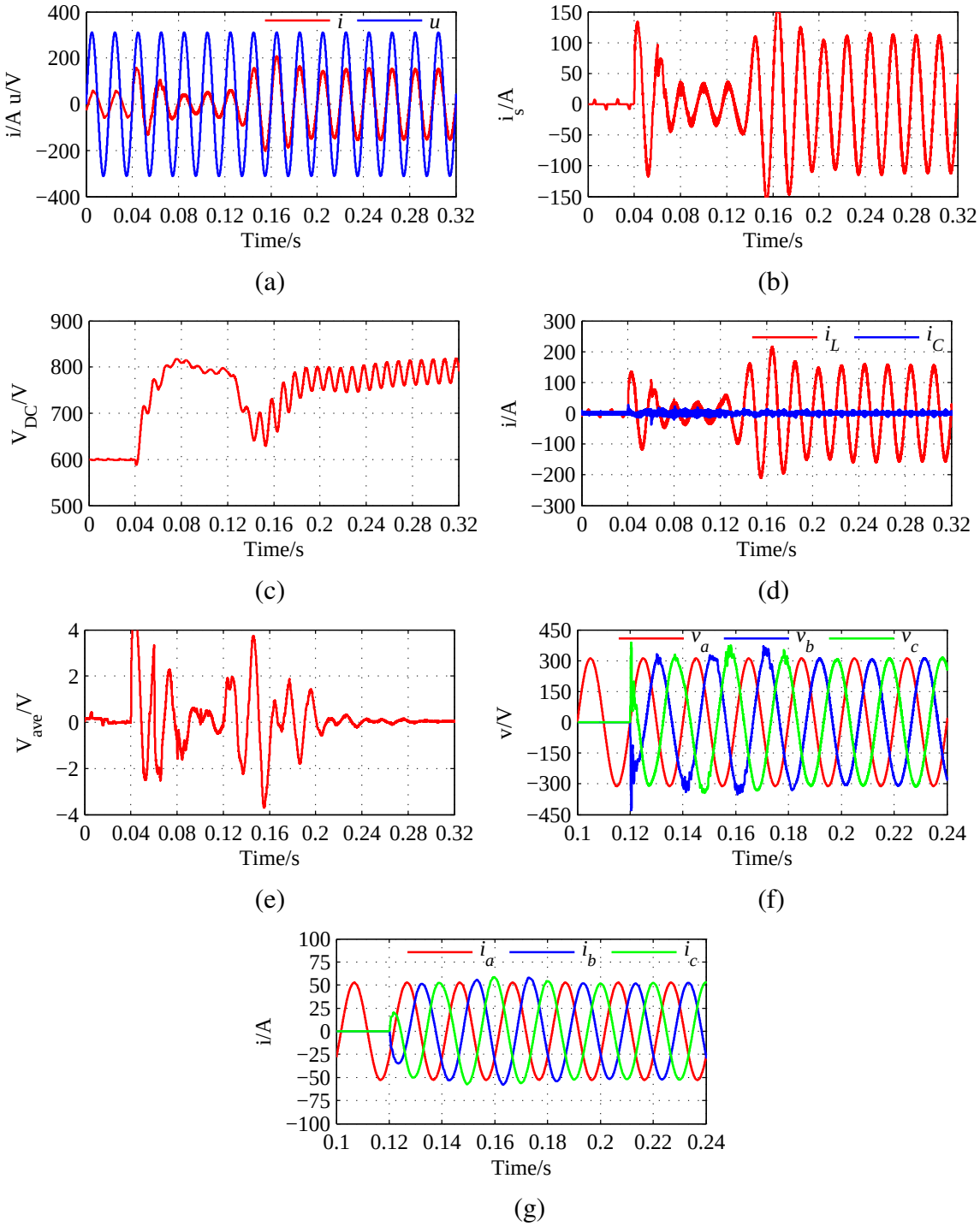


Figure 3.9: Simulations results for the case with linear balanced three-phase loads. (a) Supply current and voltage. (b) Current of the rectifier leg. (c) DC-bus voltage. (d) Inductor and capacitor currents of the neutral leg. (e) Shift of the neutral point voltage V_{ave}. (f) Three-phase voltages provided. (g) Three-phase load currents.

Table 3.2: Parameters of non-linear unbalanced three-phase loads

Phase	Parameters of the load
a	$R = 3\,\Omega$, $L = 1\,\text{mH}$, $R_r = 10\,\Omega$, $C_r = 800\,\mu\text{F}$
b	linear, with 5Ω in series with an inductor of 10mH
c	$R = 10\,\Omega$, $L = 5\,\text{mH}$, $R_r = 15\,\Omega$, $C_r = 1000\,\mu\text{F}$

current i_C was maintained small, without a visible fundamental component.

After the two phase legs were turned on, the supply current increased but was still clean and in phase with the supply voltage. The currents flowing through the rectifier leg and the neutral-leg inductor all increased because of the power consumed by the loads connected to Phase b and Phase c. The DC-bus voltage dropped but quickly recovered in about 5 cycles. The ripples in the DC bus voltage became larger because the power exchanged became heavier. The shift V_{ave} of the neutral point became larger as well because of the increased current i_L but was still within ± 3 V. The current i_C was still maintained small. The three-phase output voltages, as shown in Figure 3.9(i), settled down in about two cycles and the THD of generated Phase b and Phase c voltages was less than 2%.

3.4.2 With Non-linear Unbalanced Three-phase Loads

In this simulation, the three-phase loads were non-linear and unbalanced. Two single-phase rectifier loads shown in Figure 3.8 with different parameters were connected to Phase a and Phase c, respectively, and a linear load was connected to Phase b. The parameters of the loads are given in Table 3.2. The simulation was started at 0 s with the rectifier leg and the neutral leg turned on at 0.04 s and the phase legs turned on at 0.12 s, respectively. The results are shown in Figure 3.10.

Before the rectifier leg and the neutral leg were turned on, the supply current contained significant amount of harmonic components with THD>40% and was not in phase with the supply voltage either, as shown in Figure 3.10(a). After the rectifier leg and the neutral leg were turned on, the supply current became clean with a very low THD and was in phase with the supply voltage. The DC-bus voltage was regulated well around 800V and the neutral point was also maintained very well. The current i_C was maintained small, without a visible fundamental component.

After the two phase legs were turned on at 0.12 s, the supply current increased and

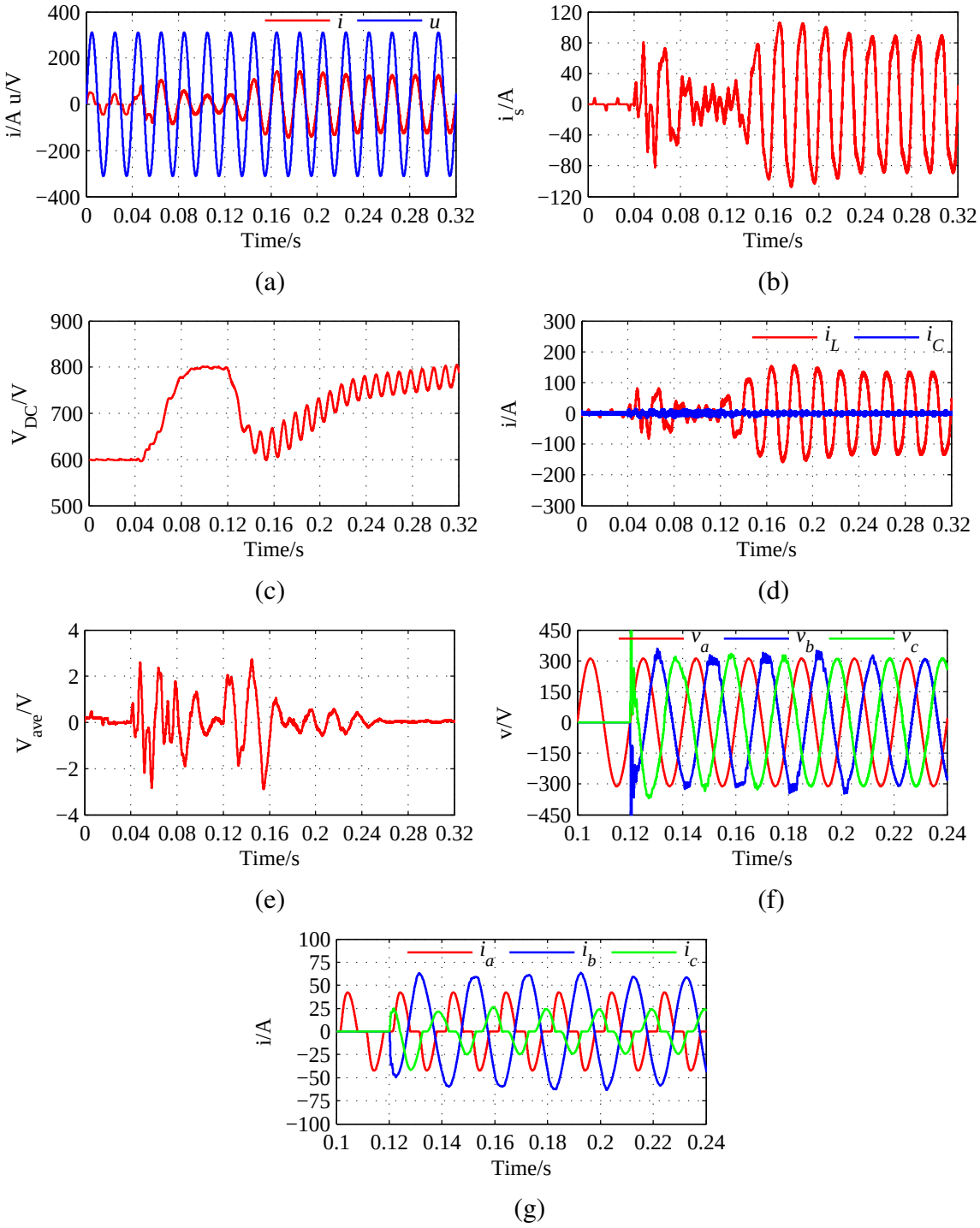


Figure 3.10: Simulations results for the case with non-linear unbalanced three-phase loads. (a) Supply current and voltage. (b) Current of the rectifier leg. (c) DC-bus voltage. (d) Inductor and capacitor currents of the neutral leg. (e) Shift of the neutral point voltage V_{ave}. (f) Three-phase voltages provided. (g) Three-phase load currents.

was still clean and in phase with the supply voltage, although the Phase *c* load was non-linear. The THD of the supply current was maintained below 1%. Because of the sudden connection of the loads on Phase *b* and Phase *c* and also the start of the two phase legs, the DC-bus voltage dropped but recovered within 7 cycles. The ripples in the DC-bus voltage became higher and the variation of the neutral point became bigger as well (but was still within ± 2 V), because of the more power exchanged with the load. The generated phase voltages quickly settled down with low THD (below 2.5%) and formed balanced three-phase voltages together with the supply voltage. The three-phase loads worked properly and independently.

3.5 Summary

In this chapter, a four-leg converter has been proposed on the basis of half-bridge rectifiers developed in Chapter 2 to provide an independent balanced three-phase power source from a single-phase supply. The three-phase voltages generated contain low voltage harmonics and the current drawn from the single-phase supply is clean and in phase with the supply voltage. A neutral leg is introduced to maintain a stable neutral point that is close to the mid-point of the DC-bus voltage, which is shared by the single-phase supply and the two phase voltages generated. The load of Phase *a* is directly fed by the single-phase supply so that two switches are reduced and the the converter only processes two thirds of the power. Because of the presence of a stable neutral point, the major functions for the converter can be implemented independently, which facilitates the controller design. In order to make sure that the current drawn from the supply is in phase with the supply voltage and the generated two phase voltages can form three-phase balanced voltages together with the supply, a synchronisation unit is needed. The generated voltage has the same level as the supply voltage so no transformer is needed for loads with the same rated voltage as the supply voltage. Simulation results have verified the performance of the proposed system.

Chapter 4

ρ-converters with Reduced Fundamental and Second-order Voltage Ripples

This chapter proposes an actively-controlled single-phase four-switch ρ-converter with considerably reduced low-frequency voltage ripples. In addition to the fundamental voltage ripple discussed in Chapters 2 and 3, the well-known second-order voltage ripple is considered here, which is another obstacle to further reduce capacitance required. In this chapter, the ρ-converter is operated in rectification mode while the inversion mode is discussed in Chapters 5 and 6. The proposed converter consists of one conventional rectification leg and one neutral leg linked with two capacitors that split the DC bus. The ripple energy in the converter is actively diverted into the lower split capacitor so that the voltage across the upper split capacitor, designed to be the DC output voltage, has very small ripples. The voltage across the lower capacitor is designed to have large ripples on purpose so that the total capacitance needed is significantly reduced and highly reliable film capacitors, instead of electrolytic capacitors, can be used. At the same time, the rectification leg is controlled independently from the neutral leg to regulate the input current to achieve unity power factor and also to maintain the DC-bus voltage. Experimental results are presented to validate the performance of the proposed strategy.

4.1 Introduction

More and more microgrids are now connected to the public grid and various loads through power converters (Zhong and Hornik, 2013b). For both AC and DC microgrids, single-phase converters are often needed when supplying DC loads. Such converters are expected to have high power density, high efficiency, high reliability and low costs. There are numerous topologies in the literature, aiming to have improved performance from these three aspects. Moreover, with the integration of renewable energy sources into the power grid, there is a trend to have bidirectional single-phase power converter as an interface between power grid and energy sources (Zhong and Hornik, 2013b; Dong et al., 2012a;b). As a result, the study of single-phase converters has attracted more and more attention.

Conventionally, bulky electrolytic capacitors are required for single-phase converters to produce smooth DC-bus voltage, due to the pulsating input power. However, the volume and weight of bulky electrolytic capacitors could be a serious problem for volume-critical and/or weight-critical applications, such as electrical vehicles (Wen et al., 2012) and aircraft power systems (Wang et al., 2011). What is worse is that electrolytic capacitors, known to have limited lifetime, are one of the most vulnerable components in power electronic systems (Stevens et al., 2002; Han and Narendran, 2011; Krein et al., 2012). As a result, in order to enhance the reliability of power electronic systems, it is highly desirable to minimise the usage of electrolytic capacitors and use highly-reliable small capacitors like film capacitors if possible, while maintaining low voltage ripples.

In general, the reduction of electrolytic capacitors can be achieved in four approaches. One approach is to inject harmonic currents to suppress fluctuations of input energy by changing control strategies for existing power switches in converters. In (Yao et al., 2012), it was proposed to reduce the DC-bus capacitor by injecting third harmonic component to the grid current. This approach benefits from fewer switches and easier implementation, which lead to lower system costs compared to other solutions. The second approach is to add an active energy storage compensator in parallel with DC-bus capacitors to bypass ripple energy that originally flows into DC-bus capacitors (Wang et al., 2011; Garcia et al., 2003; Zhang et al., 2013b; Zhong et al., 2012b; Wang et al., 2012; Pini and Barbi, 2011; Dusmez and Khaligh, 2014; Tang et al., 2015). This has been extensively studied in the last few years. Normally, the added compensator is operated as buck/boost converters to

inject/absorb ripple currents from DC bus. The third approach is based on connecting an active compensator in series with the DC bus (Wang et al., 2014). The compensator basically behaves as a voltage source to offset voltage ripples. Due to the series connection, the compensator has lower voltage stress compared to parallel compensators. The last approach is to introduce a ripple port terminated with a capacitor, as reported in (Krein et al., 2012; Harb et al., 2013), to store the ripple power. Different from other solutions, an AC capacitor instead of a DC capacitor is used to handle ripple energy, which also reduces the voltage stress on the switches.

In this chapter, a 4-switch converter is proposed to significantly reduce the DC-bus capacitance in the widely-adopted asymmetrical single-phase systems, where the midpoint of the AC side is not available. The converter only uses four switches, which is similar to a conventional bridge PWM converter, but the switches are formed as a rectification leg and a neutral leg and operated differently from a conventional full-bridge converter. The rectification leg is operated as a half-bridge converter to regulate the DC-bus voltage via controlling the grid current to make it clean and in phase with the grid voltage to achieve unity power factor. The neutral leg, consisting of two active switches, two split capacitors and one inductor, maintains a stable DC output voltage. The control of the two legs are independent from each other, which makes control design very flexible, and the corresponding control strategies can be designed according to their own objectives. Importantly, the neutral leg is able to actively divert the ripple energy from the upper split (output) capacitor to the lower split capacitor. As a result, the output voltage does not contain any low frequency ripples and hence, the upper split capacitor can be significantly reduced. Note that the voltage across the lower split capacitor is designed to have relatively large ripples on purpose because it is not supplied to any loads. Accordingly, the total usage of DC-bus capacitors could be reduced significantly so that it is now possible to use highly reliable film capacitors, instead of bulky electrolytic capacitors. This makes the converter very suitable for high-reliability applications. The selection criteria of the split capacitors are discussed with the aim to minimise their usage. This is mainly for systems without hold-up time requirement. For systems with hold-up requirement, the required capacitance needs to be large enough if no other means is applied to provide the energy required (Wang et al., 2014).

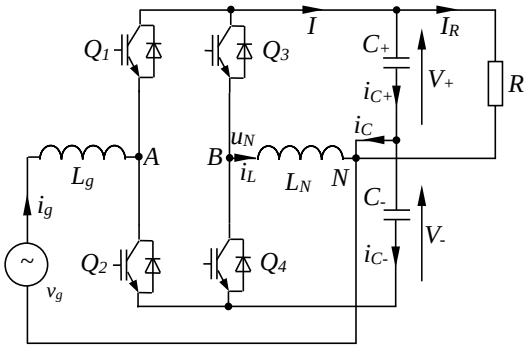


Figure 4.1: The single-phase converter under investigation.

The rest of the chapter is organised as follows. Section 4.2 introduces the converter under investigation. In Section 4.3, how to significantly reduce DC-bus capacitors is discussed and, in Section 4.4, the associated control strategies are developed. In order to achieve the minimal capacitance, the selection criteria of the split capacitors are then discussed in Section 4.5 and the impact of the different voltages across the split capacitors are analysed in Section 4.6. Experimental results are provided in Section 4.7 with an efficiency comparison made in Section 4.8 and the summary is made in Section 4.9.

4.2 The Single-phase Converter under Investigation

The converter proposed in the preliminary version of this chapter (Ming and Zhong, 2014) is investigated further in this chapter. It consists of one rectification leg and one neutral leg, as shown in Figure 4.1. The converter can be formed by adding two active switches into a conventional half-bridge PWM converter by putting a neutral leg consisting of two switches across the DC bus with their midpoint connected to the midpoint of the split capacitors through an inductor. The neutral leg is actually a typical DC/DC converter, which has been widely adopted in industry. In particular, the neutral leg has been applied to three-phase four-wire power inverters as reported in (Zhong and Hornik, 2013b; Zhong et al., 2002; Hornik and Zhong, 2013; Liang et al., 2009). According to the analysis made in (Zhong and Hornik, 2013b), the neutral leg is a stable system although the inductor is coupled with the split capacitors.

It is well known that bulky electrolytic capacitors are often needed for single-phase converters to smooth the second-order voltage ripples on the DC bus. However, the reliability,

volume and weight of electrolytic capacitors could be a serious problem for high-reliability, volume-critical and weight-critical applications (Stevens et al., 2002; Han and Narendran, 2011; Krein et al., 2012). As a result, in order to enhance the reliability and power density of converters, it is highly desirable to reduce the usage of capacitors so that highly-reliable capacitors like film capacitors could be used to replace electrolytic capacitors. However, for conventional single-phase converters, there exists a trade-off between reducing required capacitors and reducing the output voltage ripples because single-phase full-bridge converters have only one DC voltage, which is used as both the DC output and the only ripple energy buffer on the DC bus. In light of this, a lot of auxiliary circuits are proposed to construct another DC or AC voltage to store the voltage ripples, which can be connected in parallel or in series at the AC or DC sides (Wang et al., 2011; Krein et al., 2012; Wang et al., 2012; Wang and Blaabjerg, 2014; Gu et al., 2009).

For the topology shown in Figure 4.1, there are two DC voltages because of the split capacitors. This provides a possible way to operate the converters to make one of the voltages as the output voltage to supply loads and to make the other voltage as the ripple energy buffer. The total capacitance could be significantly reduced because the ripple energy is diverted from the output capacitor to the other capacitor, which could have high voltage ripples. By diverting all the ripple power to the lower capacitor C_-, the output voltage V_+ can become ripple free, which means the output capacitance C_+ can be reduced a lot because it does not need to process any low frequency ripple energy. Importantly, the capacitor C_- can also be significantly reduced because its voltage is not supplied to any loads so it can be designed to have large ripples on purpose. Accordingly, both capacitors can be significantly reduced and replaced with highly-reliable film capacitors. This improves the system power density and reliability and reduces system weight and volume. Although costly film capacitors are used to replace electrolytic capacitors, the cost arising from capacitors could still be reduced because the total capacitance required is considerably reduced.

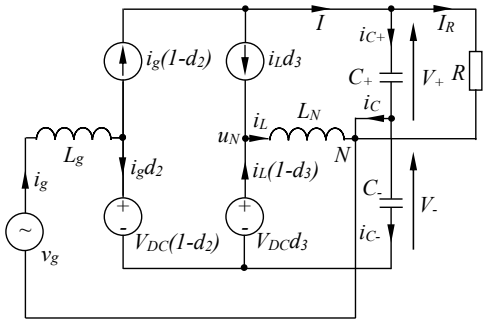


Figure 4.2: The average circuit model of the converter shown in Figure 4.1.

4.3 Reduction of the Bulky DC-bus Capacitors

In order to clearly show how to significantly reduce the DC-bus capacitors, there is a need to analyse the relationship between the ripple energy and the required capacitors for the investigated converter. For this purpose, an average circuit model is built up at first.

4.3.1 Circuit Analysis

It is assumed that the DC-bus voltage of the converter is

$$V_{DC} = V_+ + V_- \tag{4.1}$$

where V_+ and V_- are the voltages across the split capacitors C_+ and C_- with respect to the neutral point N and the negative point of the DC bus, respectively. Suppose that the grid current is

$$i_g = I_g \sin \omega t \tag{4.2}$$

and the grid voltage is

$$v_g = V_g \sin \omega t \tag{4.3}$$

in which V_g and I_g are the peak values of the grid voltage and current, respectively, and ω is the angular line frequency. Note that the grid voltage and current are supposed to be in phase in order to achieve unity power factor, and i_g is a pure AC current without a DC component.

Because the switches are operated at a frequency much higher than the fundamental frequency, the averaged variables, e.g. average currents and average voltages, can be adopted to well represent the original variables according to the averaging theory (Khalil, 2001) so that the circuit can be analysed by using the average circuit model (Srinivasan and Oruganti, 1998; Tymerski et al., 1989). The average circuit model of the rectification leg can be built following the procedures developed in (Srinivasan and Oruganti, 1998). The switches Q_1 and Q_2 are replaced with a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, where d_2 is the duty cycle of Q_2, as shown in Figure 4.2. Similarly, the average circuit model of the neutral leg can be obtained as shown in Figure 4.2, where d_3 is the duty cycle of Switch Q_3. Note that, in this chapter, the split capacitors are not necessarily the same, unlike the case in (Srinivasan and Oruganti, 1998; Lo et al., 2002; 2007), so the model in this chapter is more generic. Also note that in order to facilitate the exposition in the sequel, the duty cycle of the lower switch of the rectification leg (Q_2) and the duty cycle of the upper switch of the neutral leg (Q_3) are adopted in the model.

According to the average circuit model of the converter shown in Figure 4.2, the capacitor currents can be found as

$$i_{C+} = i_g(1-d_2) - I_R - i_L d_3 \tag{4.4}$$

$$i_{C-} = -i_g d_2 + i_L(1-d_3) \tag{4.5}$$

and the neutral current i_L can be found as

$$i_L = i_{C-} - i_{C+} + i_g - I_R. \tag{4.6}$$

In order to obtain the unity power factor, the two switches Q_1 and Q_2 can be operated complementarily to track the reference of the grid current, which is in phase with the grid voltage. Since the switching frequency is much higher than the line frequency, the duty cycle of Switch Q_2 can be calculated in the average sense as

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t \tag{4.7}$$

to maintain the DC-bus voltage V_{DC}, according to (Srinivasan and Oruganti, 1998; Lo et al., 2007). Normally, Switches Q_3 and Q_4 are operated complementarily to split the DC-bus

voltage V_{DC} into V_+ and V_- (Zhong and Hornik, 2013b; Hornik and Zhong, 2013; 2011b; Zhong et al., 2005). The duty cycle of Switch Q_3 can be calculated as

$$d_3 = \frac{V_-}{V_{DC}} \tag{4.8}$$

because the neutral leg is operated as a DC/DC buck converter. Because of the power balance between the AC and DC sides (ignoring the power losses), there is

$$\frac{V_g I_g}{2} = \frac{V_+^2}{R} \tag{4.9}$$

and the load current is

$$I_R = \frac{V_g I_g}{2V_+},$$

which is also the DC component of current I. (4.4) can then be re-written as

$$\begin{aligned} i_{C+} &= I_g \sin\omega t(\frac{V_-}{V_{DC}} + \frac{V_g}{V_{DC}}\sin\omega t) - \frac{V_g I_g}{2V_+} - \frac{V_-}{V_{DC}} i_L \\ &= \frac{V_-}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t \\ &\quad -\frac{V_g I_g V_-}{2V_+ V_{DC}} - \frac{V_-}{V_{DC}} i_L. \end{aligned} \tag{4.10}$$

Similarly, (4.5) can be re-written as

$$\begin{aligned} i_{C-} &= -I_g \sin\omega t(\frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t) + i_L(1 - \frac{V_-}{V_{DC}}) \\ &= -\frac{V_+}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t \\ &\quad +\frac{V_g I_g}{2V_{DC}} + \frac{V_+}{V_{DC}} i_L. \end{aligned} \tag{4.11}$$

As is well known, no DC currents could pass through capacitors. As a result, i_L should have a DC component so that i_{C+} and i_{C-} do not have any DC component. It can be found out from (4.10) and (4.11) that the DC component of i_L is $-I_R = -\frac{V_g I_g}{2V_+}$, i.e., the same value as the load current.

If the neutral current i_L is controlled to provide the DC component only, that is,

$$i_L = -I_R,$$

then the capacitor currents are

$$i_{C+} = \frac{V_-}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}} \cos 2\omega t$$

and

$$i_{C-} = -\frac{V_+}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}} \cos 2\omega t.$$

In addition to the same second-order ripple current $-\frac{V_g I_g}{2V_{DC}} \cos 2\omega t$ flowing through the split capacitors, the grid current i_g is split between i_{C+} and i_{C-} because in this case

$$i_{C+} + (-i_{C-}) = i_g,$$

which could lead to high voltage ripples and hence bulky electrolytic capacitors are needed. In order to reduce the voltage ripples, the current flowing through the capacitors should be regulated differently. For this reason, a different control strategy is proposed in the next subsection.

4.3.2 Reduction of DC-bus Capacitance

The idea is to push the current components of i_{C+} in (4.10) through the neutral leg instead of through the upper split capacitor so that i_{C+} does not contain any fundamental or second order ripple currents. That is to make $i_{C+} = 0$, ignoring the switching ripples. Hence, according to (4.10), the current i_L should be controlled to satisfy

$$i_L = i_g - \frac{V_g I_g}{2V_-} \cos 2\omega t - \frac{V_g I_g}{2V_+}. \tag{4.12}$$

On the other hand, i_L should also satisfy (4.6). Hence, in this case, the current flowing through the lower split capacitor should be

$$i_{C-} = -\frac{V_g I_g}{2V_-} \cos 2\omega t. \tag{4.13}$$

In other words, it only contains the second-order harmonic component or the second-order component only flows through the lower split capacitor. As a result, all the voltage ripples are then diverted to the lower capacitor C_-, which would increase the voltage ripples on C_-. However, this does not matter because there is no load connected to V_- and the voltage

V_- can tolerate a much higher ripple voltage. Hence, only a small C_- is needed. Since the upper capacitor C_+ does not contain any fundamental and second-order ripple voltage components any more, it can be reduced a lot while maintaining low voltage ripples. As a result, both capacitors C_+ and C_- can be very small, which makes it possible to replace the required bulky electrolytic capacitors with film capacitors.

4.4 Control Design

4.4.1 Control of the Neutral Leg

The neutral leg should be controlled to maintain the output voltage V_+, to remove the ripple components in i_{C+} and also to remove the fundamental component in i_{C-}.

4.4.1.1 Regulation of the output voltage V_+

Maintaining a stable output voltage V_+ with very small ripples at the desired output reference voltage V_+^* is a major target. The regulation of the sum of the voltages V_+ and V_-, i.e. the DC-bus voltage V_{DC}, is the task of the rectification leg and will be discussed in the next subsection. The neutral leg is responsible for splitting the DC-bus voltage into V_+ and V_-, which are independent from each other. Since the voltage V_+ is used as the output voltage, it can be directly controlled by forming a voltage loop and then the voltage V_- can be indirectly controlled by regulating the DC-bus voltage.

In order to regulate the output voltage V_+, it is measured and put through the hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts}, \tag{4.14}$$

where T is the fundamental period of the grid voltage, to extract its DC component, as shown in Figure 4.3. A simple proportional-integral (PI) controller is then applied to regulate the voltage. The output of the PI controller can be converted to PWM signals to drive the switches. The parameters for the PI controller can be selected according to classical design methods for a second-order system, with the characteristic equation given by

$$s^2 + \frac{K_p}{C_+}s + \frac{K_i}{C_+} = 0,$$

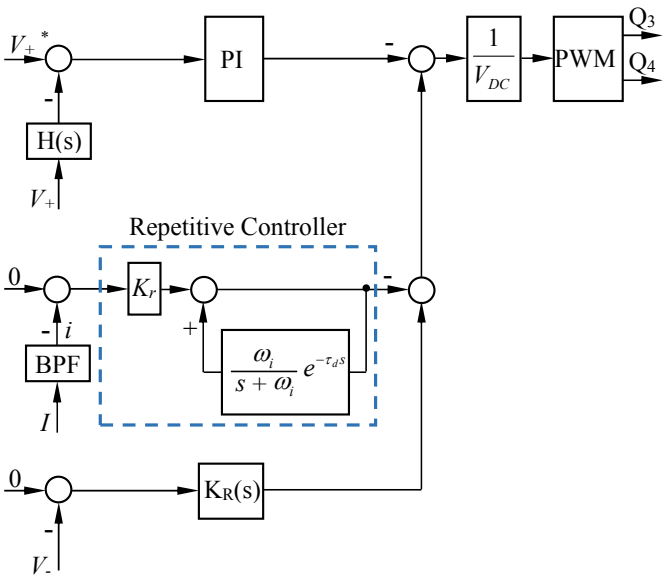


Figure 4.3: Controller for the neutral leg.

where K_p and K_i are the gains of the PI controller. These parameters can be chosen to obtain the damping coefficient of

$$\frac{K_p}{2}\sqrt{\frac{1}{C_+ K_i}} = \frac{1}{\sqrt{2}}.$$

As a result,

$$K_p^2 = 2C_+ K_i. \tag{4.15}$$

The relationship between K_p and K_i is mostly related to the capacitor C_+. In practice, K_p or K_i can be initially set to small values, which approximately satisfy (4.15), and then gradually be increased to achieve the desired performance. In this way, both parameters can be well tuned.

4.4.1.2 Removal of the ripple components in i_{C+}

As discussed before, the capacitor current i_{C+} should be maintained around zero in order to smooth the ripples of the output voltage V_+. Note that C_+ is now very small so the ripple current may flow through the DC load and it is more effective to minimize the ripple component i in the DC-bus current I. As a result, instead of controlling i_{C+}, the strategy to minimize the DC-bus ripple current i is adopted in this chapter. In order to ex-

tract this second-order ripple component, a band pass filter (BPF) is adopted, via adding a resistor–capacitor circuit on the path of the measured I to filter out the switching ripples at first and then using a digital high pass filter $\frac{s}{s+10}$ to remove the DC component. The used resistor and capacitor are 10 kΩ and 0.01 μF. As a result, the transfer function of the BPF is $\frac{10000s}{(s+10)(s+10000)}$. The cut-off frequencies of the BPF are 1.59 Hz on the lower side and 1591 Hz on the higher side so the bandwidth of the BPF is 1589 Hz.

Several possible controllers, e.g. hysteresis controllers with a variable switching frequency and repetitive controllers with a fixed switching frequency, can be applied to minimise the ripple current i. In order to reduce the stress on the switches, a repetitive controller is applied in this chapter as shown in the dashed box of Figure 4.3. Another benefit of the repetitive controller is its high performance to handle harmonics (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a). The repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where τ_d is designed based on the analysis in (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a) as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\text{s}$$

with $\omega_i = 2550$, $\tau = 0.02\,\text{s}$.

Note that the regulation of V_+ deals with the DC component but the removal of the ripple components of i_{C+} deals with non-DC components. Hence, the output of the repetitive controller can be added to the output of the PI controller for V_+ to generate the PWM signals for the switches Q_3 and Q_4, as shown in Figure 4.3. Note that the "$-$" sign at the output of the controllers is because the duty cycle controlled is d_3 instead of d_4, which is $1 - d_3$.

In general, the adoption of the BPF does not lead to any resonance of the controllers with the converter. This is mainly due to the fact that the BPF behaves as a low-pass filter at high frequencies and is cascaded with the repetitive controller, which again is a low-pass filter.

4.4.1.3 Removal of fundamental component in i_{C-}

The control of the DC-bus ripple current i to 0 leads to the fact that the ripples are now diverted to the lower capacitor C_-. In this case, the current of the capacitor C_- is expected to only have a second-order component. However, according to (4.6), when $i = 0$, there is

$$i_g = i_L - i_{C-} + I_R,$$

which means that the grid current i_g could flow through the inductor L_N and the capacitor C_- if not controlled properly. Hence, there is a need to make sure that no fundamental component flows through the capacitor C_- otherwise it would lead to increased voltage ripples without providing any benefits.

This can be achieved by forcing the fundamental component of V_- to be zero, as shown in Figure 4.3. The following resonant controller

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}, \tag{4.16}$$

with $\xi = 0.01$, $h = 1$, and $\omega = 2\pi f$, can be adopted. The output of the resonant controller is then added onto the outputs of the other two controllers before sending to the PWM conversion block, as shown in Figure 4.3. The gain K_h of the resonant controller can be selected by fine tuning through trial-and-error in practice; it is chosen as $K_h = 10$ for the experimental system to be tested. In general, a large gain should improve the performance of the control but may lead to a large charging current when starting up the system that might trigger the current protection and also may introduce noticeable disturbance into the current controller. These should be avoided. Note that the output of this controller is "+" because the voltage under control relates to V_-.

4.4.2 Control of the Rectification Leg

The control of the rectification leg is very similar to that of conventional half-bridge converters, which is mainly used to regulate the grid current and to control the whole DC-bus voltage. To be more precise, the grid current is expected to be in phase with the grid voltage and also to be clean with low harmonics. For this purpose, the grid current i_g should be measured as a feedback to form a current tracking controller. Here, the repetitive control-

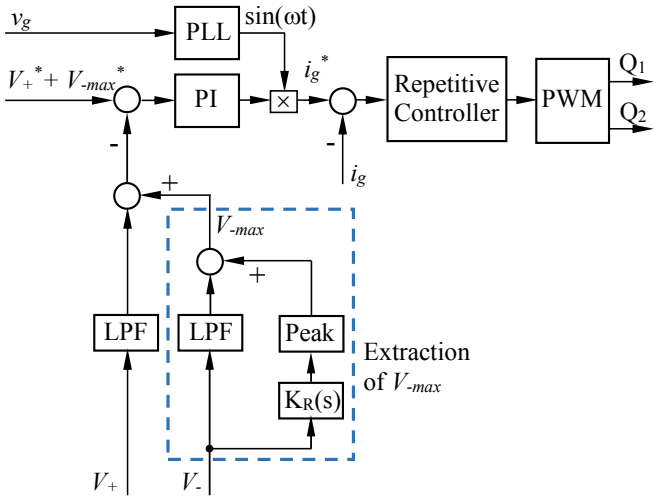


Figure 4.4: Controller for the rectification leg.

ler shown in the dashed box of Figure 4.3 is adopted again. In order to generate the grid current reference i_g^*, an outer-loop voltage controller can be constructed.

There can be different ways to construct this voltage controller; see e.g. (Cao et al., 2015). In this chapter, the voltage controller is designed to maintain the maximum voltage V_{-max} of V_- constant. Hence, the total DC-bus voltage is maintained at $V_+^* + V_{-max}^*$, with a PI controller. The output of the controller can be used as the peak value of the grid current reference i_g^*, as shown in Figure 4.4. This is multiplied with the phase signal of the grid voltage, which can be obtained from a phase-locked-loop, to form the grid current reference i_g^*. As a result, the grid current is in phase with the grid voltage to achieve the unity power factor. Here, the phase-locked-loop proposed in (Ziarani and Konrad, 2004) is adopted.

The above-mentioned control strategy of the half-bridge rectification leg is now somewhat standard (Srinivasan and Oruganti, 1998; Lo et al., 2002; 2007; Lin and Hung, 2002). What is different here is that the maximum DC-bus voltage, instead of the average DC-bus voltage, is selected as the controlled output. As a result, the objective here is set to control the maximum DC-bus voltage. For this purpose, the maximum DC-bus voltage should be extracted at first. Since the voltage V_+ is controlled to be more or less pure DC without second-order components, it is only required to extract the maximum value of the voltage V_-, which can be obtained by adding the DC component with the peak voltage of the ripple component, as shown in Figure 4.4. The hold filter (4.14) is again used to obtain the DC component. In order to extract the second-order component, the resonant filter (4.16) is

again adopted with $\xi = 0.01$, $h = 2$, and $\omega = 2\pi f$. A Peak block in Figure 4.4 is used to calculate the peak value of the ripple component. The sum of the average voltage and the peak voltage of the ripple component then forms the maximum voltage of the voltage V_-, which is denoted as V_{-max} in Figure 4.4 and is added with V_+ to obtain the maximum DC-bus voltage for feedback.

4.4.3 Stability of the System

Because of the decoupled nature of the controllers for the two legs, the stability of the system can be easily guaranteed. The controller for the rectification leg has a very typical structure, which is very mature and widely used in industry. The controller for the neutral leg has a very special structure with one current loop and two voltage loops. What is special is that these three loops are in parallel rather than cascaded so the stability of each loop can be treated individually. The current loop is designed to regulate the AC components of i_{C_+} (or i) to be around zero, i.e., to remove any non-DC components in i. At the same time, the voltage loop related to V_+ is to maintain the DC component of the voltage V_+ while the voltage loop related to V_- is designed to reduce the fundamental component of voltage V_-. Hence, the functions of the three loops are decoupled in the frequency domain for current or voltage. The three loops consist of simple PI, repetitive and resonant controllers, which have been widely analysed in the literature. See, for example, (Zhong and Hornik, 2013b). Hence, detailed analysis of the stability of the loops is not repeated in this chapter.

4.5 Selection of Components

4.5.1 Selection of Capacitor C_-

As demonstrated in (Yao et al., 2012; Gu et al., 2009), the total ripple energy stored in the split capacitors over a charging period for single-phase converters with the unity power factor is

$$E_r = \frac{V_g I_g}{2\omega}.$$

With the proposed strategy, all the ripple energy is now stored on the lower capacitor C_- instead of both capacitors C_+ and C_-. Hence,

$$C_- = \frac{2E_r}{V_{-max}^2 - V_{-min}^2} \tag{4.17}$$

where V_{-max} and V_{-min} are the maximum and minimum voltages of V_-, respectively. A small capacitor means that high V_{-max} and/or low V_{-min} is needed. However, in order to ensure the proper boost operation of the converter,

$$V_- \geqslant V_g |\sin \omega t| \tag{4.18}$$

should be satisfied. In other words,

$$V_{-min} \geqslant V_g. \tag{4.19}$$

At the same time, V_{-max} has an upper bound as well because of the limit on the devices and/or the applications. Hence, the capacitor is mainly limited by the allowed maximum voltage V_{-amax} and the required minimum capacitance C_{-min} is

$$C_- = \frac{V_g I_g}{\omega(V_{-amax}^2 - V_{-min}^2)}, \tag{4.20}$$

which can be small if V_{-amax} is high enough.

In addition, another important factor for selecting capacitors is the maximum allowable ripple currents (Wen et al., 2012; Han and Narendran, 2011; Makdessi et al., 2015). This is very important for the reliability of capacitors. In general, large current ripples lead to short lifetime. The current ripples are closely related to the voltage ripples and the equivalent impedance of capacitors. In order to evaluate the level of voltage ripples, (4.20) can be rewritten as

$$\begin{aligned} C_- &= \frac{V_g I_g}{\omega \triangle V_- (V_{-max} + V_{-min})} \\ &= \frac{V_g I_g}{2\omega \triangle V_- V_{-ave}} \end{aligned} \tag{4.21}$$

where $\triangle V_- = V_{-max} - V_{-min}$ and $V_{-ave} = \frac{V_{-max}+V_{-min}}{2}$ are the peak-peak ripple voltage and

the average voltage of V_-, respectively. Since the capacitor impedance at the second-order frequency is $\frac{1}{2\omega C_-}$, the peak-peak value $\triangle i_{C-}$ of the second-order ripple current flowing through C_- is

$$\triangle i_{C-} = \frac{\triangle V_-}{\frac{1}{2\omega C_-}} = 2\omega C_- \triangle V_-. \tag{4.22}$$

Substitute (4.21) into (4.22), then there is

$$\triangle i_{C-} = \frac{V_g I_g}{V_{-ave}}. \tag{4.23}$$

This is consistent with (4.13). The average voltage should be increased in order to reduce the ripple current. For the proposed strategy, the voltage V_- can be different or the same as V_+. As a result, the voltage V_{-ave} can be maintained at a higher value in order to reduce the ripple current. This can be naturally achieved when the maximum voltage V_{-max} is controlled at the allowable value because the higher the maximum voltage is, the higher the average voltage V_{-ave} is.

Of course, some other factors such as hold-up time requirement (Wang et al., 2014), current stress and limited voltage rating of the capacitors and switches, should be taken into account when selecting capacitors. If the maximum voltage of the capacitor is determined, then increased capacitance means increased hold-up time and reduced current stress, which is preferred in practical applications. As a result, there are several trade-offs when selecting capacitors for a certain application.

4.5.2 Selection of Inductor L_N

The fast switching of the neutral leg leads to switching ripples over the current flowing through the inductor L_N. Since the two switches Q_3 and Q_4 are operated complementarily, the on time of Q_3 is $\frac{d_3}{f_s}$ and the on time of Q_4 is $\frac{1-d_3}{f_s}$ in one PWM period. Since the switching frequency is much higher than the line frequency, it can be assumed that the current increased $\frac{V_+ d_3}{L_N f_s}$ (to withstand the positive voltage V_+) and the current decreased $\frac{V_-(1-d_3)}{L_N f_s}$ (to withstand the negative voltage V_-) in these two modes are the same. According to (4.8), the maximum peak-peak current ripple $\triangle i_{Lm}$ on the inductor L_N is reached when the duty cycle d_3 reaches the maximum, which is when the voltage V_- reaches the maximum. That

is,

$$\triangle i_{Lm} = \frac{V_+ d_{3max}}{L_N f_s} = \frac{V_+ V_{-max}}{L_N f_s (V_+ + V_{-max})}. \tag{4.24}$$

For the given maximum allowed ripple current $\triangle i_{Lm}$, the minimum inductance is

$$L_{Nmin} = \frac{V_+ V_{-max}}{\triangle i_{Lm} f_s (V_+ + V_{-max})}. \tag{4.25}$$

The inductance can be reduced if the switching frequency f_s is increased. When choosing the magnetic core for the inductor, the DC current component in i_L should be taken into consideration to avoid saturation.

Note that increasing V_{-max} helps reduce the capacitor C_- but it leads to increased inductance L_N so there is a trade-off between these two. One possible option to break this trade-off is to reduce C_- by increasing V_{-max} but decrease L_N by increasing f_s.

4.5.3 Selection of Capacitor C_+

When Q_3 is turned on, C_+ is discharged through L_N and the maximum ripple current is given in (4.24). If the switching frequency of the converter is high and the inductance in series with the DC load is considered (Salcone and Bond, 2009), it is reasonable to assume that the switching ripple current mainly flows through the capacitor C_+. According to (Mohan, 2003), the peak-peak switching ripple voltage across the capacitor C_+ is

$$\begin{aligned} \triangle V_{+s} &= \frac{\triangle i_{Lm}}{8 C_+ f_s} + \triangle i_{Lm} R_{C+} \\ &= (\frac{1}{8 C_+ f_s} + R_{C+}) \frac{V_+ V_{-max}}{L_N f_s (V_+ + V_{-max})}, \end{aligned} \tag{4.26}$$

where R_{C+} is the equivalent series resistance (ESR) of the capacitor C_+. The second part, i.e. $\triangle i_{Lm} R_{C+}$, is caused by the ESR of the capacitor. Since R_{C+} is often negligible for film capacitors, (4.26) becomes

$$C_{+min} \approx \frac{\triangle i_{Lm}}{8 f_s \triangle V_{+sm}} \tag{4.27}$$

for the given maximum switching ripple voltage $\triangle V_{+sm}$ and the maximum ripple current $\triangle i_{Lm}$. Note that increasing the switching frequency reduces C_+.

Table 4.1: Parameters of the system

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
V_+^*	200 V
V_{-max}	750 V
R	220 Ω
C_+	5 μF
C_-	5 μF
L_N	2.2 mH
L_g	2.2 mH

4.5.4 Design Example

Here, an example is given for demonstration. The selected components, as summarised in Table 4.1, are also used when building up the test rig.

For the inductor L_N with $\triangle i_{Lm} = 4$ A, the required minimum inductance is $L_N \approx 2.1$ mH, according to (4.25). In this study, 2.2 mH is used. Note that the inductor can be reduced a lot if the switching frequency f_s is significantly increased, again according to (4.25).

Based on (4.20), the required minimum capacitance is $C_{-min} = \frac{V_g I_g}{\omega(V_{-max}^2 - V_{-min}^2)} \approx 2.76\,\mu$F. Here, $I_g = 3$ A is used in the calculation, considering the losses of the converter. In order to leave some margin, the capacitor C_- is selected as $5\,\mu$F. According to (4.23), the maximum second-order ripple current is $\triangle i_{C-max} = \frac{V_g I_g}{V_{-ave}} = \frac{V_g I_g}{(V_{-max}+V_g)/2} \approx 1$ A. The capacitor C_- can then be selected based on C_{-min} and $\triangle i_{C-max}$.

For the selection of the capacitor C_+, according to (4.27), if the maximum switching ripple voltage $\triangle V_{+sm}$ is expected to be around 5 V, then $C_{+min} \approx 5$ μF.

If a conventional single-phase full-bridge converter is adopted, then the DC-bus capacitor should be larger than $\frac{V_g I_g}{2\omega \triangle V_- V_{-ave}} \approx 740$ μF in order for the output ripple voltage to be maintained lower than 5 V. For capacitors at this level, electrolytic capacitors are often needed. The experimental results presented later show that the converter under investigation can achieve 5 V output ripple voltage only with two 5 μF film capacitors. This means the DC-bus capacitors can be reduced by over 70 times while maintaining the same level of output voltage ripples.

4.6 Impact of Different Voltages V_+ and V_-

The voltages across the two split capacitors are normally maintained to be the same in similar topologies. However, as mentioned above, the voltages are controlled to be different on purpose for the proposed strategy, which contributes to suppressing the voltage ripples and reducing the required capacitors. One question that arises naturally is whether the voltage difference would cause any problem to the control of the rectification leg and the neutral leg. This is analysed in this section.

4.6.1 Impact on the Rectification Leg

The main objective of the rectification leg is to maintain the grid current to be clean and to be in phase with the grid voltage. As stated previously, the control of the rectification leg and the neutral leg are independent from each other. As a result, the regulation of the input current only depends on the rectification leg instead of both legs. According to (4.7), the maximum and minimum values of the duty cycle of the two switches in the rectification leg are

$$\begin{aligned} d_{2max} &= \frac{1}{V_{DC}}(V_+ + V_g) \\ d_{2min} &= \frac{1}{V_{DC}}(V_+ - V_g). \end{aligned}$$

Since V_+, $V_- > V_g$, then $d_{2min} > 0$ and $d_{2max} < 1$ can be achieved for any combinations of V_+ and V_-. According to the average model, the duty cycle of the switch Q_2 is

$$\begin{aligned} d_2 &= \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t \\ &= \frac{1}{V_+ + V_-}(V_+ - V_g \sin \omega t) \end{aligned} \tag{4.28}$$

If all the ripple power is provided by the lower capacitor, then (4.28) becomes

$$d_2 = \frac{1}{V_+ + \sqrt{V_{-min}^2 + \frac{P_o}{C_-}(1 - \sin 2\omega t)}}(V_+ - V_g \sin \omega t)$$

where the derivation of V_- can be found in (Gu et al., 2009) for a given load power P_o. It is clear that the obtained duty cycle contains a second-order ripple component coming from

V_-. The existence of a second-order ripple component is common for all converters based on the half-bridge structure and does not constitute any problem because the switching frequency is much higher than the second-order frequency. The only difference here is that the ripples are stored in the lower capacitor only.

Because the rectification leg is independently controlled, the input power factor and the THD of the input current can be regulated as usual and are not affected by the difference between V_+ and V_-. As a result, the regulation of the input current is not affected by the voltage difference between V_+ and V_-.

4.6.2 Impact on the Neutral Leg

The neutral leg is used for two purposes, i.e. splitting the DC-bus voltage to V_+ and V_- and diverting the ripple power to the lower capacitor C_-. According to the average model, the duty cycle of the switch Q_3 can be given as

$$\begin{aligned} d_3 &= 1 - \frac{V_+}{V_{DC}} \\ &= 1 - \frac{V_+}{V_+ + \sqrt{V_{-min}^2 + \frac{P_o}{\omega C_-}(1 - \sin 2\omega t)}}, \end{aligned}$$

which is also affected by a second-order ripple component. As long as $V_- < V_{DC}$, which is always true because $V_{DC} = V_+ + V_- > V_+, V_-$, the duty cycle d_3 can be always achieved by controlling the two switches Q_3 and Q_4 in an complementary way. Hence, the voltage difference does not cause any problem to the control of the neutral leg either.

4.6.3 Impact on the Current Stress of the Switches

The voltage difference may lead to different current stresses to the switches. The average currents are very important when selecting a switch or a diode (Srinivasan and Oruganti, 1998). As a result, they are calculated here in order for selecting suitable switches and diodes for both legs.

4.6.3.1 Switches and diodes of the rectification leg

For the rectification leg, there are two switches and two diodes in total. The current flowing through the rectification leg mainly depends on the grid current i_g. The positive cycle of the grid current i_g flows through the Switch Q_2 and the corresponding free-wheeling diode is D_1. On the other hand, the negative cycle of the grid current i_g flows through the Switch Q_1 and the corresponding free-wheeling diode is D_2. As demonstrated in (Srinivasan and Oruganti, 1998), the average currents flowing through active switches Q_1 and Q_2 and diodes D_1 and D_2 are

$$\begin{aligned} I_{Q_1} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g(1-d_2)dt = I_R(\frac{2V_-}{V_g\pi} - 0.5) \\ I_{Q_2} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g d_2 dt = I_R(\frac{2V_+}{V_g\pi} - 0.5) \\ I_{D_1} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g(1-d_2)dt = I_R(\frac{2V_-}{V_g\pi} + 0.5) \\ I_{D_2} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g d_2 dt = I_R(\frac{2V_+}{V_g\pi} + 0.5). \end{aligned} \tag{4.29}$$

It can be seen that most of the currents flow through the diodes rather than the active switches. More importantly, the currents of the active switches are different if $V_+ \neq V_-$. The same is true for the diode currents. For example, if $V_- > V_+$, which is preferred in order to reduce C_-, then $I_{Q_1} > I_{Q_2}$ and $I_{D_1} > I_{D_2}$. As a result, the power loss of the upper switch Q_1 is higher than that of the lower switch Q_2 if $V_- > V_+$. (4.29) can be used as a principle to select the active switches and diodes. Of course, the two voltages can be controlled to be the same. In this case, the average currents of the switches become the same and also, the average currents of the switches become the same too.

4.6.3.2 Switches and diodes of the neutral leg

For the neutral leg, there are also two switches and two diodes in total. The current flowing through the neutral leg mainly depends on the inductor current i_L. In order to analyse the average currents, similar analysis can be done. The only difference here is the conduction periods of Q_3, Q_4 and D_3, D_4. For example, the conduction period of Switch Q_1 in the rectification leg is from π to 2π, which is not affected by other factors like the input or output power. This is because the periods of the positive and negative cycles of the current

i_g are the same, which is π. However, it is obvious that those periods of the current i_L are not the same according to (4.12), which leads to the fact that the conduction periods of Q_3, Q_4 and D_3, D_4 are not the same. In order to calculate their average currents, there is a need to first know these periods. Let $i_L = 0$, then

$$I_g \sin \omega t - \frac{V_g I_g}{2V_-} \cos 2\omega t - \frac{V_g I_g}{2V_+} = 0,$$

or

$$\sin^2 \omega t + \frac{V_-}{V_g} \sin \omega t - \frac{1}{2} - \frac{V_-}{2V_+} = 0.$$

Hence,

$$\sin \omega t = -\frac{V_-}{2V_g} \pm \frac{1}{2} \sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}}.$$

Because of (4.19), the "$-$" sign is not valid. There are two solutions within $[0, \frac{\pi}{\omega}]$, which are

$$\begin{aligned} t_1 = &\quad \frac{1}{\omega} \arcsin\left(\frac{1}{2} \sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}} - \frac{V_-}{2V_g}\right), \\ t_2 = &\quad \frac{\pi}{\omega} - \frac{1}{\omega} \arcsin\left(\frac{1}{2} \sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}} - \frac{V_-}{2V_g}\right). \end{aligned}$$

As a result, the average currents flowing through active switches Q_3 and Q_4 and diodes D_3 and D_4 can be calculated from

$$\begin{aligned} I_{Q_3} &= \frac{1}{2\pi} \int_{t_1}^{t_2} i_L d_3 dt \\ I_{Q_4} &= \frac{1}{2\pi} \int_{t_2}^{t_1+2\pi} i_L (1 - d_3) dt \\ I_{D_3} &= \frac{1}{2\pi} \int_{t_2}^{t_1+2\pi} i_L d_3 dt \\ I_{D_4} &= \frac{1}{2\pi} \int_{t_1}^{t_2} i_L (1 - d_3) dt. \end{aligned} \tag{4.30}$$

The analytical solutions are complicated but, in principle, the currents I_{D_3} and I_{D_4} are again higher than the currents I_{Q_3} and I_{Q_4}. Moreover, because V_- is set higher than V_+, I_{Q_3} and I_{D_3} are higher than I_{Q_4} and I_{D_4}, respectively.

For certain applications with known system parameters, the average currents flowing

through the switches and diodes of both legs can be easily obtained based on the above analysis. Together with the voltage stress, i.e. the DC-bus voltage V_{DC}, suitable switches and diodes can be selected.

4.6.4 Impact on the Voltage Stress of the Switches

In order to choose suitable switches for both legs, the voltage stress of the switches is another factor to be considered.

Compared to the current stress of the switches, it is more straightforward to analyse the voltage stress of the switches. Regardless of other system parameters, the voltage stress of the switches is always the sum of the voltages V_+ and V_-. It is well known that low voltage stress generally leads to low costs and high efficiency. As a result, it is always hoped to maintain the voltage stress within a reasonable level. Either decreasing V_+ or V_- can help to reduce the voltage stress. The level of the voltage V_+ is determined by the requirement of the DC load and cannot be changed. However, the voltage V_- does have some freedom to be decreased. According to the discussion before, the proposed converter can still perform well to control the grid current and the DC output voltage as long as the minimum voltage of V_- is higher than the peak of the grid voltage. Hence, there is $V_{-min} = V_g$. Note that the ripple level of the output voltage V_+ is still very low even if $V_{-min} = V_g$. The only compromise here is the DC-bus capacitance. In order to meet a given maximum voltage stress V_{max}, the maximum voltage of V_- is then fixed, which is $V_{-max} = V_{max} - V_+$. It is clear that low voltage stress means low V_{-max}. Since both maximum and minimum values of the voltage V_- are fixed now, the minimum required capacitance can be obtained according to (4.20). The higher the voltage stress can be, the smaller the capacitance C_- can be. It is worth mentioning that high voltage stress leads to high switching loss, which decreases the efficiency. When large electrolytic capacitors are used, the voltage stress could be lower because V_{-max} could be reduced. In this case, the switching loss of the converter is lower. However, the loss caused by the ESR of the capacitors becomes higher because the required capacitance can be very large and electrolytic capacitors have to be used. The additional loss caused by the high voltage stress may have been well compensated by the reduction of the loss in capacitors.

4.6.5 Impact on Switching Ripples of the Grid Current

Since the switching frequency is much higher than the fundamental frequency, the average grid current over each switching period can be controlled to track its reference, which is a sinusoidal signal. Apart from controlling the average grid current, it is also desirable to maintain the switching ripple of the grid current under a certain level, in order not to introduce power pollution to the grid. According to (Srinivasan and Oruganti, 1998), the peak-peak switching ripple of the grid current can be given as

$$\begin{aligned} \triangle i_g &= \frac{\frac{V_-}{V_{DC}}V_{DC} + V_g \sin \omega t}{L_g f_s} d_2 \\ &= \frac{1}{L_g f_s V_{DC}}(V_+ V_- - V_g^2 \sin^2 \omega t) + \\ &\quad \frac{(V_+ - V_-)V_g}{L_g f_s V_{DC}} \sin \omega t. \end{aligned} \tag{4.31}$$

Apparently, increasing the inductor and/or increasing the switching frequency could reduce the switching current ripple. According to (4.31), the switching ripple current is related to almost all system parameters. Compared to most of the analysis in the literature, the only difference here is that the voltages V_+ and V_- are designed to be different on purpose. The first part of the switching ripple, i.e. $\frac{1}{L_g f_s}(\frac{V_+ V_-}{V_{DC}} - \frac{V_g^2}{V_{DC}} \sin^2 \omega t)$, is always positive in the positive and negative half cycles of the grid current. However, the second part, i.e. $\frac{(V_+ - V_-)V_g}{L_g f_s V_{DC}} \sin \omega t$, changes its sign during the positive and negative cycles of the grid current. For example, if $V_+ < V_-$, it is negative in the positive half cycle of the grid current but is positive in the negative half cycle of the grid current. The resulted effect is that the switching ripples of the grid current in the negative half cycle are larger than those in the positive half cycle. If $V_+ > V_-$, then the switching ripples of the grid current in the negative half cycle are smaller than those in the positive half cycle. However, the slightly different switching ripples does not constitute any noticeable problems to the grid. If needed, an LCL filter, instead of an inductor L_g, can be adopted so that the switching ripple currents can flow through the filter capacitor instead of the grid.

4.7 Experimental Results

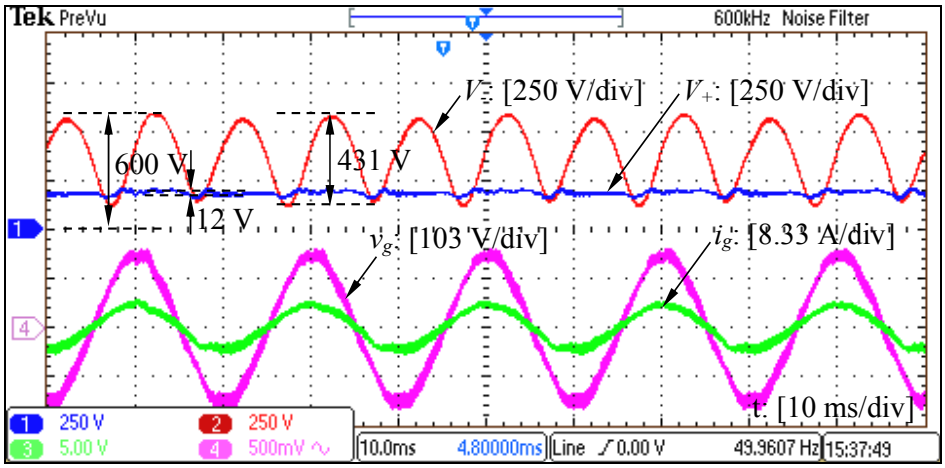
In order to validate the design and operation of the converter, experiments were conducted on a test rig in the lab. The test system consists of the investigated converter and its control circuit, which was constructed based on TMS320F28335 DSP. The main parameters of the test system are the same as the ones in the design example of Section 4.5 as summarised in Table 4.1. The system parameters like the inductor L_g and the switching frequency are selected according to the test rig and the available components in the lab and hence are not optimized for performance. Note that the two split capacitors are very small (5 μF), which demonstrates the capability of significantly reducing capacitors while maintaining low ripples on the DC output voltage. The required usage of capacitors is reduced by over 70 times from 740 μF to 10 μF. Here, two 5 μF metallized polypropylene film capacitors (MKP1848C55012JK2) are used as the two split capacitors in experiments. The system responses both in the steady state and during transient period are presented.

4.7.1 Steady-state Performance

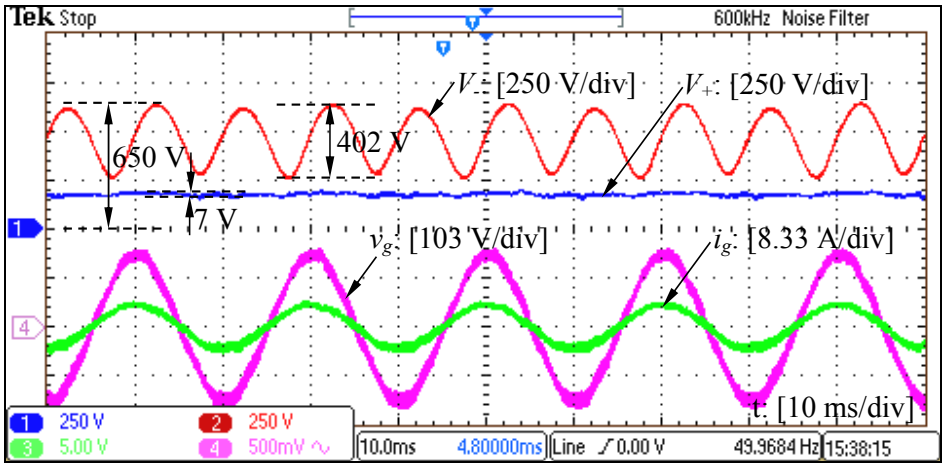
4.7.1.1 The grid current i_g and the DC voltages V_+ and V_-

The system steady-state performance with $V_+^* = 200$ V is given in Figure 4.5(a)-(d) for $V_{-max}^* = 600$, $V_{-max}^* = 650$, $V_{-max}^* = 700$ and $V_{-max}^* = 750$, respectively. It is clear that the DC output voltage V_+ is always maintained around its reference 200 V while the ripple voltage of V_- varies from 337 V to 431 V depending on the maximum voltages of V_-. Importantly, the voltage ripples of the voltage V_+ are only about 5 V when $V_{-max}^* = 700$ V and 750 V. As a result, nearly all the ripple power is now stored on the lower capacitor C_- instead of both C_+ and C_- over a wide range of V_-. It is worth again pointing out that only two 5 μF are used in the system. The reduction of capacitors and ripples on the output V_+ have been achieved at the same time.

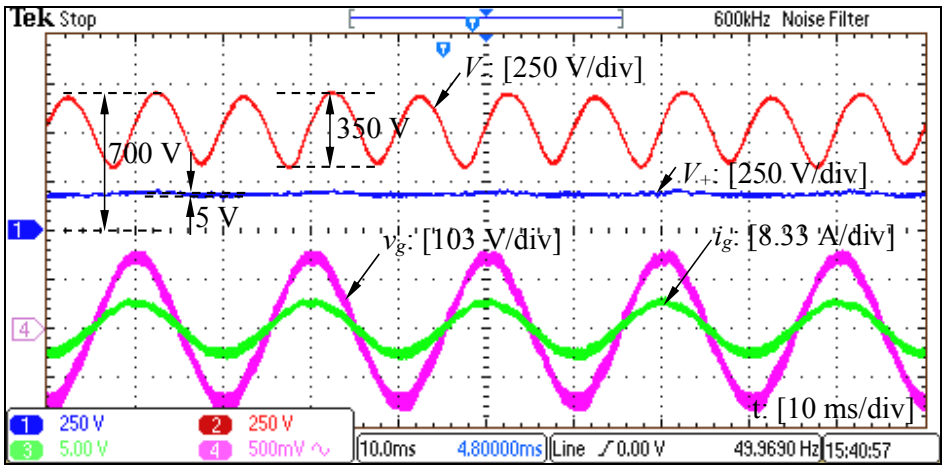
In order to clearly illustrate the relationship between the voltage ripples and the average voltage on the capacitor C_-, the steady-state performance to reduce the ripple voltage under different average voltage of V_- is shown in Figure 4.6. It can be clearly seen that the ripples of V_+ were kept around 5 V over a wide range of V_- while the ripples of V_- are much larger, ranging from 337 V to 431 V. Furthermore, the ripples of V_- decreased along with


Tek PreVu
600kHz Noise Filter
V_-: [250 V/div]
V_+: [250 V/div]
600 V
431 V
12 V
v_g: [103 V/div]
i_g: [8.33 A/div]
t: [10 ms/div]
250 V
250 V
5.00 V
500mV
10.0ms
4.80000ms
Line 0.00 V
49.9607 Hz
15:37:49

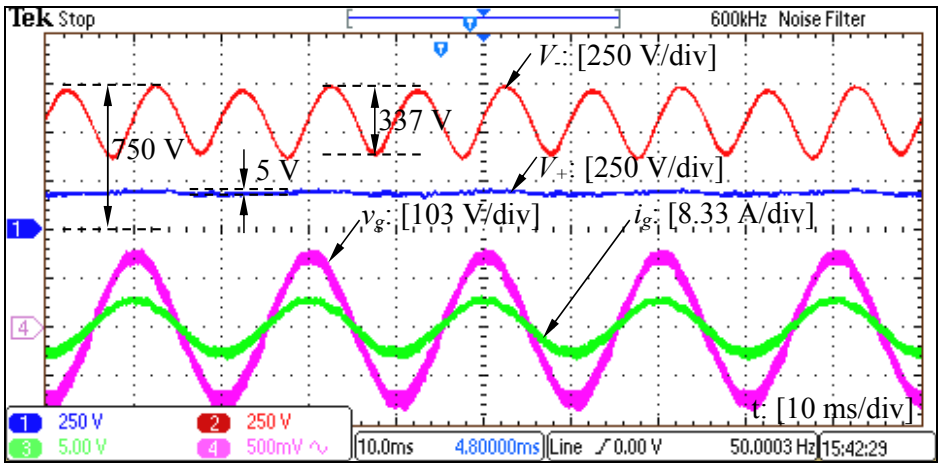
(a)


Tek Stop
600kHz Noise Filter
V_-: [250 V/div]
V_+: [250 V/div]
650 V
402 V
7 V
v_g: [103 V/div]
i_g: [8.33 A/div]
t: [10 ms/div]
250 V
250 V
5.00 V
500mV
10.0ms
4.80000ms
Line 0.00 V
49.3684 Hz
15:38:15

(b)


Tek Stop
600kHz Noise Filter
V_-: [250 V/div]
350 V
700 V
V_+: [250 V/div]
5 V
v_g: [103 V/div]
i_g: [8.33 A/div]
t: [10 ms/div]
250 V
250 V
5.00 V
500mV
10.0ms
4.80000ms
Line 0.00 V
49.9690 Hz
15:40:57

(c)



(d)

Figure 4.5: Grid voltage v_g, grid current i_g and DC voltages V_+ and V_- with $V_+^* = 200$ V: (a) when $V_{-max}^* = 600$ V, (b) when $V_{-max}^* = 650$ V, (c) when $V_{-max}^* = 700$ V and (d) when $V_{-max}^* = 750$ V.

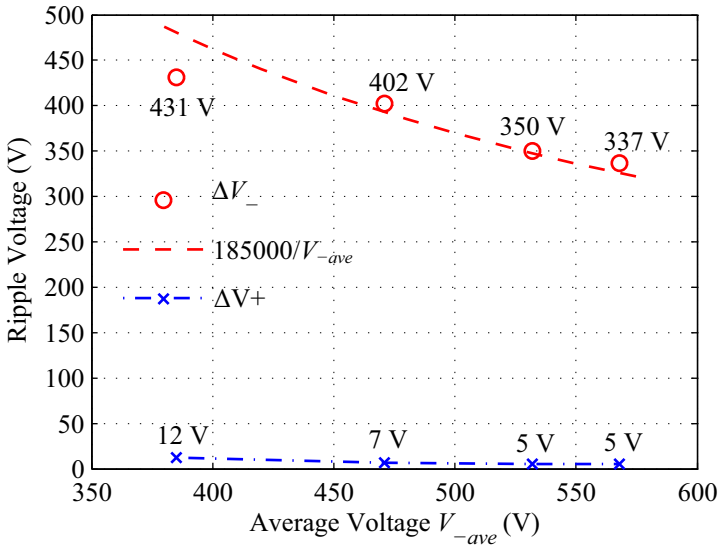


Figure 4.6: Voltage ripples of V_+ and V_- over a wide range of V_{-ave}.

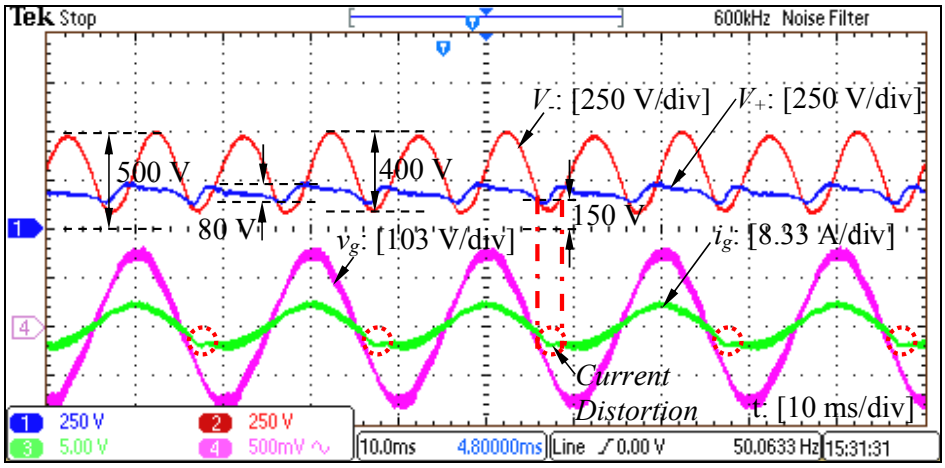


Figure 4.7: Deteriorated system performance with $V_+^* = 200$ V when $V_{-max}^* = 500$ V.

the increase of its average voltage. The obtained experimental results nicely match the condition (4.21) with $\triangle V_- = \frac{185000}{\mathrm{V}_{-\mathrm{ave}}}$ (represented by the dashed line in Figure 4.6) over a wide range of V_{-ave} as long as the boost operation of the converter is successful. Here, the number 185000 was found via curve fitting.

Moreover, the grid current i_g is always regulated to be clean and in phase with the grid voltage and, thus, the unity power factor is achieved. According to the recorded experimental data, the THD of the grid current is around 4% and the input power factor is above 0.99 for all cases. This verifies that the regulation of the grid current is not affected by large ripples of V_- and the voltage difference between V_+ and V_-. Note that the experimental test rig is not optimised for high power quality because it is not the main focus of this chapter. In light of this, the obtained results are very good.

In order to further demonstrate the operation of the system, another two results are shown in Figures 4.7 and 4.8, respectively, for the cases when the DC voltages V_+ and V_- were lower than the peak grid voltage and when the controller that removes the fundamental component from i_{C-} was disabled. As shown in Figure 4.7, the output voltage ripple becomes around 80 V, much larger than 5 V, when V_{-max}^* is set at 500 V. The relatively low voltages of V_+ and V_- also lead to distorted grid current as highlighted by the dashed circles in Figure 4.7 when both voltages are lower than the peak grid voltage. When the controller that removes the fundamental component from i_{C-} was disabled, the results are shown in Figure 4.8. The voltage V_- now consists of a noticeable fundamental component. The ex-

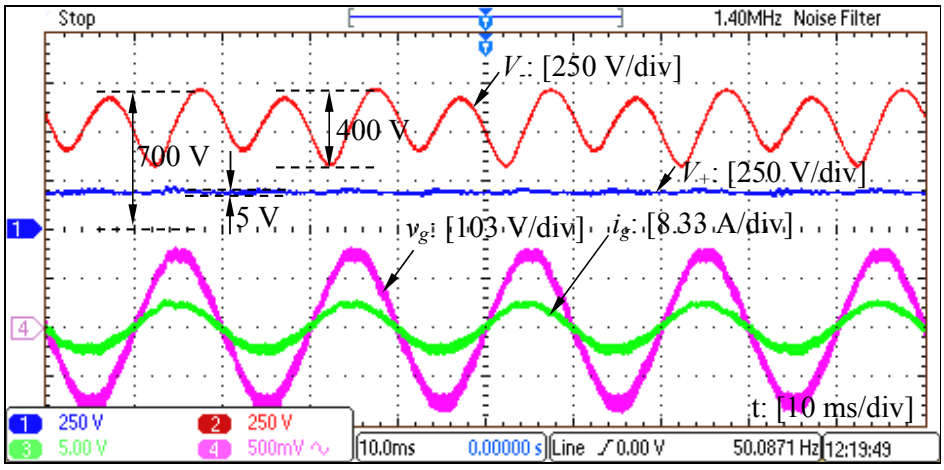


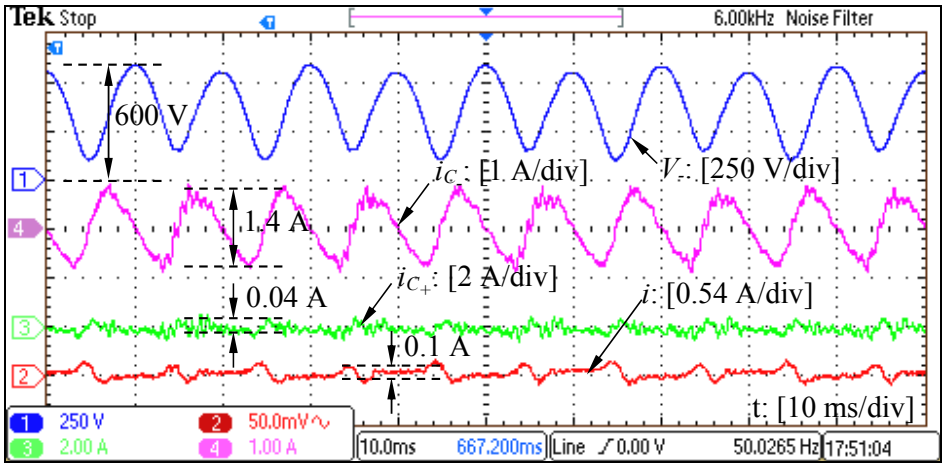
Figure 4.8: Deteriorated system performance when the controller that removes the fundamental component from i_{C-} was disabled ($V^*_{-max} = 700$ V).

perimental data of Figures 4.5(c) and 4.8 were processed in MATLAB/Simulink to extract the fundamental component and indeed the fundamental component increased from 2 V to 15 V when the resonant controller was disabled.

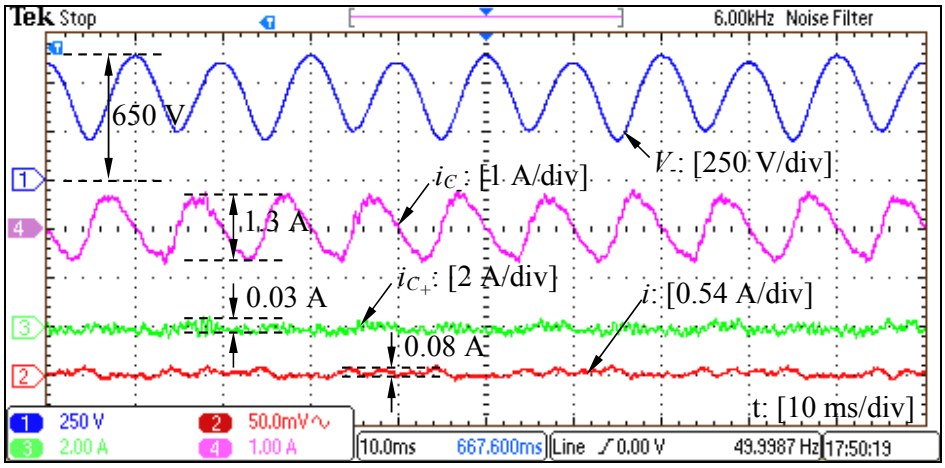
4.7.1.2 The DC-bus current and the capacitor currents

As mentioned above, the reduction of the voltage ripples is achieved by controlling the AC component i of the DC-bus current I. In order to show the system performance of the current control, the waveforms of the DC-bus current and the capacitors currents i_{C+} and i_{C-} over a wide range of V_- are shown in Figure 4.9(a)-(d). Note that a low-pass filter with a cut-off frequency of 6 kHz is applied to remove the high frequency component in the currents. It can be seen that the AC component of the DC-bus current and the current i_{C+} are always maintained around zero for different voltages of V_-. On the other hand, the ripples of the capacitor current i_{C-} are relatively large because all the ripple power is now stored on the capacitor C_-. In general, it can be seen that the higher the capacitor voltage V_-, the lower the capacitor current i_{C-}. The relationship between the capacitor voltage and the capacitor current is shown in Figure 4.10, which nicely matches the condition $\triangle i_{C-} = \frac{600}{V_{-ave}}$, where the number 600 was found via curve fitting.

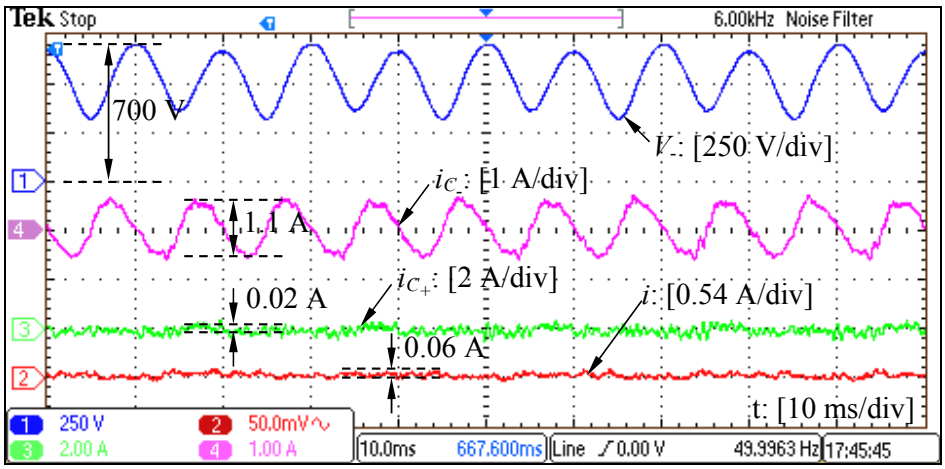
Moreover, the spectra of the DC-bus current I are shown in Figure 4.11(a) and Figure 4.11(b) to demonstrate the performance of reducing the second-order ripples in the current I for the cases without and with the repetitive controller, respectively. It is obvious that the


Tek Stop
6.00kHz Noise Filter
600 V
i_C: [1 A/div]
V: [250 V/div]
1.4 A
i_{C+}: [2 A/div]
0.04 A
i: [0.54 A/div]
0.1 A
t: [10 ms/div]
250 V
50.0mV
2.00 A
1.00 A
10.0ms
667.200ms
Line 0.00 V
50.0265 Hz
17:51:04

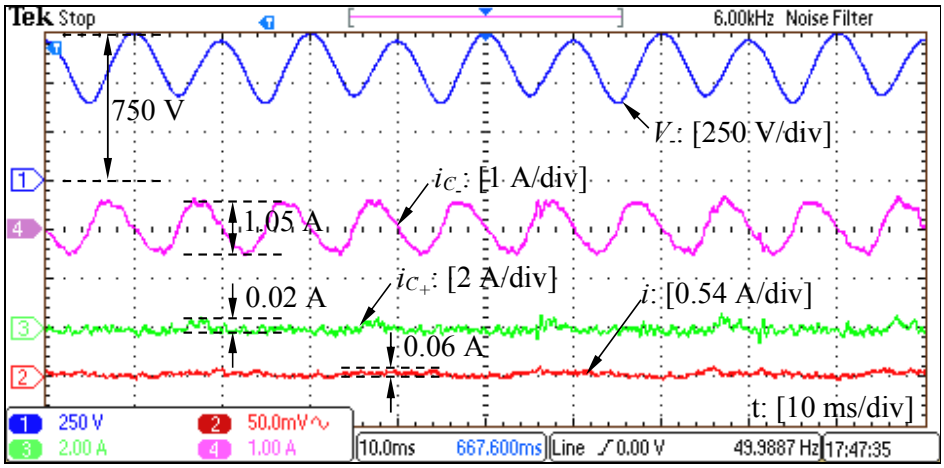
(a)


Tek Stop
6.00kHz Noise Filter
650 V
V: [250 V/div]
i_C: [1 A/div]
1.3 A
i_{C+}: [2 A/div]
0.03 A
i: [0.54 A/div]
0.08 A
t: [10 ms/div]
250 V
50.0mV
2.00 A
1.00 A
10.0ms
667.600ms
Line 0.00 V
49.3987 Hz
17:50:19

(b)


Tek Stop
6.00kHz Noise Filter
700 V
V: [250 V/div]
i_C: [1 A/div]
1.1 A
i_{C+}: [2 A/div]
0.02 A
i: [0.54 A/div]
0.06 A
t: [10 ms/div]
250 V
50.0mV
2.00 A
1.00 A
10.0ms
667.600ms
Line 0.00 V
49.3963 Hz
17:45:45

(c)



(d)

Figure 4.9: Voltage V_-, DC-bus ripple current i and capacitor currents i_{C+} and i_{C-} with $V_+^* = 200$ V: (a) when $V_{-max}^* = 600$ V, (b) when $V_{-max}^* = 650$ V, (c) when $V_{-max}^* = 700$ V and (d) when $V_{-max}^* = 750$ V.

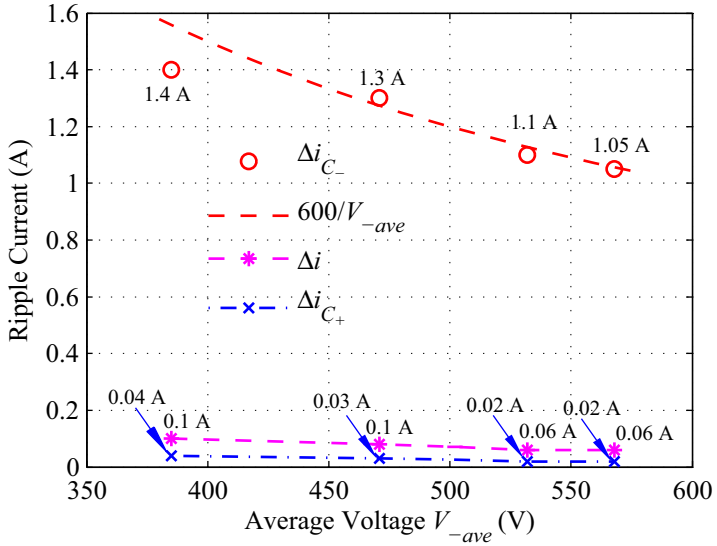
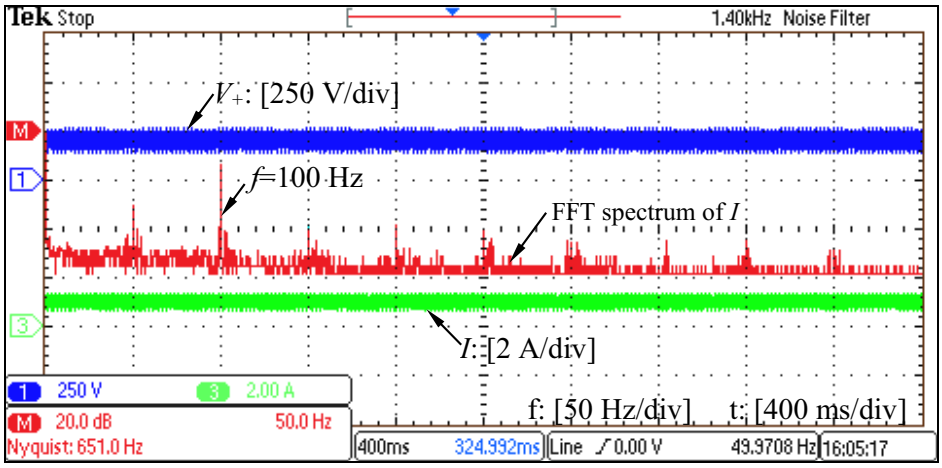
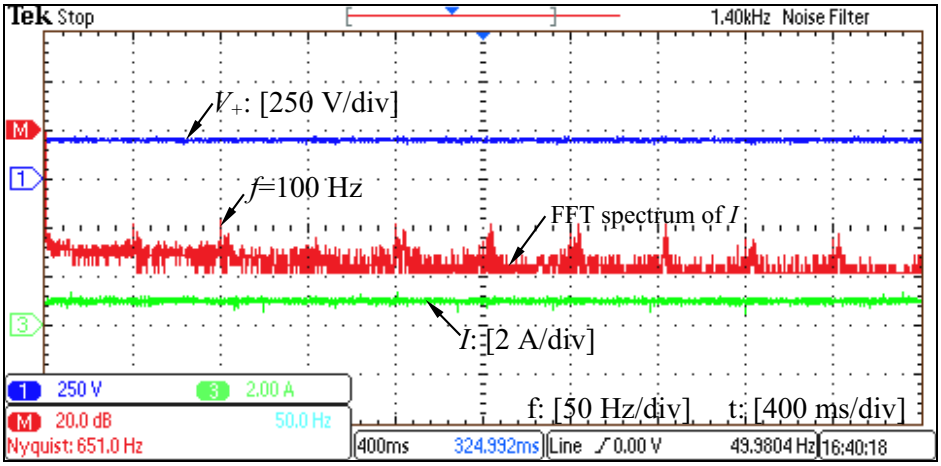


Figure 4.10: DC-bus current i and capacitor currents i_{C+} and i_{C-} over a wide range of V_{-ave}.



(a)



(b)

Figure 4.11: Comparison of (a) without and (b) with the repetitive current controller for the neutral leg.

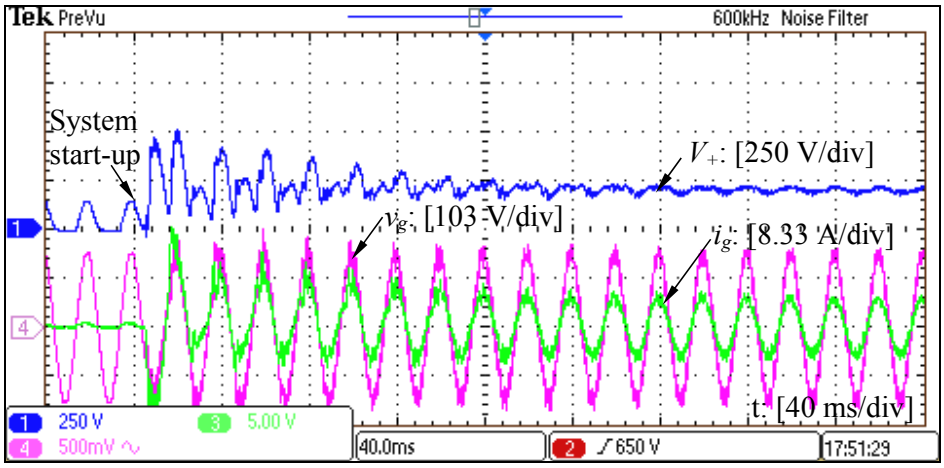


Figure 4.12: System start-up ($V_+^* = 200$ V and $V_-^* = 700$ V).

second-order harmonic component, i.e. 100 Hz, in the current I is significantly reduced when the repetitive controller is enabled. Most of the 100 Hz component is diverted to the neutral leg from the output capacitor. Due to the diverted 100 Hz current, both the ripples of the output voltage V_+ and DC-bus current I are considerably reduced as shown in Figure 4.11(b).

4.7.2 Transient Performance

4.7.2.1 System start-up

In order to demonstrate the transient response of the proposed system, the results during the system start-up are shown in Figure 4.12. The grid current first increased to charge the capacitors and then the current was maintained well back to its steady-state value after the DC output voltage was settled. The system start-up took about 200 ms, which is only about 10 cycles.

4.7.2.2 Change of the voltage reference

When the reference of the voltage V_+ was changed from 200 V to 300 V, the results are shown in Figure 4.13. The voltage V_+ was smoothly increased from 200 V to 300 V without any spikes. It is worth highlighting that the ripple level of the output voltage V_+ is always small during the transient period. However, the ripples of the voltage V_- became larger in order to tackle the increased ripple power caused by the increased voltage reference

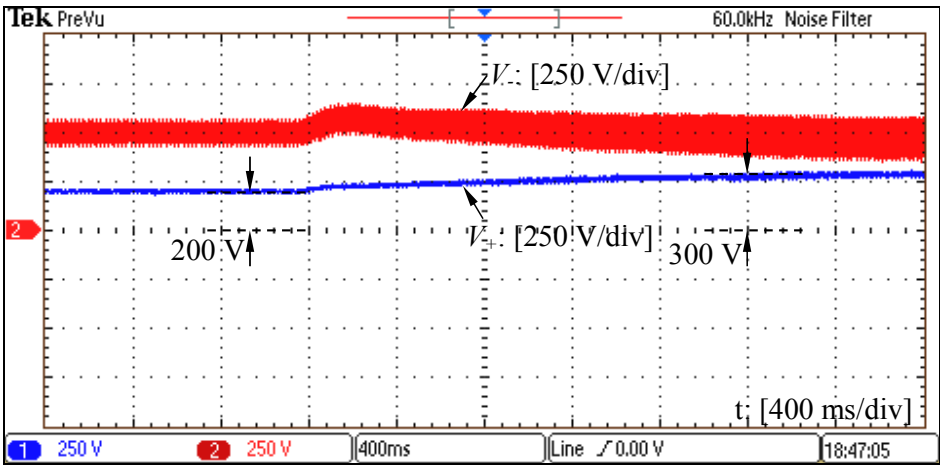
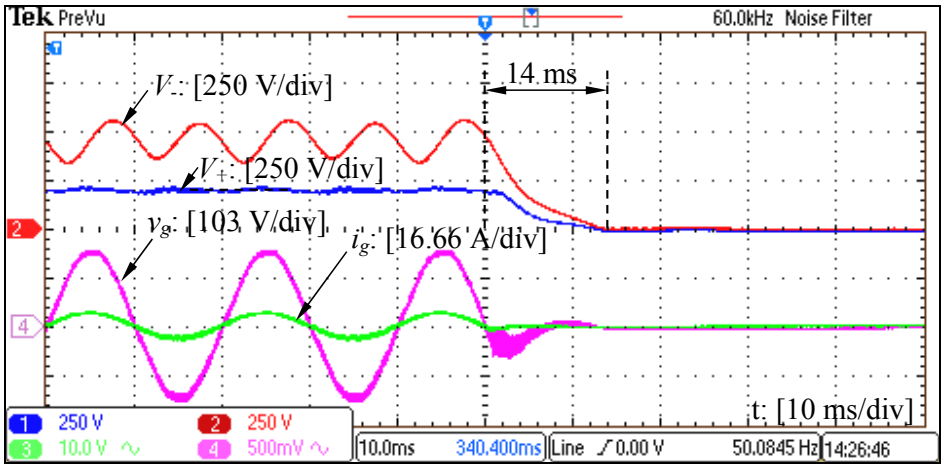


Figure 4.13: Transient response when the reference of the voltage V_+ was changed from 200 V to 300 V.

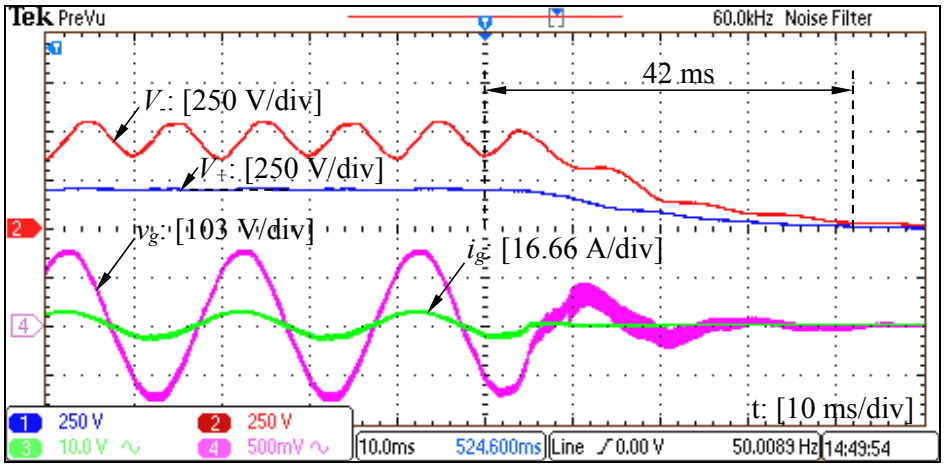
(and the power). This transient response took about 2 s, which is limited by the allowable maximum neutral current of the experimental system, and could be made much faster if the allowable maximum neutral current is increased. For the test rig, the neutral current is limited by the neutral inductor, which would be saturated if the neutral current exceeds about 5 A.

4.7.2.3 Hold-up time

Although the DC-bus capacitors are designed for systems without hold-time requirement, it is still interesting to see how the proposed converter responds to a sudden AC power outage. Here, two experiments were conducted in order to show the system performance regarding to the hold-up time under different capacitors. In order for a fair comparison, only the capacitor C_+ was changed while the other system parameters were kept unchanged. With $C_+ = 5\ \mu$F, the time for the voltage V_+ decreased from 200 V to 0 V is about 14 ms as shown in Figure 4.14(a). Of course, this time is too short for systems with hold-up requirement. A simple way to increase this time is to use a larger capacitor. The experimental result with a larger capacitor ($C_+ = 100\ \mu$F) is shown in Figure 4.14(b). Indeed, the voltage V_+ was decreased at a much slower pace, which took about 42 ms for the voltage V_+ to decrease from 200 V to 0 V. Since the main focus of this chapter is not about the hold-up time, no further mathematical analysis is made. Interested readers are referred to (Wang et al., 2014) to see how to design capacitors for single-phase converters with hold-up time requirement.



(a)



(b)

Figure 4.14: Transient response after a sudden AC power outage with (a) $C_+ = 5\ \mu$F, $C_- = 10\ \mu$F and (b) $C_+ = 100\ \mu$F, $C_- = 10\ \mu$F.

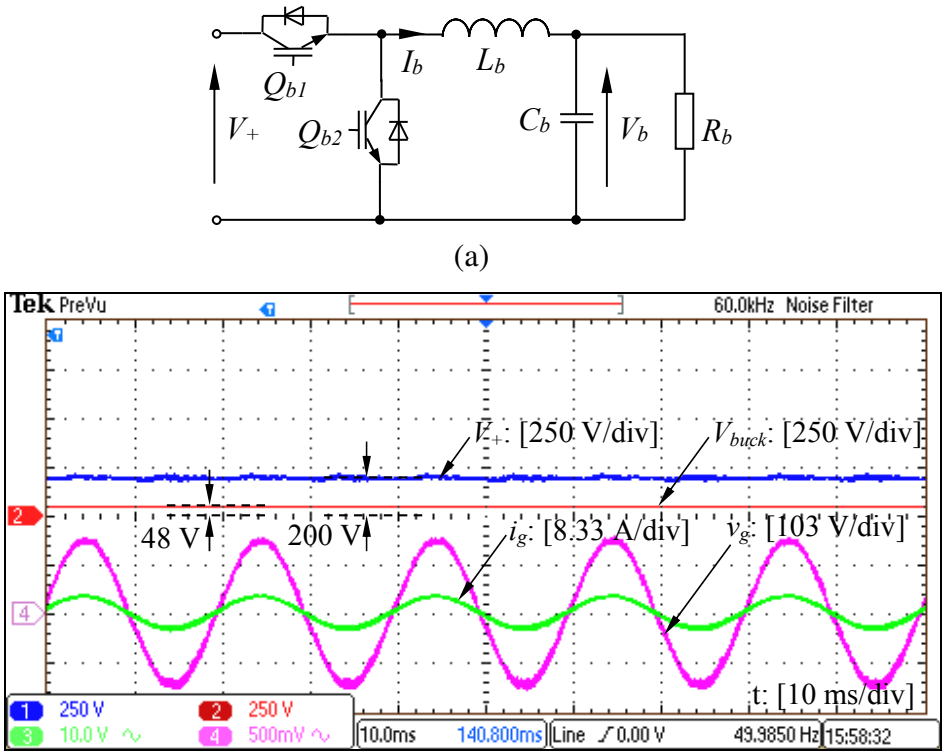


Figure 4.15: System performance with a buck DC/DC converter and a resistor as the load of the converter.

4.7.3 System Performance with a Hybrid Load

Apart from resistive loads, converters often have switching devices connected as loads. Such switching devices can include DC/DC converters and DC/AC converters. In order to validate this, a buck DC/DC converter shown in Figure 4.15(a) was built as the switching load and its output voltage V_b is regulated to be around 48 V while its input voltage V_+ is 200 V and the load R_b is 20 Ω. Note that a 470 Ω resistor is also connected across the voltage V_+, which means the equivalent load of the converter is a combination of resistive and switching loads. As shown in Figure 4.15(b), the voltage V_+ (200 V) is levelled down to the voltage V_b (48 V) and the ripples of the voltage V_+ are again kept to be very low. As a result, the proposed converter can indeed work well with both resistive and switching loads.

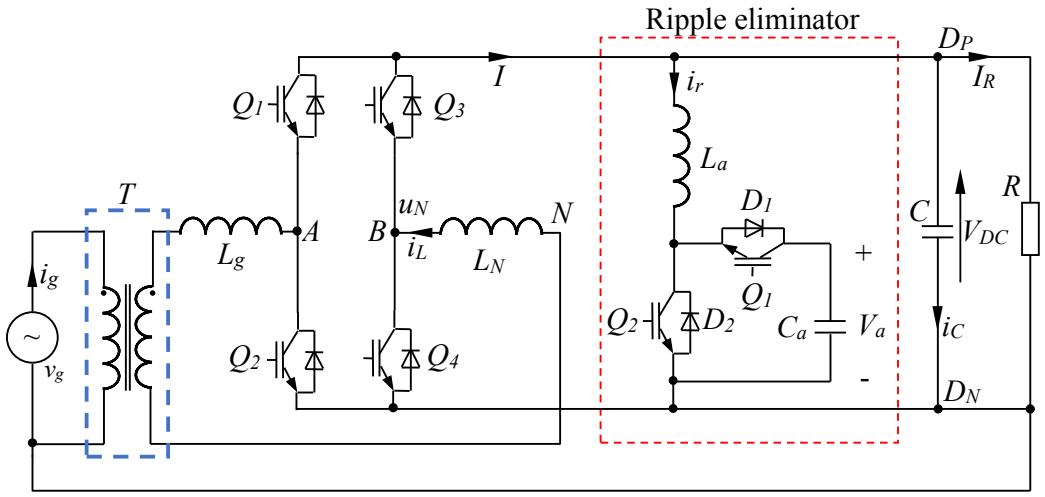


Figure 4.16: The full-bridge system used for the comparison.

4.8 Efficiency Comparison

In this section, the proposed converter is compared to a system to evaluate the efficiency performance. In order to be fair, the system used for comparison should be able to work with the widely-spread single-phase unbalanced power grid and also should have the following features: (1) a common AC and DC ground; (2) capability of working with any power factor; (3) bidirectional power flow; (4) capability of reducing the usage of DC capacitors. Because of so many integrated features, it is not easy to find a suitable solution. For example, most converters would fail if their AC and DC grounds are directly connected together. Indeed, there are a few topologies with common AC and DC ground in the literature, such as the Zigzag converter proposed in (Fujita, 2010) and the Karschny converter proposed in (Karschny, 1998). However, they are not good candidates for the comparison because the Karschny converter cannot work with non-unity power factor (Karschny, 1998) while the Zigzag converter requires relatively large and increased number of capacitors (Fujita, 2010). It is worth mentioning that the Zigzag converter benefits with multilevel outputs, which helps improve the power quality of the grid current and also to reduce the size of AC filters.

After careful comparison among different systems, the full-bridge system shown in Figure 4.16 is used for the comparison. The isolating transformer T facilitates the direct connection between AC and DC grounds. Moreover, the conventional single-phase full-

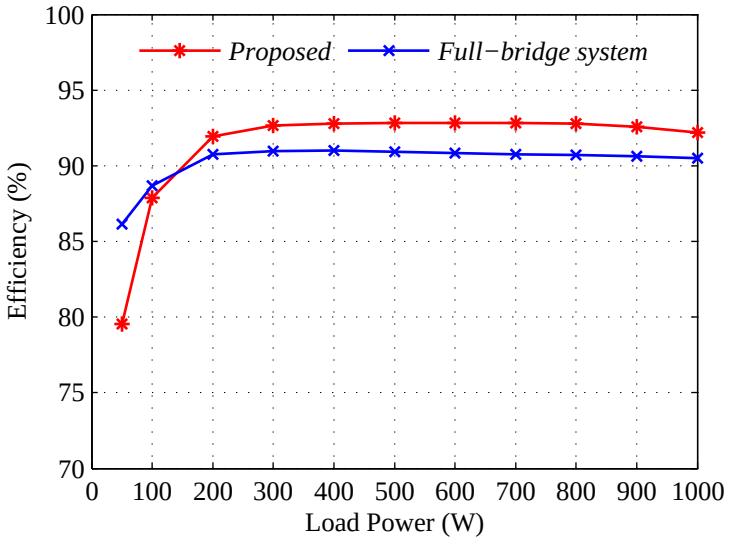


Figure 4.17: Efficiency comparison.

bridge converter is used as the interface between the AC and DC sides to achieve any power factor. At the same time, a ripple eliminator (Krein et al., 2012; Zhang et al., 2013b; Zhong et al., 2012b; Wang et al., 2012; Pini and Barbi, 2011) is hooked onto the DC bus to absorb the ripple energy. Hence, the total usage of capacitors can be significantly reduced while having low DC-bus voltage ripples.

Based on the above discussion, it is clear that the full-bridge system shown in Figure 4.16 is a good candidate for the comparison because it has all the four main features of the proposed converter. The full-bridge system and the proposed converter have their own merits. For example, the proposed converter does not need the isolating transformer and the number of used switches are only four, which means two switches are saved compared to the full-bridge system. Moreover, it is easier to commercially implement the proposed converter by using a power module with four switches. On the other hand, the full-bridge system benefits with lower voltage stress of switches because of the adopted full-bridge topology. As a result, the switching loss of the full-bridge system is expected to be lower than the proposed converter. However, because of the reduced number of switches and the removed isolating transformer, the efficiency of the proposed system could be comparable with that of the full-bridge system even if the switching loss of the proposed converter is higher.

In order to compare the efficiency between the full-bridge system and the proposed

converter, PLECS simulations of both systems were constructed. Similar method to compare efficiencies is used in Chapter 2, which has been demonstrated to be accurate enough. The same DC capacitors and switches are used for both systems for a fair comparison. A 1 kW system was built based on PLECS and MATLAB/Simulink and the system power ranging from 50 W to 1000 W was tested by changing the DC load while keeping the DC output voltage constant. The obtained result is shown in Figure 4.17. It is obvious that the proposed converter are almost always more efficient than that of the full-bridge system except when the power is low (<150 W).

As to power density, the proposed converter is absolutely higher than the full-bridge system shown in Figure 4.16. This also means reduced system cost even if the increased cost of the switches due to the increased voltage stress.

To sum up, the proposed converter is always better than the full-bridge system shown in Figure 4.16 in terms of power density, efficiency and cost, and is a very competitive solution for high power density converters.

4.9 Summary

This chapter has addressed a big issue for single-phase converters, which is to reduce DC-bus low-frequency voltage ripples and total capacitance required. It has been demonstrated that the required usage of DC-bus capacitors can be significantly reduced while maintaining low output voltage ripples by advanced control strategies. As a result, highly-reliable film capacitors can be used to replace bulky electrolytic capacitors. The elimination of DC-bus electrolytic capacitors is achieved by the neutral leg of the converter without adding any other power components. To be more precise, all the ripple energy is diverted from the upper (output) capacitor to the lower capacitor through the neutral leg so that the upper capacitor can be reduced a lot. At the same time, the voltage across the lower capacitor is designed to have large ripples as it is not supplied to any loads. In this case, both capacitors can be reduced to a level that film capacitors are cost effective to be used.

The rectification leg of the converter is used to maintain the grid current and the DC-bus voltage. Importantly, the impact of different voltages across the capacitors are analysed in detail. It has been found that the different voltages and large voltage ripples do not affect

the aforementioned functions of the two legs but do affect the selection of the switches because the upper switches and lower switches of both legs may have different voltage and current stresses. Experimental results have been presented to show that the required usage of capacitors can be reduced by over 70 times while maintaining the same level of output voltage ripples for the test rig. The converter can indeed work well without using DC-bus electrolytic capacitors.

Chapter 5

Reduction of High-frequency Common-Mode Voltages of ρ-converters

In this chapter, the reduction of common-mode currents without the need of an isolating transformer is investigated via providing a common AC and DC ground for grid-tied converters, following the ρ-converter developed in Chapter 4 that reduces the need of bulky electrolytic capacitors. Moreover, the operation of the converter as both a rectifier and an inverter is demonstrated. Because of the common AC and DC ground, the parasitic capacitance on the path of common mode currents is bypassed. The key to achieve this lies in the active control strategy that decouples the control of the two legs of the converter so that one leg is responsible for the power exchange between the DC side and the AC side and the other leg is responsible for maintaining stable voltages across the DC split capacitors and providing a path for the DC current. Experimental results are provided to validate the analysis.

5.1 Introduction

Driven by the penetration of renewable energy systems, a lot of advanced technologies regarding the integration of renewable systems with the power grid are developed in the last few years (Zhong and Hornik, 2013b). Due to parasitic capacitors between power sources in some renewable systems and the ground, the problem of high common mode (CM) currents, which reduces system efficiency and causes safety concerns like electric shock, has become a serious issue for renewable energy systems. In order to eliminate/reduce

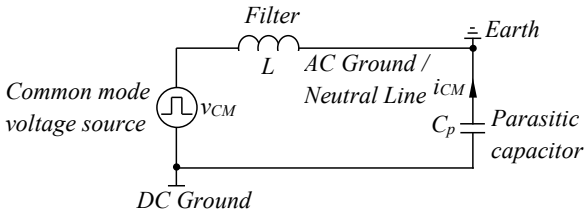


Figure 5.1: Generic equivalent circuit for analysing CM currents.

CM currents, galvanic isolation transformers are normally added between the renewable energy systems and the grid. But the adoption of transformers reduces power density and efficiency (Kerekes et al., 2011) and increases manufacturing costs. As a result, systems without transformers have attracted more and more attention. However, the absence of transformers may lead to high CM currents.

Figure 5.1 illustrates a generic equivalent circuit for analysing CM currents, which consists of a CM voltage source v_{CM}, a filter L and a parasitic capacitor C_p between the DC ground and the AC ground, which is often connected to the earth via the neutral line when an isolating transformer is not used. This closes the loop for the CM current i_{CM} and the CM voltage v_{CM}, which is generated by the switching of power switches and other reasons, appears on the parasitic capacitor C_p. If the switching frequency is high enough, the CM current i_{CM} could be very large even if the parasitic capacitor C_p is relatively small.

In general, the CM current i_{CM} mainly depends on both the behaviour of the CM voltage and the impedance in the path of the CM current. In light of this, there are four main approaches in the literature to reduce CM currents. One approach is to reduce high-frequency components in the CM voltage v_p across the parasitic capacitor C_p. This can be achieved by reducing high-frequency components in the v_{CM} e.g. changing the modulation strategies (FREDDY TAN et al., 2015; Bae and Kim, 2014) and decoupling AC and DC sides of converters during freewheeling phases (Kerekes et al., 2011; Buticchi et al., 2014; Xiao et al., 2014; Ji et al., 2013). It can also be achieved by putting passive or active components (Barater et al., 2014) in series or in parallel with v_{CM}. Although these methods to reduce v_p can reduce CM currents to some extent, they suffer from reduced voltage utilization ratio (Cavalcanti et al., 2010), reduced ability to process reactive power (Gu et al., 2013) and/or degraded performance caused by parasitic capacitors of switches (Gu et al., 2013).

The second approach is to increase the impedance in the path of the CM current. For

example, this can be achieved by increasing the filter L. Filters used for this purpose is called CM filters (Heldwein et al., 2010), which have large inductance to mitigate CM currents. However, due to the large size and heavy weight, the system power density could be reduced.

The third approach is to provide another current path between the AC ground and the DC ground so that most of the CM current flow through this path instead of the parasitic capacitor. For example, this can be achieved by connecting the AC ground to the midpoint of the DC bus, which is normally formed by split capacitors (Xiao and Xie, 2012). This makes the split capacitors in parallel with the parasitic capacitor so that most of the CM current i_{CM} can be bypassed through the split capacitors. Since the split capacitors are normally much larger than the parasitic capacitor C_p, the CM current is reduced. For example, converters based on the half-bridge topology are equipped with split capacitors (Srinivasan and Oruganti, 1998), which have the potential of forming the bypassing current path. For three-phase applications, the three-phase four-wire power converters proposed in (Zhong and Hornik, 2013b; Hornik and Zhong, 2013) also have the bypassing current path so that CM current i_{CM} can be reduced a lot. Another way is to connect the neutral point of the AC side formed by AC capacitors of the LC filters to the split capacitors (Dong et al., 2012a). In this case, the AC capacitors are in series with the split DC capacitors in the current path, which are in parallel with the parasitic capacitor C_p.

The last approach is to connect the AC ground and the DC ground together so that the CM current i_{CM} is almost completely eliminated. The elimination of CM currents is naturally achieved because the parasitic capacitor is short-circuited without any other efforts, when ignoring the parasitic inductance of the cables. One of such converters is the Karschny inverter (Karschny, 1998). Unfortunately, this inverter suffers from the complex structure, the increased number of power switches and the need of large capacitors. Another one was proposed in (Gu et al., 2013), where the concept of virtual DC bus is used to enable the direct connection between AC and DC grounds. The virtual DC bus is achieved by adding an extra active switch and an extra DC capacitor into a conventional full-bridge converter. Benefiting from its topological structure, the converter is capable of exchanging both real and reactive power with the power grid. The operation of the two converters are similar to that of conventional full-bridge converters. Moreover, it is also possible to

connect the AC and DC grounds together if the midpoints of both AC and DC sides are constructed, as reported in (Breazeale and Ayyanar, 2015).

As reported in (Kerekes et al., 2009), it is possible to have a common AC and DC ground if two series of balanced PV panels are connected to a three-phase inverter with split DC capacitors. The midpoint of the split capacitors is then connected to the grid neutral line. In this case, the CM currents can be almost completely eliminated. However, the upper and lower panels are likely to become unbalanced due to the potential induced degradation (PID) of solar panels (Omron, 2013; Fujita, 2010), even initially designed to be balanced. The unbalanced voltages could lead to the failure of the whole system. From the view of preventing the PID effect, it is better to only keep the upper PV panels. However, it is not straightforward to run the system without the lower PV panels. This is because the split DC capacitors cannot provide the required DC current to make the grid current free from DC components. It is also difficult or even impossible to maintain the voltages across the split capacitors to be balanced without employing a suitable control strategy.

In this chapter, the idea of connecting the AC ground and the DC ground together is explored further, based on the converter topology equipped with split DC capacitors. After briefly describing the grounds, grounding and common-mode currents in grid-tied converters, the challenges to connect the AC ground and the DC ground of a converter together are discussed in detail. Then, it is revealed that a single-phase four-switch converter recently reported in (Ming et al., 2016) is able to overcome these challenges, after proposing a suitable control strategy to balance the voltages across the split capacitors. Such a converter consists of a neutral leg and a conversion leg. Thanks to the neutral leg, the DC ground can be directly connected to the AC ground. Accordingly, the CM current can be almost completely eliminated when ignoring the parasitic inductance of the cables. Moreover, the DC-side voltage of the converter, which is just about half of the whole DC-bus voltage of conventional half-bridge converters, is only required to be higher than the peak value of the grid voltage. This doubles the voltage utilization ratio of conventional half-bridge converters. Note that the minimum voltage of the whole DC bus is still the same as that of the conventional half-bridge converters, which is twice of the grid voltage. Hence, the voltage stress of the switches is not changed. The conversion leg is used to control the power exchanged between the DC bus and the power grid, which simplifies the operation of the

converter. It is also worth pointing out that both real and reactive power can be exchanged without any restrictions caused by the common ground. In addition, the control of the two legs are independent from each other, which makes control design very flexible so there is no restriction on the modulation and control strategies caused by the common AC and DC ground. Moreover, the operation of this converter is very different from the conventional full-bridge converters, although both converters have two legs. The operation of the two legs in this converter is independent from each other while the two legs in conventional full-bridge converters is dependent with each other. This is the key to make it possible to connect the AC ground and the DC ground together. Compared to Chapter 4, the new contributions of this chapter include: 1) revealing the capability of this converter on reducing CM currents after presenting the challenges and benefits of providing a common AC and DC ground for grid-tied converters; 2) proposing a suitable control strategy to achieve this; 3) demonstrating the operation as an inverter, in addition to the operation as a rectifier.

5.2 Grounds and CM Currents of Grid-tied Converters

5.2.1 Ground, Grounding and Grounded Systems

In electrical engineering, ground refers to the reference point in an electrical circuit from which voltages are measured, a common return path for electric currents, or a direct physical connection to the earth. For grid-tied converters, separate reference points are often adopted for the DC and AC parts of the circuit, respectively. As a result, there are often three (or more) grounds in a grid-tied converter, i.e., the earth, an AC ground and an DC ground.

Grounding is connecting, whether intentionally or accidentally, an electrical circuit or equipment to the earth or to some conducting body that serves in place of the earth (Wiles, 2012). In this chapter, only the intentional grounding will be considered. In general, there are two kinds of groundings: equipment grounding and system grounding. Equipment grounding refers to connecting any exposed non-current carrying electrical conductors or equipment to the earth. By doing this, the voltage from the conductors or equipment to the earth can be limited, which avoids potential electrical shock. Proper equipment grounding is essential for any electrical equipment as the electrical conductors or equipment may be

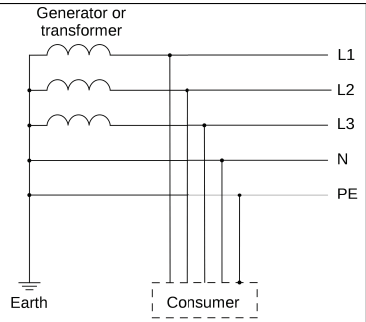
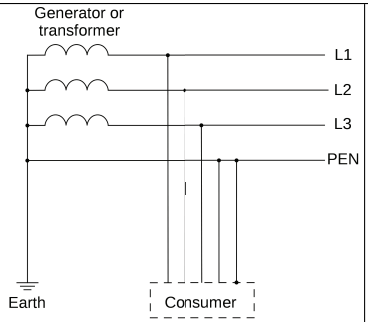
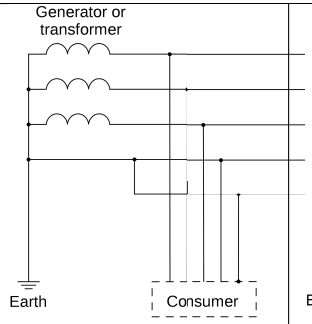
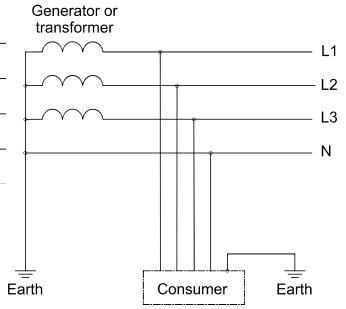
Network	TN-S	TN-C	TN-C-S	TT
Structure				
Features	Separate Protective Earth (PE) and Neutral (N) conductors from transformer to consuming device.	Combined PE and N conductor all the way from the transformer to the consuming device.	Combined PEN conductor from transformer to building distribution point, but separate PE and N conductors in fixed indoor wiring and flexible power cords.	The protective earth connection for the consumer is provided by a local earth electrode, and there is another independently installed at the generator. There is no 'earth wire' between the two
Areas	Europe	Rarely used	UK and China	Japan and UK

Figure 5.2: Four earthing networks for low-voltage systems (Wikipedia, 2014).

energized because of failed insulation. System grounding refers to connecting one of the (current-carrying) electrical conductors to the earth. For a grid-tied converter, the (current-carrying) electrical conductors that are used for grounding are normally the AC ground or the DC ground. Since a converter is often connected to the grid neutral line, the AC ground is often connected to the earth. However, DC grounds may or may not be connected to the earth, depending on the topology and the control strategy of the converter. If the DC ground is not connected to the AC ground (the earth), as shown in Figure 5.1, then a CM current i_{CM} appears.

Grounded systems are those with one of the DC conductors (either positive or negative) connected to the earth or to some conducting body that serves in place of the earth (Wiles, 2012). Otherwise, systems are ungrounded. As a result, electrical systems can be classified into grounded systems and ungrounded systems, according to the arrangement for system grounding. Note that system grounding is optional but equipment grounding is essential for safety reasons. For example, for grid-tied PV inverters, the pre-2005 edition of the US National Electrical Code (NEC) required that all PV systems have one of the DC circuit conductors grounded whenever the maximum system voltage was higher than 50 volts (NEC 690.41). However, ungrounded PV systems are now allowed according to NEC 690.35, which was added to the 2005 NEC (Wiles, 2012).

Following the above definitions for ground, grounding and grounded systems, four main earthing networks are shown in Figure 5.2. According to the International Standard IEC 60364, the two-letter codes TN, TT, and IT are used to distinguish the networks (Wikipedia, 2014). The first letter indicates the connection between earth and the power-supply equipment (generator or transformer): 'T'— Direct connection of a point with earth (Latin: terra); 'I'— No point is connected with earth (isolation), except perhaps via a high impedance (Wikipedia, 2014). The second letter indicates the connection between earth and the electrical device being supplied: 'T'— Direct connection of a point with earth; 'N'— Direct connection to neutral at the origin of installation, which is connected to the earth (Wikipedia, 2014).

Note that the equipment grounding is defined as the connection between the equipment and the line PE but not the line N because the line N is designed to be the current return path and it cannot be used for equipment grounding, although the lines PE and N have the

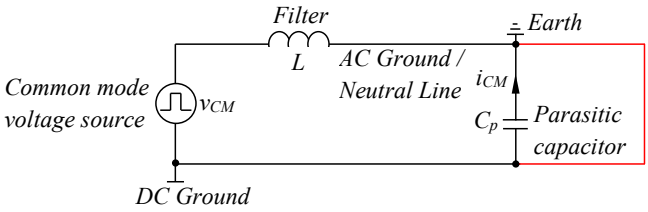


Figure 5.3: Equivalent circuit for analysing CM current of a grid-tied converter with a common AC and DC ground.

same voltage potential when ignoring the line impedance. The system grounding is not depicted in the networks, which can be achieved by connecting either the positive or the negative pole of the DC bus to the line N.

5.2.2 Benefits of Connecting AC and DC Grounds Together

As mentioned before, the AC ground of a grid-tied converter without an isolation transformer is often connected to the earth, which often results in CM currents. If the DC ground and the AC ground could be connected together, then the equivalent CM circuit can be depicted as shown in Figure 5.3, which means the parasitic capacitor C_p is short-circuited. As a result, the CM current i_{CM} is always nearly zero. Moreover, the negative pole of DC conductors (the DC ground) has almost the same voltage potential as the earth. As a result, if applied for solar power, the PID effect of solar panels can be almost prevented.

5.2.3 Challenges of Connecting AC and DC Grounds Together

As discussed above, the removal of isolation transformers is highly recommended to reduce costs and to improve system efficiency and power density (Gu et al., 2013; Meneses et al., 2013). However, most of the grounded grid-tied converters fail to work if the isolation transformers are removed. The most popular full-bridge and half-bridge converters are taken as two examples to explain the reason.

5.2.3.1 Grounding in full-bridge converters

The topology of a full-bridge converter is shown in Figure 5.4(a). The AC ground is connected to the earth and the DC ground is the negative pole of the DC bus. The parasitic capacitor is between the DC ground and the earth. The corresponding equivalent circuit for

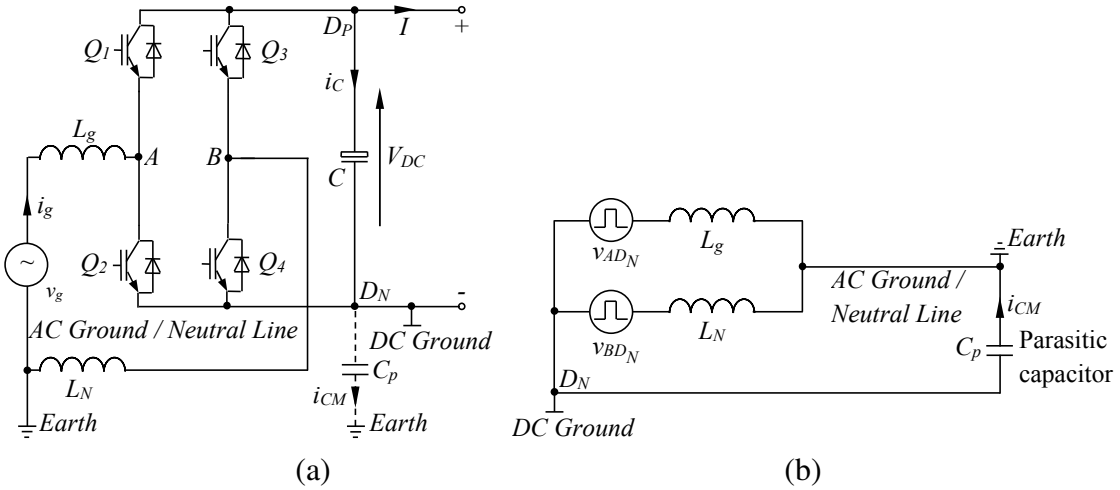


Figure 5.4: Conventional full-bridge converter: (a) topology; (b) equivalent circuit for analysing the CM current.

the CM current path is shown in Figure 5.4(b), where the equivalent common mode voltage can be found as (Dong et al., 2012a)

$$v_{CM} = \frac{v_{AD_N} + v_{BD_N}}{2} + (v_{AD_N} + v_{BD_N})\frac{L_N - L_g}{L_N + L_g}. \tag{5.1}$$

Here, v_{AD_N} and v_{BD_N} are the voltages between points A and D_N and between points B and D_N, respectively. The voltages v_{AD_N} and v_{BD_N} depend on both the system parameters and the modulation strategies. The CM current i_{CM} can be large enough to cause electrical shock if the high-frequency components in the v_{AD_N} and v_{BD_N} are high.

According to the previous discussions, the CM current could be eliminated if the AC and DC grounds were directly connected together. However, the converters would then fail to function properly and there would be no way to provide the negative AC voltage. In light of this, a negative voltage must be constituted in order to enable the connection. A possible solution is to add an additional switch and an additional DC capacitor into conventional full-bridge converters (Gu et al., 2013) to form the required negative voltage, as shown in Figure 5.5. During the negative cycle of v_{AB}, the required negative voltage is provided by the DC capacitor C_2. The detailed operation principles of this topology can be found in (Gu et al., 2013) and are not repeated here.

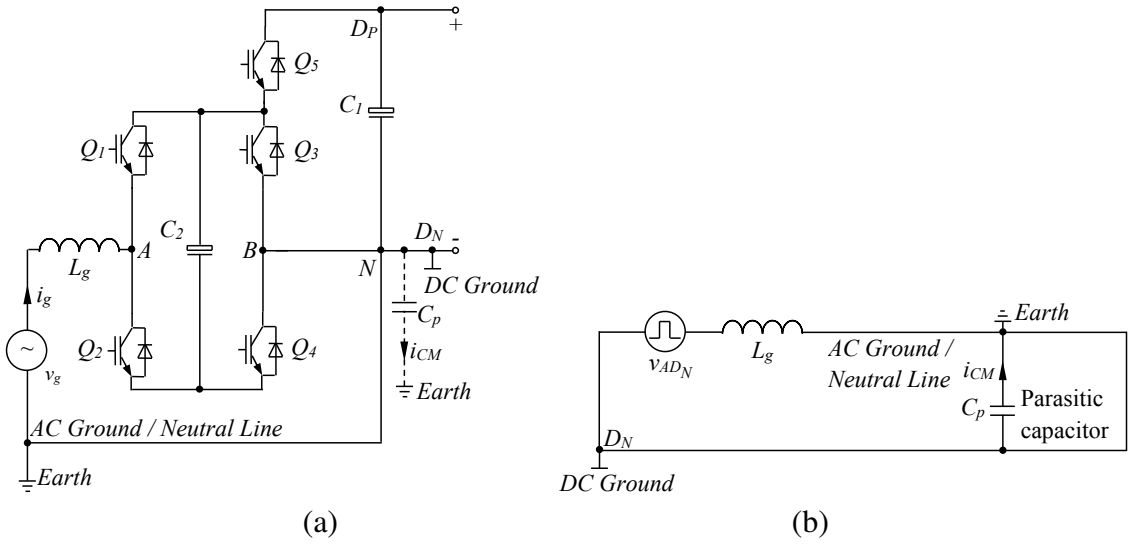


Figure 5.5: Improved full-bridge converters with a common AC and DC ground: (a) topology; (b) equivalent circuit for analysing the CM current.

5.2.3.2 Grounding in half-bridge converters

The topology of conventional half-bridge converters is shown in Figure 5.6(a) and the equivalent circuit for CM current analysis is shown in Figure 5.6(b). The CM current is reduced a lot because of the topological structure, where the two split capacitors C_+ and C_- are connected between the AC and DC grounds, in parallel with the parasitic capacitor C_p. Hence, the equivalent capacitance is much larger than C_p. The equivalent CM voltage v_{CM} is clamped to the voltages on the two capacitors, which consists of a DC component, a fundamental component and a second order component. The resulting CM current i_{CM} is much smaller and most of the CM current flows through the capacitors C_+ and C_-. The performance of reducing the CM current depends on the ratio between the parasitic capacitor C_p and the DC capacitors C_+ and C_-. The larger the DC capacitors, the smaller the CM current. However, because C_+ and C_- are normally preferred as small as possible, the CM current can still be a problem in some applications.

As mentioned previously, CM currents could be almost completely eliminated regardless of C_+ and C_- if the AC and DC grounds were connected together. However, like full-bridge converters, it is also impossible to directly connect the DC and AC grounds together for half-bridge converters. Here are the detailed reasons. There are two possible ways to connect the DC ground and AC ground together, as shown by the dot-dash lines

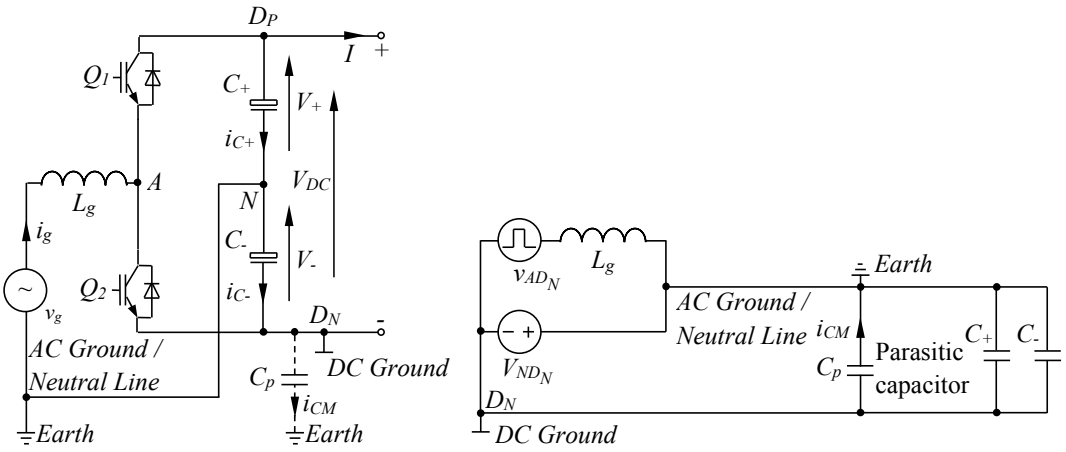


Figure 5.6: Conventional half-bridge converters: (a) topology; (b) equivalent circuit for analysing the CM current.

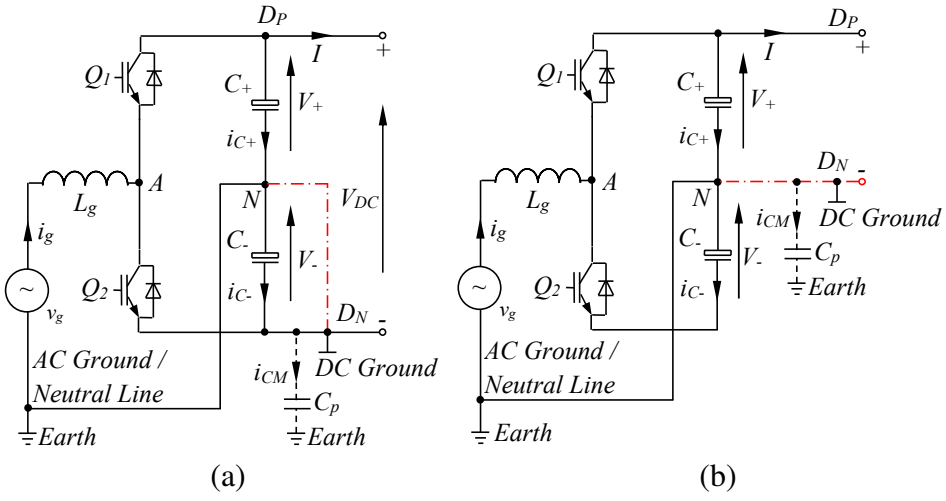


Figure 5.7: DC grounding of half-bridge converters (not feasible): (a) the negative pole of C_- is chosen as the DC grounding; (b) the negative pole of C_+ is chosen as the DC grounding.

in Figure 5.7. However, both do not work. For the case shown in Figure 5.7(a), the lower capacitor C_- is short-circuited so it would not work properly. For the case shown in Figure 5.7(b), the DC ground and the negative pole of the DC bus are moved to the mid-point of the split capacitor, i.e. the AC ground. According to the Kirchhoff's law, there is

$$i_g = i_{C_+} - i_{C_-} + I \tag{5.2}$$

where i_g, i_{C_+}, i_{C_-} and I are the currents flowing through the grid inductor, the capacitor C_+, the capacitor C_- and the DC bus, respectively. As the grid current i_g is supposed to be AC current without any DC components, the capacitors C_+ and C_- must provide the required DC current to establish (5.2). However, it is well known that capacitors cannot allow any DC currents to flow through. As a result, connecting the AC and DC grounds together in this way does not work either.

5.3 Provision of a Common AC and DC Ground to Reduce CM Currents

5.3.1 Topology under Investigation

Although conventional half-bridge converters have the potential to completely eliminate CM currents by connecting the AC and DC grounds together, it is not straightforward to do so and both options discussed in the previous section have all failed. Due to the short-circuit of the capacitor, the first option is disregarded. The second option can be viable if the required DC current I can be provided by another path instead of the capacitors. This can be achieved by adding an additional current branch to enable the connection between the AC and DC grounds.

In this chapter, a recently-proposed topology, as shown in Figure 5.8(a), has been revealed to be able to provide a common AC and DC ground. Very similarly to a conventional full-bridge converter, it consists of two legs but now the two legs, one conversion leg and one neutral leg, have different functions. The conversion leg functions as a conventional half-bridge converter. The neutral leg is put across the negative and positive points of the DC bus and the midpoint of the leg is connected to the midpoint of the split capacitors

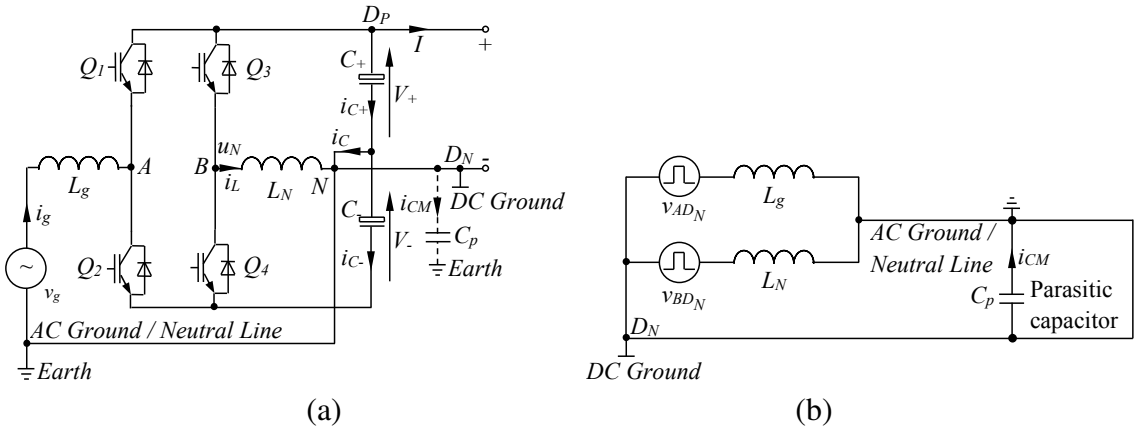


Figure 5.8: The converter with a common AC and DC ground: (a) topology; (b) equivalent circuit for analysing the CM current.

through an inductor L_N. The inductor can be treated as a part of the filter of a grid-tied converter. In this case, the inductor is used in a multiple way, i.e. to filter out harmonics and to enable the current control of the neutral leg. The main objectives of the added neutral leg are to balance the voltages V_+ and V_- and to provide the return path of the DC current I to make it work so that the AC and DC grounds can be connected together. It is worth mentioning that the two legs can be controlled independently, which makes the control design much easier and more flexible.

For this topology, the DC ground and the AC ground are directly connected together as a common ground. As a result, the CM current is almost completely eliminated because the parasitic capacitors are short circuited, as can be seen from the equivalent circuit shown in Figure 5.8(b). Moreover, this converter has the capability of operating in the rectification mode and in the inversion mode. For both modes, the power factor can be regulated to unity or other values according to system requirements. Hence, the converter has the capability of exchanging both real and reactive power with the grid, which is highly preferred for grid-tied converters. Note that the connection of the AC and DC grounds together is achieved inside the converter and the connection line can be very short, which means the parasitic line inductance is negligible.

It is worth mentioning that similar topologies have appeared in the literature, e.g. as an independently controlled neutral leg for three-phase four-wire inverters in (Zhong and Hornik, 2013b; Liang et al., 2009), but the feature of eliminating CM currents has not been explored in the literature, to the best knowledge of the authors.

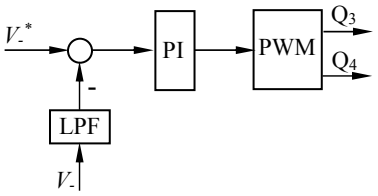


Figure 5.9: Controller for the neutral leg.

5.3.2 Operation Principles

As the conversion leg is connected to the grid, it is mainly used to exchange power between the DC side and the power grid. The operation of the conversion leg is the same as that of conventional half-bridge converters and hence, many strategies developed for conventional half-bridge converters (Srinivasan and Oruganti, 1998) can be directly applied here. Both current control and voltage control strategies can be implemented. It is worth mentioning that there is no restriction on the direction and angle of the grid current. Accordingly, both real and reactive power can be exchanged. If the control strategy is designed to be equipped with grid-support functions (Zhong and Hornik, 2013b), the converter can take part in the regulation of the grid voltage via exchanging the right amount of current (power) with the grid.

The operation of the neutral leg is independent from that of the conversion leg. As a result, the conversion leg can be designed according to its objectives to achieve the desired performance. One objective of the neutral leg is to balance the voltages across the split capacitors, which can be achieved by measuring the two voltages and fed into the controller. Another objective is to provide the return path of the DC current I. This can be naturally achieved when the DC voltages are stable. According to the Kirchhoff's law, the only path for the return DC current is the neutral leg because the DC capacitors are incapable of providing any DC currents and there is stringent requirement on the DC component in the grid current.

5.3.3 Control Design

5.3.3.1 Control of the neutral leg

The function of the neutral leg is to maintain a balanced voltage across the split capacitors and to provide a current path for the DC component. This is the same for both the

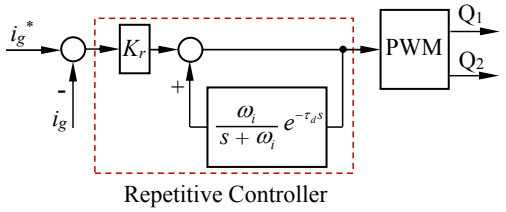


Figure 5.10: Controller for the conversion leg.

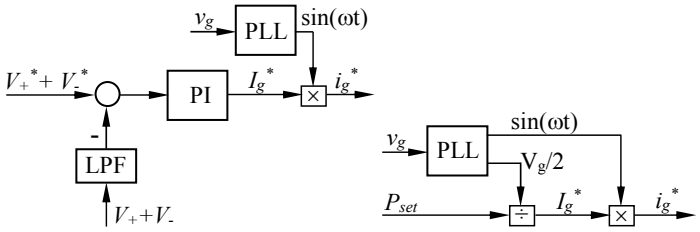


Figure 5.11: Generation of i_g^* for unity power factor (a) when operated as rectifiers and (b) when operated as inverters.

rectification mode and the inversion mode so the controller designed can be used for both modes. Assume that the DC-bus voltage is maintained by the converter in the rectification mode and is determined by the DC bus supply in the inversion mode. Then balancing the voltages of the split capacitor can be achieved by regulating either the voltage V_+ or V_-. In this chapter, regulating V_- is chosen.

In order to maintain the voltage V_-, a simple PI controller can be adopted, as shown in Figure 5.9. The voltage V_- is measured and fed through a low-pass filter (LPF) to extract the DC component. Here, the hold filter $H(s) = \frac{1-e^{-Ts/2}}{Ts/2}$ is adopted to remove the voltage ripples.

5.3.3.2 Control of the conversion leg

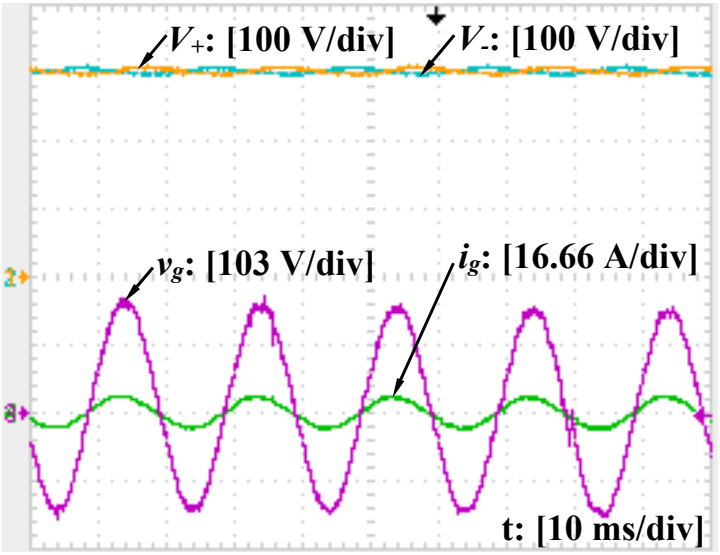
As a grid-tied converter, either the AC output voltage or the current of the converter should be regulated in order to facilitate the power exchange between the AC side and the DC side. Both current-controlled and voltage-controlled converters are widely used nowadays because they have their own benefits (Zhong and Hornik, 2013b). These can be applied to the investigated converter as well, without any limitations caused by the common AC and DC ground. In this chapter, the current-controlled mode is taken as an example to demonstrate the capability of exchanging real and reactive power between the AC side and

the DC side.

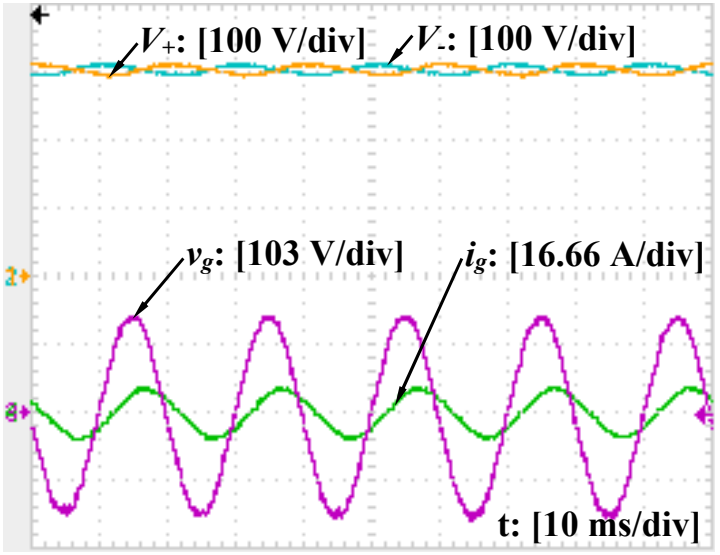
In order to regulate the grid-side current i_g, many candidate controllers, e.g., hysteresis controllers having a variable switching frequency and repetitive controllers having a fixed switching frequency, can be adopted (Zhong and Hornik, 2013b). In this chapter, the repetitive controller shown in Figure 5.10 is adopted because of the high performance in handling harmonics. The controller consists of a proportional controller K_r and an internal model. Here, $\omega_i = 2550$, $\tau = 0.02$ and $\tau_d = \tau - \frac{1}{\omega_i} = 0.0196$ s. The input to the controller is the error signal of the current with respect to the reference grid current i_g^*, of which the generation depends on the operation mode of the converter to achieve power balance between the AC side and the DC side. It is known that repetitive control is sensitive to frequency variations but this can be dealt with (Zhong and Hornik, 2013b).

When the converter is operated as a rectifier, the DC bus voltage $V_{DC} = V_+ + V_-$ should be regulated according to the load requirements at the desired value $V_{DC}^* = V_+^* + V_-^*$. This can also be easily achieved by a PI controller, as shown in Figure 5.11(a), where the DC-bus voltage is measured and fed through a low-pass filter to extract the DC component. The output of the PI controller is multiplied with the unity sinusoidal signal obtained through a phase-locked-loop (PLL) to form the grid current reference i_g^*. When the unity sinusoidal signal is in phase with the grid voltage, the unity power factor is achieved. The reactive power can be adjusted via changing the phase of the unity sinusoidal signal. Once the grid current reference is generated, the grid current controller shown in Figure 5.10 is able to track it.

When the converter is operated as an inverter, the voltage V_+ is given. In this case, the power injected to the grid can be controlled. For a given real power P_{set}, the corresponding peak grid current $I_g^* = \frac{P_{set}}{V_g/2}$. Multiplying it with the unity sinusoidal signal obtained through a phase-locked-loop (PLL), the grid current reference i_g^* can be formed, as shown in Figure 5.11(b). Similarly, when the unity sinusoidal signal is in phase with the grid voltage, the unity power factor is achieved. The reactive power can be adjusted via changing the phase of the unity sinusoidal signal. Once the grid current reference is generated, the grid current controller is able to track it.



(a)



(b)

Figure 5.12: Steady-state performance (rectification mode): (a) with the unity power factor; (b) with a non-unity power factor.

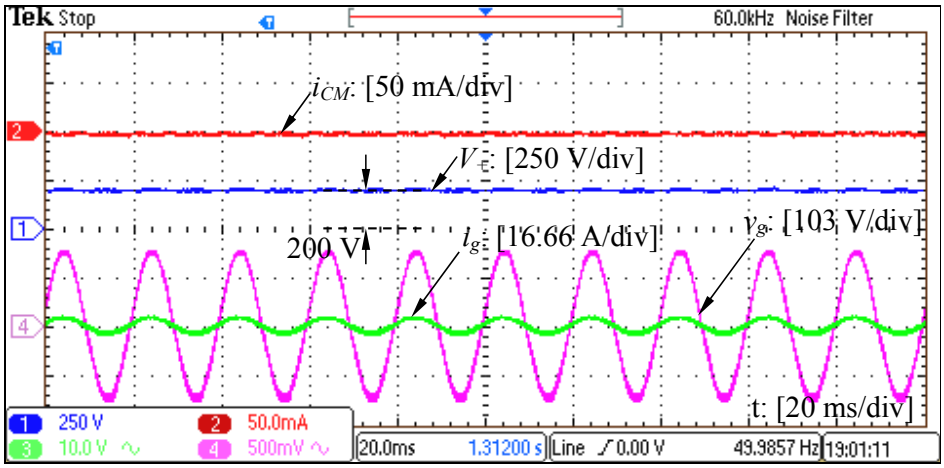
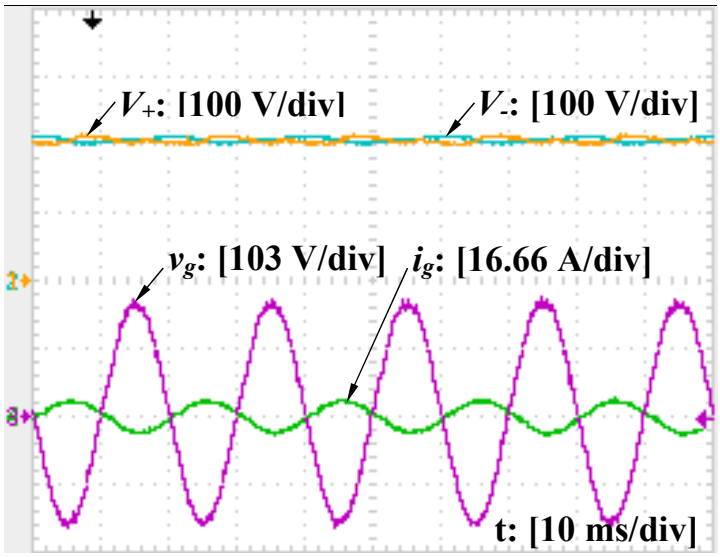


Figure 5.13: Measured CM current (rectification mode).

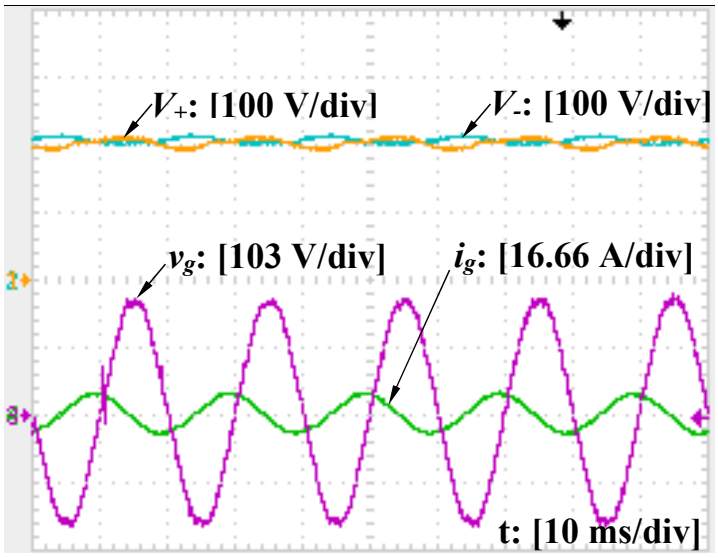
5.4 Experimental Results

In order to demonstrate the operation of the converter, an experimental rig was assembled in the laboratory. The main parameters of the system used in experiments are chosen as $V_g = 110\sqrt{2}$ V, $f = 50$ Hz, $L_g = 4.4$ mH, $L_N = 2.2$ mH and $C_+ = C_- = 1120$ μF. The four switches are operated at 20 kHz. As discussed in Chapter 4, it is possible to significantly reduce the total capacitance. However, the main focus of this chapter is to discuss the converter's capability of reducing CM currents, which is not affected by the adopted capacitance, and the components used for experiments are not optimized for small capacitance. During the experiments, both rectification and inversion modes were tested. In the rectification mode, a 470 Ω resistor was applied as the load of the converter.

For the rectification mode with the control strategies shown in Figure 5.10 and Figure 5.11(a), the results shown in Figure 5.12 demonstrates the steady state performance of the system for both the unity power factor case and a non-unity power factor case. The grid current was well regulated to be clean and the output voltage V_+ was maintained closely around its reference value 300 V. According to the recorded experimental data, the THD of the grid current is always lower than 4%. Since no special methods are used to improve the power quality of the grid current, the THD is already low enough. Also, the DC voltage V_- was well controlled to be close to V_+ by the neutral leg for the unity power factor case as shown in Figure 5.12(a). For the non-unity power factor case, the grid current i_g was not in phase with the grid voltage as shown in Figure 5.12(b), which is expected.



(a)



(b)

Figure 5.14: Steady-state performance (inversion mode): (a) unity power factor; (b) non-unity power factor.

Although the grid current was changed, the DC voltages V_+ and V_- were regulated well around 300 V, with slightly increased ripples. As a result, the converter is able to draw real and reactive power from the grid but without significantly affecting the regulation of the DC-bus voltage. In order to verify the system performance of reducing CM currents, a 0.47 μF capacitor is connected as the parasitic capacitor and the current flowing through this capacitor is measured and shown in Figure 5.13. Indeed, the CM current i_{CM} is almost completely eliminated.

For the inversion mode, a diode bridge rectifier cascaded with a variac was built up to establish V_+ at 200 V. With the control of the neutral leg, the voltage V_- was established to be around 200 V as well. Then, the investigated converter was tested in the inversion mode for both the unity power factor case and a non-unity power factor case. The controller in Figure 5.10 and 5.11(b) were applied in this mode. As shown in Figure 5.14(a), the grid current and grid voltage were exactly 180° out of phase with each other when the converter was operated in the unity power factor case. As a result, the power sent to the grid is purely real power. When the power factor was non-unity, the power sent to the grid contains reactive power, as shown in Figure 5.14(b). The grid current is always clean, with the given phase difference.

5.5 Summary

Following the proposed ρ-converters with significantly-reduced capacitance in Chapter 4, it has been shown that ρ-converters are also able to reduce CM currents without an isolating transformer for grid-tied converters because of the provision of a common AC and DC ground to bypass the parasitic capacitance and a suitable control strategy to decouple the control of the two legs in the converter. Because the controllers of the two legs are independent from each other, the controllers can be tailored to improve their performance according to their own objectives. Two simple controllers are designed as an example for the two legs, respectively, to demonstrate the operation of the converter. Importantly, the operation of the converter as an inverter has also been demonstrated in this chapter. Experimental results have demonstrated that the converter is able to bidirectionally exchanging both real power and reactive power with the grid while almost eliminating CM currents.

Chapter 6

Operation of the ρ-converter as a Self-synchronised Synchronverter with Reduced Input Current Ripples

The main focus of this chapter is to investigate the inversion mode of the ρ-converter developed in Chapters 4 and 5. The ρ-converter is controlled as a grid-tied PV inverter. It again consists of one neutral leg and one inverter leg. The presence of the neutral leg enables the direct connection between the ground of PV panels and the earth. Two main benefits are then obtained. First, the common mode currents are completely eliminated because the stray capacitors between the PV panels and the grid neutral line are bypassed. Another benefit is the voltage of the PV is only required to be higher than the peak value of the grid voltage, which is same as that of conventional full bridge inverter. In addition, the synchronverter technology designed for three-phase inverters is extended to a single-phase case to design the controller of the inverter leg. As a result, the investigated inverter becomes more grid-friendly. The control of the two legs are independent with each other, which means the controller design much easier. The performance of the whole system is evaluated in detail with the provided real-time simulation results.

6.1 Introduction

Driven by the penetration of photovoltaic (PV) systems, a lot of advanced technologies regarding PV panels and their operation in grid-connected modes are developed in the last

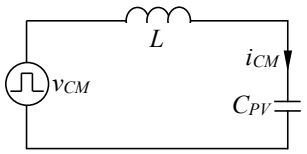


Figure 6.1: Generic equivalent circuit for CM current path

few years. Due to large stray capacitors between PV panels and the ground, PV systems are stuck with high common mode (CM) currents, which reduce the system efficiency and cause safety issues like electric shock. In order to eliminate the leakage currents, a galvanic isolation transformer is normally put between the panels and the grid. But the adoption of line frequency transformers reduces power density of the whole system and increases manufacturing costs. As a result, transformerless inverter topologies have attracted more and more attention in PV systems.

However, the absence of transformers may lead to high CM currents flowing through parasitic capacitors. Figure 6.1 illustrates a generic equivalent circuit for the CM current path, which is formed by CM voltage source v_{CM}, filter L and parasitic capacitor C_{PV}. The voltage v_{CM} is generated because of high frequency power switches. If the switching frequency is high enough, the CM current i_{CM} can be very large even if the parasitic capacitor C_{PV} is relatively small. In general, the CM current can be reduced through either mitigating the CM voltage v_{CM} (Ogasawara et al., 1998; Cavalcanti et al., 2010; Kerekes et al., 2011; Yang et al., 2012), increasing impedance L (Von Jouanne et al., 1998; Dong et al., 2012a), or providing another path for the CM current (Dong et al., 2012a; Xiao and Xie, 2012).

In this chapter, a transformerless PV inverter based on the conventional half bridge inverter is discussed. The inverter consists of one neutral leg and one inverter leg. Thanks to the neutral leg, the ground of the PV panels can be directly connected to the grid neutral line. Accordingly, the common mode current is completely eliminated so that transformers can be removed. Moreover, the DC input voltage of the inverter is only required to be higher than the peak value of the grid voltage, which is the same as that of conventional full bridge inverter. For the inverter leg, the concept of controlling three-phase inverters to mimic synchronous generators (Zhong and Weiss, 2011a; Zhong et al., 2014) is extended to a single-phase case. This makes the investigated inverter more grid-friendly. As a result, the investigated inverter can be a competitively complete solution to grid-tied PV inverter.

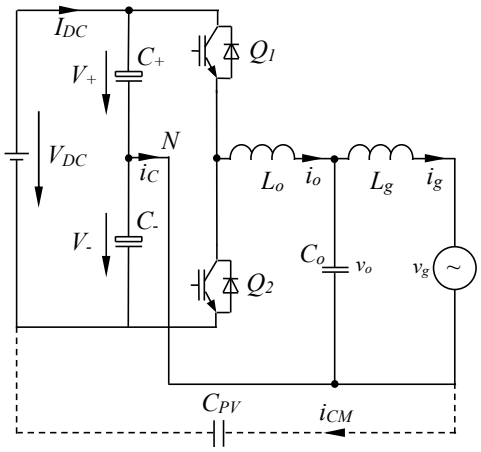


Figure 6.2: The topology of conventional half bridge inverter.

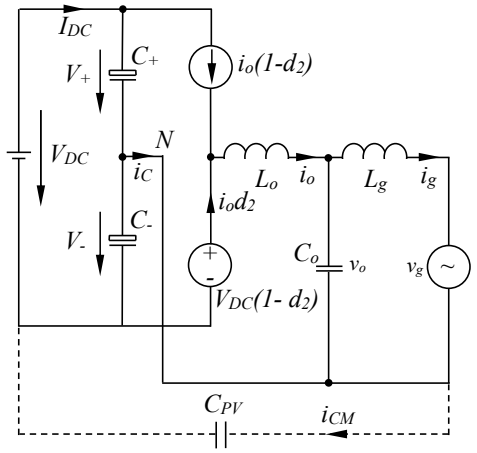


Figure 6.3: Average circuit model of conventional half bridge inverter.

The rest of the chapter is organised as follows. The operation of the conventional half bridge inverter is first reviewed in Section 6.2. In Section 6.3, the topology of the investigated transformerless inverter is given and then its operation principles together with control methods are discussed in detail. The associated control strategies for the inverter leg are developed in Section 6.4 and real-time simulation results are presented in Section 6.5, with summary made in Section 6.6.

6.2 Operation of Conventional Half Bridge Inverter

As a solution to transformerless PV inverters, the conventional half bridge inverter shown in Figure 6.2 has several advantages such as fewer power switches, reduced common mode

currents and relatively low costs. However, it suffers from high input voltage requirement, which is recognised as its main drawback (Gu et al., 2013). In this section, the operation of the conventional half bridge inverter is reviewed. In order to facilitate the analysis, the average circuit model of the half bridge inverter is first built. Assume that V_+ and V_- are the voltages across the capacitors C_+ and C_- with respect to the neutral point N and the negative point of the DC bus, respectively. Then the DC input voltage is

$$V_{DC} = V_+ + V_-.$$

Also, assume the output current of the inverter is sinusoidal

$$i_o = I_o \sin(\omega t + \varphi) \tag{6.1}$$

without any harmonics and the grid voltage is

$$v_o = V_o \sin \omega t,$$

where V_o and I_o are the peak values of the output voltage and output current, respectively, and ω is the angular line frequency. Because the two switches are operated in a complementary way, the average circuit model of the half bridge inverter can be obtained as shown in Figure 6.3. The switches Q_1 and Q_2 are replaced by a current source $i_o(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, where d_2 is the duty cycle of Q_2 and can be given by

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_o}{V_{DC}} \sin \omega t$$

as demonstrated in (Srinivasan and Oruganti, 1998) because the switching frequency is much higher than the line frequency.

6.2.1 Common Mode Current Reduction

The voltage across the parasitic capacitor is clamped by the voltages across DC capacitors. This is because the grid neutral line is directly connected to the midpoint of the DC bus. In this case, most of the high frequency common mode currents would flow through the DC capacitors but not the parasitic capacitors. Although low frequency components may still

exist, the common mode currents have been reduced to several mA, which is far below the 300 mA limit.

6.2.2 Output Voltage Range

In order to ensure the successful boost operation, each of the voltages across both capacitors must be higher than output voltage, which means

$$V_+, V_- > V_o.$$

In light of this, the required DC-bus voltage should be doubled that of conventional full bridge inverter. A natural solution is to put two DC sources in parallel with the split capacitors. In this case, the requirement on the input DC voltage is the same as that of conventional full bridge inverter. However, the requirement on the additional power source leads to increased system costs. Also, the balance of the two power sources can be a serious problem in real applications. It is also worth mentioning that the DC power source can not be put across any one of the capacitors if only one power source is present. The system fails to work properly in this case because DC capacitors are not able to provide the return DC input current.

6.3 The Investigated Transformerless Inverter

6.3.1 The Topology of the Investigated Inverter

The investigated transformerless inverter is shown in Figure 6.4, which consists of one neutral leg and one inverter leg. The investigated topology can be formed by adding the neutral leg into the conventional half bridge inverter. The added neutral leg consists of two switches and one inductor. The two switches are connected in parallel and then put between the positive and negative lines of the DC bus. The neutral inductor is put between midpoints of the switches and the split capacitors. The main objectives of the neutral leg are to balance the voltages of the capacitors and provide the return path for the DC input current. On the other hand, the inverter leg is used to generate AC output voltage in high power quality and to control the reactive and active power exchange between the PV and

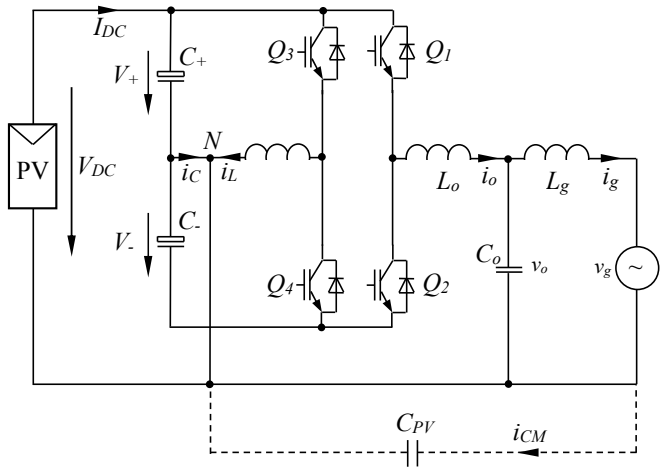


Figure 6.4: The topology of the investigated inverter.

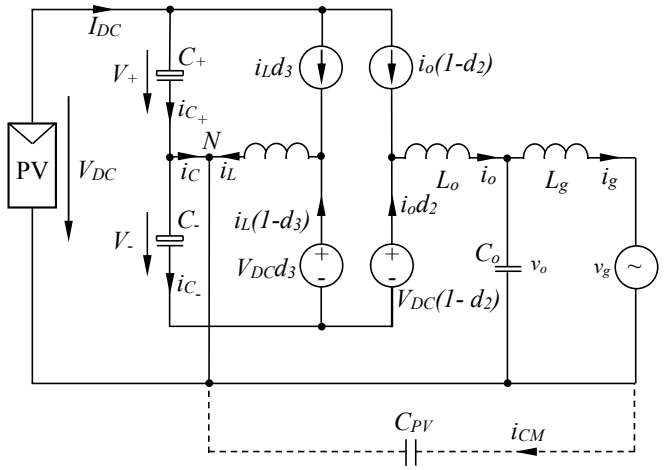


Figure 6.5: Average circuit model of the investigated inverter.

the grid. Note that the inverter leg can be operated as done for conventional half bridge inverter because the control of the neutral and the inverter leg are independent.

6.3.2 Operation Principles of the Neutral Leg

Similarly, the average model of the investigated inverter can be obtained as shown in Figure 6.5, where $d_3 = \frac{V_-}{V_{DC}}$ is the duty of the switch Q_3. According to the Kirchhoff's law, there is

$$i_C + i_L = I_{DC} - i_o. \tag{6.2}$$

The right part of the equation is the combination of a DC component plus an AC component. If the left part, the sum of i_C and i_L, can provide this combined current then the system can work properly. As well known, DC capacitors can not provide DC currents so that i_C does not contain any DC components. That is why the conventional half bridge inverter can not work when the PV is connected to any one of the DC capacitors. It is also preferred that i_C can be as small as possible so that the voltage ripples on the DC capacitors can be small. Fortunately, in the investigated inverter, another component i_L is provided, which can be DC or AC according to different control strategies of the neutral leg. As a result, (6.2) can be satisfied if

$$i_L = I_{DC} + i_o - i_C.$$

Either controlling $i_C = 0$ or $i_L = I_{DC} + i_o$ can achieve this. Obviously, the most effective way is to control i_C to 0, which also features less calculation and measurement work.

In order to enable the current control, a stable DC voltage on the capacitor C_- is needed. The voltage can be regulated to be higher and lower values, respectively, via increasing and decreasing the current i_{C_-}. Again, according to the Kirchhoff's law, there is

$$i_{C_-} = i_{C_+} - i_C. \tag{6.3}$$

If the output voltage of the PV is supposed to be absolutely direct without any low frequency ripples, then $i_{C_+} = 0$ for low frequency components. Consequently, (6.3) becomes

$$i_{C_-} = -i_C.$$

Obviously, controlling i_C can regulate the voltage on the capacitor C_-. As a result, (6.2) can be realised with the help of the neutral leg.

6.3.3 Control of the Neutral Leg

One of the main objectives of the neutral leg is to provide the return path for the output current i_o. In order to achieve this, i_C is regulated to be around zero so that all the return current is provided by the neutral leg. For this purpose, i_C should be measured as a feedback. Many current controller such as hysteresis controllers (Tilli and Tonielli, 1998) that have a variable switching frequency and repetitive controllers (Hornik and Zhong, 2011a)

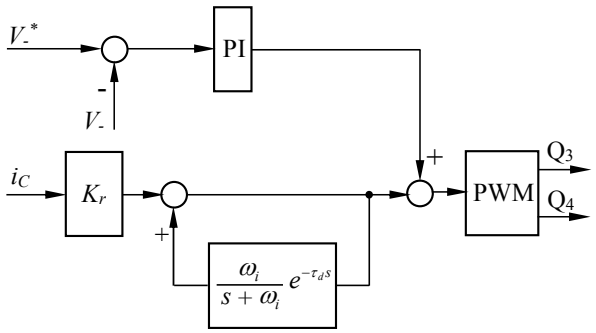


Figure 6.6: Controller for the neutral leg

that have a fixed switching frequency, can be applied here to squeeze the current i_C. Because of the excellent harmonic rejection performance, the repetitive controller shown in Figure 6.6 is used. The controller consists of a proportional controller K_r and an internal model:

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where K_r and τ_d are designed based on the analysis in (Hornik and Zhong, 2011a; Weiss and Hafele, 1999) as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\, sec,$$
$$K_r = \omega_i L_r,$$

in which L_r is the neutral line inductor and $\omega_i = 2550$, $\tau = 0.02\, sec$.

In order to enable the current control, a stable DC voltage on the capacitor C_- is needed. In this sense, a voltage loop is put in parallel with the current loop. They are added up before sending to the PWM so that the two loops are decoupled, which means the control design much easier and the resulting high performance of the system can be obtained.

6.3.4 Performance Evaluation

6.3.4.1 CM current elimination

As analysed before, although the common mode current in conventional half bridge inverter has been reduced a lot, it still suffers from the component caused by half of the DC-bus voltage. For many other typical transformerless topologies such as H5, HERIC and H6,

the disconnection between the AC ground and DC ground are incomplete so that high frequency common mode current may still exist.

For the investigated topology, the DC ground and AC neutral line are directly connected together. As a result, the common mode current is completely eliminated as the parasitic capacitors are actually short circuited.

6.3.4.2 Input voltage requirement

As the DC input is connected to the capacitor C_+, the required DC input voltage is only half of the one required by conventional half bridge inverter. In other words, the required DC input voltage is the same as that of the full bridge inverter. If two stages are used, this reduces the voltage stress on the DC/DC converter between PV panels and the transformerless inverter. If single stage is used, this is able to reduce the minimum number of the PV panels, which are put in series to obtain enough DC input voltage.

6.4 Control of the Inverter Leg as the Synchronverter

In order to make the PV inverter to be more grid-friendly, the inverter leg is controlled to be the synchronverter as proposed in (Zhong and Weiss, 2011a). There are two operating modes defined in the operation of the single-phase synchronverter (SPSV), the autonomous mode and the grid connected mode. In the autonomous mode, the SPSV generates the nominal voltage at the nominal frequency. The real and reactive power generated depend on the local load connected. In the grid connected mode, the SPSV could be controlled to generate the required amount of both real and reactive power, which includes the effects of the grid frequency and grid voltage by droop control mechanisms, or excludes those effects and generates the exact set-points of power.

The three-phase self-synchronised synchronverter proposed in (Zhong et al., 2014) is applied to a single-phase case in this chapter. Like the three-phase synchronverter, it will show later that the SPSV has several mixed control modes when it operates grid-connected. The set modes are to generate required set point P_{set} (P-mode) and/or Q_{set} (Q-mode). The frequency droop mode (F-mode) takes into account the frequency difference in the control loop to decide the amount of the real power generated. The voltage droop mode (V-mode)

Table 6.1: Switches and corresponding control modes

S_C	Mode	S_P	Mode	S_Q	Mode
1	Synchronisation	ON	P-mode	ON	V-mode
2	Normal	OFF	F-mode	OFF	Q-mode

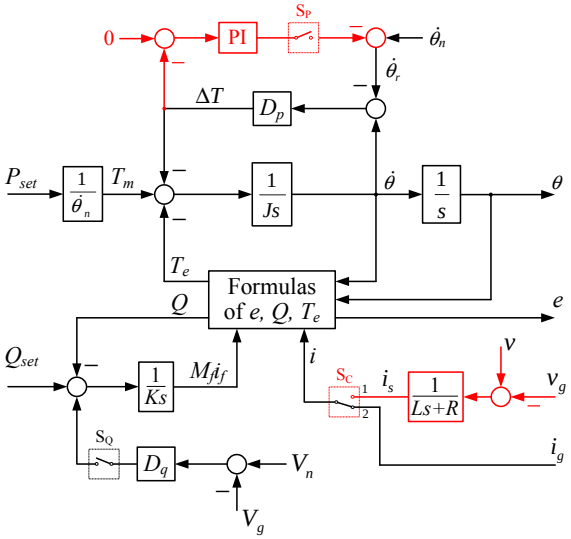


Figure 6.7: Controller for the inverter leg.

takes into account the voltage difference to decide the amount of reactive power delivered. Besides, there is a stage called the synchronisation stage when the SPSV operates in normal mode. During this stage, the output AC voltage is controlled to be synchronised with the grid voltage so that it is safe to connect the SPSV to the grid. Three switches S_P, S_Q, and S_C shown in Figure 6.7 define all the aforementioned control modes. Their functional details are given in Table 6.1.

6.4.1 Real Power Control Channel and the Frequency Droop Control Mode

The power angle is controlled by regulating the mechanical torque in the case of an synchronous generator. In SPSV, obviously the real mechanical torque is not available because it is a virtual machine. Instead, the virtual mechanical torque T_m is calculated from the power command P_{set}. Taking into account the fact that normal operation usually has grid frequency not diverged too much from its nominal value, i.e. $\dot{\theta} \approx \dot{\theta}_n$ in most of the time,

becomes

$$T_m = \frac{P_{set}}{\dot{\theta}} \approx \frac{P_{set}}{\dot{\theta}_n}, \tag{6.4}$$

where with $\dot{\theta}_n$ is the nominal grid frequency. That T_m is then fed into the control system as the set point for the electrical torque T_e. T_m is not a controllable parameter in this case, although the control objective is still similar i.e. regulating $\dot{\theta}$ to track $\dot{\theta}_g$ so that $\delta = \theta - \theta_g$ could be settled in the value that results $P_g = P_{set} - P_l$. Different power demands P_{set} will cause δ to settle in different values. Hence a compensator is designed on the top of the mechanical channel to regulate $\dot{\theta}$.

The details about how to design this loop can be found in (Zhong et al., 2014). However, it is still worth mentioning that, in droop modes, the electrical power generated no longer follows the set point, but taking into account the effect of $\triangle T$ defined by the droop coefficient D_p. For example, if $\dot{\theta}_g$ is higher than the nominal frequency $\dot{\theta}_n$, i.e. grid is under-load, then the controller will control the SPSV to generate less power than the set point P_{set} or even negative power (if the power part of the SPSV is designed with an energy storage mechanism). The power difference $\Delta P = \dot{\theta} \triangle T$ depends on D_p predefined and the dropped frequency $\Delta\dot{\theta} = \dot{\theta} - \dot{\theta}_n$ (Zhong and Weiss, 2011b).

6.4.2 Reactive Power Control Channel and the Voltage Droop Control Mode

The structure of the reactive control channel is shown in the lower part of the Figure 6.7. Again, the design of this loop is similar to the three-phase case, which can be found in (Zhong et al., 2014). In operation, this control channel preserves the characteristics of the original synchronverter. When the switch S_Q is off, $M_f i_f$ is generated depending on the tracking error between Q_{set} and Q only, via the integrator with the gain $1/K$. Therefore in the steady state the integrator can eliminate the tracking error , which results Q to track the set point Q_{set} regardless of the voltage difference between V_n and V_g. This mode is the Q-mode defined in the Table 6.1. When the switch S_Q is on, the voltage droop is enabled, the error $\triangle V = V_n - V_g$ is taken into account to generate $M_f i_f$. Therefore in the steady state Q does not track Q_{set} but keeping a steady state error depending on the voltage difference $\triangle V$.

Table 6.2: Parameters of the System

Parameters	Values
DC input voltage	200V
Grid voltage (RMS)	110 V
Line frequency	50 Hz
L_s	2.2 mH
DC-bus capacitance C_+	5000 μF
DC-bus capacitance C_-	5000 μF

6.4.3 Synchronisation Stage

Before the SPSV is connected, the voltage v must be controlled to be synchronised with the grid voltage v_g, The self-synchronised strategy (Zhong et al., 2014) to control P_g and Q_g to zero is adopted here for synchronisation. As shown in Figure 6.7, S_C is in position 1 to direct the virtual current i_s into the controller control loop; S_P and S_Q are switched on with $P_{set} = 0$ and $Q_{set} = 0$ to define the control objective. The virtual current i_s flowing on the virtual impedance R and L then could be used to replace the grid current in the calculations of T_e. The feedback Q is replaced by Q_g calculated from the grid voltage v_g and the synchronisation current i_s. In the steady state, even with the the local load connected, the zero power of P_g and Q_g implies v and v_g are synchronised, and the SPSV is entitled to be connected to the grid.

6.5 Real-time Simulation Results

Real-time simulations were carried out with the Opal-RT OP5600 to test the investigated inverter and the solver used was ode4 (Runge-Kutta) with a fixed step size of 6 μs. The parameters of the system are given in Table 6.2. The parameters of the PI controller for the voltage V_- are $K_P = 0.1$, $K_I = 10$ and the gain of the repetitive controller for neutral current i_C are $K_r = 20$.

During simulations, the neutral leg was first started before enabling the synchronverter leg. As a result, the voltages across the split capacitors can be built so as to make sure the successful operation of the synchronverter leg. The controller operation modes, including direct active and reactive power control (P-mode, Q-mode), frequency droop control (F-mode), and voltage droop control (V-mode) were investigated. The grid voltage frequency

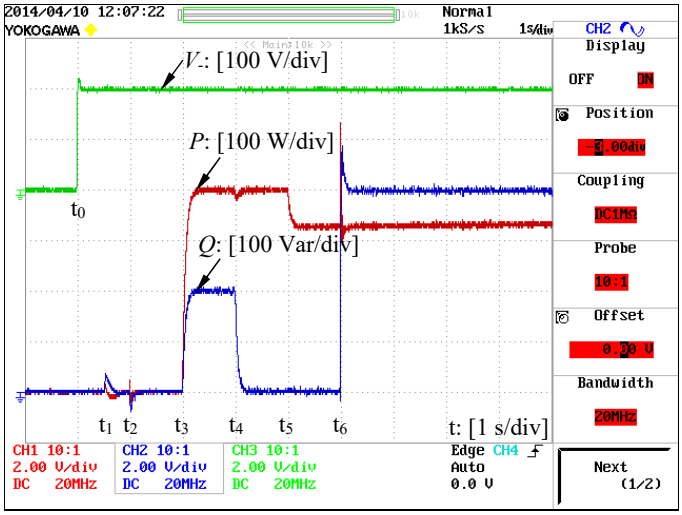


Figure 6.8: Real power P, reactive power Q and DC voltage $V_{\_}$.

$f_g = 50$ Hz and amplitude $V_g = 1.02V_n$ were set at the beginning in order to test the system performance when enabling droop control. During the simulations, the grid voltage frequency and amplitude were varied to test the droop control modes of the SPSV. The sequence of events are as follows

1) Start the neutral leg at $t_0 = 0$ s

2) Start the inverter leg with the synchronisation command at $t_1 = 0.5$ s .

3) Connect the inverter to the grid at $t_2 = 1$ s.

4) Apply the set point $P_{set} = 400$ W and $Q_{set} = 200$ Var at $t_3 = 2$ s.

5) Enable the $F-$mode and $V-$mode by, respectively, switching off S_P and S_Q at $t_4 = 3$ s.

6) Increase the grid frequency to $f_g = 50.02$ Hz at $t_5 = 4$ s.

7) Drop the grid voltage amplitude to $V_g = 0.98V_n$ at $t_6 = 5$ s.

The simulation results are shown in Figure 6.8. With the help of the neutral leg, the voltage across the capacitor $C_{\_}$ was well maintained to be balanced with the DC input voltage regardless of the modes of the SPSV. For the synchronverter leg, there is no problem connecting SPSV from the grid at $t = 1$ s. The real and reactive power shown in Figure 6.8 were regulated back to zero after connecting to the grid. This is because $P_{set} = 0$ and $Q_{set} = 0$ before $t = 2$ s. The response of the synchronverter was fast and smooth when $P_{set} = 400$ W and $Q_{set} = 200$ Var were applied at $t = 2$ s.

When the $F-$mode and $V-$mode were enabled at $t = 3$ s, the grid voltage V_g was 2%

higher than V_n. Because D_q was set to drop 100% of reactive power (i.e. 1000 Var dropped) when the grid voltage increases by 10%, the reactive power expected to be dropped in this case was

$$\triangle Q = -1000 \times \frac{2}{10} = -200\text{Var} \tag{6.5}$$

from the set point. This expected value matches well with the simulation result shown in Figure 6.8. As the grid frequency is at its nominal value, the real power was maintained to its set point even after the the $F-$mode and $V-$mode were enabled.

The simulation continued with the conditions when the grid voltage changed to higher frequency i.e. $f_g = 50.02$ Hz at $t = 4$ s and then lower voltage $V_g = 0.98V_n$ at $t = 5$ s. The inverter leg was still controlled in F-mode and V-mode. The response of the system was again fast and smooth. Similar to the explanation above, the changes of real and reactive power were expected to be $\triangle P = -70$ W and $\triangle Q = 400$ Var from their previous values. These expected values again match well with the simulation results shown in Figure 6.8.

6.6 Summary

The operation of ρ-converters developed in Chapter 4 and 5 as a PV inverter has been investigated in this chapter. The inverter consists of one neutral leg and one inverter leg. With the help of the neutral leg, the DC input voltage can be the same as that of conventional full bridge inverter, which makes the whole system easier to be implemented. More importantly, the neutral leg facilitates the direct connection between the ground of the PV and the grid neutral line. As a result, the CM current is completely eliminated. Apart from the neutral leg, the inverter leg is controlled as the synchronverter so that the whole inverter becomes more grid-friendly. Real-time simulation results have verified the performance of the investigated system.

Chapter 7

Adding a Capacitor to Bridge Rectifiers for Reduction of Low-frequency Voltage Ripples and High-frequency CM Voltages

In this chapter, an auxiliary capacitor is added to a conventional full-bridge rectifier to provide a path for low-frequency ripple currents and the high-frequency CM current. Compared to the ρ-converters in Chapters 4, 5 and 6, the proposed rectifier has much lower voltage stress on active switches and higher DC output voltage. All of these merits make the proposed rectifier more suitable for high voltage applications. Experimental results are presented to demonstrate the excellent performance of the proposed rectifier in reducing the ripples, the common-mode currents and the total capacitance needed, with comparison to the conventional bridge rectifier without the auxiliary capacitor.

The operation of the proposed rectifier is split into the operation of a half-bridge rectifier and a DC-DC converter so that the ripple energy can be diverted from the DC-bus capacitor to the auxiliary capacitor. Hence, the DC-bus capacitor can be significantly reduced while maintaining very low voltage ripples on the DC bus because it is only required to filter out switching ripples. The auxiliary capacitor is designed to allow high voltage ripples because its voltage is not supplied to any load. Accordingly, the auxiliary capacitor can also be very small as well. As a result, the total required capacitance becomes very small. The reduction ratio of the total capacitance is significant, which makes it cost-effective to use

film capacitors instead of electrolytic capacitors. Because the operation of the proposed rectifier is similar to that of a half-bridge rectifier, the proposed rectifier inherits many features of half-bridge rectifiers, e.g. the same range of DC output voltage and simple drive circuits.

7.1 Introduction

Rectifiers are widely used to convert AC voltages into DC voltages. There are numerous kinds of topologies for such rectifiers (Zhong and Hornik, 2013b), among which the conventional full-bridge rectifier with four active switches is one of the most popular topologies. Full-bridge rectifiers often need an isolation transformer, at either high or low frequencies, to cut off the current path of common mode (CM) currents in order to avoid electric shock and to reduce electromagnetic interference (EMI) (Kerekes et al., 2011). However, isolation transformers lead to low power density and reduced power efficiency (Kerekes et al., 2011). Moreover, rectifiers often need bulky electrolytic capacitors to smooth the pulsating power, in particular, for single-phase systems (Wang et al., 2012; Krein et al., 2012; Wang et al., 2011). However, it is well known that the reliability of electrolytic capacitors can be a serious problem and almost one third of failures for power electronic systems are due to the failure of electrolytic capacitors (Wang et al., 2013).

In this chapter, through adding a small auxiliary capacitor into a full-bridge rectifier, both the isolation transformer and electrolytic capacitors can be removed. The capacitor is connected between the grid neutral line and the negative line of the DC bus. As a result, the added auxiliary capacitor is actually in parallel with the parasitic capacitors and provides a path for the CM current. Hence, the CM current can be considerably reduced and the isolation transformer can be removed while still maintaining the CM current at a low level. Moreover, the operation of the rectifier is changed to the operation of a half-bridge rectifier and a DC/DC converter so that the ripple energy originally flowing through the output capacitor is now diverted to the auxiliary capacitor. As a result, the DC-bus capacitance can be significantly reduced. At the same time, the auxiliary capacitor is designed to allow large voltage ripples because no loads are connected to the auxiliary capacitor. Hence, the auxiliary capacitor can be also very small. Although the number of capacitors is increased from

one to two, the total capacitance becomes much smaller and highly-reliable film capacitors instead of electrolytic capacitors can now be used.

The impact of adding the auxiliary capacitor with large voltage ripples is analysed in detail. Because the operation of the proposed rectifier is similar to that of the half-bridge rectifier, the proposed rectifier inherits many features of the half-bridge rectifier, e.g. the same range of the DC output voltage and simple drive circuits. As a result, the proposed rectifier is suitable for loads that are originally supplied by conventional half-bridge rectifiers. The two legs of the proposed bridge rectifier are independently controlled so there is no need to synchronise the driving signals for both legs, which simplifies the design of the driver circuits. One leg is responsible for the energy exchange between the AC side and the DC side and the other leg is responsible for diverting the ripple energy to the auxiliary capacitor.

The rest of this chapter is organised as follows. In Section 7.2, the conventional full-bridge rectifiers are analysed in terms of the need of an isolation transformer and bulky electrolytic capacitors. Then, the topology and operation principles of the proposed rectifier are given in Section 7.3, followed with detailed analysis on how to reduce the CM current and the capacitance. The control strategies are presented in Section 7.4 and the selection of the components are shown in Section 7.5. The impact of adding the auxiliary capacitor and changing the operation principles is analysed in Section 7.6. Experimental results are then provided to validate the system performance in Section 7.7, with summary made in Section 7.8.

7.2 Conventional Single-phase Full-bridge Rectifier

The conventional single-phase full-bridge rectifier is shown in Figure 7.1(a), with four power switches connected as two legs. The two switches on each leg are normally operated in complementary and the two legs are operated in complementary as well. The switches are operated at high frequencies to inject the right amount of current into the DC bus so that the DC-bus voltage is regulated. The power factor of rectifiers are often required to be close to 1. A lot of technologies have been developed to improve the performance of the rectifier from different aspects such as control strategies, modulation strategies, power

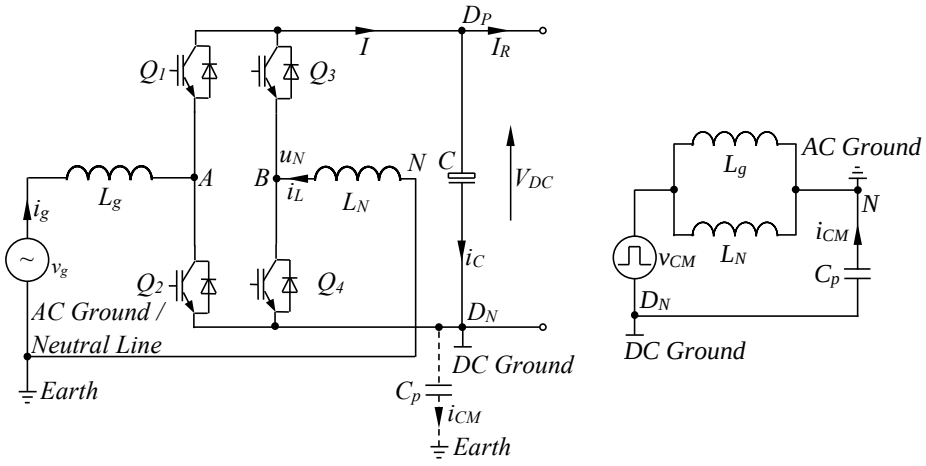


Figure 7.1: Conventional single-phase full-bridge rectifier: (a) topology; (b) equivalent circuit for analysing CM currents.

density, reliability and efficiency (Zhong and Hornik, 2013b; Kerekes et al., 2011; Wang et al., 2011).

7.2.1 The Need of an Isolation Transformer

The equivalent circuit for analysing the CM current of the conventional full-bridge rectifier is shown in Figure 7.1(b). As demonstrated in (Cavalcanti et al., 2010; Dong et al., 2012a; 2013b), the equivalent CM voltage is

$$v_{CM} = \frac{v_{AD_N} + v_{BD_N}}{2} + (v_{AD_N} + v_{BD_N})\frac{L_N - L_g}{L_N + L_g} \tag{7.1}$$

where v_{AD_N} and v_{BD_N} are the voltages between points A and D_N and between points B and D_N, respectively. The voltages v_{AD_N} and v_{BD_N} depend on both the system parameters and the modulation strategies (Hou et al., 2013; Hoseini et al., 2014).

Because of the parasitic capacitor C_p between the DC ground and the earth, a current loop is formed so the CM current i_{CM} appears. The impedance of the CM loop is

$$Z(s) = s\frac{L_N L_g}{L_N + L_g} + \frac{1}{sC_p} \tag{7.2}$$

from which the CM current can be found as

$$\begin{aligned} i_{CM} &= \frac{1}{s\frac{L_N L_g}{L_N+L_g}+\frac{1}{sC_p}} v_{CM} \\ &= \frac{sC_p}{s^2\frac{L_N L_g C_p}{L_N+L_g}+1} v_{CM}, \end{aligned} \tag{7.3}$$

which could lead to reduced system efficiency, high electromagnetic emissions and safety issues (Kerekes et al., 2011; Lopez et al., 2010). In order to limit this current, either a low-frequency or a high-frequency isolation transformer is often used, which cuts off the flowing path of the i_{CM} by providing a galvanic isolation between DC and AC sides of rectifiers (Kerekes et al., 2011; Gu et al., 2013; Lopez et al., 2010). Removing isolation transformers, of course, helps to improve system efficiency, power density and reliability. However, high level of the current i_{CM} would appear on the parasitic capacitor, which should be avoided as mentioned before.

7.2.2 The Need of Bulky DC-bus Electrolytic Capacitors

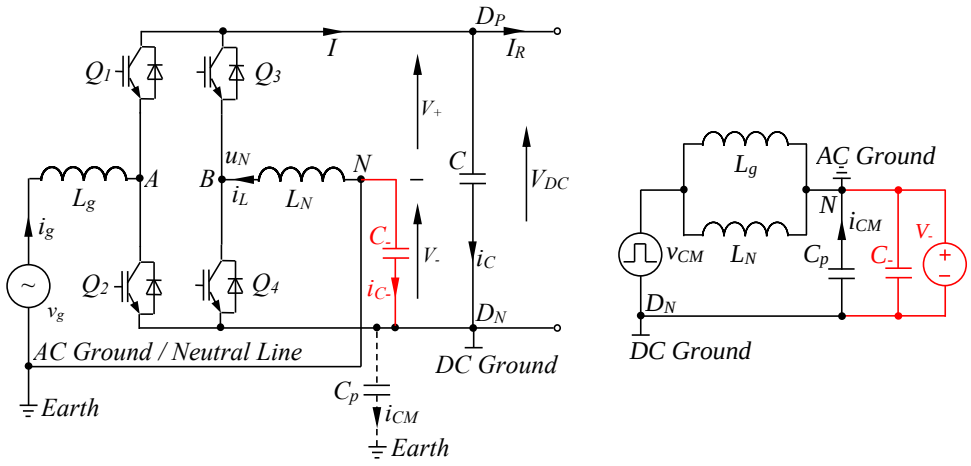
Assume that the grid voltage is

$$v_g = V_g \sin \omega t$$

where V_g is the peak value of the grid voltage and ω is the angular grid frequency. With the unity power factor, it can be assumed that the grid current is

$$i_g = I_g \sin \omega t$$

where I_g is the peak value of the grid current. As a result, the instantaneous input power $v_g i_g$ consists of a constant component $\frac{V_g I_g}{2}$ and a ripple component $-\frac{V_g I_g}{2}\cos 2\omega t$. Ideally, the power consumed by the DC load is constant, i.e. $\frac{V_g I_g}{2}$, when ignoring power losses, so an energy buffer is needed to store the ripple component. This is often achieved by using DC capacitors. Assume that all the ripple energy is stored in DC capacitors. Then the



(a) (b)

Figure 7.2: The proposed rectifier: (a) topology; (b) equivalent circuit for analysing CM current.

required DC capacitance is (Wang et al., 2012; Yao et al., 2012)

$$\begin{aligned} C &= \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)} \\ &\approx \frac{V_g I_g}{2\omega \triangle V_{DC} V_{DC0}} \end{aligned} \tag{7.4}$$

where V_{DCmax}, V_{DCmin}, $\triangle V_{DC}$ and V_{DC0} are the maximum, minimum, peak-peak and average values of V_{DC}, respectively. If $\triangle V_{DC}$ is required to be very small, the required capacitor C could be very large, which often reaches a level that only electrolytic capacitors are cost-effective to be used.

7.3 The Proposed Rectifier

7.3.1 Topology

The proposed rectifier is formed by adding a small auxiliary capacitor C_- into the conventional full-bridge rectifier between the neutral line N and the negative line D_N of the DC bus, as shown in Figure 7.2(a). Moreover, the operation of the bridge rectifier is changed: Q_1 and Q_2 are operated as a half-bridge rectifier, called the rectification leg, and Q_3 and Q_4 are operated as a DC/DC converter, called the neutral leg. They share the same neutral point N.

7.3.2 Operation Principle

For conventional full-bridge rectifiers, the two legs are operated in a complimentary way (Zhong and Hornik, 2013b). As a result, the control of the two legs are not independent. The main objectives of the two legs are to regulate the grid current and the DC-bus voltage. Note that the regulation of the DC-bus voltage can be indirectly achieved by injecting the right amount of the grid current. Hence, there is only one independent objective, i.e. the regulation of the grid current.

For the proposed rectifier, the two legs become independent from each other. They can now have their own objectives and the corresponding control strategies can be designed according to different objectives. The rectification leg is still used to regulate the grid current and to maintain the DC-bus voltage. The neutral leg can be used to achieve some other objectives, in addition to providing the return path of the grid current. One option is to divert the ripple energy from the DC bus to the auxiliary capacitor. This can be achieved by complimentarily operating the two switches of the neutral leg to absorb/inject the right amount of currents from/to the DC bus and the auxiliary capacitor. In order to make this happen, the average voltage across the auxiliary capacitor $V_{\_}$ needs to be regulated to a certain range.

7.3.3 Average Circuit Model

According to (Tymerski et al., 1989; Srinivasan and Oruganti, 1998), the average circuit model of the proposed rectifier can be built as shown in Figure 7.3. The switches Q_1 and Q_2 are replaced with a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, where d_2 is the duty cycle of Q_2. At the same time, the switches Q_3 and Q_4 are replaced with a current source $i_L(1-d_4)$ and a voltage source $V_{DC}(1-d_4)$, where d_4 is the duty cycle of Q_4.

Because the switching frequency is much higher than the line frequency, there are

$$v_g = V_{DC}(1-d_2) - V_{\_} \tag{7.5}$$

$$V_{\_} = V_{DC}(1-d_4). \tag{7.6}$$

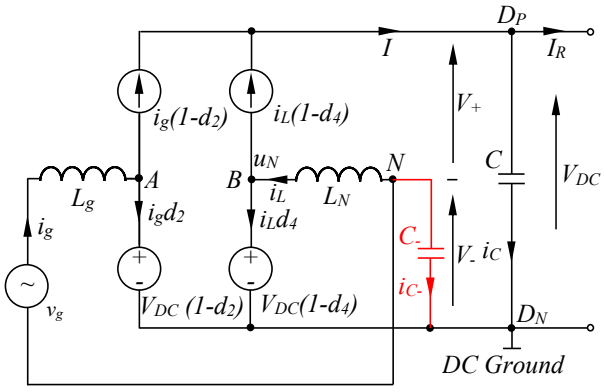


Figure 7.3: Average circuit model of the proposed rectifier.

As a result, the duty cycles of the Switch Q_2 and the Switch Q_4 can be found as

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t \tag{7.7}$$

$$d_4 = \frac{V_+}{V_{DC}}. \tag{7.8}$$

7.3.4 Reduction of the DC-bus Voltage Ripples

According to the Kirchhoff's law, there are

$$i_C = i_g(1-d_2) + i_L(1-d_4) - I_R \tag{7.9}$$

$$i_{C-} = -i_g - i_L = -I_g \sin \omega t - i_L \tag{7.10}$$

where i_C, i_{C-} and I_R are the currents flowing through the capacitor C, the capacitor C_- and the load, respectively, ignoring the switching-frequency components. Moreover, if the power losses are neglected, then the DC load current is

$$I_R = \frac{V_g I_g}{2V_{DC}}$$

because of power balance. Substituting (7.7)-(7.8) into (7.9), then

$$\begin{aligned} i_C &= i_g(1-d_2) + i_L(1-d_4) - I_R \\ &= (\frac{V_-}{V_{DC}} + \frac{V_g}{V_{DC}} \sin \omega t) I_g \sin \omega t + \frac{V_-}{V_{DC}} i_L - \frac{V_g I_g}{2V_{DC}} \\ &= \frac{V_- I_g}{V_{DC}} \sin \omega t - \frac{V_g I_g}{2V_{DC}} \cos 2\omega t + \frac{V_-}{V_{DC}} i_L \end{aligned} \tag{7.11}$$

where i_L is the current of the inductor L_N. Both capacitor currents could contain fundamental, second-order and other frequency components, which lead to voltage ripples across the capacitors C and C_- if not controlled properly.

In order to divert the ripple energy away from the capacitor C, it is required to force $i_C = 0$, or

$$i_C = \frac{V_- I_g}{V_{DC}} \sin \omega t - \frac{V_g I_g}{2V_{DC}} \cos 2\omega t + \frac{V_-}{V_{DC}} i_L = 0.$$

In other words, the current flowing through the inductor L_N should be

$$i_L = -I_g \sin \omega t + \frac{V_g I_g}{2V_-} \cos 2\omega t. \tag{7.12}$$

Substituting (7.12) into (7.10), the current flowing through the capacitor C_- becomes

$$i_{C-} = -\frac{V_g I_g}{2V_-} \cos 2\omega t, \tag{7.13}$$

which means the current i_{C-} mainly contains a second-order component. Because the voltage across the capacitor C_- is not connected to any load, it could be designed to have large voltage ripples with a small capacitor. Since i_C does not contain any low frequency currents, the capacitor C can be significantly reduced while still maintaining low voltage ripples. Although an auxiliary capacitor (C_-) is added, the total capacitance $C + C_-$ could be reduced considerably.

7.3.5 Operational Boundary

Because the voltage V_- and the current i_{C-} satisfies

$$i_{C-} = C_- \frac{dV_-}{dt},$$

there is

$$2V_- \frac{dV_-}{dt} = -\frac{V_g I_g}{C_-} \cos 2\omega t.$$

As a result,

$$V_-^2 = V_{-0}^2 - \frac{V_g I_g}{2\omega C_-} \sin 2\omega t, \tag{7.14}$$

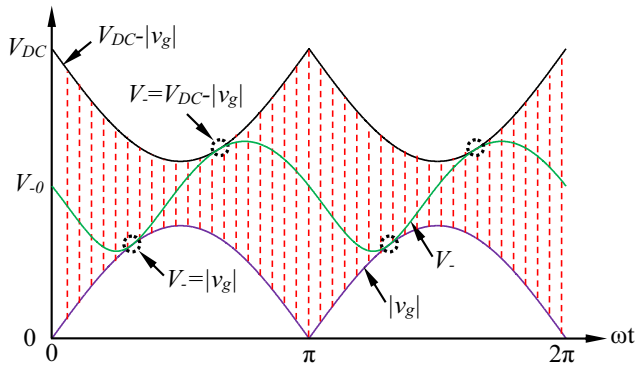


Figure 7.4: Range of the voltage V_- determined by the $|v_g|$ and $V_{DC} - |v_g|$.

where V_{-0} is the DC component of V_-. In order to ensure the boost operation of the rectifier, both the voltages V_+ and V_- should be higher than the grid voltage. As a result, both $V_- \geqslant V_g \sin \omega t$ and $V_+ = V_{DC} - V_- \geqslant V_g \sin \omega t$ for $0 \leqslant \omega t \leqslant \pi$ should be satisfied, which means

$$V_{DC} - V_g \sin \omega t \geqslant V_- \geqslant V_g \sin \omega t. \tag{7.15}$$

In this case, the operational range of the V_- is determined, which should be chosen within the part shaded by the dashed red lines shown in Figure 7.4. In the extreme case, the waveform of the voltage V_- is tangent to to the waveforms of both $V_{DC} - |V_g \sin \omega t|$ and $|V_g \sin \omega t|$. The voltage V_- then achieves its maximum allowed ripples, which means the capacitor C_- achieve its minimum value according to (7.14).

Because of $V_- \geqslant |V_g \sin \omega t|$, there is

$$V_-^2 \geqslant V_g^2 \sin^2 \omega t,$$

which means

$$\begin{aligned}
V_{-0}^2 - \frac{V_g I_g}{2\omega C_-} \sin 2\omega t &\geqslant V_g^2 \sin^2 \omega t \\
V_{-0}^2 - \frac{V_g I_g}{2\omega C_-} \sin 2\omega t &\geqslant V_g^2 \frac{1 - \cos 2\omega t}{2} \\
V_{-0}^2 - \frac{V_g^2}{2} &\geqslant -\frac{V_g^2}{2} \cos 2\omega t + \frac{V_g I_g}{2\omega C_-} \sin 2\omega t \\
V_{-0}^2 - \frac{V_g^2}{2} &\geqslant \lambda \sin(2\omega t - \arccos(\frac{V_g I_g}{2\lambda \omega C_-}))
\end{aligned} \tag{7.16}$$

where $\lambda = \sqrt{(\frac{V_g I_g}{2\omega C_-})^2 + (\frac{V_g^2}{2})^2}$.

As long as system parameters are determined, the left part of (7.16), i.e. $V_{-0}^2 - \frac{V_g^2}{2}$, is determined. Note that the right part of the (7.16) is time-varying in second-order frequency. In order to make sure that (7.16) is always satisfied, there is

$$V_{-0_{min}}^2 - \frac{V_g^2}{2} = \sqrt{(\frac{V_g I_g}{2\omega C_-})^2 + (\frac{V_g^2}{2})^2}, \tag{7.17}$$

where $V_{-0_{min}}$ is the minimum value of the V_{-0}. According to (7.14) and (7.17), the minimum value of the V_- can be given as

$$\begin{aligned} V_{-min} &= \sqrt{V_{-0_{min}}^2 - \frac{V_g I_g}{2\omega C_-}} \\ &= \sqrt{\frac{V_g^2}{2} + \sqrt{(\frac{V_g I_g}{2\omega C_-})^2 + (\frac{V_g^2}{2})^2} - \frac{V_g I_g}{2\omega C_-}} \\ &= \sqrt{\frac{V_g^2}{2} + \frac{V_g^2}{2}(\sqrt{\frac{V_g^2 I_g^2}{4\omega^2 C_-^2}\frac{4}{V_g^4} + 1} - \frac{V_g I_g}{2\omega C_-}\frac{2}{V_g^2})} \\ &= \sqrt{\frac{V_g^2}{2} + \frac{V_g^2}{2}(\sqrt{\frac{(\frac{I_g}{\omega C_-})^2}{V_g^2} + 1} - \frac{\frac{I_g}{\omega C_-}}{V_g})} \end{aligned} \tag{7.18}$$

and the maximum value of the V_- can be given as

$$\begin{aligned} V_{-max} &= \sqrt{V_{-0_{min}}^2 + \frac{V_g I_g}{2\omega C_-}} \\ &= \sqrt{\frac{V_g^2}{2} + \frac{V_g^2}{2}(\sqrt{\frac{(\frac{I_g}{\omega C_-})^2}{V_g} + 1} + \frac{\frac{I_g}{\omega C_-}}{V_g})}. \end{aligned} \tag{7.19}$$

It can be found that the V_{-min} is very close to the RMS value of the grid voltage, i.e. $\frac{V_g}{\sqrt{2}}$. According to (7.18) and (7.19), the minimum and maximum values of the V_- can be determined with a tentatively given C_-, which can be small. If the resulted V_- is greater than $V_{DC} - V_g \sin\omega t$ for $0 \leqslant \omega t \leqslant \pi$, the maximum value of the V_- should be decreased so that $V_- \leqslant V_{DC} - V_g \sin\omega t$ can be satisfied, which ensures the successful operation of

the rectifier as mentioned before. The V_{-max} can be decreased by simply increasing the capacitor C_-. In this way, the selection of the V_- and the capacitor C_- can be achieved.

7.3.6 Reduction of the CM Current

The equivalent circuit for analysing the CM current is shown in Figure 7.2(b). Because the capacitor C_- is connected in parallel with the parasitic capacitor C_p, the voltage across the parasitic capacitor is clamped to the voltage V_- and the resulting CM current is

$$i_{CM} = sC_pV_-,$$

which is significantly reduced with comparison to the original CM current (7.3) because V_- is designed to contain a DC component and a second-order ripple, which do not make much contribution to the CM current, plus a switching ripple, which is designed to be small. Hence, an isolation transformer is no longer needed. Importantly, the reduction of the CM current is achieved naturally.

7.4 Control Design

As mentioned before, the control of the two legs is independent from each other. The main objective of the rectification leg is to regulate the DC-bus voltage via controlling the grid current to be in phase with the grid voltage so that the unity power factor can be achieved as well. The control of the rectification leg is very similar to that of conventional half-bridge and full-bridge rectifier and the detailed control structure is not given here because of the page limit. Interested readers are referred to (Zhong and Hornik, 2013b; Srinivasan and Oruganti, 1998; Ming and Zhong, 2013; 2015). The following design is focused on the controller for the neutral leg. The main objective of the neutral leg is to divert the ripple energy from the DC bus to the capacitor C_-, or in other words, to make the current flowing through the capacitor C to be zero. This can be achieved by making the non-DC component of the current I to be zero. In order to achieve this, there is a need to regulate the DC component of V_- as well so that the neutral leg can work properly.

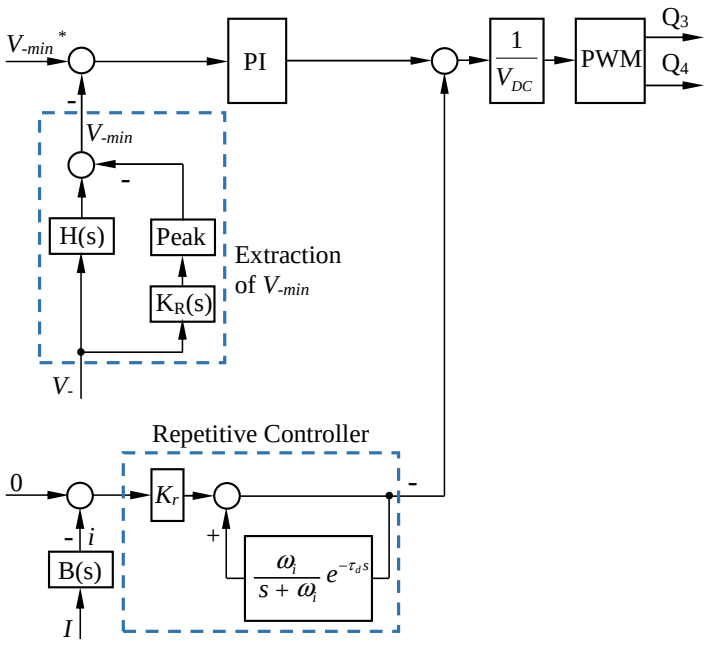


Figure 7.5: Controller for the neutral leg.

7.4.1 Regulation of the DC Component of V_{-}

According to (7.8), the regulation of the voltage V_{-} can be achieved by changing the duty cycle d_4. In order to guarantee the boost operation of the rectifier, the voltage V_{-} should be higher than the peak grid voltage. This can be achieved by controlling the average, minimum or maximum value of the voltage V_{-}. In this chapter, the control objective is to control the minimum value of the voltage V_{-} at a given value. For this purpose, the minimum value of the voltage V_{-} is extracted by using the average voltage to subtract the peak value of the voltage ripple $\triangle V_{-}$. The average voltage can be easily obtained by using the hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts} \tag{7.20}$$

where T is the fundamental period of the grid voltage, as shown in Figure 7.5. At the same time, the measured voltage V_{-} is sent to the following resonant filter (Castilla et al., 2009; Shen et al., 2010)

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{7.21}$$

to extract the $\triangle V_{-}$. The filter is tuned at the second-order harmonics with $\xi = 0.01$ and $h = 2$. Then, the peak value of $\triangle V_{-}$ can be extracted by squaring the $\triangle V_{-}$ with the result

sent to a hold filter. Once the minimum value of the voltage V_- is obtained, a simple proportional-integral (PI) controller can be adopted to regulate it at the given value via generating the right duty cycle d_4.

7.4.2 Removal of Low-Frequency Ripples from V_{DC}

In order to make the DC-bus voltage ripple-free, all the low frequency ripples should be removed from the current i_C. This can be achieved by making the DC-bus current I ripple-free. The low-frequency component of the DC-bus current I can be extracted with a band pass filter, e.g.

$$B(s) = \frac{10000s}{(s+10)(s+10000)},$$

and then used as a feedback signal. It is then compared with its reference set at zero. What is left is to design a current controller. A repetitive controller is used here, as shown in Figure 7.5. The repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where τ_d is designed based on the analysis in (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a) as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\text{s}$$

with $\omega_i = 2550$, $\tau = 0.02\,\text{s}$.

The controller used for the regulation of the voltage V_- is to deal with the DC component of the voltage V_- while the repetitive current controller is to deal with the non-DC component. As a result, they are decoupled in the frequency domain and the outputs from the two controllers can be added together to form the final duty cycle, as shown in Figure 7.5. Because these control strategies are very matured (Zhong and Hornik, 2013b), the stability of the system can be guaranteed with ease so no detailed stability analysis is carried out here.

7.5 Selection of Passive Components

In general, the principles to select passive components are to minimise their volume. There are in total four passive components, i.e., the capacitors C_- and C , the inductors L_g and L_N. How to select the capacitor C_- has been discussed before. Also, the selection criteria of the inductor L_g are extensively discussed in the literature. Basically, rules to select grid side inductor in conventional rectifiers can be directly applied here for the selection of the L_g . As a result, the following parts are mainly focused on how to select the C and L_N.

7.5.1 Selection of the Inductor L_N

Along with the switching on and off of the Switches Q_3 and Q_4, the current i_L contains switching frequency component. The inductor limits the increasing and decreasing speed of the current. From the viewpoint of limiting switching current ripples, the inductor should be as large as it can be. However, it is preferable to have a small inductor in order to reduce costs and to improve power density and dynamic response.

The operation of the neutral leg is similar to that of a DC/DC buck converter. The Switches Q_3 and Q_4 are operated complementarily, the on time of Q_4 is $\frac{d_4}{f_s}$ and the on time of Q_3 is $\frac{1-d_4}{f_s}$ in one PWM period, where f_s is the switching frequency. Since the switching frequency is much higher than the line frequency, it can be assumed that the current increased and decreased are the same during the two modes. As demonstrated in (Srinivasan and Oruganti, 1998), the peak-peak current ripple is

$$\triangle i_L = \frac{V_+ V_-}{L_N f_s V_{DC}}.$$

As a result, the maximum peak-peak current ripple $\triangle i_{Lm}$ on the inductor L_N is

$$\triangle i_{Lm} = \frac{(V_+ V_-)_{max}}{L_N f_s V_{DC}} \tag{7.22}$$

where $(V_+ V_-)_{max}$ is the maximum value of the product of V_+ and V_-. Since $V_+ + V_- = V_{DC}$, the $V_+ V_-$ reaches its maximum value when $V_+ = V_- = \frac{V_{DC}}{2}$. In order to maintain the current ripple less than a given value $\triangle i_{Lm}$, the required minimum inductor is

$$L_{Nmin} = \frac{V_{DC}}{4 f_s \triangle i_{Lm}}. \tag{7.23}$$

The inductor can be very small if f_s is high enough.

7.5.2 Selection of the Capacitor C

Since the low frequencies (both fundamental and second-order) ripples are diverted away from the the capacitor C, it is now mainly used to filter output switching frequency ripples. Those high frequency ripples come from both the rectification leg and the neutral leg. Because the grid current should not have large switching ripples, the level of the switching ripples flowing through the capacitor C is more or less the same as that of the switching ripples flowing through the neutral leg, i.e. the switching ripples flowing through the inductor L_N. According to (Mohan, 2003), the peak-peak switching voltage ripples across the capacitor C are

$$\begin{aligned} \triangle V_{DCs} &= \frac{\triangle i_{Lm}}{8Cf_s} \\ &= \frac{V_{DC}}{32CL_N f_s^2}. \end{aligned} \tag{7.24}$$

The required DC-bus capacitor C is

$$C = \frac{V_{DC}}{32\triangle V_{DCs} L_N f_s^2}. \tag{7.25}$$

In this chapter, only the effect of the switching ripples is considered when choosing the capacitor C. However, the chosen C should be large enough to fulfil the other system requirements, such as hold-up time and dynamic response, for certain applications (Wang et al., 2014).

7.5.3 Design Example

A numerical example is given here with the parameters of the system summarised in Table 7.1. These parameters are taken from the experimental test rig to be validated later.

According to (7.14), the required minimum capacitance is $C_{-min} = \frac{V_g I_g}{\omega(V_{-max}^2 - V_{-min}^2)} = \frac{\sqrt{2}\times 110\times 3.5}{100\pi(275^2-110^2)} \approx 27\ \mu$F. Here $I_g = 3.5$ A is used to take into account the power losses. The capacitor is then selected as $C_- = 30\ \mu$F in order to leave some margin.

The selection of the inductor L_N mainly depends on its capability to limit switching

Table 7.1: Parameters of the system

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
Inductor L_g	2.2 mH
Inductor L_N	2.2 mH
DC-bus voltage V_{DC}^*	400 V
Load R	690 Ω
DC-bus capacitor C	20 μF
Auxiliary capacitor C_-	30 μF

current ripples. Based on (7.23), the required minimum inductor is $L_{Nmin} = \frac{V_{DC}}{4f_s \triangle i_{Lm}} \approx 2$ mH, where $\triangle i_{Lm} = 2.5$ A. Here, a 2.2 mH inductor is used.

For the DC-bus capacitor $C = 20\ \mu$F, $\triangle V_{DCs} = \frac{V_{DC}}{32CL_N f_s^2} \approx 0.7$ V, which is small enough.

7.5.4 Comparison of the Required Volume of Capacitors

Although both of the capacitors are small, it is natural to question whether the total capacitance becomes smaller compared to that of the conventional full-bridge rectifier. In order to clearly show the reduction of the capacitors, a comparison of the required capacitors is presented based on the aim to achieve the same level of DC-bus voltage ripples. Note that V_{DC0} is equal to V_{DC} because the DC-bus voltage ripples are almost eliminated. Taking into account (7.25), the reduction ratio of the required capacitance of the proposed rectifier with comparison to that of the conventional full-bridge rectifier is

$$\begin{aligned} r &= \frac{C_{-min} + C}{\frac{V_g I_g}{2\omega \triangle V_{DC} V_{DC}}} \\ &= \left(\frac{V_g I_g}{\omega(V_{-max}^2 - V_{-min}^2)} + \frac{V_{DC}}{32 \triangle V_{DCs} L_N f_s^2}\right) \frac{2\omega \triangle V_{DC} V_{DC}}{V_g I_g} \\ &= \frac{2 \triangle V_{DC} V_{DC}}{V_{-max}^2 - V_{-min}^2} + \frac{\omega \triangle V_{DC} V_{DC}^2}{16 \triangle V_{DCs} L_N f_s^2 V_g I_g}. \end{aligned} \tag{7.26}$$

For the numerical example given before, when $\triangle V_{DC} = 5$ V, $r \approx 0.1$ and the required capacitance is reduced by about 10 times. If $\triangle V_{DC} = 2$ V, then $r \approx 0.045$, which means the required capacitance is reduced by about 22 times.

7.6 Impact of Adding the Auxiliary Capacitor C_{-}

In this section, the impact of the auxiliary capacitor is analysed in detail from several aspects, such as the regulation of the DC-bus voltage and the grid current, the voltage stress of the power switches and the efficiency. In order to facilitate the following analysis, the power transistor and diode of each switch are denoted as T and D. T_1, D_1, T_2, D_2, T_3, D_3, T_4, D_4, V_{DC} and d_2 in the conventional full-bridge rectifier are denoted as T_{f1}, D_{f1}, T_{f2}, D_{f2}, T_{f3}, D_{f3}, T_{f4}, D_{f4}, V_{fDC} and d_{f2}, respectively. T_1, D_1, T_2, D_2, T_3, D_3, T_4, D_4, V_{DC} and d_2 are specially referred to the components in the proposed rectifier.

7.6.1 Impact on the Range of the DC-bus Voltage

In order to satisfy $0 \leqslant d_2 \leqslant 1$, according to (7.7), there is $V_{DC} \geqslant 2V_g$. In other words, the minimum DC-bus voltage should be at least twice of the peak grid voltage V_g. This is the same as conventional half-bridge rectifiers and twice of conventional full-bridge rectifiers. Hence, the topology is particularly good for applications that requires high voltage ratio between the DC side and the AC side, e.g., single-phase to three-phase power conversion (Machado et al., 2006; Cipriano dos Santos et al., 2011; Enjeti and Rahman, 1993).

For the same load voltage $V_{DC} = V_{fDC}$, the proposed rectifier only requires half of the peak grid voltage V_g needed by full-bridge rectifiers. For some applications, if a transformer is needed to step down the supply voltage to ensure the boost operation of rectifiers, then the size and cost of the transformer used in the proposed rectifier would be lower than that used in full-bridge rectifier. Due to the smaller transformer, system efficiency and power density would be accordingly improved.

7.6.2 Impact on the Regulation of the Grid Current

The regulation of the grid current mainly depends on the rectification leg. Due to the auxiliary capacitor, the duty cycle is changed from $d_{f2} = 1 - \frac{V_g}{V_{fDC}}|\sin\omega t|$ to $d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t$. As a result, the duty cycle is different in order to achieve the same grid current. However, since $0 \leqslant d_2 \leqslant 1$ is always achievable, the grid current can be regulated as usual and hence, is not affected by adding the capacitor C_{-}.

7.6.3 Impact on the Voltage Stress of the Switches

For the switches of conventional full-bridge rectifiers and half-bridge rectifiers, the maximum voltage across the switches is V_{fDC}. Similarly, the maximum voltage across the switches in the proposed rectifier is V_{DC}. For the same load voltage, i.e. with $V_{DC} = V_{fDC}$, the maximum voltage on the switches are not affected after adding the auxiliary capacitor.

7.6.4 Impact on the Efficiency

In order to evaluate the impact of the auxiliary capacitor on the system efficiency, both conduction losses and switching losses should be taken into consideration. Note that, to some extent, the following comparison is unfair because the conventional full-bridge rectifier does not have the capability of reducing the electrolytic capacitors and the CM currents. Even so, the impact on the efficiency is small.

7.6.4.1 Extra conduction loss

Assume that the four switches of the proposed rectifier have the same conduction voltage drop V_{on} as the ones in the conventional full-bridge rectifier. Here, IGBTs are used for all the switches. For the Switches Q_1 and Q_2 of the rectification leg, the transported current is the grid current, which is exactly the same as the corresponding ones in the conventional full-bridge rectifier. At the same time, apart from the second-order component in the inductor current i_L, the low frequency current transported by the Switches Q_3 and Q_4 of the neutral leg is nearly the same as that of the conventional full-bridge rectifier. As mentioned previously, the second-order component of the inductor current i_L flows through the DC-bus capacitor in the conventional full-bridge rectifier. Therefore, compared to the conventional full-bridge rectifier, the only extra conduction losses are caused by the second-order component flowing through power switches Q_3 and Q_4. As a result, there is

$$\begin{aligned} P_e &= \frac{V_{on}\int_0^{2\pi}|\frac{V_g I_g}{2V_-}\cos 2\omega t|(d_3+d_4)d\omega t}{2\pi} \\ &= \frac{8V_{on}\int_0^{\frac{\pi}{4}}\frac{V_g I_g}{2V_-}\cos 2\omega t d\omega t}{2\pi} \\ &= \frac{V_{on}V_g I_g}{\pi V_-} \end{aligned}$$

Table 7.2: Summary of forced commutations of the proposed rectifier

Power Device	Number of forced commutations	Voltage	Current
D_1, D_2	1	V_{DC}	$I_g \sin \omega t$
T_1, T_2	1	V_{DC}	$I_g \sin \omega t$
D_3, D_4	1	V_{DC}	$-I_g \sin \omega t + \frac{V_g I_g}{2V_-} \cos 2\omega t$
T_3, T_4	1	V_{DC}	$-I_g \sin \omega t + \frac{V_g I_g}{2V_-} \cos 2\omega t$

where P_e is the extra conduction losses. The ratio between the extra power and the system real power is

$$\frac{P_e}{\frac{V_g I_g}{2}} = \frac{\frac{V_{on} V_g I_g}{\pi V_-}}{\frac{V_g I_g}{2}} = \frac{2V_{on}}{\pi V_-}. \tag{7.27}$$

The conduction voltage V_{on} is normally around a few volts. The level of the voltage V_- is designed according to the system power, the DC-bus voltage and the auxiliary capacitor. It is often to have $V_- \gg V_{on}$ and hence, the extra conduction losses can be negligible compared to the system power.

For the design example, the average value of the V_- is set around 215 V and the ratio $\frac{P_e}{P_o} \approx 0.0024$ with $V_{on} = 1.5$ V, which means there additional power loss is only 0.44%.

The overall conduction loss of the conventional full-bridge rectifier is $P_f = \frac{4V_{on} I_g}{\pi}$. As a result, the ratio between the extra conduction losses and the overall conduction losses is

$$\frac{P_e}{P_f} = \frac{\frac{V_{on} V_g I_g}{\pi V_-}}{\frac{4V_{on} I_g}{\pi}} = \frac{V_g}{4V_-}.$$

For the design example, the conduction loss of the proposed rectifier is $\frac{P_e}{P_f} \approx 18\%$ higher than the condition losses of the conventional full-bridge rectifier.

Both the aforementioned ratios indicates that the proposed rectifier has low extra conduction loss while achieving the elimination of the isolation transformer and the bulky electrolytic capacitors.

Table 7.3: Summary of forced commutations of the conventional full-bridge rectifier

Power Device	Number of forced commutations	Voltage	Current
D_{f1}, D_{f2}, D_{f3}, D_{f4}	2	V_{DC}	$I_g \sin \omega t$
T_{f1}, T_{f2}, T_{f3}, T_{f4}	2	V_{DC}	$I_g \sin \omega t$

7.6.4.2 Extra switching loss

Both legs of the proposed rectifier are operated at switching frequency. As a result, there are two forced commutation switches in one switching period, as shown in Table 7.2. Similar analysis can be done for the conventional full-bridge rectifier and the results are shown in Table 7.3. It is clear that the switching losses of the proposed rectifier are almost the same as those of the conventional full-bridge rectifier. The only extra switching loss is caused by the second-order component in the current flowing through D_3, D_4, T_3 and T_4. Since the voltage stress in the two rectifiers is the same, this loss mainly depends on the level of the second-order current.

7.6.4.3 Efficiency comparison

In order to evaluate the performance of the proposed system on efficiency, an efficiency comparison is made, between the proposed rectifier and the conventional full-bridge rectifier. The PLECS simulations for both systems are built for this purpose. Similar method for efficiency comparison is used in Chapter 2, which has been demonstrated to be accurate enough. The systems were tested from 50 W to 1000 W by changing DC load R. Note that the DC-bus voltage is always kept at 400 V. The obtained result is shown in Figure 7.6. It can be found that the efficiency of the proposed rectifier is lower than that of the full-bridge rectifier when the power is lower than 400 W. However, along with the increase of system power, their efficiencies become almost the same.

Actually, it is worth mentioning that the above efficiency comparison is unfair because the full-bridge rectifier cannot achieve the reduction of the CM current and DC-bus voltage ripples while the proposed rectifier can. Normally, an isolation transformer is required in the full-bridge rectifier to reduce CM voltage, which introduces about 2% decrease on

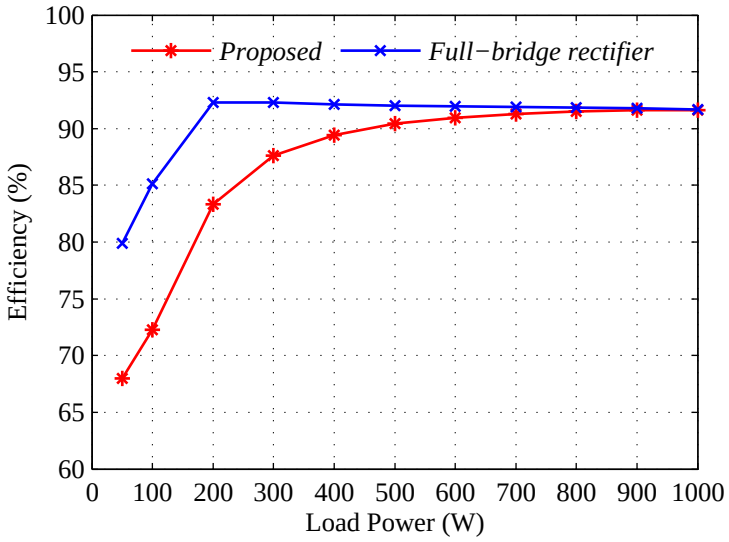


Figure 7.6: Efficiency comparison.

system efficiency (Kerekes et al., 2011). At the same time, if a parallel active filter is used to reduce DC-bus voltage ripples in full-bridge rectifier, it is expected that the system efficiency could be reduced about 3% (Wang et al., 2012). As a result, the efficiency of the proposed rectifier is very likely to become higher than that of the full-bridge system, which includes both the isolation transformer and the active filter.

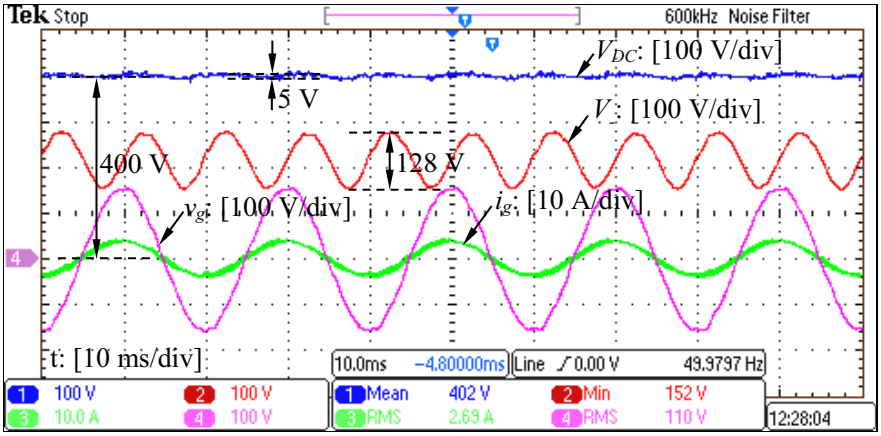
7.7 Experimental Results

In order to validate the proposed rectifier, a test rig was assembled in the lab. The test rig is based on a control system with TMS320F28335 DSP and some auxiliary parts such as sensors and conditioning circuits. The code of the control system is built by MATLAB/SIMULINK R2013a and then downloaded to the DSP for execution with the sampling frequency of 4 kHz. The other system parameters are the same as the ones given in Table 7.1. The capacitors used are one 20 μF metallized polypropylene film capacitor for C and one 30 μF for C_{-}, respectively.

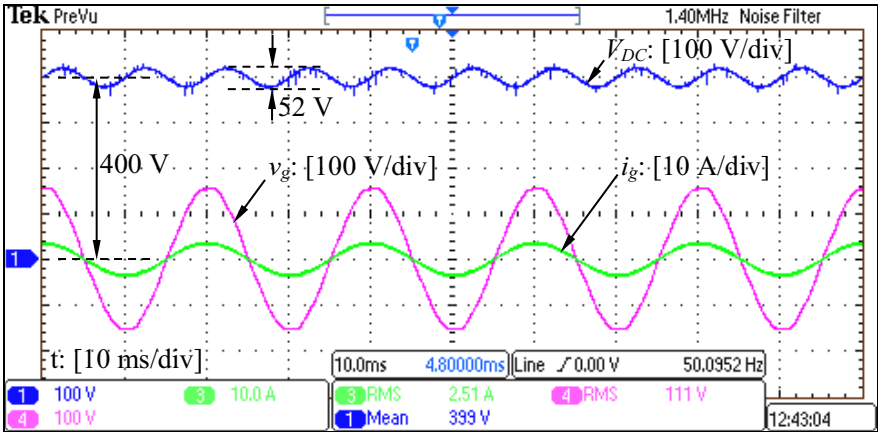
7.7.1 Normal Operation

The reference of the DC-bus voltage V_{DC} 400 V is slightly higher than the required voltage $2V_g$. In order to demonstrate the performance improvement of adding the auxiliary capa-

C_{-} connected to N (proposed)

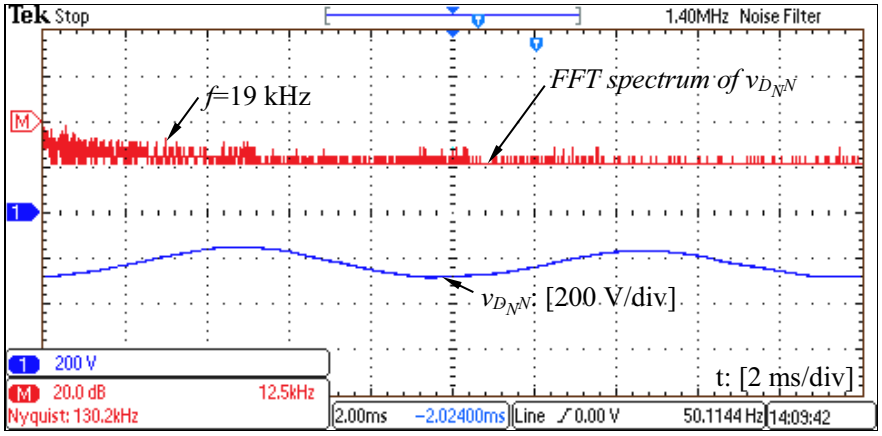


C_{-} connected to D_P (conventional)

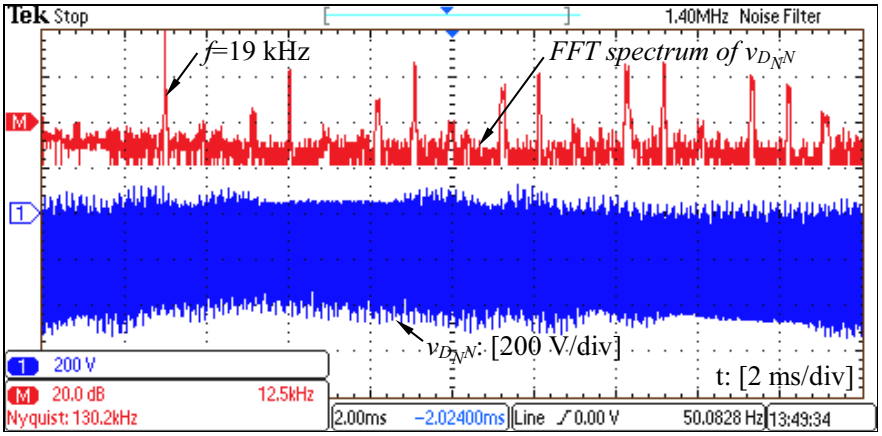


(a)

C_- connected to N (proposed)

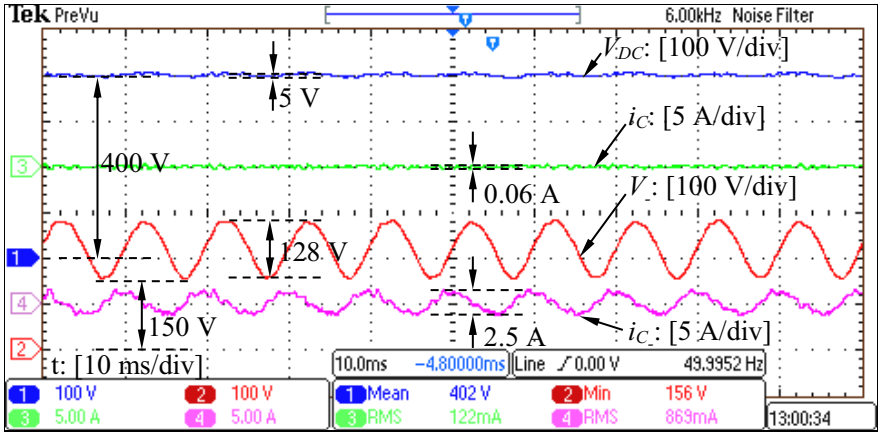


C_- connected to D_P (conventional)

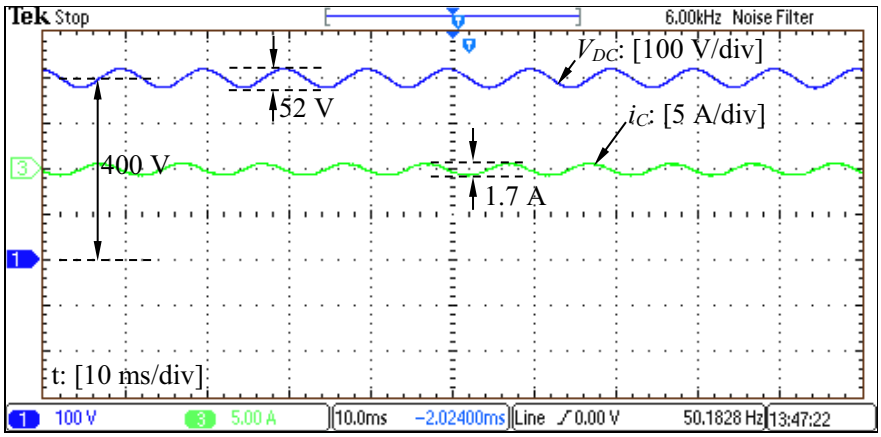


(b)

C_- connected to N (proposed)



C_- connected to D_P (conventional)



(c)

Figure 7.7: Experimental results: (a) DC voltages V_{DC} and V_-, grid voltage v_g and grid current i_g; (b) common mode voltage v_{D_NN} and its FFT spectra; (c) DC voltages V_{DC} and V_-, capacitor currents i_C and i_{C-} after applying a 6 kHz low-pass filter to filter out the switching ripples.

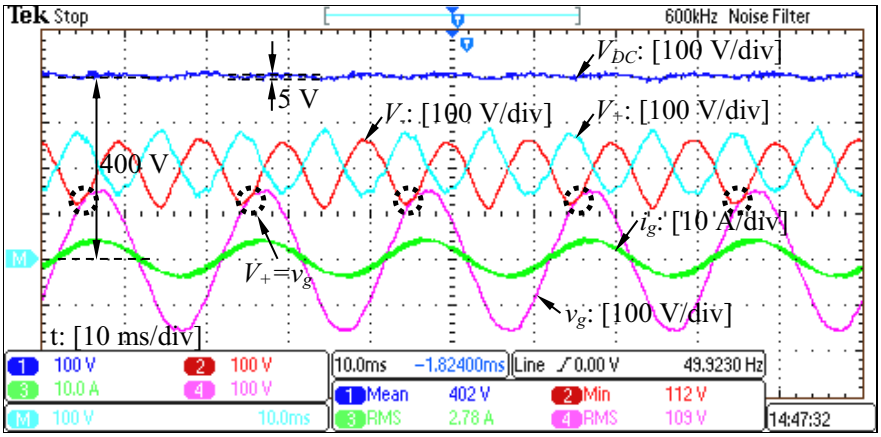
citor, the experiments were carried out for two cases: one for the proposed topology with C_- connected to the neutral point N and the other for the conventional full-bridge with C_- connected to the positive pole D_P of the DC bus (in parallel with C). For the proposed topology, V_{-min} is set at 150 V. The results are shown in Figure 7.7. The DC-bus voltage V_{DC} for the proposed topology is maintained very well around its reference with very low voltage ripples (around 5 V). However, the conventional full-bridge rectifier has very high voltage ripples (around 52 V). For the proposed topology, the voltage V_- across the capacitor C_- has high voltage ripples, at around 128 V, but this is expected. Because of the allowable large voltage ripples, the auxiliary capacitor C_- can be small and hence the total capacitance is reduced significantly.

Apart from having low output voltage ripples, it is also important to have clean grid current, which is expected to be in phase with the grid voltage to achieve the unity power factor. As shown in Figure 7.7(a), the grid current is well regulated to be in phase with the grid voltage for both cases. According to the experimental data, the total harmonic distortion (THD) of the grid current is around 4% and the power factor is above 0.99. Note that no special efforts are made to improve the power quality of the test rig and, hence, the quality of the grid current is very good. For the conventional full-bridge rectifier, the THD of the grid current is about 3.2%, which is more or less the same as that of the proposed rectifier.

For both rectifiers, the CM voltage v_{D_NN} is tested via measuring the voltage between points D_N and N, which are the DC and AC grounds, respectively, and the results are shown in 7.7(b). Also, the FFT spectra of the CM voltage is given in order for comparison. Obviously, the high-frequency components of the v_{D_NN}, which contribute to most of CM currents, are significantly reduced in the proposed rectifier compared those in conventional bridge rectifier.

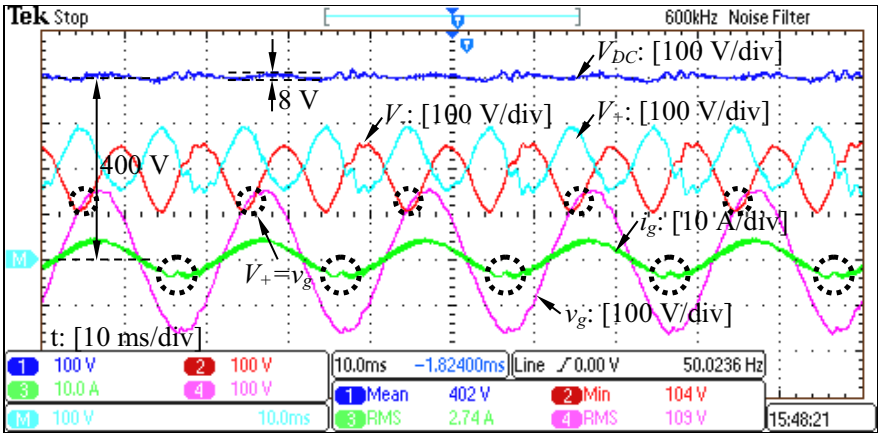
In order to demonstrate how the ripple power is diverted from C to C_-, the corresponding capacitor current i_C and i_{C-} are shown in Figure 7.7(c) after applying a filter having a bandwidth of 6 kHz to filter out the switching ripples. For the proposed rectifier, the current i_C is around 0.06 A without visible low-frequency components and hence, the output voltage V_{DC} can be almost ripple-free. For the conventional bridge rectifier, the current i_C is around 1.7 A because most of the second-order current flow through DC-bus capacitors.

Critical case: $V^*_{-min} = 112$ V



(a)

Deteriorated case: $V^*_{-min} = 104$ V



(b)

Figure 7.8: Examination of the operational boundary.

On the other hand, the second-order harmonic current in the proposed rectifier is diverted to the auxiliary capacitor C_-, as expected, and the current i_{C-} has relatively large ripples as designed, at 2.5 A.

7.7.2 Examination of the Operational Boundary

In order to examine the operational boundary of the rectifier, the results with $V_{-min} = 112$ V and $V_{-min} = 104$ V are shown in Figure 7.8. According to (7.15), both voltage V_+ and V_- should be higher than the grid voltage. When $V_{-min} = 112$ V, the voltage V_- is almost equal to the grid voltage during some period (highlighted by dashed cycles) as shown in

Figure 7.8(a). The grid current under this case does not have any noticeable distortion and can be still well regulated. However, when $V_{-min} = 104$ V, which is lower than 110 V, the grid current has some distortions (highlighted by dashed cycles) as shown in Figure 7.8(b) (highlighted by dashed cycles). The above results are well consistent with the analysis made in the Section 7.3.5.

7.8 Summary

An auxiliary capacitor has been added to the widely-used full-bridge rectifiers with four switches, which has resulted in significantly-reduced CM currents and DC-bus voltage ripples with small capacitors. Because of the added auxiliary capacitor, the operation of the rectifier is very different from that of the conventional full-bridge rectifiers. The two legs become independent from each other, which makes the design of both legs very flexible. One leg remains to take the responsibility of exchanging energy with the grid to achieve unity power factor and to regulate the DC-bus voltage; the other leg is to divert the ripple energy from the DC-bus capacitor to the auxiliary capacitor. Although the number of capacitors is increased from one to two, it has been demonstrated that the total capacitance needed becomes much smaller. As a result, it becomes cost-effective to use film capacitors to replace bulky electrolytic capacitors, which improves power density and reliability. Finally, experimental results for both the proposed rectifier and the full-bridge rectifier are presented and compared to validate the high performance of the proposed rectifier.

Chapter 8

θ-converters with Further Reduced Total Capacitance Compared to ρ-converters

In this chapter, the aforementioned research on the ρ-converter is moved forward to develop a single-phase θ-converter, which further reduces the total capacitance required and low-frequency voltage ripples compared to that in the ρ-converter. Again, the AC and DC grounds are directly connected together so that the common mode current is completely eliminated without extra efforts. Hence, isolation transformers are no longer needed. Moreover, there are also two capacitors in the proposed converter. One of them is used as the output capacitor and the ripple current flowing through the output capacitor is *instantaneously* diverted to another capacitor. The output capacitor is sized only for switching-frequency ripples and it can be very small. At the same time, the capacitor with the diverted ripple current is used to store system ripple power and it is designed to have large voltage ripples because the voltage across it does not supply any loads. As a result, only a small capacitor is needed for this purpose. In this case, the total capacitance required becomes much smaller with comparison to that of conventional converters. The reduction of the total capacitance and the output voltage ripples are achieved at the same time. A comparison is made on total capacitance required between the proposed θ-converter and ρ-converter. Experimental results are presented to demonstrate the high performance of the proposed system.

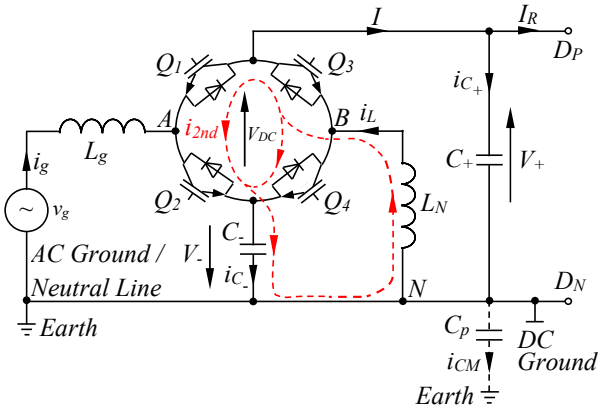


Figure 8.1: The ρ-converter.

8.1 Introduction

As discussed in Chapters 4, 5 and 6, it is possible to reduce voltage ripples and the required DC-bus capacitance in ρ-converters with common AC and DC ground. As shown in Figure 8.1, ρ-converters have two capacitors that are symmetrically connected across the DC bus in a split manner. System ripple power is stored in the lower one of the split capacitors and the upper one is used as the output capacitor, which is sized only for switching-frequency ripples. In this case, the total capacitance required can be significantly reduced compared that in conventional converters. Accordingly, both bulky electrolytic capacitors and isolation transformers can be removed. Importantly, only four switches are used and hence, the ρ-converter is very compact. A converter with similar structure can be found in (Breazeale and Ayyanar, 2015), which was specially designed for split-phase power grid.

In this chapter, a converter with common AC and DC ground is proposed. The elimination of the CM current is naturally achieved because of the common AC and DC ground. Moreover, there are two capacitors in the converter. Due to the shape of the converter, the proposed converter is called θ-converter. One of the capacitors is used as the output voltage to supply DC loads, which is only required to be high enough to filter out switching-frequency ripples. As a result, it can be very small. At the same time, another capacitor is used to stored all the system ripple but it is not used to supply any DC loads. In this case, the voltage across it can be designed to have large voltage ripple on purpose. Due to the allowed large voltage ripples, only a small capacitor is needed. Accordingly, the total capacitance required is significantly reduced compared to that in conventional converters.

Highly-reliable capacitors can be used without increasing system costs because of reduced capacitance. Due to the removed isolation transformers and electrolytic capacitors, the system power density and reliability are significantly improved. The removal is mainly achieved by the neutral leg, which is one of the two legs in the θ-converter. Another leg, i.e. the rectification leg, is mainly used to control the power exchange between the AC and DC sides. Both real and reactive power can be processed without any restrictions on the power factor. Note that the control of the two legs is independent from each other. The detailed control strategies are designed for the two legs, respectively.

The main difference is the location of one of the two capacitors, when comparing the θ-converter with the ρ-converter. The location of the output capacitor is kept same. In the ρ-converter shown in Figure 8.1, the capacitor used for storing the ripple power is placed between the AC neutral line and negative line of the DC bus. However, the location of this capacitor is changed and it is placed between the positive line and negative line of the DC-bus in the θ-converter. Although this change seems small, the total capacitance required is further reduced to be a very low level. For the experimental system presented later, this capacitance is reduced by 172 times compared to that of conventional converter and by about 3.5 times compared to that of the ρ-converter. The further reduction is because the ripple current can now be *instantaneously* tracked while it is tracked on average for the ρ-converter. It is also because the voltage level of the capacitor used to store the ripple power becomes higher and hence, this capacitor can be reduced in order to achieve the same voltage ripples.

The following parts of this chapter are organised as follows. In Section 8.2, the topology and operation principles of the θ-converter are given with the discussion on how to achieve the reduction of the output voltage ripples and total capacitance required in Section 8.3. In order to further optimize the performance of the θ-converter, how to select components such as capacitors and inductors are given with the aim to minimise their usage. The θ-converter is compared to the ρ-converter in the Section 8.5 mainly from the view of total capacitance required. The associated controllers for the two legs are developed in Section 8.6. After that, intensive experimental results are presented to validate the operation and performance of the θ-converter in Section 8.7, with summary made in Section 8.8.

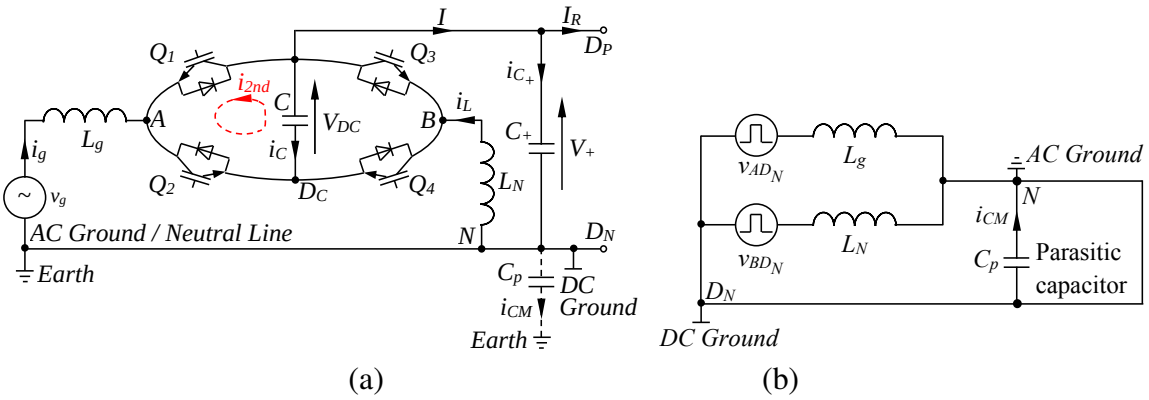


Figure 8.2: The proposed θ-converter: (a) topology; (b) equivalent circuit for analysing the CM current.

8.2 The Proposed θ-converter

As shown in Figure 8.2(a), the proposed converter consists of two legs, i.e. a conversion leg and a neutral leg. Only four switches are used to construct the converter. For the conversion leg, there are two switches, i.e. Q_1 and Q_2, and one inductor L_g. Moreover, the neutral leg is comprised of two switches, i.e. Q_3 and Q_4, two capacitors C_+ and C and one inductor L_N. Because of the shape formed by the two legs and the capacitor C, the proposed converter is named as θ-converter. It is worth highlighting that the θ-converter can be operated in the rectification mode and in the inversion mode. For both modes, there is no restriction on power factor. This means the θ-converter has the capability of bidirectionally exchanging both real and reactive power with the grid, which is highly preferred for grid-tied converters.

The equivalent circuit of the θ-converter for analysing CM currents is shown in Figure 8.2(b). It can be found the CM current i_{CM} is completely eliminated because the AC and DC grounds are directly connected together. As a result, isolation transformers are no longer required, which is naturally achieved without any special efforts on control and/or modulation strategies.

The conversion leg of the θ-converter is mainly used to control the grid current i_g and the DC-bus voltage V_{DC}. At the same time, the neutral leg is responsible to regulate the output voltage V_+ and to divert the second-order ripple power from the output capacitor C_+. Instead of the capacitor C_+, the ripple power is now stored in the capacitor C, which is connected across the DC bus. The output capacitor C_+ is sized only for switching-frequency

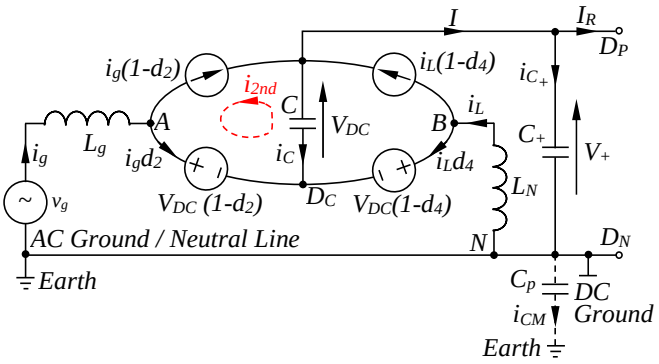


Figure 8.3: Average circuit model of the θ-converter.

ripples and hence, a very small capacitor is enough. At the same time, the capacitor C does not supply any loads and hence, it can be designed to have large voltage ripples on purpose. In this case, this capacitor can be very small as well. The total capacitance required, i.e. $C+C_+$, can be significantly reduced with comparison to that of conventional converters.

All the above objectives are achieved by two legs with only four switches. The two legs can have their own control objectives because they are independent from each other. Accordingly, it is possible to flexibly apply advanced control strategies to each leg according to their own objectives. Design of the controllers for both legs is presented later.

In order to facilitate the following analysis, the converter operated in rectification mode is taken as an example. Only slight changes are required on the analysis when the converter is operated in inversion mode.

8.3 Reduction of DC Voltage Ripples and Total Capacitance Required

8.3.1 Circuit Analysis

For the AC side of the θ-converter, the grid current is often controlled to be in phase with the grid voltage for the unity power factor. In this case, it can be assumed that the grid voltage and the grid current are

$$\begin{aligned} v_g &= V_g \sin \omega t \\ i_g &= I_g \sin \omega t, \end{aligned}$$

respectively, where V_g is the peak grid voltage, I_g is the peak grid current and ω is the grid angular frequency. The product of the v_g and i_g results in the system power, which contains a DC component and a second-order ripple component. As demonstrated in (Gu et al., 2009; Yao et al., 2012), the system input ripple energy for single-phase converters with the unity power factor is

$$E_r = \frac{V_g I_g}{2\omega}. \tag{8.1}$$

For the DC side of the converter, there is

$$V_+ = V_{DC} - V_-$$

where V_+ and V_{DC} are the voltages across the capacitors C_+ and C, respectively, and V_- is the voltage between N and D_C as shown in Figure 8.2(a). Note that the output voltage of the converter is V_+ not V_{DC} or V_-. Because of the power balance, the system input ripple energy (8.1) also appears at the DC side. For conventional converters, bulky electrolytic capacitors are often used to smooth this ripple energy so that the output voltage ripples can be maintained at a low level.

Since the switching frequency is of several orders compared to the grid frequency, the grid current can be controlled to well track its reference. As a result, it can be supposed that the fundamental component of the grid current is constant during one switching cycle. According to the demonstration made in (Srinivasan and Oruganti, 1998), there is

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t$$

where d_2 is the duty cycle of the Switch Q_2. Since the two switches of the conversion leg is operated in complementary, the duty cycle of the Switch Q_1 is

$$\begin{aligned} d_1 &= 1 - d_2 \\ &= \frac{V_-}{V_{DC}} + \frac{V_g}{V_{DC}} \sin \omega t. \end{aligned}$$

Hence, the average circuit model of the conversion leg can be built as shown in Figure 8.3. The switches Q_1 and Q_2 are represented by a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, respectively.

Similarly, the model of the neutral leg can be built. As shown in Figure 8.3, the Switches Q_3 and Q_4 are represented by a current source $i_L(1-d_4)$ and a voltage source $V_{DC}(1-d_4)$, respectively. For the neutral leg, it is actually operated as a DC/DC converter. In this case, there is

$$d_4 = \frac{V_+}{V_{DC}} \tag{8.2}$$

where d_4 is the duty cycle of the Switch Q_4. Due to the complementary operation, the duty cycle of the Switch Q_3 is

$$\begin{aligned} d_3 &= 1-d_4 \\ &= \frac{V_-}{V_{DC}}. \end{aligned}$$

8.3.2 Reduction of Output Voltage Ripples and the Output Capacitor C_+

Since the impedance of the output capacitor at the second-order frequency is $\frac{1}{2\omega C_+}$, the peak-peak value of the output voltage ripples can be given as

$$\triangle V_+ = \frac{1}{2\omega C_+}\triangle i_{C_+} \tag{8.3}$$

where $\triangle i_{C_+}$ is the peak-peak value of the second-order current flowing through the capacitor C_+. It is clear that the level of the $\triangle V_+$ depends on the current $\triangle i_{C_+}$ and the capacitor C_+. The smaller the capacitor C_+ is, the larger the output voltage ripples $\triangle V_+$ are. As a result, there exists a trade off between the reduction of the output voltage ripples and the output capacitor. According to (8.3), it is possible to break this deadlock by minimising the current $\triangle i_{C_+}$. As long as the current $\triangle i_{C_+}$ is around zero, the $\triangle V_+$ can be very small even if a small capacitor C_+ is used. In this case, the reduction of the $\triangle V_+$ and the C_+ can be achieved at the same time without any trade-off.

According to the average circuit model of the converter, there is

$$i_{C_+} = i_L + i_g - I_R \tag{8.4}$$

where i_{C_+}, i_L and I_R are the currents flowing through the capacitor C_+, the inductor L_N and the load, respectively. Because of the power balance between the AC and DC sides

(without considering losses), there is

$$I_R = \frac{V_g I_g}{2V_+}. \tag{8.5}$$

Substitute (8.5) into (8.4), then

$$i_{C_+} = i_L + I_g \sin \omega t - \frac{V_g I_g}{2V_+}.$$

If let $i_{C_+} = 0$, then

$$i_L = -I_g \sin \omega t + \frac{V_g I_g}{2V_+}, \tag{8.6}$$

which can be achieved by the control of the neutral leg. The detailed control strategies can be found in the control design part presented later.

8.3.3 Reduction of the Capacitor C

Due to the significantly-reduced current flowing through the output capacitor C_+, the system ripple energy E_r is now mainly stored in the capacitor C. As a result, there is

$$\begin{aligned} C &= \frac{E_r}{\triangle V_{DC} V_{DC0}} \\ &= \frac{V_g I_g}{2\omega \triangle V_{DC} V_{DC0}} \end{aligned} \tag{8.7}$$

where $\triangle V_{DC}$ and V_{DC0} are the peak-peak and average values of the voltage V_{DC}, respectively. Since the voltage V_{DC} does not supply any loads, it can be designed to have large ripples. As a result, a small capacitor C is already enough.

Based on the above discussion, it is apparent that both the capacitors C and C_+ are very small and hence, the total capacitance required, i.e. $C + C_+$, can be very small as well. Compared to the capacitance required in conventional converters, the total capacitance required in the θ-converter is significantly reduced. It is then cost-effective to use highly-reliable film capacitors to replace original electrolytic capacitors. Detailed discussions on how much the total capacitance can be reduced are given in the next section.

8.4 Selection of the Components

From the view of power density and reliability, it is preferred to minimise the usage of passive components. In this section, how to select the capacitors C and C_+ and the inductor L_N is first discussed and a design example is given in the last.

8.4.1 Selection of the Capacitor C

In order to clearly demonstrate the minimum capacitance of the C, (8.7) can be re-formed as

$$C = \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)} \tag{8.8}$$

where V_{DCmax} and V_{DCmin} are the maximum and minimum values of the voltage V_{DC}. Since $V_{DC} = V_+ + V_-$, the voltages V_{DCmax} and V_{DCmin} depend on both voltages V_+ and V_-. The voltage V_+ is the output voltage of the converter, which is set according to the DC load R. As a result, there are

$$V_{DCmin} = V_+ + V_{-min} \tag{8.9}$$

$$V_{DCmax} = V_+ + V_{-max} \tag{8.10}$$

where V_{-min} and V_{-max} are the minimum and maximum values of the voltage V_-. In order to ensure the successful operation of the converter, the voltage V_- must be higher than the peak grid voltage, which means

$$V_{-min} = V_g \tag{8.11}$$

in order to leave some margin. On the other hand, the voltage V_{-max} mainly depends on allowed voltages of both capacitors and switches. If the lower one of the two allowed voltages is V_a, then

$$V_{-max} = V_a - V_+. \tag{8.12}$$

Substitute (8.11) and (8.12) into (8.9) and (8.10), respectively, then

$$V_{DCmin} = V_+ + V_g$$

$$V_{DCmax} = V_a.$$

According to (8.8), the minimum capacitance can be given as

$$\begin{aligned} C_{min} &= \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)} \\ &= \frac{V_g I_g}{\omega(V_a^2 - (V_+ + V_g)^2)}. \end{aligned} \tag{8.13}$$

It can be found that the higher the voltage V_a is, the smaller the capacitor C can be.

Apart from the minimum capacitance, it is also desirable to know the current flowing through the capacitor in order to select a right capacitor. According to the average circuit model of the θ-converter, there is

$$\begin{aligned} i_C &= i_g(1-d_2) + i_L(1-d_4) - i_{C_+} - I_R \\ &= I_g \sin\omega t(1 - \frac{V_+}{V_{DC}} + \frac{V_g}{V_{DC}}\sin\omega t) + i_L(1 - \frac{V_+}{V_{DC}}) - i_{C_+} - I_R \\ &= \frac{V_- I_g}{V_{DC}}\sin\omega t - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_g I_g}{2V_{DC}} - \frac{V_g I_g}{2V_+} + \frac{V_- i_L}{V_{DC}} - i_{C_+}, \end{aligned} \tag{8.14}$$

where i_C is the current flowing through the capacitor C. If i_{C_+} is around zero, then (8.14) becomes

$$\begin{aligned} i_C &= \frac{V_- I_g}{V_{DC}}\sin\omega t - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_g I_g}{2V_{DC}} - \frac{V_g I_g}{2V_+} + \frac{V_- i_L}{V_{DC}} - i_{C_+} \\ &= \frac{V_- I_g}{V_{DC}}\sin\omega t - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_g I_g}{2V_{DC}} - \frac{V_g I_g}{2V_+} + \frac{V_-}{V_{DC}}(I_R - i_g) \\ &= -\frac{V_g I_g}{2V_{DC}}\cos 2\omega t + \frac{V_g I_g}{2V_{DC}} - \frac{V_g I_g}{2V_+} + \frac{V_- V_g I_g}{2V_+ V_{DC}} \\ &= -\frac{V_g I_g}{2V_{DC}}\cos 2\omega t. \end{aligned} \tag{8.15}$$

There is only a second-order component $-\frac{V_g I_g}{2V_{DC}}\cos 2\omega t$ in the current i_C (without considering switching-frequency component). The peak-peak value of the current i_C is

$$\triangle i_C = \frac{V_g I_g}{V_{DC}}. \tag{8.16}$$

With both (8.13) and (8.16), the capacitor C can be well selected.

8.4.2 Selection of the Inductor L_N

The inductor current i_L is controlled to track its reference (8.6) by complementarily switching on and off the switches Q_3 and Q_4. As a result, the i_L contains both low-frequency and switching-frequency components. Both of them are important when selecting the inductor. For the low-frequency component, the maximum absolute value of the current i_L is

$$i_{Lmax} = I_g + \frac{V_g I_g}{2V_+} \tag{8.17}$$

according to (8.6). As a result, the selected inductor L_N should have a maximum current higher than $I_g + \frac{V_g I_g}{2V_+}$ in order to avoid saturation.

For the switching-frequency component, its peak-peak value is

$$\triangle i_L = \frac{V_+ d_3}{L_N f_s}$$

because of the complementary operation of the neutral leg. Since the voltage V_+ is set according to the load R, the $\triangle i_L$ reaches to its maximum value $\triangle i_{Lmax}$ when the duty cycle d_3 is maximized. That is,

$$\triangle i_{Lmax} = \frac{V_+ d_{3max}}{L_N f_s} = \frac{V_+(1-\frac{V_+}{V_a})}{L_N f_s} \tag{8.18}$$

where d_{3max} is the maximum value of the d_3. The minimum inductance can be then given as

$$L_{Nmin} = \frac{V_+(1-\frac{V_+}{V_a})}{\triangle i_{Lm} f_s}, \tag{8.19}$$

which can be reduced if the switching frequency f_s is increased. On the other hand, high V_a leads to a high minimum inductance, which should be avoided, although high V_a helps to reduce the total capacitance required. As a result, there is a trade-off between minimising the inductor L_N and the total capacitance. It is possible to break this trade-off by increasing the switching frequency f_s.

Table 8.1: Parameters of the θ-converter

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
Inductor L_g	2.2 mH
Inductor L_N	2.2 mH
DC output voltage V_+^*	200 V
Load R	220 Ω
Capacitor C_+	5 μF
Capacitor C	6 μF

8.4.3 Selection of the Output Capacitor C_+

Because most of the system ripple energy is diverted from the capacitor C_+, it is mainly used to smooth switching-frequency ripples. The level of the switching-frequency ripple current flowing through the capacitor C_+ mainly depends on the current i_L because the grid current i_g is supposed to have low switching-frequency ripples. As a result, the peak-peak switching voltage ripples across the capacitor C_+ can be given as (Mohan, 2003)

$$\triangle V_+ = \frac{\triangle i_{Lmax}}{8C_+ f_s}.$$

Then, the capacitance required is

$$\begin{aligned} C_+ &= \frac{\frac{V_+(1-\frac{V_+}{V_a})}{L_{Nmin} f_s}}{8 f_s \triangle V_+} \\ &= \frac{V_+(1-\frac{V_+}{V_a})}{8 f_s^2 \triangle V_+ L_{Nmin}}. \end{aligned} \tag{8.20}$$

It is obvious that the switching frequency f_s plays an important role when selecting the capacitor C_+. High f_s leads to low capacitance required.

8.4.4 Design Example

In order to further demonstrate how to select the capacitors and the inductor, a design example is given here. The related system parameters are summarised in Table 8.1. If let $\triangle i_{Lm} = 4$ A, then the required minimum inductance is $L_{Nmin} \approx 1.97$ mH according to

(8.19) with $V_a = 800$ V. Here, a 2.2 mH inductor is used in order to leave some margin. According to (8.13), there is $C_{min} = \frac{V_g I_g}{\omega(V_a^2-(V_+ + V_g)^2)} \approx 2.88\ \mu$F if $I_g = 3$ A. Let $\triangle V_+ = 6$ V, then $C_+ = \frac{\triangle i_{Lm}}{8 f_s \triangle V_+} \approx 4.38\ \mu$F according to (8.20). In order to leave some margin, a 6 μF and a 5 μF capacitors are selected as C and C_+, respectively.

8.5 Comparison of the θ-converter with the ρ-converter

In this section, the performance of the θ-converter is compared to that of the ρ-converter. The corresponding topologies of the ρ-converter and the θ-converter are shown in Figure 8.1 and Figure 8.2, respectively. The following comparisons are made mainly from the view of second-order ripple current, output voltage ripples, total capacitance required and inductor current. In order for a fair comparison, the DC component and second-order ripple components of the V_{DC} are set to be approximately the same for the θ-converter and ρ-converter. This can be achieved by selecting different capacitance for the capacitors C and C_-. At the same time, the reference of the output voltages in both converters are set to be the same. In this case, the system ripple energy and the voltage stress of the switches are similar for both converters. In order to facilitate the following analysis, V_+, $\triangle V_+$, V_-, $\triangle V_-$, V_{DC}, $\triangle V_{DC}$, Q_1, Q_2, Q_3, Q_4, R and L_N in the ρ-converter are denoted as $V_{+\rho}$, $\triangle V_{+\rho}$, $V_{-\rho}$, $\triangle V_{-\rho}$, $V_{DC\rho}$, $\triangle V_{DC\rho}$, $Q_{1\rho}$, $Q_{2\rho}$, $Q_{3\rho}$, $Q_{4\rho}$, R_ρ and $L_{N\rho}$, respectively. V_+, $\triangle V_+$, V_-, $\triangle V_-$, V_{DC}, $\triangle V_{DC}$, Q_1, Q_2, Q_3, Q_4, R and L_N are specially referred to the components in the θ-converter.

8.5.1 The Flowing Path of the Second-order Ripple Current

As discussed before, there exists a second-order ripple power for single-phase converters. Due to the power balance, the ripple power appears at both the AC and DC sides. Currents at the DC side shall then contain second-order components in order to have the ripple power. However, the current at the AC side, i.e. the grid current, only contains a fundamental component. In other words, second-order currents do not flow through the AC side although the second-order ripple power appear at both sides. It is important to analyse the flowing path of second-order ripple currents because the currents determine the total capacitance required, the DC-bus voltage ripples and the output voltage ripples. For example, if

the ripple currents can be diverted from the output capacitor, then output voltage becomes ripple-free and the output capacitor required can be significantly reduced.

According to the average models of both converters, the second-order current first appears at the switches of the conversion leg, i.e. the Switches Q_1, Q_2 and the Switches $Q_{1\rho}$, $Q_{2\rho}$. For example, the currents flowing through the Switches Q_1 and Q_2 are

$$i_{Q_1} = \frac{V_- I_g}{V_{DC}} \sin \omega t + \frac{V_g I_g}{2V_{DC}} - \frac{V_g I_g}{2V_{DC}} \cos 2\omega t \tag{8.21}$$

$$i_{Q_2} = \frac{V_+ I_g}{V_{DC}} \sin \omega t - \frac{V_g I_g}{2V_{DC}} + \frac{V_g I_g}{2V_{DC}} \cos 2\omega t, \tag{8.22}$$

respectively. It can be found that both of them contain a fundamental component, a DC component and a second-order component. The sum of the two currents is

$$\begin{aligned} i_{Q_1} + i_{Q_2} &= \frac{V_- I_g}{V_{DC}} \sin \omega t + \frac{V_+ I_g}{V_{DC}} \sin \omega t \\ &= I_g \sin \omega t, \end{aligned}$$

which is actually the grid current i_g. In other words, the current i_g is divided into two parts due to the on and off operation of the Switches Q_1 and Q_2. One of them flows through the Switch Q_1 and the other flows through the Switches Q_2. Similarly, the corresponding currents in the ρ-converter can be given as

$$i_{Q_{1\rho}} = \frac{V_{-\rho} I_g}{V_{DC\rho}} \sin \omega t + \frac{V_g I_g}{2V_{DC\rho}} - \frac{V_g I_g}{2V_{DC\rho}} \cos 2\omega t \tag{8.23}$$

$$i_{Q_{2\rho}} = \frac{V_{+\rho} I_g}{V_{DC\rho}} \sin \omega t - \frac{V_g I_g}{2V_{DC\rho}} + \frac{V_g I_g}{2V_{DC\rho}} \cos 2\omega t. \tag{8.24}$$

Again, there is $i_{Q_{1\rho}} + i_{Q_{2\rho}} = i_g$.

Because of $V_+ \approx V_{+\rho}$, $V_- \approx V_{-\rho}$ and $V_{DC} \approx V_{DC\rho}$, there are $i_{Q_1} \approx i_{Q_{1\rho}}$ and $i_{Q_2} \approx i_{Q_{2\rho}}$. As a result, the currents flowing through the grid and the conversion leg are almost the same for the two converters. According to (8.21), (8.22) and (8.23), (8.24), there exists the same second-order current $\frac{V_g I_g}{2V_{DC}} \cos \omega t$. It is well known that a closed-loop is needed for a current. As a result, the other parts of converters need to provide return path for this second-order current, which is defined as i_{2nd} here.

For the θ-converter, there are

$$\begin{aligned} i_{Q_1} &= i_C + i_{C_+} + I_R - i_{Q_3} \\ i_{Q_2} &= -i_C - i_{Q_4}. \end{aligned}$$

In order to provide the return second-order current i_{2nd} from i_{Q_1} and i_{Q_2}, either i_C, i_{C_+}, I_R, i_{Q_3} or i_{Q_4} should contain components in second order. According to the average model shown in Figure 8.3, the currents flowing through the Switches Q_3 and Q_4 are

$$i_{Q_3} = -\frac{V_- I_g}{V_{DC}} \sin \omega t + \frac{V_g I_g V_-}{2V_+ V_{DC}} \tag{8.25}$$

$$i_{Q_4} = -\frac{V_+ I_g}{V_{DC}} \sin \omega t + \frac{V_g I_g V_+}{2V_+ V_{DC}}. \tag{8.26}$$

As a result, the currents i_{Q_3} and i_{Q_4} do not contain any second-order components and hence, the Switches Q_3 and Q_4 are not in the return path of the second-order current i_{2nd}. As mentioned previously, second-order currents are diverted from the output capacitor C_+ and hence, the capacitor current i_{C_+} and the load current I_R do not have any second-order components either. In this case, the capacitor C is the only path for the return second-order current in the θ-converter.

On the other hand, there are

$$\begin{aligned} i_{Q_{1\rho}} &= i_{C_{+\rho}} + I_{R_\rho} - i_{Q_{3\rho}} \\ i_{Q_{2\rho}} &= -i_{C_{-\rho}} - i_{Q_{4\rho}} \end{aligned}$$

for the ρ-converter. Similarly, either $i_{C_{+\rho}}$, I_{R_ρ}, $i_{Q_{3\rho}}$, $i_{C_{-\rho}}$or $i_{Q_{4\rho}}$ should contain second-order components. According to the average model of the ρ-converter, the currents flowing through the Switches $Q_{3\rho}$ and $Q_{4\rho}$ can be given as

$$i_{Q_{3\rho}} = -\frac{V_- I_g}{V_{DC}} \sin \omega t + \frac{V_g I_g}{2V_{DC}} \cos 2\omega t + \frac{V_g I_g V_-}{2V_+ V_{DC}} \tag{8.27}$$

$$i_{Q_{4\rho}} = -\frac{V_+ I_g}{V_{DC}} \sin \omega t + \frac{V_g I_g V_+}{2V_- V_{DC}} \cos 2\omega t + \frac{V_g I_g}{2V_{DC}}. \tag{8.28}$$

It is obvious that the currents $i_{Q_{3\rho}}$ and $i_{Q_{4\rho}}$ both contain second-order components. At the

Table 8.2: Summary of components carrying i_{2nd}

	Components	Number of components
The θ-converter	Switches Q_1, Q_2 and capacitor C	3
The ρ-converter	Switches $Q_{1\rho}$, $Q_{2\rho}$, $Q_{3\rho}$ and $Q_{4\rho}$, capacitor C_- and inductor $L_{N\rho}$	7

same time, the current flowing through the capacitor C_- is

$$i_{C-\rho} = -\frac{V_g I_g}{2V_{-\rho}} \cos 2\omega t,$$

which is in second order. Since the output capacitor $C_{+\rho}$ and the load R_ρ do not carry any low frequency components, the components that carry the return second-order current i_{2nd} are the Switches $Q_{3\rho}$ and $Q_{4\rho}$, the inductor $L_{N\rho}$ and the capacitor C_-.

According to the above discussions, it becomes obvious that the components that carry the i_{2nd} in both converters are very different. A summary of the related components is given in Table 8.2. Also, the corresponding paths are depicted by dashed red lines as shown in Figure 8.1 and Figure 8.2, respectively, for the the ρ-converter and θ-converter.

It is inevitable that the current i_{2nd} flows through Switches Q_1 and Q_2. In order to form a return path for the i_{2nd} , at least one more component is needed, which should be connected between the Switches Q_1 and Q_2. As a result, the minimum number of the the components carrying i_{2nd} is three. According to the Table 8.2, it can be found that only one more component, i.e. the capacitor C, is added to carry the return current i_{2nd} in the θ-converter. In this case, the number of the components carrying i_{2nd} is already minimised.

On the other hand, seven components are used to carry the current i_{2nd} in the ρ-converter. Obviously, four more components are needed, which leads to higher losses and degraded tracking performance of the current i_{2nd}.

8.5.2 The Ripples of the Output Voltage V_+

As mentioned before, the reduction of the output voltage ripples is achieved by diverting the second-order ripple current i_{2nd} from the output capacitor. For the θ-converter, it is diverted from the output capacitor C_+ to the capacitor C. Since the current flowing through the capacitor C is *continuous*, the ripple current i_{2nd} can be *instantaneously* diverted from the output capacitor. Because of the *instantaneous* diversion, the θ-converter is expected to have high performance on the reduction of the output voltage ripples.

On the other hand, the corresponding ripple current is *averagely* diverted from the output capacitor in the ρ-converter because currents flowing through the Switches Q_3 and Q_4 are *discontinuous*. As a result, the performance of the ρ-converter to reduce the output voltage ripples is degraded compared to that of the θ-converter.

Apparently, the θ-converter has better performance to reduce the output voltage ripples because of the *instantaneous* current diversion. In other words, the capacitance of the C_+ can be further reduced in order to achieve the same level of output voltage ripples. Experimental results are provided later to verify the comparison of the output voltage ripples of the two converters. Importantly, the instantaneous current diversion is naturally achieved without affecting the operation of the neutral leg and the conversion leg. The control of the two legs are still independent from each other in the θ-converter.

8.5.3 Comparison of the Capacitors C_- and C

For the ρ-converter, all the system ripple power is stored in the capacitor C_-. As a result, there is

$$C = \frac{V_g I_g}{2\omega V_{-0} \triangle V_-} \tag{8.29}$$

where V_{-0} and $\triangle V_-$ are the average and peak-peak values of the voltage V_-, respectively. Since the DC-bus voltage V_{DC} is assumed to be approximately the same for both converters, there are $V_{-0} \approx V_{DC0} - V_+$ and $\triangle V_- \approx \triangle V_{DC}$. (8.29) can be then reformulated as

$$C_- = \frac{V_g I_g}{2\omega (V_{DC0} - V_+) \triangle V_{DC}}.$$

On the other hand, the capacitor C is used to store the ripple power for the θ-converter.

According to (8.7), the ratio between the two capacitors is

$$\begin{aligned}\frac{C}{C_-} &= \frac{\frac{V_g I_g}{2\omega V_{DC0}\triangle V_{DC}}}{\frac{V_g I_g}{2\omega(V_{DC0}-V_+)\triangle V_{DC}}} \\ &= \frac{V_{DC0}-V_+}{V_{DC0}} \\ &= 1-\frac{V_+}{V_{DC0}}.\end{aligned}$$

It is clear that the capacitor C is always smaller than the capacitor C_- because $1-\frac{V_+}{V_{DC0}}<1$.

8.5.4 Comparison of the Total Capacitance Required

For conventional converters, the DC-bus capacitance required is

$$C_v = \frac{V_g I_g}{2\omega V_{+0}\triangle V_+}$$

in order to achieve a set level of output voltage ripples $\triangle V_+$. Low $\triangle V_+$ lead to high capacitance C_v. The ratio between the capacitance required in conventional converters and that in the θ-converter is

$$r_\theta = \frac{C_v}{C+C_+}.$$

On the other hand, the capacitance required is

$$C_{v\rho} = \frac{2V_g I_g}{2\omega V_{+0}\triangle V_{+\rho}}$$

in order for conventional converters to achieve the $\triangle V_{+\rho}$. Note that $\triangle V_+ < \triangle V_{+\rho}$ because of the better performance of the θ-converter to reduce output voltage ripples. The ratio between the total capacitance required in conventional converters and that in the ρ-converter is

$$r_\rho = \frac{C_{v\rho}}{C_-+C_+}.$$

Based on the above discussion, there is

$$\begin{aligned}\frac{r_\theta}{r_\rho} &= \frac{C_v}{C+C_+}\times\frac{C_-+C_+}{C_{v\rho}} \\ &= \frac{\triangle V_{+\rho}(C_-+C_+)}{\triangle V_+(C+C_+)}.\end{aligned}$$

Because $\triangle V_{+\rho} > \triangle V_+$ and $C_- > C$, $\frac{r_\theta}{r_\rho}$ is always greater than one. Accordingly, the total capacitance required in the θ-converter is further reduced with comparison that in the ρ-converter. How much the total capacitance can be reduced depends on system parameters. For the system with parameters summarised in Table 8.1, there are $C_v \approx 1900$ μF and $C_{v\rho} \approx 740$ μF. As a result, $r_\theta = \frac{C_v}{C+C_+} \approx \frac{1900}{5+6} \approx 172$, $r_\rho = \frac{C_{v\rho}}{C_-+C_+} \approx \frac{740}{5+10} \approx 49$ and $\frac{r_\theta}{r_\rho} \approx 3.5$. Here, $\triangle V_+ = 2$ V and $\triangle V_{+\rho} = 5$ V according to the experiments presented later. In other words, the total capacitance required in the θ-converter is reduced by about 172 times compared to that in conventional converters and by about 3.5 times compared to that in the ρ-converter.

8.5.5 Comparison of Capacitor Currents

Both converters have two capacitors. The output capacitor C_+ in both converters has the same function, i.e. filtering out switching-frequency ripples. As a result, the current flowing through this capacitor is almost the same for both converters. On the other hand, the currents flowing through the capacitors C and C_- are different, although they are used to store the same ripple power. This is because the voltages across the capacitors C and C_- are different. According to the average circuit model of the ρ-converter (Ming and Zhong, 2014), there is

$$i_{C_{-\rho}} = -\frac{V_g I_g}{2V_-}\cos 2\omega t.$$

According to (8.15), there is

$$\frac{i_{C_{-\rho}}}{i_C} = \frac{V_{DC}}{V_-}, \tag{8.30}$$

which means $i_C < i_{C_{-\rho}}$ because $V_{DC} > V_-$. In this case, the capacitor C is expected to have longer lifetime in general because of the reduced ripple current.

8.5.6 Comparison of the Inductor Current i_L

Apart from the inductance, it is also important to know the maximum current flowing through the inductor L_N. It is possible that the inductor becomes saturated when the current is higher than the maximum value, which should be avoided.

For the ρ-converter, the current flowing through the inductor $L_{N\rho}$ is

$$i_{L\rho} = -I_g \sin \omega t + \frac{V_g I_g}{2V_-} \cos 2\omega t + \frac{V_g I_g}{2V_+}. \tag{8.31}$$

Compared to (8.6), (8.31) has one more second-order component $\frac{V_g I_g}{2V_{-\rho}} \cos 2\omega t$. The derivative of (8.31) is

$$\begin{aligned}
\frac{di_{L\rho}}{dt} &= \frac{d(-I_g \sin \omega t + \frac{V_g I_g}{2V_-} \cos 2\omega t + \frac{V_g I_g}{2V_+})}{dt} \\
&= \frac{d(-I_g \sin \omega t + \frac{V_g I_g}{2V_-}(1 - 2\sin^2 \omega t) + \frac{V_g I_g}{2V_+})}{dt} \\
&= \frac{d(-I_g \sin \omega t + \frac{V_g I_g}{2V_-} - \frac{V_g I_g}{V_-} \sin^2 \omega t + \frac{V_g I_g}{2V_+})}{dt} \\
&= -\omega I_g \cos \omega t - \frac{V_g I_g}{V_-} \times 2 \sin \omega t \times \omega \cos \omega t \\
&= -\omega I_g \cos \omega t - \frac{2\omega V_g I_g}{V_-} \sin \omega t \cos \omega t.
\end{aligned}$$

In order to extract the maximum value of the current $i_{L\rho}$, let $\frac{di_{L\rho}}{dt} = 0$. That is

$$-\omega I_g \cos \omega t - \frac{2\omega V_g I_g}{V_-} \sin \omega t \cos \omega t = 0.$$

There are four possible solutions, which depend on system parameters. Among the four solutions, there are two solutions for sure, which are

$$\begin{aligned}
t_1 &= \frac{\pi}{2\omega} \\
t_2 &= \frac{3\pi}{2\omega}.
\end{aligned}$$

On the other hand, there are another two solutions

$$\begin{aligned}
t_3 &= \frac{\pi}{\omega} + \frac{1}{\omega} \arcsin \frac{V_{-\rho}}{2V_g} \\
t_4 &= \frac{2\pi}{\omega} - \frac{1}{\omega} \arcsin \frac{V_{-\rho}}{2V_g}
\end{aligned}$$

if $V_- \leqslant 2V_g$. Specially, there is $t_3 = t_4 = t_2 = \frac{3\pi}{2\omega}$ when $V_- = 2V_g$.

The maximum value of the current $i_{L\rho}$ may be reached with any one of the above four

solutions, which depends on system parameters. Since there are four possible solutions, there are four possible peak values of the current $i_{L\rho}$. With solutions t_1 and t_2, the peak currents are

$$i_{L\rho p}\big|_{t=t_1} = I_g + \frac{V_g I_g}{2V_-} - \frac{V_g I_g}{2V_+} \tag{8.32}$$

and

$$i_{L\rho p}\big|_{t=t_2} = I_g - \frac{V_g I_g}{2V_-} + \frac{V_g I_g}{2V_+}. \tag{8.33}$$

Note that $i_{L\rho p}\big|_{t=t_1} \neq i_{L\rho p}\big|_{t=t_2}$ unless $V_+ = V_{-\rho}$.

On the other hand, the peak currents reached at $t = t_3$ and $t = t_4$ are the same. There is

$$\begin{aligned} i_{L\rho p}\big|_{t=t_3,t_4} &= -I_g(-\frac{V_-}{2V_g}) + \frac{V_g I_g}{2V_-} - \frac{V_g I_g}{V_-}(-\frac{V_-}{2V_g})^2 + \frac{V_g I_g}{2V_+} \\ &= \frac{V_- I_g}{2V_g} + \frac{V_g I_g}{2V_-} - \frac{V_g I_g}{V_-}\frac{V_-^2}{4V_g^2} + \frac{V_g I_g}{2V_+} \\ &= \frac{V_- I_g}{2V_g} + \frac{V_g I_g}{2V_-} - \frac{V_- I_g}{4V_g} + \frac{V_g I_g}{2V_+} \\ &= \frac{V_- I_g}{4V_g} + \frac{V_g I_g}{2V_-} + \frac{V_g I_g}{2V_+}. \end{aligned} \tag{8.34}$$

The maximum value of the current $i_{L\rho}$ can be obtained when $t = t_1$, $t = t_2$ or $t = t_3$, t_4, which depends on system parameters.

For the θ-converter, it is much more straightforward to know the maximum value of the inductor current i_L because of the absence of the second-order component $\frac{V_g I_g}{2V_-}\cos 2\omega t$. According to (8.17), the maximum current flowing through the inductor L_N is $i_{Lmax} = I_g + \frac{V_g I_g}{2V_+}$ in the θ-converter.

In order to identify the relation between the inductor current in the two converters, the i_{Lmax} is compared to $i_{L\rho p}\big|_{t=t_1}$, $i_{L\rho p}\big|_{t=t_2}$ and $i_{L\rho p}\big|_{t=t_3,t_4}$, respectively.

The difference between i_{Lmax} and $i_{L\rho p}\big|_{t=t_2}$ is $\frac{V_g I_g}{2V_-}$, which is always greater than zero. As a result, $i_{Lmax} > i_{L\rho p}\big|_{t=t_2}$ is always true.

Moreover, the difference between the i_{Lmax} and the $i_{L\rho p}\big|_{t=t_3,t_4}$ is

$$\begin{aligned} i_{Lmax} - i_{L\rho p}\big|_{t=t_3,t_4} &= I_g + \frac{V_g I_g}{2V_+} - \frac{V_- I_g}{4V_g} - \frac{V_g I_g}{2V_-} - \frac{V_g I_g}{2V_+} \\ &= I_g(1 - (\frac{V_-}{4V_g} + \frac{V_g}{2V_-})) \end{aligned}$$

Since $V_g \leqslant V_- \leqslant 2V_g$ when $t = t_3, t_4$, there is

$$\frac{\sqrt{2}}{2} \leqslant \frac{V_-}{4V_g} + \frac{V_g}{2V_-} \leqslant \frac{3}{4}.$$

In this case, $i_{Lmax} - i_{L\rho p}\big|_{t=t_3,t_4} > 0$, which means $i_{Lmax} > i_{L\rho p}\big|_{t=t_3,t_4}$.

The difference between the i_{Lmax} and the $i_{L\rho p}\big|_{t=t_1}$ is

$$\begin{aligned} i_{Lmax} - i_{L\rho p}\big|_{t=t_1} &= I_g + \frac{V_g I_g}{2V_+} - I_g - \frac{V_g I_g}{2V_-} + \frac{V_g I_g}{2V_+} \\ &= \frac{V_g I_g}{V_+} - \frac{V_g I_g}{2V_-}. \end{aligned}$$

As a result, there are $i_{Lmax} > i_{L\rho p}\big|_{t=t_1}$ when $V_+ < 2V_-$ and $i_{Lmax} < i_{L\rho p}\big|_{t=t_1}$ when $V_+ > 2V_-$. Specially, $i_{Lmax} = i_{L\rho p}\big|_{t=t_1}$ when $V_+ = 2V_-$.

To sum up, the maximum current flowing through the inductor L_N in the θ-converter is higher than that in the ρ-converter when $V_+ < 2V_-$. On the other hand, this maximum current in the θ-converter is lower than that in the ρ-converter when $V_+ > 2V_-$. The two converters have the same maximum inductor current when $V_+ = 2V_-$.

8.6 Control Design

In general, there are three control objectives, i.e. to maintain the output voltage V_+, to maintain the DC-bus voltage V_{DC} and to control the grid current i_g. The first objective is mainly achieved by the control of the neutral leg while the others are mainly achieved by the control of the conversion leg. In this section, the controllers for both legs are presented. Note that the control of the two legs are independent from each other and hence, the design of the controllers is very flexible. Again, only the rectification mode is considered here.

8.6.1 Control of the Neutral Leg

Regardless of switching components, there might exist two main components, i.e. a DC component and a low-frequency component, in the output voltage V_+. In order to maintain the voltage V_+, both components are needed to be considered.

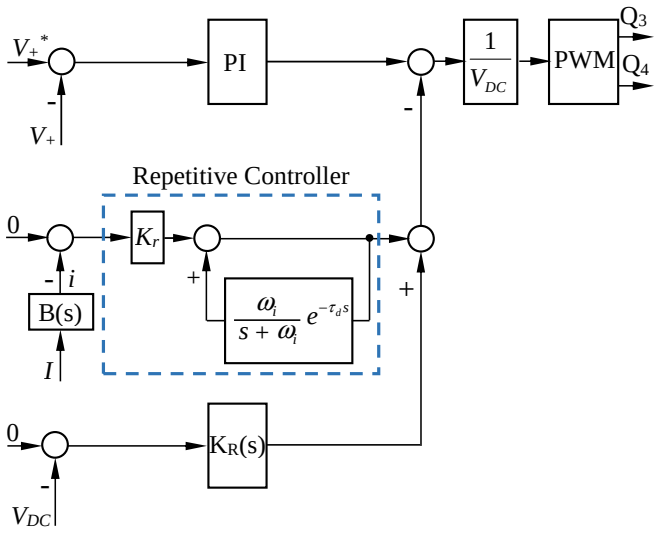


Figure 8.4: Controller for the neutral leg.

8.6.1.1 Regulation of the DC component of the V_+

The DC component of the voltage V_+ needs to be maintained at its reference according to load requirement. In order to achieve this, the voltage V_+ should be measured as a feedback and then a simple proportional-intergral (PI) controller can be used as shown in Figure 8.4.

8.6.1.2 Removal of the low-frequency component in the V_+

Here, the DC-bus current I is measured as a feedback and the aim is to remove low-frequency component in the current I. By doing this, the low-frequency component in the V_+ can be removed because the current flowing through the output capacitor becomes ripple-free. For this purpose, there is a need to first extract the low-frequency component in the current I. Note that the current I contains a DC component, a switching-frequency component and a low-frequency component. Here, a band pass filter

$$B(s) = \frac{10000s}{(s+10)(s+10000)}$$

is used as shown in Figure 8.4. The reference of the extracted low-frequency component is set to be zero and the left work is to design a current controller. Because of high performance to handle harmonics, a repetitive current controller is adopted, which is formed by a

proportional gain K_r and an internal model

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where τ_d is designed as (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a)

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\mathrm{s}$$

with $\omega_i = 2550$, $\tau = 0.02\,\mathrm{s}$.

8.6.1.3 Removal of the fundamental component in the V_{DC}

Since the low-frequency component in the current I is removed, there is

$$i_C = i_g(1-d_2) + i_L(1-d_4) - I_R.$$

It can be found that the capacitor current i_C may contain a fundamental component because the grid current i_g and the inductor current i_L are in fundamental frequency. However, it is expected that the current i_C only has a second-order component and should not function as the return path of the grid current. Fundamental components required to form the return grid current should be provided by the neutral leg not the capacitor C. Since the key objective of the controller is not to remove the fundamental component in the V_{DC}, it is permitted for the V_{DC} to have some fundamental ripples. A simple controller is enough if the fundamental component can be limited at a low level. Here, the following resonant controller (Castilla et al., 2009; Shen et al., 2010)

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{8.35}$$

of which the gain at frequency $h\omega$ is K_h with zero phases, is adopted to reduce the fundamental component. In order to tune the controller at the fundamental frequency, ξ and h are chosen as 0.01 and 1, respectively. The gain K_h can be tuned by trial-and-error in experiments.

As shown in Figure 8.4, the final duty cycle is formed by the sum of the above three loops. Since the loops are decoupled in frequency domain, they can be added together

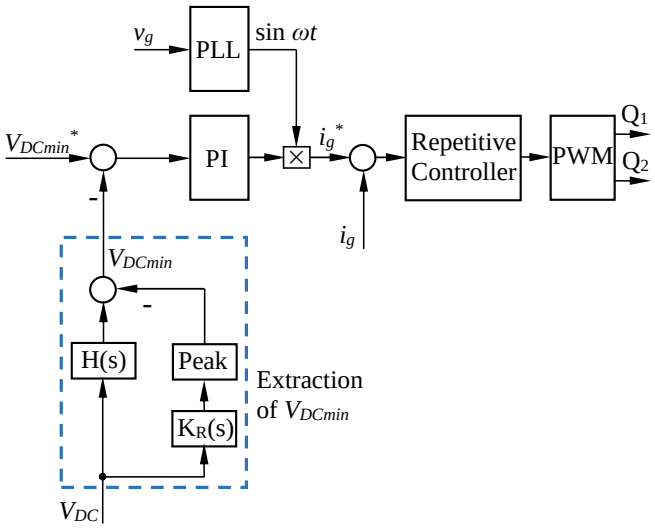


Figure 8.5: Controller for the conversion leg.

without affecting the other loops. As long as each loop is stable, the stability of the whole controller can be guaranteed.

8.6.2 Control of the Conversion Leg

8.6.2.1 Control of the grid current i_g

In order to achieve the unity power factor, it is desirable to control the grid current to be in phase with the grid voltage. Also, the grid current is expected to have low harmonics so as to avoid introducing power pollution to the grid. The repetitive controller used for the neutral leg is again adopted here to improve the tracking performance of the grid current. The left work is to generate the reference of the grid current, which should be in phase with the grid voltage. As a result, the phase signal of the grid voltage needs to be extracted. A phase-locked-loop (PLL) (Ziarani and Konrad, 2004) is used for this purpose as shown in Figure 8.5. Apart from the phase signal, the peak value of the grid current is required. According to the power balance between the AC and DC sides, this value can be obtained if the DC-bus voltage V_{DC} is maintained at its reference, which is discussed in the next paragraph.

8.6.2.2 Regulation of minimum value of the V_{DC}

It is possible to control the maximum, average and minimum values of the voltage V_{DC}. Compared to controlling the average voltage, controlling the maximum and minimum voltages have more benefits. For example, if the maximum voltage is controlled, then the DC-bus voltage can always reach to highest level for different loads, which helps to reduce the total capacitance required. On the other hand, if the minimum voltage is controlled, then the DC-bus voltage always has lowest values for different loads. In this case, the converter has better performance on the efficiency because switching losses are reduced because of the minimised DC-bus voltage. Here, the minimum value of the voltage V_{DC} is set as the control target. The extraction of the minimum value from the measured V_{DC} can be achieved by using the average value minus the peak value of the $\triangle V_{DC}$. The average value of the V_{DC} can be easily obtained by using the following hold filter

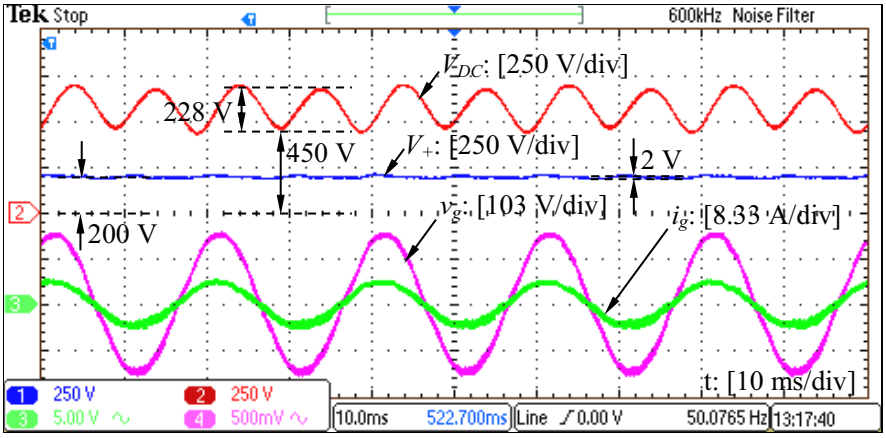
$$H(s) = \frac{1 - e^{-Ts}}{Ts} \tag{8.36}$$

where T is the fundamental period of the grid voltage, as shown in Figure 8.5. At the same time, the measured voltage V_{DC} is sent to the $K_R(s)$ with $\xi = 0.01$, $h = 2$ and $K_h = 1$. Then, the needed peak value of the $\triangle V_{DC}$ can be extracted by squaring the $\triangle V_{DC}$ with the result sent to a hold filter. Then the minimum value of the voltage V_{DC} can be obtained by using the average value of the V_{DC} to minus the peak value of the $\triangle V_{DC}$ (see Figure 8.5). Here, a simple PI is used as the voltage controller to generate the right peak value of the grid current.

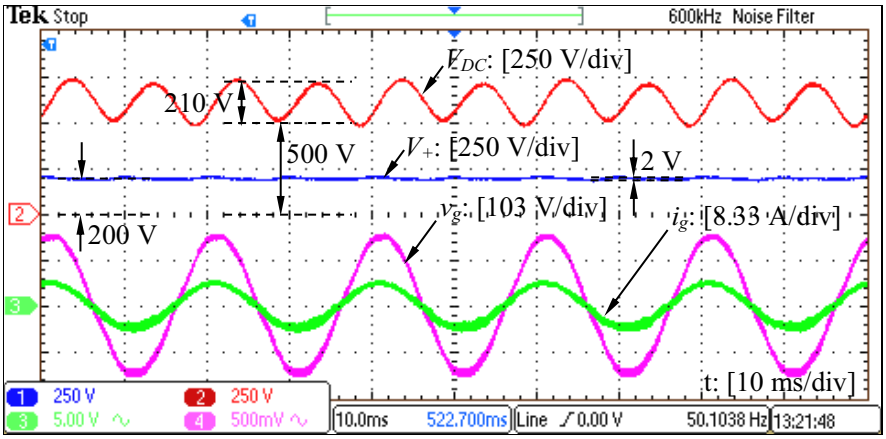
8.7 Experimental Results

In order to validate the proposed system, intensive experiments were conducted on a prototype, which is based on IGBTs controlled by TMS320F28335 DSP. The system parameters used for experiments are the same as those summarised in Table 8.1. Here, a 5 μF and a 6 μF metallized polypropylene film capacitors are used as the capacitors C_+ and C in experiments, respectively. Compared to conventional converters, the total capacitance required in the θ-converter is reduced by about 172 times from 1900 μF to 11 μF. Both steady-state and transient performance were tested and the corresponding results are shown in Figure

Case I: $V^*_{DCmin} = 450$ V

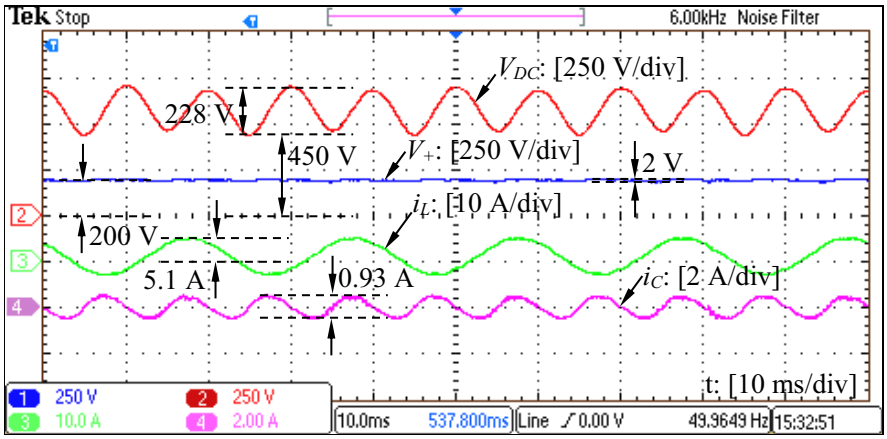


Case II: $V^*_{DCmin} = 500$ V

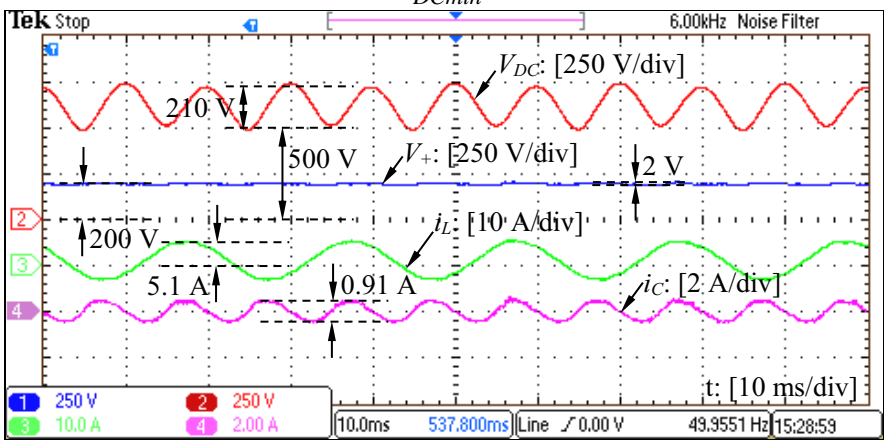


(a)

Case I: $V^*_{DCmin} = 450$ V



Case II: $V^*_{DCmin} = 500$ V



(b)

Figure 8.6: The steady-state performance of the θ-converter when $V^*_+ = 200$ V: (a) grid voltage v_g, grid current i_g and DC voltages V_+ and V_{DC} ; (b) inductor current i_L and capacitor current i_C.

8.6-8.9. Moreover, similar experiments for the ρ-converter were also conducted in order to validate the comparison between the θ-converter and the ρ-converter. The related results are shown in Figure 8.10. Note that a 10 μF metallized polypropylene film capacitor is used as the capacitor C_- in the θ-converter in order to keep the voltage V_{DC} to be similar. The capacitor C_+ in both converters is kept the same, which is 5 μF.

8.7.1 System Steady-state Performance

In order to test the system steady-state performance, both the cases with $V^*_{DCmin} = 450$ V and $V^*_{DCmin} = 500$ V were considered. The obtained experimental results can be found in Figure 8.6.

8.7.1.1 Grid current i_g and DC voltages V_+ and V_{DC}

As shown in Figure 8.6(a), the grid current i_g was always well controlled to be in phase with the grid voltage for both cases. According to the recorded experimental data, the total harmonic distortion (THD) of the grid current is around 4%, which is already very low because no special efforts were made to improve the power quality of the grid current. Moreover, the power factor was above 0.99 for both cases and hence, the unity power factor is achieved.

Apart from the grid current, the DC output voltage V_+ is also well maintained. Importantly, it has very low voltage ripples for both cases, which are about 2 V. Most of the system ripple power is now stored in the capacitor C instead of the output capacitor C_- and hence, the voltage across the capacitor C, i.e. the voltage V_{DC}, has very large voltage ripples as shown in Figure 8.6(a). When $V^*_{DCmin} = 450$ V, there is $\triangle V_{DC} = 228$ V, which is much larger than the output voltage ripple. According to (8.8), the voltage $\triangle V_{DC}$ is decreased along with the increase of the V_{DCmin}. Indeed, the voltage $\triangle V_{DC}$ was decreased to 210 V when V^*_{DCmin} was raised to 500 V (compare the left column and right column of Figure 8.6(a)).

8.7.1.2 The currents i_L and i_C

According to (8.6), the inductor current i_L contains a DC component and a fundamental component. As shown in Figure 8.6(b), the i_L indeed has a DC component and an AC component in fundamental frequency. It can be found that the DC offset is around 0.9 A,

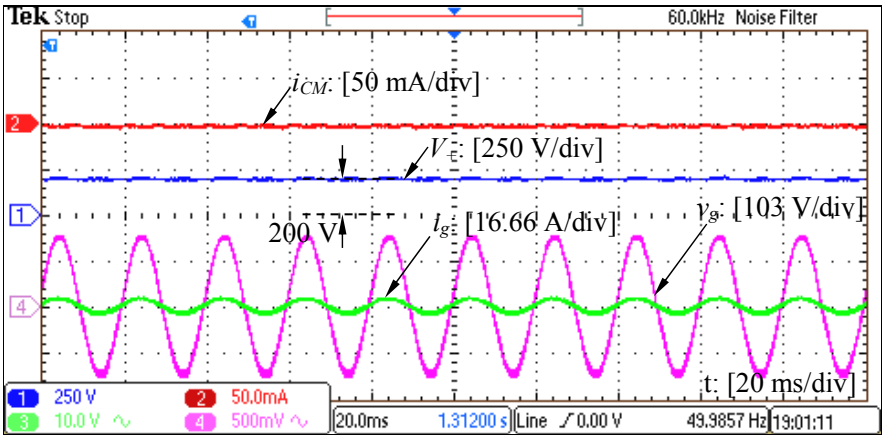


Figure 8.7: The measured CM current i_{CM}

which is almost equal to the theoretical DC current $I_{DC} = \frac{200}{220} \approx 0.909$ A. Also, it can be found that the fundamental component in the i_L has the same phase and peak-peak value as the grid current. Note that a 6 kHz noise filter was applied to filter out switching-frequency component in the currents so that it is possible to clearly see the other components.

According to (8.15), the current i_C should be mainly composed by a second-order component (without considering switching-frequency component). Indeed, the measured i_C is in second order as shown in Figure 8.6(b). Compared to the Case I, the peak-peak value of the current i_C in Case II is lower because of the higher V_{DC} , which is consistent with (8.16).

8.7.1.3 The CM current i_{CM}

A 0.47 μF capacitor was connected as the parasitic capacitor and the current flowing through this capacitor is the CM current i_{CM}. The measured i_{CM} is shown in Figure 8.7. It is clear that the i_{CM} is indeed zero. As a result, the objective to eliminate CM current is achieved.

8.7.2 System Transient Response

In order to test the system dynamic performance, two transient cases (system start-up and change of the output voltage) are considered.

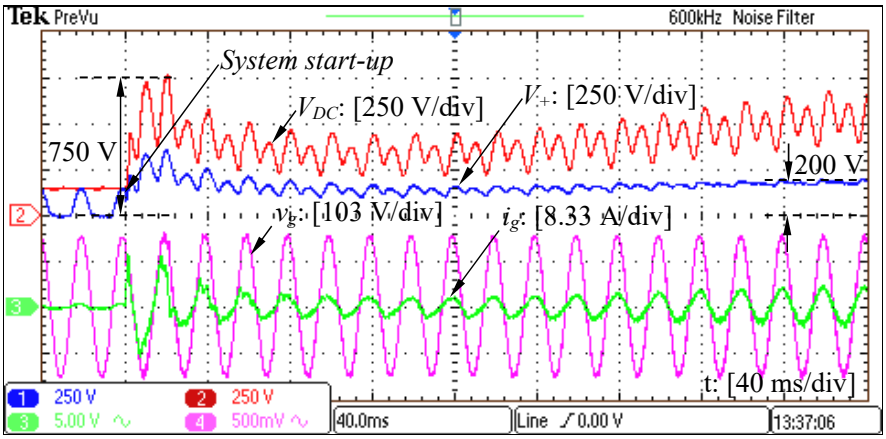


Figure 8.8: System start-up

8.7.2.1 System start-up

As shown in Figure 8.8, the system was disabled first and then was suddenly started. It can be seen that the output voltage V_+ was quickly regulated to its reference (200 V) and the whole start-up period only took about 12 fundamental cycles. During the start-up, the grid current was first dramatically increased to charge the output capacitor and then was quickly decreased to its steady-state value.

8.7.2.2 Change of the output voltage

Another experiment was done by changing the reference of the output voltage V_+ from 200 V to 300 V. As shown in Figure 8.9, the output voltage V_+ was smoothly increased to 300 V without any spikes. It is worth highlighting that the ripples of the voltage V_+ were always maintained at very low levels during the whole transient period. It took about 1.6 s for this transient response. The relatively slow response is because of the limited maximum current of the inductor L_N, which is about 5 A. If higher than 5 A, the inductor L_N may become saturated. Accordingly, system gains are limited and the result is the slow transient response. In other words, the transient response can be much faster if system gains are increased.

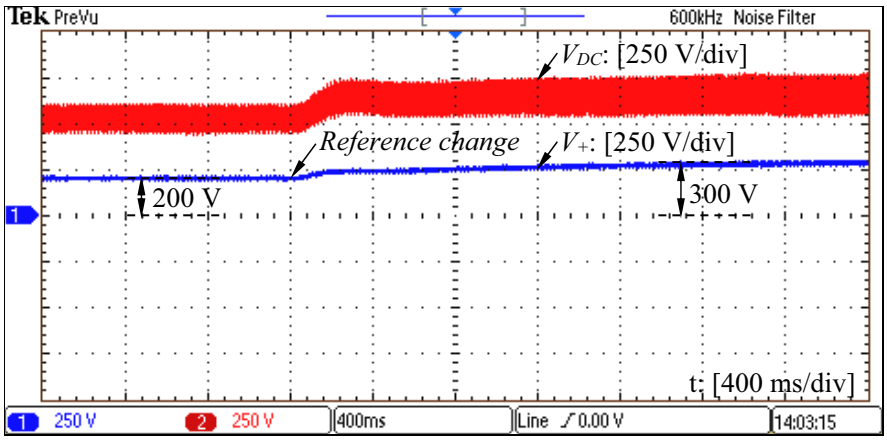
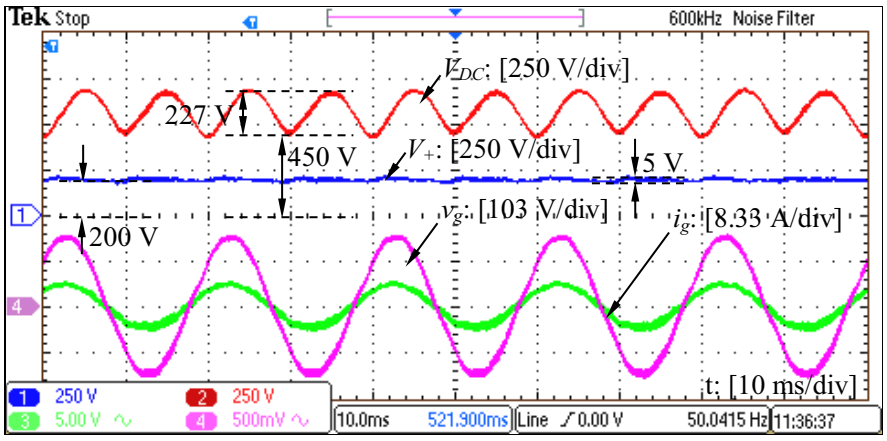
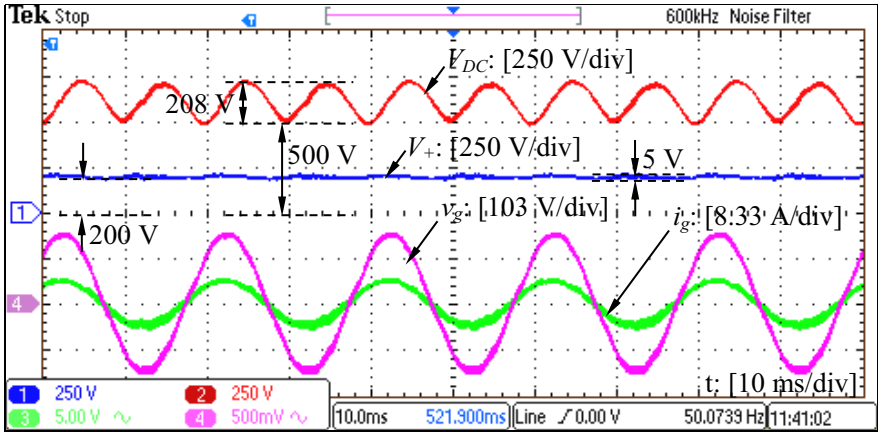


Figure 8.9: System transient response when the reference of the voltage V_+ was changed from 200 V to 300 V

Case I: $V^*_{DCmin} = 450$ V

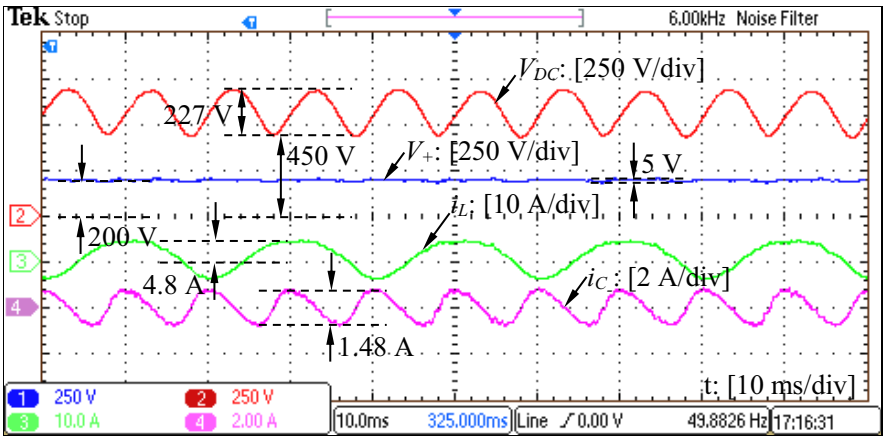


Case II: $V^*_{DCmin} = 500$ V

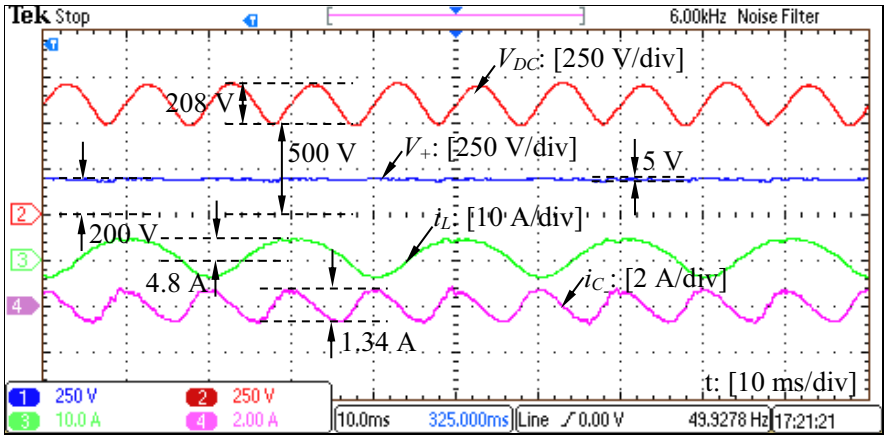


(a)

Case I: $V^*_{DCmin} = 450$ V



Case II: $V^*_{DCmin} = 500$ V



(b)

Figure 8.10: The steady-state performance of the ρ-converter when $V^*_+ = 200$ V: (a) grid voltage v_g, grid current i_g and DC voltages V_+ and V_{DC}; (b) inductor current i_L and capacitor current $i_{C\_}$.

8.7.3 Comparison with the ρ-converter

As shown in Figure 8.10, the Case I with $V^*_{DCmin} = 450$ V and the Case II with $V^*_{DCmin} = 500$ V were considered for the ρ-converter.

8.7.3.1 Output voltage ripples

Compared to the output voltage V_+ shown in Figure 8.6(a), the output voltage V_+ in Figure 8.10(a) obviously has larger ripples. To be more precise, the ripples of the output voltage V_+ were increased from 2 V to 5 V. On the other hand, the ripples of the DC-bus voltage V_{DC} were kept almost the same on purpose. As a result, the θ-converter has better performance on the reduction of output voltage ripples, which is consistent with the analysis made in Section 8.5.

8.7.3.2 The current i_L

As discussed before, the only difference of the current i_L in the θ-converter and the ρ-converter is the second-order component. As shown in Figure 8.10(b), the i_L in the ρ-converter indeed has a second-order component, which makes the top of the i_L becomes flat. On the other hand, the i_L in the θ-converter does not have this component (see 8.6(b)).

Moreover, there are $i_{Lmax} = 5.1$ A and $i_{L\rho max} = 4.8$ A with $V_+ < 2V_-$, which are consistent consistent with the theoretical analysis made in Section 8.5.6.

8.7.3.3 The capacitor currents i_C and i_{C_-}

As can be seen from Figure 8.6(b) and Figure 8.10(b), the peak-peak value of the capacitor current i_C (about 0.93 A) in the θ-converter is lower than that of the capacitor current i_{C_-} (around 1.48 A) in the ρ-converter. This is consistent with (8.30).

8.8 Summary

The θ-converter with common AC and DC ground has been proposed in this chapter. Both isolation transformers and bulky electrolytic capacitors have been removed from the converter. The removal of isolation transformers is naturally achieved because of the common

AC and DC ground. At the same time, the output capacitor is significantly reduced because it does not need to process any low-frequency ripples and only needs to be sized for switching-frequency ripples. All the system ripple power is stored on another capacitor, which is connected across the DC bus. The stored ripple power is *instantaneously* equal to the system ripple power. As a result, the system performance to reduce output voltage ripples is promising. Since the DC-bus voltage (higher than the output voltage) does not supply any loads, it is designed to have large voltage ripples on purpose. In this case, only a small capacitor is needed in order to store all the system ripple power. As a result, the total capacitance required is significantly reduced compared to that of conventional converters. Moreover, the normal objectives of conventional converters like unity power factor have been achieved without any compromise. Importantly, all the above objectives are achieved by two legs with only four switches and hence, the θ-converter is very compact. It is very flexible to design controllers for the two legs because they are independent from each other. Intensive experimental results have been presented to validate the performance of the converter.

Chapter 9

θ-converters with Significantly-Reduced Neutral Inductor

Following the development of the θ-converter to eliminate low-frequency voltage ripples and high-frequency CM voltages, this chapter is focused on further improving the performance of the θ-converter. The improvement is achieved by the reduction of a passive component in the θ-converter, i.e., the neutral inductor. The location of the inductor in the θ-converter is changed but without affecting the other functions of the converter. It is analysed and verified by experiments that the current flowing through the inductor can be reduced at least three times and hence, the size of the inductor can be reduced by at least about nine times. Together with the significantly-reduced required capacitance, the proposed converter becomes a very competitive solution to single-phase converters. How to operate the system to achieve the reduction of the inductor and the capacitors is discussed in detail. Moreover, selection criteria on passive components used in the proposed converter are discussed in order to minimise their usage. Intensive experimental results are presented to demonstrate that the proposed converter can indeed reduce the inductor current while the other functions of the θ-converter are well maintained.

9.1 Introduction

As discussed in Chapter 8, the θ-converter can achieve the elimination of the transformers and the reduction of required capacitors in the widely-used asymmetrical single-phase power grid. As shown in Figure 9.1, the θ-converter is very compact because only four

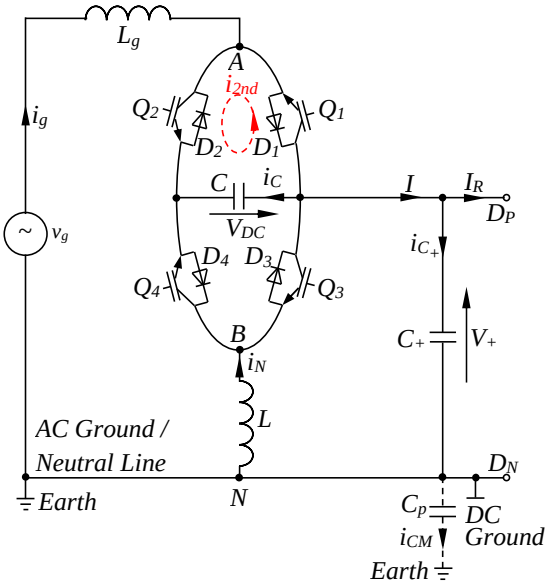


Figure 9.1: The θ-converter.

switches are used. The AC and DC ground is common so that CM currents can be naturally eliminated. At the same time, the reduction of required capacitors is achieved by diverting ripple energy from the output capacitor to another capacitor, which is designed to hold large ripples because it does not supply any loads. As a result, both capacitors can be very small. It has been analysed and verified by experiments that the total required capacitance can be reduced by above 172 times compared to that in conventional single-phase converters. Highly-reliable film capacitors can then be cost-effective to be used. As a result, the θ-converter can be a very competitive solution to high power density and high reliability single-phase converters.

Apart from the four switches and the two film capacitors, there are still two inductors in the θ-converter. One of the inductors is connected to the grid for the purpose of controlling the grid current, which is common in power converters. Another inductor is specially used for the control of the DC output voltage of the converter, which does not exist in other power converters. The current flowing through this inductor is the sum of the grid current and the DC output current, which can be high. Inevitably, the size of this inductor becomes very large, which degrades the system power density.

In this chapter, an improved θ-converter is developed to reduce the size of the inductor through reducing the current carried by the inductor. The inductor is moved away from the

return path of the grid current. As a result, it only carries the DC output current. Since the maximum value of the DC output current is much smaller compared to that of the grid current, the current flowing through the inductor can be reduced compared to that in the θ-converter. Accordingly, the size of the inductor becomes smaller. According to the analysis presented later, the current can be reduced by about at least three times and the corresponding reduction of the size of the inductor is about at least nine times. Together with the reduced requirement on capacitors, the proposed converter is very suitable for volume- and weight-critical long-life applications.

The following parts of this chapter are organized as follows. In Section 9.2, the topology, features and the operation of the proposed converter are analysed. After that, how to reduce the inductor current and the required capacitance is discussed in Section 9.3 and the Section 9.4, respectively. With the aim to minimise the usage of passive components, their selection criteria are presented in Section 9.5. The performance of the proposed converter is then fully evaluated in Section 9.6. Experimental results are provided in Section 9.7 for verification followed by the summary made in Section 9.8.

9.2 The Proposed Converter

9.2.1 Topology, Features and Operation Principles

9.2.1.1 Topology

As shown in Figure 9.2(a), the proposed converter consists of two legs, i.e. the conversion leg and the neutral leg, with only four switches. The grid is connected between points A and N with a series inductor L_g. On the other hand, the DC load is connected between points D_P and D_N. In this case, the DC output voltage is the V_+ not the V_{DC}. Another inductor, i.e. L, is added in order to enable the regulation of the voltage V_+.

The proposed converter can be formed by only changing the location of the inductor L in the θ-converter. Despite of a small change, the reduction of the current flowing through the inductor L is achieved without affecting the other functions of the system. Detailed discussions on how to achieve the reduction are made later.

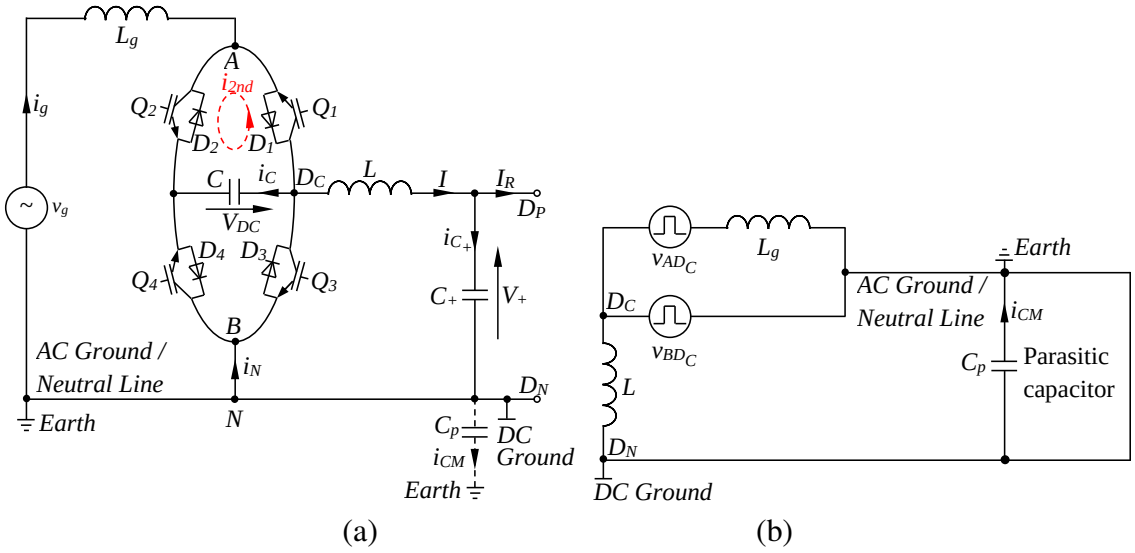


Figure 9.2: The proposed converter: (a) topology; (b) equivalent circuit for analysing the CM current.

9.2.1.2 Features

One of important features of the converter is the common AC and DC ground. To be more precise, the AC ground point N and the DC ground point D_N are directly connected together as shown in Figure 9.2(a). The resulted benefit is the completely eliminated CM current. In order to clearly demonstrate the removal of CM current, the equivalent circuit for analysing the CM current is shown in Figure 9.2(b). The parasitic capacitor C_p is actually short-circuited because of the common AC and DC ground. Accordingly, the current flowing through the C_p, i.e. the CM current i_{CM}, is completely eliminated. In this case, isolation transformers are no longer required and can be removed from the converter without causing large CM current.

Another important feature of the converter is the significantly-reduced capacitance required. It is well known that the power in single-phase converters contains a second-order component, which results in second-order voltage ripples at the DC side. Bulky capacitors are often required to smooth the ripples in conventional converters. For the proposed converter, there are two capacitors C and C_+. The capacitor C_+ is the output capacitor and hence, it should be with low voltage ripples. On the other hand, the voltage across the C can be with large ripples because the capacitor C is not connected to any loads. Through proper control of the proposed converter, most of the system ripple energy can be diverted

to the capacitor C instead of the capacitor C_+. Accordingly, the capacitor C_+ can be very small because it does not need to process any low-frequency ripple energy. At the same time, the capacitor C_+ can be also very small because it can hold large voltage ripples as discussed before. As a result, the total capacitance required, i.e. $C + C_+$, is very small. Compared to that of conventional single-phase converters, the capacitance is significantly reduced. Detailed theoretical analysis on the reduction is presented later, which is also verified by experiments.

Compared to the θ-converter, the proposed converter has an unique feature: the current flowing through the inductor L, i.e. i_L, is reduced. The current i_L in the proposed converter is reduced by at least three times compared to that in the θ-converter. The main benefit resulting from the reduced current is the reduced size of the inductor L, which becomes at most one-ninth of the size of the L in the θ-converter.

9.2.1.3 Operation principles

The conversion leg is composed by the inductor L_g and the Switches Q_1 and Q_2, which is mainly responsible to control the power exchanged between the AC and DC sides of the converter. Note that both switches are in bidirectional, which means the converter has the capability to bidirectionally process both real and reactive power. The two switches are operated in a complementary way. In practice, a certain amount of dead time is required in order to avoid shoot-through problem.

At the same time, the neutral leg is formed by the inductor L, the capacitors C and C_+ and the Switches Q_3 and Q_4. Again, these two switches are operated in complementary. The operation of the neutral leg is similar to that of a bidirectional DC/DC converter. The main objective of the neutral leg is to maintain the DC voltage V_+, which might contain both DC and second-order components.

9.2.2 Circuit Analysis

9.2.2.1 Average circuit model

In order to achieve the unity power factor, the grid current should be controlled to be in phase with the grid voltage. With this assumption, the grid voltage and the grid current can

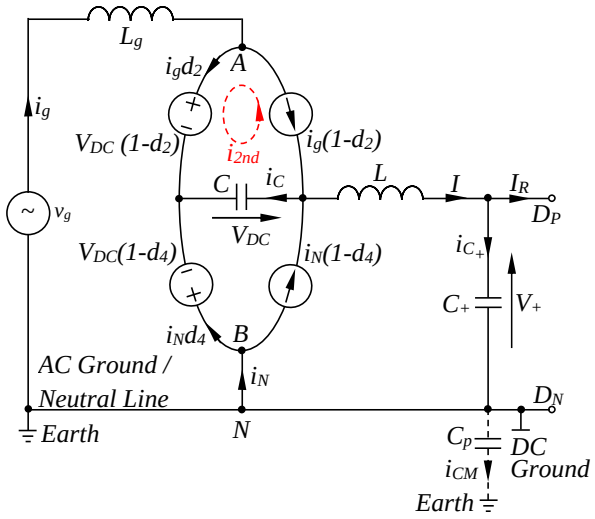


Figure 9.3: Average circuit model of the proposed converter.

be denoted as

$$\begin{aligned} v_g &= V_g \sin \omega t \\ i_g &= I_g \sin \omega t, \end{aligned}$$

respectively, where V_g is the peak grid voltage, I_g is the peak grid current and ω is the grid angular frequency.

As demonstrated in (Srinivasan and Oruganti, 1998; Tymerski et al., 1989), there is

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t$$

where d_2 is the duty cycle of the Switch Q_2 and, V_+ and V_{DC} are the voltages across the capacitors C_+ and C, respectively. Since the Q_1 and Q_2 are operated in complementary, the duty cycle of the Switch Q_1 is

$$\begin{aligned} d_1 &= 1 - d_2 \\ &= \frac{V_-}{V_{DC}} + \frac{V_g}{V_{DC}} \sin \omega t \end{aligned} \tag{9.1}$$

where $V_- = V_{DC} - V_+$. Hence, the average circuit model of the conversion leg can be built as shown in Figure 9.3. The switches Q_1 and Q_2 are represented by a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, respectively.

Table 9.1: Summary of operation modes

Mode	Q_1	Q_2	Q_3	Q_4	v_{AB}
1	0	1	0	1	0
2	1	0	0	1	V_{DC}
3	1	0	1	0	0
4	0	1	1	0	$-V_{DC}$

Similarly, the model of the neutral leg can be built. As shown in Figure 9.3, the Switches Q_3 and Q_4 are represented by a current source $i_L(1-d_4)$ and a voltage source $V_{DC}(1-d_4)$, respectively. For the neutral leg, it is actually operated as a DC/DC converter. In this case, the duty cycle of the Switch Q_4 is

$$d_4 = \frac{V_+}{V_{DC}}. \tag{9.2}$$

Due to the complementary operation, the duty cycle of the Switch Q_3 is

$$\begin{aligned} d_3 &= 1-d_4 \\ &= \frac{V_-}{V_{DC}}. \end{aligned} \tag{9.3}$$

9.2.2.2 Operation modes and modulation strategy

According to the on and off state of the four switches, different modes of the proposed converter are resulted, which are summarised in Table 9.1. Since the two switches of the same leg are operated in complementary, there are four modes in total. In Mode 1 and Mode 3, the voltage between points A and B, i.e. v_{AB}, is 0. On the other hand, the voltage v_{AB} is V_{DC} and $-V_{DC}$ in the Mode 2 and Mode 4, respectively. The four modes of the circuit are shown in Figure 9.4(a)-(d), respectively. For a certain mode, solid lines are paths to carry currents while paths denoted by dashed lines do not carry currents in this mode. It should be mentioned that currents can flow through either diodes or transistors of switches. During the Mode 1, the positive half cycle of the grid current flows through the transistor of the Switch Q_2 and then the diode of the Switch Q_4 while the negative half cycle flows through the transistor of the Switch Q_4 and then the diode of the Switch Q_2. Similar analysis can be made for the other modes.

Since the two legs have their own objectives, both of them need to be operated at high frequency. Due to the lower grid current ripples, the bipolar PWM is adopted here. As

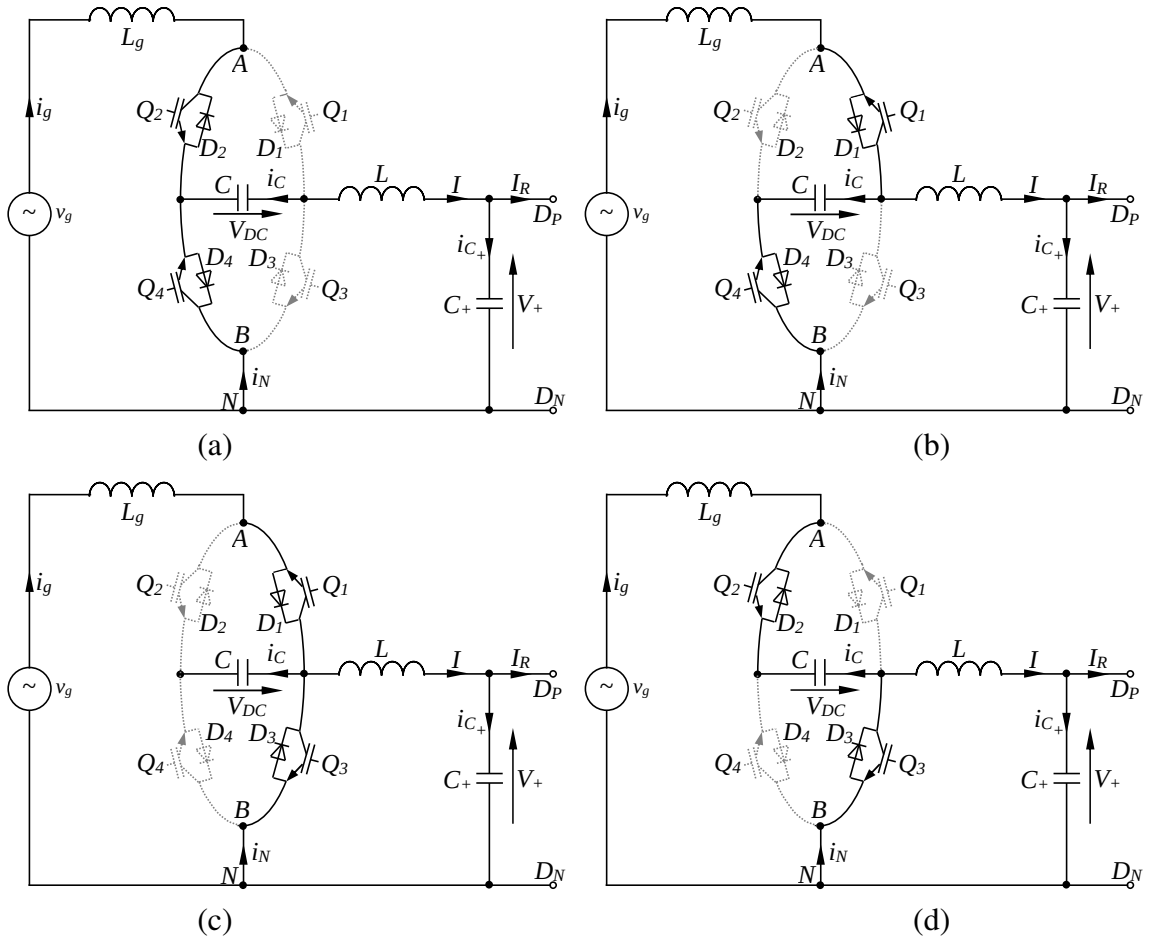


Figure 9.4: Operation modes of the proposed converter: (a) mode 1 ($v_{AB} = 0$); (b) mode 2 ($v_{AB} = V_{DC}$); (c) mode 3 ($v_{AB} = 0$); (d) mode 4 ($v_{AB} = -V_{DC}$).

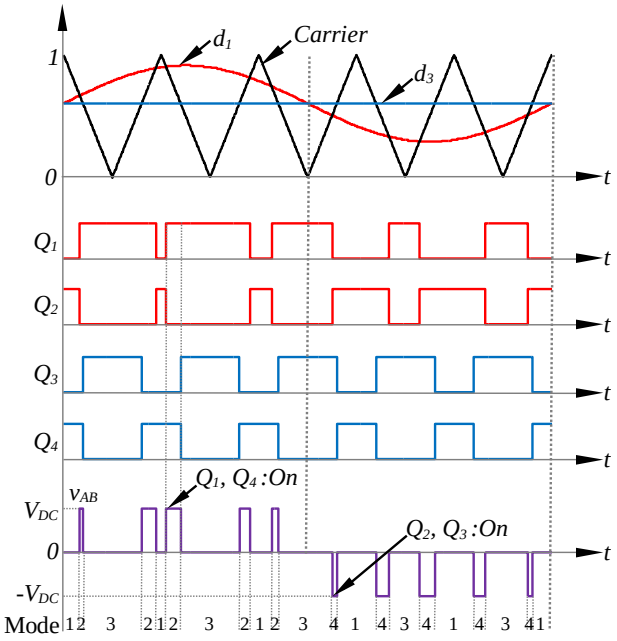


Figure 9.5: Bipolar operation of the proposed converter.

shown in Figure 9.5, the four switches are actually divided into two groups. The Switches Q_1 and Q_2 are modulated by d_1 while the Switches Q_3 and Q_4 are modulated by d_3. According to (9.1) and (9.3), the DC component in d_1 and d_3 is the same. The only difference is that there is a fundamental AC component in d_1. This leads a fact that d_1 is always higher than d_3 in the positive half cycle of d_1, while d_1 is always lower than d_3 in the negative half cycle of d_1. The resulted impact is that the on time of the Switch Q_1 is always longer than that of the Switch Q_3 in the positive half cycle. On the other hand, the on time of Switch Q_3 is always longer than that of the Switch Q_1 in the negative half cycle. In this case, the Mode 4 and Mode 2 do not appear in the positive and negative half cycles, respectively. It can be also observed that equivalent frequency of the voltage v_{AB} is higher than the switching frequency, which helps to reduce the size of the required inductor for the purpose of smoothing high-frequency ripples in the grid current.

During the positive half cycle, the circuit rotates in the sequence of "Mode 1, Mode 2, Mode 3 and Mode 2," and the voltage v_{AB} accordingly rotates in the sequence of "0, V_{DC}, 0 and V_{DC}". During the negative half cycle, the circuit rotates in the sequence of "Mode 4, Mode 1, Mode 4 and Mode 3," and the voltage v_{AB} accordingly rotates in the sequence of "$-V_{DC}$, 0, $-V_{DC}$ and 0".

9.3 Reduction of the Current Flowing through the Inductor L

In this section, the proposed converter is compared with the θ-converter mainly from the view of the inductor L. After a careful comparison between the two converters, it is confirmed that the only difference between the two converters is the location of the inductor L. To be more precise, the inductor L is put in the path of the current i_N in the θ-converter while it is put in the path of the current I in the proposed converter. As a result, the current flowing through the L, which is denoted as i_L, can be very different.

In order to facilitate the following analysis, i_L, V_+, V_{DC}, Q_1, Q_2, Q_3, Q_4, R, L_g and L in the θ-converter are denoted as $i_{L\theta}$, $V_{+\theta}$, $V_{DC\theta}$, $Q_{1\theta}$, $Q_{2\theta}$, $Q_{3\theta}$, $Q_{4\theta}$, R_θ, $L_{g\theta}$ and L_θ, respectively. i_L, V_+, V_{DC}, Q_1, Q_2, Q_3, Q_4, R, L_g and L are only referred to components of the proposed converter.

9.3.1 The Flowing Path of the Grid Current i_g

The grid current i_g is mainly controlled by the conversion leg in both converters. In this case, the i_g, of course, flows through the switches Q_1 and Q_2 and also the inductor attached to the conversion leg, i.e. L_g. As the return path of the grid current, the switches Q_3 and Q_4 also carry the grid current in both converters. The only difference is that the inductor L does not carry the i_g in the proposed converter while it does carry the i_g in the θ-converter. The components carrying the current i_g are summarised in Table 9.2. In this case, the currents i_L and $i_{L\theta}$ are obviously different.

9.3.2 Reduction of the Current and Size of the Inductor L

According to the average model of the proposed converter, there is

$$i_L = I_R = \frac{V_g}{2V_+} I_g$$

Table 9.2: Summary of components carrying i_g

	Components	Number of components
The proposed converter	Switches Q_1, Q_2, Q_3, Q_4 and the inductor L_g	5
The θ-converter	Switches $Q_{1\theta}$, $Q_{2\theta}$ $Q_{3\theta}$ and $Q_{4\theta}$, inductor $L_{g\theta}$ and inductor L_θ	6

without considering switching frequency components. On the other hand, there is

$$\begin{aligned} i_{L\theta} &= I_{R\theta} + i_{g\theta} \\ &= \frac{V_{g\theta}}{2V_{+\theta}} I_{g\theta} + I_{g\theta} \sin \omega t \end{aligned}$$

in the θ-converter. It is easy to find out that their maximum values are

$$\begin{aligned} i_{Lmax} &= \frac{V_g}{2V_+} I_g \\ i_{L\theta max} &= \frac{V_{g\theta}}{2V_{+\theta}} I_{g\theta} + I_{g\theta}, \end{aligned}$$

respectively. In order for a fair comparison, the two converters are supposed to be run at the same power level, which means $V_{g\theta} = V_g$, $I_{g\theta} = I_g$ and $V_{+\theta} = V_+$. In this case, there is

$$\begin{aligned} \frac{i_{L\theta max}}{i_{Lmax}} &= \frac{\frac{V_{g\theta}}{2V_{+\theta}} I_{g\theta} + I_{g\theta}}{\frac{V_g}{2V_+} I_g} \\ &= 1 + \frac{2V_+}{V_g}. \end{aligned} \tag{9.4}$$

Because $V_+ > V_g$ for ensuring the boost operation of the converter, it can be found that

$$\frac{i_{L\theta max}}{i_{Lmax}} > 3 \tag{9.5}$$

is always true. As a result, the maximum current flowing through the inductor L is reduced at least by three times in the proposed converter compared to that in the θ-converter. The

size of the inductor can be accordingly reduced. The ratio between the size of the inductor L in the two converters can be approximatively given as

$$\begin{aligned} r_L &= \frac{E_{L_\theta}}{E_L} \\ &= \frac{\frac{1}{2}Li_{L_{\theta max}}^2}{\frac{1}{2}Li_{Lmax}^2} \\ &= (\frac{i_{L_{\theta max}}}{i_{Lmax}})^2 > 9, \end{aligned} \tag{9.6}$$

which means the size of the inductor is reduced by at least nine times. As a result, the power density of the converter can be significantly improved.

9.4 Reduction of Output Voltage Ripples and Total Capacitance Required

9.4.1 Reduction of DC Output Voltage Ripples

The instantaneous power from the AC side is

$$\begin{aligned} p &= v_g i_g \\ &= V_g I_g \sin^2 \omega t \\ &= \frac{V_g I_g}{2} - \frac{V_g I_g}{2} \cos 2\omega t. \end{aligned}$$

Note that the power arising from the inductor L_g is neglected here in order to simplify the analysis, which is very small compared to the power p. It is clear that the instantaneous power is composed by a constant component $\frac{V_g I_g}{2}$ and a second-order ripple component $-\frac{V_g I_g}{2}\cos 2\omega t$. Due to the power balance between the AC and DC sides without considering power losses, both components appear at the DC side. Accordingly, there is

$$V_{DC} i_C + V_+ (i_{C_+} + I_R) = \frac{V_g I_g}{2} - \frac{V_g I_g}{2} \cos 2\omega t \tag{9.7}$$

in which the left part is the instantaneous power at the DC side. If the output voltage V_+ is ripple-free, there is

$$\frac{dV_+}{dt} = i_{C+} = 0$$

without considering switching-frequency ripples. Then, (4.9) becomes

$$V_{DC}i_C + V_+ I_R = \frac{V_g I_g}{2} - \frac{V_g I_g}{2}\cos 2\omega t. \tag{9.8}$$

Because of the power balance between the AC and DC sides (without considering losses), there is

$$V_+ I_R = \frac{V_g I_g}{2}. \tag{9.9}$$

and hence, (9.8) becomes

$$i_C = -\frac{V_g I_g}{2V_{DC}}\cos 2\omega t. \tag{9.10}$$

As mentioned above, the neutral leg is operated as a DC/DC converter and the (9.10) can be achieved by the control of the neutral leg. $i_{C_+} = 0$ is then naturally achieved and the output voltage V_+ becomes ripple-free.

9.4.2 Reduction of Total Capacitance Required

9.4.2.1 Reduction of the capacitor C_+

Since the capacitor C_+ does not process any low frequency ripples, a very small capacitor is already enough, which is mainly used to filter out high frequency ripples.

9.4.2.2 Reduction of the capacitor C

All the second-order ripple energy is now stored in the capacitor C and hence, the required capacitance is

$$\begin{aligned} C &= \frac{V_g I_g}{\omega \triangle V_{DC}(V_{DCmax} + V_{DCmin})} \\ &= \frac{V_g I_g}{2\omega \triangle V_{DC} V_{DCave}} \end{aligned} \tag{9.11}$$

where $\triangle V_{DC}$, V_{DCmax}, V_{DCmin} and V_{DCave} are the peak-peak, maximum, minimum and average values of the voltage V_{DC}. Because the capacitor C is not connected to any loads, the voltage across the C is allowed to have large voltage ripples. As long as $\triangle V_{DC} V_{DCave}$ is high enough, the capacitor C can be also very small.

Based on the above analysis, both the capacitor C_+ and the capacitor C are small and the

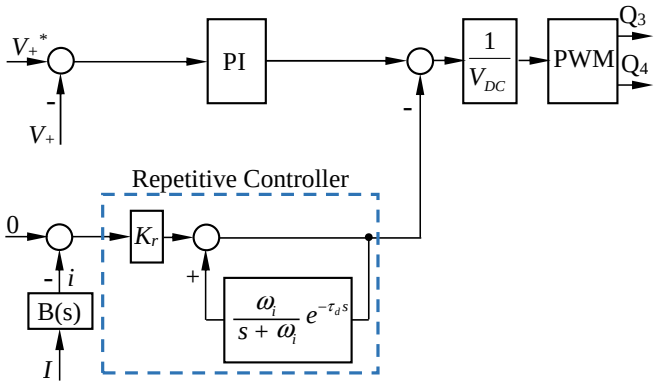


Figure 9.6: Controller for the neutral leg.

sum of them is still much smaller compared to the total capacitance required in conventional single-phase converters. The detailed comparison is introduced in the next section after the selection of components.

9.4.3 Control Design

In order to achieve the reduction of the inductor and capacitors, the two legs should be controlled properly. It is worth highlighting that the control design of the two legs is independent from each other. Advance control techniques can be applied to each leg according to their own objectives.

9.4.3.1 Control of the neutral leg

The neutral leg mainly aims to maintain the output voltage V_+. The DC component in the V_+ should be well regulated at its reference, while the second-order component in the V_+ is expected to be completely removed. In order to simultaneously achieve the two goals, a control strategy with parallel structure is designed as shown in Figure 9.6. A proportional-integral (PI) controller is adopted to maintain the DC component. At the same time, a parallel-connected current loop is designed in order to remove the second-order component in the V_+. According to the discussion before, the removal can be achieved through minimising second-order component in the current I. For this purpose, this second-order component, which is denoted as i, should be first extracted from the current I. Here, a band-pass-filter (BPF) is used, the transfer function of which is $B(s) = \frac{10000s}{(s+10)(s+10000)}$. The cut-off frequencies of the BPF are 1.59 Hz and 1591 Hz so the bandwidth of the BPF

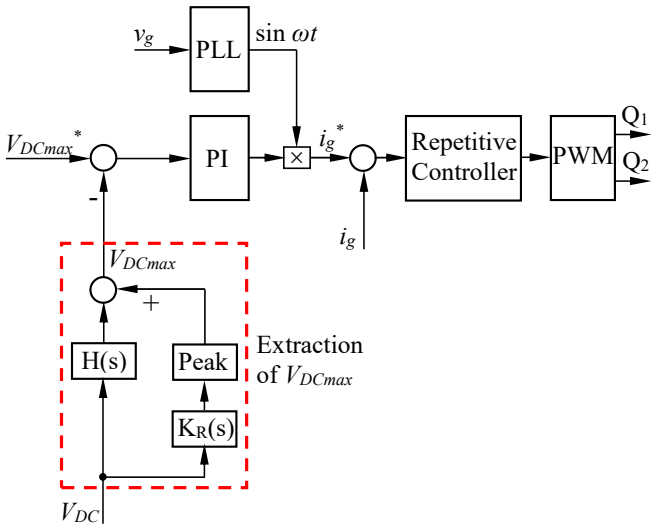


Figure 9.7: Controller for the conversion leg.

is about 1589 Hz.

Many current controllers can be applied to minimise the i. Here, a repetitive controller is used because of its strong capability to handle harmonics. As shown in Figure 9.6, the adopted repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}},$$

where τ_d is designed based on the analysis made in (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a) as $\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\text{s}$ with $\omega_i = 2550$, $\tau = 0.02\,\text{s}$.

The sum of the above two loops forms the controller for the neutral leg, as shown in Figure 9.6. Because the two loops are connected in parallel, it is straightforward to guarantee the stability of the controller as long as each of the loops is stable, which can be easily achieved.

9.4.3.2 Control of the conversion leg

The main objective of the conversion leg is to control the power exchange drawn from the grid by the converter. Many advanced well-known control strategies for grid-connected converters can be applied here. For example, if the robust droop controller (Zhong, 2013b) is applied to control the conversion leg, the proposed converter could take part in the regulation of the grid voltage to support the stability of the grid.

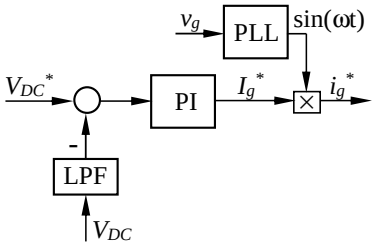


Figure 9.8: Generation of the i_g^* for the unity power factor.

Since the control design is not the main focus of this chapter, only a simple example is given here to demonstrate basic rules to design the controller for the conversion leg. In order to control the power exchanged with the grid, the most common way is to control the grid current. The repetitive controller used for the neutral leg is again adopted here as shown in Figure 9.7. The grid current reference i_g^* can be simply generated through a PI controller, the input of which is the error of the voltage V_{DC} (see Figure 9.8). How to design such PI controller is very matured and hence, is not discussed here. Note that the following low-pass-filter (LPF)

$$H(s) = \frac{1 - e^{-Ts}}{Ts}, \tag{9.12}$$

where T is the fundamental period of the grid voltage, is adopted to avoid introducing second-order harmonics to the grid current, as shown in Figure 9.8. The output of the PI controller is acted as the peak value of the i_g^*. The phase signal of the i_g^* is obtained using a phase-locked-loop (PLL). The product of the peak value and the phase signal can then form the i_g^*.

9.5 Selection of the Passive Components

In order to have high power density and reliability, it is desirable to minimise required passive components. There are four of them in the proposed converter, i.e. inductors L_g, L and capacitors C_+ and C. For the selection of the inductor L_g, strategies developed for conventional grid-connected single-phase converters can be directly used and hence, only criteria to select the other three components are discussed in the following parts.

9.5.1 Selection of the Inductor L

The inductor current I is controlled by complementarily switching on and off the switches Q_3 and Q_4. Accordingly, the I contains both DC and switching-frequency components. Assume that the peak-peak value of the switching component in the I is $\triangle i_s$, then the maximum value of the inductor current is

$$I_{max} = I_R + \frac{\triangle i_s}{2}. \tag{9.13}$$

The selected inductor L should have a maximum current higher than I_{max} to avoid saturation. Since the neutral leg is operated as a DC/DC converter, there is

$$\triangle i_s = \frac{V_+ d_3}{L f_s}$$

where f_s is the switching frequency and the level of the voltage V_+ is set according to the load requirement. In this case, the $\triangle i_s$ reaches to its maximum value when d_3 is maximised. That is

$$\triangle i_{smax} = \frac{V_+ d_{3max}}{L_N f_s} = \frac{V_+(1 - \frac{V_+}{V_{DCmax}})}{L_N f_s} \tag{9.14}$$

where d_{3max} is the maximum value of the d_3. The minimum inductance can be then given as

$$L_{min} = \frac{V_+(1 - \frac{V_+}{V_{DCmax}})}{\triangle i_{smax} f_s}, \tag{9.15}$$

which can be reduced if the switching frequency f_s is increased. The inductor L can be then well selected. To sum up, the maximum allowed current of the inductor should be higher than the I_{max} defined by (9.13) and the minimum inductance required should be larger than the L_{min} defined by (9.15).

9.5.2 Selection of the Capacitor C_+

The capacitor C_+ is now mainly used to filter out switching-frequency ripples because most of ripple energy is diverted to the capacitor C. The capacitor C_+ is only sized to limit switching-frequency ripple under a certain level. Since the capacitor C_+ is connected in series with the inductor L, they have more or less the same switching-frequency current.

As a result, the peak-peak switching voltage ripples across the capacitor C_+ can be given as (Mohan, 2003)

$$\triangle V_{+s} = \frac{\triangle i_{smax}}{8C_+ f_s}.$$

For a required level of the maximum switching ripples $\triangle V_{+sm}$, the minimum capacitance required is

$$\begin{aligned} C_{+min} &= \frac{\frac{V_+(1-\frac{V_+}{V_{DCmax}})}{L_{min} f_s}}{8 f_s \triangle V_{+sm}} \\ &= \frac{V_+(1-\frac{V_+}{V_{DCmax}})}{8 f_s^2 \triangle V_{+sm} L_{min}}. \end{aligned} \tag{9.16}$$

The switching frequency f_s is important when selecting the capacitor C_+. The higher the f_s is, the lower the C_+ can be.

9.5.3 Selection of the Capacitor C

In order to clearly demonstrate the minimum capacitance of the C, (9.11) can be re-formed as

$$C = \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)}. \tag{9.17}$$

The voltage V_{DCmax} mainly depends on the voltage rating of the switches. After leaving some margins, if the maximum allowed voltage of the switches is V_a, then

$$V_{DCmax} = V_a. \tag{9.18}$$

Since $V_{DC} = V_+ + V_-$ and the V_+ is set according to load requirement, there is

$$V_{DCmin} = V_+ + V_g. \tag{9.19}$$

because V_- should be greater than V_g to guarantee the successful boost operation of the converter.

Substitute (9.18) and (9.19) into (9.17) and then the minimum capacitance can be given

Table 9.3: Parameters of the proposed converter

Parameters	Values
Grid voltage (RMS)	110 V
Grid frequency f	50 Hz
Switching frequency f_s	19 kHz
Inductor L_g	2.2 mH
Inductor L	2.2 mH
DC output voltage V_+^*	200 V
Load R	220 Ω
Capacitor C_+	5 μF
Capacitor C	6 μF

as

$$\begin{aligned} C_{min} &= \frac{V_g I_g}{\omega(V_{DCmax}^2 - V_{DCmin}^2)} \\ &= \frac{V_g I_g}{\omega(V_a^2 - (V_+ + V_g)^2)}. \end{aligned} \tag{9.20}$$

It can be found that the higher the voltage V_a is, the smaller the capacitor C can be.

In order to select a right capacitor, it is also desirable to know the maximum second-order ripple current flowing through the capacitor. According to (9.10), the peak-peak value of the i_C is

$$\triangle i_C = \frac{V_g I_g}{V_{DC}}. \tag{9.21}$$

With both (9.20) and (9.21), the capacitor C can be well selected.

9.5.4 Design Example

A design example is given here to further demonstrate the selections. The parameters of the investigated system are summarised in Table 9.3. If $\triangle i_{smax} = 4$ A, then the minimum inductance is $L_{min} \approx 1.9$ mH, according to (9.15) when $V_a = 700$ V. In order to leave some margin, a 2.2 mH inductor is chosen. Based on (9.20), the minimum required capacitance is $C_{min} = \frac{V_g I_g}{\omega(V_a^2 - (V_+ + V_g)^2)} \approx 4.1$ μF if $I_g = 3$ A. If the maximum switching ripple voltage $\triangle V_{+sm} = 6$ V, then $C_{+min} = \frac{\triangle i_{max}}{8 \triangle V_{+sm} f_s} \approx 4.38$ μF. In the experiments presented later, a 5 μF and a 6 μF film capacitors are selected as C_+ and C, respectively.

9.6 Performance Evaluation

9.6.1 The Total Capacitance Required

In order to clearly demonstrate the system performance to reduce capacitance, the total capacitance required in the proposed converter is compared to that in conventional single-phase converters. The ratio of them can be given as

$$\begin{aligned} r_C &= \frac{C_{+min}+C_{min}}{\frac{V_g I_g}{2\omega \triangle V_+ V_+}} \\ &= (\frac{V_+(1-\frac{V_+}{V_a})}{8f_s^2 \triangle V_{+sm} L_{min}} + \frac{V_g I_g}{\omega(V_a^2-(V_++V_g)^2)}) \\ &\quad \times \frac{2\omega \triangle V_+ V_+}{V_g I_g} \\ &= \frac{\omega \triangle V_+ V_+^2 (1-\frac{V_+}{V_a})}{4V_g I_g f_s^2 \triangle V_{+sm} L_{min}} + \frac{2\triangle V_+ V_+}{V_a^2-(V_++V_g)^2}. \end{aligned} \tag{9.22}$$

For the design example given before, if $\triangle V_{DC} = 5$ V, then $r_C \approx 0.0114$ and the required capacitance is reduced by about 87 times in theory. If $\triangle V_{DC} = 2$ V, then $r_C \approx 0.0045$. In this case, the total capacitance required is reduced by about 220 times in theory. In practice, the capacitors are normally selected to be slightly larger than their minimum values to leave some margin for transient responses. As a result, the actual r_C may become slightly larger than its theoretical value.

The experimental results presented later show that the proposed converter can maintain the output voltage ripples at around 2 V with only a 5 μF and a 6 μF capacitors. In this case, the actual $r_C \approx 0.0058$, which means the capacitance is reduced by about 172 times compared to that in conventional single-phase converters. Film capacitors becomes cost-effective to be used for this level of capacitors.

9.6.2 Voltage Stress

Instead of depending on other system parameters, the voltage stress of the switches is always the voltage V_{DC}. It is desirable to maintain the voltage stress within a reasonable level so as to reduce switching losses and costs arising from switches. As mentioned before, both voltages V_+ and V_- needs to be higher than the peak grid voltage, which means the

sum of them, i.e. the V_{DC}, should be higher than doubled peak grid voltage. As long as $V_{DC} > 2V_g$ is satisfied, the proposed converter can work properly to draw grid current in any power factors, to maintain DC voltages and to reduce the total capacitance required. The first two objectives can be achieved without any compromise for all V_{DC} that are higher than $2V_g$. However, the system performance to reduce total capacitance is degraded along with the decrease of the V_{DC}. According to (9.22), the higher the V_{DC} is, the lower the total capacitance can be. In other words, the voltage stress should be high enough to guarantee the system performance to reduce capacitance. In practice, 1200 V switches are already enough for the proposed converter with universal AC voltage (88 V 264 V). For specific applications, the voltage stress can be tailored by selecting appropriate capacitors, according to (9.16) and (9.20).

9.6.3 Current Stress of Switches

Apart from the voltage stress, the average currents of switches are also important when selecting switches or diodes (Srinivasan and Oruganti, 1998). As a result, they are discussed here so that suitable switches and diodes for both legs can be well selected.

9.6.3.1 Switches and diodes of the conversion leg

There are two transistors and two diodes for the conversion leg. The average currents flowing through these transistors and diodes mainly depend on the level of the grid current i_g. According to the analysis of the four operation modes, the positive half cycle of the i_g flows through either the transistor of the Q_2 or the diode of the Q_1. On the other hand, the negative half cycle of the i_g flows through either the transistor of the Q_1 or the diode of the Q_2. In this case, the average currents flowing through the switches Q_1 and Q_2 and diodes

D_1 and D_2 are

$$\begin{aligned} I_{Q_1} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g(1-d_2)dt = I_R(\frac{2(V_{DC}-V_+)}{V_g\pi} - 0.5) \\ I_{Q_2} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g d_2 dt = I_R(\frac{2V_+}{V_g\pi} - 0.5) \\ I_{D_1} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g(1-d_2)dt = I_R(\frac{2(V_{DC}-V_+)}{V_g\pi} + 0.5) \\ I_{D_2} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g d_2 dt = I_R(\frac{2V_+}{V_g\pi} + 0.5). \end{aligned} \tag{9.23}$$

Obviously, the average current are very related to the voltages V_+ and V_{DC}.

9.6.3.2 Switches and diodes of the neutral leg

For the neutral leg, there are again two transistors and two diodes in total. The current flowing through the neutral leg mainly depends on the current i_N, which is equal to $-I_g \sin\omega t + \frac{V_g I_g}{2V_+}$. Unlike the current i_g, the periods of positive and negative cycles of the i_N depend on system parameters. In order to calculate the average currents, it is required to first know these periods. If let $i_N = 0$, then

$$-I_g \sin\omega t + \frac{V_g I_g}{2V_+} = 0.$$

Hence,

$$\sin\omega t = \frac{V_g}{2V_+}.$$

There are two solutions within $[0, \frac{2\pi}{\omega}]$, which are

$$\begin{aligned} t_1 &= \frac{1}{\omega}\arcsin\frac{V_g}{2V_+} \\ t_2 &= \frac{\pi}{\omega} - \frac{1}{\omega}\arcsin\frac{V_g}{2V_+}. \end{aligned}$$

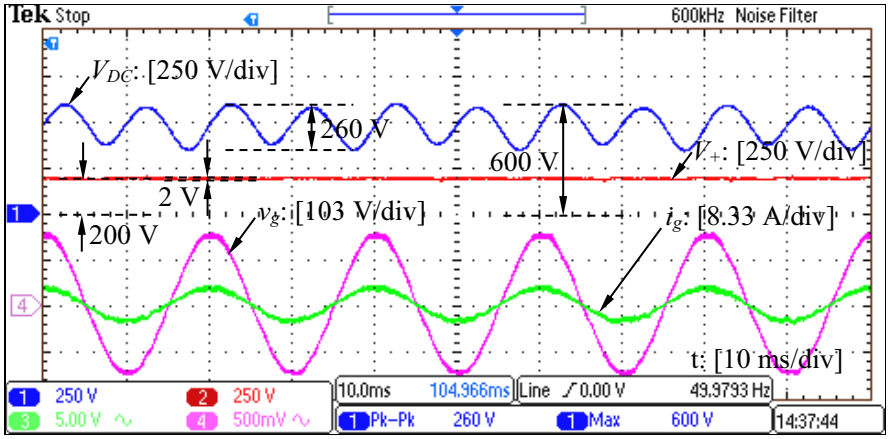
As a result, the average currents flowing through active switches Q_3 and Q_4 and diodes D_3 and D_4 can be calculated from

$$\begin{aligned} I_{Q_3} &= \frac{1}{2\pi}\int_{t_1}^{t_2} i_N d_3 dt \\ I_{Q_4} &= \frac{1}{2\pi}\int_{t_2}^{t_1+\frac{2\pi}{\omega}} i_N (1-d_3) dt \\ I_{D_3} &= \frac{1}{2\pi}\int_{t_2}^{t_1+\frac{2\pi}{\omega}} i_N d_3 dt \\ I_{D_4} &= \frac{1}{2\pi}\int_{t_1}^{t_2} i_N (1-d_3) dt. \end{aligned} \tag{9.24}$$

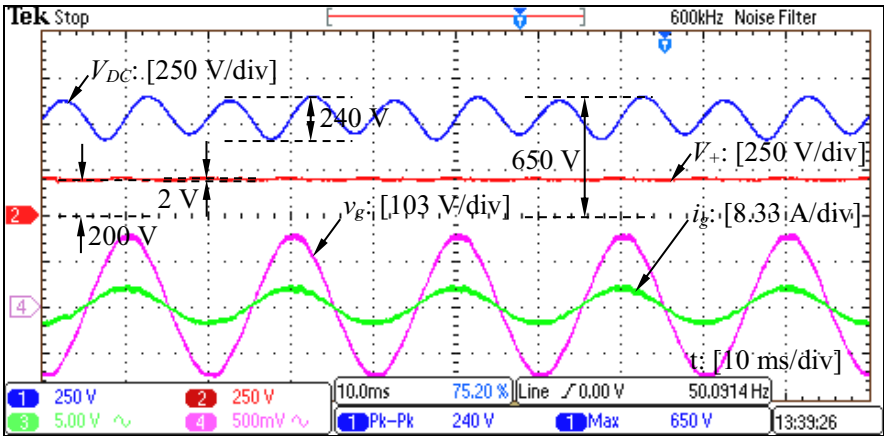
For certain applications with known system parameters, the average currents flowing through the switches and diodes of both legs can be easily obtained based on the above analysis.

9.7 Experimental Results

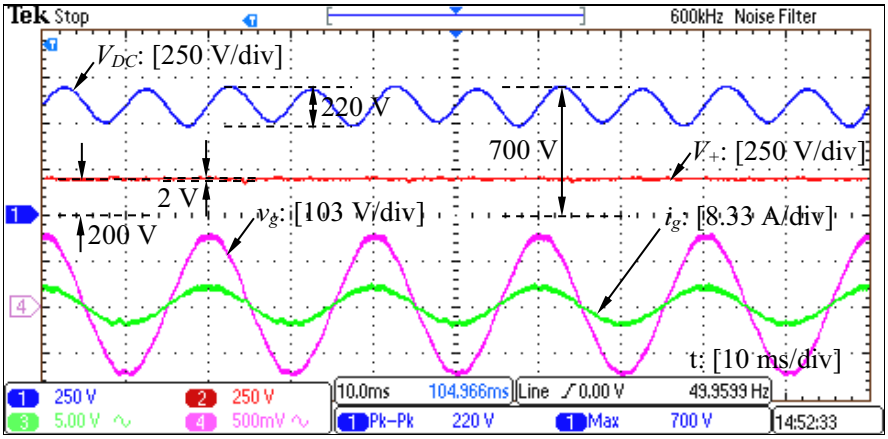
For verification of the system performance in practice, a prototype was assembled with parameters summarised in Table 9.3. One 5 μF and one 6 μF metallized polypropylene film capacitors are used as the capacitors C_+ and C in experiments, respectively. Bulky and vulnerable electrolytic capacitors are removed from the system. It is worth highlighting again that the total capacitance required in the proposed converter is considerably reduced by about 172 times in comparison with that in conventional single-phase converters. For the other system parameters, e.g. the inductor L_g and the switching frequency f_s, they are selected according to the available components in the laboratory and also the characteristics of the prototype. In the following parts of this section, measured experimental results during steady-state and transient responses are presented in Figure 9.9-9.16. Both cases with the unity and non-unity power factors are considered in order to well demonstrate the system capability to work with any power factors. In order for comparison, some waveforms of the θ-converter are also presented.


Tek Stop
600kHz Noise Filter
V_{DC}: [250 V/div]
260 V
600 V
V_+: [250 V/div]
2 V
200 V
v_g: [103 V/div]
i_g: [8.33 A/div]
t: [10 ms/div]
250 V
250 V
5.00 V
500mV
10.0ms
104.966ms
Line 0.00 V
49.3793 Hz
Pk-Pk 260 V
Max 600 V
14:37:44

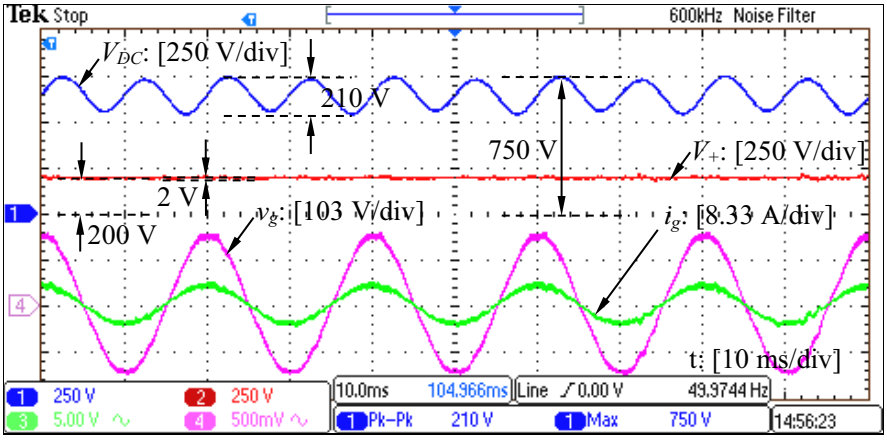
(a)


Tek Stop
600kHz Noise Filter
V_{DC}: [250 V/div]
240 V
650 V
V_+: [250 V/div]
2 V
200 V
v_g: [103 V/div]
i_g: [8.33 A/div]
t: [10 ms/div]
250 V
250 V
5.00 V
500mV
10.0ms
75.20 %
Line 0.00 V
50.0914 Hz
Pk-Pk 240 V
Max 650 V
13:39:26

(b)



(c)



(d)

Figure 9.9: Grid voltage v_g, grid current i_g and DC voltages V_+ and V_- under unity power factor with $V_+^* = 200$ V and (a) $V_{DCmax} = 600$ V; (a) $V_{DCmax} = 650$ V; (a) $V_{DCmax} = 700$ V; (a) $V_{DCmax} = 750$ V.

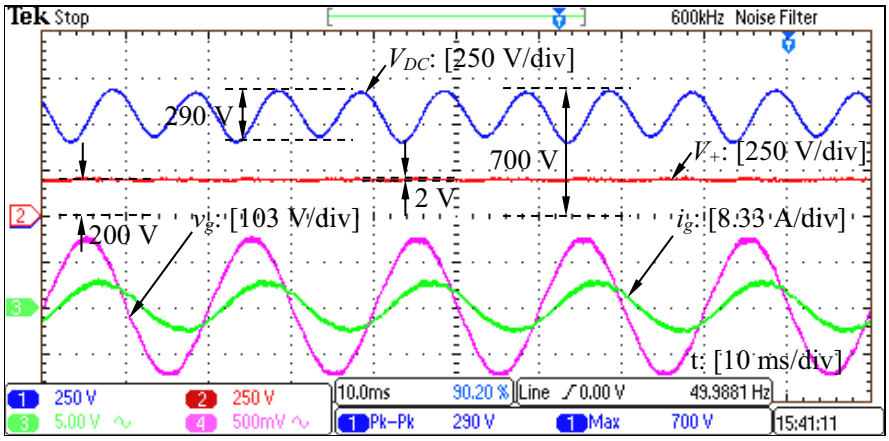


Figure 9.10: Grid voltage v_g, grid current i_g and DC voltages V_+ and V_{DC} under a non-unity power factor with $V_+^* = 200$ V and $V_{DCmax} = 700$ V.

9.7.1 Steady-state Performance

9.7.1.1 The grid current i_g and the DC voltages V_+ and V_{DC}

The system performance with unity power factor was recorded and the corresponding results are shown in Figure 9.9(a)-(d) for cases with $V_{DCmax}^* = 600$ V, $V_{DCmax}^* = 650$ V, $V_{DCmax}^* = 700$ V and $V_{DCmax}^* = 750$ V, respectively. For the AC side of the converter, the grid current i_g is always controlled well to be clean and to be in phase with the grid voltage over a wide range of V_{DCmax}. According to the recorded experimental data, the total harmonic distortion (THD) of the grid current is always lower than 4% , which is already very low since no special efforts are made for improving the quality of the grid current. For the DC side of the converter, the DC output voltage V_+ is with very low voltage ripples, which are only about 2 V, although the output capacitor is very small. Moreover, the DC-bus voltage V_{DC} is regulated well according to the set reference of its maximum value. Most of system ripple energy is now stored in the capacitor C instead of the output capacitor C_+.

In addition, the corresponding waveforms with a non-unity power factor are shown in Figure 9.10. The grid current is again very clean with low THD. The reference of the grid current is delayed by 2 ms compared with the grid voltage on purpose. Indeed, the time difference between the grid voltage and the current is 2 ms as shown in Figure 9.10. It is observed that the DC output voltage V_+ again has very low ripples while the DC-bus voltage V_{DC} does have large ripples as expected. As a result, the power factor does not affect the control of the DC voltages.

9.7.1.2 The voltage v_{AB}

In order to verify the analysis on the modulation strategy, the voltage v_{AB} is measured together with the grid current i_g during a few fundamental cycles and a few switching-frequency cycles as shown in Figure 9.11(a) and (b), respectively. According to Figure 9.11(a), it is obvious that the voltage v_{AB} rotated between zero and V_{DC} and rotated between zero and $-V_{DC}$ during positive and negative half cycles, respectively. This is well consistent with the analysis made in the Section 9.2.2. In addition, the waveforms shown in Figure 9.11(b) were captured during the positive half cycle of the grid current and hence, the voltage v_{AB} is either zero or V_{DC}. In general, the experimental waveform of the v_{AB} (see 9.11(b)) well matches with its theoretical waveform of the v_{AB} (see Figure 9.5), which verifies the effectiveness of the modulation strategy.

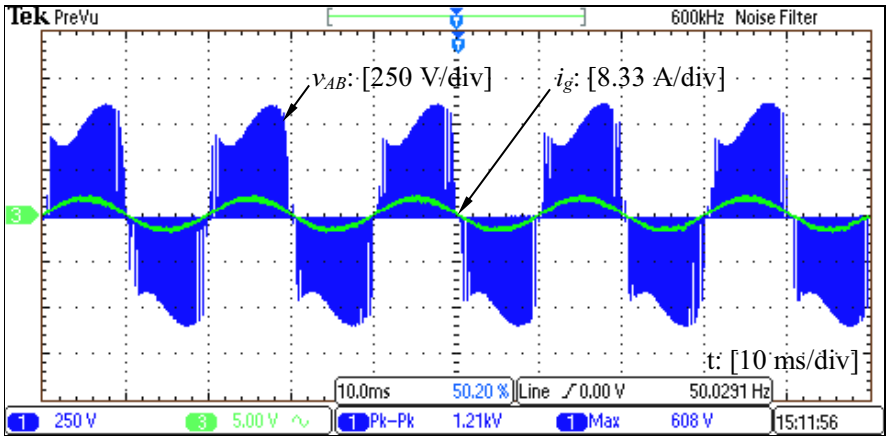
9.7.1.3 The CM current i_{CM} and the current I

A 0.47 μF capacitor is connected between the DC ground and the earth to mimic the parasitic capacitor. In this case, the current flowing through this capacitor is the CM current i_{CM}. The current i_{CM} was measured in experiments and the corresponding waveform is shown in Figure 9.12. It is clear that the i_{CM} is indeed zero, which is consistent to the theoretical analysis made before.

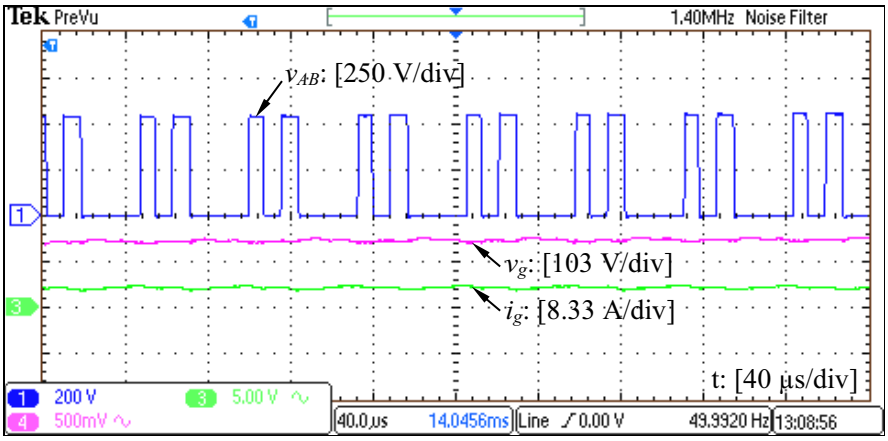
The spectrum of the current I was measured with and without the repetitive current controller for the neutral leg to demonstrate the performance of reducing second-order ripples in the current I. The corresponding results are shown in Figure 9.13(a) and Figure 9.13(b), respectively. Note that a 2.9 kHz filter is applied to clearly show low-frequency components in the I and the V_+. Obviously, the second-order (100 Hz) component in the current was diverted from the current I when the repetitive controller was activated, which leads to significantly-reduced ripples in the voltage V_+.

9.7.1.4 Comparison of the Inductor Current

As shown in Figure 9.14, the current flowing through the inductor L in the θ-converter was measured. It can be found that the maximum value of the inductor current is $i_{L\theta max} = 5.1$ A. As shown in Figure 9.13(b)), the maximum value of the current I is $i_{Lmax} = 1.42$ A. Note that the same system parameters used for the proposed converter are applied to the



(a)



(b)

Figure 9.11: The voltage v_{AB} and the grid current i_g when $V_+^* = 200$ V and $V_{DCmax}^* = 600$ V: (a) during a few fundamental-frequency cycles; (b) during a few switching-frequency cycles.

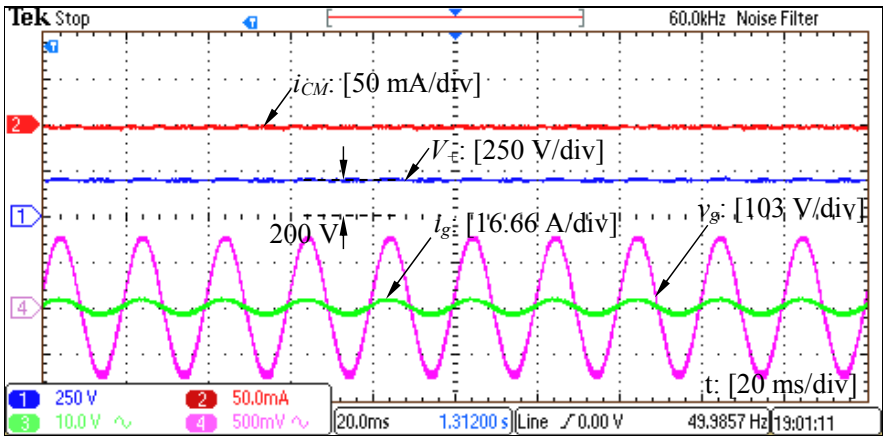
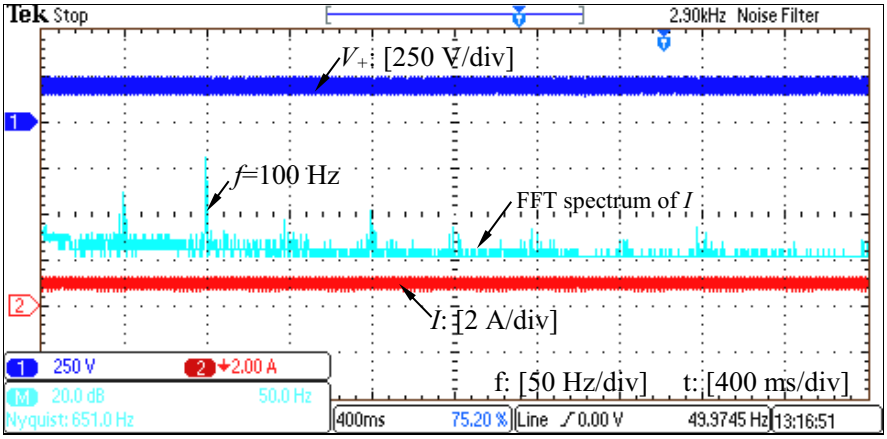
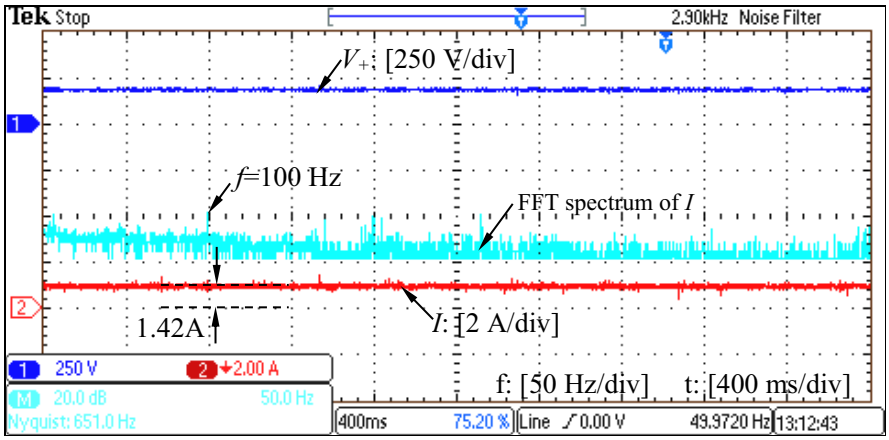


Figure 9.12: Measured CM current i_{CM}.



(a)



(b)

Figure 9.13: Comparison of (a) without and (b) with the repetitive current controller for the neutral leg.

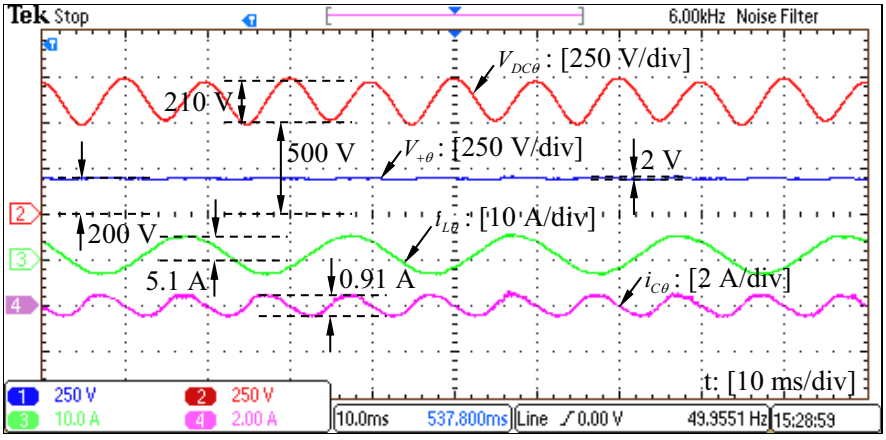


Figure 9.14: Measured current flowing through the inductor L in the θ-converter.

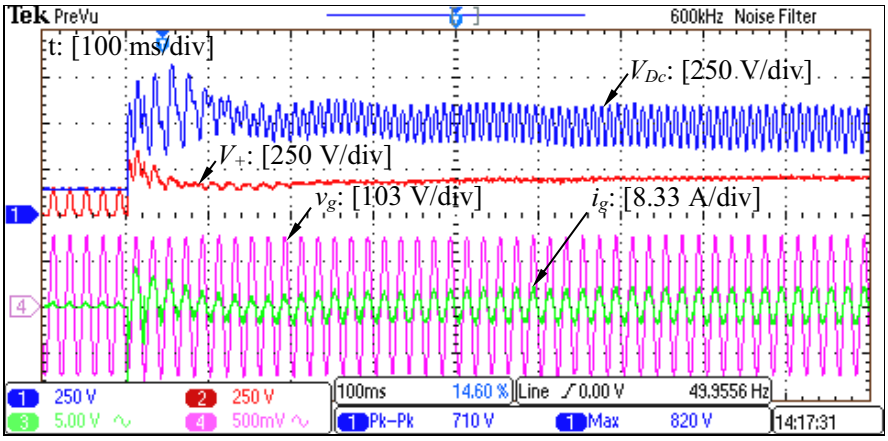


Figure 9.15: System start-up ($V_+^* = 200$ V and $V_{DCmax}^* = 600$ V).

θ-converter for a fair comparison. According to (9.4), the theoretical ratio between the two maximum values is $\frac{i_{L\theta max}}{i_{Lmax}} = 1 + \frac{2V_+}{V_g} = 1 + \frac{2\times 200}{110\sqrt{2}} \approx 3.57$. The ratio in experiments is $\frac{5.1}{1.4} \approx 3.59$, which well matches with its theoretical value.

9.7.2 Transient Response

9.7.2.1 System start-up

In order to demonstrate the transient response of the proposed converter, the waveforms when the system was started were captured as shown in Figure 9.15. Note that the system was initially run as a uncontrolled diode bridge and the grid current was seriously distorted. After the system was started, the output voltage V_+ was quickly maintained at its reference and the whole process only took about 300 ms, which is about 15 fundamental cycles.

9.7.2.2 Change of the output voltage reference

As shown in Figure 9.16, the reference of the output voltage V_+ was stepped from 200 V to 300 V. It took about 240 ms for the voltage V_+ to be settled at 300 V. The whole process is very smooth without spikes. Due to the increased system power, the ripples of the voltage V_{DC} becomes larger and the grid current becomes higher as expected. On the other hand, the ripples of the output voltage V_+ are always kept to be very low, which is important because the load is connected across the V_+.

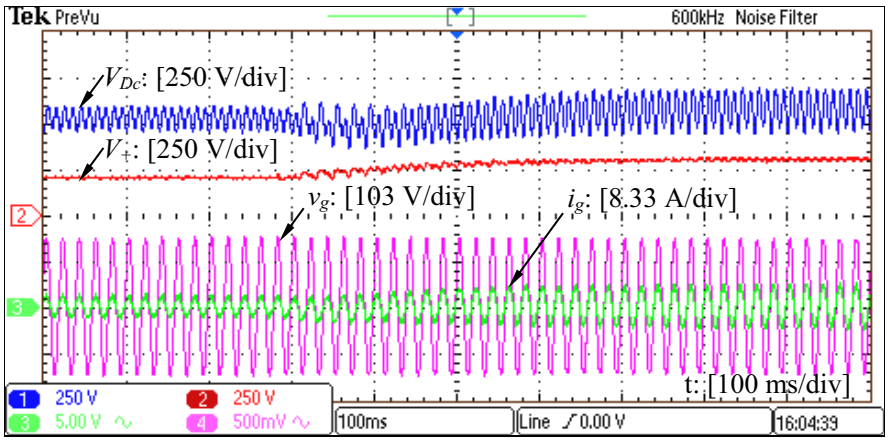


Figure 9.16: Transient response when the reference of the output voltage V_+ was stepped from 200 V to 300 V.

9.8 Summary

A single-phase four-switch converter has been proposed in this chapter. The proposed converter is developed on the basis of the θ-converter, which is proposed in Chapter 8. The location of the neutral inductor in the θ-converter is changed to form the proposed converter. Because of this change, the grid current does not flow through the neutral inductor any more. In this case, the neutral-inductor current is reduced by at least three times and the size of the inductor is accordingly reduced by at least about nine times. The other functions of the θ-converter, e.g. control of the grid current, elimination of the CM current and reduction of total capacitance, are well maintained. Only four active switches are used to achieve all the aforementioned functions. Selection criteria for the capacitors and the inductor have been discussed with the aim to minimise their usage and a design example has been given for demonstration. The presented experimental results have demonstrated that the proposed converter can indeed achieve the reduction of the inductor current while well maintaining the other functions of the θ-converter.

Chapter 10

DCM Ripple Eliminator to Reduce Low-frequency Voltage Ripples and Total Capacitance Required in DC Systems

In this chapter, a discontinuous-current-mode (DCM) ripple eliminator, which is a bi-directional buck-boost converter terminated with an auxiliary capacitor, is proposed to replace bulky capacitors in general DC systems while the aforementioned chapters are focused on some specific topologies. The low-frequency voltage ripples on the terminals (i.e., the DC bus) can be transferred to the auxiliary capacitor and the ripples on the auxiliary capacitor can vary in a wide range. Compared to the research in previous chapters, the proposed ripple eliminator is more effective for general DC systems, although several more power components are required.

For the proposed eliminator, the average voltage of the auxiliary capacitor can be controlled either lower or higher than the DC-bus voltage, which offers a wide operational range for the ripple eliminator and also the possibility of further reducing the auxiliary capacitance. Hence, the total capacitance required can be much smaller than the originally needed. After proposing a control strategy to transfer the voltage ripples to the auxiliary capacitor, three control strategies are proposed to regulate the auxiliary-capacitor voltage to maintain proper operation. Intensive experimental results are presented to demonstrate the performance.

10.1 Introduction

Voltage ripples and current ripples are main problems in DC microgrids or DC bus in renewable energy system and smart grid, which has drawn great attention from researchers in recent years(Zhong and Hornik, 2013b; Keyhani et al., 2010). Numerous strategies have been developed to counteract the ripples to obtain a smooth DC bus for backward-stage loads and forward-stage sources (Zhang et al., 2014; Babaei and Seyed Mahmoodieh, 2014; Ma et al., 2013). For backward-stage loads, stable DC input sources are desired to facilitate the control of converters in DC/DC or DC/AC applications; for forward-stage sources, an energy tank (e.g., bulky capacitors) is needed to absorb the ripple energy in the rectifier outputs and, moreover, active power factor correction (PFC) should be added as well to avoid the adverse impact of DC outputs on the AC grid. For AC systems and DC/AC applications, the elimination of voltage or current harmonics has also been extensively used to reduce the total harmonic distortion (THD) of AC voltages/currents (Keyhani et al., 2010; Zhong, 2013a; Sreeraj et al., 2014; Dai et al., 2008).

For systems powered from batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the lifetime of batteries and fuel cells (Li et al., 2011b; Baek et al., 2013). Generally, current ripples should be less than 10% of the rated current for batteries (Wen et al., 2012). For volume-critical and/or weight-critical applications, such as electrical vehicles (Wen et al., 2012) and aircraft power systems (Wang et al., 2011), the volume and weight of large capacitors could cause a serious problem. Another problem is the limited lifetime of large electrolytic capacitors so it is advantageous if small capacitors can be used to achieve low voltage ripples. Actually, electrolytic capacitors are also well known as sources of reliability issues. Therefore, active control strategies to reduce voltage and current ripples have received a lot of attention in recent years, aiming to improve the reliability of the whole system and reduce system volume, weight and cost (Li et al., 2006; Du et al., 2012; Lenwari et al., 2006; Chen and Hui, 2012; Dai et al., 2005).

In principle, voltage ripples on a DC bus mainly stem from the ripple current flowing through the DC bus, which leads to the so-called ripple power. Accordingly, if the ripple power is counteracted by an energy storage system or a buffer then there are no large voltage ripples in the system (Picard). From this viewpoint, three solutions with different circuit topologies (boost/buck, flyback/buck and multimode buck/boost) were proposed

and compared for a high-voltage energy storage system to minimize the size of the DC-bus capacitor in (Picard). Moreover, the flyback/buck topology, with three power switches, one inductor and one capacitor, was selected as the best choice due to its excellent trade-off between the small size and the acceptable complexity and costs.

Recently, a buck/boost bi-directional converter terminated with a capacitor was adopted to achieve the reduction of the DC-bus capacitor and to implement a high power density single-phase PWM rectifier in (Wang et al., 2011; Chao et al., 2009; Li et al., 2011a). The system is operated in the buck mode to absorb energy from the DC bus and in the boost mode to inject energy back to the DC bus. The inductor current is regulated with average-current control in the discontinuous current mode (DCM) and the auxiliary capacitor voltage is less than the DC-bus voltage. Through the energy absorbing and injecting processes, the DC-bus ripple power/energy can be diverted actively to the capacitor. The performance of the system is very good and it is particularly suitable for aircraft applications where no voltage higher than the DC-bus voltage is allowed.

A voltage bus conditioner, with two power switches, one inductor and one capacitor, was proposed in (Kim et al., 2009; Chang et al., 2011; Mollov, 2011) to mitigate the bus voltage transients for distributed power systems with large impulsive backward-stage loads and simulation results were presented to validate the strategy. There, detailed analysis was carried out with an averaged small-signal model, based on which the corresponding control law was developed. The main control principle was to maintain the current through the DC-bus capacitor to be zero, which can result in a ripple-free DC-bus voltage. Two control strategies, a PI controller and a sliding mode controller, were designed and compared to mitigate DC-bus voltage transients caused by multiple parallel loads. In this chapter, the same topology, called a ripple eliminator, is adopted to absorb/inject the ripple energy introduced by the input source to reduce the DC-bus voltage ripples. It is in principle a buck-boost converter terminated with an auxiliary capacitor, of which the voltage can be controlled to be lower or higher than the DC-bus voltage. This widens the operational range, e.g. to meet the requirement of heavily-loaded applications, and offers the possibility of further reducing the auxiliary capacitance. As a result, the total capacitance needed is reduced. A controller is proposed to divert the ripple power on the DC bus to the auxiliary capacitor after analysing the operational principle of the circuit. In order for the energy

transfer to be achieved properly, the average voltage of the auxiliary capacitor needs to be regulated at a certain level. This can be achieved via controlling the average voltage, the voltage ripple ratio or the minimum voltage of the auxiliary capacitor, at a given value. All these three control strategies are developed and verified with experimental results. With comparison to (Kim et al., 2009; Chang et al., 2011; Mollov, 2011), the main contributions of this chapter include 1) carrying out detailed analysis of the operational modes, which has led to the explicit calculation of PWM duty cycles for the switches and simplified current controller; 2) providing guidelines for selecting the major components; 3) proposing three methods to regulate the auxiliary-capacitor voltage with unique characteristics and advantages, which widens the ripple eliminator for different applications; 4) carrying out extensive experiments to demonstrate the excellent performance of the ripple eliminator and to verify the relationship between the ripple voltage and average voltage on the auxiliary capacitor as well as the proposed control strategies. It is shown that the three methods are good for different applications but the most appropriate method is to regulate the minimum voltage of the auxiliary capacitor. Note that the cost analysis is not carried out and will be reported in the future after proper prototypes are built. Nevertheless, according to (Wang et al., 2011), the efficiency drop after replacing electrolytic capacitors with active controlled ripple eliminators is not significant but the power density could be significantly increased. The most important thing is that this reduces the usage of electrolytic capacitors and enhances system reliability.

The rest of the chapter is organised as follows. Various aspects of the ripple eliminator, including the topology, its operation, control and design, are detailed in Section 10.2. Then, extensive experimental results are presented in Section 10.3 with the summary made in Section 10.4.

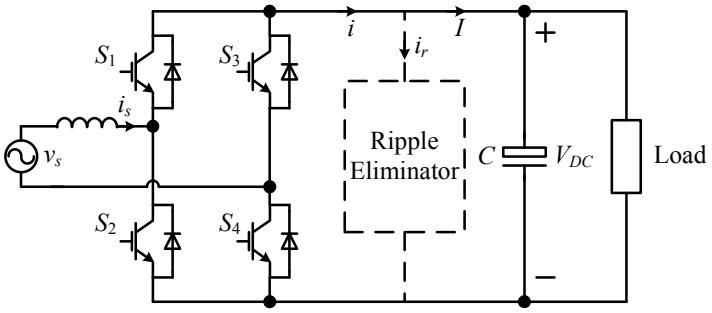


Fig. 10.1: Sketch view of a single-phase PWM rectifier.

10.2 The Ripple Eliminator under Study

There are different settings to investigate the ripples in DC microgrids or DC systems. In this chapter, a typical single-phase PWM-controlled rectifier, as shown in Fig. 10.1, is taken as an example to facilitate the presentation. Because the input current of such a rectifier is controlled to be sinusoidal and often in phase with the input voltage, the instantaneous power taken at the AC side is pulsating but the power consumed by the load at the DC side is often a constant (ideally). The difference of the two is called the ripple power. If there are capacitors on the DC bus, then the ripple power should be taken by the capacitors, which leads to voltage ripples on the DC bus because the capacitance cannot be infinite. In order to analyse the voltage ripples of the DC bus, the net change of the energy stored in the DC-bus capacitor over a charging period (i.e. a quarter cycle of the supply), called the ripple energy, can be calculated as demonstrated in (Wang et al., 2011) as

$$E_r = \frac{\sqrt{P_o^2 + \left[\frac{\omega L P_o^2}{V_s^2 \cos^2\phi} - P_o\left(\frac{\sin\phi}{\cos\phi}\right)\right]^2}}{\omega}, \tag{10.1}$$

where ϕ is the phase difference between the voltage and the current of the AC supply, P_o is output power of the rectifier, E_r is Ripple energy, L is the input inductor at the AC side and V_s and I_s are peak values of the grid voltage and grid current, respectively. When the input current is in phase with the voltage, $\phi = 0$. In this case, the ripple energy is

$$E_r = \frac{I_s}{\omega}\sqrt{V_s^2 + (\omega L I_s)^2}. \tag{10.2}$$

When E_r is high, the DC-bus capacitor needed can be very large in order to maintain the ripples below a certain level.

In recent years, there have been a lot of interests in diverting the ripple power away from the DC bus into another energy storage device or a buffer, as mentioned before. Because the voltage of the buffer is allowed to vary in a much wider range without affecting the proper operation of the system, the capacitance needed can be considerably reduced. Such a strategy, called a ripple eliminator, is studied in this chapter.

Although the PWM-controlled rectifier is taken as an example in this chapter to facilitate the presentation, the strategy studied can be applied to other DC systems, e.g. inverters

powered by fuel cells or batteries and other DC systems that are interfaced with an AC source/sink, without changing the topology. The only change that may be needed is the way of detecting the ripple current flowing through the DC bus.

10.2.1 Topology

The proposed ripple eliminator to divert the ripple power away from the DC bus into another energy storage device is shown in Fig. 10.2. It is in principle a buck-boost converter terminated with an auxiliary capacitor C_a, which is operated as the energy-storage device or the buffer for the ripple power. The inductor L_a is operated as an energy-transferring device between the DC bus and the auxiliary capacitor.

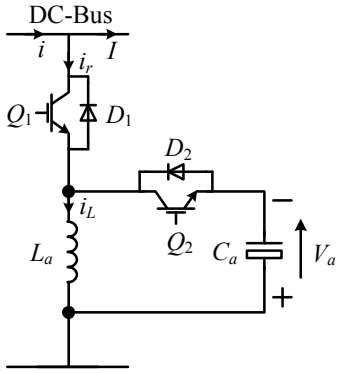


Fig. 10.2: The ripple eliminator under study.

In order to eliminate the voltage ripples on the DC bus, all the ripple power should be diverted to the auxiliary capacitor C_a. In other words, the current I needs to be maintained purely constant and the ripple current i_r in the DC-bus current i should flow or be diverted through the ripple eliminator. Because i_r is an AC current, diverting i_r through the ripple eliminator involves two operating modes: charging and discharging the auxiliary capacitor C_a. The inductor current should be controlled in the average-current mode so that the current i_r is at the right value. The ripple eliminator is operated in the Discontinuous Conduction Mode (DCM) in this chapter because the duty cycle of PWM for power switches in this case can be calculated directly as demonstrated below and there is no need to measure the inductor current for control purposes, which saves one current sensor and simplifies the controller design.

Since this ripple eliminator is a buck-boost converter in both the charging mode and the

discharging mode, the voltage across C_a can be lower or higher than the DC-bus voltage. When it is controlled to be higher than the DC-bus voltage, it offers the possibility of further reducing the capacitance C_a because the energy stored in the capacitor is $\frac{1}{2}C_aV_{a0}^2$ and the ripple energy corresponding to the voltage ripple ΔV_a is

$$\begin{aligned}&\frac{1}{2}C_a(V_{a0}+\frac{1}{2}\Delta V_a)^2-\frac{1}{2}C_a(V_{a0}-\frac{1}{2}\Delta V_a)^2\\&=C_aV_{a0}\Delta V_a\end{aligned} \tag{10.3}$$

where V_a, V_{a0} and ΔV_a are the voltage, its DC component and its peak-peak ripple across the capacitor C_a, respectively. For a given required ripple energy, e.g. E_r, the larger the V_{a0} the smaller the C_a; the larger the voltage ripple ΔV_a the smaller the C_a. When V_{a0} is fixed, then C_a is in inverse proportion to ΔV_a. Hence, this ripple eliminator allows the auxiliary capacitance C_a or the voltage ripple ΔV_a on C_a to be reduced considerably via increasing the voltage V_{a0}. Once the ripple energy is diverted to C_a, the DC-bus capacitor is only needed to deal with the ripples caused by the high-frequency switching. As a result, both C and C_a can be made small so that it is possible to use film capacitors instead of electrolytic capacitors, which significantly enhances the reliability of the system (Chen and Hui, 2012). Moreover, because of the high switching frequency for Q_1 and Q_2, the inductor L_a can be made very small as well. Hence, the ripple eliminator can be made very small and of high power density. Note that the ripple eliminator can be sealed in one package so that the high-voltage part of the circuit is not accessible.

Without looking closely, the topology seems very similar to the one studied in (Wang et al., 2011). However, it is different because 1) the topology studied in (Wang et al., 2011) is operated as a buck converter in the charging mode and as a boost converter in the discharging mode; 2) the voltage across the auxiliary capacitor in (Wang et al., 2011) has to be lower than the DC-bus voltage and it is impossible to further reduce the auxiliary capacitor C_a by increasing the voltage level of the auxiliary capacitor. The strategy proposed in this chapter is able to halve the DC-bus voltage ripples with the same hardware, as demonstrated by the experimental results later.

10.2.2 Operation in the Charging Mode

When i_r is positive, the ripple eliminator works in the charging mode and transfers the ripple energy from the DC bus to C_a via L_a. In this mode, Q_2 is always OFF and Q_1 is driven by a PWM signal with the diode D_2 freewheeling the inductor current to the capacitor.

When Q_1 is ON with a duty cycle of $D_c = \frac{T_1}{T_r}$, the inductor current increases to withstand the DC-bus voltage V_{DC} and its rising rate is

$$K_{c1} = \frac{V_{DC}}{L_a} \tag{10.4}$$

where D_c is the duty cycle in the charging mode, T_1 and T_2 are rising period and falling period of the inductor current in a switching cycle, respectively.

When Q_1 is OFF, the inductor current decreases to withstand the auxiliary-capacitor voltage and the falling rate is

$$K_{c2} = -\frac{V_a}{L_a}. \tag{10.5}$$

The typical current waveforms when $V_a < V_{DC}$ and $V_a > V_{DC}$ are shown in Fig. 10.3(a) and (b), where V_{DC} is the DC-bus voltage. They are in the same shape but with different falling rates. The inductor absorbs energy from the DC bus when being energized during the rising-period T_1 of the inductor current so the ripple current is diverted from the DC bus only during T_1 (the hatched area in Fig. 10.3(a) and (b)). Its average over a switching cycle should be equal to the reference ripple current i_r^*. Hence, the duty cycle D_c for Q_1 can then be obtained as

$$D_c = \sqrt{\frac{2i_r^* f_r L_a}{V_{DC}}}, \tag{10.6}$$

according to V_{DC} and the reference ripple current i_r^* (the positive part). Moreover, the current falling time can also be found as

$$\begin{aligned} T_2 &= \frac{D_c T_r K_{c1}}{-K_{c2}} \\ &= \frac{D_c V_{DC}}{f_r V_a}. \end{aligned} \tag{10.7}$$

10.2.3 Operation in the Discharging Mode

When i_r is negative, the ripple eliminator works in the discharging mode and transfers the stored ripple energy from C_a to the DC bus via L_a. In this mode, Q_1 is always OFF and Q_2 is driven by a PWM signal to discharge the auxiliary capacitor. The inductor freewheeling current flows through the diode D_1 when Q_2 is OFF.

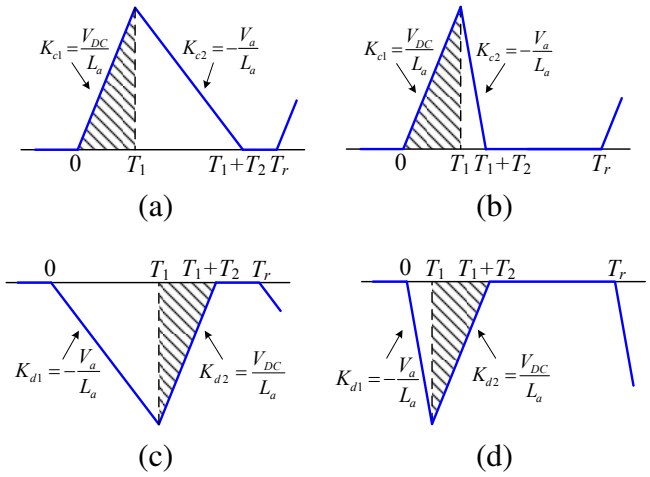


Fig. 10.3: Typical current waveform of the inductor: (a) $V_a < V_{DC}$ in the charging mode. (b) $V_a > V_{DC}$ in the charging mode. (c) $V_a < V_{DC}$ in the discharging mode. (d) $V_a > V_{DC}$ in the discharging mode.

When Q_2 is ON with a duty cycle of $D_d = \frac{T_1}{T_r}$, the inductor current increases to withstand the auxiliary-capacitor voltage and its rising rate is

$$K_{d1} = -\frac{V_a}{L_a}. \tag{10.8}$$

When Q_2 is OFF, the inductor current decreases to withstand the DC-bus voltage and the current is diverted to the DC bus to compensate the ripple current. The falling rate of the inductor current is

$$K_{d2} = \frac{V_{DC}}{L_a}. \tag{10.9}$$

The typical current waveforms when $V_a < V_{DC}$ and $V_a > V_{DC}$ are shown in Fig. 10.3(c) and (d), with differences in the rising rates. The reference ripple current i_r^* should be equal to the average of the current diverted to the DC bus during the falling-period T_2 of the inductor

current (the hatched area in Fig. 10.3(c) and (d)) over a switching cycle. Hence,

$$-i_r^* T_r = \frac{1}{2} K_{d2} T_2^2. \tag{10.10}$$

Since the peak inductor current satisfies

$$-K_{d1} T_1 = K_{d2} T_2, \tag{10.11}$$

therefore, the duty cycle D_d is

$$D_d = \frac{\sqrt{-2 i_r^* f_r L_a V_{DC}}}{V_a}, \tag{10.12}$$

which can be obtained according to V_{DC}, V_a and the reference ripple current i_r^* (the negative part). Note that D_d is affected by V_a but D_c is not.

10.2.4 Design and Parameter Selection

In order to ensure that the inductor is operated in the DCM, the inductor should release all its stored energy in each switching cycle. Hence,

$$T_1 + T_2 \leq T_r. \tag{10.13}$$

That is

$$D_c T_r (1 + \frac{V_{DC}}{V_a}) \leq T_r \tag{10.14}$$

for the charging mode and

$$D_d T_r (1 + \frac{V_a}{V_{DC}}) \leq T_r \tag{10.15}$$

for the discharging mode. These should be satisfied when the ripple current reaches the rated maximum ripple current I_{rm}. These two conditions actually become the same as

$$\frac{2 I_{rm} f_r L_a}{V_{DC}} (1 + \frac{V_{DC}}{V_a})^2 \leq 1, \tag{10.16}$$

which is equivalent to

$$\frac{L_a}{V_{DC}} \leq \frac{V_a^2}{2 I_{rm} f_r (V_a + V_{DC})^2}. \tag{10.17}$$

Moreover, the inductor peak current should be maintained below the maximum peak current I_{Lp} of the inductor. That is,

$$D_c T_r \frac{V_{DC}}{L_a} \leq I_{Lp} \tag{10.18}$$

for the charging mode and

$$D_d T_r \frac{V_a}{L_a} \leq I_{Lp} \tag{10.19}$$

for the discharging mode. These should be satisfied when the ripple current reaches the rated maximum ripple current I_{rm} and the inductor current reaches the maximum peak current I_{Lp}. In this case, these two conditions become the same as

$$\frac{2I_{rm}}{f_r I_{Lp}^2} \leq \frac{L_a}{V_{DC}}. \tag{10.20}$$

Combining it with (10.17), there is

$$\frac{2I_{rm}}{f_r I_{Lp}^2} \leq \frac{L_a}{V_{DC}} \leq \frac{V_a^2}{2I_{rm} f_r \left(V_a + V_{DC}\right)^2}. \tag{10.21}$$

This can be re-written as

$$2(\frac{I_{rm}}{I_{Lp}})^2 \leq \frac{I_{rm} f_r L_a}{V_{DC}} \leq \frac{V_a^2}{2\left(V_a + V_{DC}\right)^2}, \tag{10.22}$$

where $I_{rm} f_r L_a$ reflects the voltage dropped on L_a caused by I_{rm} at the switching frequency f_r. This relationship is shown in Fig. 10.4 and can be adopted to determine L_a. It is clear that L_a can be reduced via increasing f_r. Moreover, when I_{rm} is increased, L_a can be reduced. These are all consistent with normal principles. The selection range for L_a increases when the voltage of the auxiliary capacitor is increased and/or the ratio $\frac{I_{Lp}}{I_{rm}}$ is increased. The extreme case is

$$0 < I_{rm} f_r L_a < \frac{1}{2} V_{DC}, \tag{10.23}$$

which can be used to approximately choose L_a after determining V_{DC}, I_{rm} and f_r.

If the condition (10.21) holds, then

$$\frac{2I_{rm}}{f_r I_{Lp}^2} \leq \frac{V_a^2}{2I_{rm} f_r \left(V_a + V_{DC}\right)^2}. \tag{10.24}$$

That is,

$$\frac{V_a}{V_{DC}} \geq \frac{2I_{rm}}{I_{Lp} - 2I_{rm}}. \tag{10.25}$$

This relationship is shown in Fig. 10.5. It describes the required minimum voltage of the auxiliary capacitor to guarantee the normal DCM operation for a given ratio of the inductor peak current to the maximum ripple current I_{rm}. It can be seen that, for a given ripple energy value, increasing the voltage of the auxiliary capacitor does not only further reduces the auxiliary capacitor but also helps reduce the current rating of the inductor. Note that $V_a > V_{DC}$ if $I_{Lp} < 4I_{rm}$. In other words, if I_{Lp} is chosen smaller than $4I_{rm}$ then the auxiliary-capacitor voltage should be higher than V_{DC}. It is worth noting that although the auxiliary-capacitor voltage used in (10.25) is V_a instead of V_{a0}, it is quite accurate to treat V_a as V_{a0} because the maximum ripple current appears around the point when the auxiliary-capacitor voltage crosses the average value V_{a0}, assuming that the losses in the ripple eliminator is small.

10.2.5 Control of the Ripple Current

For single-phase applications, e.g. the one shown in Fig. 10.1, the ripple power on the DC bus is dominated by a second-order harmonic component. In order to minimize the ripple energy in the DC bus, the ripple eliminator should draw all the ripple current i_r in i. After measuring the DC-bus current before the connecting point of the DC bus and the ripple eliminator, the second-order harmonic component can be obtained via passing the current i through the resonant filter (Zhong et al., 2011; Lenwari et al., 2006)

$$K_R(s) = \frac{2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}, \tag{10.26}$$

where $h = 2$ and f and ω are frequency and angular frequency of the AC supply, respectively. In order to cope with frequency variations, ξ can be chosen as $0.01 \sim 0.02$. Once the ripple current is obtained, the duty cycles in the charging mode and in the discharging

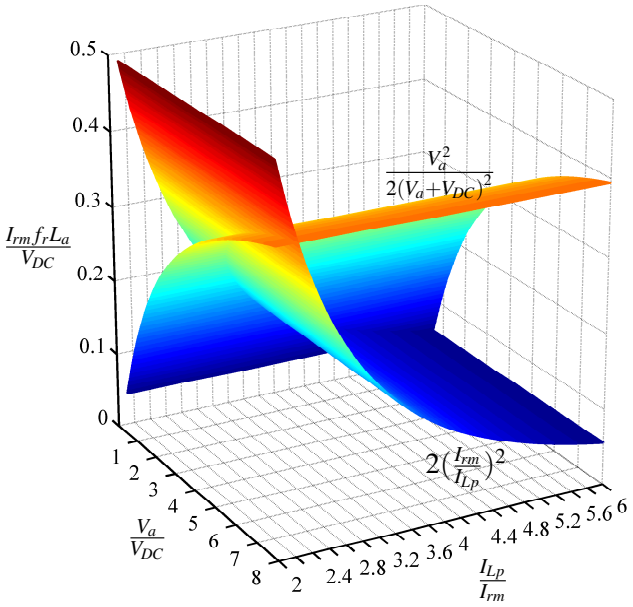


Fig. 10.4: Selection of $\frac{I_{rm}f_rL_a}{V_{DC}}$: between the two surfaces $\frac{V_a^2}{2(V_a+V_{DC})^2}$ and $2(\frac{I_{rm}}{I_{Lp}})^2$.

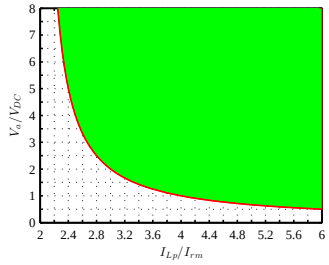


Fig. 10.5: DCM operation region characterized by $\frac{V_a}{V_{DC}}$ and $\frac{I_{Lp}}{I_{rm}}$.

mode can be calculated from (10.6) and (10.12) to generate the gate signals g_{Q1} and g_{Q2}, respectively. The resulting control strategy is shown in Fig. 10.6, with the injection of an additional DC bias current I_a^* that is needed to establish and maintain a stable auxiliary-capacitor voltage, which is to be discussed in the next subsection. If the ripple current is not dominated by a second-order harmonic component, then $K_R(s)$ needs to be changed accordingly.

10.2.6 Control of the Auxiliary-capacitor Voltage

Since the voltage ripples on the DC bus are transferred to the auxiliary capacitor, there are significant ripples in the voltage V_a. Its DC component V_{a0} can be obtained after passing

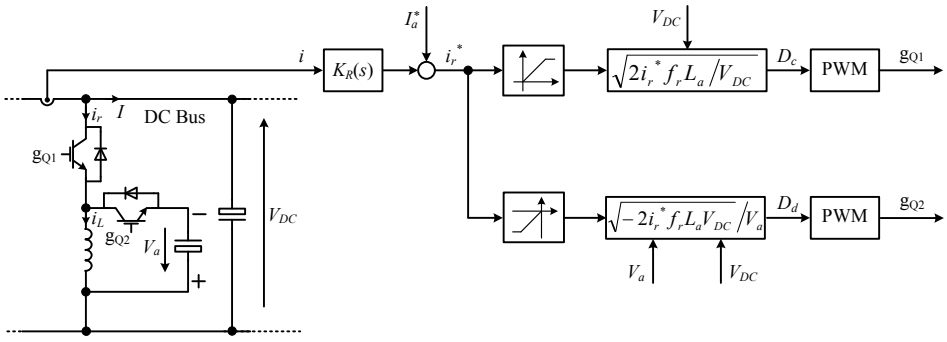


Fig. 10.6: Control strategy for the ripple eliminator.

the voltage V_a through the hold filter

$$H(s) = \frac{1 - e^{-Ts/2}}{Ts/2}, \tag{10.27}$$

because the fundamental frequency of the ripple is twice of the AC supply frequency $T = \frac{1}{f}$. In order to maintain the auxiliary-capacitor voltage, three control methods are proposed in this chapter to meet different requirements.

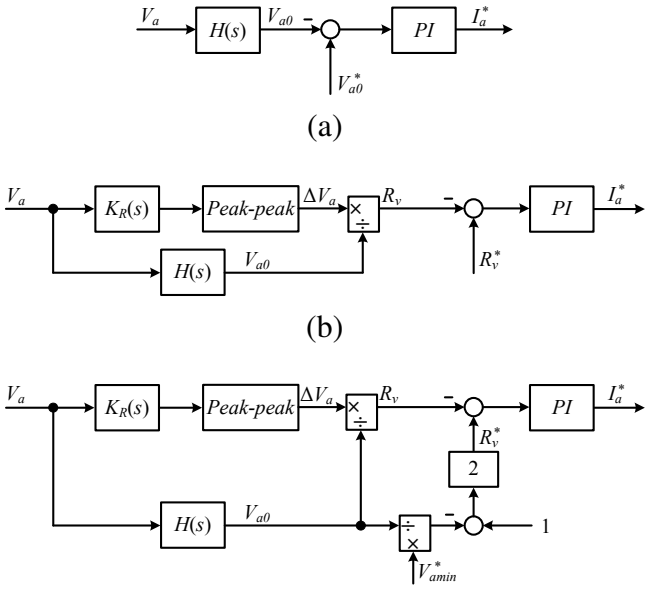


Fig. 10.7: Regulation of the auxiliary-capacitor voltage to generate I_a^*. (a) Method A: To maintain a given average voltage V_{a0}^*. (b) Method B: to maintain a given ripple ratio R_v^*. (c) Method C: To maintain a given minimum voltage V_{amin}^*.

10.2.6.1 Method A: To maintain V_{a0} at a given value V_{a0}^*

This is the most straightforward requirement and can be easily achieved with a PI controller, after comparing the DC component V_{a0} with the given value V_{a0}^*. As a result, the PI controller generates the required DC bias current I_a^* to charge the auxiliary capacitor. The resulting controller is shown in Fig. 10.7(a). The input of the PI controller is the difference of the auxiliary-capacitor voltage from the given value V_{a0}^* and the output is the additional current I_a^* to be injected to the ripple eliminator, i.e. the DC offset of the reference ripple current i_r^*. The tuning of the PI controller can be started with a proportional gain K_P to achieve the expected time constant T_c of the loop from I_a^* to V_{a0}^*, which is approximately

$$T_c = \frac{C_a}{K_p}.$$

The integral gain can then be chosen initially to be the same as K_p. If needed, some fine tuning through trial-and-error can be carried out. In practice, a small T_c may lead to a large charging current that might trigger the current protection.

If the ripple energy increases, then the voltage ripple ΔV_a on the auxiliary capacitor would increase as well according to (10.3). This would cause the minimum voltage V_{amin} to decrease accordingly. When V_{amin} decreases below a certain level, the ripple energy could not be compensated sufficiently. Therefore, the given average voltage V_{a0}^* should be chosen high enough to cope with the variation of ripple energy on the DC bus. An indicative value for V_{amin} can be obtained from (10.25) as $\frac{2I_{rm}}{I_{Lp}-2I_{rm}}V_{DC}$; see the experimental verification in Subsection 10.3.2. This is often not an issue because the idea of ripple eliminators is to increase V_{a0}^* as much as practically possible.

10.2.6.2 Method B: To maintain a given ripple ratio R_v^* for V_a

As illustrated in (Zhao et al., 2013; Lee et al., 2007; Venet et al., 1999), increased voltage ripples lead to increased capacitor currents, which accelerates the ageing process of the capacitor. Hence, for applications with high voltage ripples, it is better to maintain the voltage ripple ratio within a certain range so that the capacitor current is limited. This is beneficial to extend the life cycle of the auxiliary capacitor.

The ripple ratio R_v of V_a is the ratio of the ripple amplitude ΔV_a (peak-peak) to the

average voltage V_{a0}, i.e.,

$$R_v = \frac{\Delta V_a}{V_{a0}} \times 100\%. \tag{10.28}$$

In order to improve the performance under different loading conditions, the ripple ratio of V_a can be maintained so that the average voltage V_{a0} can be automatically regulated when the load changes. This can be achieved with the strategy shown in Fig. 10.7(b), where the resonant filter (10.26) is adopted to pick up the voltage ripples in V_a so that the peak-peak value can be obtained as ΔV_a. Because of the scaling factor from the voltage V_a to the ripple ratio R_v^*, the parameters of the PI controller can be obtained by scaling the parameters of the PI controller used in Method A by $\frac{V_{a0}}{R_v^*}$ as the starting point of the tuning process. Since the order of the system is low, the range of the parameters is very wide, which makes it very easy to tune the parameters.

Substituting (10.28) into (10.3), the corresponding ripple energy the auxiliary capacitor handles is $R_v C_a V_{a0}^2$. For a desiredV_{a0}, the ripple ratio increases with the ripple energy. Hence, Method B is good for systems with high ripple energy and Method A is good for systems with low ripple energy.

10.2.6.3 Method C: To maintain a given minimum voltage V_{amin}^* for V_a

As discussed above, in order to maintain the normal operation of the ripple eliminator in the DCM, the voltage of the auxiliary capacitor should be controlled to be higher than a certain value. It is then natural to regulate V_a so that it is higher than a minimum voltage V_{amin}^*. This can be achieved with the strategy shown in Fig. 10.7(c), where the ripple ratio R_v^* in Method B is automatically adjusted according to the operational condition as

$$R_v^* = 2(1 - \frac{V_{amin}^*}{V_{a0}}). \tag{10.29}$$

By doing this, the voltage stress of the auxiliary capacitor can be kept at the minimum while maintaining good performance under different load conditions. The parameters of the PI controller can be chosen the same as the ones for Method B because the only change is to set the reference R_v^* as a specific value given in (10.29).

The difference from Method B is that the minimum voltage is kept constant and the ripple ratio changes here when the load changes but with Method B the ripple ratio is

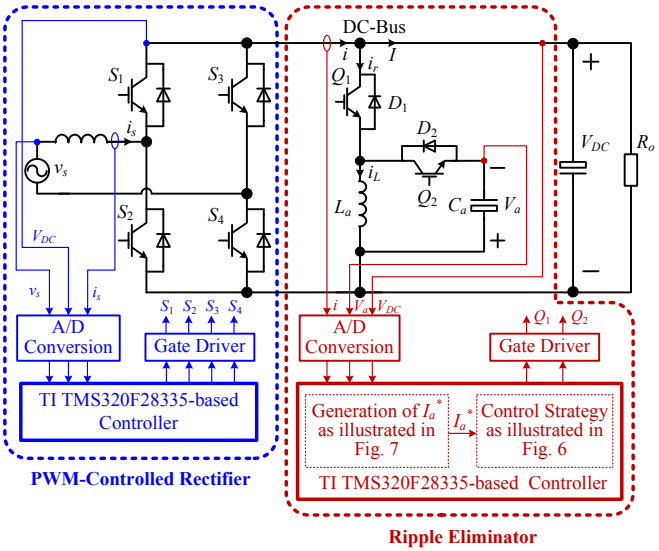


Fig. 10.8: Overall control schematic of the test rig.

Table 10.1: Parameters of the experimental system

Parameters	Values
Supply voltage (RMS)	230 V
Supply frequency f	50 Hz
Switching frequency of the PWM-controlled rectifier	10 kHz
Switching frequency of the ripple eliminator f_r	18 kHz
AC-side inductor L	2.2 mH
DC-bus capacitance C	110 μF
DC-bus voltage V_{DC}	400 V
Rectifier load (resistor R_o)	170 Ω
Auxiliary inductance L_a	0.55 mH
Auxiliary capacitance C_a	165 μF

kept constant and the minimum voltage changes. In other words, Method C actually keeps the minimum voltage stress on the auxiliary capacitor without affecting the current tracking performance. In addition, maintaining the minimum voltage can reduce the operating voltage of the capacitor. Therefore, the voltage rating of the capacitor needed in the ripple eliminator can be reduced accordingly. In summary, Method C is the most appropriate one among the three methods.

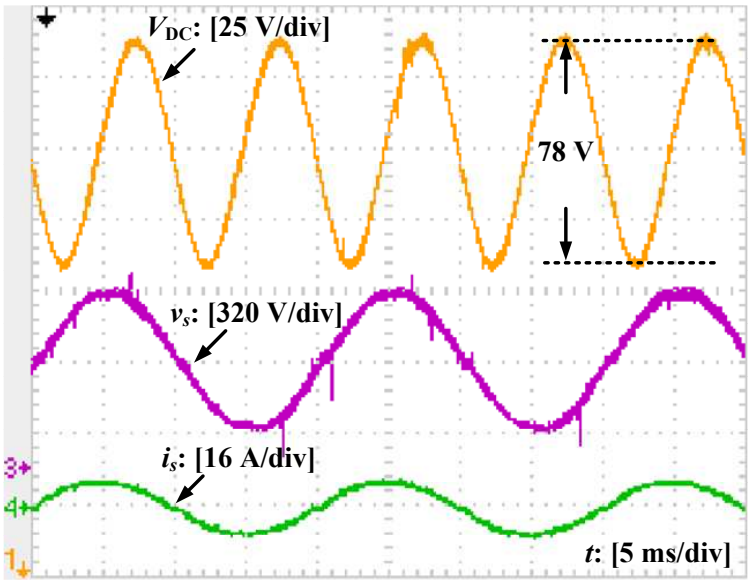
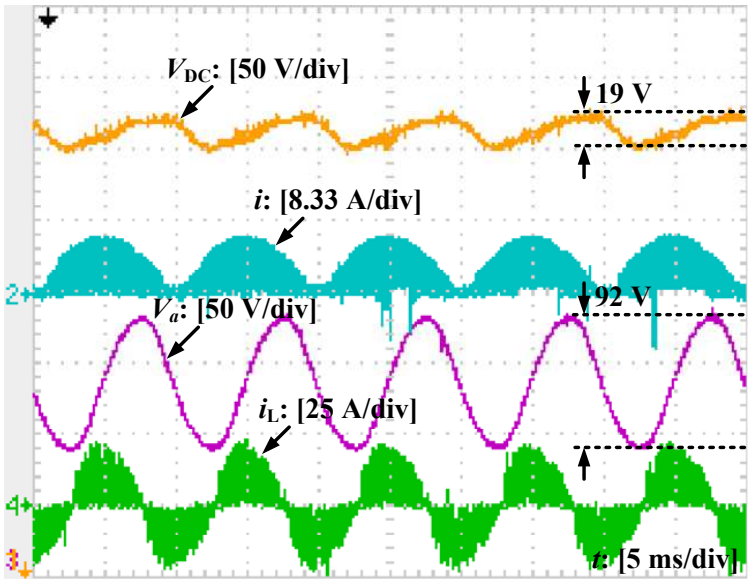
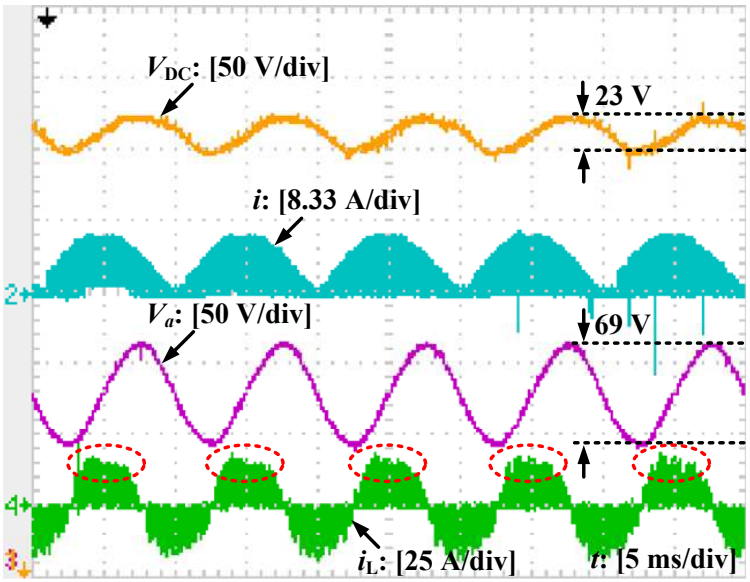


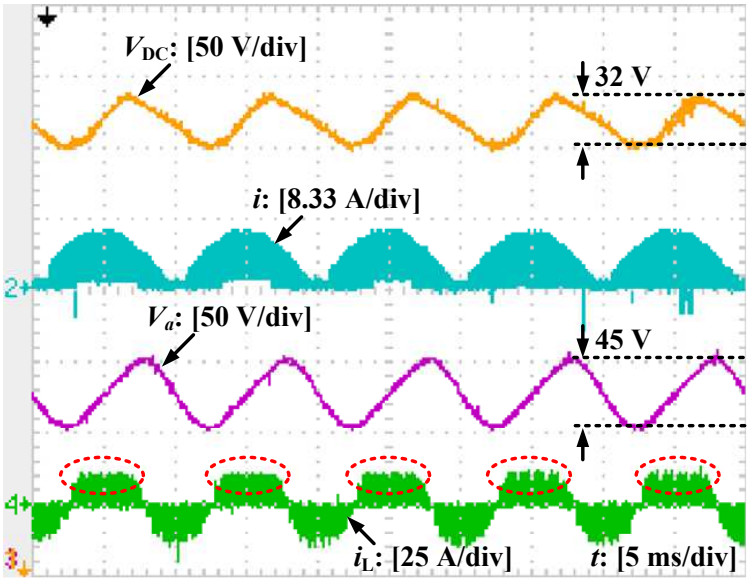
Fig. 10.9: Experimental results of the PWM-controlled rectifier.



(a)



(b)



(c)

Fig. 10.10: Steady-state experimental results of the buck/boost strategy in (Wang et al., 2011): (a) $V_{a0}^{*} = 200$ V. (b) $V_{a0}^{*} = 250$ V. (c) $V_{a0}^{*} = 300$ V.

10.3 Experimental Results

In order to verify the proposed strategy, some experiments were carried out with a 1 kW prototype. The test rig consists of a single-phase PWM-controlled rectifier and the ripple eliminator, as shown in Fig. 10.8. The rectifier and the ripple eliminator were controlled

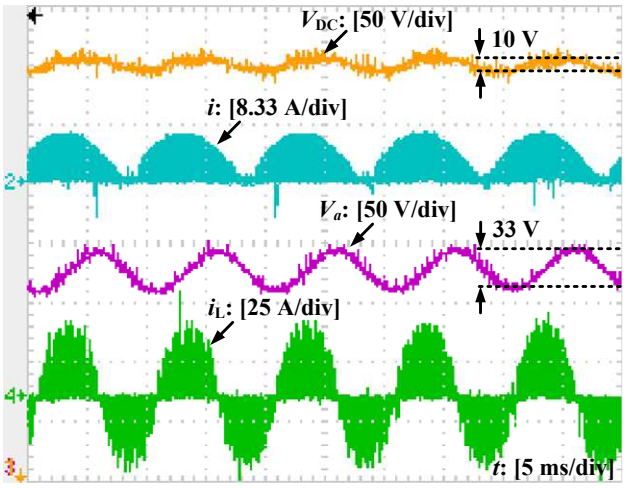
separately using two TI TMS320F28335 without any communication. The parameters of the system are listed in Table 10.1. In order to demonstrate the effectiveness of the ripple eliminator later, experiments were carried out on the test rig without the ripple eliminator at first. The results are shown in Fig. 10.9. The input current is in phase with the input voltage but the voltage ripple on the DC-bus is 78 V.

10.3.1 Performance of the Strategy in (Wang et al., 2011)

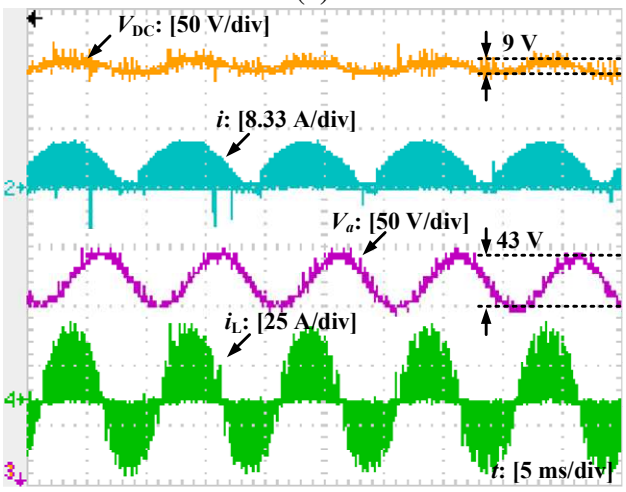
In order to demonstrate the performance of the ripple eliminator, the experimental system was re-configured according to the topology and the control strategy proposed in (Wang et al., 2011). The results when the auxiliary-capacitor voltage was maintained at 200 V, 250 V and 300 V are shown in Fig. 10.10. The DC-bus voltage ripples were reduced from the original 78 V to 19 V when the auxiliary-capacitor voltage was controlled at 200 V. However, the voltage ripple increased to 23 V when the auxiliary-capacitor voltage was controlled at 250 V because the positive part of the ripple current was not well diverted to the auxiliary capacitor, as can be seen from the positive part of the current i_L (highlighted in the figure with dashed ovals) because the auxiliary-capacitor voltage cannot be higher than a certain value in the charging mode. When the auxiliary-capacitor voltage was controlled at 300 V, the performance was deteriorated further and the ripple voltage increased to 32 V and the positive part of the ripple current was not diverted well at all.

10.3.2 Performance of the Eliminator Controlled with Method A

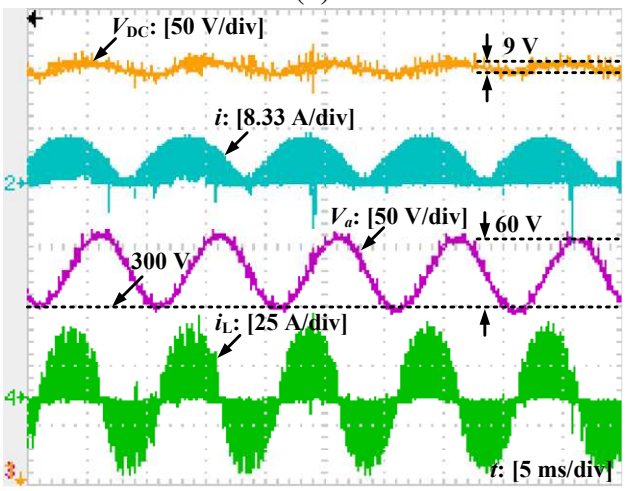
The ripple eliminator was tested with Method A to maintain a given V_{a0}^* ($V_{a0}^* = 600$ V), where the PI controller was easily tuned as $K_P = 0.01$ and $K_I = 0.02$. The results are shown in Fig. 10.11 (a). Moreover, the voltage V_{a0} was also controlled to 400 V (the same as V_{DC}) and 300 V (lower than V_{DC}), respectively. The DC-bus voltage ripples are all reduced to 9~10 V. What is more important is that the higher the V_{a0} the smaller the ripple on C_a, with the lowest of 33 V for $V_{a0} = 600$ V, which means the capacitance of C_a can be further reduced as well. Since the voltage of the auxiliary capacitor can be regulated flexibly in a wide range, in particular, without an upper limit, the ripple eliminator can be packed as a module and installed on different DC microgrids at different voltage levels, which facilitates the manufacture of ripple eliminators.



(a)

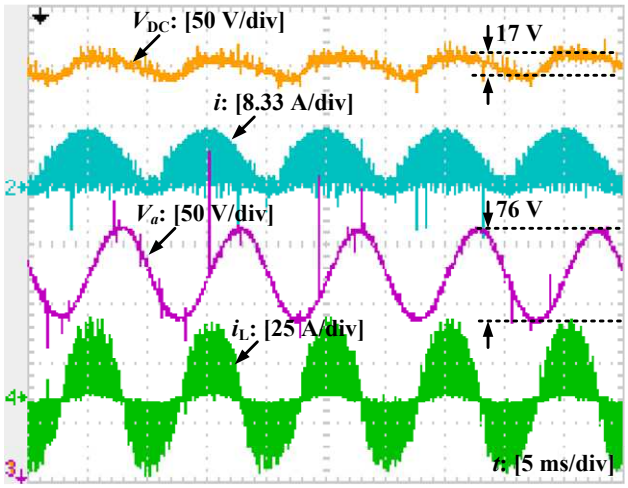


(b)

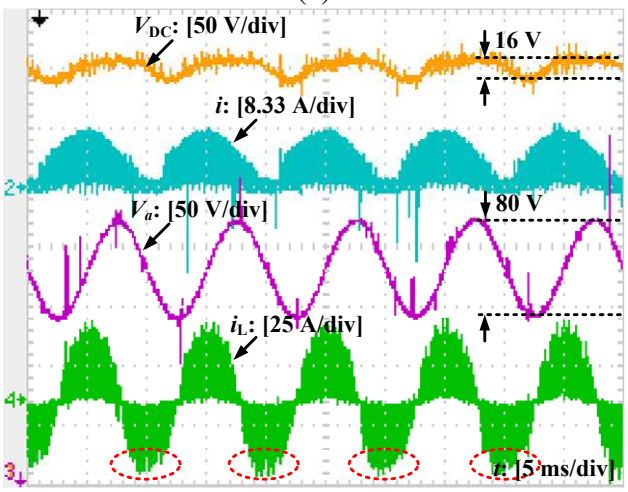


(c)

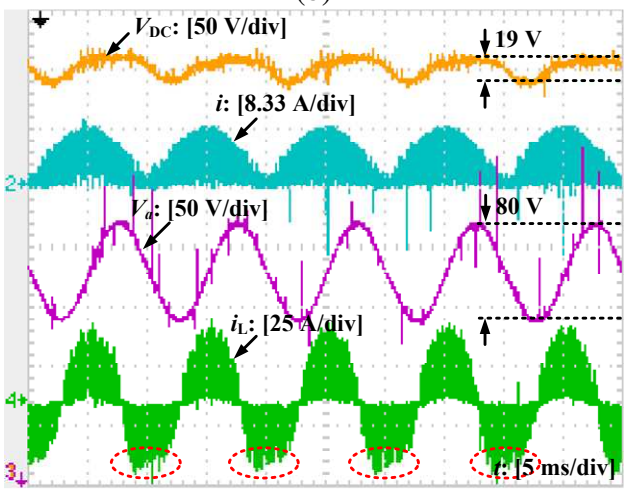
Fig. 10.11: Experimental results of the ripple eliminator with different methods(steady-state): (a) Method A to maintain $V_{a0}^* = 600$ V. (b) Method B to maintain a fixed ripple ratio $R_v^* = 10\%$. (c) Method C to maintain a given minimum voltage $V_{amin}^* = 300$ V.



(a)



(b)



(c)

Fig. 10.12: Experimental verification of the required minimum auxiliary-capacitor voltage: (a) $V_{a0}^{*} = 280$ V. (b) $V_{a0}^{*} = 260$ V. (c) $V_{a0}^{*} = 250$ V.

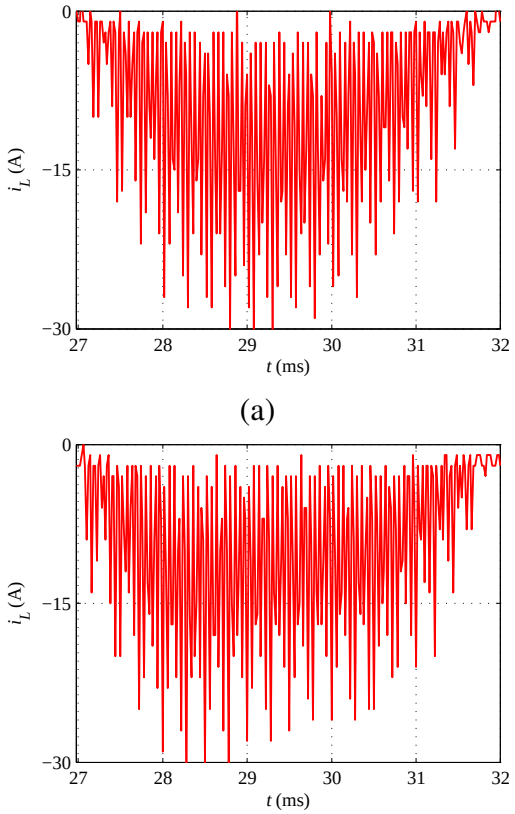


Fig. 10.13: Expanded negative parts of current i_L: (a) $V_{a0}^* = 280$ V. (b) $V_{a0}^* = 250$ V.

In order to demonstrate the lower-limit requirement on the auxiliary-capacitor voltage, the ripple eliminator was tested with $V_{a0}^* = 250$ V, 260 V and 280 V, respectively, and the results are shown in Fig. 10.12. When $V_{a0}^* = 250$ V, the negative part of the current i_L (highlighted in the figure with dashed ovals) does not closely follow the shape of the ripple current to be compensated, of which the major component is a second-order harmonics, so the ripple current was not diverted well to the ripple eliminator. This can be easily seen when comparing the figures with those in Fig. 10.11 and also from the expanded negative parts of current i_L for $V_{a0}^* = 250$ V and 280 V shown in Fig. 10.13, which are re-drawn from the oscilloscope data recorded. The performance became better when the auxiliary-capacitor voltage was increased. When the ripple current was diverted well to the ripple eliminator, the ripple current and the peak inductor current were measured approximately to be $I_{rm} = 7$ A and $I_{Lp} = 35$A. According to (10.25), the minimum auxiliary-capacitor voltage required is 267 V. When $V_{a0}^* = 260$ V, the ripple current was still not diverted well (although

only slightly), as highlighted in the figure, but when $V_{a0}^{*} = 280$ V, the ripple current was diverted well. It can be seen from the waveforms that indeed the ripple (inductor) current reaches the maximum value around the point when V_a crosses the average value V_{a0} and it is very accurate to replace V_a in (10.25) with V_{a0} to calculate the minimum auxiliary-capacitor voltage required.

10.3.3 Performance of the Ripple Eliminator Controlled with Method B

The ripple eliminator was tested with Method B to maintain a given ripple ratio R_v^*, where the PI controller was easily tuned with trial-and-error to be $K_P = 0.1$ and $K_I = 0.1$. The results are shown in Fig. 10.11 (b) for $R_v^* = 10\%$. In addition, the ripple ratio R_v was also controlled to be 4% and 20%, respectively. Due to the limited pages, not all results are given here. Since the ripple ratio of $R_v^* = 4\%$ is very tight, V_{a0} has to be high and it increased to about 710 V. It went down to 465 V and 328 V for $R_v^* = 10\%$ and 20%, respectively. The DC-bus voltage ripples were all kept at 9 V and the voltage ripple ratio was also regulated accurately.

10.3.4 Performance of the Ripple Eliminator Controlled with Method C

The ripple eliminator was tested with Method C to maintain a given minimum auxiliary-capacitor voltage V_{amin}^*, where the PI controller used in Method B with $K_P = 0.1$ and $K_I = 0.1$ was used. The results are shown in Fig. 10.11 (c) for $V_{amin}^* = 300$ V. Moreover, the minimum auxiliary-capacitor voltage V_{amin} was also controlled to be 400 V and 500 V, respectively. Due to the page limit , the results were omitted. The DC-bus voltage ripples were kept at 9 V or 10 V and the minimum voltage for V_a was also regulated accurately. The corresponding voltage ripples on C_a was changed to 48 V and 38 V, respectively.

10.3.5 Summary of Steady-state Performance with the Three Control Methods

From (10.3), it can be seen that, for the same ripple energy, the ripple voltage on the auxiliary capacitor is determined by the average voltage. This does not change with the control method adopted. Fig. 10.14 shows the experimental result with Method B for the given ripple ratio $R_v^* = 20\%$. The ripple voltage is 64V and the average voltage is 328V. This is very close to the case shown in Fig. 10.11(c), where Method C was adopted with the given minimum voltage 300V, ripple voltage 60V and average voltage of about 330V.

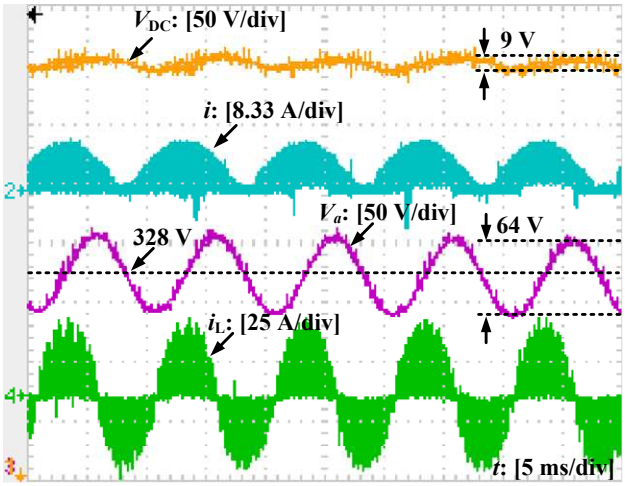


Fig. 10.14: Experimental results of the ripple eliminator with Method B to maintain a given ripple ratio $R_v^* = 20\%$.

In order to illustrate the relationship between the ripple voltage and average voltage on the auxiliary capacitor more clearly, the steady-state performance of the ripple eliminator under different cases tested with the three different methods is summarised in Table 10.2 and the voltage ripples on the DC bus and on the auxiliary capacitor are shown in Fig. 10.15. The DC-bus voltage ripples ΔV_{DC} were maintained to be 9~10 V over a wide range of V_{a0}. When V_{a0} dropped to below the minimum required voltage, the DC-bus voltage ripples increased. The voltage ripples ΔV_a on the auxiliary capacitor dropped when the voltage V_{a0} increased. The condition $V_{a0}\Delta V_a = constant$ given in (10.3) is demonstrated nicely when the ripple eliminator worked properly over a wide range of V_{a0} as shown in Fig. 10.15, where the experimental data fit well around the dashed line of $\frac{20290}{V_{a0}}$, although different control methods were adopted. Here, the number 20290 was found via curve

Table 10.2: Summary of the steady-state performance

Variables	Values											
Average auxiliary-capacitor voltage V_{a0} (V)	252	266	290	309	328	330	404	429	465	524	631	706
Ripple voltage on the auxiliary capacitor ΔV_a (V)	80	80	76	65	64	60	52	48	43	38	33	27
Ripple voltage on the DC bus ΔV_{DC} (V)	19	16	17	9	9	9	10	9	9	10	10	9
Method adopted	A	A	A	A	B	C	A	C	B	C	A	B

fitting.

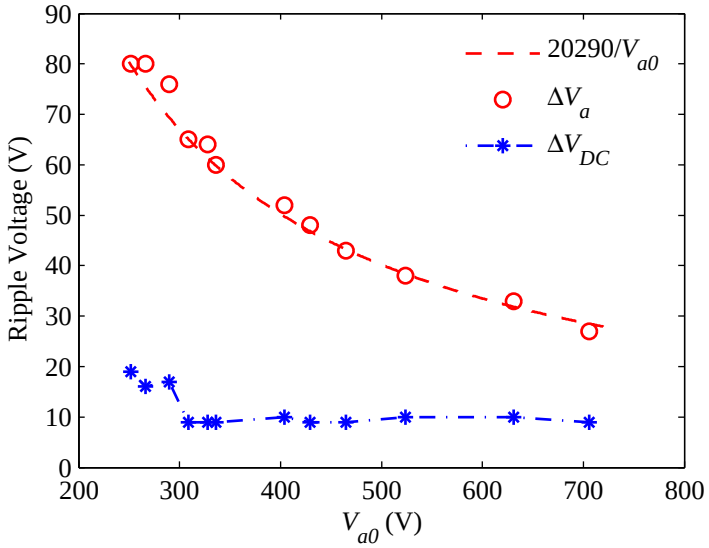


Fig. 10.15: Voltage ripples on the DC bus (ΔV_{DC}) and the capacitor C_a (ΔV_a) over a wide range of V_{a0}.

It is worth noting that the performance of the proposed strategy is much better than the one proposed in (Wang et al., 2011) when the auxiliary voltage is increased. However, if the auxiliary voltage is controlled to be the same level, then the performance is similar because the condition $V_{a0}\Delta V_a = constant$ still holds. For example, when the average auxiliary capacitor voltage is controlled to be 250V, the ripple voltage on the DC-bus is 19V for the proposed strategy, according to Table 10.2, and it is 23V for the strategy proposed in (Wang et al., 2011), according to Fig. 10.10(b).

10.3.6 Start-up and Stop of the Ripple Eliminator

When the system is initially started, the voltage V_a is zero, which makes D_d and I_a^* very large and, consequently, D_c is very large as well. As a result, a large current is drawn from the DC bus to charge the capacitor C_a. In order to prevent triggering the current protection, soft-start schemes can be adopted. Fig. 10.16(a) shows the soft-start performance of the ripple eliminator controlled with Method A for $V_{a0}^* = 400$ V. The reference ripple current i_r^* was gradually linearly increased from 10% to 100% within the first 18 ms. Moreover, the actual auxiliary-capacitor voltage V_{a0} was replaced with $5 + 2000t$ V within the first 40 ms (i.e., $V_{a0} = 5 \sim 85$V). The ripple eliminator quickly reacted and reduced the DC-bus voltage

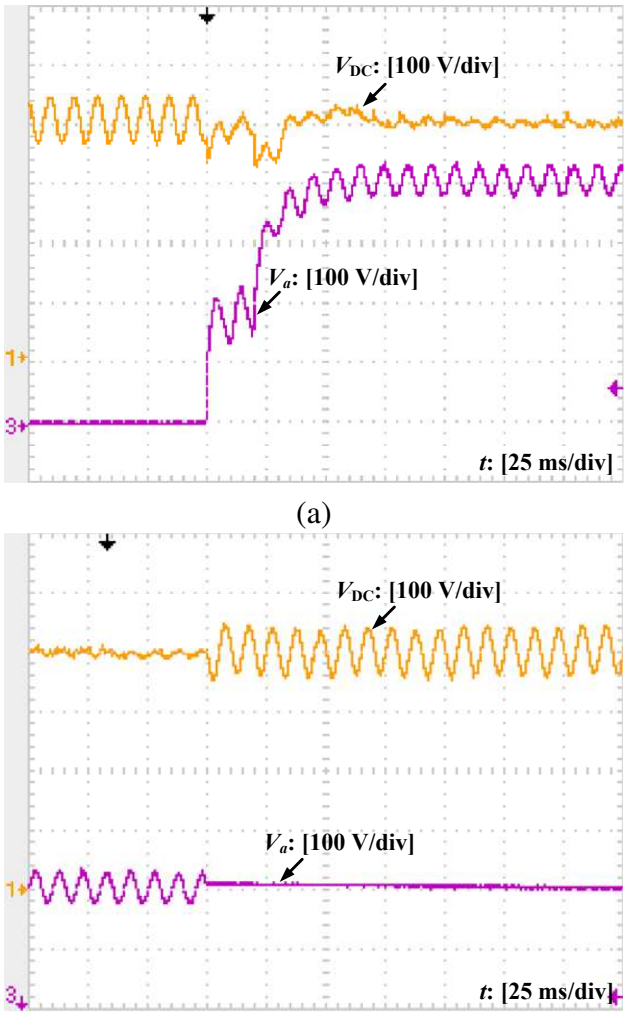


Fig. 10.16: Start-up and stop of the ripple eliminator controlled with Method A ($V_{a0}^{*} =$ 400V): (a) Start-up. (b) Stop.

ripple within 40 ms, resulting in very good dynamic performance. Of course, other soft-start options, e.g., to add a saturation unit to limit the lowest output from $H(s)$ or to regulate the charging current, could be adopted. Fig. 10.16(b) shows the experimental results when disabling the ripple eliminator. The DC-bus voltage ripple increased immediately.

Fig. 10.17 shows the start-up and stop of the ripple eliminator with Method B. A similar soft-start method was also adopted to avoid triggering the current protection. In order to demonstrate that the proposed strategy is not sensitive to the selection of the PI control parameters, $K_P = 160$ and $K_I = 160$ were used. The system was still stable although the response was a bit slower.

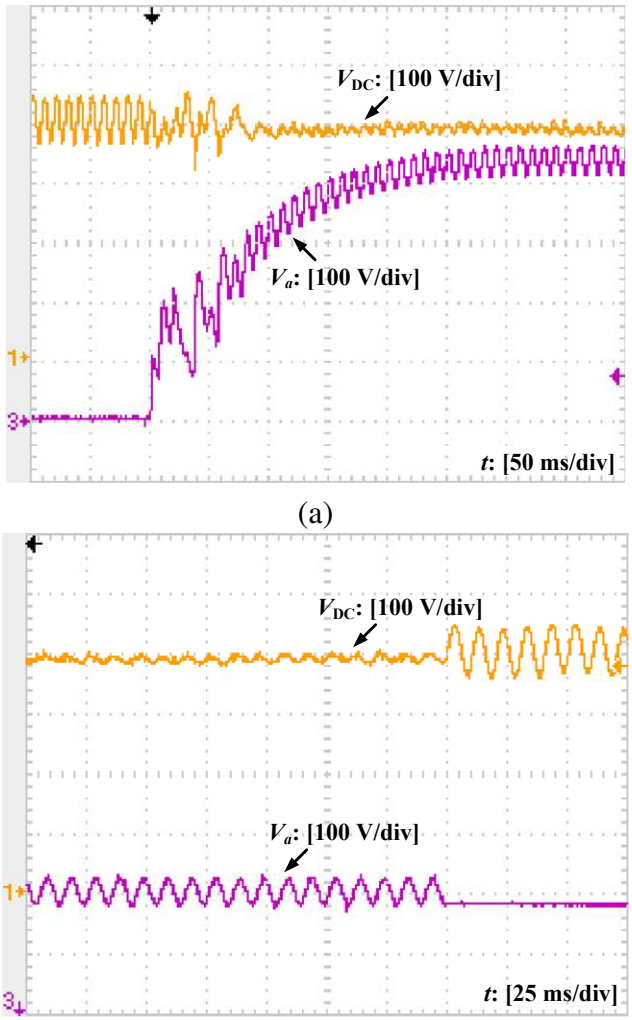


Fig. 10.17: Start-up and stop of the ripple eliminator controlled with Method B ($R_v^* = 10\%$): (a) Start-up. (b) Stop.

10.4 Summary

In this chapter, a ripple eliminator has been adopted to reduce the voltage ripples on a DC bus caused by the input source and, as a result, the conventionally needed large capacitance on the DC bus can be reduced. The ripple eliminator is a buck-boost converter terminated with an auxiliary capacitor and can transfer the voltage ripples on the DC bus to the auxiliary capacitor by diverting the ripple current on the DC bus to the ripple eliminator. The operational principle of the ripple eliminator is analysed in detail and a control strategy is proposed to achieve the function. The voltage on the auxiliary capacitor can be regulated either lower or higher than the DC-bus voltage, which relaxes the constraints on the system

design and also makes it possible to further reduce the auxiliary capacitance via increasing the voltage of the auxiliary capacitor. Hence, the total capacitance needed can be significantly reduced. In order to maintain proper operation, the average voltage of the auxiliary capacitor needs to be maintained above a certain level and three different strategies are proposed for this purpose to directly regulate the average voltage, the voltage ripple ratio or the minimum voltage. Experimental results have been presented to demonstrate the proposed strategy.

Chapter 11

CCM Ripple Eliminator to Further Reduce Low-frequency Voltage Ripples and Total Capacitance Required in DC Systems

In this chapter, a single-phase PWM-controlled rectifier is taken as an example to investigate how active control strategies can improve the power quality of DC systems, reduce voltage ripples and, at the same time, reduce the usage of electrolytic capacitors. The concept of ripple eliminators proposed in the Chapter 10 is further developed and the ratio of capacitance reduction is quantified. With such ripple eliminators, this power quality problem is formulated as a control problem to actively divert the ripple current on the DC bus. An advanced control strategy based on the repetitive control is proposed to one possible implementation of ripple eliminators in CCM. Experimental results are presented to validate the strategy, with comparison to the DCM ripple eliminator proposed in Chapter 10. It is found that the proposed CCM ripple eliminator leads to nearly four times improvement of performance than that of the DCM ripple eliminator.

11.1 Introduction

As discussed in Chapter 1, there are in total six approaches to reduce low-frequency voltage ripples. Some of the approaches are only effective in some specific DC systems while

the others are applicable to different kinds of DC systems. For example, the method of injecting harmonics to mitigate pulsating power is specially designed for rectifier systems (Wang et al., 2010; Gu et al., 2009). In DC systems, there might be different kinds of widely-distributed sources and loads and hence, it is hard to apply this method to all sources and/or loads. From this point of view, it becomes obvious that the last two approaches are more effective to improve the power quality for general DC systems, although more power components are required. Compared to the sixth approach, i.e. adding a series eliminator, the fifth approach, i.e., adding a shunt eliminator, is more suitable for general DC systems because it does not need to cut off any lines for connecting eliminators. Shunt eliminators can be simply hooked onto the DC bus for the purpose of reducing voltage ripples to improve power quality in DC systems.

The main focus of this chapter is to investigate how advanced control strategies could improve the performance of the fifth approach for DC systems, rather than optimizing the system performance through topological design. The fifth approach, i.e. bypassing the ripple energy with a shunt circuit, called a ripple eliminator (Cao et al., 2015), is taken as an example to further develop this general concept so that the ripples on the DC bus is eliminated and the capacitance needed is reduced. The level of reduction of capacitance is quantified. Moreover, it is found that the capability of diverting the ripple current away from the DC bus is the key for improving the performance. Hence, it is important to adopt a control strategy that is able to track periodic signals and the repetitive control strategy (Hara et al., 1988; Hornik and Zhong, 2011a; Zhong and Hornik, 2013a) is then applied to achieve instantaneous current tracking at a fixed switching frequency. Furthermore, it is preferred to operating the ripple eliminator in the continuous current mode (CCM) rather than in the discontinuous current mode (DCM) because the current tracking is instantaneous in CCM but is in the average sense in DCM. Because the ripple current is diverted instantaneously in CCM, the voltage ripples can be reduced considerably. The topology in (Wang et al., 2012), where a flicker-free AC–DC LED driver with a flyback PFC converter was designed and the strategy about how to remove the ripple power through tracking the ripple current generated by the flyback converter was analysed, is taken as an example to demonstrate the performance improvement by designing a suitable controller. This topology was also investigated in (Kyritsis et al., 2007; 2008). It is a bidirectional buck-boost converter that

is able to divert the ripple current *instantaneously*. The voltage of the auxiliary capacitor is higher than the DC-bus voltage, which helps improve the current tracking performance and reduce the required capacitance to achieve the same performance.

The rest of the chapter is organised as follows. In Section 11.2, a single-phase H-bridge PWM rectifier is taken as an example to analyse the ripple energy and ripple voltage in a DC system. In Section 11.3, the concept of ripple eliminators is further developed and the level of reduction of capacitance is quantified. In Section 11.4, the operation principle of the ripple eliminator under investigation is discussed and in Section 11.5 the control strategy of the ripple eliminator is developed based on repetitive control. Experimental results with comparison to a ripple eliminator reported in the literature are provided in Section 11.6, with the summary made in Section 11.7.

11.2 Analysis of Ripple Energy and Ripple Voltage

In order to facilitate the analysis in this chapter, a single-phase H-bridge PWM-controlled rectifier as shown in Figure 11.1 is used as an example, with all the components assumed to be ideal to simplify the analysis in the sequel. Most of the findings can be easily applied to other applications.

If the input current of the rectifier is regulated to be sinusoidal as $i_s = \sqrt{2}I_s \sin(\omega t)$ and in phase with the input voltage $v_s = \sqrt{2}V_s \sin(\omega t)$, then the input power is

$$p_s = v_s i_s = V_s I_s - V_s I_s \cos(2\omega t), \tag{11.1}$$

where V_s and I_s are the RMS values of the input voltage and current, respectively, and ω is the angular line frequency. Note that the power drawn from the AC source consists of a constant $V_s I_s$ and a second-order ripple component $-V_s I_s \cos(2\omega t)$.

In order to analyse the voltage ripples of the DC bus, the net change of the energy stored in the DC-bus capacitor over a charging period (i.e. a quarter cycle of the supply), called the ripple energy, can be calculated as (Wang et al., 2011)

$$E_r = \frac{V_s I_s}{\omega}. \tag{11.2}$$

As demonstrated in (Wang et al., 2011), the voltage ripple (peak-peak) on the DC-bus

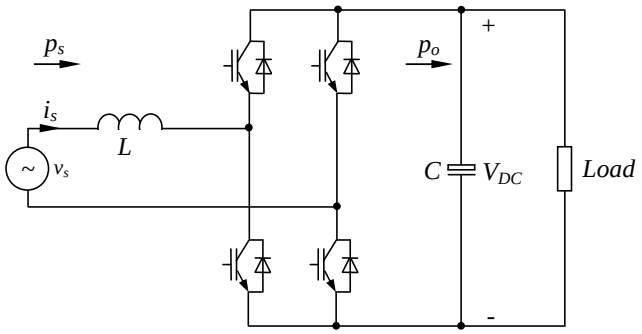


Figure 11.1: Single-phase H-bridge PWM-controlled rectifier.

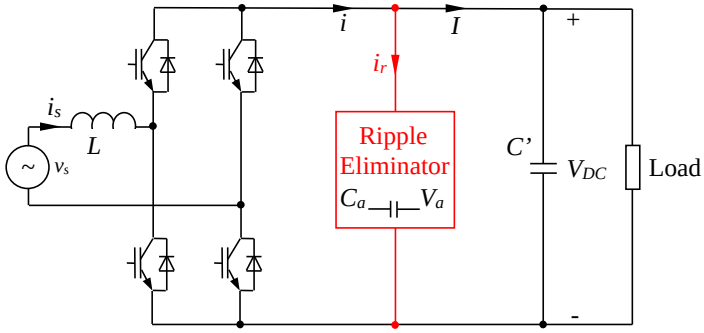


Figure 11.2: The concept of ripple eliminators.

capacitor can be calculated as

$$\triangle V_{DC} \approx \frac{E_r}{CV_{DC0}} \tag{11.3}$$

where V_{DC0} is the average value of the voltage V_{DC}. It is clear that when increasing the capacitor C the DC-bus voltage ripple is decreased but this increases the weight, volume and cost of the system and decreases the reliability of the system, which should be avoided if possible.

11.3 Ripple Eliminators and the Level of Capacitance Reduction

In order to break the deadlock between minimising the required capacitors and reducing voltage ripples, another design degree of freedom, called the ripple eliminator (Cao et al., 2015), can be introduced to replace the bulky DC-bus capacitor, as shown in Figure 11.2.

The basic idea is to introduce an auxiliary capacitor C_a in the ripple eliminator so that the ripples on the DC bus can be transferred onto C_a. The voltage V_a across the auxiliary capacitor C_a is allowed to vary within a wide range with a large ripple $\triangle V_a$. This concept can be regarded as the general form of the strategies proposed in the literature, e.g. (Wang et al., 2011; 2012).

Since the ripple eliminator is operated to divert the ripple energy on the DC bus to the auxiliary capacitor, there is no need to use a large electrolytic capacitor on the DC bus and the ripple power on the auxiliary capacitor should be equal to the DC-bus ripple power in the ideal case. Applying (11.3) to the auxiliary capacitor, there is

$$C_a \approx \frac{E_r}{\triangle V_a V_{a0}}, \tag{11.4}$$

where $\triangle V_a$ and V_{a0} are the peak-peak and average voltages of the auxiliary capacitor. Note that the ripple energy E_r is determined by the DC bus and not affected by the added ripple eliminator. Note also that the auxiliary capacitor is designed to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor is

$$r_a = \frac{\triangle V_a}{V_{a0}}.$$

Then (11.4) can be re-written as

$$C_a \approx \frac{E_r}{r_a V_{a0}^2}. \tag{11.5}$$

It is clear that for the same ripple ratio r_a, the capacitance is in inverse proportion to the square of the voltage across it, which means the auxiliary capacitance can be significantly reduced via increasing its operating voltage.

If the same ripple energy E_r needs to be taken care of by a DC-bus capacitor C, as shown in Figure 11.1, then, according to (11.3), the voltage ripple ratio r of the DC bus is about

$$r \approx \frac{E_r}{C V_{DC0}^2}.$$

This means the auxiliary capacitor needed can be reduced to

$$C_a \approx \frac{r}{r_a}(\frac{V_{DC0}}{V_{a0}})^2 C$$

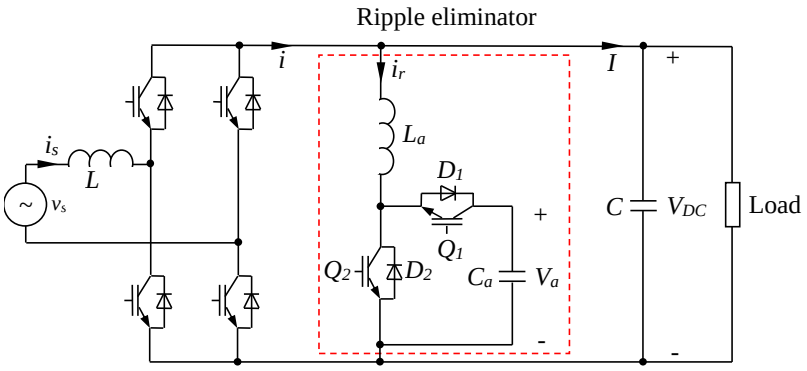


Figure 11.3: The ripple eliminator under Investigation.

by a factor of

$$R_d = \frac{r_a}{r}\left(\frac{V_{a0}}{V_{DC0}}\right)^2 = \frac{\Delta V_a V_{a0}}{\Delta V_{DC} V_{DC0}}. \tag{11.6}$$

The capacitance C_a can be reduced by 1) allowing the voltage ripple ratio higher than that of the original DC bus, 2) adopting an operating voltage V_{a0} higher than V_{DC0} for C_a. The topology in (Wang et al., 2011) adopts a higher voltage ripple ratio and the strategy in (Cao et al., 2015) adopts both.

Note that (11.6) is independent of applications. It sets the basic guidelines for designing different ripple eliminators. Some other guidelines include: 1) a ripple eliminator needs to be able to provide bi-directional current path so that the ripple current can flow through; 2) the remaining level of ripples on the DC bus is determined by the performance of the ripple eliminator so the ripple eliminator needs to be controlled properly; 3) The hold-up time requirement (Wang et al., 2014), current stress and limited voltage rating of the capacitors should be taken into account when choosing capacitors. If the maximum voltage of the capacitor is determined, then increased capacitance means longer hold-up time and lower current stress, which are preferred in some applications. As a result, there are several trade-offs when selecting capacitors and they should be considered together for certain applications. If all the ripple current in i is bypassed through the ripple eliminator then the DC-bus capacitor C' only needs to take care of the switching ripples and hence small capacitors can be used.

11.4 The Ripple Eliminator under Investigation

In this chapter, a practical implementation of the ripple eliminator concept to be studied is shown in the dashed box of Figure 11.3, which is actually a bi-directional boost-buck converter. It can also be regarded as one phase of an inverter with the DC bus provided by the auxiliary capacitor C_a so it is able to divert a bidirectional current i_r away from the DC bus. This topology was studied in (Wang et al., 2012), where a flicker-free LED driver with a flyback PFC converter was designed and the strategy about how to remove the ripple energy through tracking the ripple current generated by the flyback converter was analysed in detail, and in (Kyritsis et al., 2007; 2008), where an active filter for single stage grid-connected PV modules was developed to eliminate the low frequency PV current ripple.

In order to track the ripple current, switches Q_1 and Q_2 can be controlled in two different switching modes. One is only to control Q_2 (Q_1, resp.) in the positive (negative, resp.) half cycle of the ripple current, which corresponds to the charging (discharging) mode. In the charging mode, Q_2 is controlled by a PWM signal and Q_1 is always OFF, which provides the path for the positive half cycle of the ripple current i_r, and hence, the ripple eliminator is operated as a boost converter. In the discharging mode, Q_2 is always OFF and Q_1 is controlled by a PWM signal, which provides the path for the negative half cycle of the ripple current i_r, and the circuit is operated as a buck converter. Therefore, the direction of the current flowing through the auxiliary inductor can only be negative or positive in one switching period.

Another switching mode is to control the two switches complementarily. That means switches Q_1 and Q_2 are controlled by two inverse PWM signals to track the ripple current and the voltage across the auxiliary inductor can be V_{DC} and $V_{DC} - V_a$ depending on the ON-OFF combinations of these two switches. In one PWM period, if Q_1 is ON, Q_2 is controlled by an inverse signal to keep OFF and vice versa. Different from the previous operation mode, the inductor current can be positive or negative even during one switching period. This is a very good feature because the current can be tracked very well no matter at zero-crossing points or at large current ripple conditions. In the previous mode, the sharp turn at the zero-crossing points causes rich harmonic content, which is hard for the controller to track. Since the final control objective is to reduce DC-bus voltage ripples, it

does not matter if the auxiliary current ripple is slightly large because of the high switching frequency. With the same system parameters, large ripple means a small inductor is needed, which can reduce the size of the ripple eliminator. In this chapter, in order to make full use of the ripple eliminator under different working conditions, Q_1 and Q_2 are operated complementarily to track the ripple current.

11.5 Control of the Ripple Eliminator

11.5.1 Formulation of the Control Problem

As discussed before, the DC voltage ripple is caused by the pulsating input energy. After the ripple eliminator is introduced to bypass the ripple current flowing through the capacitor, the DC-bus voltage then becomes ripple free, apart from switching ripples, and equal to the DC-bus voltage. Hence, the current to be diverted should be

$$i_r = -\frac{V_s I_s}{V_{DC0}} \cos(2\omega t), \tag{11.7}$$

which is a second-order harmonic current. Note that the current i_r could be different for other DC systems but it does not affect the analysis above. The control objective of the ripple eliminator is then to instantaneously divert i_r in (11.7) away from the DC bus through the ripple eliminator so that the current flows through the load does not contain ripples other than switching ripples. In other words, the control problem is to instantaneously track the ripple current i_r that corresponds to the ripple power via controlling Q_1 and Q_2.

Tracking the i_r can be achieved in terms of either averaged values or instantaneous values, which corresponds to the DCM or CCM operation of the ripple eliminator. Of course, the current tracking performance in CCM is better than that in DCM. Hence, the CCM operation is preferred. On the other hand, the inductor will have a relatively large size in order to keep the ripple current continuous. This can be mitigated if the ripple eliminator can be operated at high switching frequencies. For example, if MOSFETs instead of IGBTs are used to construct the eliminator, then the switching frequency can be very high, e.g., at 200 kHz, so that only a small inductor is needed. When it is operated in DCM, the inductor can be smaller but the maximum current flowing through the switches is much higher in DCM than that in CCM because of the average tracking. High current means high cost for

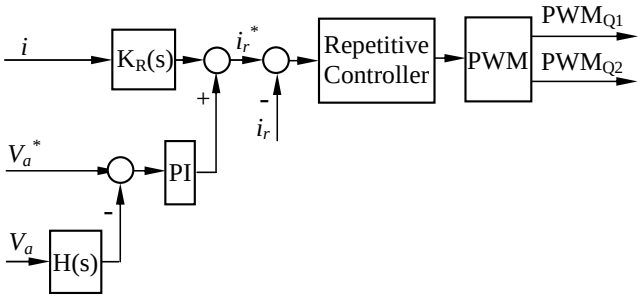


Figure 11.4: Control strategy for the ripple eliminator.

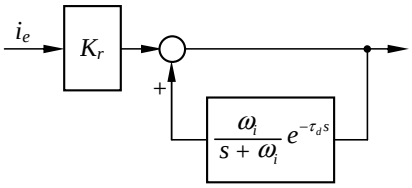


Figure 11.5: The repetitive controller.

switches.

In this chapter, the CCM operation is chosen because of its high performance for current tracking. The ripple current tracking can be achieved in two steps: 1) to generate a reference ripple current and 2) to track the reference ripple current. Moreover, in order to make sure that the current tracking can be achieved properly, the voltage across the auxiliary capacitor C_a should be regulated as well. The proposed overall control strategy is shown in Figure 11.4, which is explained in detail in the following subsections.

11.5.2 Regulation of the Auxiliary Capacitor Voltage

The operation of the ripple eliminator relies on a properly regulated auxiliary capacitor voltage, which is designed to allow a significant amount of ripples. In order to maintain the average DC component at a certain value, a low-pass filter can be adopted to remove ripples. Here, the hold filter

$$H(s) = \frac{1 - e^{-\tau s/2}}{\tau s/2} \tag{11.8}$$

where τ is the fundamental period of the system, is adopted to extract the average value of the voltage for control. Once the average voltage is obtained, it can be easily regulated at a given value V_a^* by using a PI controller, as shown in Figure 11.4, via charging or discharging the ripple eliminator. It is also possible to design the controller to regulate the

maximum or minimum value of the voltage, as reported in (Cao et al., 2015).

11.5.3 Generation of the Reference Ripple Current i_r^*

The second-order harmonic current of the current i between the rectifier and the ripple eliminator can be extracted by using the following resonant filter

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}$$

tuned at the second harmonic frequency with $\xi = 0.01$, $h = 2$, and $\omega = 2\pi f$. If the harmonic current has components at other frequencies, then $K_R(s)$ can be designed to include the corresponding term. For example, if there is a 3rd-order harmonic current, then $K_R(s)$ can include a term with $h = 3$. The extracted current can be added to the output of the PI controller that regulates the auxiliary capacitor voltage to form the reference ripple current i_r^*, as shown in Figure 11.4.

11.5.4 Design of a Repetitive Controller to Track the Reference Ripple Current

As explained before, the control problem is essentially a current tracking problem. Since the reference ripple current is periodic, the repetitive control strategy (Zhong and Hornik, 2013b; Hornik and Zhong, 2011a) can be adopted to achieve excellent tracking performance with a fixed switching frequency, as shown in Figure 11.4.

A repetitive controller contains an internal model, which is a local positive feedback loop involving a delay term and a low-pass filter, as shown in Figure 11.5. It introduces high gains at the fundamental and all harmonic frequencies of interest and hence, it is able to eliminate periodic errors (Hara et al., 1988), according to the internal model principle (Francis and Wonham, 1975). From the controllers designed with advanced control algorithms, e.g., the ones in (Hornik and Zhong, 2011a), the controllers that work with the repetitive control strategy can be very simple. In this chapter, since the problem is a current tracking problem, the proportional controller K_r cascaded with the internal model obtained in (Hornik and Zhong, 2011a; Zhong and Hornik, 2013b) with the H_∞ control strategy, as shown in Figure 11.5, is adopted. Here, $i_e = i_r^* - i_r$ is the current tracking error.

Table 11.1: Parameters of the test rig

Parameters	Values
Supply voltage (RMS)	230 V
Line frequency	50 Hz
PWM frequency	10 kHz
L	2.2 mH
L_a	2.2 mH
DC-bus capacitance C	110 μF
Auxiliary capacitance C_a	165 μF
DC-bus voltage V_{DC}	400 V

Based on the analysis in (Hornik and Zhong, 2011a; Weiss and Hafele, 1999), τ_d is selected as

$$\tau_d = \frac{\tau}{2} - \frac{1}{\omega_i} = 0.0099 \text{ s}$$

for $\omega_i = 10000$ rad/sec and $\tau = \frac{1}{f} = 0.02$ s. The proportional gain can be determined by following the procedures of H_∞ control design proposed in (Hornik and Zhong, 2011a; Zhong and Hornik, 2013b) or simply by tuning with trial-and-error.

11.6 Experimental Results

In order to verify the proposed control method, a test rig that consists of a 1.1 kW single-phase PWM-controlled rectifier and three kinds of ripple eliminators was built. The parameters of the PWM rectifier are summarized in Table 11.1. In this study, the ripple voltage ratio is selected below 10% for all the auxiliary capacitor voltage references from 500 V to 700 V. According to (11.5), C_a should be around 160 μF and is chosen as $C_a = 165\,\mu$F. Of course, this ratio could be greater than 10% in order to further decrease the capacitance needed as long as the auxiliary capacitor voltage is higher than the DC-bus voltage to ensure the normal operation of the ripple eliminator.

11.6.1 Control of the Single-phase PWM-controlled Rectifier

The PWM rectifier is adopted as an example for generating voltage/current ripples in a DC system. It is controlled to draw a clean sinusoidal current from the source that is in phase with the voltage source. This can be achieved with the controller shown in Fig-

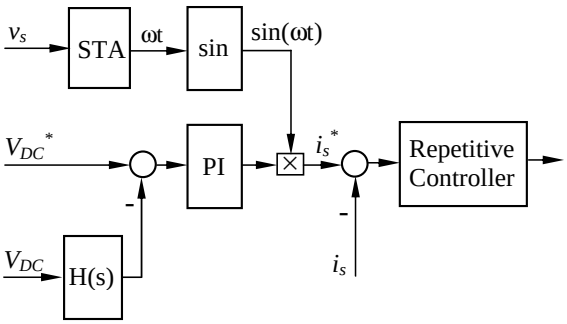


Figure 11.6: Controller for a single-phase PWM-controlled rectifier.

ure 11.6, which mainly consists of three parts: 1) a synchronisation unit to generate a clean sinusoidal current signal that is in phase with the source so that the reactive power drawn from the supply is controlled to be zero; 2) a PI controller that regulates the DC-bus voltage V_{DC} according to the DC-bus reference voltage V_{DC}^* to generate the right amplitude for the current reference; and 3) a current controller to track the reference current that is formed according to the output of the PI controller and the synchronisation signal. Here, the sinusoid-tracking algorithm (STA) (Ziarani and Konrad, 2004) is adopted to provide the phase information $\sin \omega t$ for the input current, as shown in Figure 11.6. In order to obtain the DC component of the DC-bus voltage, the hold filter (11.8) is adopted to remove the voltage ripples. This is able to reduce the ripple component in the reference current, which helps improve the power quality of the current drawn from the voltage source.

Since the reference current is periodic, the repetitive controller designed for the ripple eliminator can also be adopted to track the reference current, as shown in Figure 11.6.

11.6.2 Validation

11.6.2.1 Without the ripple eliminator

Figure 11.7 shows the experimental results of the single-phase PWM-controlled rectifier without the ripple eliminator. The input current was well regulated to be in phase with the source voltage to achieve the unity power factor. However, the DC-bus voltage ripple is about 90 V, which is often not acceptable in practice.

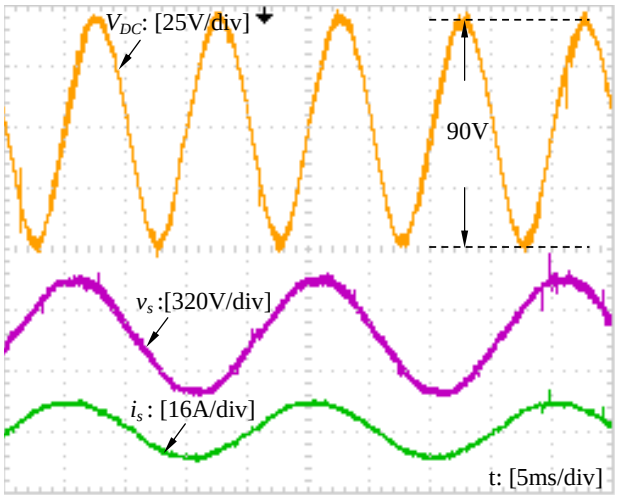
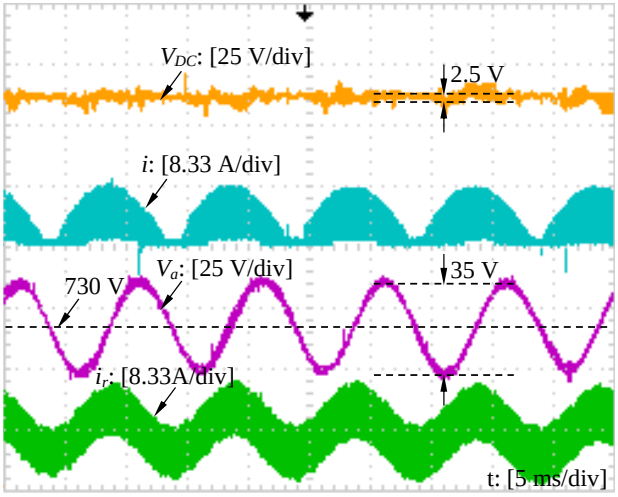


Figure 11.7: Experimental results when the ripple eliminator was not activated: DC-bus voltage V_{DC}, input voltage v_s and input current i_s.

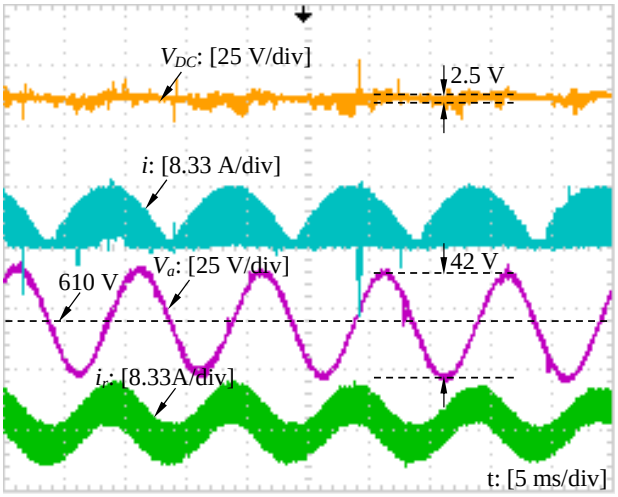
11.6.2.2 With the ripple eliminator activated

Figure 11.8 shows the results with the ripple eliminator activated. In order to investigate the effect of the auxiliary capacitor voltage on the reduction of the voltage ripple, different auxiliary capacitor voltages at 500 V, 600 V and 700 V were tested. Generally, it can be seen that the DC-bus voltage ripple was significantly reduced for all these three voltages. The performance is improved when the auxiliary capacitor voltage is increased because the inductor current tracking performance is improved when the auxiliary capacitor voltage increases. The DC-bus voltage ripple is around 2.5 V when the auxiliary capacitor voltage is 600 V and 700 V, which represents 36 times of improvement. Moreover, the voltage ripple on the auxiliary capacitor decreased with the increase of its DC voltage. The corresponding voltage ripples ΔV_{DC} and ΔV_a are shown in Figure 11.9. Based on the analysis in Section 11.3, the product of $\triangle V_a$ and V_{a0} should be a constant if the auxiliary capacitor is not changed. Indeed, the product is equal to about 25000 for the three different voltages 500 V, 600 V or 700 V. Moreover, the current ripple of the auxiliary inductor shown in Figure 11.8(b) crosses zero in most of PWM cycles.

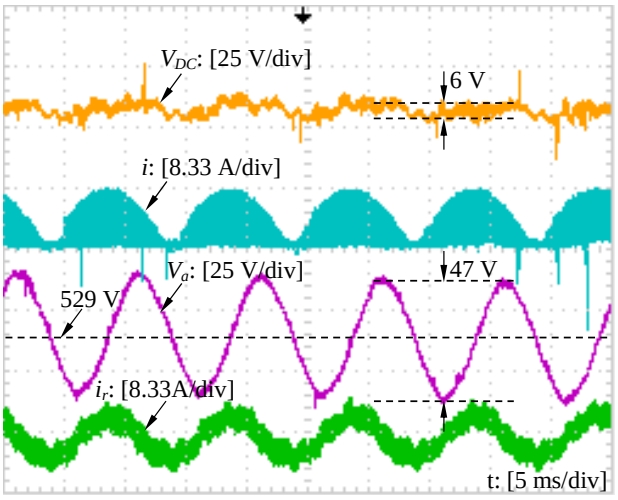
The high-frequency current ripples of the auxiliary-inductor current increased along with the increase of the auxiliary-capacitor voltage. Figure 11.10 shows the theoretical and experimental results of the auxiliary-inductor current ripples Δi_r. It can be seen that the experimental results match the calculated values well.



(a)



(b)



(c)

Figure 11.8: Experimental results with different auxiliary capacitor voltages: (a) $V_a^* = 700$ V. (b) $V_a^* = 600$ V. (c) $V_a^* = 500$ V.

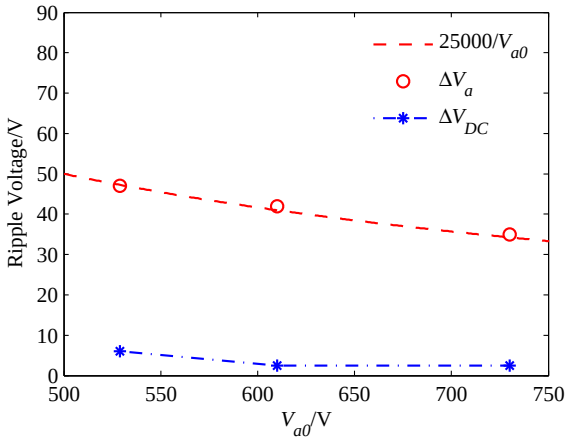


Figure 11.9: Voltage ripples on the DC bus (ΔV_{DC}) and the capacitor C_a (ΔV_a) of the proposed ripple eliminator tested over a wide range of V_{a0}.

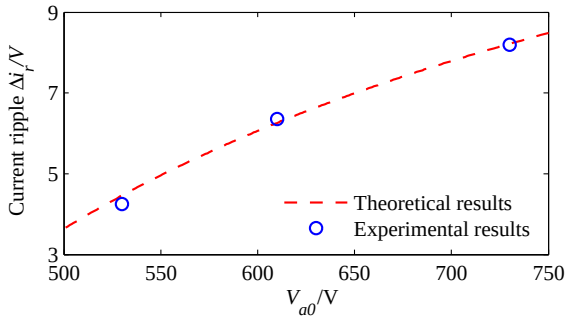
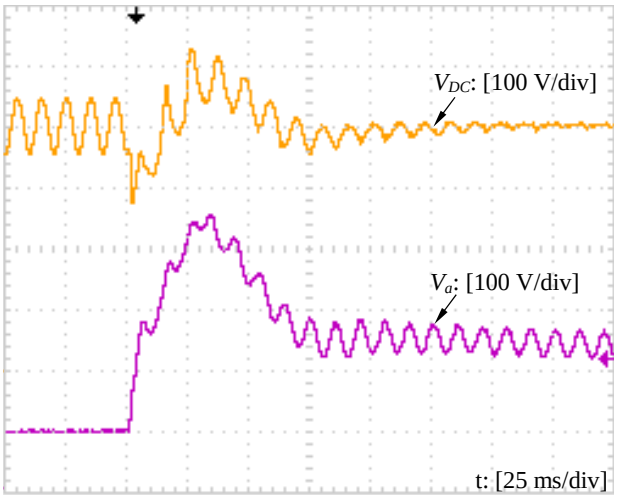
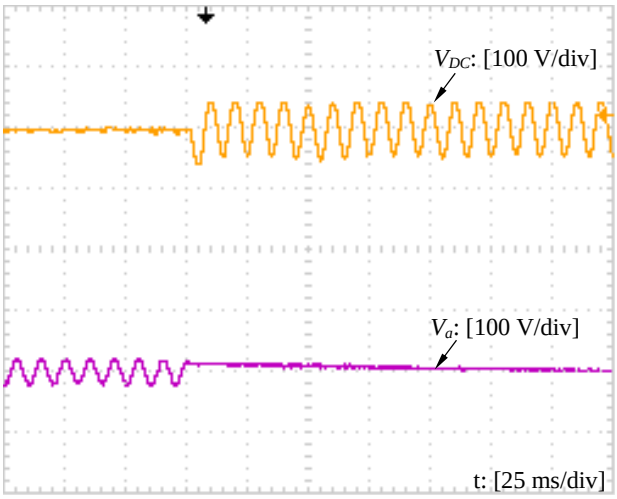


Figure 11.10: Current ripples Δi_r on the inductor L_a over a wide range of V_{a0}.



(a)



(b)

Figure 11.11: Dynamic performance of the proposed ripple eliminator ($V_{a0}^{*} = 600$ V): (a) Start-up. (b) Stop.

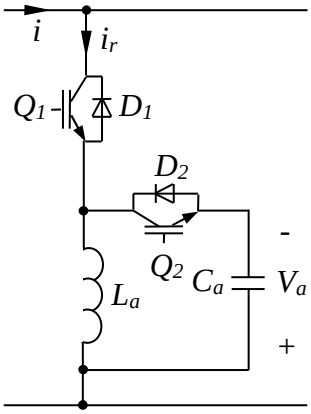
11.6.2.3 Dynamic performance

The dynamic performance of the ripple eliminator was tested. As shown in Figure 11.11(a), the voltage ripple was almost removed from the DC-bus voltage after the eliminator was activated for about seven line cycles. When the ripple eliminator was deactivated, the ripples of the DC-bus voltage immediately went back to about 90 V, as shown in Figure 11.11(b).

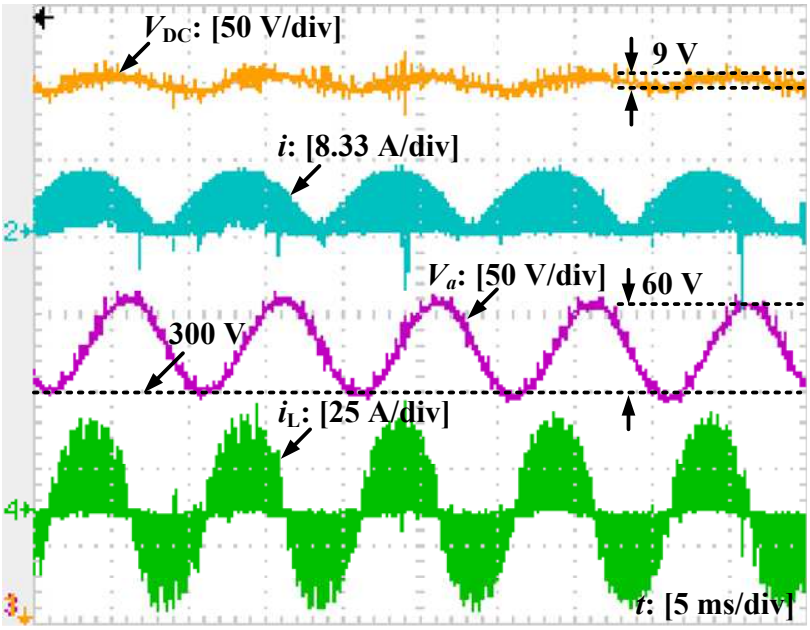
11.6.2.4 Comparison with the DCM ripple eliminator in (Cao et al., 2015)

The experimental results for the ripple eliminator reported in (Cao et al., 2015), as shown in Figure 11.12(a), are presented for comparison. The only difference in this topology is that the power switch Q_2 is swapped with the inductor L_a and the direction of the switch Q_1 is reversed. This makes the ripple eliminator either a buck or a boost converter and hence, the voltage of the auxiliary C_a can be higher or lower than the DC-bus voltage.

The inductor L_a is changed to 0.55 mH so that the eliminator can be operated in DCM as studied in (Cao et al., 2015) and the load is slightly lighter, 1 kW instead of 1.1 kW. The other parameters of the system are the same as given in Table 11.1. The experimental results are shown in Figure 11.12(b) when the minimum of the auxiliary voltage was regulated at 300 V. The DC-bus voltage ripple is about 9 V, which is almost 4 times of 2.5 V shown in



(a)



(b)

Figure 11.12: The DCM ripple eliminator studied in (Cao et al., 2015): (a) topology; (b) experimental results with $V^*_{amin} = 300$ V.

Figure 11.8(b) and 11.8(c) obtained with the proposed control strategy. The investigated eliminator can remove more than 97% of the voltage ripples from the DC bus but the DCM one shown in Figure 11.12(a) can only eliminate about 90% of the voltage ripples. Moreover, the voltage ripple of the auxiliary capacitor C_a increased to about 60 V because of the lower average voltage. It is also worth noting that the peak value of the compensation ripple current i_r nearly reached 30A, which is about 7 times of the peak current obtained in this chapter.

11.7 Summary

The concept of ripple eliminators has been further developed to improve the power quality and reduce the voltage ripples in DC systems and, at the same time, reduce the capacitance needed and the usage of electrolytic capacitors. After deriving the reduction ratio of the capacitance required, the focus of this chapter is on the design of an advanced control strategy so that the ripple current can be instantaneously compensated. Compared to the Chapter 10 and some other related research in the literature, this chapter has the following unique contributions: 1) It has been revealed that the capability of of instantly diverting the ripple current away from the DC bus is the key to improve the performance. As a result, ripple eliminators that can be operated in CCM to *instantaneously* divert ripple currents are preferred; 2) the repetitive control strategy is proposed to control one exemplar ripple eliminator, with the ripple energy provided by a single-phase PWM-controlled rectifier. It *instantaneously* compensates the ripple current on the DC bus so that the voltage ripples on the DC bus can be significantly reduced. Experimental results have demonstrated that the proposed strategy is valid and offers several times of performance improvement with comparison to a DCM ripple eliminator reported in the literature. It has been confirmed that it is important to operate ripple eliminators in CCM to instantaneously track the ripple current so that the DC-bus voltage ripples can be minimised to the greatest extent.

Chapter 12

Conclusions and Future Work

This chapter first concludes the work presented from Chapter 2 to Chapter 11 and then summarises some aspects that can be concentrated for future work.

12.1 Conclusions

In this thesis, active control techniques have been applied to innovatively address two fundamental challenges in power electronic converters, i.e. the need of bulky electrolytic capacitors and isolation transformers, in a holistic way. Such techniques pave the way to develop highly compact and reliable power electronic converters with minimum number of switches and passive components.

The focus has been first placed on the reduction of fundamental voltage ripples in conventional half-bridge converters. An actively-controlled neutral leg is added so that fundamental voltage ripples can be diverted from DC outputs. It has been demonstrated that the output voltage ripples are significantly reduced and, hence, the required capacitance to achieve the same level of voltage ripples is reduced compared to that in conventional half-bridge rectifiers. Then, the half-bridge converter with the neutral leg has been applied to construct a conversion system to generate independent three-phase voltage outputs from a single-phase voltage supply. The corresponding active control strategies have been proposed to properly operate the system. It is worth mentioning that only eight switches are needed, which means four of them have been saved compared to conventional solutions in the literature.

In addition to fundamental voltage ripples, the ρ-converter has been proposed to reduce

second-order and high-frequency CM voltage ripples in a holistic way. One of the two legs in the ρ-converter, i.e. the neutral leg, is actively controlled to divert all the ripples into the lower split capacitor so that the voltage across the upper split capacitor, designed to be the DC output voltage, has very small ripples in both fundamental and second-order frequencies. It has been demonstrated that the total capacitance required can be reduced by more than 70 times compared to that in conventional full-bridge converters so that film capacitors are cost-effective to be used. Moreover, high-frequency CM voltage ripples have been completely eliminated because the AC and DC grounds of the ρ-converter are directly connected together. As a result, isolation transformers are no longer needed. Measured CM voltages in experiments have been given for verification. In addition, the inversion mode of the ρ-converter has been discussed, which is controlled to mimic synchronous generators so that the converter can take part in the regulation of system voltage and frequency. As a result, the bidirectional ρ-converter has been fully functional, which can holistically remove fundamental, second-order and high-frequency CM voltage ripples with only four active switches.

The performance of the ρ-converter has been improved by further reduction of capacitors and also by the reduction of the neutral inductor, which are again achieved by using active control techniques. It has been found that the total capacitance required and the size of the neutral inductor can be reduced by more than 2.5 times and 9 times, respectively, compared to those in the ρ-converter. As a result, the power density, efficiency and reliability of the ρ-converter have been considerably improved.

Most of the aforementioned research are devoted to controlling voltage ripples in some specific PEC. In order to reduce low-frequency voltage ripples in *general* DC systems, two actively-controlled ripple eliminators have been proposed. One of ripple eliminators is operated in DCM with the feature that the voltage across the auxiliary capacitor in the eliminator can be either higher or lower than DC-bus voltage, which relaxes the constraints on the system design and also makes it possible to further reduce the auxiliary capacitance via increasing the voltage of the auxiliary capacitor. Then, another ripple eliminator has been proposed, which is operated in CCM. A comparison has been made between the two ripple eliminators and it has been found that instantaneous current tracking is the key to reduce voltage ripples and total capacitance required to the greatest extent. As a result,

CCM ripple eliminators are preferred.

12.2 Future Work

In order to further optimize the performance of systems proposed in the thesis, future research can be focused on the following aspects:

1. Reduction of voltage stress on active switches: The DC-bus voltage of the ρ-converter and θ-converter needs to be higher than the doubled grid voltage, which leads to doubled voltage stress on active switches compared to that of conventional full-bridge converters. Future research efforts can be focused on how to reduce this voltage stress by re-designing topologies of converters and/or employing advanced modulation strategies.

2. Widening DC output voltage: It is possible to combine Z-source and/or multi-terminal DC/DC converters with the developed power converters in a compact way, aiming to widen the range of the DC voltage with minimized number of switches and passive components and minimized power losses, and accordingly expand the application range of the converters.

3. Reducing impact of parasitic inductors in neutral line: The reduction of high-frequency CM voltages is achieved because AC and DC grounds of converters are directly connected together. In practice, power lines used for the connection are not pure resistive but have some parasitic inductors, which can affect the performance of reducing CM voltages. This may be solved by adding a small neutral capacitor and how to select such capacitor should be well explored in order to avoid introducing any resonance with the other parts of converters.

4. Two independent ripple-free outputs: It has been demonstrated that it is possible to use only four switches to provide two DC outputs with reduced fundamental voltage ripples. However, the outputs still contain a certain level of second-order voltage ripples. It is interesting to find out whether it is possible to remove second-order ripples from the two outputs at the same time but with the minimised number of switches.

5. Further improvement of efficiency: Soft-switching techniques can be introduced to reduce switching losses and hence help to improve efficiency of the developed converters. The key is to construct negative bias voltage and alternative current path to achieve zero-voltage on and zero-current off. Another possible optimization on efficiency could be achieved by integrating three-level T-type converter topology to the developed converters, which would also reduce filters required at the AC side of the developed converters and improve the system performance on the regulation of AC currents.

References

Afridi, K., M. Chen, and D. Perreault: 2014, 'Enhanced Bipolar Stacked Switched Capacitor Energy Buffers'. *IEEE Trans. Ind. Appl.* **50**(2), 1141–1149.

Babaei, E. and M. Seyed Mahmoodieh: 2014, 'Calculation of Output Voltage Ripple and Design Considerations of SEPIC Converter'. *IEEE Trans. Ind. Electron.* **61**(3), 1213–1222.

Bae, Y. and R.-Y. Kim: 2014, 'Suppression of Common-Mode Voltage Using a Multicentral Photovoltaic Inverter Topology With Synchronized PWM'. *IEEE Trans. Ind. Electron.* **61**(9), 4722–4733.

Baek, J.-B., W.-I. Choi, and B.-H. Cho: 2013, 'Digital Adaptive Frequency Modulation for Bidirectional DC-DC Converter'. *IEEE Trans. Ind. Electron.* **60**(11), 5167–5176.

Barater, D., G. Buticchi, E. Lorenzani, and C. Concari: 2014, 'Active Common-Mode Filter for Ground Leakage Current Reduction in Grid-Connected PV Converters Operating With Arbitrary Power Factor'. *IEEE Trans. Ind. Electron.* **61**(8), 3940–3950.

Blaabjerg, F., S. Freysson, H.-H. Hansen, and S. Hansen: 1997, 'A new optimized space-vector modulation strategy for a component-minimized voltage source inverter'. *IEEE Trans. Power Electron.* **12**(4), 704–714.

Boroyevich, D., I. Cvetkovic, R. Burgos, and D. Dong: 2013, 'Intergrid: A Future Electronic Energy Network?'. *IEEE Journal of Emerging and Selected Topics in Power Electronics* **1**(3), 127–138.

Bose, B.: 2001, *Modern Power Electronics and AC Drives*. Englewood Cliffs, NJ: Prentice-Hall.

Breazeale, L. and R. Ayyanar: 2015, 'A Photovoltaic Array Transformer-Less Inverter With Film Capacitors and Silicon Carbide Transistors'. *IEEE Trans. Power Electron.* **30**(3), 1297–1305.

Buticchi, G., D. Barater, E. Lorenzani, C. Concari, and G. Franceschini: 2014, 'A Nine-Level Grid-Connected Converter Topology for Single-Phase Transformerless PV Systems'. *IEEE Trans. Ind. Electron.* **61**(8), 3951–3960.

Cao, X., Q. Zhong, and W. Ming: 2015, 'Ripple Eliminator to Smooth DC-Bus Voltage and Reduce the Total Capacitance Required'. *IEEE Trans. Ind. Electron.* **62**(4), 2224–2235.

Castilla, M., J. Miret, J. Matas, L. Garcia de Vicuna, and J. Guerrero: 2009, 'Control Design Guidelines for Single-Phase Grid-Connected Photovoltaic Inverters With Damped Resonant Harmonic Compensators'. *IEEE Trans. Ind. Electron.* **56**(11), 4492–4501.

Cavalcanti, M., K. de Oliveira, A. de Farias, F. Neves, G. Azevedo, and F. Camboim: 2010, 'Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems'. *IEEE Trans. Ind. Electron.* **57**(4), 1360–1368.

Chang, H.-S., B.-H. Lee, H.-M. Woo, J.-D. La, and Y.-S. Kim: 2011, 'Study of the control technique of the voltage bus conditioner for a DC power distribution system with multiple parallel loads in the electrical vehicle'. In: *Electrical Machines and Systems (ICEMS), 2011 International Conference on*. Beijing, China, pp. 1–5.

Chao, K.-H., P.-T. Cheng, and T. Shimizu: 2009, 'New control methods for single phase PWM regenerative rectifier with power decoupling function'. In: *Proc. of International Conference Power Electronics and Drive Systems (PEDS)*. pp. 1091–1096.

Chen, M., K. Afridi, and D. Perreault: 2013, 'Stacked Switched Capacitor Energy Buffer Architecture'. *IEEE Trans. Power Electron.* **28**(11), 5183–5195.

Chen, W. and S. Hui: 2012, 'Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current'. *IEEE Trans. Power Electron.* **27**(3), 1598–1607.

Choi, W., J. Howze, and P. Enjeti: 2006, 'Development of an equivalent circuit model of a fuel cell to evaluate the effects of inverter ripple current'. *Journal of Power Sources* **158**(2), 1324 – 1332.

Cipriano dos Santos, E., C. Jacobina, J. Dias, and N. Rocha: 2011, 'Single-Phase to Three-Phase Universal Active Power Filter'. *IEEE Trans. Power Del.* **26**(3), 1361–1371.

Corless, R., G. Gonnet, D. Hare, D. Jeffrey, and D. Knuth: 1996, 'On the Lambert W function'. *Advances in Computational Mathematics* **5**, 329–359. Available at http://www.apmaths.uwo.ca/∼rcorless/frames/papers.htm, accessed on 3/9/2005.

da Silva, C., R. Pereira, L. da Silva, G. Lambert-Torres, B. Bose, and S. Ahn: 2010, 'A Digital PLL Scheme for Three-Phase System Using Modified Synchronous Reference Frame'. *IEEE Trans. Ind. Electron.* **57**(11), 3814–3821.

Dai, M., M. Marwali, J.-W. Jung, and A. Keyhani: 2005, 'A PWM rectifier control technique for three-phase double conversion UPS under unbalanced load'. In: *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, Vol. 1. pp. 548–552 Vol. 1.

Dai, M., M. Marwali, J.-W. Jung, and A. Keyhani: 2008, 'Power Flow Control of a Single Distributed Generation Unit'. *IEEE Trans. Power Electron.* **23**(1), 343–352.

Dong, D., I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli: 2013a, 'Grid-Interface Bidirectional Converter for Residential DC Distribution Systems—Part One: High-Density Two-Stage Topology'. *IEEE Trans. Power Electron.* **28**(4), 1655–1666.

Dong, D., F. Luo, D. Boroyevich, and P. Mattavelli: 2012a, 'Leakage Current Reduction in a Single-Phase Bidirectional AC–DC Full-Bridge Inverter'. *IEEE Trans. Power Electron.* **27**(10), 4281–4291.

Dong, D., F. Luo, X. Zhang, D. Boroyevich, and P. Mattavelli: 2013b, 'Grid-Interface Bidirectional Converter for Residential DC Distribution Systems—Part 2: AC and DC Interface Design With Passive Components Minimization'. *IEEE Trans. Power Electron.* **28**(4), 1667–1679.

Dong, D., T. Thacker, I. Cvetkovic, R. Burgos, D. Boroyevich, F. Wang, and G. Skutt: 2012b, 'Modes of Operation and System-Level Control of Single-Phase Bidirectional PWM Converter for Microgrid Systems'. *IEEE Transactions on Smart Grid* **3**(1), 93–104.

Du, X., L. Zhou, H. Lu, and H.-M. Tai: 2012, 'DC Link Active Power Filter for Three-Phase Diode Rectifier'. *IEEE Trans. Ind. Electron.* **59**(3), 1430–1442.

Dusmez, S. and A. Khaligh: 2014, 'Generalized Technique of Compensating Low-Frequency Component of Load Current With a Parallel Bidirectional DC/DC Converter'. *IEEE Trans. Power Electron.* **29**(11), 5892–5904.

Enjeti, P. and A. Rahman: 1993, 'A new single-phase to three-phase converter with active input current shaping for low cost AC motor drives'. *IEEE Trans. Ind. Appl.* **29**(4), 806–813.

Francis, B. and W. Wonham: 1975, 'The internal model principle for linear multivariable regulators'. *Applied Mathematics and Optimization* **2**(2), 170–194.

FREDDY TAN, K., N. Abd Rahim, W. Hew, and H. Che: 2015, 'Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter'. *IEEE Trans. Ind. Electron.* **62**(1), 322–331.

Fujita, H.: 2010, 'A high-efficiency solar power conditioner using a zigzag-connected chopper converter'. In: *Power Electronics Conference (IPEC), 2010 International*. pp. 1681–1687.

Garcia, O., M. Martinez-Avial, J. Cobos, J. Uceda, J. Gonzalez, and J. Navas: 2003, 'Harmonic reducer converter'. *IEEE Trans. Ind. Electron.* **50**(2), 322–327.

Gu, L., X. Ruan, M. Xu, and K. Yao: 2009, 'Means of Eliminating Electrolytic Capacitor in AC/DC Power Supplies for LED Lightings'. *IEEE Trans. Power Electron.* **24**(5), 1399–1408.

Gu, Y., W. Li, Y. Zhao, B. Yang, C. Li, and X. He: 2013, 'Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems'. *IEEE Trans. Power Electron.* **28**(2), 793–805.

Han, L. and N. Narendran: 2011, 'An Accelerated Test Method for Predicting the Useful Life of an LED Driver'. *IEEE Trans. Power Electron.* **26**(8), 2249–2257.

Hara, S., Y. Yamamoto, T. Omata, and M. Nakano: 1988, 'Repetitive control system: A new type servo system for periodic exogenous signals'. *IEEE Trans. Autom. Control* **33**, 659–668.

Harb, S., M. Mirjafari, and R. Balog: 2013, 'Ripple-Port Module-Integrated Inverter for Grid-Connected PV Applications'. *IEEE Trans. Ind. Appl.* **49**(6), 2692–2698.

Heldwein, M., T. Nussbaumer, and J. Kolar: 2010, 'Common mode modelling and filter design for a three-phase buck-type pulse width modulated rectifier system'. *IET Power Electronics* **3**(2), 209–218.

Hoang, K., Z. Zhu, and M. Foster: 2011, 'Influence and Compensation of Inverter Voltage Drop in Direct Torque-Controlled Four-Switch Three-Phase PM Brushless AC Drives'. *IEEE Trans. Power Electron.* **26**(8), 2343–2357.

Hornik, T. and Q.-C. Zhong: 2010, 'H^∞ repetitive voltage control of grid-connected inverters with frequency adaptive mechanism'. *IET Proc. Power Electron.* **3**(6), 925–935.

Hornik, T. and Q.-C. Zhong: 2011a, 'A current control strategy for voltage-source inverters in microgrids based on H^∞ and repetitive control'. *IEEE Trans. Power Electron.* **26**(3), 943–952.

Hornik, T. and Q.-C. Zhong: 2011b, 'H^∞ current control strategy for the neutral point of a three-phase inverter'. In: *Proc. of the 50th IEEE Conference on Decision and Control and European Control Conference*. pp. 520–525.

Hornik, T. and Q.-C. Zhong: 2013, 'Parallel PI Voltage–H^∞ Current Controller for the Neutral Point of a Three-Phase Inverter'. *IEEE Trans. Ind. Electron.* **60**(4), 1335–1343.

Hoseini, S., J. Adabi, and A. Sheikholeslami: 2014, 'Predictive modulation schemes to reduce common-mode voltage in three-phase inverters-fed AC drive systems'. *IET Power Electronics* **7**(4), 840–849.

Hou, C.-C., C.-C. Shih, P.-T. Cheng, and A. M. Hava: 2013, 'Common-Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters'. *IEEE Trans. Power Electron.* **28**(4), 1971–1979.

Itoh, J.-I. and F. Hayashi: 2010, 'Ripple Current Reduction of a Fuel Cell for a Single-Phase Isolated Converter Using a DC Active Filter With a Center Tap'. *IEEE Trans. Power Electron.* **25**(3), 550 –556.

Ji, B., J. Wang, and J. Zhao: 2013, 'High-Efficiency Single-Phase Transformerless PV H6 Inverter With Hybrid Modulation Method'. *IEEE Trans. Ind. Electron.* **60**(5), 2104–2115.

Kan, J., S. Xie, Y. Tang, and Y. Wu: 2014, 'Voltage-Fed Dual Active Bridge Bidirectional DC/DC Converter With an Immittance Network'. *IEEE Trans. Power Electron.* **29**(7), 3582–3590.

Karschny, D.: 1998, 'Wechselrichter'.

Kerekes, T., M. Liserre, R. Teodorescu, C. Klumpner, and M. Sumner: 2009, 'Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies'. *IEEE Trans. Power Electron.* **24**(9), 2202–2211.

Kerekes, T., R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas: 2011, 'A New High-Efficiency Single-Phase Transformerless PV Inverter Topology'. *IEEE Trans. Ind. Electron.* **58**(1), 184–191.

Keyhani, A., M. N. Marwali, and M. Dai: 2010, *Integration of Green and Renewable Energy in Electric Power Systems*. Hoboken, NJ: John Wiley & Sons.

Khalil, H. K.: 2001, *Nonlinear Systems*. Prentice Hall.

Kim, Y.-J., B.-J. Seok, H.-S. Jung, J.-D. La, and Y.-S. Kim: 2009, 'A Voltage Bus Conditioner with reduced capacitive storage'. In: *Electrical Machines and Systems (ICEMS), 2009 International Conference on*. Tokyo, Japan, pp. 1–6.

Kjaer, S., J. Pedersen, and F. Blaabjerg: 2005, 'A review of single-phase grid-connected inverters for photovoltaic modules'. *IEEE Trans. Ind. Appl.* **41**(5), 1292–1306.

Krein, P., R. Balog, and M. Mirjafari: 2012, 'Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port'. *IEEE Trans. Power Electron.* **27**(11), 4690–4698.

Kulkarni, C., G. Biswas, X. Koutsoukos, K. Goebel, and J. Celaya: 2010, 'Experimental studies of ageing in electrolytic capacitors'. In: *Annual Conference of the Prognostics and Health Management Society 2010*.

Kwak, S. and H. Toliyat: 2005, 'A hybrid solution for load-commutated-inverter-fed induction motor drives'. *IEEE Trans. Ind. Appl.* **41**(1), 83–90.

Kwon, J.-M., K. Eung-Ho, B.-H. Kwon, and K.-H. Nam: 2009, 'High-Efficiency Fuel Cell Power Conditioning System With Input Current Ripple Reduction'. *IEEE Trans. Ind. Electron.* **56**(3), 826–834.

Kyritsis, A., N. Papanikolaou, and E. Tatakis: 2007, 'A novel Parallel Active Filter for Current Pulsation Smoothing on single stage grid-connected AC-PV modules'. In: *Power Electronics and Applications, 2007 European Conference on*. pp. 1–10.

Kyritsis, A., N. Papanikolaou, and E. Tatakis: 2008, 'Enhanced Current Pulsation Smoothing Parallel Active Filter for single stage grid-connected AC-PV modules'. In: *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*. pp. 1287–1292.

Lamar, D., J. Sebastian, M. Arias, and A. Fernandez: 2012, 'On the Limit of the Output Capacitor Reduction in Power-Factor Correctors by Distorting the Line Input Current'. *IEEE Trans. Power Electron.* **27**(3), 1168–1176.

Lee, D.-C. and Y.-S. Kim: 2007, 'Control of Single-Phase-to-Three-Phase AC/DC/AC PWM Converters for Induction Motor Drives'. *IEEE Trans. Ind. Electron.* **54**(2), 797–804.

Lee, K., T. Jahns, G. Venkataramanan, and W. Berkopec: 2007, 'DC-Bus Electrolytic Capacitor Stress in Adjustable-Speed Drives Under Input Voltage Unbalance and Sag Conditions'. *IEEE Trans. Ind. Appl.* **43**(2), 495–504.

Lenwari, W., M. Sumner, and P. Zanchetta: 2006, 'A Novel High Performance Current Control for Shunt Active Filters'. In: *Proc. of the 12th International Power Electronics and Motion Control Conference (EPE-PEMC)*. pp. 1671–1676.

Li, H., K. Zhang, and H. Zhao: 2011a, 'Active DC-link power filter for single phase PWM rectifiers'. In: *Proc. of IEEE 8th International Power Electronics and ECCE Asia conference (ICPE & ECCE*. pp. 2920–2926.

Li, K., J. Liu, G. Xiao, and Z. Wang: 2006, 'Novel load ripple voltage-controlled parallel DC active power filters for high performance magnet power supplies'. *IEEE Trans. Nucl. Sci.* **53**(3), 1530–1539.

Li, Q. and P. Wolfs: 2008, 'A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations'. *IEEE Trans. Power Electron.* **23**(3), 1320–1333.

Li, S., G.-R. Zhu, S.-C. Tan, and S. Hui: 2015, 'Direct AC/DC Rectifier With Mitigated Low-Frequency Ripple Through Inductor-Current Waveform Control'. *IEEE Trans. Power Electron.* **30**(8), 4336–4348.

Li, X., W. Zhang, H. Li, R. Xie, M. Chen, G. Shen, and D. Xu: 2011b, 'Power Management Unit With Its Control for a Three-Phase Fuel Cell Power System Without Large Electrolytic Capacitors'. *IEEE Trans. Power Electron.* **26**(12), 3766–3777.

Liang, J., T. Green, C. Feng, and G. Weiss: 2009, 'Increasing Voltage Utilization in Split-Link, Four-Wire Inverters'. *IEEE Trans. Power Electron.* **24**(6), 1562–1569.

Lin, B.-R. and T.-L. Hung: 2002, 'Single-phase half-bridge converter topology for power quality compensation'. *IEE Proceedings-Electric Power Applications* **149**(5), 351–359.

Liu, C. and J.-S. Lai: 2007, 'Low Frequency Current Ripple Reduction Technique With Active Control in a Fuel Cell Power System With Inverter Load'. *IEEE Trans. Power Electron.* **22**(4), 1429–1436.

Liu, W., K. Wang, H. Chung, and S. Chuang: 2015, 'Modeling and Design of Series Voltage Compensator for Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter'. *IEEE Trans. Power Electron.* **30**(5), 2534–2548.

Lo, Y.-K., C.-T. Ho, and J.-M. Wang: 2007, 'Elimination of the Output Voltage Imbalance in a Half-Bridge Boost Rectifier'. *IEEE Trans. Power Electron.* **22**(4), 1352–1360.

Lo, Y.-K., T.-H. Song, and H.-J. Chiu: 2002, 'Analysis and elimination of voltage imbalance between the split capacitors in half-bridge boost rectifiers'. *IEEE Trans. Ind. Electron.* **49**(5), 1175–1177.

Lopez, O., F. Freijedo, A. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy: 2010, 'Eliminating Ground Current in a Transformerless Photovoltaic Application'. *IEEE Trans. Energy Convers.* **25**(1), 140–147.

Ma, F., A. Luo, X. Xu, H. Xiao, C. Wu, and W. Wang: 2013, 'A Simplified Power Conditioner Based on Half-Bridge Converter for High-Speed Railway System'. *IEEE Trans. Ind. Electron.* **60**(2), 728–738.

Machado, R., S. Buso, and J. Pomilio: 2006, 'A Line-Interactive Single-Phase to Three-Phase Converter System'. *IEEE Trans. Power Electron.* **21**(6), 1628–1636.

Makdessi, M., A. Sari, P. Venet, P. Bevilacqua, and C. Joubert: 2015, 'Accelerated Ageing of Metallized Film Capacitors Under High Ripple Currents Combined With a DC Voltage'. *IEEE Trans. Power Electron.* **30**(5), 2435–2444.

Meneses, D., F. Blaabjerg, O. García, and J. A. Cobos: 2013, 'Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application'. *IEEE Trans. Power Electron.* **28**(6), 2649–2663.

Ming, W.-L. and Q.-C. Zhong: 2013, 'Single-phase voltage-doubler with mismatched capacitors for balanced output voltages and reduced DC-bus voltage ripples'. In: *IEEE Energy Conversion Congress and Exposition (ECCE)*. pp. 4830–4836.

Ming, W.-L. and Q.-C. Zhong: 2014, 'Single-phase half-bridge rectifiers with extended voltage ranges and reduced voltage ripples'. In: *Power Electronics for Distributed Generation Systems (PEDG), 2014 IEEE 5th International Symposium on*. pp. 1–6.

Ming, W.-L. and Q.-C. Zhong: 2015, 'A Single-Phase Rectifier Having Two Independent Voltage Outputs With Reduced Fundamental Frequency Voltage Ripples'. *IEEE Trans. Power Electron.* **30**(7), 3662–3673.

Ming, W.-L., Q.-C. Zhong, and X. Zhang: 2016, 'A Single-Phase Four-Switch Rectifier With Significantly Reduced Capacitance'. *IEEE Trans. Power Electron.* **31**(2), 1618–1632.

Mohan, N.: 2003, *Power electronics: converters, applications, and design*. Hoboken, NJ : John Wiley and Sons.

Mollov, S.: 2011, 'A simple adaptive control for a novel voltage bus conditioner with reduced capacitive storage'. In: *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*. Birmingham, UK, pp. 1–10.

Ogasawara, S., H. Ayano, and H. Akagi: 1998, 'An active circuit for cancellation of common-mode voltage generated by a PWM inverter'. *IEEE Trans. Power Electron.* **13**(5), 835–841.

Omron: 2013, 'PID-preventive transformerless PV inverter'. Technical report, Omron Corporation. http://industrial.omron.co.za/en/solutions/green-automation/pid-causes-70-power-reduction.

Picard, J., 'High-voltage energy storage: the key to efficient hold-dup'. Technical report, Texas Instruments. Available at http://focus.ti.com/download/trng/docs/seminar/Topic_5_Picard.pdf.

Pini, S. H. and I. Barbi: 2011, 'A Single-Phase High-Power-Factor Rectifier, Based on a Two-Quadrant Shunt Active Filter'. *IEEE Trans. Power Electron.* **26**(11), 3131–3143.

Qin, H. and J. Kimball: 2012, 'Generalized Average Modeling of Dual Active Bridge DC–DC Converter'. *IEEE Trans. Power Electron.* **27**(4), 2078–2084.

Qin, H. and J. Kimball: 2014, 'Closed-Loop Control of DC–DC Dual-Active-Bridge Converters Driving Single-Phase Inverters'. *IEEE Trans. Power Electron.* **29**(2), 1006–1017.

Rodriguez, P., J. Pou, J. Bergas, J. Candela, R. Burgos, and D. Boroyevich: 2007, 'Decoupled Double Synchronous Reference Frame PLL for Power Converters Control'. *IEEE Trans. Power Electron.* **22**(2), 584–592.

Salcone, M. and J. Bond: 2009, 'Selecting film bus link capacitors for high performance inverter applications'. In: *Electric Machines and Drives Conference, 2009. IEMDC '09. IEEE International*. pp. 1692–1699.

Salmon, J. C.: 1993, 'Circuit topologies for single-phase voltage-doubler boost rectifiers'. *IEEE Trans. Power Electron.* **8**(4), 521–529.

Serban, I.: to be published, 'Power Decoupling Method for Single-Phase H-bridge Inverters with no Additional Power Electronics'. *IEEE Trans. Ind. Electron.* Early Access.

Shen, G., X. Zhu, J. Zhang, and D. Xu: 2010, 'A New Feedback Method for PR Current Control of LCL-Filter-Based Grid-Connected Inverter'. *IEEE Trans. Ind. Electron.* **57**(6), 2033–2041.

Singh, B. and S. Singh: 2010, 'Single-phase power factor controller topologies for permanent magnet brushless DC motor drives'. *IET Proc. Power Electron.* **3**(2), 147–175.

Soares de Freitas, I., C. Jacobina, and E. dos Santos: 2010, 'Single-Phase to Single-Phase Full-Bridge Converter Operating With Reduced AC Power in the DC-Link Capacitor'. *IEEE Trans. Power Electron.* **25**(2), 272–279.

Sreeraj, E., E. Prejith, K. Chatterjee, and S. Bandyopadhyay: 2014, 'An Active Harmonic Filter Based on One-Cycle Control'. *IEEE Trans. Ind. Electron.* **61**(8), 3799–3809.

Srikanthan, S. and M. Mishra: 2010, 'DC Capacitor Voltage Equalization in Neutral Clamped Inverters for DSTATCOM Application'. *IEEE Trans. Ind. Electron.* **57**(8), 2768–2775.

Srinivasan, R. and R. Oruganti: 1998, 'A unity power factor converter using half-bridge boost topology'. *IEEE Trans. Power Electron.* **13**(3), 487–500.

Stevens, J., J. Shaffer, and J. Vandenham: 2002, 'The service life of large aluminum electrolytic capacitors: effects of construction and application'. *IEEE Trans. Ind. Appl.* **38**(5), 1441–1446.

Tang, Y., Z. Qin, F. Blaabjerg, and P. C. Loh: 2015, 'A Dual Voltage Control Strategy for Single-Phase PWM Converters With Power Decoupling Function'. *IEEE Trans. Power Electron.* **30**(12), 7060–7071.

Tilli, A. and A. Tonielli: 1998, 'Sequential design of hysteresis current controller for three-phase inverter'. *IEEE Trans. Ind. Electron.* **45**(5), 771–781.

Tymerski, R., V. Vorperian, F. Lee, and W. Baumann: 1989, 'Nonlinear modeling of the PWM switch'. *IEEE Trans. Power Electron.* **4**(2), 225–233.

Venet, P., A. Lahyani, G. Grellet, and A. Ah-Jaco: 1999, 'Influence of aging on electrolytic capacitors function in static converters: Fault prediction method'. *The European Physical Journal Applied Physics* **5**(01), 71–83.

Von Jouanne, A., H. Zhang, and A. Wallace: 1998, 'An evaluation of mitigation techniques for bearing currents, EMI and overvoltages in ASD applications'. *IEEE Trans. Ind. Appl.* **34**(5), 1113–1122.

Wai, R.-J. and C.-Y. Lin: 2010, 'Active Low-Frequency Ripple Control for Clean-Energy Power-Conditioning Mechanism'. *IEEE Trans. Ind. Electron.* **57**(11), 3780–3792.

Wai, R.-J. and C.-Y. Lin: 2011, 'Dual Active Low-Frequency Ripple Control for Clean-Energy Power-Conditioning Mechanism'. *IEEE Trans. Ind. Electron.* **58**(11), 5172–5185.

Wang, B., X. Ruan, K. Yao, and M. Xu: 2010, 'A Method of Reducing the Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers'. *IEEE Trans. Power Electron.* **25**(3), 592–601.

Wang, H. and F. Blaabjerg: 2014, 'Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview'. *IEEE Trans. Ind. Appl.* **50**(5), 3569–3578.

Wang, H., H.-H. Chung, and W. Liu: 2014, 'Use of a Series Voltage Compensator for Reduction of the DC-Link Capacitance in a Capacitor-Supported System'. *IEEE Trans. Power Electron.* **29**(3), 1163–1175.

Wang, H., M. Liserre, and F. Blaabjerg: 2013, 'Toward Reliable Power Electronics: Challenges, Design Tools, and Opportunities'. *IEEE Ind. Electron. Mag.* **7**(2), 17–26.

Wang, R., F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara: 2011, 'A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage'. *IEEE Trans. Power Electron.* **26**(5), 1430–1443.

Wang, S., X. Ruan, K. Yao, S.-C. Tan, Y. Yang, and Z. Ye: 2012, 'A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver'. *IEEE Trans. Power Electron.* **27**(11), 4540–4548.

Weiss, G. and M. Hafele: 1999, 'Repetitive control of MIMO systems using H^∞ design'. *Automatica* **35**(7), 1185–1199.

Weiss, G., Q.-C. Zhong, T. Green, and J. Liang: 2004, 'H^∞ repetitive control of DC-AC converters in micro-grids'. *IEEE Trans. Power Electron.* **19**(1), 219–230.

Wen, H., W. Xiao, X. Wen, and P. Armstrong: 2012, 'Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems'. *IEEE Trans. Veh. Technol.* **61**(7), 2950–2964.

Wikipedia: 2014, 'Earthing system — Wikipedia, The Free Encyclopedia'.

Wiles, J. C.: 2012, 'Photovoltaic System Grounding'. Technical report, New Mexico State University. Available at http://www.solarabcs.org/about/publications/reports/systemgrounding/pdfs/SystemGrounding_studyreport.pdf.

Win, T. S., Y. Baba, E. Hiraki, T. Tanaka, and M. Okamoto: 2012, 'A half-bridge inverter based Active Power Quality Compensator using a constant DC capacitor voltage control for electrified railways'. In: *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, Vol. 1. pp. 314–320.

Wolfgang, E.: 2007, 'Examples for failures in power electronics systems'. In: *ECPE Tutorial on Reliability of Power Electronic Systems*.

Xiao, H., X. Liu, and K. Lan: 2014, 'Zero-Voltage-Transition Full-Bridge Topologies for Transformerless Photovoltaic Grid-Connected Inverter'. *IEEE Trans. Ind. Electron.* **61**(10), 5393–5401.

Xiao, H. and S. Xie: 2012, 'Transformerless Split-Inductor Neutral Point Clamped Three-Level PV Grid-Connected Inverter'. *IEEE Trans. Power Electron.* **27**(4), 1799–1808.

Yang, B., W. Li, Y. Gu, W. Cui, and X. He: 2012, 'Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System'. *IEEE Trans. Power Electron.* **27**(2), 752–762.

Yao, K., X. Ruan, X. Mao, and Z. Ye: 2011, 'Variable-Duty-Cycle Control to Achieve High Input Power Factor for DCM Boost PFC Converter'. *IEEE Trans. Ind. Electron.* **58**(5), 1856–1865.

Yao, K., X. Ruan, X. Mao, and Z. Ye: 2012, 'Reducing Storage Capacitor of a DCM Boost PFC Converter'. *IEEE Trans. Power Electron.* **27**(1), 151–160.

Zhang, C., D. Jiang, H. Zheng, and L. Ye: 2013a, 'A Bi-Directional Buck/Boost Voltage Balancer for DC Distribution System'. In: *Digital Manufacturing and Automation (ICDMA), 2013 Fourth International Conference on*. pp. 9–13.

Zhang, L., X. Ren, and X. Ruan: 2014, 'A Bandpass Filter Incorporated Into the Inductor Current Feedback Path for Improving Dynamic Performance of the Front-End DC-DC Converter in Two-Stage Inverter'. *IEEE Trans. Ind. Electron.* **61**(5), 2316–2325.

Zhang, X. and C. Gong: 2013, 'Dual-Buck Half-Bridge Voltage Balancer'. *IEEE Trans. Ind. Electron.* **60**(8), 3157–3164.

Zhang, X., X. Ruan, H. Kim, and C. K. Tse: 2013b, 'Adaptive Active Capacitor Converter for Improving Stability of Cascaded DC Power Supply System'. *IEEE Trans. Power Electron.* **28**(4), 1807–1816.

Zhao, K., P. Ciufo, and S. Perera: 2013, 'Rectifier Capacitor Filter Stress Analysis When Subject to Regular Voltage Fluctuations'. *IEEE Trans. Power Electron.* **28**(7), 3627–3635.

Zhong, Q.-C.: 2013a, 'Harmonic Droop Controller to Reduce the Voltage Harmonics of Inverters'. *IEEE Trans. Ind. Electron.* **60**(3), 936–945.

Zhong, Q.-C.: 2013b, 'Robust droop controller for accurate proportional load sharing among inverters operated in parallel'. *IEEE Trans. Ind. Electron.* **60**(4), 1281–1290.

Zhong, Q.-C., F. Blaabjerg, J. Guerrero, and T. Hornik: 2011, 'Reduction of voltage harmonics for parallel-operated inverters'. In: *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE)*. pp. 473–478.

Zhong, Q.-C., F. Blaabjerg, J. Guerrero, and T. Hornik: 2012a, 'Improving the Voltage Quality of an Inverter via Bypassing the Harmonic Current Components'. In: *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE)*. Raleigh, North Carolina.

Zhong, Q.-C., T. Green, J. Liang, and G. Weiss: 2002, 'H^∞ control of the neutral leg for 3–phase 4–wire DC-AC converters'. In: *Proc. of the 28th Annual IEEE Conference of Industrial Electronics (IECON)*.

Zhong, Q.-C., L. Hobson, and M. Jayne: 2005, 'Generating a neutral point for 3-phase 4-wire DC-AC converters'. In: *Proc. of IEEE Compatibility in Power Electronics (CPE)*. pp. 126–133.

Zhong, Q.-C. and T. Hornik: 2013a, 'Cascaded Current-Voltage Control to Improve the Power Quality for a Grid-connected Inverter with a Local Load'. *IEEE Trans. Ind. Electron.* **60**(4), 1344–1355.

Zhong, Q.-C. and T. Hornik: 2013b, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Wiley-IEEE Press.

Zhong, Q.-C., J. Liang, G. Weiss, C. Feng, and T. Green: 2006, 'H^∞ control of the neutral point in 4–wire 3–phase DC-AC converters'. *IEEE Trans. Ind. Electron.* **53**(5), 1594–1602.

Zhong, Q.-C., W.-L. Ming, X. Cao, and M. Krstic: 2012b, 'Reduction of DC-bus voltage ripples and capacitors for single-phase PWM-controlled rectifiers'. In: *Proc. IECON 2012 - 38th Annual Conf. IEEE Industrial Electronics Society*. pp. 708–713.

Zhong, Q.-C., P.-L. Nguyen, Z. Ma, and W. Sheng: 2014, 'Self-synchronised Synchronverters: Inverters without a Dedicated Synchronisation Unit'. *IEEE Trans. Power Electron.* **29**(2), 617–630.

Zhong, Q.-C. and G. Weiss: 2011a, 'Synchronverters: Inverters That Mimic Synchronous Generators'. *IEEE Trans. Ind. Electron.* **58**(4), 1259–1267.

Zhong, Q.-C. and G. Weiss: 2011b, 'Synchronverters: Inverters that mimic synchronous generators'. *IEEE Trans. Ind. Electron.* **58**(4), 1259–1267.

Zhu, G., X. Ruan, L. Zhang, and X. Wang: to be published, 'On the Reduction of Second Harmonic Current and Improvement of Dynamic Response for Two-Stage Single-Phase Inverter'. *IEEE Trans. Power Electron.*

Zhu, G., S. Tan, Y. Chen, and C. Tse: 2013, 'Mitigation of Low-Frequency Current Ripple in Fuel-Cell Inverter Systems Through Waveform Control'. *IEEE Trans. Power Electron.* **28**(2), 779–792.

Zhu, X., X. Li, G. Shen, and D. Xu: 2010, 'Design of the Dynamic Power Compensation for PEMFC Distributed Power System'. *IEEE Trans. Ind. Electron.* **57**(6), 1935–1944.

Ziarani, A. K. and A. Konrad: 2004, 'A Method of Extraction of Nonstationary Sinusoids'. *Signal Processing* **84**(8), 1323–1346.