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Gupta, Swati and Hannah, Stuart and Gleskova, Helena (2014) Correlation between the structure of the dielectric monolayer and the performance of low-voltage transistors based on pentacene. In: Organics, Photonics and Electronics: Faraday Discussion 174, 2014-09-08 - 2014-09-10, University of Strathclyde. , http://dx.doi.org/10.1039/C4FD90074J

CORRELATION BETWEEN THE STRUCTURE OF THE DIELECTRIC MONOLAYER AND THE PERFORMANCE OF LOW-VOLTAGE TRANSISTORS BASED ON PENTACENE

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➢ INTRODUCTION

Alkyl phosphonic acids (C_nPA) are becoming a material of choice for passivation of high-k oxides in organic thin-film transistors with ultra-thin gate dielectrics. A monolayer of phosphonic acid inserted between the inorganic oxide and the organic semiconductor provides two main benefits: (i) the density of the charge carrier traps associated with the surface –OH groups of the oxide is reduced because these groups act as binding sites for the organic molecules; and (ii) the low surface energy of the organic monolayer may reduce the density of defects in the subsequently deposited conjugated polymer.

To date such monolayers have been assembled from solutions only. We have recently developed a vapour-phase self-assembly of n-octylphosphonic acid (C_8PA) monolayer in vacuum that leads to a well chemisorbed monolayer of C_8PA. When such a monolayer is attached to ~ 9-nm thick aluminium oxide to form an ultra-thin dielectric implemented in low-voltage organic thin-film transistors based on pentacene, the transistor performance exhibits measurable changes upon alteration of the structure of the C_8PA monolayer.

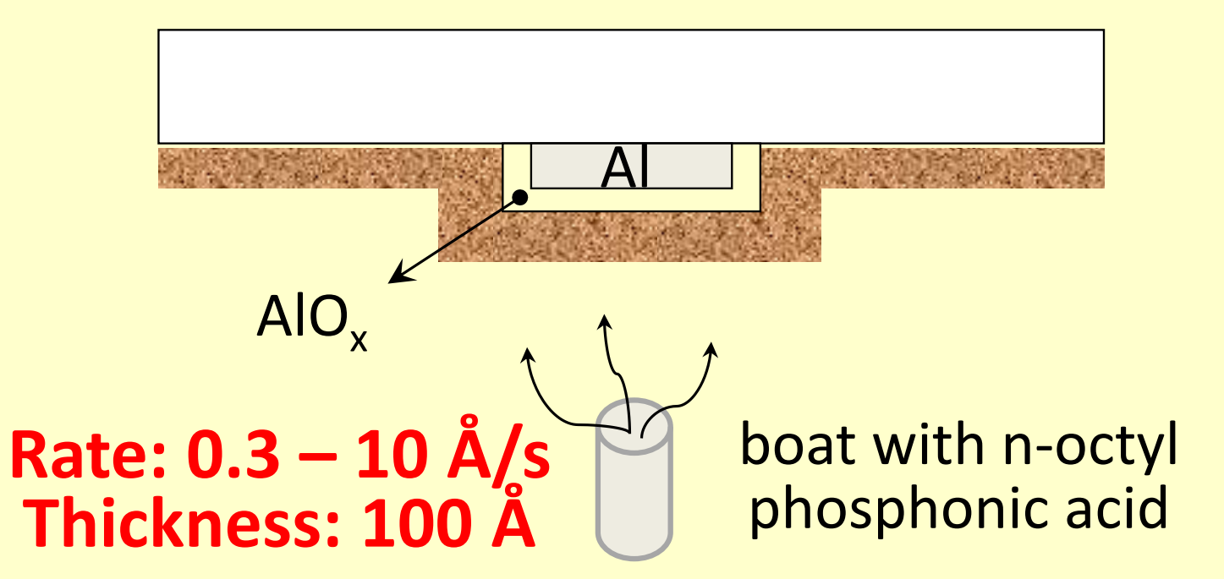
➢ AIM

- Seek correlation between the structure of the dielectric and the short- and long-term performance of organic thin-film transistors
- Optimize the vapour-phase self-assembly of n-octylphosphonic acid monolayer

➢ EXPERIMENTAL DETAILS

N-octylphosphonic acid growth

Substrate temperature:
25 – 150°C



Rate: 0.3 – 10 Å/s
Thickness: 100 Å

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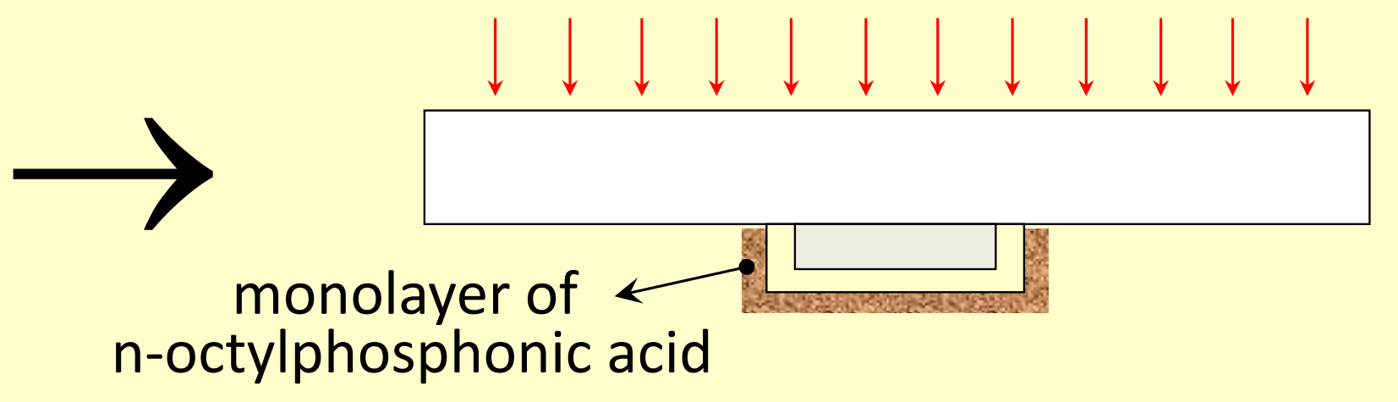
Monolayer formation

Anneal: 160°C, 25 – 210 min



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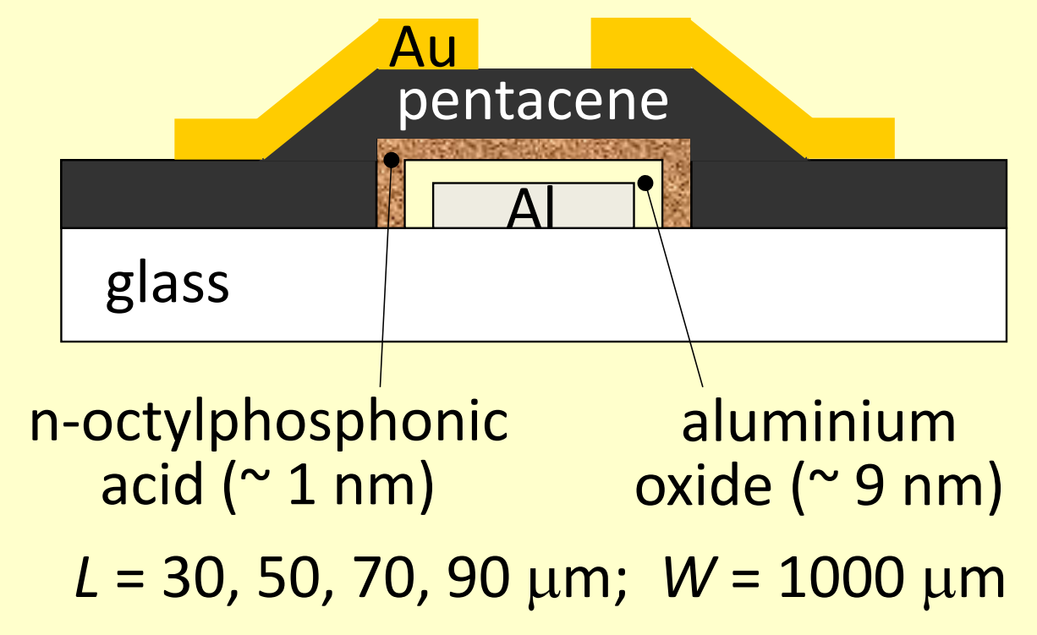
Transistor cross-section



L = 30, 50, 70, 90 µm; W = 1000 µm

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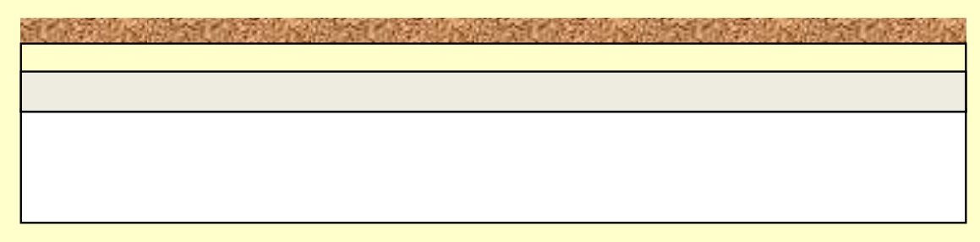
Samples for FTIR, AFM and WCA



FTIR – Fourier Transform Infrared Spectroscopy
AFM – Atomic Force Microscopy
WCA – Water Contact Angle Measurement

- Fully dry fabrication process
- AlO_x is prepared by UV/ozone oxidation of aluminium
- All other layers are thermally evaporated in Minispectros vacuum system (K.J. Lesker)

➢ BIAS STRESS

Performed on 3 sets of transistors with altered C_8PA monolayer preparation:

a) C_8PA deposited at 25°C at 3 Å/s and annealed at 160°C for 25 – 210 minutes (**Post-growth anneal series**)
 - 50-nm-thick pentacene deposited at 25°C at 0.24 Å/s, 50-nm-thick Au deposited at 3 Å/s

b) C_8PA deposited at 25 – 150°C at 3 Å/s and annealed at 160°C for 180 minutes (**Growth temperature series**)
 - 50-nm-thick pentacene deposited at 70°C at 0.24 Å/s, , 50-nm-thick Au deposited at 3 Å/s

c) C_8PA deposited at 25°C at 0.3 – 10 Å/s and annealed at 160°C for 180 minutes (**Growth rate series**)
 - 50-nm-thick pentacene deposited at 55°C at 0.24 Å/s, , 50-nm-thick Au deposited at 3 Å/s

- All transistors were bias-stressed up to 5000 seconds with $V_{gs} = V_{ds} = -3$ V and the source electrode grounded
- Transfer characteristics measured at certain intervals to determine V_t, S, μ, and I_d
- Time constant τ and stretching parameter β determined for each of ΔV_t, ΔS, $\mu/\mu(t{=}0)$, and $I_d/I_d(t{=}0)$

$$\Delta V_t = |V_t(t) - V_t(0)| = |V_t(\infty) - V_t(0)| . \left[1 - e^{-(t/\tau_{Vt})^{\beta_{Vt}}}\right]$$

$$\Delta S(t) = S(t) - S(0) = \left(S(\infty) - S(0)\right) . \left[1 - e^{-(t/\tau_S)^{\beta_S}}\right]$$

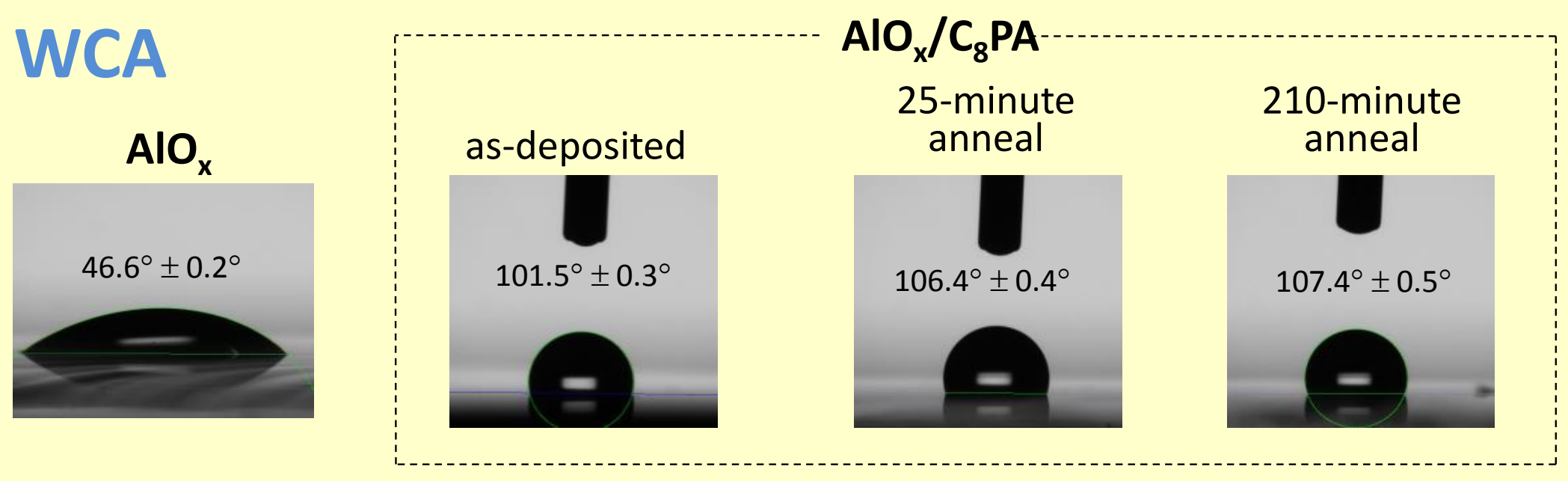
$$\frac{\mu(t)}{\mu(0)} = \frac{\mu(\infty)}{\mu(0)} + \left[1 - \frac{\mu(\infty)}{\mu(0)}\right] . e^{-(t/\tau_\mu)^{\beta_\mu}}$$

$$\frac{I_d(t)}{I_d(0)} = \frac{I_d(\infty)}{I_d(0)} + \left[1 - \frac{I_d(\infty)}{I_d(0)}\right] . e^{-(t/\tau_{Id})^{\beta_{Id}}}$$

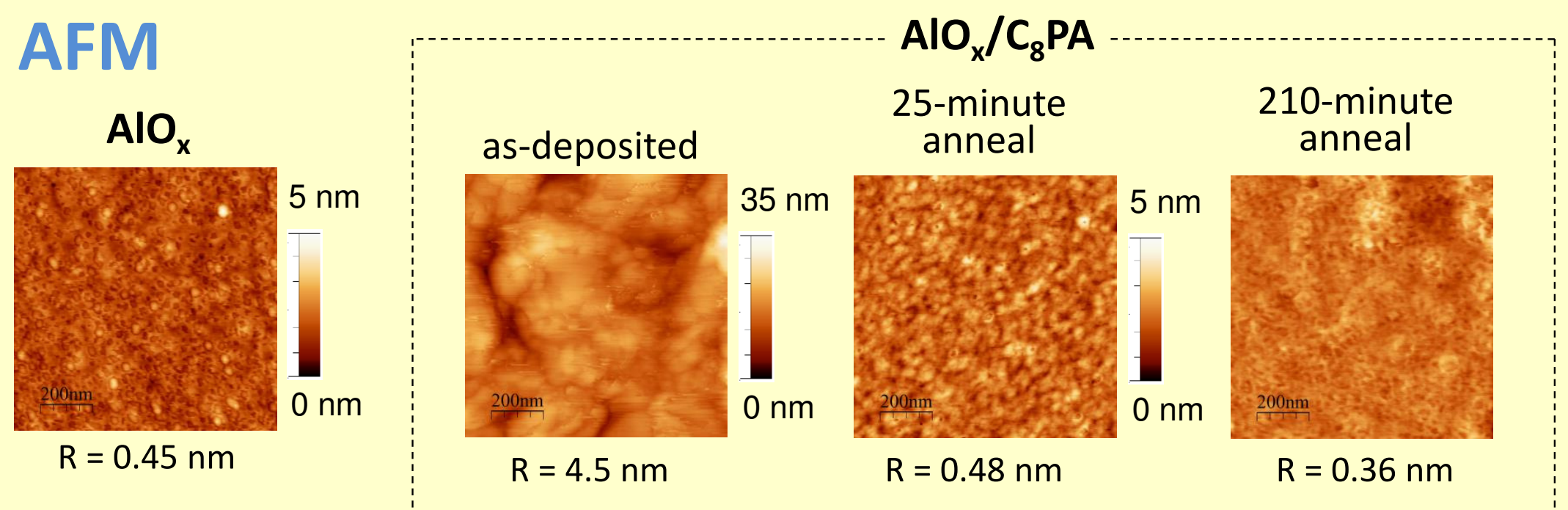
➢ RESULTS

POST-GROWTH ANNEAL SERIES

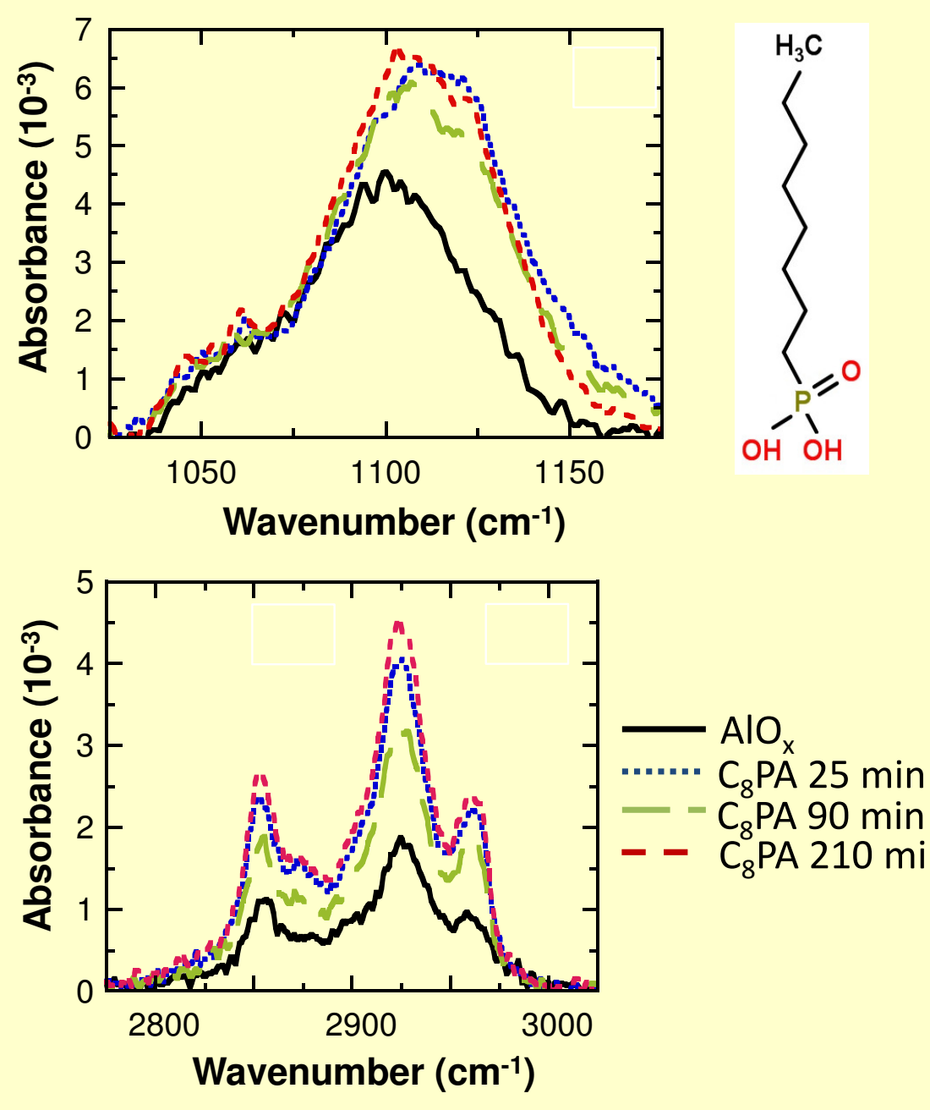
WCA



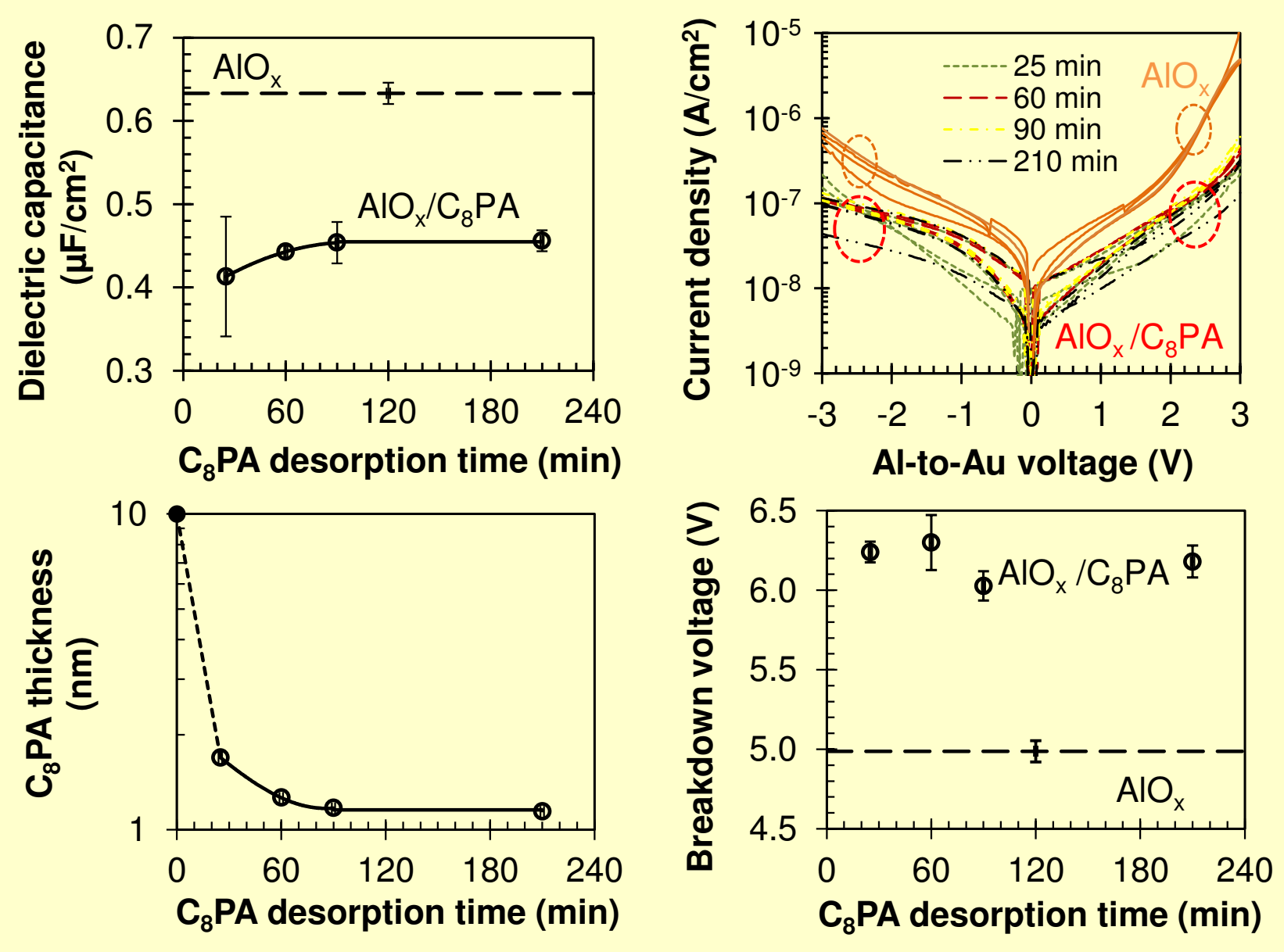
AFM



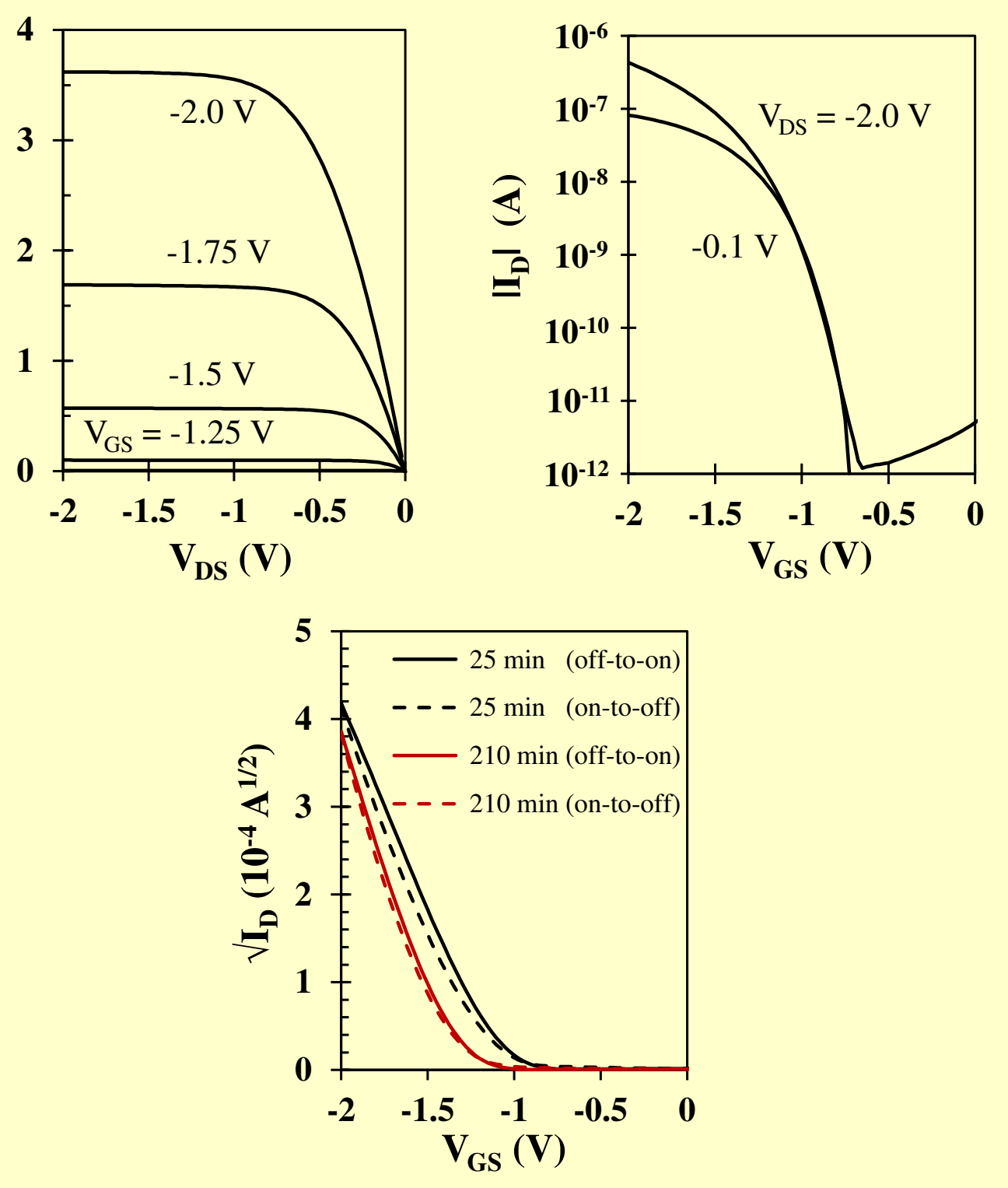
FTIR



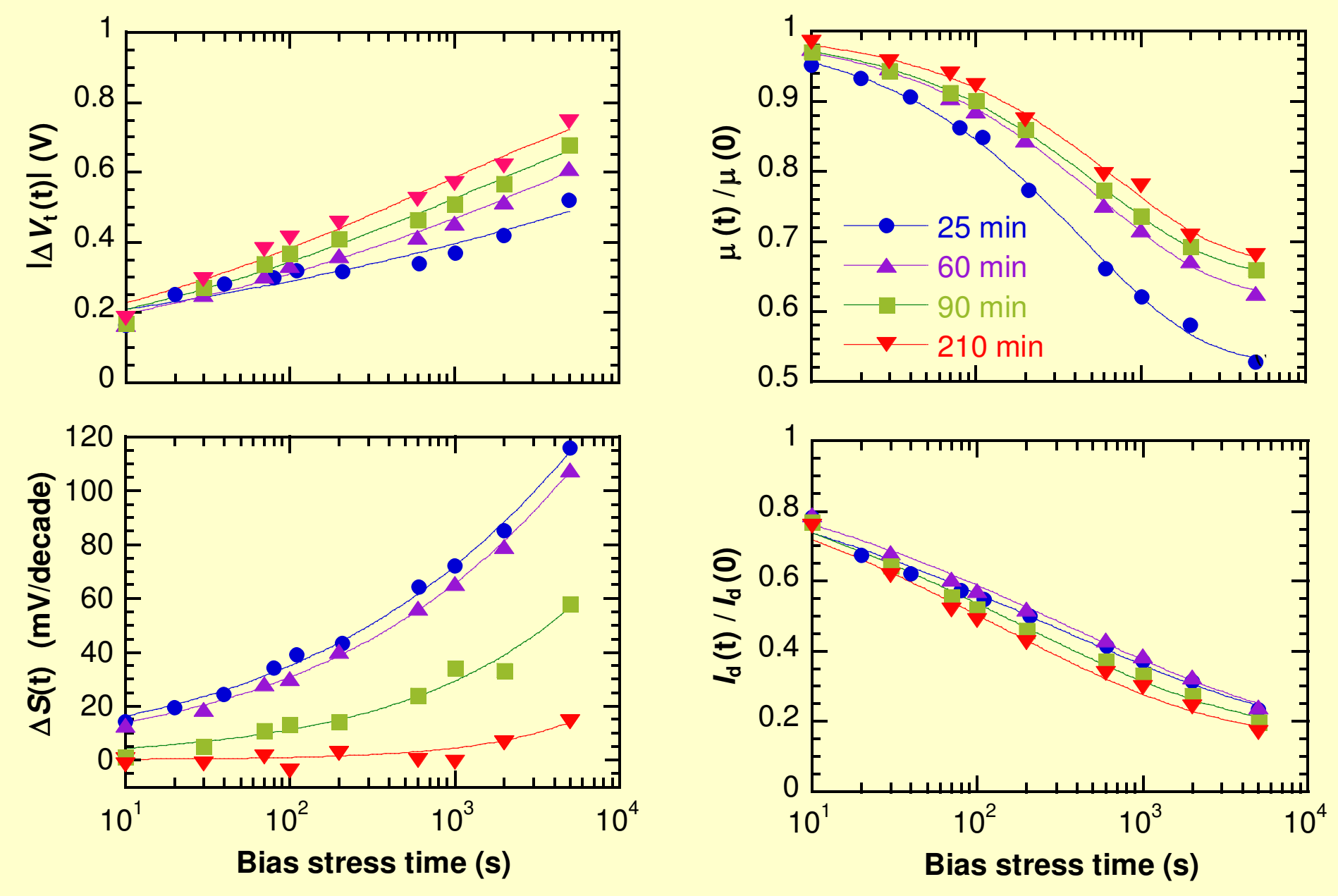
GATE DIELECTRIC PROPERTIES



AS-FABRICATED TRANSISTORS



BIAS STRESS



C_8PA annealing time (min)	τ_{Vt} (s)	β_{Vt}	τ_S (s)	β_S	τ_μ (s)	β_μ	τ_{Id} (s)	β_{Id}
25	3.3×10^6	0.15	4.0×10^4	0.35	4.5×10^2	0.61	3.0×10^2	0.29
60	8.8×10^3	0.23	7.0×10^4	0.36	5.7×10^2	0.61	3.7×10^2	0.30
90	1.6×10^3	0.26	5.3×10^6	0.42	5.7×10^2	0.61	1.8×10^2	0.33
210	7.5×10^2	0.28	3.7×10^{10}	0.72	7.0×10^2	0.65	1.4×10^2	0.34

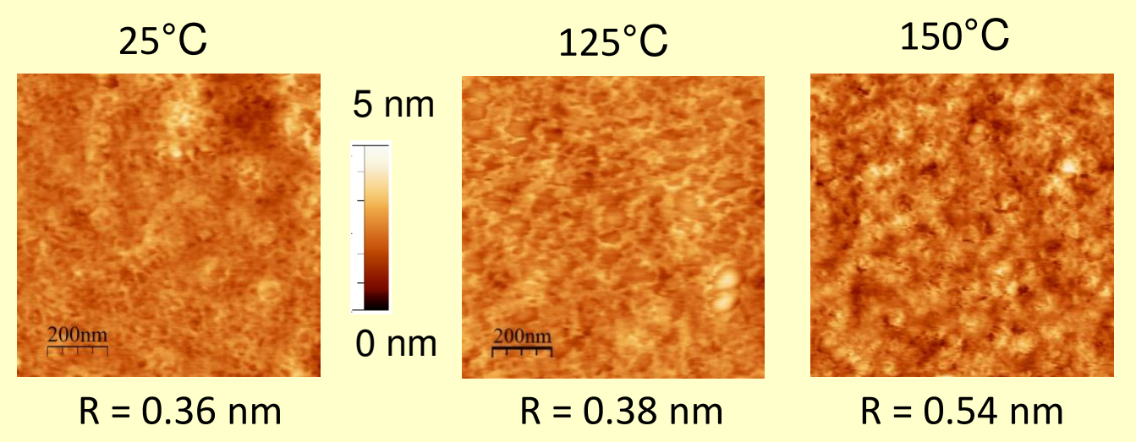
- Long post-growth anneal leads to the lowest surface roughness, highest water contact angle and best molecular ordering of C_8PA monolayer.
- Properties are similar to C_8PA monolayers assembled from solution.
- Long post-growth C_8PA anneal also leads to the highest stretching factors for the threshold voltage and subthreshold slope.

GROWTH TEMPERATURE SERIES

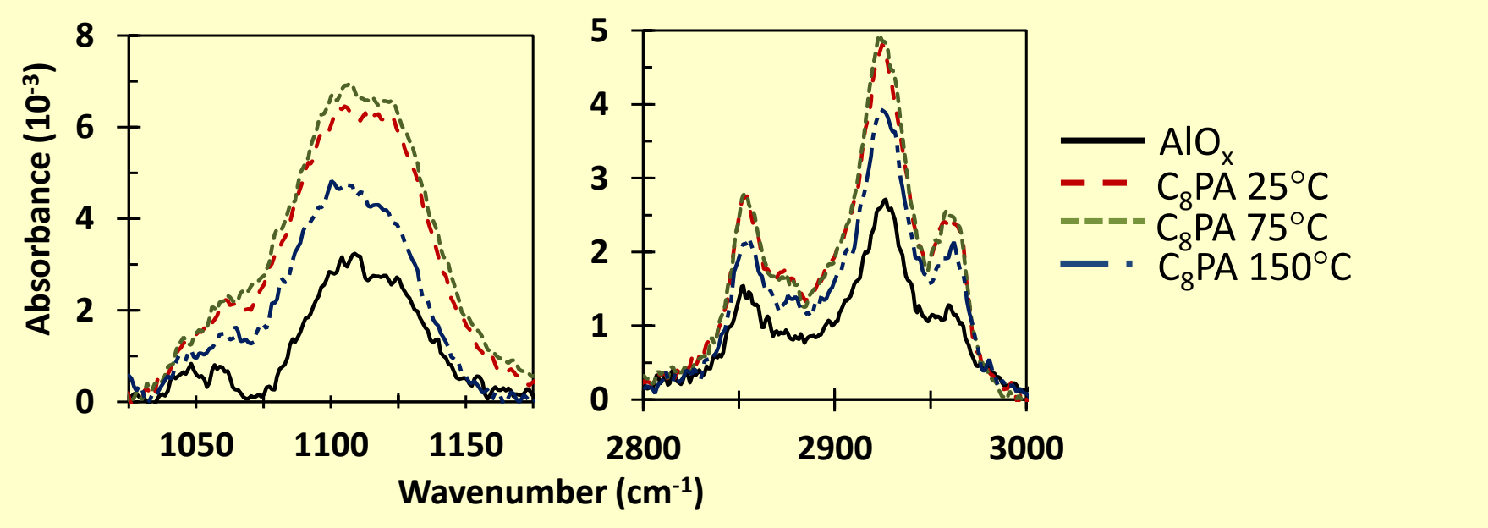
WCA

Growth T (°C)	WCA (°)
25	113.5 ± 1.4
75	112.1 ± 1.4
125	111.1 ± 0.7
150	107.9 ± 0.8

AFM



FTIR



BIAS STRESS

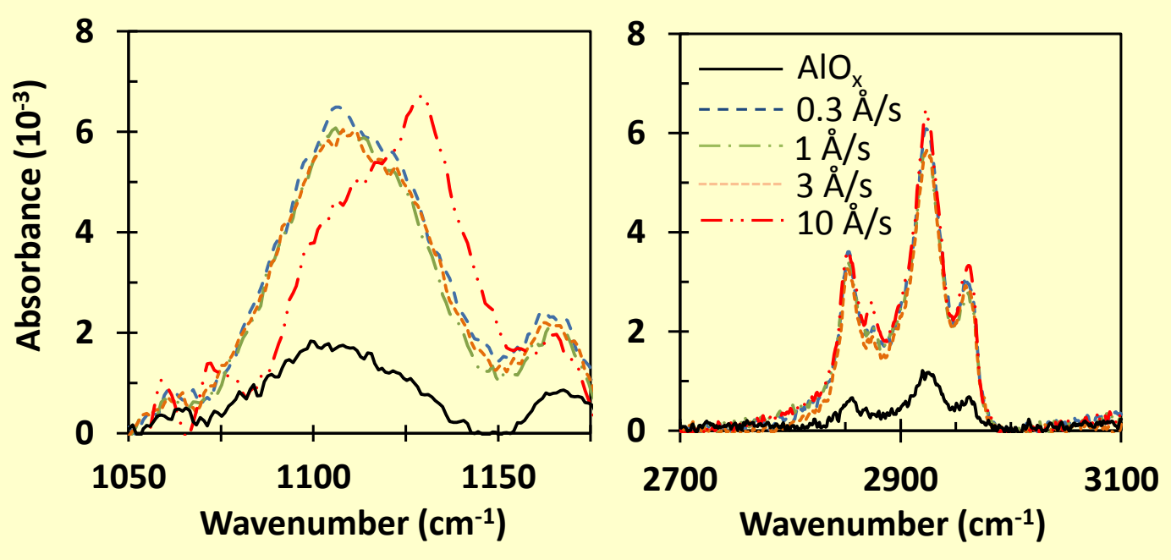
C_8PA growth T (°C)	τ_{Vt} (s)	β_{Vt}	τ_S (s)	β_S	τ_μ (s)	β_μ	τ_{Id} (s)	β_{Id}
25	2.6×10^2	0.30	9.5×10^{10}	0.70	3.6×10^2	0.65	2.2×10^2	0.34
75	6.7×10^2	0.27	1.1×10^4	0.60	3.8×10^2	0.53	2.2×10^2	0.35
125	6.9×10^2	0.25	1.7×10^4	0.59	5.6×10^2	0.53	2.6×10^2	0.37
150	2.9×10^3	0.25	5.0×10^3	0.51	5.7×10^2	0.50	2.6×10^2	0.38

GROWTH RATE SERIES

WCA

Rate (Å/s)	WCA (°)
0.3	111.5 ± 0.3
1	112.1 ± 0.5
3	109.3 ± 0.6
10	109.9 ± 1.3

FTIR



BIAS STRESS

C_8PA growth rate (Å/s)	τ_{Vt} (s)	β_{Vt}	τ_S (s)	β_S	τ_μ (s)	β_μ	τ_{Id} (s)	β_{Id}
0.3	5.4×10^2	0.35	7.5×10^2	0.58	1.6×10^3	0.62	2.4×10^2	0.38
1	5.8×10^2	0.37	9.2×10^2	0.60	1.0×10^3	0.63	2.8×10^2	0.44
3	7.0×10^2	0.37	1.4×10^3	0.60	1.1×10^3	0.63	4.6×10^2	0.44
10	5.4×10^2	0.35	1.5×10^3	0.59	1.3×10^3	0.70	3.2×10^2	0.39

➢ CONCLUSIONS

- Correlation between monolayer structure and long-term transistor stability was uncovered.
- C_8PA annealing has the largest effect on the bias-induced transistor degradation, then the growth temperature and finally the evaporation rate.
- The best C_8PA properties were obtained at 25°C, 1-3 Å/s and 210-minute anneal. This correlates with improved transistor performance.
- These conditions lead to highest values of β for V_t and S indicating narrower distribution of carrier traps.
- Pentacene growth also has a minor effect on the values of β and τ.

➢ ACKNOWLEDGEMENTS

We would like to thank the School of Engineering of University of Glasgow for transistor fabrication support, P. Šutta from New Technology Research Centre of University of West Bohemia for FTIR measurements, and D. Lamprou from Strathclyde Institute for Pharmacy and Biological Sciences, University of Strathclyde, for WCA measurements. In addition, our thanks go to R. Ulijn from Pure and Applied Chemistry, University of Strathclyde, for access to an AFM.

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