COMPARISON OF 2 V ORGANIC THIN-FILM TRANSISTORS FABRICATED ON FREE-STANDING COMMERCIAL PEN FOILS

Stuart Hannah and Helena Gleskova

Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom
(stuart.hannah.2013@uni.strath.ac.uk)

➢ INTRODUCTION

Large-area, roll-to-roll (R2R) fabrication of thin-film circuits on plastic foils demands low-cost manufacturing and the integration of devices onto flexible plastic substrates. We have developed a fully dry process to fabricate low-voltage organic thin-film transistors (OTFTs) featuring a 10-nm-thick bi-layer dielectric based on aluminium oxide (AlO_x) and n-octylphosphonic acid (C_8PA) monolayer. Two commercially available polyethylene naphthalate (PEN) plastic foils were compared as possible flexible substrates for OTFTs. Teonex Q65FA features an adhesive layer on the bottom side to prevent film slippage during R2R processing, while Optfine PQA1 includes a planarisation layer on the top (device) side.

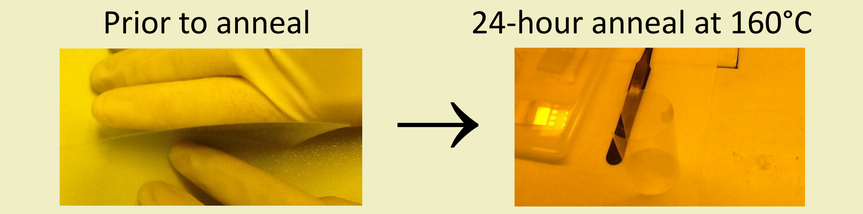
➢ AIMS

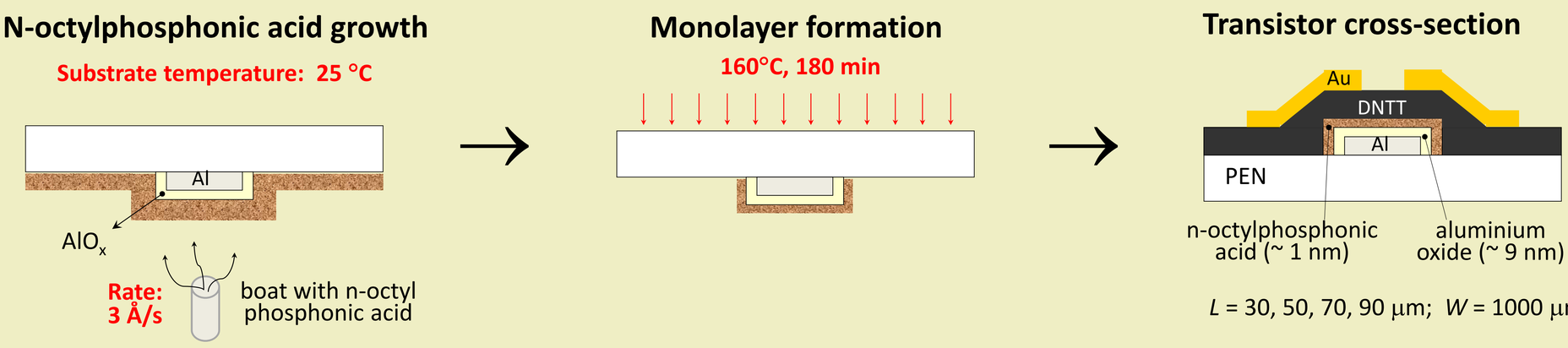
- Study the effect of annealing at 160°C on bare Teonex and Optfine PEN foils .
- Fabricate low-voltage OTFTs on both substrates.
- Compare Al/AlO_x/C_8PA/DNTT/Au and Al/AlO_x/DNTT/Au transistors and metal-insulator-metal (MIM) structures fabricated on each PEN foil.

➢ EXPERIMENT

- Teonex and Optfine PEN films were pre-annealed at 160°C for 24 hours prior to OTFT fabrication.
- Subsequently, Al/AlO_x/C_8PA/DNTT/Au and Al/AlO_x/DNTT/Au OTFTs were fabricated on non-annealed Optfine and pre-annealed Teonex foils.

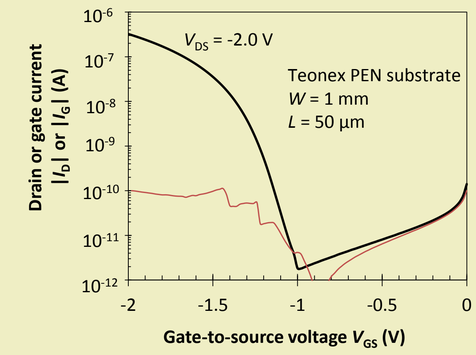
➢ ANNEAL: OPTFINE SUBSTRATE





L = 30, 50, 70, 90 μm; W = 1000 μm

- 15 nm of DNTT was deposited at room temperature at rates of 0.4 Å/s and 0.6 Å/s on Teonex and Optfine respectively.
- AlO_x prepared by UV/ozone oxidation of aluminium.
- All other layers are thermally evaporated in Minispectros vacuum system (K.J. Lesker).



Linear regime ($|V_{DS}| < |V_{GS}-V_t|$):

$$I_D = \mu C \frac{W}{L}(V_{GS} - V_t)V_{DS}$$

$$\mu_{lin} = \frac{\partial I_D}{\partial V_{GS}} \cdot \frac{1}{C V_{DS} \frac{W}{L}}$$

Saturation regime ($|V_{DS}| > |V_{GS}-V_t|$):

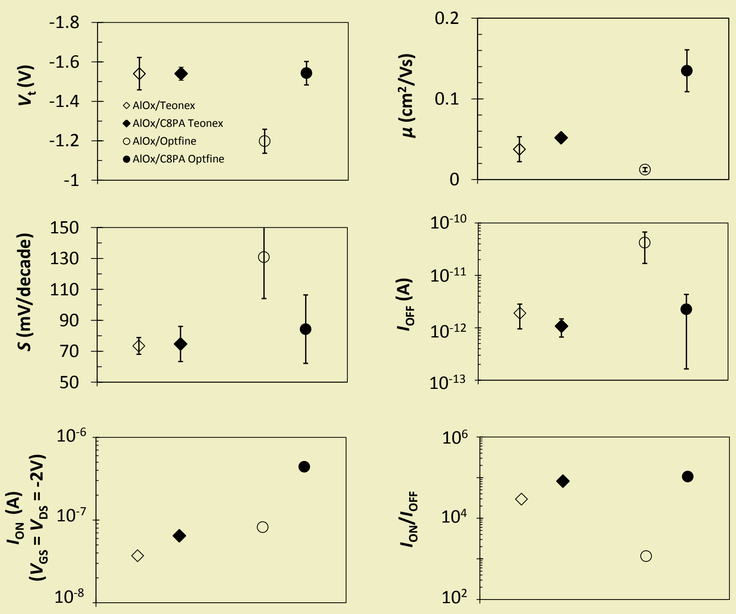
$$I_D = \mu C \frac{W}{2L}(V_{GS} - V_t)^2$$

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}}\right)^2 \cdot \frac{1}{C\frac{W}{2L}}$$

➢ RESULTS: GATE DIELECTRIC

	Teonex Q65FA		Optfine PQA1	
	AlO_x	AlO_x/C_8PA	AlO_x	AlO_x/C_8PA
Capacitance (μF/cm²)	0.74	0.66	0.86	0.43
Current @ -2 V (A/cm²)	4.42×10^{-7}	2.57×10^{-7}	2.32×10^{-7}	8.39×10^{-8}

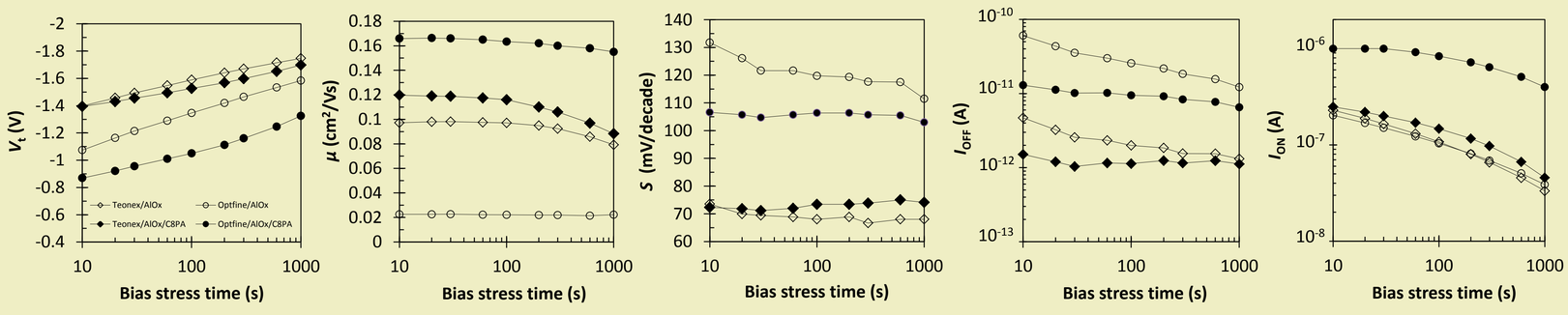
➢ RESULTS: TRANSISTORS



➢ RESULTS: BIAS STRESS

- Performed on 4 transistors: Teonex Q65FA – bare-AlO_x OTFT, Teonex Q65FA – AlO_x/C_8PA OTFT, Optfine PQA1 – bare-AlO_x OTFT, and Optfine PQA1 – AlO_x/C_8PA OTFT.
- Bias stress performed about 1 week after the initial measurements shown on the left were taken.
- Bias stress up to 1000 seconds with V_{GS} = −2 V, whilst grounding the source and drain electrodes.
- At certain intervals, transfer characteristics were measured to determine OTFT parameters including V_t, μ, S, I_{OFF} and I_{ON}.

	Teonex Q65FA				Optfine PQA1			
	AlO_x OTFT bias stress		AlO_x/C_8PA OTFT bias stress		AlO_x OTFT bias stress		AlO_x/C_8PA OTFT bias stress	
	0 s	1000 s	0 s	1000 s	0 s	1000 s	0 s	1000 s
V_t (V)	−1.20	−1.75	−1.27	−1.70	− 0.40	−1.58	− 0.72	−1.33
μ (cm²/Vs)	0.090	0.079	0.11	0.088	0.018	0.022	0.16	0.16
S (mV/dec)	85	68	78	74	166	111	112	103
$\lvert I_{OFF}\rvert$ (A)	1.4×10^{-11}	1.3×10^{-12}	1.8×10^{-12}	1.1×10^{-12}	2.8×10^{-10}	1.2×10^{-11}	1.7×10^{-11}	6.5×10^{-12}
$\lvert I_{ON}\rvert$ (A)	3.6×10^{-7}	3.3×10^{-8}	3.2×10^{-7}	4.6×10^{-8}	4.0×10^{-7}	3.9×10^{-8}	9.9×10^{-7}	4.0×10^{-7}



➢ CONCLUSIONS

- Teonex PEN is easier to handle, since it remained flat upon heating at 160°C.
- Optfine PEN curves significantly upon heating and presents a substantial challenge if used as a free-standing substrate with our OTFT fabrication procedure.
- Planarisation layer on Optfine PEN results in about a factor of three greater field-effect mobility for AlO_x/C_8PA OTFTs compared with Teonex PEN.
- OTFTs on Optfine PEN appear to remain more stable after application of bias stress in terms of mobility compared with OTFTs on Teonex PEN.

EPSRC Engineering and Physical Sciences Research Council

Stuart Hannah is a recipient of a DTG PhD Scholarship funded by Engineering and Physical Sciences Research Council (EPSRC).
He would like to thank the School of Engineering at the University of Glasgow for transistor fabrication support. Thanks is also given to Dupont Teijin for providing PEN substrates for this experiment.

University of Strathclyde Engineering