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# ALUMINIUM OXIDE PREPARED BY ATOMIC LAYER DEPOSITION IN ORGANIC THIN-FILM TRANSISTORS OPERATING AT 2 V: COMPARISON WITH UV-OZONE OXIDATION

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## INTRODUCTION

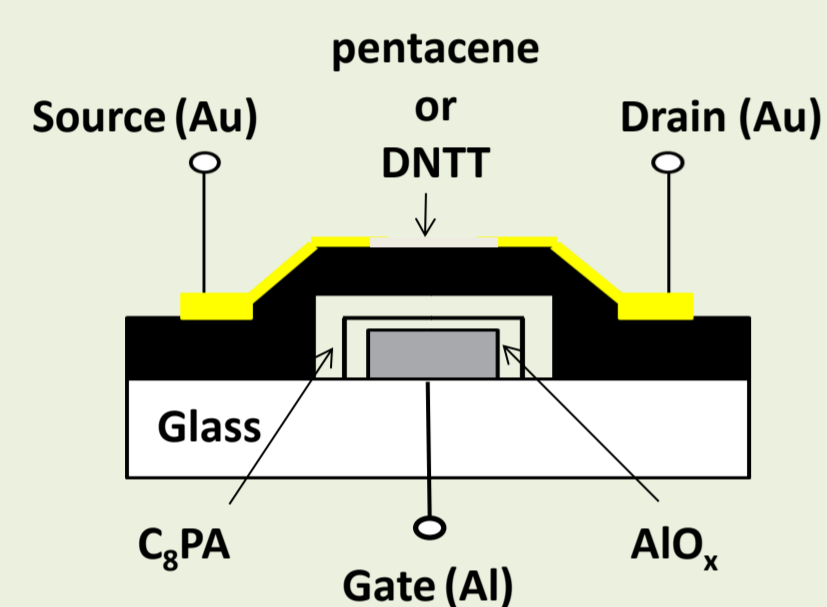
Large-area, roll-to-roll fabrication of thin-film circuits demands layer thickness uniformity over large areas. Previously, a 10-nm-thick dry bi-layer dielectric based on aluminium oxide ( $\text{AlO}_x$ ) prepared by UV-ozone oxidation and n-octylphosphonic acid ( $\text{C}_8\text{PA}$ ) monolayer prepared by vacuum evaporation has been developed for organic thin-film transistors (OTFTs) based on pentacene. Here we compare such OTFTs to similar transistors that incorporate ALD- $\text{AlO}_x/\text{C}_8\text{PA}$  bi-layer. In addition, a 12.9-nm-thick ALD- $\text{AlO}_x$  exposed to UV-ozone for 60 minutes was incorporated into OTFTs based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT).

## AIMS

- Use atomic layer deposition (ALD) to grow thin layers of  $\text{AlO}_x$  for low-voltage OTFTs.
- Compare Al/ALD- $\text{AlO}_x/\text{C}_8\text{PA}$ /pentacene/Au and Al/UV-ozone- $\text{AlO}_x/\text{C}_8\text{PA}$ /pentacene/Au transistors and metal-insulator-metal (MIM) structures.
- Fabricate Al/ALD- $\text{AlO}_x$ /DNTT/Au and Al/ALD- $\text{AlO}_x/\text{C}_8\text{PA}$ /DNTT/Au OTFTs and compare them with pentacene OTFTs.

## EXPERIMENT

- Two devices incorporated thin ALD- $\text{AlO}_x$  (12.9 nm) and two used thicker (36.8 nm) ALD- $\text{AlO}_x$ . ALD performed from  $\text{H}_2\text{O}$  and TMA at  $160^\circ\text{C}$ .
- Within each pairing, one sample underwent a 2-minute UV-ozone clean prior to  $\text{C}_8\text{PA}$  assembly and/or pentacene evaporation. All other transistor layers were identical to UV-ozone- $\text{AlO}_x$  (9 nm) OTFTs.  $W = 1000 \mu\text{m}$  and  $L = 30, 50, 70$  and  $90 \mu\text{m}$ .
- In the DNTT OTFTs the ALD- $\text{AlO}_x$  (12.9 nm) layer was exposed to UV-ozone for 60 minutes prior to  $\text{C}_8\text{PA}$  self-assembly. Source/drain and gate contacts are similar to pentacene transistors.



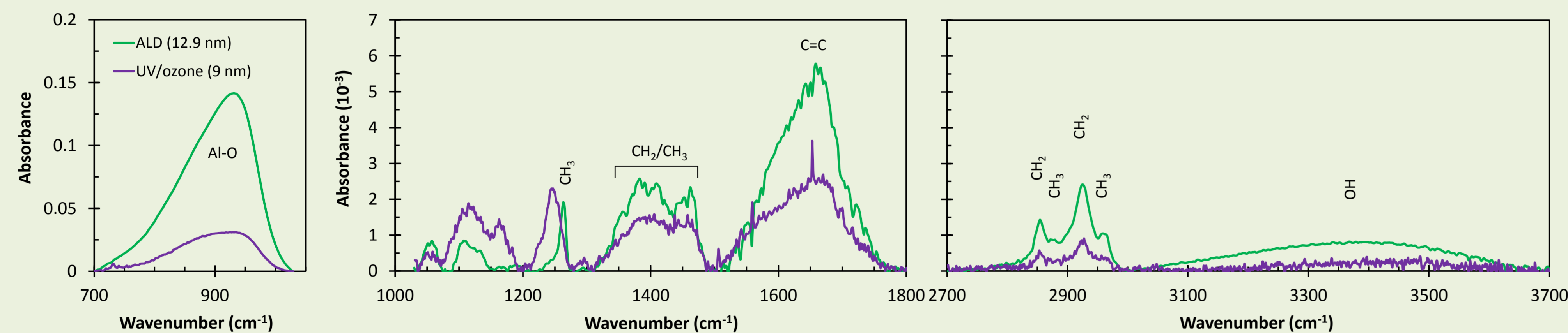
Linear regime ( $|V_{DS}| < |V_{GS} - V_t|$ ):

$$I_D = \mu C \frac{W}{L} (V_{GS} - V_t) V_{DS} \quad \mu_{lin} = \frac{\partial I_D}{\partial V_{GS}} \cdot \frac{1}{C V_{DS}} \cdot \frac{W}{L}$$

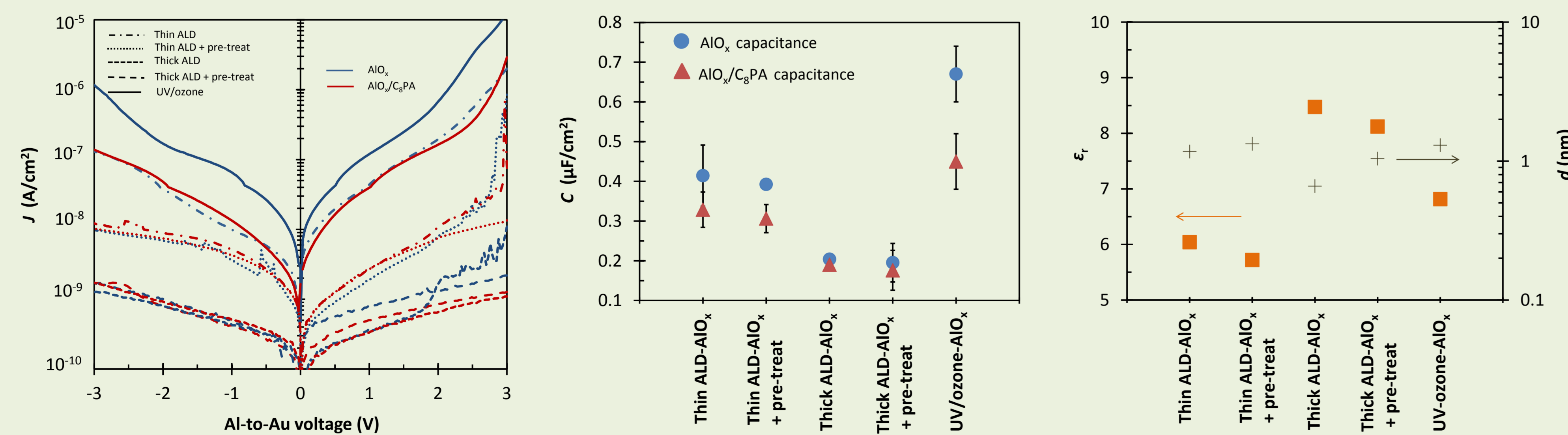
Saturation regime ( $|V_{DS}| > |V_{GS} - V_t|$ ):

$$I_D = \mu C \frac{W}{2L} (V_{GS} - V_t)^2 \quad \mu_{sat} = \left( \frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \cdot \frac{1}{C} \cdot \frac{W}{2L}$$

## FTIR



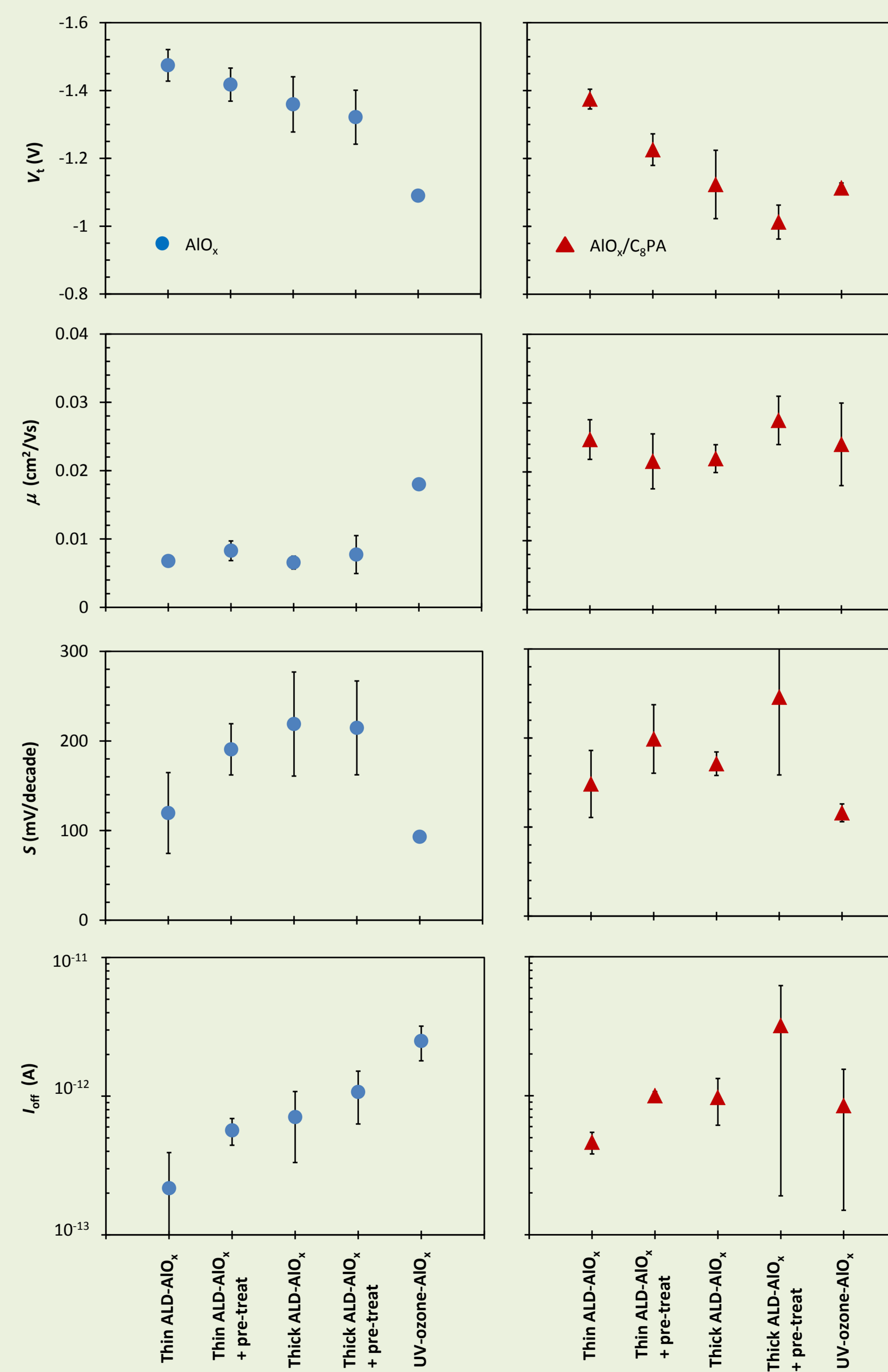
## RESULTS: MIM STRUCTURES



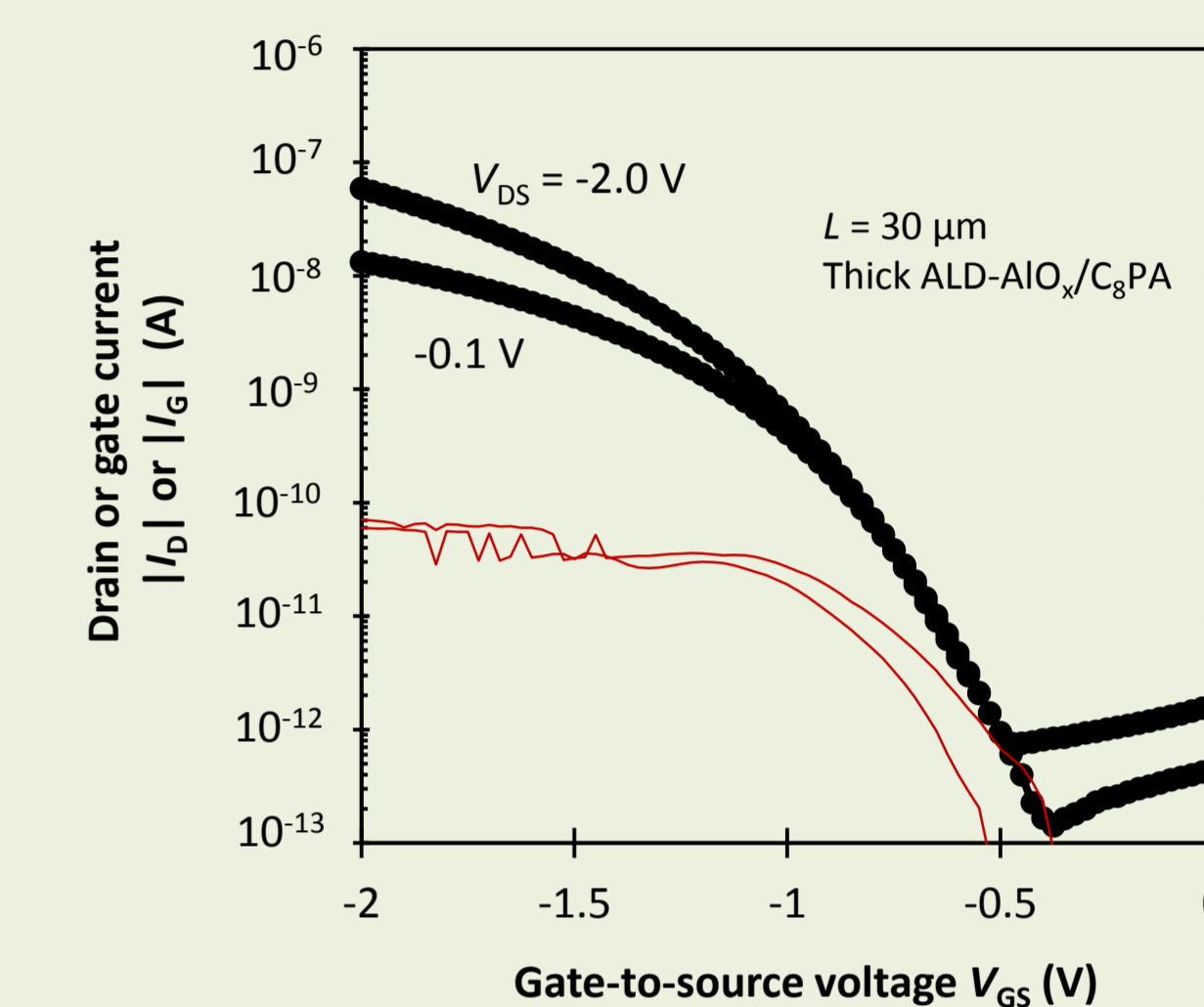
## CONCLUSIONS

- Leakage current density and capacitance are lower for ALD- $\text{AlO}_x$ ; primarily as a result of the thicker layer.
- $\text{C}_8\text{PA}$  self-assembly is not affected by the  $\text{AlO}_x$  layer or by its treatment.
- UV-ozone- $\text{AlO}_x$  leads to the lowest threshold voltage. Other parameters are comparable to OTFTs with ALD- $\text{AlO}_x$ .
- DNTT OTFTs show greatly improved transistor performance over pentacene devices; DNTT offers lower threshold voltage and substantially higher mobility.

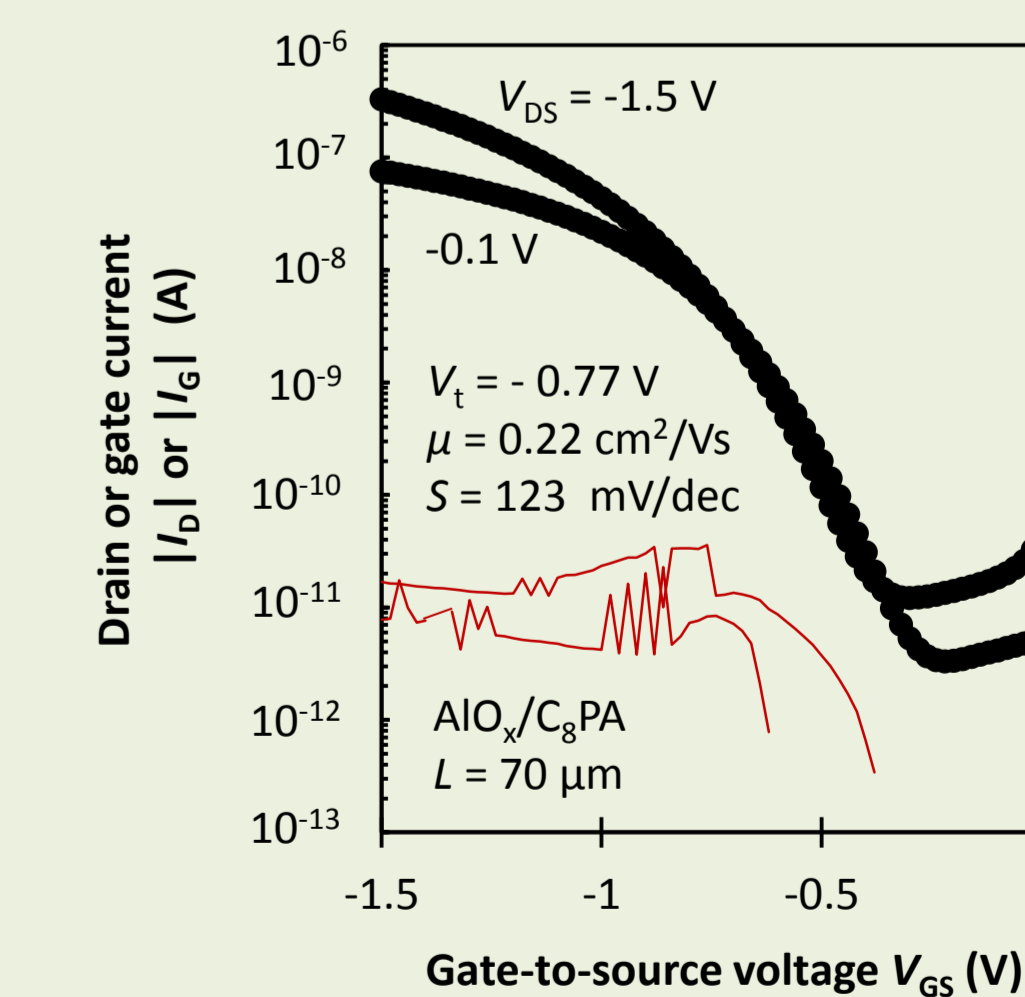
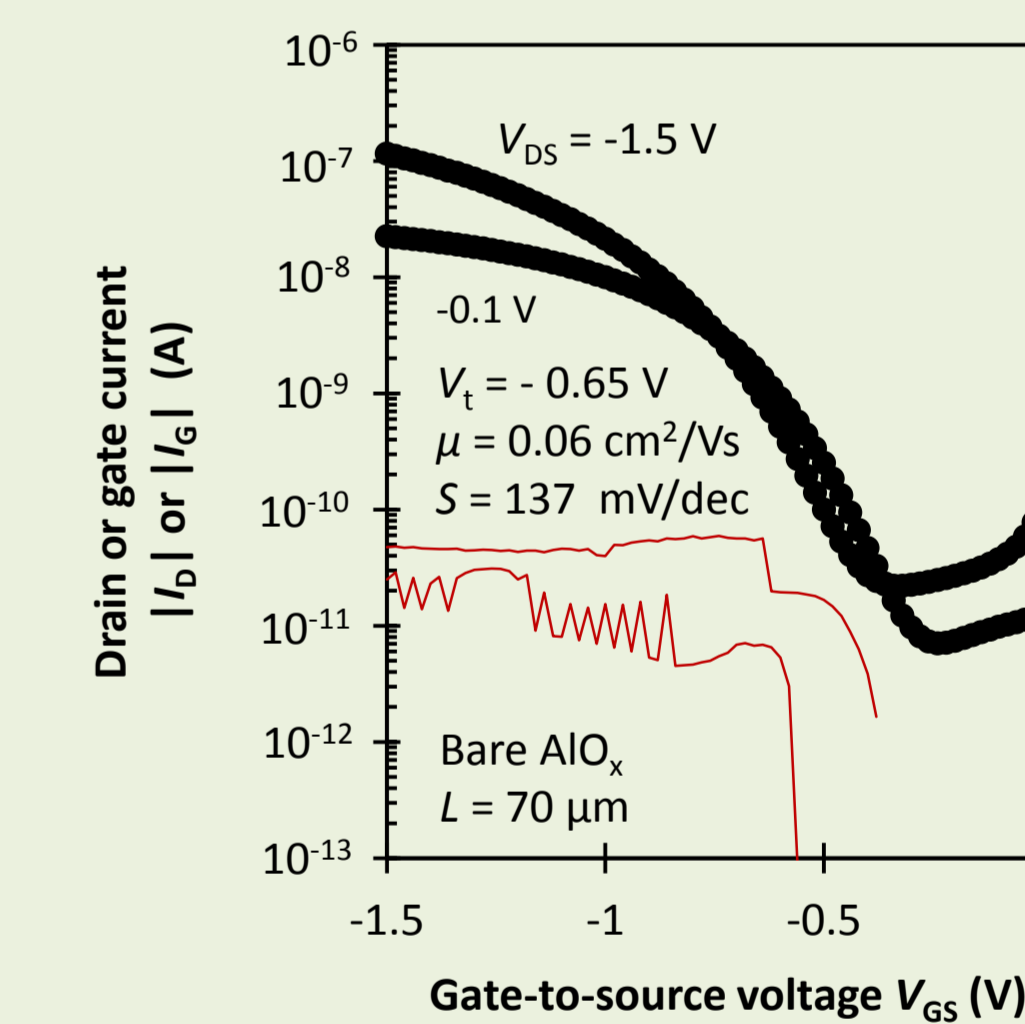
## RESULTS: PENTACENE TRANSISTORS



## PENTACENE TRANSISTORS



## DNTT TRANSISTORS



## ACKNOWLEDGEMENTS

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