DC Fault Detection and Location in Meshed Multi-terminal HVDC Systems Based on DC Reactor Voltage Change Rate

Rui Li, Lie Xu, Senior Member, IEEE and Liangzhong Yao, Senior Member

Abstract —The change rate of the DC reactor voltage with predefined protection voltage thresholds is proposed to provide fast and accurate DC fault detection in a meshed multi-terminal HVDC system. This is equivalent to the measurement of the second derivative of the DC current but has better robustness in terms of EMI noise immunization. In addition to fast DC fault detection, the proposed scheme can also accurately discriminate the faulty branch from the healthy ones in a meshed DC network by considering the voltage polarities and amplitudes of the two DC reactors connected to the same converter DC terminal. Fast fault detection leads to lower fault current stresses on DC circuit breakers and converter equipment. The proposed method requires no telecommunication, is independent of power flow direction, and is robust to fault resistance variation. Simulation of a meshed three-terminal HVDC system demonstrates the effectiveness of the proposed DC fault detection scheme.

Index Terms—DC fault protection, DC reactor voltage change rate, fault detection, modular multilevel converter (MMC), meshed multi-terminal HVDC system.

I. Introduction

For a large multi-terminal HVDC system, in the event of a DC fault, it is desirable that the converters connected to the healthy DC lines continue operating without disruption while the faulty branches are quickly isolated [1-3]. This raises the requirement of fast fault detection and faulty line identification to isolate the DC fault quickly and accurately.

In [4, 5], the DC currents are measured at both ends of each cable and the current difference is used to detect and locate the fault. However, fast telecommunication is required, leading to increased cost and reduced reliability considering possible communication interruption [6]. To improve fault detection reliability, the DC current is measured locally as a backup to communication failure [7]. Compared with the fault detection approach based on telecommunication, the backup method requires longer time to detect the fault and the fault location cannot be evaluated accurately.

A slow handshaking approach is proposed in [8] to avoid communication among terminals and to accurately identify the faulty branch. The DC switches at both ends of the faulty branch are then commanded to open to isolate the fault. However, this method leads to prolonged shut down of the complete system due to the slow fault detection and isolation. The DC transformer present in [9] can rapidly isolate the fault once the fault is detected but though with significant additional capital cost and power loss.

Based on a fault current model, the relationship between DC-link voltage and fault distance is derived in [10] to locate the fault and avoid the use of telecommunication. However, this method can only give a rough indication of the fault location and requires solid-state or fast hybrid DC circuit breakers (DCCBs) to clear the fault in around 1ms. Based on the circuit analysis of the capacitor discharge stage, the fault location approach discussed in [11] is capable of accurately evaluating the fault distance in a meshed DC network when the fault resistance is close to zero. However, with higher short-circuit resistance, the estimated fault distance error increases significantly. The methods presented in [10] and [11] only estimate the fault location but do not consider fault detection.

All the existing fault detection methods that are based on the measurements of DC voltage, DC current, or the currents flowing through semiconductor devices require considerable time period and thus lead to high fault current stresses for the stations and circuit breakers.

The derivative of DC voltage is proposed in [12] to quickly detect and locate DC faults in a bipole HVDC grid. However, the influence of the arm reactor is not considered and it is assumed that the converter output DC voltage remains unchanged immediately following a DC fault. In addition, high DC voltage derivative is observed when the fault is cleared by circuit breakers, resulting in interference to the protection controller. In [13], the DC current derivative is used to detect a DC fault. However, a DC capacitor is connected at the station terminal to support the DC voltage and the circuit breaker opening time is not considered. The severe transients following fault clearance may also falsely trigger protection on adjacent healthy DC cables.

Traveling waves are introduced in [14] and the multiplication of DC voltage and current derivatives are used to detect a DC fault without communication. However, it requires the calculation of both voltage and current derivatives that can be affected by measurement noise etc. Reference [15] proposes methods for continuous operation of a multi-terminal HVDC system during a DC fault and introduces a meshed three-terminal HVDC system with DC reactors on each end of the DC cables. However, the detailed fault detection approach is not presented.

This study focuses on fast and accurate DC fault detection and location in a meshed multi-terminal HVDC system based

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R. Li and L. Xu are with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, G1 1XW UK (e-mail: rui.li@strath.ac.uk, lie.xu@strath.ac.uk).

L.Z. Yao is with China Electric Power Research Institute, Xiaoying Road, Beijing, 100192, China (email: yaoliangzhong@epri.sgcc.com.cn).

on DC reactor voltage change rate. Fault location in this work means the discrimination of the faulty branch from the healthy ones in order to correctly open the DCCBs which are connected to the faulty cables. The paper is organized as follows. In Section II, the fault detection theory by measuring the voltage across the DC terminal reactor is introduced. DC fault detection in a meshed three-terminal HVDC system is discussed in Section III, considering the arm reactor influence. Fast, accurate, and robust DC fault detection using the proposed methods is presented in Section IV. The proposed DC fault detection scheme is assessed in Section V and finally, Section VI presents the conclusions of the study.

II. Fault Detection Theory with DC Terminal Inductances

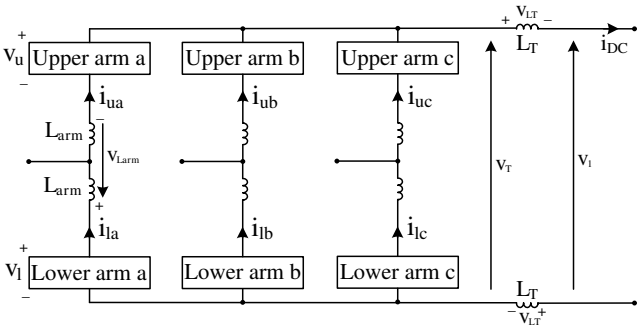


Fig. 1. Modular multilevel converter (MMC) with DC terminal reactors.

In normal operation, the converter generates the rated DC voltage V_{DC} and the voltages across the upper and low arm reactors (L_{arm}) and each of the two terminal reactors (L_T), as shown in Fig. 1, can be assumed to be zero:

$$v_u + v_l = V_{DC} = v_T = v_l \tag{1}$$

$$v_{Larm} = v_{LT} = 0 \tag{2}$$

where v_u and v_l are the upper and lower arm voltages respectively; v_T is the MMC terminal voltage; v_l is the DC voltage after the DC reactors; v_{Larm} is the total voltage across the two arm reactors on each phase; and v_{LT} is the voltage across the terminal reactor L_T.

After a DC fault occurs, the stations initially remain operational before converter fault detection. The DC fault results in rapid reduction of v_l and high DC voltages are imposed on the arm reactors L_{arm} ($v_{Larm}>0$) and the terminal reactors L_T ($v_{LT}>0$). At the initial fault stage, the DC components dominate the fault arm currents [15]. The MMC terminal voltage v_T drops below the rated DC voltage V_{DC} and the converter continues producing V_{DC} after the DC fault ($v_T=v_u+v_l-v_{Larm}$, $v_u+v_l=V_{DC}$, $v_T\leq V_{DC}$). For the MMC station, each arm is a series-connection of N_{arm} submodules (SMs) with the SM capacitance of C_{SM}. By using the sorting algorithm, the SM capacitor voltages can be balanced in each arm and thus the SM capacitors are equally discharged during the fault [16-18]. Thus, the equivalent phase capacitance C_{eP} in Fig. 2 (a) is obtained as [19]:

$$C_{eP} = 2C_{SM}/N_{arm}. \tag{3}$$

In Fig. 1, the total voltage stress for the two arm reactors on each phase can be approximated as:

$$v_{Larm} = V_{DC} - v_T. \tag{4}$$

The DC fault currents in each phase i_{fj} (j=a, b and c) can be regarded as identical and can be expressed as

$$i_{fa} = i_{fb} = i_{fc} = \frac{1}{2L_{arm}}\int_{t_0}^{t} v_{Larm}dt = \frac{1}{2L_{arm}}\int_{t_0}^{t}(V_{DC} - v_T)dt \tag{5}$$

where t_0 is the instant when the DC fault occurs. Then the upper arm current of phase j is

$$i_{uj} = \tfrac{1}{2}i_j + \tfrac{1}{3}I_{DC} + i_{fj} = \tfrac{1}{2}i_j + \tfrac{1}{3}I_{DC} + \frac{1}{2L_{arm}}\int_{t_0}^{t} v_{Larm}dt \tag{6}$$

where i_j is the AC side current of phase j and I_{DC} is the rated DC current.

The voltage across the terminal reactor causes an increase in the DC current i_{DC} as:

$$v_{LT} = L_T\frac{di_{DC}}{dt} \tag{7}$$

$$i_{DC} = I_{DC} + \frac{1}{L_T}\int_{t_0}^{t} v_{LT}dt \tag{8}$$

where v_{LT} is the DC voltage across the station terminal reactor. The DC current is the sum of the three-phase arm currents and thus (8) can be rewritten according to (6) as:

$$i_{DC} = \sum_{j=a,b,c} i_{uj} = I_{DC} + \frac{3}{2L_{arm}}\int_{t_0}^{t} v_{Larm}dt \,. \tag{9}$$

Comparing (8) to (9), the relationship between the voltages across the arm and terminal reactors is

$$v_{Larm} = \frac{2L_{arm}}{3L_T}v_{LT}\,. \tag{10}$$

Substituting (10) into (6) yields

$$i_{uj} = \tfrac{1}{2}i_j + \tfrac{1}{3}I_{DC} + \frac{1}{3L_T}\int_{t_0}^{t} v_{LT}dt\,. \tag{11}$$

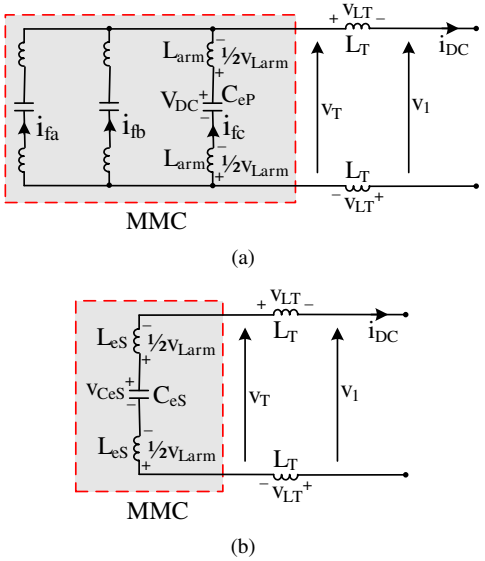


Fig. 2. Equivalent DC circuit of a converter station with terminal reactors: (a) considering each phase and (b) considering MMC.

As the arm and terminal reactors share the fault DC voltage, the following equations are obtained by considering (7) and

(10):

$$v_{Larm} + 2v_{LT} = \tfrac{2}{3} L_{arm} \frac{di_{DC}}{dt} + 2L_T \frac{di_{DC}}{dt} = V_{DC} - v_l \quad (12)$$

$$v_{LT} = \frac{3L_T}{6L_T + 2L_{arm}} (V_{DC} - v_l). \quad (13)$$

Thus, the equivalent DC circuit of the station during the fault is further simplified as the equivalent capacitance C_{eS} in series with the equivalent arm inductance L_{eS}, as shown in Fig. 2 (b). The initial capacitor voltage v_{CeS} is the rated DC voltage V_{DC} and C_{eS} and L_{eS} are expressed as:

$$C_{eS} = 3C_{eP} = 6C_{SM}/N_{arm}, \qquad L_{eS} = \tfrac{1}{3} L_{arm}. \quad (14)$$

Fig. 3 shows the typical waveforms for an ±400kV/1200MW MMC system during a DC fault at the DC cable 250km away from the station at time t_0=1s. The voltage across the DC terminal reactor L_T in steady state is near zero but rapidly increases from zero to 10kV in 2.4ms after fault initiation as demonstrated in Fig. 3 (d). Thus the voltage change across the station terminal reactor is the most sensitive variable to a DC fault among the possible local V, I measurements. By properly analyzing the voltage across the terminal reactor, the fault can be quickly detected. Based on this observation, the use of the voltage change across the terminal reactor which equals to the second derivative of the DC current, is proposed for detecting and locating DC faults at the station.

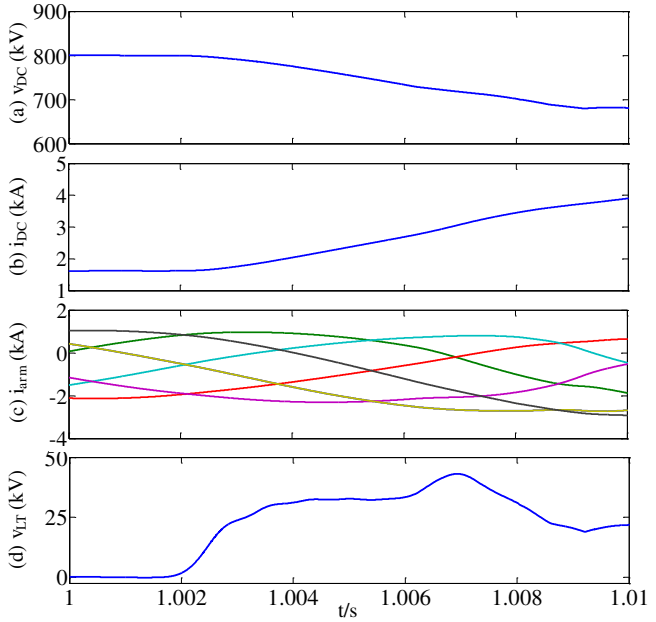


Fig. 3. Alternative measurements for DC fault detection: (a) DC voltage, (b) DC current, (c) arm currents, and (d) voltage across the station DC terminal reactor.

III. DC Fault Detection of Meshed Three-Terminal HVDC System

A. Meshed Three-Terminal HVDC System

Fig. 4 shows a typical meshed three-terminal HVDC system incorporating DC reactors at each end of the DC cables. A symmetric monopole HVDC structure is adopted as its interface transformer does not suffer DC voltage stresses in normal operation. In addition, this structure is robust to a pole-to-ground fault, which does not cause steady-state fault currents for the test system [20]. The pi section model is widely used in the literature to simulate the HVDC cables for transient studies [21-27]. To obtain satisfactory simulation accuracy, each cable is modeled with 10 pi sections in this paper to simulate high frequency behavior during a fault [22, 28]. The pole-to-pole DC fault is the most serious fault case for HVDC systems and is thus considered in this paper [11, 13, 29, 30]. The parameters of the test system are listed in Table I.

As MMCs typically use hundreds of submodules per arm in HVDC application, it is extremely time consuming to simulate the whole system using detailed switching models, which considers the switching behavior of the IGBTs/diodes. To reduce computation time and accelerate the simulation, average models are widely adopted to represent the MMC behavior [31-35]. It has demonstrated that such average models provide adequate accuracy for DC fault detection studies [12, 13, 32, 33] and are thus adopted in this study.

In Fig. 4, Station S_2 regulates the DC voltage of the DC network while S_1 and S_3 import rated active power P_1 and P_3 into the HVDC network. When a DC fault occurs at Cable i (i=1, 2, or 3), the circuit breakers connected to the faulty cable are opened once the fault is detected, whereas the other DCCBs on the healthy branches remain closed in order to allow continuous power transfer. Strategies for selecting the correct DCCBs to open will be discussed in this paper. The DCCBs are modeled with an opening time of 2ms [12, 20, 36, 37] and all the DC terminal reactors are set at 200mH in this study to limit the fault current and also to be used for fault detection.

TABLE I
Nominal Parameters of the Modeled Test System.

Parameter	Nominal Value
DC-link voltage	±400kV
Power rating of stations S_1, S_2 and S_3	700MW, 1200MW, 500MW
Number of SMs per arm	380
SM capacitor voltage	2.105kV
Arm inductance	0.05p.u.
Interface transformer ratio	400kV/480kV
Interface transformer leakage inductance	0.2p.u.
Number of DC cable pi sections	10
R, L and C of DC cables	10mΩ/km, 0.56mH/km, 0.26μF/km
DC terminal reactor	200mH

B. Fault Detection Indicator

As previously described, the change rate of the DC reactor voltage can provide a fast and accurate detection of a DC fault in a HVDC system. In the proposed scheme, a time interval Δt for the voltage across the terminal reactor to rise from an initial threshold V_{LTt1} to the protection threshold V_{LTt2} is used to depict the derivative of DC reactor voltage:

$$\frac{V_{LTt2} - V_{LTt1}}{\Delta t} = \frac{\Delta v_{LT}}{\Delta t} = \frac{dv_{LT}}{dt} = L_T \frac{d^2 i_{DC}}{dt^2}. \quad (15)$$

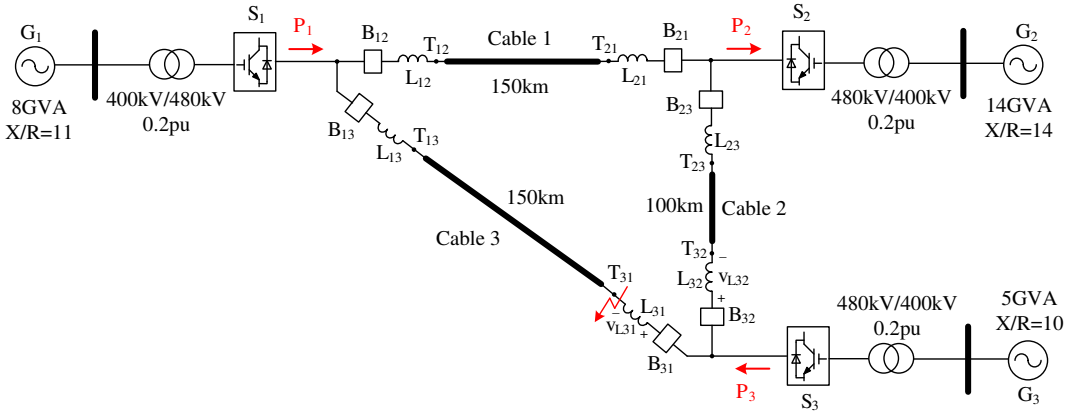


Fig. 4. Meshed three-terminal HVDC transmission system with DC reactor at each end of the DC cables.

With predefined thresholds V_{LTt1} and V_{LTt2}, the derivative of the DC reactor voltage is determined by the time interval Δt. By monitoring Δt, the change rate of the DC reactor voltage is used to provide faster fault detection, location, and isolation, yielding low fault current stresses on converter components and circuit breakers.

To improve robustness of the proposed scheme, the minimum fault detection time is introduced. The voltage across the DC reactor is measured continuously and only a fault detection that lasts longer than a minimum fault detection time is valid. In other words, if the time interval Δt is less than the minimum fault detection time, it is considered as false and there is no fault protection activation. This would avoid potential EMI issues and thus the proposed DC fault detection approach can be more robust than the method presented in [12-14] where the instantaneous measurements could potentially trigger a false detection.

As shown in (15), the time interval Δt also depicts the behavior of the second derivative of the DC current. The proposed scheme is thus similar to the measurement of the second derivative of the DC current but has better robustness in terms of EMI noise immunization.

In a multi-terminal HVDC system, it is required for stations to distinguish a relevant fault from an irrelevant fault [38]. Taking station S_1 as an example, the fault at Cable 2 does not trigger the protection action and is an irrelevant fault for S_1. However, for the fault on Cable 1 or 3, which is a relevant fault for station S_1, the corresponding circuit breakers B_{12} or B_{13} are required to open to isolate the fault. For a relevant fault, the voltage across the terminal reactor increases faster than that during an irrelevant DC fault. Thus, the measured time interval Δt is shorter for relevant fault compared to irrelevant fault, and a time threshold can be used to distinguish the two faults, as will be detailed in Section IV A.

Compared to over-current based fault detection method, the proposed strategy is particular effective when the initial DC current in a converter has opposite direction to the fault current. Under such operation conditions, the DC current and the DC component of the arm current reverse and cross zero after fault occurrence and consequently, it takes them much longer to reach the over-current threshold, resulting in a slower fault detection. However, the proposed detection scheme is based on terminal reactor voltage change rate which is independent to power flow direction.

C. Influence of Arm Inductance on the Fault Detection

In the meshed three-terminal HVDC system shown in Fig. 4, two DC reactors are connected at each pole of the stations. Its DC fault detection is different to that in a radial system and the influence of the arm inductance needs to be considered.

A pole-to-pole DC fault at the terminal T_{31} in Fig. 4 is considered here to illustrate the influence of the arm inductance on fault detection. After fault occurrence at $t=t_0$, the station S_3 and the non-fault Cable 2 are discharged through the circuit as depicted by Fig. 5, where C_{eC} is the equivalent capacitor on the terminal of Cables 2 with the voltage of v_{CeC} and

$$v_{CeC}(t_0) = \tfrac{1}{2} v_{CeS}(t_0) = \tfrac{1}{2} V_{DC}. \tag{16}$$

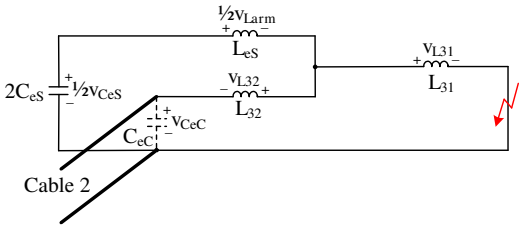


Fig. 5. Single pole equivalent circuit at the station terminal with a pole-to-pole DC fault at T_{31} in the meshed three-terminal HVDC network as illustrated in Fig. 4.

The voltages across the reactors during normal operation are approximately zero:

$$v_{L31}(t_{0-}) = v_{L32}(t_{0-}) = \tfrac{1}{2} v_{Larm}(t_{0-}) = 0. \tag{17}$$

A DC fault at the station terminals results in the immediate increase of the voltage across the reactors, as the rated DC voltage is shared between the arm reactors and the DC reactors at the station terminal immediately following the fault as:

$$v_{L31}(t_{0+}) - v_{L32}(t_{0+}) = v_{L31}(t_{0+}) + \tfrac{1}{2} v_{Larm}(t_{0+}) = \tfrac{1}{2} V_{DC} \tag{18}$$

$$v_{L31}(t_{0+}) = \frac{L_{31}}{\frac{L_{eS} L_{32}}{L_{eS} + L_{32}} + L_{31}} \tfrac{1}{2} V_{DC} = \frac{L_{eS} L_{31} + L_{31} L_{32}}{2\left(L_{eS} L_{32} + L_{eS} L_{31} + L_{31} L_{32}\right)} V_{DC} \tag{19}$$

$$v_{L32}(t_{0+}) = -\tfrac{1}{2}v_{Larm}(t_{0+}) = -\frac{\frac{L_{eS}L_{32}}{L_{eS}+L_{32}}}{\frac{L_{eS}L_{32}}{L_{eS}+L_{32}}+L_{31}}\tfrac{1}{2}V_{DC} = -\frac{L_{eS}L_{32}}{2\left(L_{eS}L_{32}+L_{eS}L_{31}+L_{31}L_{32}\right)}V_{DC}. \quad (20)$$

In addition to the DC reactor voltage v_{31}, the voltage v_{32} across the DC reactor L_{32} also increases immediately, due to the equivalent arm inductance L_{eS}. This results in short time interval Δt for the adjacent healthy branch (Cable 2, Fig. 4) and the corresponding circuit breakers B_{32} would be falsely opened. To suppress the influence of the arm inductance and avoid false fault detection, the voltage polarities and amplitudes of the two DC reactors are considered in the fault detection in a meshed network.

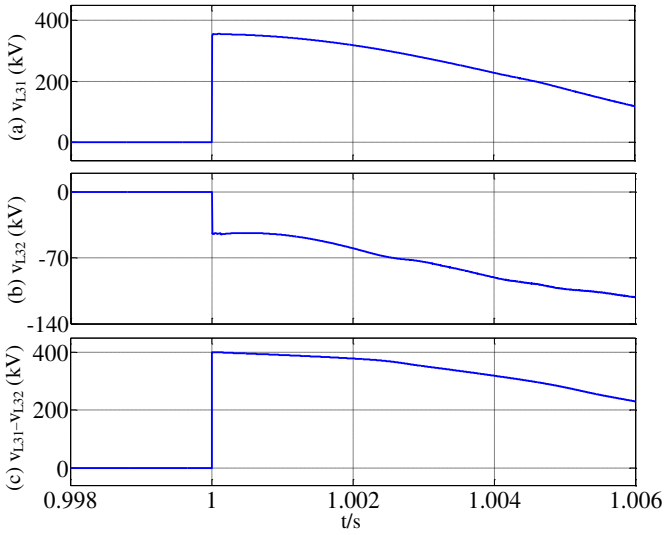


Fig. 6. Voltages across the reactors at the station terminals in a meshed three-terminal HVDC network, with a pole-to-pole DC fault applied at T_{31}: (a) DC reactor voltage v_{L31}, (b) DC reactor voltage v_{L32}, and (c) difference between DC reactor voltages (v_{L31}- v_{L32}).

Following the fault, the voltage across the reactor on the faulty branch increases rapidly and becomes greater than that on the healthy branch. In addition, the DC reactor voltages of the faulty and healthy branches are positive and negative respectively, as depicted by (19) and (20). Based on these observations, only a positive, higher amplitude DC reactor voltage is considered as the thresholds V_{LTt1} and V_{LTt2} in (15). By comparing the amplitudes and polarities of the two locally accessible DC reactor voltages, potential false fault detection caused by the arm reactors is avoided in a meshed HVDC system and the faulty branch can be identified quickly. Thus, the DC circuit breakers connected with the faulty branch can be quickly opened to isolate the fault.

As shown in Fig. 6, all the reactor voltages prior to the fault are approximately zero. After a pole-to-pole DC fault occurs at T_{31} at t_0=1s, the voltages across the station DC terminal reactors increase from zero to 360kV and -40kV respectively, which are in agreement with (19) and (20).

IV. Sensitivity, Accuracy, and Robustness Consideration

A. Discrimination of the Faulty Branch from the Healthy Ones in a Meshed DC Network

To discriminate the faulty branch from the healthy ones, the time threshold needs to be properly set such that the fault can be quickly detected and the corresponding DCCBs can be correctly commanded to open.

Station S_1 is considered here to illustrate the proposed fault detection and location method when a pole-to-pole DC fault occurs at different locations in the test model. As shown in Fig. 7, where the threshold voltages V_{LTt1} and V_{LTt2} are set at 5kV and 10kV respectively, Δt is less than 100μs for all the relevant fault cases, whilst Δt is great than 270μs during an irrelevant cable fault. Thus the threshold of fault location indication time is set at 180μs in this study. If the time interval Δt is less than the threshold 180μs, it indicates that the fault occurs on the relevant cable and the DCCBs connected on the faulty branch shall be commanded to open, according to the aforementioned principle in Section III C. If Δt is longer than 180μs, the station remains operational and no protection action is activated.

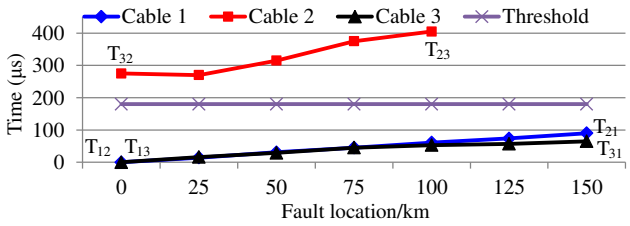


Fig. 7. Fault location indication time Δt of station S_1 when a fault occurs at relevant (Cables 1 and 3) and irrelevant cables (Cable 2).

Fig. 8 displays the fault detection time of station S_1 when a fault occurs on different cables. When the fault is applied at the terminal T_{13} in Fig. 4, it only takes microseconds for S_1 to detect the relevant fault. With the increase of distance to station S_1, the detection time for a relevant fault increases, as illustrated in Fig. 8. However, all the relevant fault can be detected in less than 1.4ms at S_1, much short than the conventional approaches that measure DC voltage or current [4, 5, 7, 8, 39].

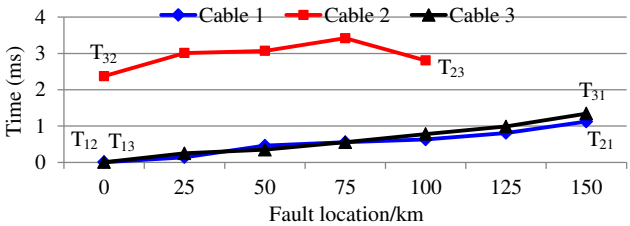


Fig. 8. Fault detection time of station S_1 when a fault occurs on different cables.

When a fault is applied at Cable 2 (irrelevant fault for Station S_1), the longest fault detection time of S_1 is 3.4ms as shown in Fig. 8. As an irrelevant fault does not impose the station to overcurrent risk, S_1 needs to remain operational and

no DCCB actions are required at the S_1 terminal. As a result, the relatively long irrelevant fault detection time (3.4ms) has no negative effect on the system performance during a DC fault.

The fault detection times of the test system in Fig. 4 are listed in Table II. Considering the fault at the middle point of Cable 3, the DC reactor voltage of station S_1 reaches the threshold voltages 5kV and 10kV after 510μs and 560μs respectively from fault initiation and the corresponding indication time Δt is 50μs, shorter than the threshold of 180μs. Thus, a relevant fault is reported after 560μs from fault occurrence and circuit breaker B_{13} is commanded to open. Due to the same distance to the fault location, the fault detection time of station S_3 is identical to that of S_1. For station S_2, an irrelevant fault is reported 2495μs after fault initiation since the indication time Δt is longer than 180μs, leading to its continues operating.

As shown in Table II, all the selected fault cases can be detected quickly while the fault location is accurately identified. The longest relevant fault detection time, after which the circuit breaker on the fault branch is commanded to open, is less than 1.4ms. Considering the operational speed of the control system in real applications, the aforementioned minimum fault detection time is set at 50μs to avoid false fault detection caused by EMI, etc.

TABLE II
Fault Detection Time of the Mesh HVDC Network with DC Cables.

Fault Location		Terminal T_{13}	Terminal T_{12}	Terminal T_{21}	Terminal T_{23}	Terminal T_{32}	Terminal T_{31}	Middle point of Cable 3
Station S_1	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	5	5	1035	2400	2095	1280	510
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	5	5	1125	2805	2375	1345	560
	Fault location indication time: Δt (μs)	**0**	**0**	**90**	**405**	**280**	**65**	**50**
Station S_2	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	2230	1035	5	5	685	1505	2220
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	2545	1125	5	5	745	1780	2495
	Fault location indication time: Δt (μs)	**315**	**90**	**0**	**0**	**60**	**275**	**275**
Station S_3	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	1280	2190	1705	685	5	5	510
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	1345	2495	2130	745	5	5	560
	Fault location indication time: Δt (μs)	**65**	**305**	**425**	**60**	**0**	**0**	**50**

B. Influence of Short-circuit Resistance and Power Reversal

As being demonstrated, the proposed schemes can detect and locate a solid pole-to-pole DC fault quickly and accurately when the short-circuit resistance is almost zero. This section assesses the DC fault detection performance for different short-circuit resistances. The potential impact of maximum power reversal under normal operation on fault detection is also tested.

The approach in [11] evaluates the fault with zero short-circuit resistance, while for a fault with considerable short-circuit resistance, significant errors are introduced into the evaluation results. The proposed fault detection methods only monitor the local DC reactor voltages and are independent of the voltage at fault location. Thus, they are insensitive to different short-circuit resistances, yielding high reliability.

As shown in Table III, due to the short-circuit resistance between the positive and negative poles, it takes longer for the DC reactor voltage to increase to the thresholds (5kV and 10kV) than that with zero short-circuit resistance shown in Table II. However, the fault location indication time Δt of stations S_1 and S_3 is still lower than the preset threshold (180μs), even with 1000Ω (1p.u.) short-circuit resistance. This indicates a DC fault with large short-circuit resistance can still be detected quickly and accurately by the proposed detection scheme.

TABLE III
Detection Time When a Pole-to-pole DC Fault Is Applied at T_{31} with Different Short-circuit Resistances, Where the Base Power and Voltage Are 700MW and ±400kV Respectively.

		Short-circuit resistance: 100Ω (0.1p.u.)	Short-circuit resistance: 1000Ω (1p.u.)
		Short-circuit power: 6400MW	Short-circuit power: 640MW
Station S_1	Δt_1 (μs)	1360	1585
	Δt_2 (μs)	1430	1675
	Δt (μs)	**70**	**90**
Station S_2	Δt_1 (μs)	1635	6820
	Δt_2 (μs)	1975	∞
	Δt (μs)	**340**	∞
Station S_3	Δt_1 (μs)	5	15
	Δt_2 (μs)	10	35
	Δt (μs)	**5**	**20**

With 1000Ω (1p.u.) short-circuit resistance, the terminal reactor voltage of station S_2 is always lower than 10kV and the fault location indication time Δt can not be measured (becomes infinite in theory). Hence no relevant fault is

detected and S_2 remains operational. The time Δt_1 for the reactor voltage to increase to the initial threshold (5kV) needs to be reset if the reactor voltage is always lower than the protection threshold (10kV) after a considerable measurement period.

During a power reversal, the DC current changes direction and considerable voltage could appear across the DC reactors. Fig. 9 shows the DC reactor voltage where the power is reversed at a rate of 24GW/s, much higher than that would be experienced in real systems. As demonstrated in Fig. 9 (b), the voltage across the station terminal DC reactor is much lower than the thresholds 5kV and 10kV using the proposed approach even with such a fast power reversal. As a result, no fault is reported and false detection is avoided even with such a fast reversal rate.

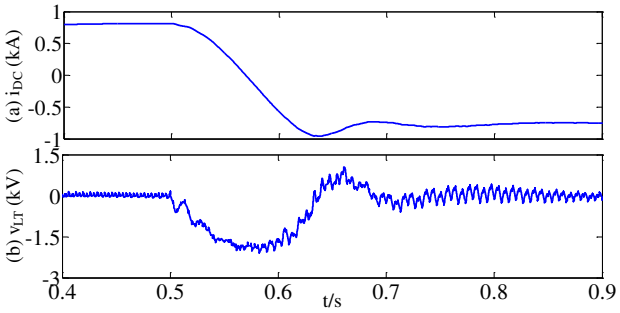


Fig. 9. Simulated waveforms with power reversal from 1.2GW to -1.2GW from t=0.5s to t=0.6s: (a) DC current and (b) voltage across the station terminal DC reactor.

C. Interference by Circuit Breaker Opening

The opening of DCCBs can affect the change rate of the DC reactor voltage. However, as shown below, this is unlikely to cause the false action of the circuit breakers on the healthy branches by using the proposed scheme.

After fault initiation, the voltage across the DC terminal reactor rapidly increases from zero. The proposed method uses a time interval Δt for the voltage across the terminal reactor to rise from an initial threshold V_{LTt1} (5kV) to the protection threshold V_{LTt2} (10kV) to depict the derivative of the DC reactor voltage. If the measurement indicates an irrelevant fault, further calculation of the voltage change rate for the DC reactors connected to the healthy branches is disabled and no further action will be taken so as to avoid any potential false trigger during the transient caused by the opening of DCCBs on the remote faulty branches.

D. Comparison between the Proposed and Other Derivative Measurement Based Methods

The proposed fault detection scheme and other approaches that use the measured DC voltage derivative [12] or DC current derivative [13] all require no telecommunication. However, the proposed method has better performance than the others considering the detection speed, accuracy, reliability, and robustness.

In the proposed scheme, the change rate of the DC reactor voltage equivalent to the second derivative of the DC current is monitored with predefined protection voltage thresholds, to ensure faster fault detection capability. As shown in Fig. 3 (b), the fault is detected at 2.4ms after fault initiation whereas the DC current is still much lower than 2pu. This indicates the proposed method can detect the fault earlier than the scheme measuring DC current derivative in [13], where the DC current peak is close to 5pu.

In a meshed HVDC system, false fault detection caused by the arm reactors can be avoided by comparing the amplitudes and polarities of the locally accessible DC reactor voltages, yielding accurate fault detection with high reliability. By introducing the minimum fault detection time, the proposed scheme has better EMI noise immunization compared to the approaches in [12] and [13] where the instantaneous measurements could trigger a false detection, leading to higher reliability and better robustness.

To measure the DC reactor voltage, additional voltage dividers are required in the presented approach though their costs are trivial when compared to the total cost of a HVDC project especially when considering the fast and accurate fault detection capability of the proposed scheme.

V. Performance Evaluation

The proposed DC fault detection scheme is assessed using the meshed three-terminal HVDC model shown in Fig. 4. The simulated scenarios assume a permanent pole-to-pole DC fault at T_{31} at time t_0=1s, as illustrated in Fig. 4. The results with the proposed approach are compared to those obtained using conventional approach, where the protection threshold of the arm current peak is set at 2p.u. The detailed comparison is listed in Table IV and shown in Figs. 10-13.

TABLE IV
Comparison between the Proposed Scheme and Conventional Approach during a DC Fault at T_{31}.

		Conventional approach	Proposed scheme
Fault detection time	Station S_1	2.863ms	1.345ms
	Station S_2	N/A	1.780ms
	Station S_3	1.458ms	0.05ms
Station status	Station S_1	blocked	operational
	Station S_2	operational	operational
	Station S_3	blocked	blocked
Current peak of DCCB	DCCB B_{31}	3.5kA	2.5kA
	DCCB B_{13}	5.7kA	4.9kA
Energy absorbed by DCCB	DCCB B_{31}	3.4MJ	1.6MJ
	DCCB B_{13}	8. 6MJ	5.9MJ
Maximum $\int i^2(t)dt$ of arm currents in station S_3		4.3kA^{2}s	3.1kA^{2}s

A. Station S_3

Fig. 10 compares the arm currents of station S_3 using the two methods indicating significant reduction by the proposed one. According to the proposed approach, S_3 detects the fault and identifies it as a relevant fault on Cable 3 after 0.05ms from fault initiation, faster than conventional approach

(1.458ms), as listed in Table IV. Then the circuit breaker B_{31}, connected on the faulty branch at the station terminal, is commanded to open in order to isolate the fault whilst station S_3 continues operating. Due to the nearest fault location and the required opening time of the circuit breaker (2ms), the peak arm current of S_3 reaches the current protection threshold (2p.u.) before the fault is isolated by B_{31} and the converter is immediately blocked to protect the switches.

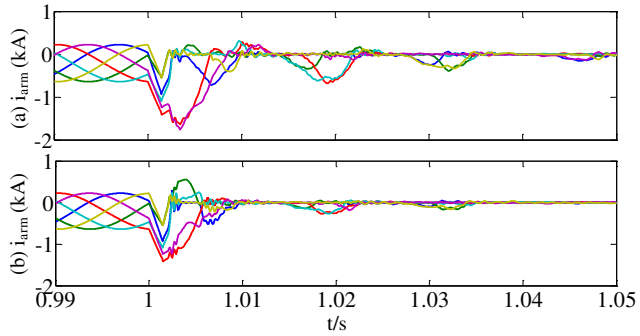


Fig. 10. Arm currents of station S_3 with: (a) conventional fault detection and (b) proposed scheme.

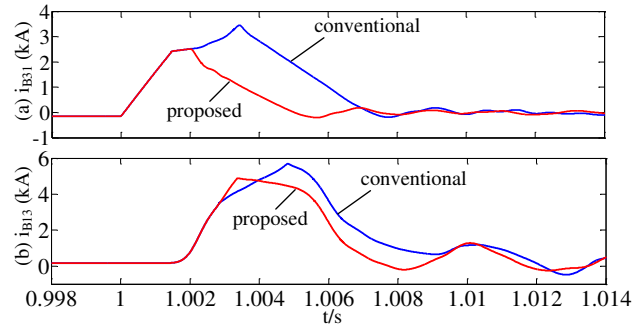


Fig. 11. Currents flowing through DC circuit breakers with the conventional fault detection approach and the proposed scheme: (a) breaker B_{31} and (b) breaker B_{13}.

The calculated maximum $\int i^2(t)dt$ of the fault currents flowing through the anti-parallel diodes after the blocking of station S_3 until the fault isolation by B_{31} are 3.1kA^{2}s for the proposed method and 4.3kA^{2}s for the conventional approach, as indicated in Table IV.

The DC current flowing through the circuit breaker B_{31} continues to increase following the fault and reaches a peak of 2.5kA, lower than that with conventional approach (3.5kA), as shown in Fig. 11 (a). Compared to the conventional approach, the reduced fault detection time by the proposed method leads to lower DC breaking current and hence reduced energy absorption for B_{31} (1.6MJ compared to 3.4MJ for the conventional approach), as can be seen in Table IV.

B. Station S_1

Station S_1 detects the fault on Cable 3 after 1.345ms from the fault initiation. Then circuit breaker B_{13} is commanded to open to isolate the fault with the opening time of 2ms. Benefiting from the fast fault detection ability of the proposed approach, the arm current peak is lower than the current protection threshold of 2p.u. and S_1 remains operational to transfer power, as can be seen in Fig. 12 (b). In contrast, station S_1 would have to be blocked due to overcurrent resulted from slower fault detection and isolation if conventional method was to be adopted, Fig. 12 (a).

Similar to station S_3, the fault is isolated earlier at terminals of station S_1 by circuit breaker B_{13}, yielding reduced capacity of B_{13}, as evident in Fig. 11 (b) and Table IV.

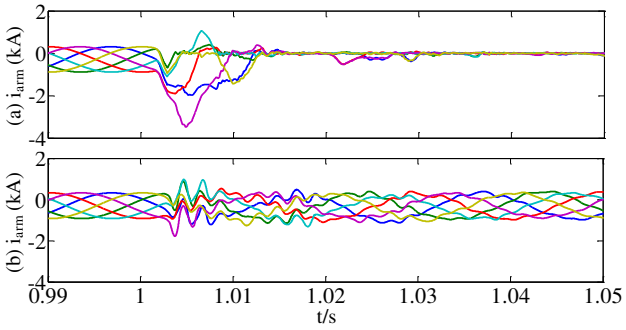


Fig. 12. Arm currents of station S_1 with: (a) conventional fault detection and (b) proposed scheme.

C. Station S_2

Stations S_2 detects the fault after 1.505ms from the fault initiation and identifies it as an irrelevant fault at 1.00178s (i.e. 1.78ms after fault initiation) using the proposed approach. Thus S_2 remains operational to transfer power as seen in Fig. 13 (b).

The simulation results show that fast, accurate, and robust DC fault detection and location can be achieved by the proposed scheme. This reduces the DCCB requirement and the fault current stress on the converter semiconductors, while the power transfer between stations S_1 and S_2 can continue.

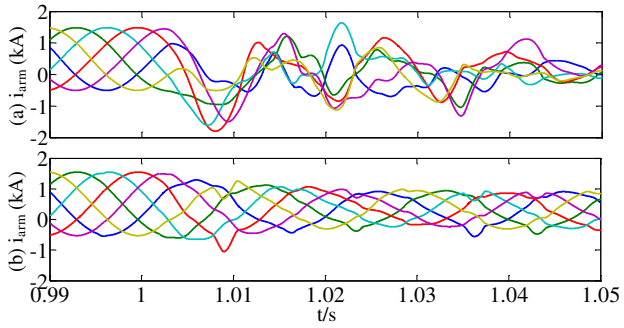


Fig. 13. Arm currents of station S_2 with: (a) conventional fault detection and (b) proposed scheme.

VI. Discussion

A. Fault Detection of HVDC Network with Both DC Cable and Overhead Line (OHL)

To validate the effectiveness of the proposed scheme for the DC network with both DC cable and OHL, the transmission line between stations S_1 and S_3 (Cable 3) in Fig. 4 is replaced by a 150km OHL. The parameters of the OHL are adopted from those suggested in the CIGRE B4 DC Grid Test System: 11.4mΩ/km, 0.9356mH/km, and 0.0123μF/km [40]. All the other parameters and operation condition remain unchanged from previous studies.

The fault propagates faster along the OHL than the cables due to the smaller capacitance and the fault can be detected

earlier. Thus, the threshold of fault location indication time needs to be reduced for the DC reactor on the OHL, to discriminate the faulty branch from the healthy ones. In the tested HVDC network, the threshold times are set at 130μs and 45μs for the DC reactors connected to the DC cable and OHL, respectively.

As mentioned in Section III C, the two locally accessible DC reactor voltages are compared and only a positive, higher amplitude DC reactor voltage is considered as the thresholds V_{LTt1} and V_{LTt2}. When the positive, higher amplitude voltage is measured across the DC reactor on the OHL, the time interval Δt is compared to the threshold time of 45μs. If Δt is less than the threshold 45μs, it indicates that the fault occurs on the relevant OHL. Otherwise, the fault is located on the irrelevant DC cable, and thus the station keeps operating and no protection action is activated. When the voltage across the DC reactor on the DC cable is positive and has higher amplitude, the time interval Δt is compared to the threshold time of 130μs to discriminate the relevant faults from the irrelevant ones.

The fault detection times of the tested model with both DC cable and OHL are listed in Table V, where the shaded parts indicate the positive, higher amplitude voltage is measured across the DC reactor on the OHL (L_{13} and L_{31} for stations S_1 and S_3 respectively). The fault location indication time Δt is less than the threshold 45μs for all the relevant OHL fault cases, whilst Δt is great than 45μs during an irrelevant fault.

Similarly, the relevant faults can be identified from the irrelevant ones when the positive, higher amplitude voltage is measured across the reactor on the DC cable (unshaded parts in Table V). The fault in the meshed HVDC network with both OHL and DC cable can still be fast detected and accurately located by the proposed scheme.

TABLE V
Fault Detection Time of the Mesh HVDC Network with Both DC Cable and OHL.

Fault Location		Terminal T_{13}	Terminal T_{12}	Terminal T_{21}	Terminal T_{23}	Terminal T_{32}	Terminal T_{31}	Middle point of OHL
Station S_1	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	5	5	1290	1660	565	345	135
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	5	5	1355	1740	635	365	145
	Fault location indication time: Δt (μs)	**0**	**0**	**65**	**80**	**70**	**20**	**10**
Station S_2	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	1910	1285	5	5	845	1505	1655
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	2100	1350	5	5	890	1795	1850
	Fault location indication time: Δt (μs)	**190**	**65**	**0**	**0**	**45**	**290**	**195**
Station S_3	Time for reactor voltage to increase to 5kV: Δt_1 (μs)	345	590	2280	850	5	5	135
	Time for reactor voltage to increase to 10kV: Δt_2 (μs)	365	670	2390	895	5	5	145
	Fault location indication time: Δt (μs)	**20**	**80**	**110**	**45**	**0**	**0**	**10**

B. Consideration of Different DC Terminal Inductances

To test the sensitivity of the proposed scheme with different DC terminal inductance, the inductance of all the DC terminal reactors is reduced from 200mH to 100mH, whist all the other parameters and operation condition are the same as that presented in Section III A.

Station S_1 is considered to demonstrate the influence of the DC reactor on the fault detection. With smaller DC terminal inductance (from 200mH to 100mH), the maximum fault location indication time Δt for a relevant fault (at Cables 1 and 3) is reduced from 90μs to 65μs, and the minimum Δt for an irrelevant fault (at Cables 2) is lowered from 275μs to 185μs. Although the difference between the relevant and irrelevant fault location indication time Δt is reduced from 185μs (275μs-90μs) to 120μs (185μs-65μs), the fault can still be identified with smaller DC reactance (100mH), by setting the threshold at 125μs.

VII. Conclusion

The change rate of DC reactor voltage with predefined protection voltage thresholds is proposed to detect a DC fault in a meshed multi-terminal HVDC system with DC reactors connected on each end of the DC cables. The fault voltage distribution among the DC terminal inductances and the arm inductances is analyzed using the parallel-series equivalent circuit. The DC reactor voltage is continuously monitored to quickly and accurately detect and discriminate the fault. All the measurements are local and no telecommunication is required, yielding high reliability and low cost. The proposed approaches provide fast DC fault detection and location and thus the fault can be isolated quickly and reliably. This leads to reduced fault current stress on stations and circuit breakers. The methods are also independent of the power flow direction and a DC fault with significant short-circuit resistance can be detected and discriminated quickly and accurately. The proposed methods provide an attractive approach with high robustness and reliability for application in future meshed multi-terminal HVDC systems.

VIII. References

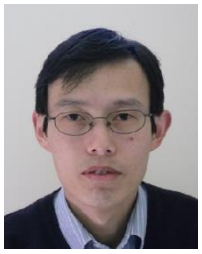
[1] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and Operation of a Hybrid Modular Multilevel Converter," IEEE Trans. Power Electron., vol. 30, pp. 1137-1146, 2015.

[2] T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-Frequency Operation of a DC/AC/DC System for HVDC

Applications," IEEE Trans. Power Electron., vol. 29, pp. 4107-4115, 2014.
[3] R. Li, J. E. Fletcher, L. Xu, D. Holliday, and B. W. Williams, "A Hybrid Modular Multilevel Converter With Novel Three-Level Cells for DC Fault Blocking Capability," IEEE Trans. Power Del., vol. 30, pp. 2017-2026, 2015.
[4] J. D. Park and J. Candelaria, "Fault Detection and Isolation in Low-Voltage DC-Bus Microgrid System," IEEE Trans. Power Del., vol. 28, pp. 779-787, 2013.
[5] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of HVDC Transmission System Topology on Multiterminal DC Network Faults," IEEE Trans. Power Del., vol. PP, pp. 1-1, 2014.
[6] W. Wenyuan and M. Barnes, "Power Flow Algorithms for Multi-Terminal VSC-HVDC With Droop Control," IEEE Trans. Power Sys., vol. 29, pp. 1721-1730, 2014.
[7] J. Descloux, P. Rault, S. Nguefeu, J. B. Curis, X. Guillaud, F. Colas, et al., "HVDC meshed grid: Control and protection of a multi-terminal HVDC system," CIGRE, 2012.
[8] T. Lianxiang and O. Boon-Teck, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," IEEE Trans. Power Del., vol. 22, pp. 1877-1884, 2007.
[9] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," IEEE Trans. Power Electron., vol. 30, pp. 108-123, 2015.
[10] Y. Jin, J. E. Fletcher, and J. O'Reilly, "Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design," IEEE Trans. Power Del., vol. 25, pp. 2308-2318, 2010.
[11] Y. Jin, J. E. Fletcher, and J. O'Reilly, "Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables," IEEE Trans. Ind. Electron., vol. 59, pp. 3827-3837, 2012.
[12] J. Sneath and A. D. Rajapakse, "Fault Detection and Interruption in an Earthed HVDC Grid using ROCOV and Hybrid DC Breakers," IEEE Trans. Power Del., vol. PP, pp. 1-1, 2014.
[13] J. Marvik, D. S, and S. K, "Protection scheme for multi-terminal radial vsc hvdc system without communication between terminals," CIGRE, pp. 1-10, 2015.
[14] J. Wang, B. Berggren, K. Linden, and J. Pan, "Multi-terminal DC system line protection requirement and high speed protection solutions," CIGRE, pp. 1-9, 2015.
[15] R. Li, L. Xu, D. Holliday, F. Page, S. J. Finney, and B. W. Williams, "Continuous Operation of Radial Multiterminal HVDC Systems Under DC Fault," IEEE Trans. Power Del., vol. 31, pp. 351-361, 2016.
[16] D. Fujin and C. Zhe, "A Control Method for Voltage Balancing in Modular Multilevel Converters," IEEE Trans. Power Electron., vol. 29, pp. 66-76, 2014.
[17] Q. Jiangchao and M. Saeedifard, "Reduced Switching-Frequency Voltage-Balancing Strategies for Modular Multilevel HVDC Converters," IEEE Trans. Power Del., vol. 28, pp. 2403-2410, 2013.
[18] S. Gum Tae, L. Hee-Jin, N. Tae Sik, C. Yong-Ho, L. Uk-Hwa, B. Seung-Taek, et al., "Design and Control of a Modular Multilevel HVDC Converter With Redundant Power Modules for Noninterruptible Energy Transfer," IEEE Trans. Power Del., vol. 27, pp. 1611-1619, 2012.
[19] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits," IEEE Transactions on Power Delivery, vol. 30, pp. 385-394, 2015.
[20] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of HVDC Transmission System Topology on Multiterminal DC Network Faults," IEEE Trans. Power Del., vol. 30, pp. 844-852, 2015.
[21] R. Li, J. Fletcher, L. Xu, and B. Williams, "Enhanced Flat-Topped Modulation for MMC Control in HVDC Transmission Systems," IEEE Transactions on Power Delivery, vol. PP, pp. 1-1, 2016.
[22] N. R. Chaudhuri, R. Majumder, B. Chaudhuri, and P. Jiuping, "Stability Analysis of VSC MTDC Grids Connected to Multimachine AC Systems," IEEE Trans. Power Del., vol. 26, pp. 2774-2784, 2011.
[23] W. Wang, M. Barnes, and O. Marjanovic, "Droop control modelling and analysis of multi-terminal VSC-HVDC for offshore wind farms," in AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on, 2012, pp. 1-6.
[24] J. Song-Manguelle, M. H. Todorovic, R. K. Gupta, Z. Di, C. Song, L. J. Garces, et al., "A Modular Stacked DC Transmission and Distribution System for Long Distance Subsea Applications," Industry Applications, IEEE Transactions on, vol. 50, pp. 3512-3524, 2014.
[25] E. Kontos, "Control and Protection of VSC-based Multi-terminal DC Networks," TU Delft, Delft University of Technology, 2013.
[26] R. S. Geetha, R. Deekshit, and G. Lal, "Performance analysis of a voltage source converter HVDC system connected to an independent power generating station," in Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on, 2012, pp. 1-7.
[27] R. T. Pinto, S. F. Rodrigues, E. Wiggelinkhuizen, R. Scherrer, P. Bauer, and J. Pierik, "Operation and power flow control of multi-terminal DC networks for grid integration of offshore wind farms using genetic algorithms," Energies, vol. 6, pp. 1-26, 2012.
[28] X. Jianzhong, A. M. Gole, and Z. Chengyong, "The Use of Averaged-Value Model of Modular Multilevel Converter in DC Grid," IEEE Trans. Power Del., vol. 30, pp. 519-528, 2015.
[29] R. Zeng, L. Xu, L. Yao, S. J. Finney, and Y. Wang, "Hybrid HVDC for Integrating Wind Farms With Special Consideration on Commutation Failure," IEEE Transactions on Power Delivery, vol. 31, pp. 789-797, 2016.
[30] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, "Hybrid Cascaded Modular Multilevel Converter With DC Fault Ride-Through Capability for the HVDC Transmission System," IEEE Trans. Power Del., vol. 30, pp. 1853-1862, 2015.
[31] R. Li, L. Xu, L. Yao, and B. W. Williams, "Active Control of DC Fault Currents in DC Solid-State Transformers during Ride-Through Operation of Multi-Terminal HVDC Systems," IEEE Transactions on Energy Conversion, vol. PP, pp. 1-1, 2016.
[32] F. B. Ajaei and R. Iravani, "Enhanced Equivalent Model of the Modular Multilevel Converter," IEEE Trans. Power Del., vol. 30, pp. 666-673, 2015.
[33] Y. Feng, L. Weixing, W. Xitian, and X. Da, "Fast Voltage-Balancing Control and Fast Numerical Simulation Model for the Modular Multilevel Converter," IEEE Trans. Power Del., vol. 30, pp. 220-228, 2015.
[34] D. C. Ludois and G. Venkataramanan, "Simplified Terminal Behavioral Model for a Modular Multilevel Converter," IEEE Trans. Power Electron., vol. 29, pp. 1622-1631, 2014.
[35] W. Jun, R. Burgos, and D. Boroyevich, "Switching-Cycle State-Space Modeling and Control of the Modular Multilevel Converter," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 2, pp. 1159-1170, 2014.
[36] T. Eriksson, M. Backman, and S. Halen, "A low loss mechanical HVDC breaker for HVDC Grid applications," Proc. Cigré Session, Paris, France, 2014.
[37] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, et al., "HVDC circuit breakers for HVDC grid applications," in Proc. Cigré AORC Technical Meeting, Tokyo, Japan, 2014.
[38] E. Caro, A. J. Conejo, and A. Abur, "Breaker Status Identification," IEEE Trans. Power Sys., vol. 25, pp. 694-702, 2010.
[39] T. Lianxiang and O. Boon-Teck, "Protection of VSC-multi-terminal HVDC against DC faults," in Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual, 2002, pp. 719-724 vol.2.
[40] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetière, J. Jardini, and H. Saad, "The CIGRE B4 DC grid test system," Electra, vol. 270, pp. 10-19, 2013.

Rui Li received the M.S. and Ph.D degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2008 and 2013, respectively. Since 2013, he has been working as a research associate with University of Strathclyde in Glasgow, UK.

His research interests include HVDC transmiision system, grid integration of renewable power, power electronic converters, and energy conversion.



Lie Xu (M'03–SM'06) received the B.Sc. degree in Mechatronics from Zhejiang University, Hangzhou, China, in 1993, and the Ph.D. degree in Electrical Engineering from the University of Sheffield, Sheffield, UK, in 2000.

He is currently with the Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK. He previously worked in Queen's University of Belfast and ALSTOM T&D, Stafford, UK. His research interests include power electronics, wind energy generation and grid integration, and application of power electronics to power systems.

Liangzhong Yao (SM'12) received the M.Sc. and Ph.D. degrees in electrical power engineering from Tsinghua University, Beijing, China, in 1989 and 1993, respectively.

He joined the State Grid of China in 2011 and is now the Vice President of China Electric Power Research Institute (CEPRI), Beijing. He was a Postdoctoral Research Associate at the University of Manchester (formerly the University of Manchester Institute of Science and Technology), Manchester, U.K., from 1995 to 1999; a Senior Power System Analyst in the Network Consulting Department at ABB U.K. Ltd. from 1999 to 2004; and the Department Manager for Network Solutions, Renewables and Smart Grids Technologies at ALSTOM Grid Research & Technology Centre, Stafford, U.K., from 2004 to 2011.

Dr. Yao is a Chartered Engineer, a Fellow of the IET, and a member of CIGRE.