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**Suo, Zhiwen and Li, Gengyin and Xu, Lie and Li, Rui and Wang, Weisheng and Chi, Yongning (2016) Hybrid MMC based multi-terminal DC/DC converter with minimized FBSMs ratio considering DC fault isolation. IET Renewable Power Generation. ISSN 1752-1416 , <http://dx.doi.org/10.1049/iet-rpg.2016.0281>**

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# Hybrid MMC Based Multi-terminal DC/DC Converter with Minimized FBSMs Ratio Considering DC Fault Isolation

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**Abstract:** An isolated high-power multi-terminal DC/DC converter is studied in this paper, based on hybrid MMC configuration consisting of full-bridge submodules (FBSMs) and half-bridge submodules (HBSMs). To decrease the investment and power losses, a reduced arm FBSMs ratio (less than 0.5) scheme is adopted. A detailed analysis on the relationship of the DC/DC converter inner AC voltage and the arm FBSMs ratio under reduced DC voltage is presented. Based on this, a control strategy during DC fault is proposed which continues operating the converter connected to the faulty DC side with reactive current absorption. Under the same arm FBSMs ratio, compared to the conventional strategy of blocking the faulty side converter during a DC fault, the proposed unblocking method with reactive current injection can not only achieve greater DC fault current declining rate, but also ensure maximum power transfer between the interconnected healthy DC grids by maintaining a higher inner AC voltage in the DC/DC converter. The two strategies are compared and validated by simulations using PSCAD/EMTDC under different arm FBSMs ratio.

## 1. Introduction

It has been well accepted that HVDC technology is more attractive and likely to be the only feasible option for connecting large offshore wind farms over long distance. Compared to simple point-to-point DC transmission system, DC grid is expected to provide higher power supply reliability and equipment redundancy, more adaptable power supply mode, and more flexible and secure power flow control [1-3].

Although the prospect of DC grid offers many benefits, one of the main challenges is the interconnection of different DC networks. For connecting DC networks with different DC voltage levels and catering for the need of network protection and power flow control, DC/DC converters are required. Thus the development of DC/DC converters suitable for high power / high voltage application is one of the key challenges for implementing future multi-voltage levels, multi-terminal DC grid [4-6].

As the conventional DC/DC topologies designed for low or medium voltage and power range are not suitable for HVDC applications, many studies have been carried out on high-power high-voltage DC/DC converters for HVDC system [7-17]. Modular Multilevel Converter (MMC) is now the optimal technical solution for HVDC applications due to its significant advantages, e.g. industrial scalability, low single device switching frequency, superior harmonic performance, DC fault isolation capability, etc.,[18]. A modular multilevel DC/DC converter with bidirectional fault blocking capability is presented in [9], which uses multiple interleaved strings of cascaded submodules (SMs) to perform single-stage bidirectional DC/DC conversion, offering a substantial improvement in utilization of total installed SM rating. However, extremely large output filter inductance may have to be installed to eliminate the fundamental AC component. A similar topology with bidirectional interrupting DC currents capability has been presented in [10]. The proposed high voltage DC auto transformer is also a single-stage converter consisting of two series connected voltage source converters with an AC link allowing energy transfer between the upper and lower converters, where the sum of the two DC voltages forms the high level DC voltage and the lower converter forms the low level DC voltage. This leads to significant cost reduction, though its lacking of galvanic isolation may limit its application in HV grid.

If two MMCs are connected front-to-front through an AC transformer, they can also operate as a bidirectional DC/DC converter. Such a converter topology has been reported in [13], which uses a particular modulation strategy where both MMCs contribute to the voltage elevation besides the AC transformer stage. The use of medium frequency transformation reduces the volume of passive components. However, the transformer is subject to high  $dv/dt$  at the rising and falling edges of the square waveform AC link voltage leading to increased technical requirements and costs. To avoid this problem, a quasi two-level (Q2L) DC/DC converter has been proposed in [14], where the converter generates a square wave with controllable  $dv/dt$  by employing the SM voltages to create transient intermediate voltage level.

This significantly reduces the size of the capacitors used in the SMs compared to conventional MMC.

Soft-switching characteristics of the Q2L DC/DC converter is then analyzed in [15] and [16].

Although the front-to-front configuration can handle DC fault by blocking both sides of the MMCs, for a multi-terminal DC/DC converter interconnecting more than two DC grids, DC fault on one grid will cause the blocking of all the MMCs in the DC/DC converter, affecting the power transfer between the healthy DC grids in a multi-section HVDC interconnection system [19].

Recently, the hybrid MMC design concept has been proposed which combines different SM topologies in order to optimize converter performances [19-25]. A three-terminal DC/DC converter based on a simplified hybrid MMC configuration is proposed in [19]. Different from the basic hybrid MMC with half FBSMs and half HBSMs per arm [22], this MMC structure is a simplified configuration with less semiconductor devices, but also has the advantage of being able to block the DC/DC converter terminal connected to faulty DC grid, while continues operating the other terminals connected to healthy DC grids. By utilizing the FBSMs negative level output, the converter can achieve continued operation without converter blocking during a DC fault [25-27]. A STATCOM operation scheme of the MMC adopting clamp double submodule (CDSM-MMC) is also proposed in [26] with arms alternately turned on.

So far, the researchers are mainly focusing on the hybrid MMC configuration with arm FBSMs ratio (the ratio of FBSMs to the total number of SMs per arm) greater than (e.g. the Boost FBSM-MMC presented in [25] with a ratio of 0.67) or equal to 0.5. If the ratio decreases further, the conduction losses and investment can be further reduced. However, the number of the FBSMs for fault blocking may become insufficient and thus, extra control strategy needs to be designed to isolate the fault accordingly.

This paper proposes a DC fault isolation strategy, i.e. converter unblocking with additional reactive current injection for multi-terminal DC/DC converter based on hybrid MMC with reduced arm FBSMs ratio (less than 0.5). Compares with conventional converter blocking strategy, by unblocking the faulty side converter with reactive current injection, the converter can be designed to use fewer semiconductor

This paper is a post-print of a paper submitted to and accepted for publication in IET Renewable Power Generation and is subject to Institution of Engineering and Technology Copyright. The copy of record is available at IET Digital Library. devices and have lower power losses, and to achieve faster fault isolation during a DC fault with less impact on the healthy grids. The proposed strategy is verified by a three-terminal DC test system using PSCAD/EMTDC simulation.

## 2. Hybrid MMC Based DC/DC Converter Design Principle

### 2.1. Basic Configuration

Fig. 1a presents a three-terminal DC/DC converter comprising three hybrid MMCs interconnected by two two-winding transformers. Taking hybrid MMC<sub>2</sub> as an example to demonstrate the converter configuration, each arm is a combination of F FBSMs and (N-F) HBSMs, where N is the SM number per arm.  $U_{dc2n}$  is the nominal DC-link voltage,  $L_2$  is the arm inductance, and  $U_{c2}$  is the nominal SM capacitor voltage.  $u_{pj2}$  and  $u_{nj2}$  ( $j=a,b,c$ ) are the output voltages of the upper and lower arms respectively and the equivalent output phase voltage  $e_{j2}$  is then expressed as  $(u_{nj2}-u_{pj2})/2$ . The arm currents of the upper and lower arms are respectively denoted as  $i_{pj2}$  and  $i_{nj2}$ , and  $i_{j2}$  is the input AC phase current.

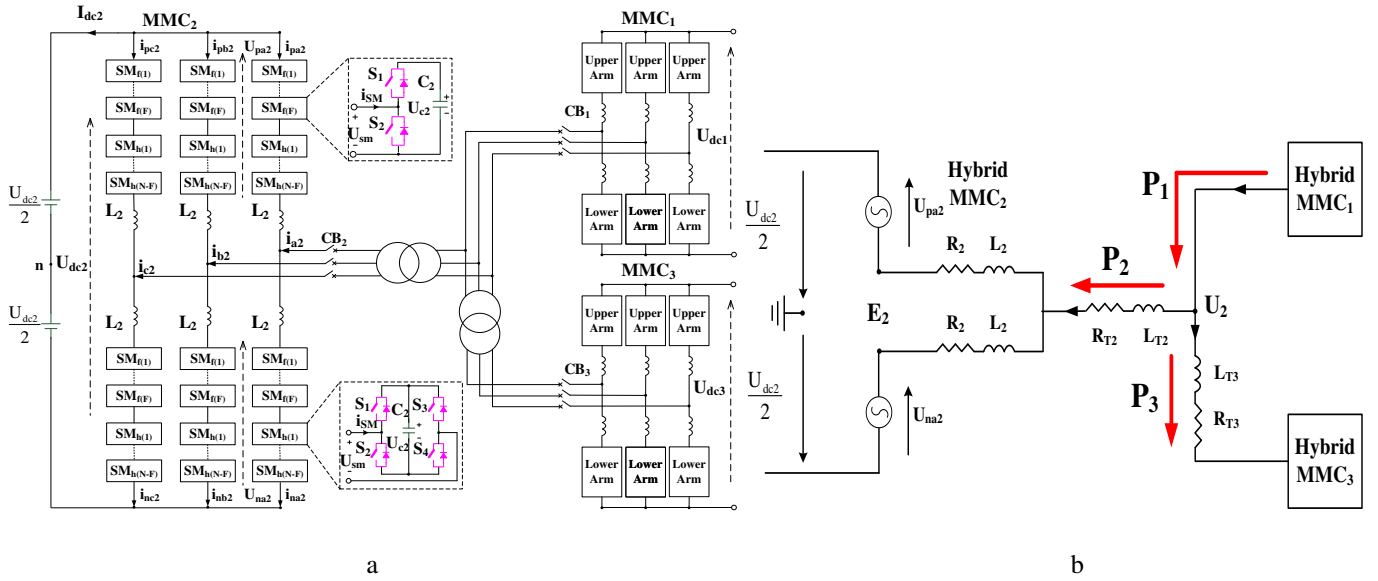
Assuming the SM capacitor voltages are balanced at the nominal value, the arm voltage is in the range of  $0 \sim NU_{c2}$ , without utilizing the negative voltage generating capability of the FBSMs [22]. Thus, the nominal DC and AC phase peak voltages at the maximum modulation of 1 are expressed as

$$\begin{cases} U_{dc2n} = NU_{c2} \\ E_m = \frac{NU_{c2}}{2} = \frac{U_{dc2n}}{2} \end{cases} \quad (1a)$$

In some occasions, HVDC systems need to be operated at reduced DC voltages, e.g. DC-based deicing or during a DC fault. If the AC phase peak voltage remains unchanged from  $E_m$ , some of the FBSMs can be used to generate  $-U_{c2}$  state in each arm so as to reduce the DC voltage. The arm voltage is in the range of  $-k_2NU_{c2} \sim NU_{c2}$  and the minimum DC voltage the converter can operate is given as

$$U_{dc2min} = (1 - 2k_2)U_{dc2n} \quad (1b)$$

where  $k_2$  is the ratio of FBSMs to the total number of SMs per arm and equals  $F/N$ . Similar relationship



**Fig. 1. Hybrid MMC based multi-terminal DC/DC converter**  
a Configuration of the hybrid MMC based DC/DC converter  
b Equivalent Circuit for the hybrid MMC based DC/DC converter

Under normal operation, one MMC in the hybrid MMC based DC/DC converter operates as a voltage source to generate an inner AC voltage with constant amplitude and frequency, and the other MMCs control the power flows between the inner AC sides and connected DC terminals [19]. Defining  $U_2$  (line-to-line rms voltage) shown in Fig. 1b as the inner AC voltage, which is converted to the terminal voltage level of MMC<sub>2</sub>, when a DC pole-to-pole fault happens on one side of the connected DC grid, depending on the arm voltage produced by the FBSMs, the inner AC voltage of the multi-terminal DC/DC converter may have to be reduced accordingly in order to prevent over current feeding from the AC side. However, the inner AC voltage of the DC/DC converter should also be kept as high as possible to ensure maximum active power exchange between the healthy DC grids. In order to achieve the minimum arm FBSMs ratio, assuming the inner AC voltage of the DC/DC converter is controlled by hybrid MMC<sub>1</sub> to  $U_2$ , the relationship between  $U_2$  and the equivalent output voltage  $E_2$  (line-to-line rms voltage) generated by MMC<sub>2</sub> can be derived according to the positive current direction shown in Fig.1b as

$$E_2 = \sqrt{(U_2 - \Delta U'_2)^2 + (\delta U'_2)^2} \quad (2)$$

$$\Delta U'_2 = \sqrt{3}(R_{eq} I_p + X_{eq} I_Q); \delta U'_2 = \sqrt{3}(X_{eq} I_p - R_{eq} I_Q) \quad (3)$$

where  $I_p$  and  $I_Q$  are the active and reactive phase rms current of MMC<sub>2</sub>,  $R_{eq}$  and  $X_{eq}$  are the equivalent resistance and reactance (sum of arm and transformer leakage reactance referred to MMC<sub>2</sub> AC side).

Neglecting the resistance, under a certain inner AC voltage  $U_2$  and reduced DC voltage  $U'_{dc2}$ , the required minimum arm FBSMs ratio for MMC<sub>2</sub> can be expressed as

$$k_2 = \frac{E_{j2peak} - \frac{U'_{dc2}}{2}}{U_{dc2n}} = \frac{\sqrt{24(U_2 - \sqrt{3}X_{eq}I_Q)^2 + 72(X_{eq}I_p)^2} - 3DU_{dc2n}}{6U_{dc2n}} \quad (4)$$

where  $E_{j2peak}$  is the equivalent output phase peak voltage,  $D$  is the ratio between the reduced and nominal DC voltages and is given as  $U'_{dc2}/U_{dc2n}$ . Similar relationship can also be derived using equation (19) in [28] by setting  $k_{MMC}=1$ .

Equation (4) indicates  $k_2$  can be reduced (i.e. less FBSM) by injecting extra positive reactive current (increase  $I_Q$  in (4)) into MMC<sub>2</sub>, leading to reduced investment and conduction losses of MMC<sub>2</sub> during normal operation. The same concept can be equally applied to the hybrid MMC<sub>1</sub> and MMC<sub>3</sub>.

## 2.2. Arm Current and Capacitor Voltage Balancing Consideration

As the MMCs have limited current capability, under reduced DC voltage a corresponding reduction in active power (current) must be simultaneously applied. Defining the ratio of the active power flowing into hybrid MMC<sub>2</sub> under reduced and nominal DC voltage as  $n$ , and neglecting converter power losses, the three-phase AC and DC powers under reduced DC voltage are

$$P'_{dc2} = nP_2 = DU_{dc2n}I'_{dc2} = \frac{3}{2}E_m I'_m \cos \varphi \quad (5)$$

where  $I'_{dc2}$ ,  $I'_m$  are the DC and phase peak current under reduced DC voltage,  $\varphi$  is the power factor angle,  $P_2$  is the nominal active power transfer between the AC and DC sides of the hybrid MMC<sub>2</sub>.

The upper and lower arm currents under reduced DC voltage can be expressed as (6), considering the DC and fundamental AC components [22]:

$$\begin{cases} i_{pj2} = -\frac{I'_{dc2}}{3} - \frac{I'_m}{2} \cos(\omega t - \varphi) \\ i_{nj2} = -\frac{I'_{dc2}}{3} + \frac{I'_m}{2} \cos(\omega t - \varphi) \end{cases} \quad (6)$$

The peak arm current is

$$\hat{I}_{arm} = \frac{I'_{dc2}}{3} + \frac{I'_m}{2} \quad (7)$$

Assuming  $I_{peak}$  is the maximum allowed arm current considering the semiconductor device's current capability, to ensure safe operation of the converter, the following equation must be satisfied:

$$\hat{I}_{arm} \leq I_{peak} \quad (8)$$

Substituting (5) and (7) into (8), the necessary active power reduction ratio can be derived as

$$n \leq \frac{3DU_{dc2n} \cos \varphi I_{peak}}{(2D + \cos \varphi) P_2} \quad (9)$$

Equation (9) shows the maximum active power reduction ratio under a reduced DC voltage to ensure continuous operation of the multi-terminal DC/DC converter. It should be noted that the ratio would be further reduced by considering the increased reactive current in order to reduce the required FBSMs per arm.

Due to the increase of DC current under reduced DC voltage, thereby the reduced discharging time, the arm currents must maintain both positive and negative within one fundamental period to avoid HBSMs capacitor voltages unbalance [22]. Thus the DC and AC currents need to meet the following requirement

$$\frac{I'_{dc2}}{3} \leq \frac{I'_m}{2} \quad (10)$$

Substituting (5) into (10), the required power factor can be derived as

$$\cos \varphi \leq 2D \quad (11)$$



Equation (11) indicates the power factor may decrease accordingly under reduced DC voltage, which implies that reactive current will be needed to ensure enough discharging time for HBSMs to ensure capacitor voltage balancing.

The capacitor voltage balancing strategy for the hybrid MMC based DC/DC converter, which uses similar principles as conventional HBSM based MMC when  $N_{on}$  (the number of inserted SM) is positive, with all the SMs participating in the regulation of capacitor voltage balancing. When  $N_{on}$  is negative, only FBSMs are involved in the capacitor voltage balancing process [22].

### 3. DC Fault Isolation Strategies of the Hybrid MMC Based DC/DC Converter

A DC pole-to-pole fault is one of the most serious faults that must be considered for HVDC design and operation, and has significant impacts on device parameters, control strategies and protection configurations. An unblocking DC fault isolation strategy is proposed in the paper, which allows for continuous operation of the faulty side converter with active control of its reactive current injection. As a comparison, the conventional fault isolation method of blocking the faulty side converter during a fault with coordinated control of inner AC voltage will also be briefly introduced.

#### 3.1. Blocking of the faulty side converter

After a DC pole-to-pole fault, if the series-connected voltage of the FBSMs, which are inserted into the fault current path, is higher than the peak AC line-to-line voltage, the DC fault can be isolated following the blocking of the converter [22]. Base on this, the minimum FBSMs number per arm required to isolate the DC fault can then be determined.

Base on (1a), the following relationship should be satisfied to block the DC pole-to-pole fault [29]:

$$2U_{arm} \geq E_{l-1max} = \frac{\sqrt{3}U_{dc2n}}{2} = \frac{\sqrt{3}NU_{c2}}{2} \quad (12)$$

$2U_{arm}$  is the sum of the upper arm FBSMs voltage on one phase and the lower arm FBSMs voltage on another phase.  $E_{l-1max}$  is the peak line-to-line voltage applied at the converter AC terminals.

The required minimum arm FBSMs ratio to ensure successfully blocking the DC fault can be determined [29]

$$k_2 \geq \frac{\sqrt{3}}{4} \quad (13)$$

By blocking hybrid MMC<sub>2</sub>, hybrid MMC<sub>3</sub> can maintain normal operation and transmit original active power from AC to DC side. However, if  $k_2$  is further reduced (e.g. for cost reduction), the DC fault cannot be isolated simply by blocking the faulty side converter.

Unlike the AC/DC converter, the inner AC voltage of the hybrid MMC based DC/DC converter can be actively controlled by hybrid MMC<sub>1</sub>. To ensure the DC fault at hybrid MMC<sub>2</sub> can be blocked, the maximum allowed inner AC line-to-line rms voltage can be determined as

$$U_2 = \sqrt{2}k_2U_{dc2n} \quad (14)$$

To implement this strategy, hybrid MMC<sub>1</sub> can be switched to active control mode after detecting DC over-current on hybrid MMC<sub>2</sub>. The detection time delay can be negligible because communications are all within the DC/DC converter. However, under such condition, the active power flowing through hybrid MMC<sub>3</sub> will be reduced due to the reduction of the inner AC voltage.

### 3.2. Unblocking of the faulty side converter

When the DC voltage drops to zero as the result of DC fault on MMC<sub>2</sub>, there is no active power exchange between its AC and DC sides. By substituting  $D = 0$  and  $I_p = 0$  in (4), the controlled inner AC voltage is given as:

$$U_2 = \sqrt{3}X_{eq}I_Q + \frac{\sqrt{6}k_2U_{dc2n}}{2} \quad (15)$$

Equation (15) indicates that allowing MMC<sub>2</sub> to absorb a certain amount of reactive power into the converter can raise the inner AC voltage to a higher level, thus ensuring maximum active power exchange between MMC<sub>1</sub> and MMC<sub>3</sub>. As the arm current in hybrid MMC<sub>2</sub> only contains reactive current, previously

mentioned HBSCMs charging problem will not exist as there are always sufficient charging and discharging times due to the zero DC offset in the arm current.

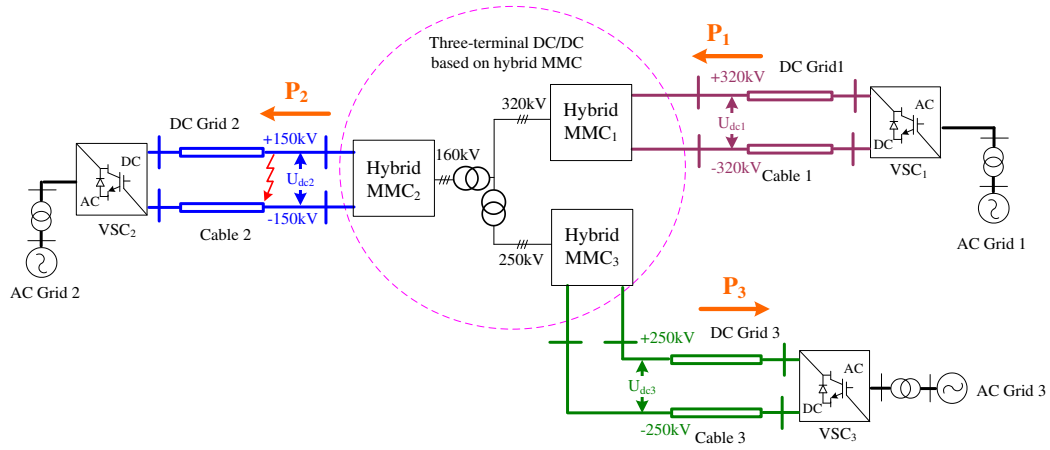
However, under such a condition, a small amount of energy is still required from the AC side of the MMC<sub>2</sub> to compensate the converter power losses to ensure the SM capacitor voltages are maintained at the rated values. Thus, a SM capacitor voltage balance controller is added. The complete control diagram of the hybrid MMC<sub>2</sub> during DC faults is shown in Fig. 2,  $\omega$  is the rated angular frequency, and the frequency can be chosen higher than 50Hz, e.g. 350Hz, to reduce the volume [12]. The SM capacitor average voltage is compared with the required SM reference value, which is used as an input to produce a d-axis reference  $i_d^*$  for active power. While the q-axis reference  $i_q^*$  for reactive power is set directly without the outer loop (within the maximum value 1p.u.). Its purpose is to keep  $U_2$  close to its original value to ensure maximum active power transfer between the healthy MMC<sub>1</sub> and MMC<sub>3</sub>.

It should be emphasized that the additional reactive current absorbed by the faulty side converter during the fault has to be provided by the remaining healthy converters, which could affect their active power transmission capability due to their current limitation. For instance, assuming the rated capacities of MMC<sub>1</sub>, MMC<sub>2</sub> and MMC<sub>3</sub> are 1p.u., 0.5p.u., and 0.5p.u., respectively, when a DC pole-to-pole fault happens at MMC<sub>2</sub>, it absorbs full capacitive current of 0.5 p.u.. Under such a condition, the required reactive current can be entirely provided by MMC<sub>1</sub> without affecting the active power transmission between MMC<sub>1</sub> and MMC<sub>3</sub> (maximum 0.5 p.u. active power). However, if a DC pole-to-pole fault happens at MMC<sub>1</sub>, considering the limitations of the arm current and converters capacity, the DC power transfer between MMC<sub>2</sub> and MMC<sub>3</sub> will need to be reduced to less than 0.5 p.u., and the reactive current absorbed by MMC<sub>1</sub> during the DC fault can be equally distributed between MMC<sub>2</sub> and MMC<sub>3</sub>. The strategy can also be applied to multi-terminal DC/DC converter, and the needed reactive current during DC fault condition can be provided by the healthy converters according to their rated capacities.



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#### 4. Comparison of the Fault Isolation Strategies



**Fig. 3. Three-terminal DC test system**

The proposed fault isolation strategy is compared with the conventional blocking strategy, taking the three-terminal DC test system shown in Fig. 3 as an example. The parameters of the test system are listed in Table 1. It should be noted that the capacitor reference voltage of hybrid MMC<sub>2</sub> can be set to 25kV to accelerate the simulation time without significantly affecting the quality of the outcome [23, 30, 31].

**Table 1** Nominal parameters of the three-terminal DC test system

| Component   | Value                            |
|---|----------------------------------|
| Hybrid MMC <sub>1,2,3</sub> rated power                   | 1000MW,500MW,500MW               |
| AC-side voltage1, 2, 3 (nominal line-to-line rms voltage) | 320kV,160kV,250kV                |
| DC-side voltage1,2,3                                      | 640kV,300kV,500kV                |
| Number of SMs per arm (hybrid MMC <sub>2</sub> )          | 12                               |
| Capacitor reference voltage (hybrid MMC <sub>2</sub> )    | 25kV                             |
| SM capacitor(hybrid MMC <sub>2</sub> )                    | 1000 μF                          |
| Number of SMs per arm (hybrid MMC <sub>2</sub> )          | 25kV                             |
| Inductance per arm( hybrid MMC <sub>2</sub> )             | 0.2 p.u. (Based on 160 kV/500MW) |
| AC transformer inductance ( hybrid MMC <sub>2</sub> )     | 0.2 p.u.                         |

According to (14) and (15), the relationships between the FBSMs ratio  $k_2$  and the inner AC voltage  $U_2$  for the two DC fault isolation strategies, i.e. converter blocking and unblocking are now rewritten as

$$\begin{cases} k_2 = \frac{\sqrt{2}}{2U_{dc2n}}U_2 \\ k_2 = \frac{\sqrt{6}}{3U_{dc2n}}U_2 - \frac{\sqrt{2}X_{eq}I_Q}{U_{dc2n}} \end{cases} \quad (17)$$

Fig. 4 shows the inner AC line-to-line rms voltage (p.u.) as the function of the arm FBSMs ratio under the different fault isolation strategies during a DC pole-to-pole fault.

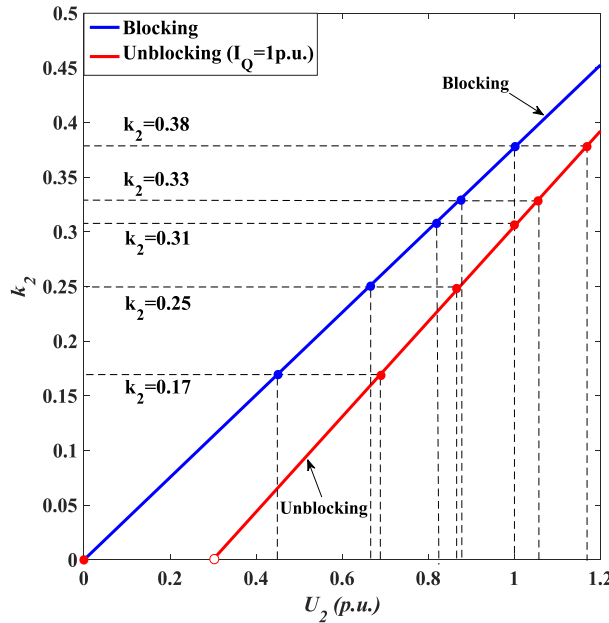


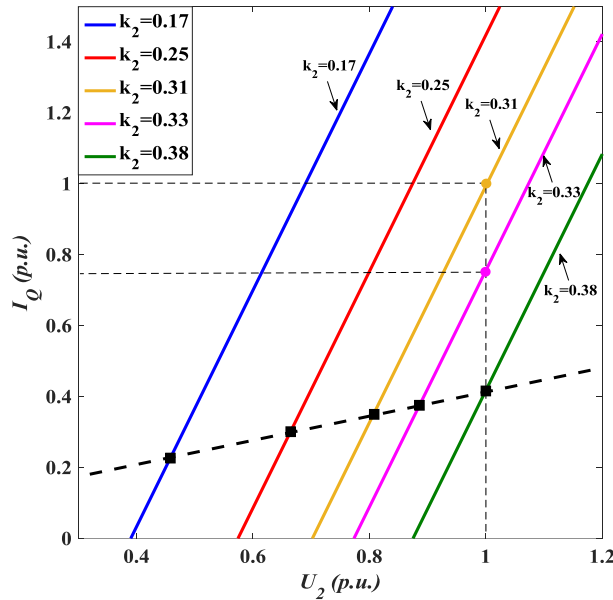
Fig. 4. Relationship of  $k_2$  and  $U_2$  adopting different fault isolation strategies

As shown in Fig. 4, under the same arm FBSMs ratio  $k_2$ , unblocking of the fault side converter with 1 p.u. reactive current injection can achieve higher  $U_2$  compared to that of converter blocking. This means that for the same  $k_2$ , more active power can be transmitted between DC grid 1 and 3 ( $MMC_1$  and  $MMC_3$ ) with converter unblocking as the inner AC voltage amplitude can remain at a higher value than simply blocking the converter.

Due to the low probability of DC pole-to-pole fault, a criterion of active power reduction ratio (namely  $U_2$  reduction ratio) between the healthy DC grids in case of one adjacent DC grid fault may be set

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up in advance according to the system requirement. The required arm FBSMs ratio  $k_2$  for the hybrid MMC<sub>2</sub> can then be obtained according to (17). For instance,  $U_2$  is set as 0.8 p.u. in case of DC faults, which means the active power transmission between the healthy DC grids will be restricted to 0.8 p.u.. The values of  $k_2$  according to (17) are 0.30 with converter blocking and 0.22 for the case of converter unblocking with 1 p.u. reactive current injection, respectively. This means that with the proposed unblocking strategy, the required number of FBSMs can be reduced compared to simply blocking the converter during a DC fault, leading to reduced power losses during normal operation and cost. As shown in Fig. 4, if  $U_2$  is set at 1 p.u., the corresponding arm FBSMs ratio  $k_2$  are 0.38 and 0.31, respectively for converter blocking and unblocking.



**Fig. 5. Relationship of  $I_Q$  and  $U_2$  adopting the unblocking strategy under different  $k_2$**

Without blocking the converter, Fig. 5 shows the inner AC line-to-line rms voltage (p.u.) as the function of the reactive current injection (p.u.) under different arm FBSMs ratio. The x-axis values of the square dots represent the inner AC voltages that can be achieved with the relevant  $k_2$  when the faulty side converter is blocked. As can be seen, under a certain  $k_2$ , the blocking strategy can achieve nearly 15% higher inner AC voltage  $U_2$  than the unblocking strategy without reactive current injection. However, when the injected reactive current is higher than the bold dashed line formed by the square dots shown in

Fig. 5, the unblocking strategy has more advantage over the blocking strategy. It can be seen that under a certain  $k_2$ , the bigger the reactive current injection is, the higher the inner AC voltage can remain. Also, under the same  $U_2$ , smaller  $k_2$  is required with higher reactive current injection.

**Table 2** Impact of  $k_2$  variation on  $U_2$  utilizing different fault isolation strategies

| Strategies   | $k_2$ |      |      |      |      |      |
|--|-------|------|------|------|------|------|
|  | $U_2$ | 0.17 | 0.25 | 0.31 | 0.33 | 0.38 |
| <b>Blocking</b>  |       | 0.44 | 0.66 | 0.82 | 0.88 | 1.00 |
| <b>Unblocking1<br/>(<math>I_Q=0.764\text{p.u.}</math>)</b> |       | 0.61 | 0.80 | 0.94 | 1.00 | 1.10 |
| <b>Unblocking2<br/>(<math>I_Q=1\text{p.u.}</math>)</b>     |       | 0.68 | 0.87 | 1.00 | 1.06 | 1.17 |

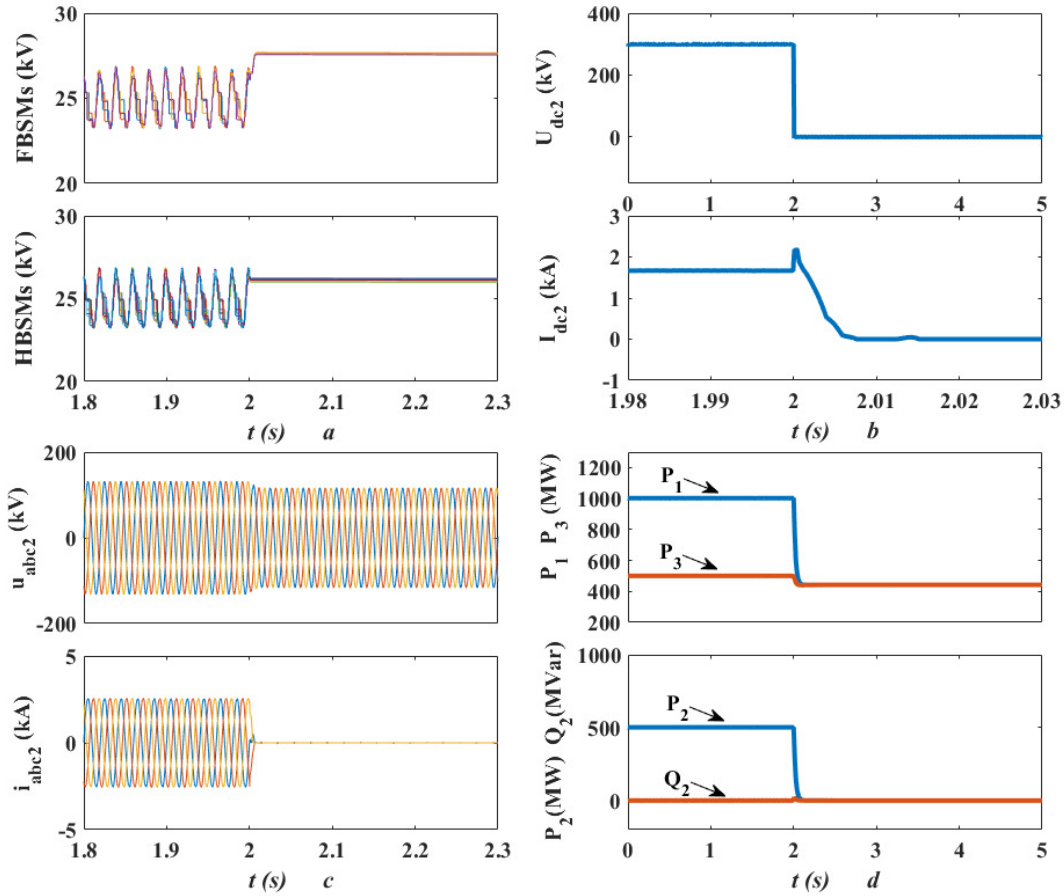
Table 2 shows the impact of  $k_2$  variation on  $U_2$  utilizing different proposed fault isolation strategies for a few specific cases. Due to different slopes of the curves, the inner AC voltage boost effect for unblocking scheme is more obvious under smaller  $k_2$ . Also, the minimum arm FBSMs ratio can be achieved by maximum reactive current injection (e.g. 1p.u.). For example,  $U_2$  can remain at the nominal value by absorbing 0.764 p.u. reactive current into the converter with  $k_2$  being 0.33, compared to  $k_2$  being 0.38 when the converter is blocked. The  $k_2$  can be further reduced to 0.31 by absorbing 1 p.u. reactive current.

## 5. Simulation results

To verify the proposed fault isolation strategies, a three-terminal DC test system containing a hybrid MMC based DC/DC converter shown in Fig. 3 is developed using the parameter listed in Table 1. Average model is adopted for hybrid MMC<sub>1</sub> and MMC<sub>3</sub> to accelerate the simulation speed [19], whereas a more detailed model of hybrid MMC<sub>2</sub> is built with a total of 12 SMs per arm comprising  $12k_2$  FBSMs and  $12(1-k_2)$  HBSMs. Each SM has a capacitance of  $1000\mu\text{F}$  and is rated at 25kV. The nominal inner AC voltage  $U_2$  is controlled by hybrid MMC<sub>1</sub> to 160kV, with a frequency of 50Hz. In order to achieve greater DC fault current decline rate, the preset DC current reference  $I_{dc2ref}$  shown in Fig. 2 is set to half of the nominal DC



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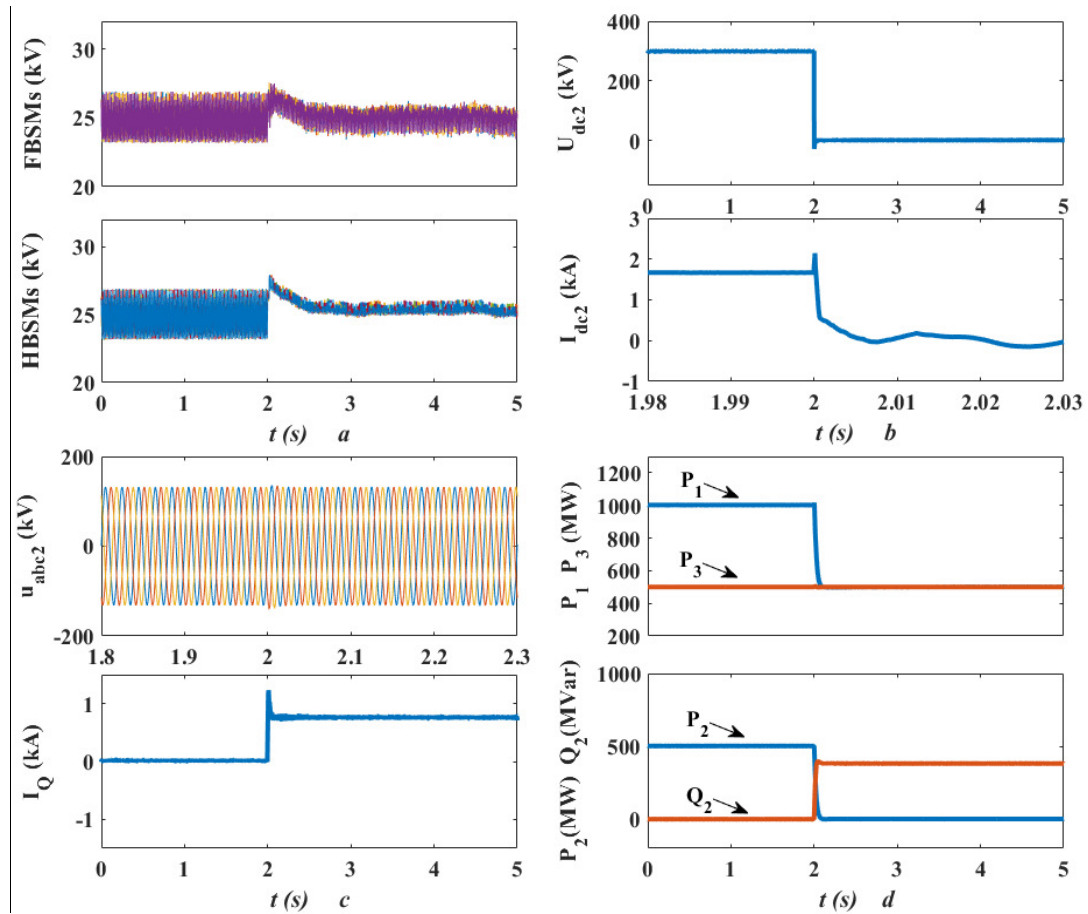
**Fig. 6. Simulation results for blocking of the hybrid MMC<sub>2</sub> under a DC pole-to-pole fault when  $k_2=0.33$**

- a MMC<sub>2</sub> SMs capacitor voltages
- b MMC<sub>2</sub> DC terminal voltage and current
- c MMC<sub>2</sub> AC voltage and current
- d Active power of MMC<sub>1,2,3</sub> and reactive power of MMC<sub>2</sub>

Fig.6 shows the simulation results for blocking of the hybrid MMC<sub>2</sub> during fault when  $k_2$  equals 0.33 (FBSM: HBSM=1:2). As illustrated in Fig. 6, a permanent DC pole-to-pole fault is initiated at the hybrid MMC<sub>2</sub> DC terminal at 2s. After detecting the DC current exceeding the threshold value (1.2p.u.), all the IGBTs in the hybrid MMC<sub>2</sub> are blocked, and active control of hybrid MMC<sub>1</sub> is activated by controlling the inner AC voltage to 0.88p.u. to ensure that no AC fault current flows through MMC<sub>2</sub> to the faulty DC side. This causes the active power flowing into DC grid 3 to reduce from 500MW to 442MW. Meanwhile, the DC current at MMC<sub>2</sub> drops quickly down to zero with  $\Delta t$  being 3ms, where  $\Delta t$  is the time interval for the

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fault current decaying from peak to preset DC current reference value. The FBSMs capacitor voltages in MMC<sub>2</sub> increase from the nominal value of 25kV to 27.6kV due to the initial charging from the AC side.



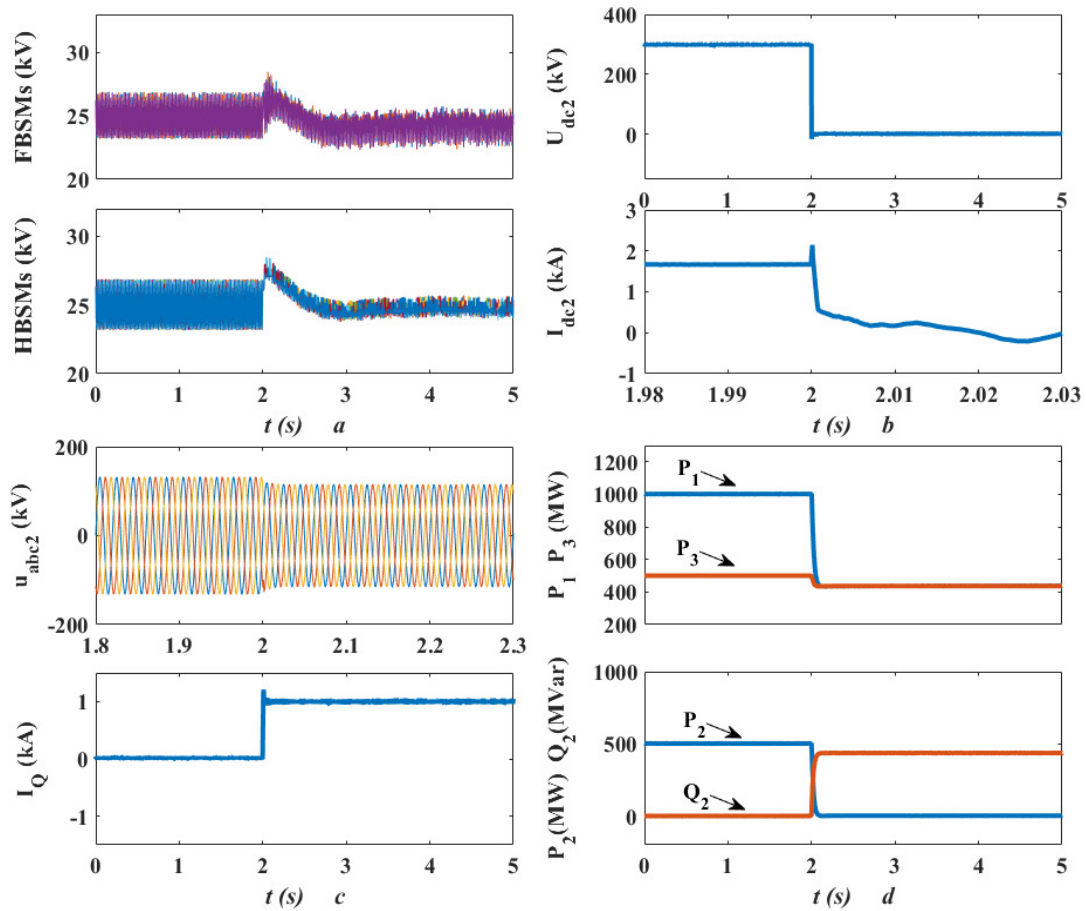
**Fig. 7. Simulation results for unblocking of the hybrid MMC<sub>2</sub> under a DC pole-to-pole fault when  $k_2=0.33$**

- a MMC<sub>2</sub> SMs capacitor voltages
- b MMC<sub>2</sub> DC terminal voltage and current
- c MMC<sub>2</sub> AC voltage and reactive current (positive for flowing into MMC<sub>2</sub>)
- d Active power of MMC<sub>1,2,3</sub> and reactive power of MMC<sub>2</sub>

Fig.7 shows the simulation results without blocking hybrid MMC<sub>2</sub> under the same  $k_2$ . The DC voltage quickly drops to zero after the fault, and the active power flowing into hybrid MMC<sub>2</sub> reduces to zero accordingly. Compared with the conventional blocking scheme, the inner AC voltage can remain unchanged after fault (i.e.  $U_2$  remains at 1 p.u.) by absorbing 0.764p.u. reactive current (i.e. 382MVar reactive power) into MMC<sub>2</sub>. Consequently, active power transmission to DC grid 3 is not affected. Negative level output at the hybrid MMC<sub>2</sub> DC terminal can also be seen due to the function of added closed-loop DC inrush current controller, which accelerates the DC current reduction with  $\Delta t$  of 0.4ms,

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being one-seventh the time of conventional blocking scheme. Also, the FBSMs and HBSMs capacitor voltages slightly deviate from the reference value when the DC fault happens, and then gradually return to normal values due to the effect of the added capacitor voltage balance controller. It demonstrates that the proposed unblocking of the fault side converter with reactive current injection scheme can not only block the DC fault more quickly, but also continue operating to regulate the inner AC current, ensuring the maximum active power transfer between the healthy grids. This feature shows excellent DC fault ride-through capability of the hybrid MMC based multi-terminal DC/DC converter.



**Fig. 8.** Simulation results for unblocking of the hybrid MMC<sub>2</sub> under a DC pole-to-pole fault when  $k_2=0.25$

- a MMC<sub>2</sub> SMs capacitor voltages
- b MMC<sub>2</sub> DC terminal voltage and current
- c MMC<sub>2</sub> AC voltage and reactive current (positive for flowing into MMC<sub>2</sub>)
- d Active power of MMC<sub>1,2,3</sub> and reactive power of MMC<sub>2</sub>

Fig. 8 shows the simulation results for unblocking of the hybrid MMC<sub>2</sub> under a DC pole-to-pole fault when  $k_2$  equals 0.25 (FBSM: HBSM=1:3). By absorbing 1 p.u. reactive current (i.e. 435MVar reactive power) into the faulty side converter, the inner AC voltage can be raised to 0.87p.u. with coordinate control of hybrid MMC<sub>1</sub> and MMC<sub>2</sub>, which is nearly the same value compared with the conventional blocking scheme when  $k_2$  equals 0.33. It implies that by fully utilizing the faulty side converter capacity, the active power flowing into the DC grid 3 can be maintained at the same level but using less FBSMs, leading to reduced power losses and cost.

## 6. Conclusions

A high power multi-terminal DC/DC converter based on hybrid MMC with DC fault blocking capability for interconnecting large HVDC systems has been studied in this paper. A converter unblocking strategy during a DC fault is proposed, which allows for continuous operation of the faulty side converter with active control of its reactive current injection. The proposed method is compared to the conventional fault isolation method of blocking the faulty side converter during a DC fault. Simulations are carried out to validate the effectiveness of the proposed strategy. The results show that the proposed scheme of unblocking the faulty side converter with a certain amount reactive current injection can achieve faster DC fault isolation and has less impact on the healthy grids when compared with the conventional blocking strategy. The proposed fault isolation scheme allows for significant economy savings for hybrid MMC based DC/DC converter due to the reduced arm FBSMs ratio, making it possible to be employed in the future multi-terminal DC grid with different voltage levels.

## 7. Acknowledgments

This work was supported in part by the National High Technology Research and Development Program of China (863 Program) under Grant 2015AA050101.

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