

Design and fabrication of diffractive atom chips for laser cooling and trapping

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Abstract It has recently been shown that optical reflection gratings fabricated directly into an atom chip provide a simple and effective way to trap and cool substantial clouds of atoms (Nshii et al. in *Nat Nanotechnol* 8:321–324, 2013; McGilligan et al. in *Opt Express* 23(7):8948–8959, 2015). In this article, we describe how the gratings are designed and microfabricated and we characterise their optical properties, which determine their effectiveness as a cold atom source. We use simple scalar diffraction theory to understand how the morphology of the gratings determines the power in the diffracted beams.

1 Introduction

Atom chips [3, 4] are microfabricated devices [5] which control and manipulate ultracold atoms in a small, integrated package. Because they provide a convenient way to trap [6–9], guide [3, 10] and detect atoms [11], atom chips are becoming increasingly important for clocks [12, 13], Bose–Einstein condensates [14–16], matter wave interferometers [17–20] and quantum metrology [20]. In recent years, there has been great progress towards integrating a

wide range of optical, electric and magnetic elements into atom chips, but the magneto-optical trap (MOT) [21, 22]—the element responsible for initial capture and cooling of the atoms—has remained external to the chip.

An early attempt to integrate the MOT used deep pyramidal mirrors etched into a thick silicon substrate [8]. These manipulate a single incident laser beam into the overlapping beams required by a MOT. With beams of size L , the number of atoms captured scales as L^6 [9], a dependence that rolls over to $L^{3.6}$ as the size increases to some centimetres [21]. The large pyramids favoured by this scaling are not compatible with the normal 500 μm thickness of a silicon wafer. Although thick wafers are available, days of etching are needed to make pyramids of mm size and additional polishing is required to achieve optical quality surfaces [8, 23, 24]. For these reasons, the integrated pyramid is unsuitable for applications requiring more than $\sim 10^4$ atoms. Figure 1 illustrates a recent extension of this idea where the MOT beams are now formed using microfabricated diffraction gratings, which replace the sloping walls of the pyramid [25, 26]. The gratings are easily fabricated on any standard substrate material and can readily be made on the centimetre scale. This allows the MOT to capture up to 10^8 atoms above the surface of the chip, where they can be conveniently transferred to magnetic traps [3]. Because they only need a small depth of etching, the gratings preserve the 2D nature of the structure and sit comfortably with other elements on the chip. Alternatively, for devices that only require the reliable production of a MOT, the grating chip can be placed outside the wall of a glass cell and used to trap atoms on the inside.

Figure 2 shows two 1D-grating MOT chips, which have already been demonstrated [1]. Chip A has three square grating areas arranged symmetrically to leave a plane area in the centre. Chip B has the same geometry, but the

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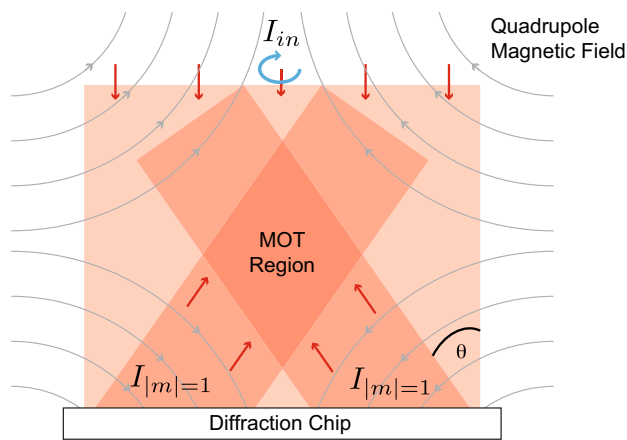


Fig. 1 Principle of the grating chips. A normally incident laser beam of intensity I_{in} is diffracted by metal reflection gratings, written into the surface of a chip. The gratings diffract the incoming light according to the Bragg condition $m\lambda = d \sin \theta$, where λ is the wavelength of light and d the grating period. By design, these structures diffract light only into the first-order beams ($m = \pm 1$) with an intensity $I_{|m|=1}$. Together with the magnetic quadrupole field, oriented as illustrated, the overlapping beams provide the light required for a magneto-optical trap (MOT). The angular momentum of the input beam, indicated by the blue arrow, is opposite to the local magnetic field direction, and the helicity of the light is well preserved after diffraction

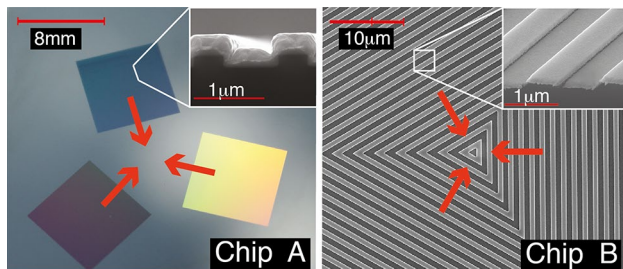


Fig. 2 One-dimensional grating chips of threefold radial symmetry, used to make 4-beam integrated MOTs. Red arrows indicate the diffracted beams used for trapping. Chip A is made by optical lithography, while chip B (shown magnified) is patterned by e-beam lithography. Insets Scanning electron microscope images of the grating lines

grating pattern covers the whole surface and, in particular, extends all the way to the centre. In this article, we describe the design and fabrication of each chip and compare the expected and measured optical properties of each. The article is organised as follows: in Sect. 2, we outline the simple scalar diffraction model that we used to design the chips. Section 3 describes how the gratings were fabricated. In Sect. 4, we measure the dimensions of the fabricated gratings and the optical properties of the diffracted beams, and we compare the performance achieved with the theoretical expectations. Finally, in Sect. 5 we summarise our findings.

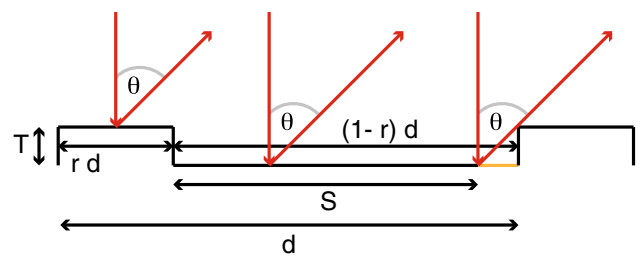


Fig. 3 Idealised diffraction grating profile, with period d , duty factor r , and depth T . S represents the effective length of the bottom facet, which is shortened because some light is shadowed by the step. Normally incident light is diffracted at an angle θ

2 Design of the chips

The atoms trapped by the MOT are held by optical scattering forces in the presence of a magnetic quadrupole field. Ideally, these forces should sum to zero at the centre of the quadrupole, which can be achieved by appropriate choices of intensity and polarisation of the light. The chips described here have symmetry that automatically balances the forces parallel to the surface, but balance in the normal direction has to be designed. Let the incident power P_{in} over an area A of the chip produce power ηP_{in} in each diffracted beam. The corresponding intensity is $I_{diff} = \eta P_{in} / (A \cos \theta)$, where θ is the angle to the normal, as shown in Fig. 1. With N diffracted beams participating in the MOT, the total intensity contributing to the upward force is $N I_{diff} \cos \theta = N \eta P_{in} / A = N \eta I_{in}$. The vertical balance of intensities therefore requires $N \eta = 1$. For chips A and B in Fig. 2, which use three diffracted beams, this condition becomes $\eta = 1/3$ [26]. In practice, the optimum diffracted intensity is somewhat higher because the polarisations of the upward and downward beams are not the same.

To estimate the power diffracted from our gratings, we approximate them by the ideal profile shown in Fig. 3. The elementary period d contains a top face of width rd and a bottom face of width $(1-r)d$ that is lower by a depth T . Light diffracted at an angle θ from the lower face is shadowed by the step, so that the effective width of the face is $S = (1-r)d - T \tan \theta$. The phase difference between rays coming from the centre of the top surface and the centre of the effective bottom surface is

$$\phi = k \left[\frac{1}{2} (d - T \tan \theta) \sin \theta - T(1 + \cos \theta) \right], \quad (1)$$

where $k = 2\pi/\lambda$ and λ is the wavelength of the light. With a normally incident field E_{in} , and assuming power reflectivity ρ , the diffracted field at (large) distance R is approximated by the Fraunhofer integral.

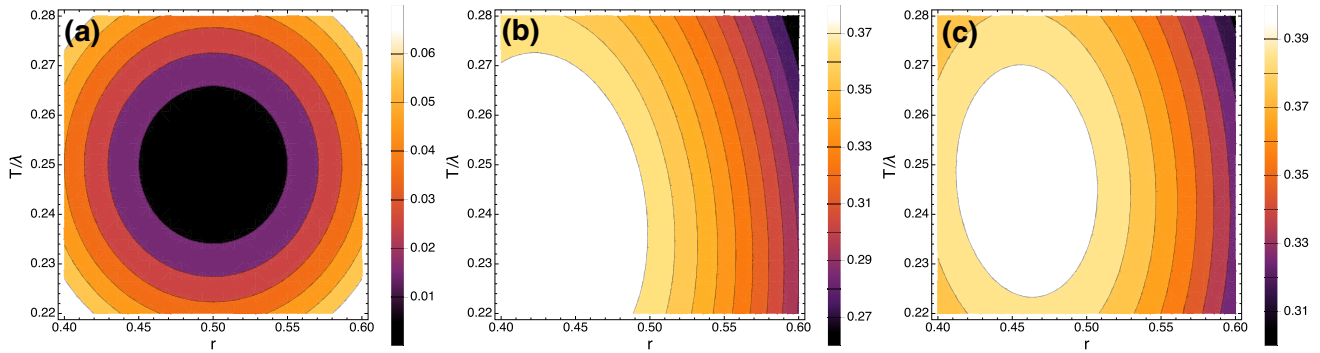


Fig. 4 Power in a single diffraction order, normalised to the incident power and plotted as a function of duty factor r and grating depth T divided by wavelength λ . Reflectivity is taken to be $\rho = 1$. **a** The zero-order case given by Eq. (5). This is the region near minimum power, where $r \simeq 1/2$ and $T \simeq \lambda/4$. The minimum is wide enough to

forgive minor fabrication errors. **b** Fraction of power in the $m = +1$ order of chip A, calculated from Eq. (4) with $d = 1.19 \mu\text{m}$ and $\lambda = 780\text{nm}$. **c** Fraction of power in the $m = +1$ order of chip B, calculated from Eq. (4) with $d = 1.48 \mu\text{m}$ and $\lambda = 780\text{nm}$

$$\frac{E(\theta)}{E_{\text{in}}} = \frac{\sqrt{\rho}}{\sqrt{R\lambda}} \left[\int_{-rd/2}^{rd/2} dx e^{ikx \sin \theta} + e^{i\phi} \int_{-S/2}^{S/2} dx e^{ikx \sin \theta} \right] \times \left(\sum_{n=1}^N e^{iknd \sin \theta} \right). \tag{2}$$

Here, the first line describes the diffraction from one elementary unit of the grating, as illustrated in Fig. 3, while the last factor sums over the contribution from all N grating periods.

The intensity distribution, obtained by squaring equation (2), has a comb of narrow peaks coming from the grating factor, with maxima at the Bragg angles given by $\sin \theta = m\lambda/d$, where m is an integer. Because many lines of the grating are illuminated, the single-period factor is essentially constant over the small angular spread across one of the Bragg peaks. This makes it straightforward to integrate across the m^{th} Bragg peak to find the total diffracted power P_m in that order. The result is

$$\frac{P_m}{P_{\text{in}}} = \frac{\rho}{d^2} \left| \int_{-rd/2}^{rd/2} dx e^{i2\pi mx/d} + e^{i\phi} \int_{-S/2}^{S/2} dx e^{i2\pi mx/d} \right|^2, \tag{3}$$

P_{in} being the power incident on the N illuminated lines of the grating. Evaluating these integrals,

$$\frac{P_m}{P_{\text{in}}} = \frac{\rho}{m^2 \pi^2} [\sin^2(m\pi r) + \sin^2(m\pi S/d) + 2 \cos(\phi) \sin(m\pi r) \sin(m\pi S/d)]. \tag{4}$$

Let us first consider diffraction into the $m = 0$ order—i.e. retro-reflection of the incident beam. This needs to be avoided as a strong upward beam of the wrong polarisation is detrimental to the MOT [1]. For chip A, there is a plane surface in the central region, which can either be cut away

to leave an aperture, or coated with an absorbing layer. For chip B, where the grating structure runs all the way into the middle, the retro-reflection can be suppressed instead by a suitable choice of the grating parameters. On using Eq. (1) to eliminate ϕ , Eq. (4) gives

$$\frac{P_0}{P_{\text{in}}} = \rho \left[1 + 2r(r-1) \left(1 - \cos\left(\frac{4\pi T}{\lambda}\right) \right) \right]. \tag{5}$$

This goes to zero when $r = \frac{1}{2} \left(1 + \frac{i}{\tan(2\pi T/\lambda)} \right)$. Since r must be real, we require $\tan(2\pi T/\lambda) = \infty$, which leaves $r = \frac{1}{2}$. It is desirable to minimise the depth T so that S remains as large as possible for the first diffraction order. We therefore choose $T = \lambda/4$. Figure 4a shows how P_0/P_{in} varies when r and T deviate from this ideal condition, as they inevitably will in practice. We see that deviations of up to 10% in either T or r give rise to a P_0/P_{in} of only one or two per cent, making the design robust against minor fabrication errors.

We turn now to the first-order beams, which (together with the incident beam) are responsible for making the MOT. To ensure efficient use of the available power, we choose gratings where $d < \lambda/2$, so that there are no diffracted beams except for those having $m = 0$ and $|m| = 1$.

The plots in Fig. 4b (for chip A) and Fig. 4c (for chip B) show the power P_1 in the $m = +1$ order (normalised to P_{in}) when the grating depth T and duty factor r are varied. We see that this power is close to a maximum when the retro-reflected power is zero, but can be increased a little by reducing r slightly below 0.5. This has the effect of making rd and S more nearly equal, which improves the contrast of the grating. A little is also gained by reducing T/λ , so that the width S of the lower surface is increased. As with the minimum of P_0 , this maximum of P_1 is sufficiently forgiving that we are not troubled by minor fabrication errors.

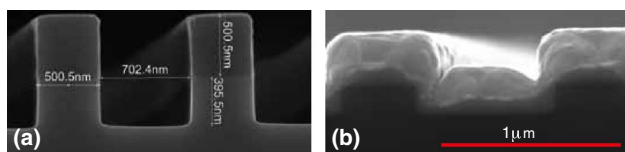


Fig. 5 **a** Scanning electron microscope images of chip A. **a** A deep trench calibrates the etching rate prior to the main fabrication and shows a profile close to that of our model, as illustrated in Fig. 3. **b** The final chip after etching to a depth of $T \sim 195$ nm and coating with 200 nm of gold. This brings the duty factor r close to $1/2$

The MOT works because the scattering force in the presence of a magnetic field depends on the polarisation of the light [25]. For that reason, it would be ideal to go beyond this simple scalar model of the diffraction to consider polarisation. However, that theory is quite challenging and is beyond the scope of this article. Instead we have relied on experiment to determine the polarisation of the diffracted beam, as discussed further in Sect. 4.

3 Fabrication

Chips A and B are produced by two different fabrication methods, which we now describe.

3.1 Chip A: photolithography using silicon substrate

Chip A, as shown in Fig. 2a, is a 32 mm square of silicon in which three 8-mm-square lamellar gratings are etched by photolithography. This is then covered with gold to achieve the desired high reflectivity at 780 nm. We choose a grating period of $1.2 \mu\text{m}$, which is close to the minimum that can be reliably made by this method. Although we aim for a duty factor of $r = \frac{1}{2}$, the bottom face is designed to be 700 nm wide, anticipating that r will move towards $1/2$ after the gold is added.

To begin, we make a reticle by direct ebeam writing on chromium-coated quartz. This is a $5\times$ magnified version of one square grating. A $\langle 100 \rangle$ -orientated 150-mm-diameter silicon wafer is then coated with SPR660 photoresist to a thickness of $0.8 \mu\text{m}$ and exposed to de-magnified images of the reticle, using light of 365 nm wavelength. A stepper motor manoeuvres the reticle to each grating position in turn, to produce an image of 12 chips—32 gratings in total—on the wafer. The resist is then developed, and the exposed silicon is removed by reactive ion etching using an inductively coupled $\text{SF}_6/\text{C}_4\text{F}_8$ plasma. With a typical etch rate of ~ 5 nm/s, this forms a grating of the desired depth— $\lambda/4 = 195$ nm—in under 1 minute. The wafer is then stripped of the remaining resist by plasma ashing, before cleaning with a piranha solution to remove any remaining

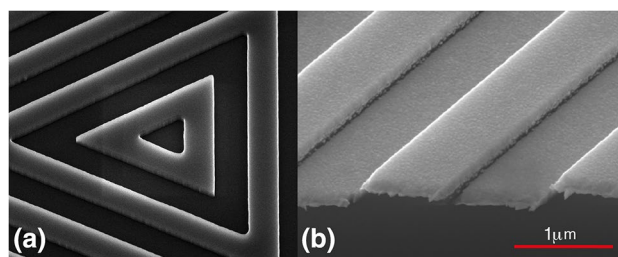


Fig. 6 Scanning electron microscope images of chip B. **a** The centre of chip B, etched to a depth of 195 nm, before coating. The triangles are equilateral, but distorted by the angle of view. **b** After coating with aluminium

organic contaminants. Figure 5a shows a scanning electron microscope image of a deep grating that was made to calibrate the etch rate. One can see in this image the high quality of the profile and the few-nm accuracy of the widths produced.

In order to give the gratings a high reflectivity, we apply a 5 nm-thick adhesion layer of chromium (by dc sputtering) followed by 200 nm-thick layer of gold (by rf sputtering). The finished grating is shown in Fig. 5b. From this and similar scans, we measure a final depth of $T = 207(5)$ nm, a period of $d = 1.19(1) \mu\text{m}$ and a duty factor of $r = 0.51(5)$, the latter being due in part to some systematic variation across the chip.

3.2 Chip B: electron-beam lithography using silicon substrate

Chip B is a 22 mm square of silicon, coated with aluminium, in which a grating is etched by electron-beam lithography. The grating consists of nested triangles, as shown magnified in Fig. 2b, that continue outward to fill a 20 mm square. The lamellar surface profile is designed to have a depth of 195 nm, a period of $1.5 \mu\text{m}$ and a duty factor of $1/2$. Unlike the photolithography used for chip A, the e-beam fabrication used here is not at all challenged by the resolution we require. However, the large size of the pattern over all does present a challenge.

A $\langle 100 \rangle$ -orientated 100-mm-diameter silicon wafer is coated with ZEP520A e-beam resist to a thickness of 350 nm, which is then patterned using a high-speed e-beam writer (Vistec VB6 with 50 MHz scan speed). With 11 chips, covering a total area of 44 cm^2 , this takes 25 h of continuous writing. Particular care is needed to ensure the electron-beam direction does not drift over this time, thereby introducing phase variations across individual gratings. The wafer is then etched and cleaned in the same way as chip A. The scanning electron microscope image in Fig. 6a shows the centre of the etched grating and illustrates the high quality of the fabrication.

After evaporating 100nm of aluminium, the grating is imaged again, as shown in Fig. 6b. From this and similar scans, we measure the final parameters $T = 190(5)$ nm, $d = 1.48(1)$ μm and $r = 0.46(5)$.

4 Measurement of optical properties

The two different coatings—gold for chip A and aluminium for chip B—are motivated by two ways of operating. With the chip inside a vacuum, the required $\sim 1/3$ power in each diffracted beam (see Sect. 2) is provided by an aluminium coating. The higher reflectivity of gold is needed for a chip outside the window of a glass cell because the diffracted beams suffer reflection losses when they pass through the window. There is no significance to the different thicknesses used—it is sufficient for the metal film to be large compared with the skin depth. The reflectivity of each chip was determined by measuring the power in a 780nm laser beam reflected from a flat, un-etched area and comparing this with the incident power. We found $\rho = 0.972(6)$ for chip A and $\rho = 0.822(6)$ for chip B.

In order to measure the diffracted power ratio P_m/P_{in} , a few-milliwatt laser beam of 780nm wavelength was spatially filtered using a single-mode fibre and then collimated to form a beam of approximately 1mm full-width-half-maximum. This was sent through a polarising beam splitter and then circularly polarised by a quarter-wave plate, as it would be to make a MOT. Roughly 1 m from the wave plate, the light was retro-reflected from a flat area of the chip and sent back through the wave plate and beam splitter. The circular polarisation of the incident light was optimised by adjusting the angle of the quarter-wave plate to extinguish the light returning through the beam splitter. Next, a translation stage moved the chip so that the light was incident on a grating, and a power meter then recorded the incident power P_{in} and the power P_1 diffracted into first order. (The $m = 1$ beams were easily separated from $m = 0$ because of the large diffraction angle -41° for grating A and 32° for B).

We measured each of the three gratings on chip A, with the results $P_1/P_{\text{in}} = 0.326(2)$, $0.323(2)$, $0.386(2)$. These are to be compared with the power ratio given by Eq. (4) after inserting the measured grating dimensions and reflectivity. That gives $0.340_{-0.36}^{+0.21}$, in good agreement with the measurements. The small variation in both theory and experiment is due predominantly to r . This translates into a variation of the diffracted power because chip A, having $r = 0.51(5)$, operates on the high- r side of the maximum plotted in Fig. 4b, where the derivative with respect to r is not zero.

Measurements on the three gratings of chip B gave $P_1/P_{\text{in}} = 0.381(2)$, $0.381(2)$, $0.380(2)$, showing a good

level of reproducibility. This is due in part to better uniformity of the e-beam lithography, but also, chip B operates with $r = 0.46(5)$, which is very close to the maximum of the plot in Fig. 4c, where P_1 is insensitive to variation of r . The power ratio given by Eq. (4) for chip B is $0.328_{-0.9}^{+0.2}$. While this is qualitatively similar to the measured fraction, it does not agree within the measurement uncertainty, and we cannot find any plausible adjustment of parameters that might bring them into agreement. We are forced to conclude that our diffraction theory is not able to predict the diffracted power with this high level of accuracy and suspect that the limitation is due to our use of the effective width S , defined by ray optics and therefore not strictly justified. In the case of chip B, the zeroth-order beam passes through the MOT, so it is important with this chip to have a low P_0 . In order to measure this, we rotated the chip by approximately 5mrad to separate the $m = 0$ diffracted beam from the incident beam. This measurement gave $P_0 = 0.005(1)$, in good agreement with $0.007_{-0.7}^{+0.20}$ from Eq. (4).

The magneto-optical trapping force depends on the polarisation of the light, relative to the direction of the local magnetic field [21]. This is discussed for our particular geometry in [25], which shows that the MOT works well when diffraction of the beam reverses its helicity. We therefore checked the polarisation of the first-order diffracted beams using a second combination of quarter-wave plate and polarising beam splitter, adjusted to project the state of the beam onto the basis of left- and right-handed polarisations. Photodetectors at the two beam splitter outputs measured the powers P_L and P_R in each circular polarisation. The fraction of power with reversed helicity from the three gratings on Chip A was 88, 90 and 98 %, and we note that better helicity reversal coincided in each case with higher power. On chip B, we measured 97, 98 and 99 %. This high degree of polarisation is more than adequate to make a strong MOT with either chip [1]. Indeed, although we do not have any calculation for comparison, it seems surprisingly high given the obvious anisotropy of the surface and of the diffraction geometry. We note that the variation in polarisation is greater across chip A than chip B, and again, we ascribe this to the two different methods of fabrication.

5 Summary and conclusions

Optical reflection gratings fabricated on an atom chip offer a simple way to build a large, robust, integrated magneto-optical trap (MOT) for atoms [1]. In this paper, we have discussed the main design considerations and have described how suitable chips can be fabricated using two methods: optical lithography and e-beam lithography. Using scalar Fraunhofer diffraction theory and an idealised model

of the lamellar profile, we have provided an account of the expected MOT beam intensities. This theory agrees well with experiment down to the level of a few per cent of the incident power, but not with the higher-precision measurements made on the aluminium-coated chip B. We have shown that it is possible to suppress the back-reflection, while at the same time diffracting a large fraction of the power into the two first-order beams. The power in these beams depends on the choice of period d , duty factor r and depth T of the grating. These parameters vary a little over the optically fabricated chip A, and rather less over the e-beam fabricated chip B. In either case, we show how to minimise the effect of inhomogeneity on the diffracted beam intensity by operating at the intensity maximum with respect to r and T . We also find that the circular polarisation of the light is surprisingly well preserved after diffraction into the first-order beams.

The design principles and theoretical model developed here make this new method accessible to anyone who may wish to incorporate such an integrated trap into an atom chip. We anticipate that this approach will facilitate future quantum technologies using cold and ultracold atoms [27].

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