Enhanced Flat-Topped Modulation for MMC Control in HVDC Transmission Systems

Rui Li, John E. Fletcher, Senior Member, IEEE, Lie Xu, Senior Member, IEEE, and Barry W. Williams

Abstract—Flat-topped modulation is a member of the family of triplen-series injection techniques that have been extensively utilized in PWM inverter systems to increase the DC-link, and hence semiconductor, utilization. We propose the use of an optimized flat-topped modulation scheme for the modular multilevel converter (MMC) control. The optimized flat-topped waveform minimizes the magnitude of the triplen harmonics, particularly compared to the popular space-vector modulation (SVM) technique, while fully utilizing the DC voltage. This has particular advantages if the converter-side of the interfacing transformer is earthed. Under such conditions, the zero-sequence earthing current is affected by the triplen series injected into the sinusoidal modulating functions. Therefore, it is critical to minimize the injected triplen harmonics. The operating principle of the flat-topped scheme is presented and the Fourier coefficients are compared with the SVM technique. Additionally, the influence of the proposed control scheme on MMC performance is evaluated mathematically. Simulation of a point-to-point HVDC link using average model demonstrates the effectiveness of the proposed MMC operational schemes. The third harmonic of the flat-topped modulation is reduced by 33%, which lowers the potential zero-sequence current flowing to earth. Compared to conventional sinusoidal modulation, the submodule capacitance is reduced by 25%. This significantly lowers submodule cost, volume, and weight. Station conduction losses are expected to reduce by 11%, yielding higher efficiency and lowering cooling system capacity. In addition to the improvement under normal operation, the proposed control scheme also reduces the fault current by 13.4%.

Index Terms—HVDC transmission, modular multilevel converter (MMC), flat-topped modulation, space-vector modulation (SVM), submodule capacitance, zero-sequence current.

I. Introduction

Modular multilevel converters (MMCs) are voltage source converters (VSCs) suited to high-voltage DC (HVDC) transmission systems. With a large number of submodules (SMs) per arm, it can generate a staircase voltage that approximates a sinusoidal waveform, with extremely low harmonic distortion; thus no AC filters are needed. Additionally, switching losses are significantly reduced, and low dv/dt enables the use of transformers with low insulation requirements [1-5]. Due to these significant advantages, MMC deployment in HVDC system is increasing.

A three-phase transformer is used on the MMC AC-side to isolate the grid and the converter and match the AC and DC voltages. Thus sinusoidal modulation is capable of generating the required voltage and controlling the MMC, although the DC voltage is not fully utilized and consequently neither are the semiconductors. Sinusoidal modulation has good harmonic characteristics and can be simply implemented in digital controllers. As a result, it is widely used as a modulation technique for MMCs [6-8].

Selective harmonic elimination (SHE) modulation is introduced in [9] to control the hybrid multilevel converter and reduce switching losses. However, the active switches of the main power stage still suffer high voltage stresses. Trapezoidal modulation is utilized in the solid-state DC transformer and in the hybrid cascaded MMC in [10] and [11] respectively to reduce switching losses and effectively utilize the DC voltage to produce an output AC voltage with higher fundamental amplitude. However, this is achieved at the expense of higher capital cost and a larger footprint.

By adding zero-sequence components into the reference voltage, discontinuous modulation [12, 13] fully utilizes the DC voltage and reduces switching losses. However, additional SMs are required in each arm to avoid over-modulation and reduce SM capacitor voltage ripple. In [14], the second harmonic is injected into the arm current to optimize the current distribution among the SMs and reduce SM capacitor voltage ripple, but at the expense of higher semiconductor current stresses.

Space-vector modulation (SVM), is another attractive approach for MMC control. By injecting triplen harmonics, the DC voltage utilization ratio is increased from ½ to $1/\sqrt{3}$, compared to sinusoidal modulation [15-17]. In [18], the MMC was first proposed for high voltage application and SVM is adopted to effectively utilize the DC voltage. However, it is a burden for the controller to implement the presented SVM. The advantage of SVM over sinusoidal modulation is discussed in [19] and the system performance under a DC fault is improved. However, the influence of SVM during normal operation is not considered.

MMC dynamics under both balanced and unbalanced grid conditions with SVM are evaluated in [17]. However, the

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influence of the triplen harmonics on losses and SM capacitance is not considered. Modified space-vector nearest level modulation (NLM) is discussed in [20] to increase the DC voltage utilization ratio thus reduce the DC voltage. However, the reduced DC voltage means a higher DC current requirement in order to transfer rated power, resulting in higher power transmission losses.

In the VSC-HVDC system, the three-phase transformer may use a Yn/D configuration where the neutral is earthed on grid-side [21, 22]. However, a D/Yn transformer connection with converter-side neutral earthed is introduced in [23-25] to limit the DC overvoltage during a single phase-to-ground fault and a DC pole-to-ground fault.

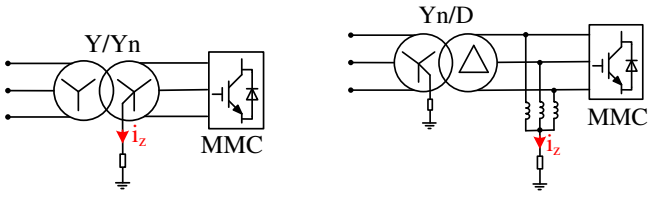

Fig. 1. Transformer converter-side earthing arrangements in the Zhoushan HVDC project (±200kV) near Shanghai China (the first 5-terminal MMC-HVDC project in the world in operation): (a) Yangshan station and (b) Dinghai and Daishan stations [26-28].

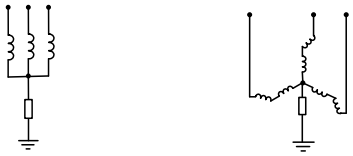

Fig. 2. Alternative earthing approaches for a D winding of the interface transformer: (a) three-phase earthing reactor [26-28] and (b) zig-zag transformer [29, 30].

In the Zhoushan project (±200kV) near Shanghai China, which is the first 5-terminal MMC-HVDC project in the world and is in operation, Yangshan station uses Y/Yn transformer with the converter-side earthed, Fig. 1 (a). Dinghai and Daishan stations use conventional Yn/D transformer with grid-side earthed and a three-phase reactor with neutral point earthed through a resistance is connected on the converter-side to earth these two station converters, as shown in Fig. 1 (b) [26-28].

In addition to the three-phase earthing reactor as shown in Fig. 1 (b) and Fig. 2 (a), the zig-zag transformer in Fig. 2 (b) is also capable of providing the earthing point for a D winding of the interfacing transformer on the converter-side or grid-side [29, 30].

However, the earthing point on the transformer converter-side provides a zero-sequence current path and the zero-sequence component of the converter-side three-phase currents flows to earth through the earthing point. If SVM was adopted, the zero-sequence current i_z would be critical due to the high triplen harmonic voltages produced by SVM, which would cause distorted three-phase currents on the converter-side and high losses in the earthing resistance.

To reduce the triplen harmonics in SVM while effectively utilize the DC voltage, a novel flat-topped modulation scheme with reduced zero-sequence harmonics compared with SVM is introduced in [31] to drive a motor and reduce the computational burden for the controller. The flat-topped modulation waveform is simply scaled as the voltage requirement changes, so the injected zero-sequence has a fixed harmonic spectrum with reference to the fundamental. In our proposed Mode II modulation scheme, the injected triplen-series changes dynamically thereby reducing and optimizing the magnitude of the required triplen harmonics. This leads to improved performance in the MMC as will be demonstrated.

This paper aims to enhance the triplen harmonics and fully utilize the DC voltage in order to improve the performance of MMC in a HVDC system. The paper is organized as follows. In Section II, the novel flat-topped modulation scheme for MMC control is proposed and its harmonic characteristics and advantages over SVM are analyzed. The influence of the proposed control scheme on converter losses, SM capacitance, and DC fault currents are discussed in Section III. System performance of the proposed MMC control scheme is assessed by a point-to-point HVDC link using an average model in Section IV. Finally Section V draws conclusions.

II. Enhanced Flat-Topped Modulation Scheme

A. Operating Principle

The proposed flat-topped modulation is achieved by subtracting a triplen series waveform from the original three-phase sinusoidal references. The triplen series waveform is generated by threshold-limiting the sinusoidal references. The technique increases the DC voltage utilization ratio and ensures sinusoidal line voltages at the MMC AC terminals.

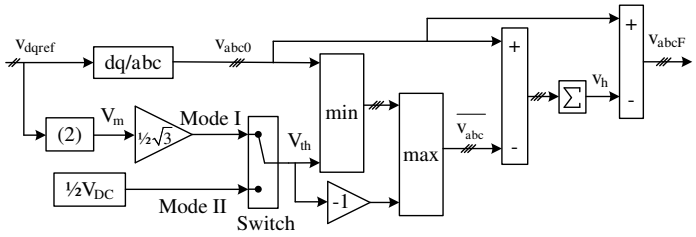

Fig. 3. Proposed flat-topped modulation for MMC control.

As illustrated in Fig. 3, the command voltages v_{dref} and v_{qref} (v_{dqref}, Fig. 3) are obtained from the current control loop in synchronous rotating coordinates. Transforming v_{dref} and v_{qref} to three-phase stationary coordinates, the original three-phase reference voltages v_{j0} (j=a, b, c) (v_{abc0}, Fig. 3) can be obtained and are assumed as:

$$\begin{cases} v_{a0} = V_m \sin(\omega t) \\ v_{b0} = V_m \sin(\omega t - 2\pi/3) \\ v_{c0} = V_m \sin(\omega t + 2\pi/3) \end{cases} \quad (1)$$

where ω is the grid angular velocity; V_m is the fundamental amplitude and is derived by:

$$V_m = \sqrt{v_{dref}^2 + v_{qref}^2}. \quad (2)$$

Limiting the original reference voltages v_{j0} (j=a, b, c) in the range of $\pm V_{th}$, the following equation is obtained:

$$\overline{v_j} = \max\left[-V_{th}, \min\left(V_{th}, v_{j0}\right)\right], \qquad j = a, b, c \tag{3}$$

where V_{th} is voltage threshold and is actively set as:

$$V_{th} = \sqrt{3}/2\, V_m = \sqrt{3}/2 \sqrt{v_{dref}{}^2 + v_{qref}{}^2}. \tag{4}$$

Subtracting $\overline{v_j}$ ($\overline{v_{abc}}$, Fig. 3) from v_{j0} and summing the resulting three-phase components together yields the required injected signal:

$$v_h = \sum_{j=a,b,c} \left(v_{j0} - \overline{v_j}\right). \tag{5}$$

Then the three-phase reference voltages of the flat-topped modulation v_{jF} (j=a, b, c) (v_{abcF}, Fig. 3) are derived by injecting the harmonic voltage v_h into the original three-phase voltages v_{j0} (j=a, b, c):

$$v_{jF} = v_{j0} - v_h, \qquad j = a, b, c. \tag{6}$$

As shown in Fig. 4 (b), the three-phase voltages v_{jF} (j=a, b, c) have flat tops which cover a sextant ($\pi/3$ radians) of the fundamental. In a period of $2\pi/3\omega$, the harmonic voltage in Fig. 4 (b) is govern by:

$$v_h = \begin{cases} V_m\left[\sin(\omega t) - \dfrac{\sqrt{3}}{2}\right], & -\pi < 3\omega t \le 0 \\ V_m\left[\sin\left(\omega t - \dfrac{2\pi}{3}\right) + \dfrac{\sqrt{3}}{2}\right], & 0 < 3\omega t \le \pi \end{cases}. \tag{7}$$

The harmonic voltage v_h is then expressed by the Fourier series:

$$v_h = \sum_{n=1}^{\infty} \frac{\sqrt{3} V_m \sin\left[(2n-1)3\omega t\right]}{2\pi(2n-1)(3n-2)(3n-1)}. \tag{8}$$

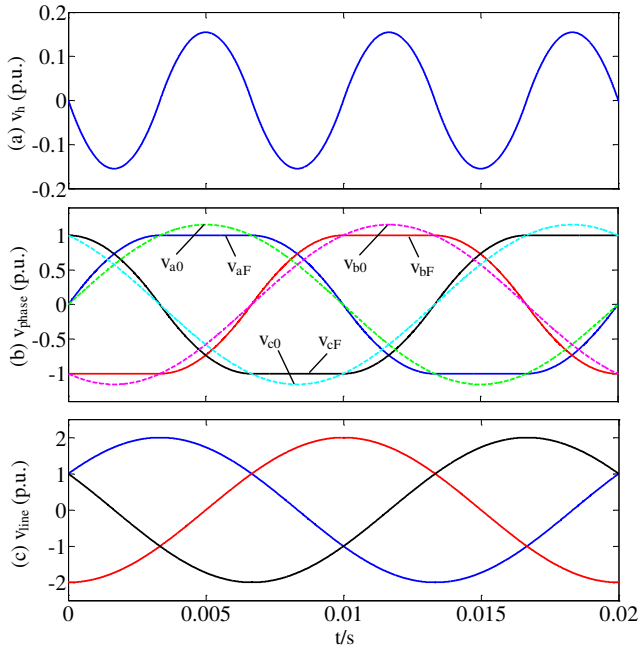

Fig. 4. Reference voltages of the proposed flat-topped modulation for MMC control, normalized to ½V_{DC} and $m_h = 2/\sqrt{3}$: (a) injected triplen harmonics, (b) phase voltages referenced to the DC-link mid-point, and (c) line voltages.

The harmonic voltage v_h contains only triplen harmonics (h=3rd, 9th, 15th, …), which are cophasal and are not present in the line voltages, as shown in Fig. 4 (c). With V_m in the range of (0~ $V_{DC}/\sqrt{3}$), where V_{DC} is the DC voltage, the peak of reference phase voltage v_{jF} (j=a, b, c) are limited by (3) and (4) and do not exceed ½V_{DC}. Thus, the DC voltage utilization ratio is increased from ½ to $1/\sqrt{3}$, compared to sinusoidal modulation. The fundamental amplitude V_m can be greater than ½V_{DC} while over-modulation is avoided.

Ignoring the voltage drop across the arm inductances, the transformer leakage inductances, and the grid inductances, a modulation index m is defined as the ratio between the fundamental amplitude and half the DC voltage:

$$m = \frac{V_m}{½V_{DC}}. \tag{9}$$

Thus, the modulation index of the flat-topped modulation m_F is in the range of (0~ $2/\sqrt{3}$). The maximum fundamental amplitude of the phase voltage is increased from ½V_{DC} (1p.u.) to $V_{DC}/\sqrt{3}$ ($2/\sqrt{3}$ p.u.) by using flat-topped modulation, while output voltage peak remains ½V_{DC} (1p.u.), as demonstrated in Fig. 4 (b). As a result, with the same peak of output voltage, the relationship between the modulation indices of the flat-topped modulation m_F and that of sinusoidal modulation m_0 is:

$$m_F = 2/\sqrt{3}\, m_0. \tag{10}$$

B. Comparison between SVM and Flat-Topped Modulation

The proposed flat-topped modulation has the same voltage generating capability as SVM but with reduced triplen harmonics. From (6) and (8), the phase voltage of the flat-topped modulation, referenced to the mid-point of the DC-link, is rewritten as:

$$v_{aF} = V_m \sin(\omega t) + \sum_{n=1}^{\infty} \frac{\sqrt{3} V_m \sin\left[(2n-1)3\omega t\right]}{2\pi(2n-1)(3n-2)(3n-1)}. \tag{11}$$

The components of the triplen harmonics are then derived and listed in Table I. Compared to SVM, the injected triplen harmonics in the proposed flat-topped scheme are enhanced. The dominant third harmonic is reduced from 20.67% to 13.8% (by 33%) while the voltage generating capability remains unchanged. The triplen harmonics in the flat-topped modulation attenuate faster and are lower than that of SVM. The lower triplen harmonics indicate the proposed scheme can reduce the zero-sequence current flowing to the earth point on the converter-side.

Although the zero-sequence voltage exists in the MMC station with converter-side of the transformer unearthed, the zero-sequence current is always zero as there is no zero-sequence current path. However, the zero-sequence voltage causes the voltage variation of transformer terminals. As third harmonic voltage is reduced by 33% by the proposed control scheme, the voltage variation of transformer terminals is correspondingly reduced.

Additionally, the proposed modulation scheme avoids the sector determination and the calculation of time duration for which the space vector is applied. This makes it easy to implement and does not cause extra computational burden for the controller, even for MMC with several hundred SMs per arm.

SVM is widely used in the control of the two-level VSC, as it gives the lowest switching-frequency generated current ripple compared with other modulation methods, e.g. sinusoidal modulation and dead band modulation [15, 16, 31]. The proposed flat-topped scheme can be used to control two-level VSC, but its current ripple is slightly higher than SVM, as the top of the proposed approach is flat. However, the current ripple is not a concern in MMC-HVDC application, where the output voltage typically has hundreds of levels and therefore produces minimal AC current ripple. This characteristic makes the proposed flat-topped modulation scheme more suitable for the MMC-HVDC application than for conventional two-level modulation.

Mode I scheme is proposed in [31] to control a two-level VSC and drive a motor. However, the influence of zero-sequence harmonics on the converter performance is not considered as low power drive systems are rarely concerned by the impact of the low-frequency common-mode voltage developed by triplen-series injection. In this paper, the application of Mode I in the MMC control is mathematically analysed and its influence on MMC performance is evaluated, where the SM capacitance, station conduction losses, DC fault currents are all significantly reduced.

TABLE I
Comparison of Harmonic Components between SVM and the Flat-Topped Modulation.

COMPONENT	1st	3rd	9th	15th	21st	27st
Space-Vector Modulation	1	20.67%	2.07%	0.74%	0.38%	0.23%
Flat-Topped Modulation	1	13.8%	0.46%	0.1%	0.04%	0.01%

C. Mode II Flat-Topped Modulation

As depicted by (3) and (4), the voltage limit is actively set at $\sqrt{3}/2\,V_m$ according to the command voltages v_{dref} and v_{qref}. This control scheme (noted as Mode I) injects triplen harmonics over the entire modulation index range of (0~ $2/\sqrt{3}$). Alternatively, by setting the voltage limit V_{th} at $\frac{1}{2}V_{DC}$ rather than $\sqrt{3}/2\,V_m$, Fig. 3, the triplen harmonic injection is only used when the modulation index m_F is greater than one ($1<m_F\leqslant 2/\sqrt{3}$). With m_F in the range of (0~1), no triplen harmonics are injected in this control scheme (noted as Mode II), which further enhances the harmonic characteristics of the flat-topped modulation.

In normal operation, the modulation index m_F does not exceed unity and the original three-phase reference voltages v_{abc0} are not greater than $\frac{1}{2}V_{DC}$. With the voltage limit V_{th} set at $\frac{1}{2}V_{DC}$, Fig. 3, the harmonic voltage v_h is zero and the three-phase reference voltages of the flat-topped modulation v_{abcF} equal the original three-phase voltages v_{abc0}:

$$v_{abcF} = v_{abc0} - v_h = v_{abc0} - 0 = v_{abc0}. \quad (12)$$

There is no injected triplen harmonics and MMCs are operated with sinusoidal modulation in Mode II scheme during normal operation. Thus, the zero-sequence current flowing to the earth point is further reduced, compared to Mode I, and is around zero, as sinusoidal modulation will not produce zero-sequence voltage. When Mode II injects triplen harmonics, it only injects those necessary to maintain the reference voltage peak of individual phase legs at $\frac{1}{2}V_{DC}$. So the injected triplen harmonics are chosen with the objective function to limit the reference voltage in the range of $\pm\frac{1}{2}V_{DC}$.

Fig. 5 shows the command voltages v_{phase_I} and v_{phase_II} of Mode I and II control scheme with flat-topped modulation, where the modulation index m_F increases from 0 to $2/\sqrt{3}$. When m_F is less than unity, triplen harmonics are only injected in Mode I scheme (v_{phase_I}) while an MMC is operated with sinusoidal reference waveforms in Mode II (v_{phase_II}). After m_F exceeds unity, triplen harmonics are gradually injected in Mode II. With the maximum modulation index $2/\sqrt{3}$, the two operating modes have the same reference waveforms. With m_F in the range of (1~ $2/\sqrt{3}$), the injected triplen-series of the proposed Mode II modulation scheme changes dynamically and the THD of phase voltage is always lower than that of Mode I. This further reduces the voltage variation of transformer terminals, neutral point (where relevant) and the potential zero-sequence current.

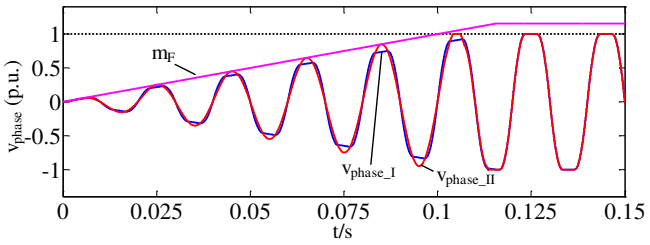

Fig. 5. Reference phase voltages v_{phase_I} and v_{phase_II} (relative to the midpoint of the DC-link) of the proposed Mode I and II control scheme with the variation of m_F from 0 to $2/\sqrt{3}$, which is normalized to $\frac{1}{2}V_{DC}$.

III. INFLUENCE OF FLAT-TOPPED MODULATION ON MMCS

In this section, the influence of the proposed flat-topped modulation scheme on MMC performance is discussed in normal operation and during a pole-to-pole DC fault.

A. Power Losses

The conduction losses are higher than the switching losses in MMCs for HVDC application and are the dominant part of station converter losses. Thus, only the conduction losses are discussed.

By using the enhanced flat-topped modulation scheme, the DC voltage utilization ratio is increased from $\frac{1}{2}$ to $1/\sqrt{3}$, and thus higher converter-side AC voltage can be used. As the transferred power is fixed, the AC current i_{ACF} is correspondingly reduced by 13.4%, compared to sinusoidal modulation:

$$i_{ACF} = \tfrac{1}{2}\sqrt{3}I_{m0}\sin(\omega t - \varphi) \quad (13)$$

where I_{m0} is the AC current amplitude in sinusoidal modulation control; and φ is the phase angle between the phase voltage and current. There is no zero-sequence current path for the MMC station with converter-side of the transformer unearthed. Additionally, the Mode II flat-topped modulation does not inject triplen harmonics under normal operation and thus the zero-sequence current i_z, flowing to the earth point on the converter-side, can be suppressed to around zero. As a result, the zero-sequence current is not considered in (13).

As depicted in [32], the AC current amplitude I_{m0} can be expressed in terms of the DC current I_{DC}, (13) is then rewritten as:

$$i_{ACF} = \frac{\sqrt{3}}{2}\frac{4I_{DC}}{3m_0\cos\varphi}\sin(\omega t - \varphi) = \frac{4I_{DC}}{3m_F\cos\varphi}\sin(\omega t - \varphi). \quad (14)$$

Considering the DC and fundamental frequency components, the arm current is described as:

$$i_{armF} = \tfrac{1}{3}I_{DC} + \tfrac{1}{2}i_{ACF} = \tfrac{1}{3}I_{DC}\left[1 + \frac{2\sin(\omega t - \varphi)}{m_F\cos\varphi}\right]. \quad (15)$$

For simplicity, the forward voltages of the IGBT and freewheel diode are assumed to be identical and denoted as V_{fd}. As the number of semiconductors in the current path per arm equals N (the SM number per arm), according to (15), the conduction loss of the station converter can be calculated as:

$$\begin{aligned} P_{lossF} &= \frac{6}{2\pi}\int_0^{2\pi} NV_{fd}\left|i_{armF}\right| d(\omega t) \\ &= \frac{4NV_{fd}I_{DC}}{\pi}\left(\frac{\sqrt{4 - m_F^2\cos^2\varphi}}{m_F\cos\varphi} + \arccos\sqrt{1 - \tfrac{1}{4}m_F^2\cos^2\varphi}\right). \end{aligned} \quad (16)$$

As Mode I and II have the same arm currents during normal operation, (15), the conduction losses of Mode I and II are identical and can both expressed by (16). The circulating current among the three-phase legs can be controlled around zero by proportional-resonant (PR) control, thus its influence on conduction losses is slight and not accounted for in (16).

Similarly, the conduction loss of the station converter with the sinusoidal modulation is:

$$P_{loss0} = \frac{4NV_{fd}I_{DC}}{\pi}\left(\frac{\sqrt{4 - m_0^2\cos^2\varphi}}{m_0\cos\varphi} + \arccos\sqrt{1 - \tfrac{1}{4}m_0^2\cos^2\varphi}\right). \quad (17)$$

TABLE II
Nominal Parameters of the Test System.

PARAMETER	Nominal Value
DC-link voltage	±320kV
Power rating	1200MW
AC grid voltage	400kV
SM number per arm	256
SM capacitor voltage	2.5kV
SM capacitance	7.7mF
Arm inductance	0.05p.u.
Number of pi sections for DC cable	10
R, L and C of DC cable	10mΩ/km, 0.5mH/km, 0.23μF/km
DC cable length	100km

A station converter with parameters listed in Table II is tested, where the modulation indexes are $m_0 = \sqrt{3}/2$ and $m_F = 2/\sqrt{3}m_0 = 1$. The conduction power losses of the test station with sinusoidal modulation and the enhanced flat-topped modulation are 6.2MW and 5.5MW respectively, from (17) and (16). Both Mode I and II control schemes with flat-topped modulation reduce the station conduction losses by 11%, compared to sinusoidal modulation. This significantly reduces station conduction losses, yielding higher efficiency and a reduced capacity cooling system.

B. SM Capacitance Requirements

The specified maximum capacitor voltage ripple typically determines the SM capacitance requirement [21]. This section presents the process of sizing the capacitances for the MMC with the proposed flat-topped scheme.

Besides the third harmonic, the voltage v_h contains other triplen harmonics. However, as listed in Table I, the third harmonic is the dominant frequency in the triplen harmonics and the influence of other triplen harmonics is ignored (purely third harmonic injection is a valid concept for increasing the DC voltage utilization ratio by 15.5%). Higher converter-side AC voltage is used for the flat-topped scheme due to the higher voltage generating capability:

$$v_{ACF} = \frac{V_{DC}}{2}\left[m_F\sin\omega t + m_h\sin 3\omega t\right] \quad (18)$$

where m_h is the modulation index of third harmonic voltage. The modulation index m_h in Mode I control scheme with flat-topped modulation is fixed at m_h=0.138m_F, as listed in Table I. For the Mode II flat-topped modulation, m_h is zero during normal operation and increases to m_h=0.138m_F, in order to generate the maximum AC voltages.

From (18), the arm voltage is expressed as:

$$v_{armF} = \tfrac{1}{2}V_{DC}\left[1 - m_F\sin\omega t - m_h\sin 3\omega t\right]. \quad (19)$$

According to (15) and (19), integrating the arm voltage multiplied by the arm current, the arm energy variation of the flat-topped modulation is

$$\begin{aligned} &\Delta E_{armF}(\omega t) = \frac{1}{\omega}\int_0^{\omega t} v_{armF}i_{armF}\,d(\omega t) = \\ &\frac{V_{DC}I_{DC}}{6\omega}\left\{-\frac{2}{m_F\cos\varphi}\left[\cos(\omega t - \varphi) - \cos\varphi\right] + m_F\left[\cos(\omega t) - 1\right] + \frac{1}{2\cos\varphi}\left[\sin(2\omega t - \varphi) + \sin\varphi\right]\right\} \\ &-\frac{m_hV_{DC}I_{DC}}{6\omega}\left\{-\frac{\cos(3\omega t) - 1}{3} + \frac{1}{m_F\cos\varphi}\left[\tfrac{1}{2}\sin(2\omega t + \varphi) - \tfrac{1}{4}\sin(4\omega t - \varphi) - \tfrac{3}{4}\sin\varphi\right]\right\}. \end{aligned} \quad (20)$$

Equation (20) is the universal expression of the arm energy variation with the flat-topped modulation and the difference of the Mode I and II is the third harmonic modulation index m_h, which is set at m_h=0.138m_F and m_h=0 for Mode I and II respectively.

Similarly, the arm energy variation with the sinusoidal modulation is:

$$\begin{aligned} &\Delta E_{arm0}(\omega t) = \\ &\frac{V_{DC}I_{DC}}{6\omega}\left\{-\frac{2}{m_0\cos\varphi}\left[\cos(\omega t - \varphi) - \cos\varphi\right] + m_0\left[\cos(\omega t) - 1\right] + \frac{1}{2\cos\varphi}\left[\sin(2\omega t - \varphi) + \sin\varphi\right]\right\}. \end{aligned} \quad (21)$$

For the test station with parameters listed in Table II, where the modulation indexes are $m_0 = \sqrt{3}/2$ and $m_F = 2/\sqrt{3}m_0 = 1$, the energy variations per arm are obtained from (20) and (21) and illustrated in Fig. 6. The peak-to-peak energy variations per arm with sinusoidal modulation and Mode I and II schemes with flat-topped modulation are 2.15MJ, 1.61MJ, and 1.65MJ,

respectively. Thus, with ±10% voltage ripple [21], their SM capacitances are C_{SM0}, $0.75C_{SM0}$, and $0.768C_{SM0}$, respectively. Compared with sinusoidal modulation, the SM capacitance with Mode I control scheme is reduced by 25%, which significantly reduces the SM volume, weight, and capital cost. Although Mode I has the same AC currents and fundamental AC voltages as Mode II, the arm energy variation is further reduced by the injected third harmonic in Mode I.

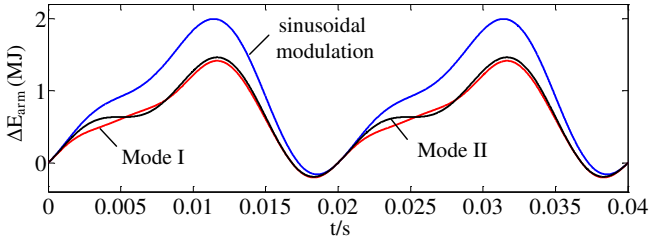

Fig. 6. Energy variations per arm with the sinusoidal modulation and flat-topped scheme, for $m_0=\sqrt{3}/2$, m_F=1, V_{DC}=640kV, P=1200MW, and φ=0.

C. Pole-to-Pole DC Fault Currents

As a pole-to-pole DC fault is a significant challenge for the MMC application in HVDC transmission systems, the influence of the proposed scheme on DC fault currents is discussed in this section. In the event of a DC short-circuit, high currents flow through the freewheel diodes in the half-bridge SM based MMC. The currents flow from the AC grid into the fault on the DC-side, even if the station converter is blocked immediately. The low impedance of the short-circuit path leads to a steep rise in fault current which may cause serious damage to the converters and may result in shutdown of the entire HVDC network [9, 33-35].

To limit circulating currents and DC fault currents, the arm inductance L_{arm} is required and its absolute value can be calculated from the p.u. value α:

$$L_{arm}=\alpha\frac{V_{LRMS}^{\ 2}}{\omega P}=\frac{3\alpha m^2 V_{DC}^{\ 2}}{8\omega P} \tag{22}$$

where V_{LRMS} is the RMS line voltage and P is the rated power. Equation (22) defines the relationship between the arm inductance and the modulation index and is in agreement with (9). With the same arm inductance p.u. value α, the arm inductance is increased by a third by using the flat-topped control scheme:

$$\frac{L_{armF}}{L_{arm0}}=\frac{m_F^{\ 2}}{m_0^{\ 2}}=\frac{\left(2/\sqrt{3}\right)^2}{1^2}=4/3. \tag{23}$$

Similarly, with the same p.u. value and the increased converter-side voltage, the converter-side transformer leakage inductance L_{TcF} increases by a third:

$$L_{TcF}=4/3\,L_{Tc0}. \tag{24}$$

On the gird-side, the grid voltage is constant and thus, with the same p.u. value, the absolute value of the grid-side leakage inductance L_{TgF} remains unchanged:

$$L_{TgF}=L_{Tg0}. \tag{25}$$

Transforming the converter-side inductances to the grid-side, the total AC-side inductance L_{ACF} with flat-topped control scheme is the same as with sinusoidal modulation:

$$\begin{aligned}L_{ACF}&=\frac{L_{armF}+L_{TcF}}{n_F^{\ 2}}+L_{TgF}+L_g=\frac{4/3\left(L_{arm0}+L_{Tc0}\right)}{\left(2n_0/\sqrt{3}\right)^2}+L_{Tg0}+L_g\\&=\frac{L_{arm0}+L_{Tc0}}{n_0^{\ 2}}+L_{Tg0}+L_g=L_{AC0}\end{aligned} \tag{26}$$

where L_g is the grid inductance; n_0 and n_F are the ratio between the converter-side line voltage and the grid-side line voltage for sinusoidal modulation and flat-topped scheme respectively. As the grid voltage remains unchanged and the converter-side voltage is increased from 1p.u. to $2/\sqrt{3}$ p.u. in the flat-topped scheme, as depicted by (10), the ratio n_F is greater than n_0:

$$n_F=2/\sqrt{3}\,n_0. \tag{27}$$

For a pole-to-pole DC fault at the station terminals, which is the most serious fault case for the station, the fault current on the transformer grid-side i_{fgF} remains unchanged due to the constant grid voltage and the unchanged total AC-side inductance L_{ACF}, as shown by (26). However, due to the increased ratio n_F, (27), the fault current on the transformer converter-side i_{fcF} is expected to be reduced by 13.4% by using the proposed control scheme with flat-topped modulation, which reduces the current stress on the freewheel diodes and DC circuit breakers, during a DC fault:

$$i_{fcF}=\frac{i_{fgF}}{n_F}=\frac{i_{fg0}}{2n_0/\sqrt{3}}=1/2\sqrt{3}i_{fc0}=0.866i_{fc0}. \tag{28}$$

IV. Performance Evaluation

The MMC performance with the proposed flat-topped modulation is assessed using a point-to-point HVDC link model as shown in Fig. 7, in the MATLAB/Simulink® environment. In the test system, MMC_1 imports rated active power from the AC grid G_1 to the DC-side at unity power factor while MMC_2 is configured to regulate the DC-link voltage level at ±320 kV, also at unity power factor. Both the stations (MMC_1 and MMC_2) are modeled as conventional half-bridge SM based MMCs using average models and have the same parameters listed in Table II.

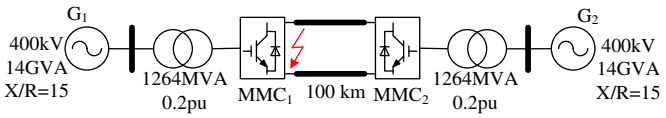

Fig. 7. Point-to-point HVDC link using average model.

Although Mode I control scheme reduces the third harmonic by 33% compared to that of SVM, the zero-sequence current still flows to the earthing point on the converter-side of the transformer. Thus, Mode I scheme is applicable for MMC-HVDC system with transformer converter-side unearthed and uses conventional Yn/D transformer with grid-side earthed in the test HVDC link. To keep accordance, the Yn/D transformer is adopted in Section IV A and C.

To demonstrate the significant advantage of the Mode II scheme over SVM, in terms of zero-sequence current reduction, the Y/Yn configuration of the transformer earthed on converter-side is used in Section IV B. This transformer

arrangement is also used in Yangshan station of the Zhoushan multi-terminal HVDC project, Fig. 1 (a). The three-phase earthing reactor as shown in Fig. 2 (a) is connected between the grid and the interface transformer to properly earth the grid-side.

TABLE III
AC voltages of the Test HVDC link.

PARAMETER	Sinusoidal modulation	SV modulation	Mode I	Mode II
Transformer grid-side and converter-side voltages	400kV/339kV	400kV/392kV	400kV/392kV	400kV/392kV
Modulation index	$\sqrt{3}/2$	1	1	1

Although the grid voltages are the same, higher converter-side AC voltage is used for the flat-topped control scheme due to its higher voltage generating capability, as aforementioned. Thus, with the sinusoidal modulation index m_0 set at $\sqrt{3}/2$, the converter-side RMS line voltages of sinusoidal modulation and the flat-topped scheme are obtained as 339kV and 392kV respectively, Table III, according to (9) and (10).

A. Comparison between Sinusoidal Modulation and Proposed Control Scheme

The MMC performance with the proposed control scheme under normal operation is compared to that with sinusoidal modulation, Fig. 8, where only the waveforms of MMC_1 are displayed for simplicity.

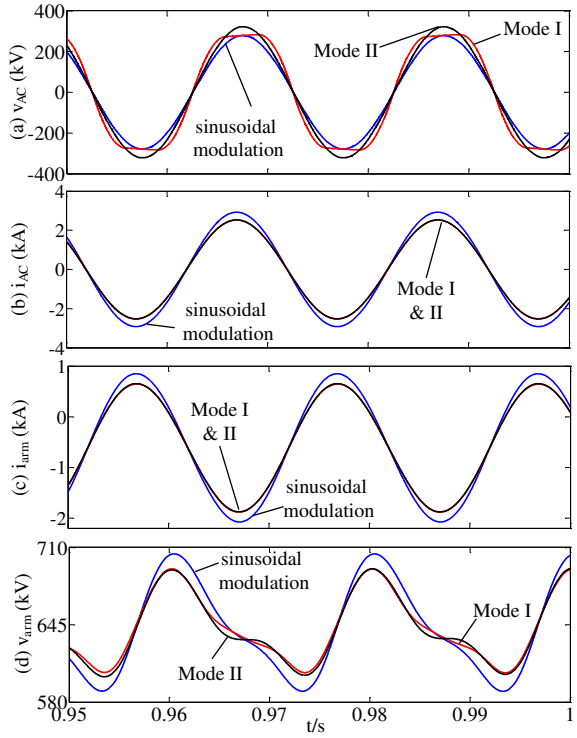

Fig. 8. Comparison between sinusoidal modulation and proposed control scheme in normal operation: (a) AC phase voltages referenced to the DC-link mid-point, (b) AC currents, (c) arm currents, and (d) arm voltages.

The output phase voltages referenced to the mid-point of the DC-link are shown in Fig. 8 (a). The voltage peaks with sinusoidal modulation and Mode I control scheme using flat-topped modulation are both controlled around 277kV. However, benefitting from the injected triplen harmonics, the fundamental voltage amplitude of the latter is around 320kV, higher than sinusoidal modulation control (277kV).

When the modulation index does not exceed unity in Mode II, the reference voltage of the converter does not contain triplen harmonics and has higher amplitude (320kV) compared to conventional sinusoidal modulation, Fig. 8 (a). Once the amplitude of the demand voltage, v_{abc0}, exceeds the threshold V_{th} (hence sinusoidal modulation will generate distorted phase voltages), triplen harmonics are injected by the proposed Mode II flat-topped modulation scheme to generate a higher fundamental voltage.

As shown in Fig. 8 (b), the injected triplen harmonics of Mode I only exist in the converter phase voltages referenced to the mid-point of the DC-link and do not affect the quality of the line voltage and current as they are co-phasal. With the same transferred power of 1200MW, the transformer converter-side current peak with the proposed scheme is reduced from about 2.9kA to 2.5kA.

As the arm current is the sum of one third the DC current and half the AC current, from Fig. 8 (c), the arm current peaks with the enhanced flat-topped modulation scheme are reduced approximately by 10%, compared with sinusoidal modulation, yielding lower semiconductor current stresses and conduction losses. Fig. 8 (d) shows the simulated arm voltages. With the same SM capacitance, the peak-to-peak ripple with sinusoidal modulation and with Mode I and II schemes are 125kV, 93kV, and 95kV respectively, which are in good agreement with the calculated values from (21) and (20).

To reduce computation time and accelerate the simulation, the average model is used in this work instead of the detailed model [36-40]. As only one capacitor is used per arm in the average model, SM capacitor voltage balancing is not considered. By using a sorting algorithm [3, 41, 42], SM capacitor voltages can be balanced in a detailed model with the proposed flat-topped modulation.

B. Comparison between SVM and Mode II Control Scheme

In the Mode II control scheme, the voltage threshold V_{th} is set at $\frac{1}{2}V_{DC}$. During normal operation, the DC voltage V_{DC} is controlled at the rated value (640kV) and the amplitude of the command voltage v_{abc0} is less than or equal to $\frac{1}{2}V_{DC}$ ($\frac{1}{2}\times640$kV=320kV). Thus, no triplen harmonics are injected in normal operation, as shown in Fig. 8 (a). For a DC fault that causes a reduction in the DC voltage (lower than 640kV), the MMCs cannot generate the required voltage with sinusoidal modulation, when the amplitude of the command voltages v_{abc0} is greater than half the DC voltage. Triplen harmonics are then injected, as presented in Section II, to improve the voltage generating capability of the MMCs. This also applies to the

operating condition where the AC grid voltage increases abnormally.

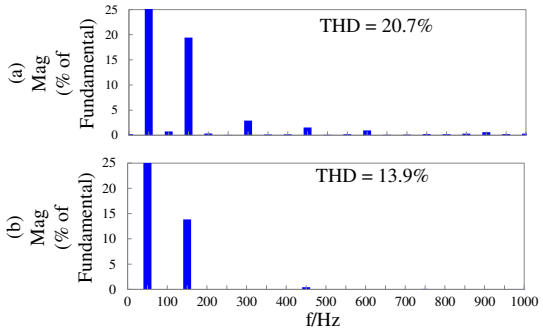

Fig. 9. FFT analysis of output phase voltages with: (a) SVM and (b) flat-topped control scheme with $m_F = 2/\sqrt{3}$.

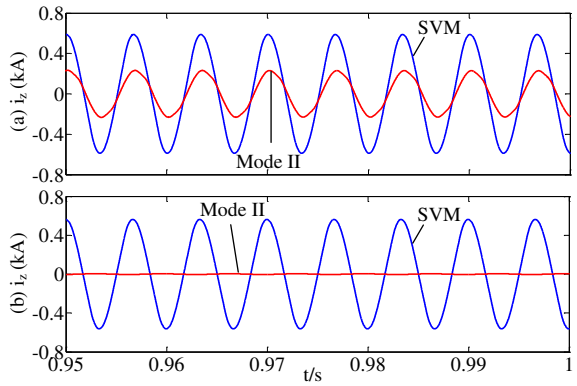

Fig. 10. Transformer converter-side zero-sequence currents with SVM and Mode II control scheme using flat-topped modulation: (a) abnormal situation and (b) normal operation.

Fig. 9 shows the FFT analysis of output phase voltage of MMC with $m_F = 2/\sqrt{3}$. The third harmonic dominates the triplen harmonics in the proposed flat-topped modulation and is lower than that with SVM, which is in agreement with Table I. In addition to third harmonic, all other triplen harmonics of the flat-topped modulation are lower than that with SVM. The THD of output phase voltage is therefore reduced from 20.7% to 13.9%, yielding a lower zero-sequence voltage component. This significantly lowers the converter-side zero-sequence current that flows to earth through the neutral point of Y/Yn transformer with converter-side earthed, Fig. 10 (a).

The output voltages of the MMC can be regulated well by the flat-topped scheme over the entire operating range, in addition to no-load and rated operating conditions.

The triplen harmonic content of SVM remains unchanged with the reduction of modulation index and the THD of phase voltage is always around 20%. Differently, the triplen harmonics are reduced gradually in the proposed Mode II control scheme with flat-topped modulation, after the remote DC fault is eliminated or the AC grid voltage restores to rated value. Once the system recovers from the abnormal situation, the modulation waveforms return to sinusoidal and do not contain triplen harmonics. As a result, the zero-sequence current i_z is close to zero in normal operation and lower than that with SVM, Fig. 10 (b).

The high triplen harmonics in SVM cause zero-sequence current flowing to earth through the neutral point of Y/Yn transformer with the converter-side earthed, Fig. 10 (a). Due to the zero-sequence current, the three-phase currents (converter-side) are not balanced, although the three-phase grid voltages are sinusoidal and balanced.

The Y/Yn transformer in the Zhoushan HVDC project, Fig. 1 (a), is taken as an example to demonstrate that the proposed flat-topped modulation can reduce the zero-sequence current flowing to earth, in the HVDC system with converter-side of the transformer earthed. In addition to the Y/Yn arrangement, all the HVDC systems with the transformer converter-side earthed have the issue of the zero-sequence current when SVM is used, e.g. D/Yn transformer with converter-side earthed [23-25], three-phase earthing reactor and the zig-zag transformer providing an earthing point [26-30], etc. Thus the flat-topped modulation scheme is an attractive proposition to reduce the zero-sequence current.

C. Performance during a Pole-to-Pole DC Fault

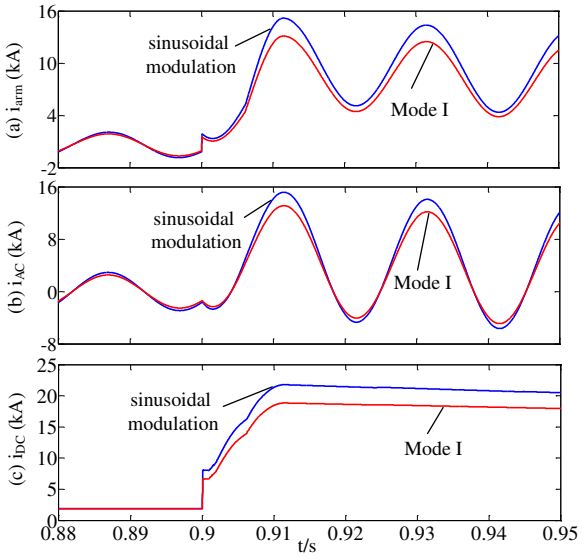

Fig. 11. Comparison between sinusoidal modulation and proposed control scheme during pole-to-pole DC fault: (a) arm currents, (b) AC currents, and (c) DC currents.

In this scenario, a permanent pole-to-pole DC fault is applied at the terminals of MMC_1 at t=0.9 s, Fig. 7. Both the stations are blocked after the fault and the circuit breaker action is not considered. As illustrated in Fig. 11 (a), the fault arm current peak is reduced from 15.2kA to 13.1kA by using the proposed control scheme, yielding lower fault current stresses on freewheel diodes. This is in good agreement with (28). The fault AC currents have the same peaks with arm currents and are also reduced to 86.6%, Fig. 11 (b). Similarly, the fault DC current peak is reduced by 13.4% and thus the lower capacity DC circuit breakers can potentially be used to isolate the fault, which reduces the capital cost and conduction losses of circuit breakers.

Only the waveforms for Mode I are shown in Fig. 11 for simplicity as Mode II has an identical effect on the reduction of fault current with Mode I.

V. Conclusion

The enhanced flat-topped modulation of MMC is proposed in this paper and the harmonic characteristics are presented by Fourier analysis. Compared to SVM, the dominant third harmonic is reduced by 33% and thus the voltage variation of the transformer terminals, neutral point and the potential zero-sequence current are correspondingly lowered. The Mode I control scheme with flat-topped modulation is a preferred option for the HVDC station without the transformer converter-side earthed, as its SM capacitance is slightly lower than that of Mode II. However, considering the zero triplen harmonics in Mode II during normal operation, Mode II control scheme provides a preferable option for the HVDC station with converter-side earthed.

Due to the injected triplen harmonics and higher voltage generating capability compared to sinusoidal modulation, SM capacitance with flat-topped scheme is reduced by 25%, which significantly reduces both the volume and capital cost of SMs. Additionally, station converter conduction losses are reduced by 11% and the capacity of cooling system is thus reduced. Although the converter-side voltage is increased, the DC fault currents are expected to be reduced by 13.4%, yielding lower fault current stresses on semiconductors and DC circuit breakers. Simulation results are in good agreement with the analysis, which demonstrates the effectiveness of the presented modulation scheme.

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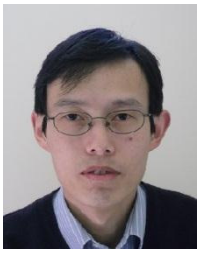

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