Long Term Testing and Analysis of Dielectric Samples Under DC Excitation

Edward Corr[1], W.H. Siew[2] and Weijia Zhao[3]
Institute for Energy and Environment
University of Strathclyde
Glasgow, UK
1 edward.corr@strath.ac.uk, 2 wh.siew@strath.ac.uk and 3 weijia.zhao@strath.ac.uk

***Abstract*— This paper details testing conducted under DC conditions on a dielectric sample containing internal voids. The DC testing was conducted using a ramp method to vary the voltage applied to the dielectric sample. The dielectric sample was de-energised for a week prior to two separate identical ramp tests and the results are presented showing the variability of PD activity. After the second ramp test an additional ramp test was performed in quick succession and PD activity was reduced, emphasizing the importance of de-energising the sample between tests. A major challenge associated with void type dielectric samples is ensuring that repeatable results are generated and possible approaches are discussed.**

Keywords— Cable insulation, Condition monitoring, HVDC transmission, Partial Discharges.

I. INTRODUCTION

HVDC transmission systems are expected to form a critical component in the UK power network in the coming decades. A number of applications are suited to HVDC transmission links; Interconnection to neighbouring countries (mainland Europe), bypassing bottlenecks in the transmission system (boundary between Scotland and England) and the connection of isolated generation sources (in particular offshore wind).

To minimise lost revenue for the system operator condition monitoring of HVDC transmission links could be employed to minimise the system downtime. Any system downtime brings significant costs for system repair and lost revenue from power transfer activities. Partial discharge (PD) detection is a common method employed to assess the condition of insulation in AC systems. The characteristics of PD under DC conditions are less understood than under AC conditions.

The majority of research to date on partial discharge testing under DC conditions has been conducted at TU Delft [1] and further research groups have built on this work [2]-[4]. The relevant test standard for PD detection is IEC 60270 which mainly deals with PD under AC conditions. Suggested revisions to IEC 60270 for PD detection under DC conditions are discussed by Hauschild *et al* [5] which recommends longer term testing under DC conditions with tens of minutes as opposed to tens of seconds under AC conditions.

This paper discusses the testing conducted on a dielectric sample under AC and DC conditions. The AC testing was performed to confirm the AC inception voltage and the dominant PD source in the samples under test. The DC testing was conducted using ramp test method [6]-[7]. AC analysis was performed by the visual inspection of phase resolved partial discharge (PRPD) plots [8]. In contrast there is no phase reference under DC conditions thus statistical methods must be employed for DC PD analysis [1].

This work builds on previous work detailing ramp testing of dielectric samples under DC conditions [9]-[10]. The ramp profile has been altered to reflect findings in previous work. The dielectric sample of most interest for HVDC systems is voids in insulation material representing internal discharge. Generally a void type dielectric sample requires extended periods of de-energisation (shorted to ground) for a number of hours/days prior to DC testing, to ensure representative PD activity is produced. The overall aim of this work is to discuss the issue of gaining repeatable results from a void like dielectric sample.

II. METHOD

One dielectric sample was tested in this paper. The sample was designed to represent internal discharge, five voids in an epoxy disc between two brass plain electrodes (Fig. 1). The five voids are air bubbles introduced during the casting of the epoxy disk sample. Two methods were adopted for AC and DC tests on the dielectric sample.

A. Method for AC testing

AC PD testing was performed according to IEC 60270 using the test circuit detailed in Fig. 2. The aim of the AC test was to determine the AC inception voltage for repetitive and sustained PD. The test voltage was incrementally increased until repetitive and sustained PD was observed on the PD

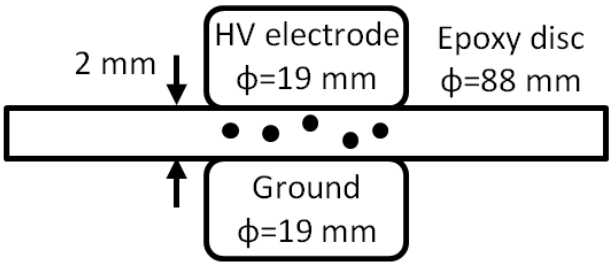

Fig. 1. Illustration of five voids in epoxy dielectric sample, not actual layout of voids.

The PhD research is funded by the EPSRC, project reference number EP/G037728/1.

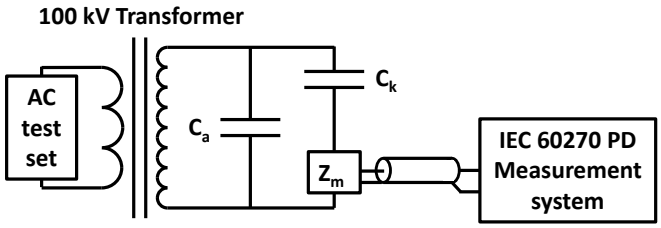

Fig. 2. AC test circuit with IEC 60270 detection system. The circuit consists of a C_a the sample under test, C_k the coupling capacitor and Z_m the measuring impedance connected to the IEC 60270 PD measurement system.

measurement system. The PD data was recorded over a 10 second period where charge from the PD pulses and the phase reference was recorded. PRPD plots are used analyse the PD behaviour from the voids sample.

B. Method for DC testing

A ramp test method was used during DC PD testing on the dielectric sample. Previous work [9] has been conducted using the peak value of the AC inception voltage (V_R) to determine three hold voltages for DC PD ramp testing. The three hold voltages are defined as $V_R/2$, V_R and $3V_R/2$. In the initial work the hold periods were 30 minutes. In this work the hold-duration at the lower voltages has been shortened and the hold-duration at $3V_R/2$ has been extended to 80 minutes. The revised ramp profile enables more data to be gathered whilst the PD from the dielectric samples was more active at elevated voltage. The data under analysis in this paper was gathered during the 80 minute hold at $3V_R/2$.

The test circuit and PD measurement system is detailed in Fig. 3. An AC power supply and a transformer were used to provide an elevated AC voltage. A diode rectifier converts the AC output from the transformer to DC to be applied to the standard IEC 60270 PD test circuit.

In previous work it was found that the voids sample required prolonged periods of de-energisation to discharge the sample. The sample was grounded for one week between two ramp tests. The PD emission from the dielectric sample was recorded using the PD measurement system for the full ramp test. The recorded parameters are PD charge and time of occurrence. A cumulative histogram was used to show the number of PD events which exceed certain charge levels. A histogram was used to show the number of PD events which fall into certain charge ranges. The relative PD behaviour in the two tests will be compared for consistency.

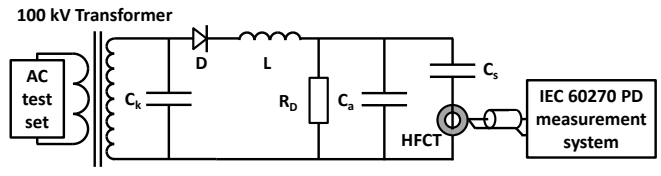

Fig. 3. DC test circuit diagram. AC test set connected to; a 100 kV transformer (100/0.38 kV single phase), coupling capacitor (C_k) of 1 nF, diode for rectification (D), an inductance (L), resistive divider (R_D) for voltage measurements (230:1), the sample under test (C_a), DC coupling capacitor (C_s) and IEC 60270 PD measurement system connected to the HFCT (Z_{trans}=4.3 V/A).

III. Results

The results from AC and DC testing are detailed in this section.

A. AC Results

The inception voltage for the voids sample was 8 kV rms. The PRPD plot for the voids sample at 8 kV rms is detailed in Fig. 4. The PRPD behaviour for a void type discharge leads the test voltage peak and the PD activity generally extinguishes after the test voltage peaks. The PRPD plot shows similar behaviour in the first and third quadrants, as expected for a void type discharge. The AC testing has confirmed that the dominant PD source in the dielectric sample is internal discharge. The inception voltage has been determined and this voltage will be used to define the voltage steps in the DC ramp-test.

B. DC Results

Two DC tests were conducted on the voids in epoxy dielectric sample. In both cases, prior to each ramp test, the sample was de-energised for a week. The AC inception voltage of the sample was 8 kV rms and thus the peak value was 11.3 kV. The three hold voltage for the ramp test was 5.6 kV, 11.3 kV and 17 kV. Initial testing on the five-void sample found that an additional step in the ramp should be added. The final hold voltage was 20 kV for 80 minutes to ensure consistent and repetitive PD from the dielectric sample.

1) DC ramp 1

In the first test 85 PD events were recorded over the 94 minute ramp test: the polarity of all the PD events was all positive. The only exception was over the voltage drop from 20 kV to 5.6 kV at 92 minutes where negative PD events were detected. The PD activity over the first ramp test is detailed in Fig. 5.

The results show a concentration of PD activity around the rise in voltage between each step with PD activity generally reducing in magnitude and less frequent following a change in voltage. This behaviour was expected for an internal discharge sample [1]. The PD measurement system was saturated at both $3V_R/2$ and $1.8V_R$ and the attenuation was quickly increased when this was encountered to avoid loss of PD data. The 80 minutes of hold data at 20 kV was not affected by the saturation issue. During the 80 minute hold at 20 kV 27 PD

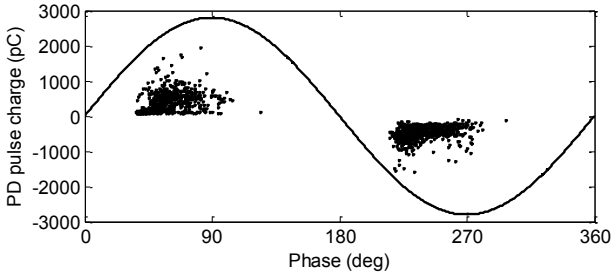

Fig. 4. PRPD plot for the five voids sample at 8 kV rms, PD data (shown as dots) is leading the test voltage peaks of the AC supply (black line).

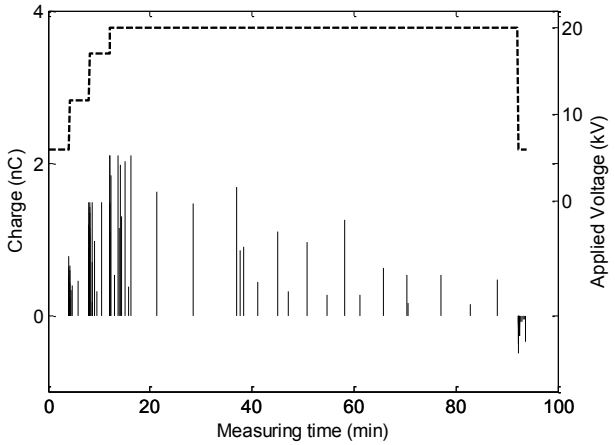

Fig. 5. PD charge pulses and voltage ramp for the first 94 minute test.

events were recorded.

Two methods were applied to the PD data to assess the distribution of PD charge magnitude over the 80 minute hold period. The first method was the use of histograms, which enable a visual representation of the spread of PD data. Fig. 6 details the histograms generated from the recorded PD activity. The second method was the calculation of skewness and kurtosis, a numerical approach to characterise the distribution of the raw PD data. Skewness is a measure of the symmetry of the distribution around the mean and kurtosis is a measure of the sharpness of the peak of the distribution. The skewness for the 80 minutes of hold data was 0.38 and the kurtosis was found to be 1.76.

1) DC ramp 2

The second ramp test utilized the same ramp profile. Before the test the attenuation of the PD measuring system was set to the maximum required in the first positive test to avoid saturation of the measurement system. In this test 179 PD events were recorded during the 94 minute ramp. The PD activity over the second ramp test is detailed in Fig. 7.

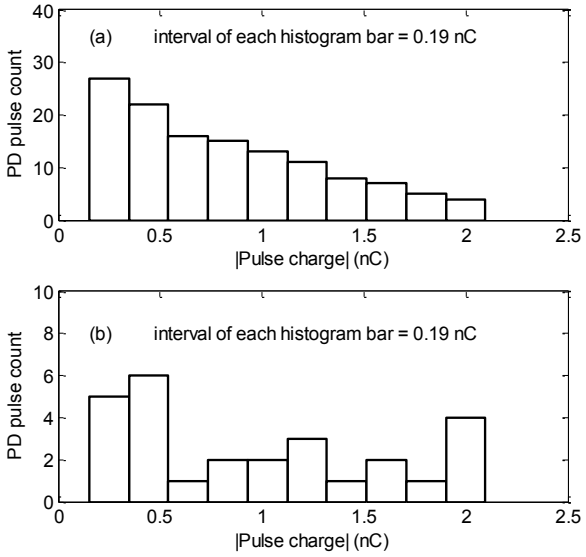

Fig. 6. Statistical analysis for the first ramp test for the 80 minute hold at 20 kV (a) cumulative histogram detailing the number of PD events which exceed certain charge levels (b) histogram detailing the number of PD events which fall into certain charge ranges.

The results show PD activity increases in frequency and magnitude following a voltage change. Following the voltage change the PD generally decays and continues sporadically over the 80 minute hold at 20 kV. The PD events are generally smaller and more frequent than the first positive test. This difference is reflected in the histograms with a larger number of smaller PD events evident in the data.

In the second test twice as many PD events were recorded in the first bar of the histogram (Fig. 8 (b)) than during the whole of the first ramp test. The skewness for the 80 minutes of hold data was 2.6 and the kurtosis was 10.31. The second ramp test has a more positive skew, more of the charge data was focused in the lower end of the distribution. The value of kurtosis was also higher indicating a shaper peak in the distribution of data. The skewness and kurtosis provides numerical values for the distributions of data in each of the two ramp tests.

A further ramp test was performed in quick succession to the second ramp test and the total number of PD events reduced from 179 to 103 events. This shows the relative reduction in PD activity that occurs once the dielectric sample has been energized. It should be noted that the further ramp has more PD events than the first ramp (85). The importance of the de-energisation period between subsequent ramp tests needs further investigation to ensure repeatable results are obtained.

IV. Discussion

The ramp profile used in previous work consisted of a hold of 30 minutes on all voltage steps. A revised ramp profile was adopted with the final hold voltage extended to 80 minutes and all holds at lower voltages shortened to 4 minutes. The aim of this change was to allow more PD activity to be recorded at the highest voltage in the ramp test. The increased PD activity ensures statistical analysis methods are more effective with more data available.

An additional voltage step was added to the DC ramp profile. Initial testing indicated that the 80 minute hold voltage

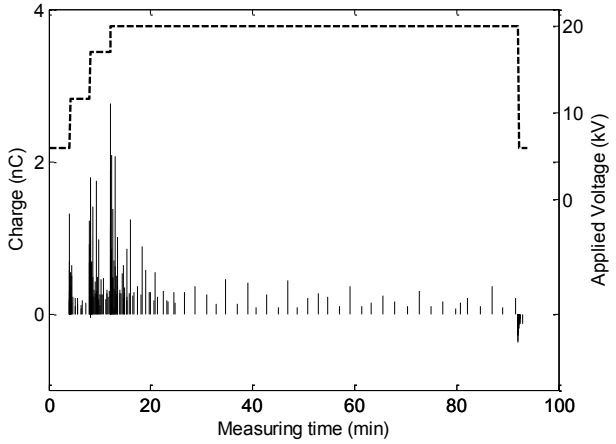

Fig. 7. PD charge pulses and voltage ramp for the second 94 minute test.

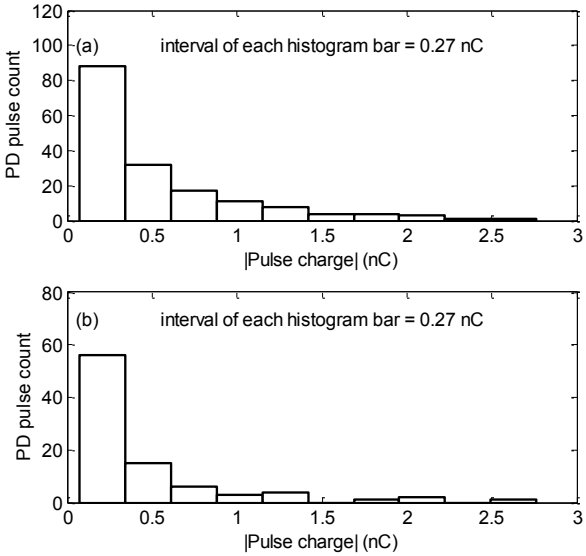

Fig. 8. Statistical analysis for the second ramp test for the 80 minute hold at 20 kV (a) cumulative histogram detailing the number of PD events which exceed certain charge levels (b) histogram detailing the number of PD events which fall into certain charge ranges.

should be raised from 17 kV ($3V_R/2$) to 20 kV ($1.8V_R$). This was achieved adding a further step to the ramp. The final ramp had four steps in total, three steps ($V_R/2$, V_R and $3V_R/2$) where the hold was for 4 minutes and the final 80 minute hold at $1.8V_R$. This change was made to ensure PD was apparent from the sample for the 80 minute hold.

A reduction in PD activity was apparent when the de-energisation period was removed for the ramp test which was in quick succession to the second ramp. The ability to perform repeatable and consistent tests on void type dielectric samples requires further investigation. Possible ways of achieving this could be; to perform polarity reversal on the dielectric sample to dislodge trapped charge on the void walls or strategic use of AC tests either pre or post DC PD testing.

The first ramp test produced 85 PD events over the full ramp test and this was significantly less than in the second ramp test where 179 events were recorded. The distribution of PD charge was different in the two tests. The second test had a larger number of smaller PD events making up a significant proportion of the PD activity. The difference in distributions was reflected in the measures of skewness and kurtosis for both 80 of the minute holds at 20 kV.

V. Conclusion

This paper has demonstrated the process of testing a dielectric sample under AC conditions to establish the inception voltage (the voltage at which repetitive and sustained PD was apparent from the dielectric sample). The PD behaviour of the dielectric sample was confirmed by the visual inspection of a PRPD plot.

The ramp test method was employed for DC testing of the dielectric sample. The AC inception voltage was used as a basis for calculating the hold voltages in the DC ramp. Modifications were required to the ramp to ensure repetitive PD was apparent during the 80 minute hold.

The distribution of PD data was analysed in a number of ways. A visual approach to assess the spread of PD data was employed through the use of a cumulative histogram and a histogram. The use of statistical methods (skewness and kurtosis) enabled the analysis of the distribution of PD activity from the dielectric sample in a numerical approach.

The test results discussed in this paper highlight the variability of PD activity when performing DC testing on a void type dielectric sample. The reduction in PD activity observed when performing back to back DC testing on a voids type sample confirmed that without a de-energisation period PD activity reduced. The impact of the de-energisation period on the dielectric sample requires further investigation due to the difference in PD activity recorded in the first and second ramps. The work has also demonstrated the need to investigate test methods to ensure more consistent results are produced from void type dielectric samples.

Acknowledgment

The PhD research is funded by the EPSRC, project reference number EP/G037728/1 and is done in collaboration with High Voltage Partial Discharge Ltd (HVPD).

References

[1] P.H.F. Morshuis and J.J. Smit, “Partial discharges at dc voltage: their mechanism, detection and analysis”, IEEE Trans. Dielectr. Electr. Insul, Vol. 12, No. 2, pp. 328-340, Apr. 2005.

[2] W. Si, J. Li, P. Yuan and Y Li, “Digital detection, grouping and classification of partial discharge signals at DC voltage”, IEEE Trans. Dielectr. Electr. Insul, Vol. 15, No. 6, pp. 1663-1674, Dec. 2008.

[3] H.Q. Niu, A. Cavallini and G.C. Montanari, “Identification of partial discharge phenomena in HVDC apparatus”, IEEE Int. Symposium on Electr. Insul, pp. 373-376, June 2008.

[4] P. Morshuis and G. Hoogenraad, ”Partial discharge diagnostics for DC equipment”, Int. Symp. on Electr. Insul, pp. 407-410, June 1996.

[5] W. Hauschild, E. Lemke, 2014, High-Voltage Test and Measuring Techniques, Springer, 281-283

[6] R.S. Bever, J.L. Westrom, “Partial discharge testing under direct voltage conditions”, IEEE Trans. Aerosp. Electron. Syst, Vol. AES-18, No. 1, pp. 82-93, Jan. 1982.

[7] R.S. Bever, “Ramp technique for partial discharge testing”, IEEE Trans. Electr. Insul, Vol 20, No. 1, pp. 38-46, Feb. 1985.

[8] F.H. Kreuger, “Partial discharge detection in high-voltage equipment”, Butterworth and Co. LTD, London, UK, 1989, pp. 129-152.

[9] E. Corr, W.H. Siew, “Analyses of partial discharges in dielectric samples under DC excitation”, UPEC, Sept. 2015.

[10] M. Seltzer-Grant, W.H. Siew, E. Corr, X. Hu, M. Zhu, M. Judd, A. Reid and A. Neumann, “Laboratory and field partial discharge measurement in HVDC power cables”, 9th International Conference on Insulated Power Cables (Jicable), June 2015.