DESIGN, AUTOMATION & TEST IN EUROPE
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The European Event for Electronic System Design & Test

Model Based Design For 4G And 5G Wireless Communications *Software Defined Radio* Using Matlab & Simulink

Bob Stewart (Presenter)
Louise Crockett, Kenneth Barlee, Dale Atkinson

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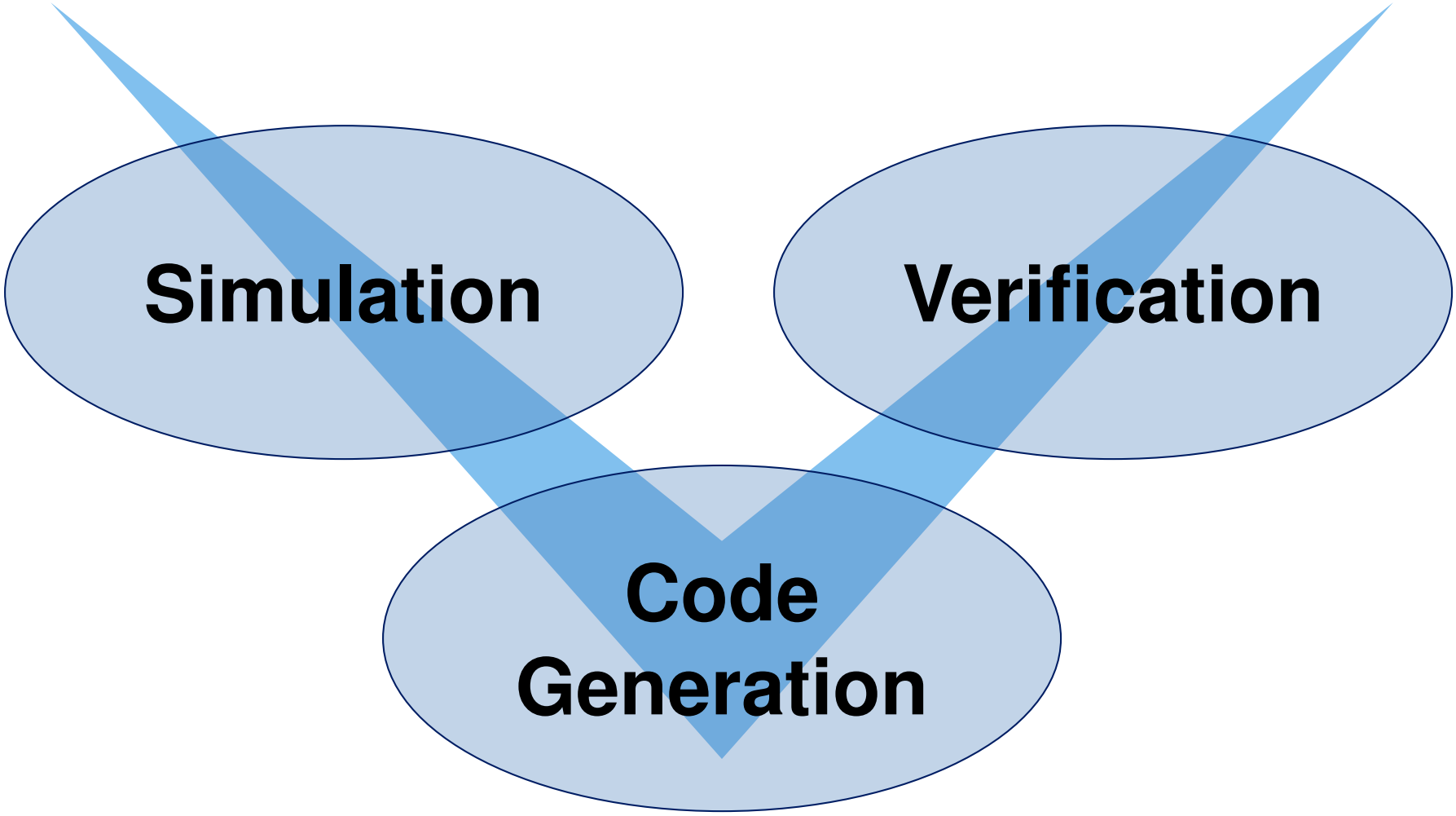
MathWorks®

Model Based Design and Verification, 16th March 2016

Model Based Design for 4G & 5G Wireless Communications
Software Defined Radio Using Matlab & Simulink



Bob Stewart, MathWorks Professor, University of Strathclyde

Software Defined Radio – 'White Space' Networks

- **Glasgow TV White Space Pilot: 2013-2015**

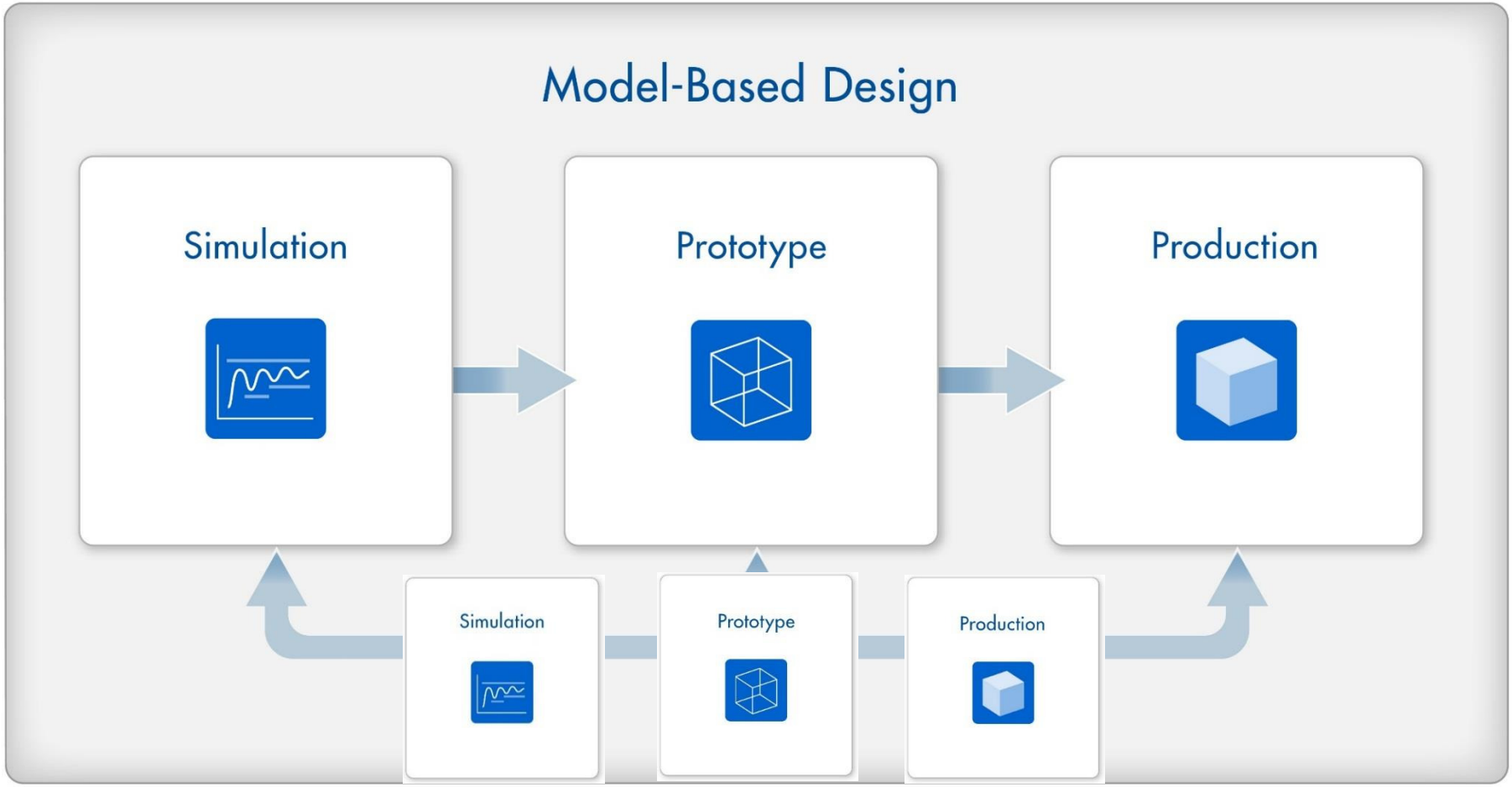
  (Part of UK OfCom Pilot Programmes: http://media.ofcom.org.uk/news/2015/tvws-statement/)

Project Partners:

Microsoft sky SPECTRUM BRIDGE The Scottish Government 6HARMONICS CONNECTING PEOPLE & THINGS ADAPTRUM MEDIATEK MathWorks

Model-Based Design

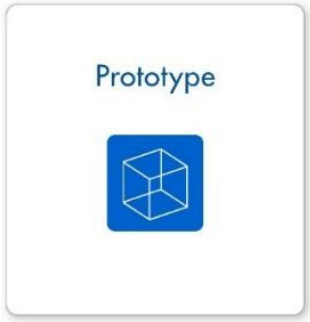
A single shared development environment



Model-Based Design

A single shared development environment

Simulate DSP & Communications algorithms and realise fixed point implementations



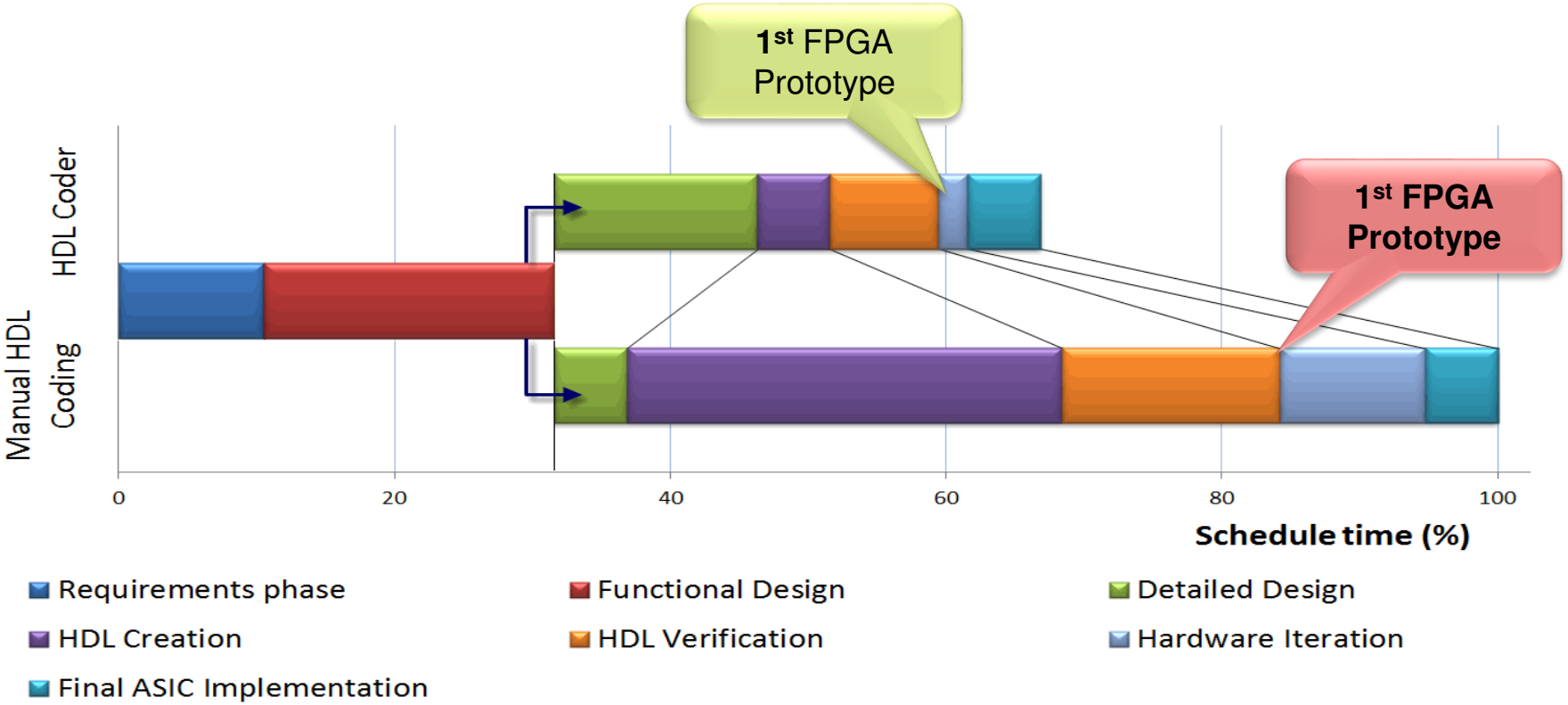
Prototype HDL implementations and validate performance via co-simulation

Produce design on target FPGA and Supported radio hardware.

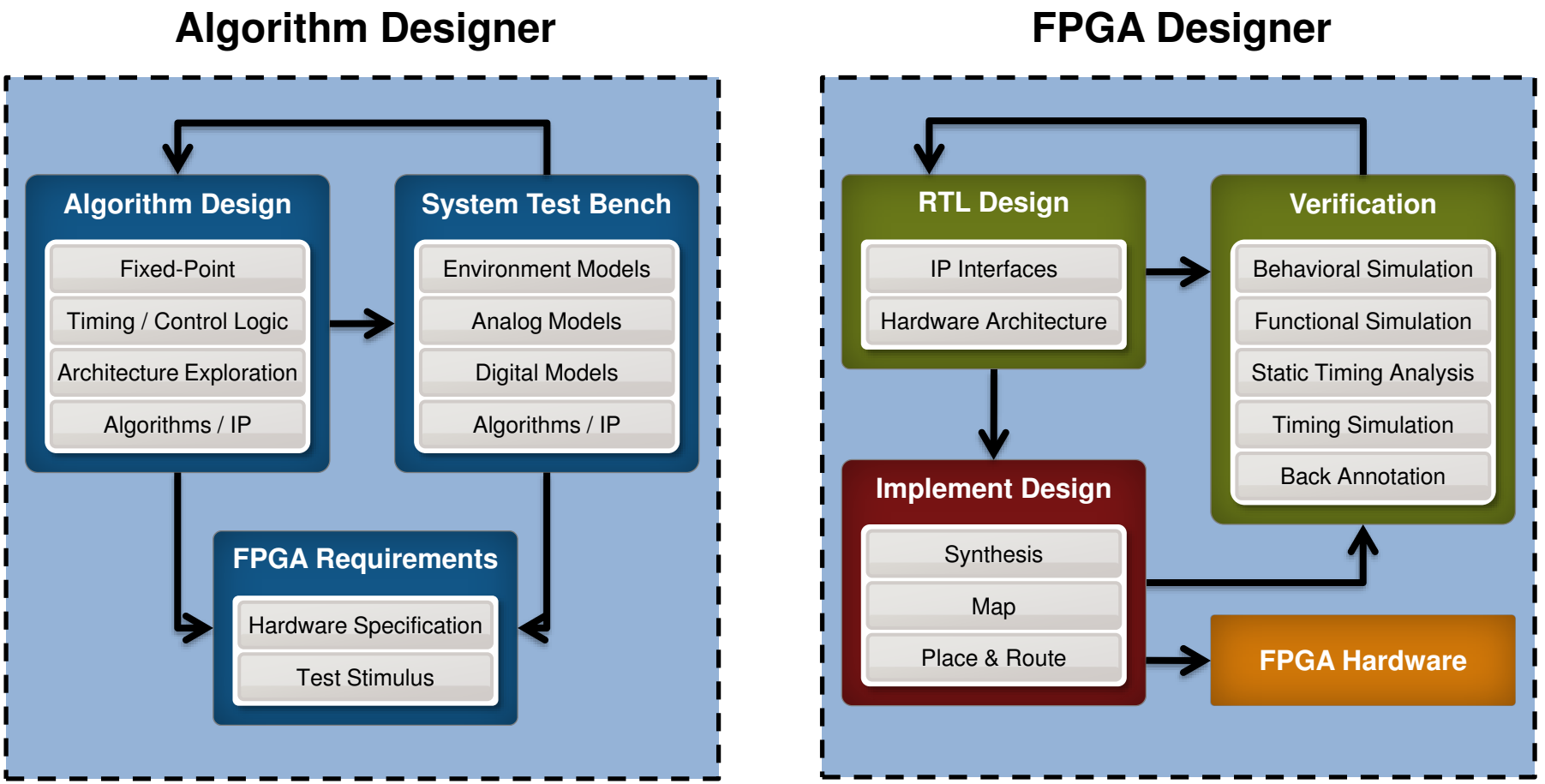
Why Model-Based Design for FPGA Systems?

Reduce implementation time

- Reduced FPGA prototype development schedule
- Shorter design iteration cycles
- Improved product quality

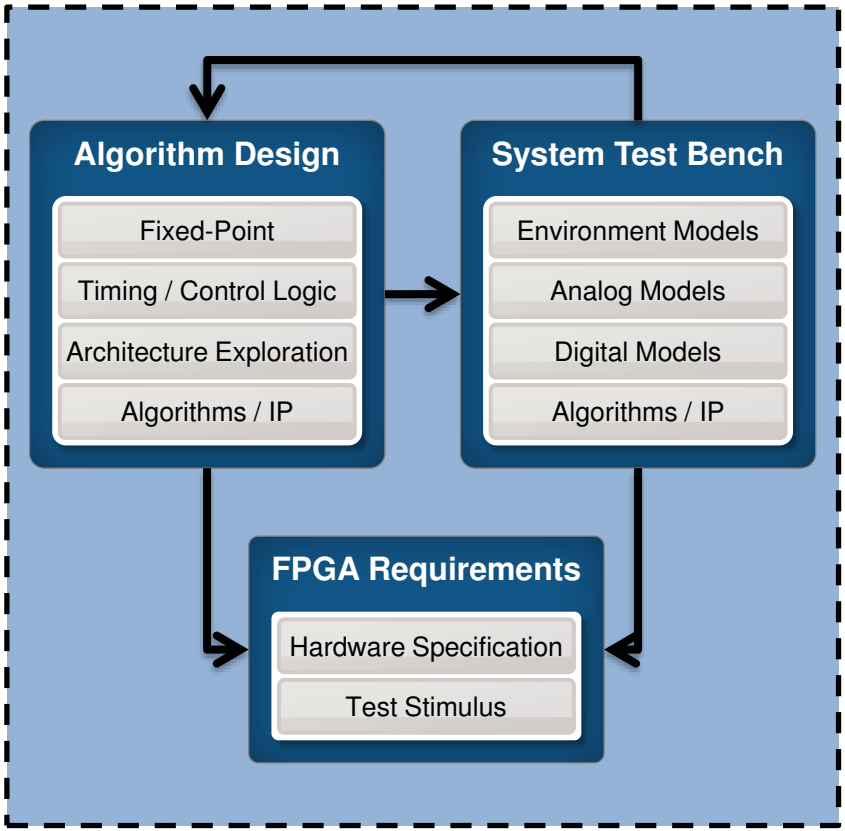


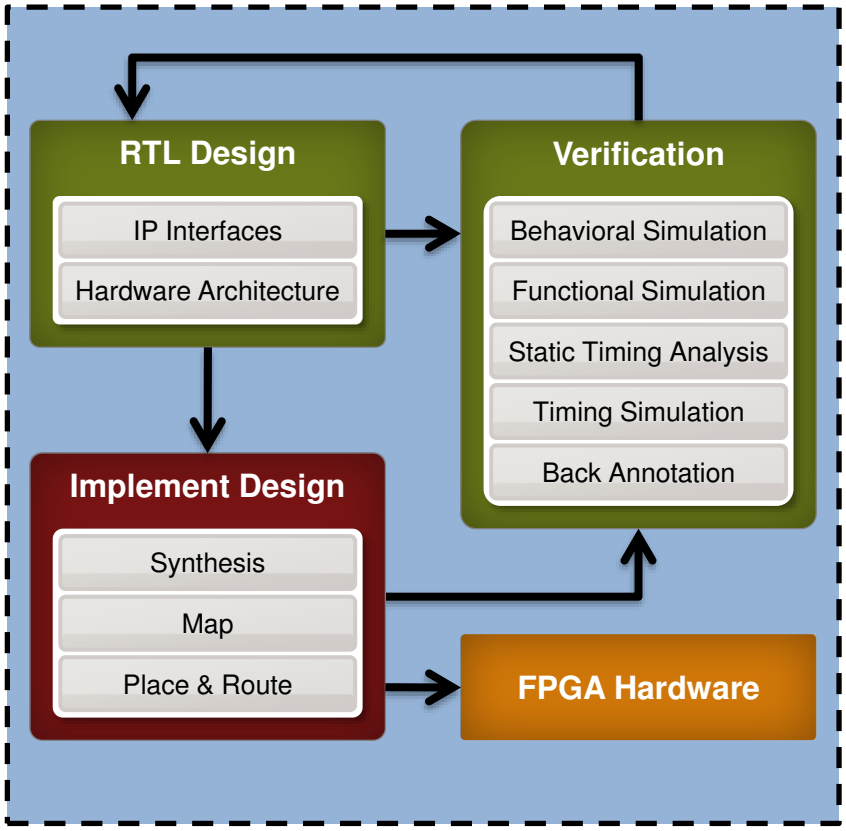
Separate Views Implementation



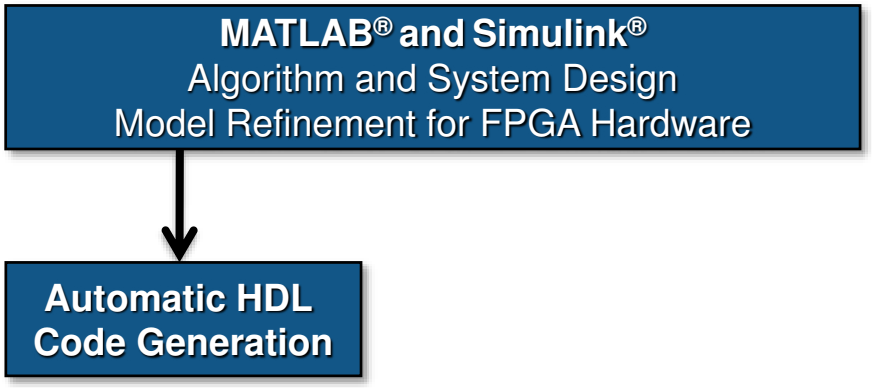
Model-Based Design for Implementation

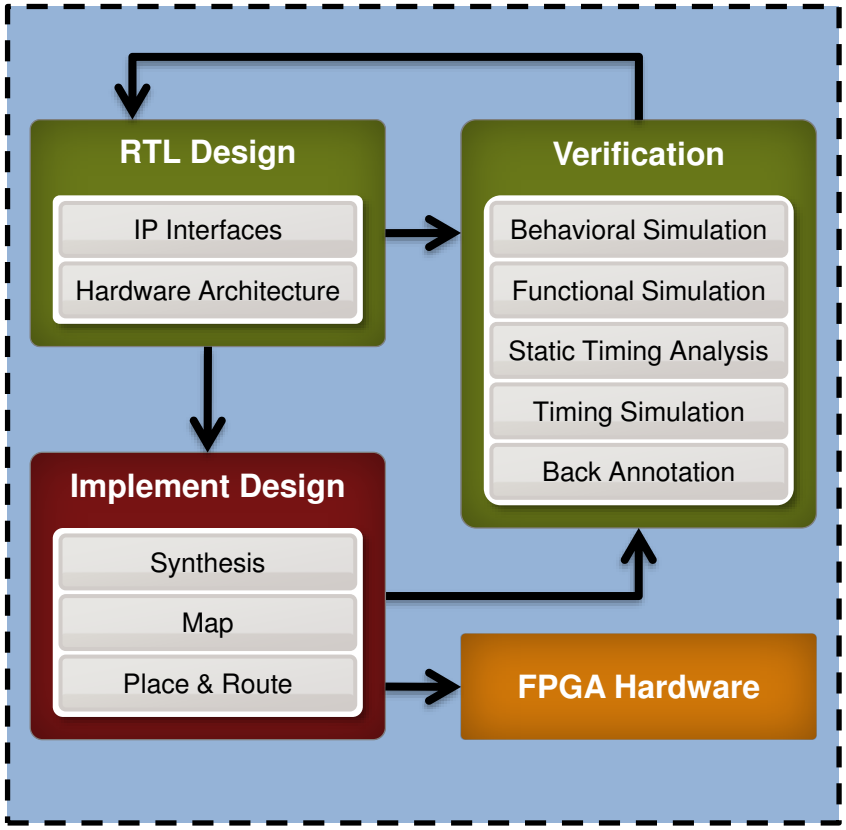
MATLAB® and Simulink®
Algorithm and System Design





Model-Based Design for Implementation





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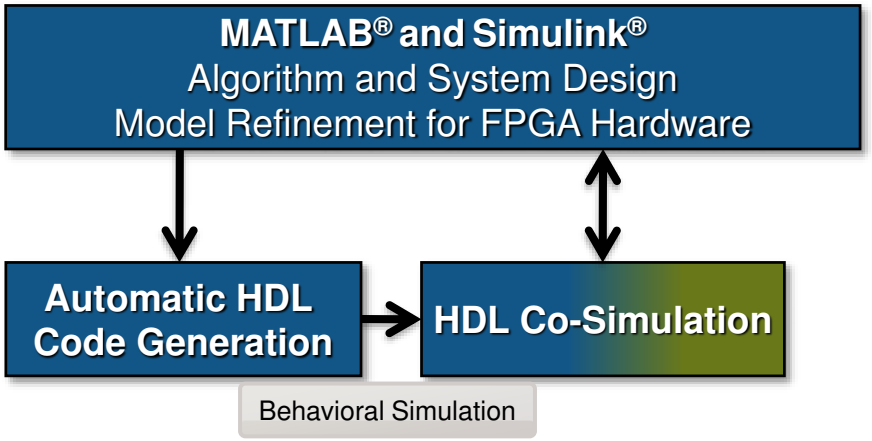

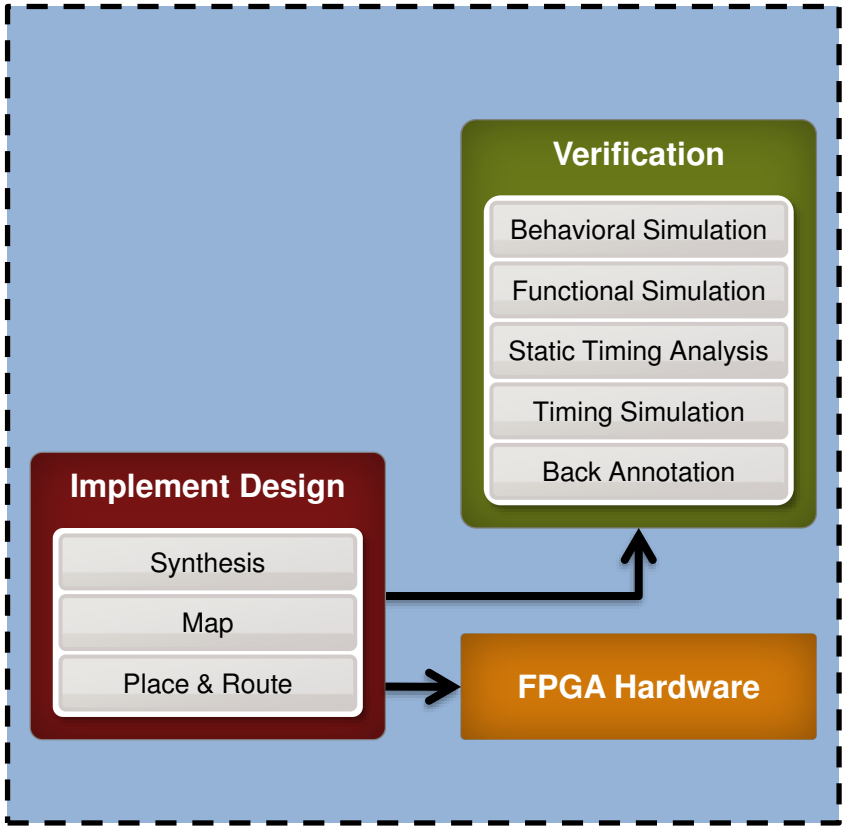

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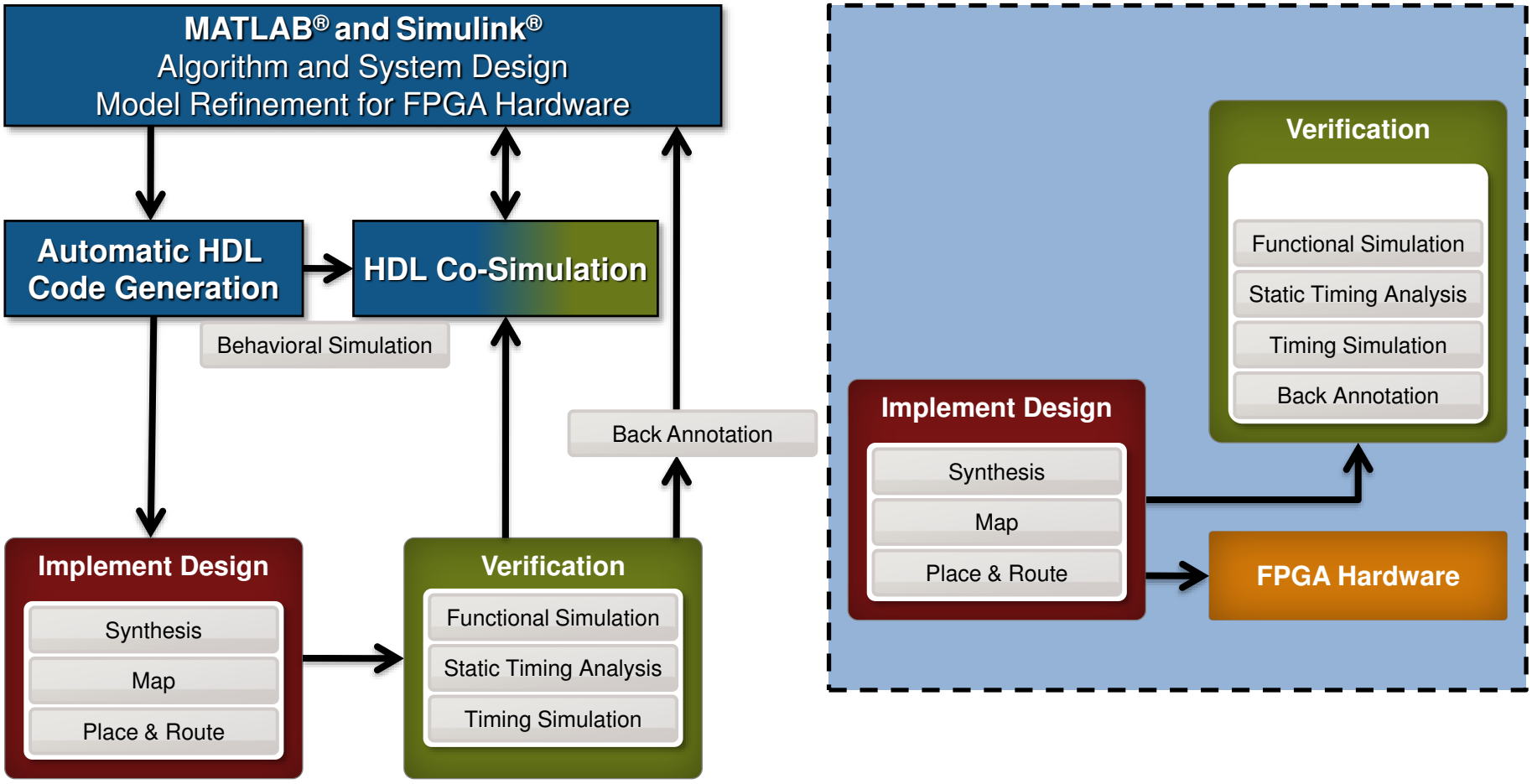

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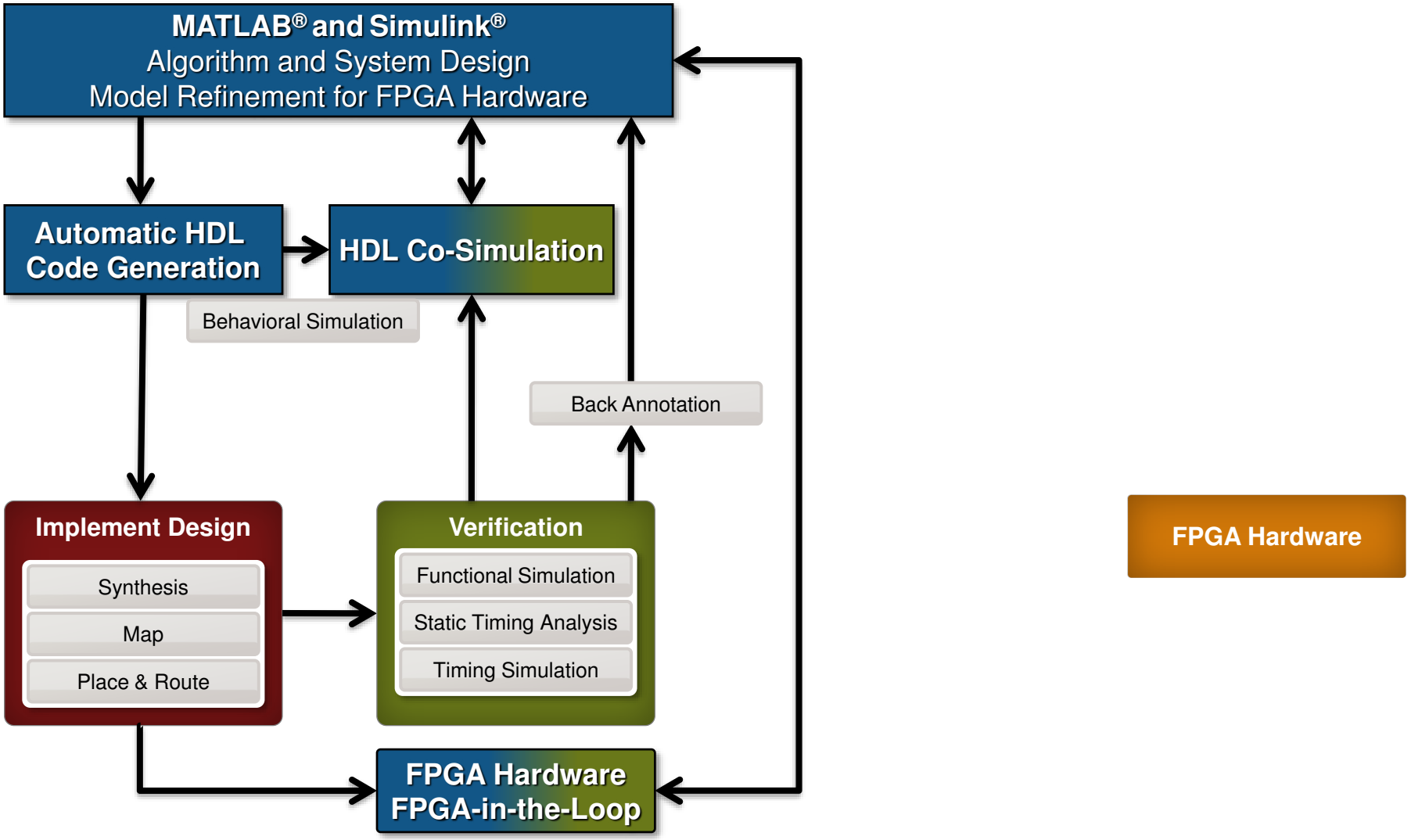
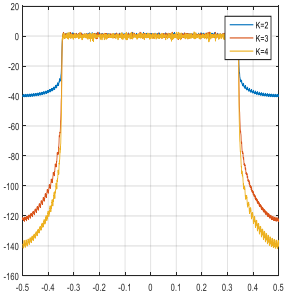


So what is 5G?

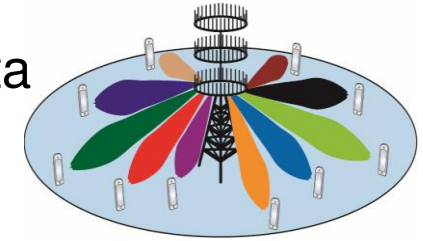
Generation	Device

Some 5G DSP and Comms Challenges

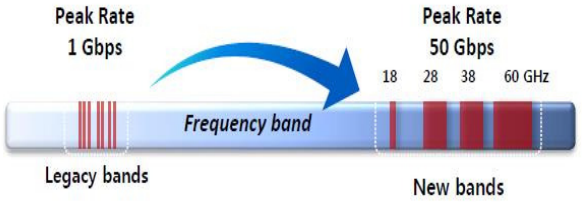


- **New Modulation Schemes**
  - Performance characteristics of FBMC, UFMC, etc.
- **More Antennas**
  - Beamforming and precoding algorithms
  - Antenna arrays and Massive MIMO

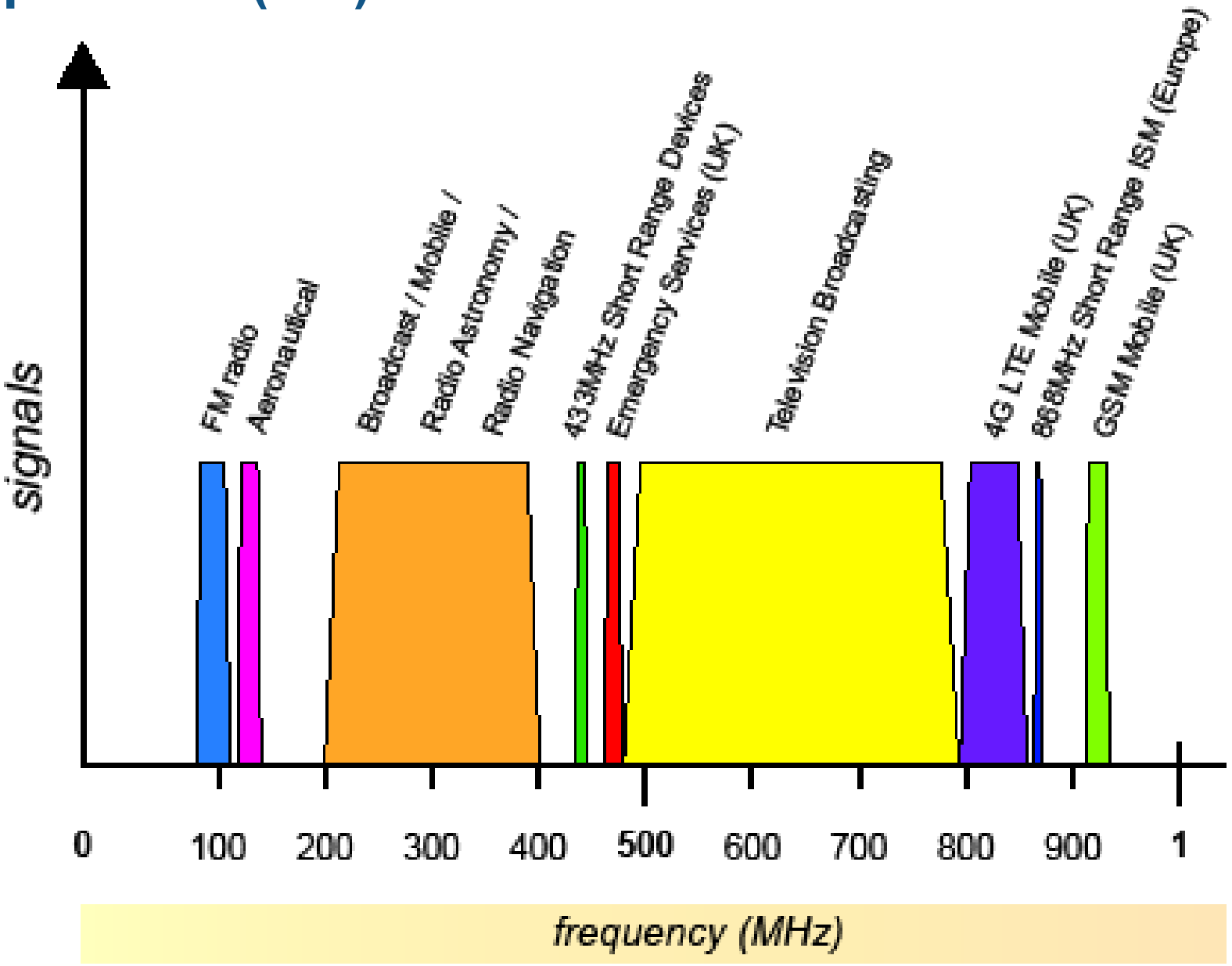
- **New Frequency Bands**
  - RF system architectures design in
  - Advanced Antenna, RF and DSP Co-Design
  - Channel modeling from real-world measurement data



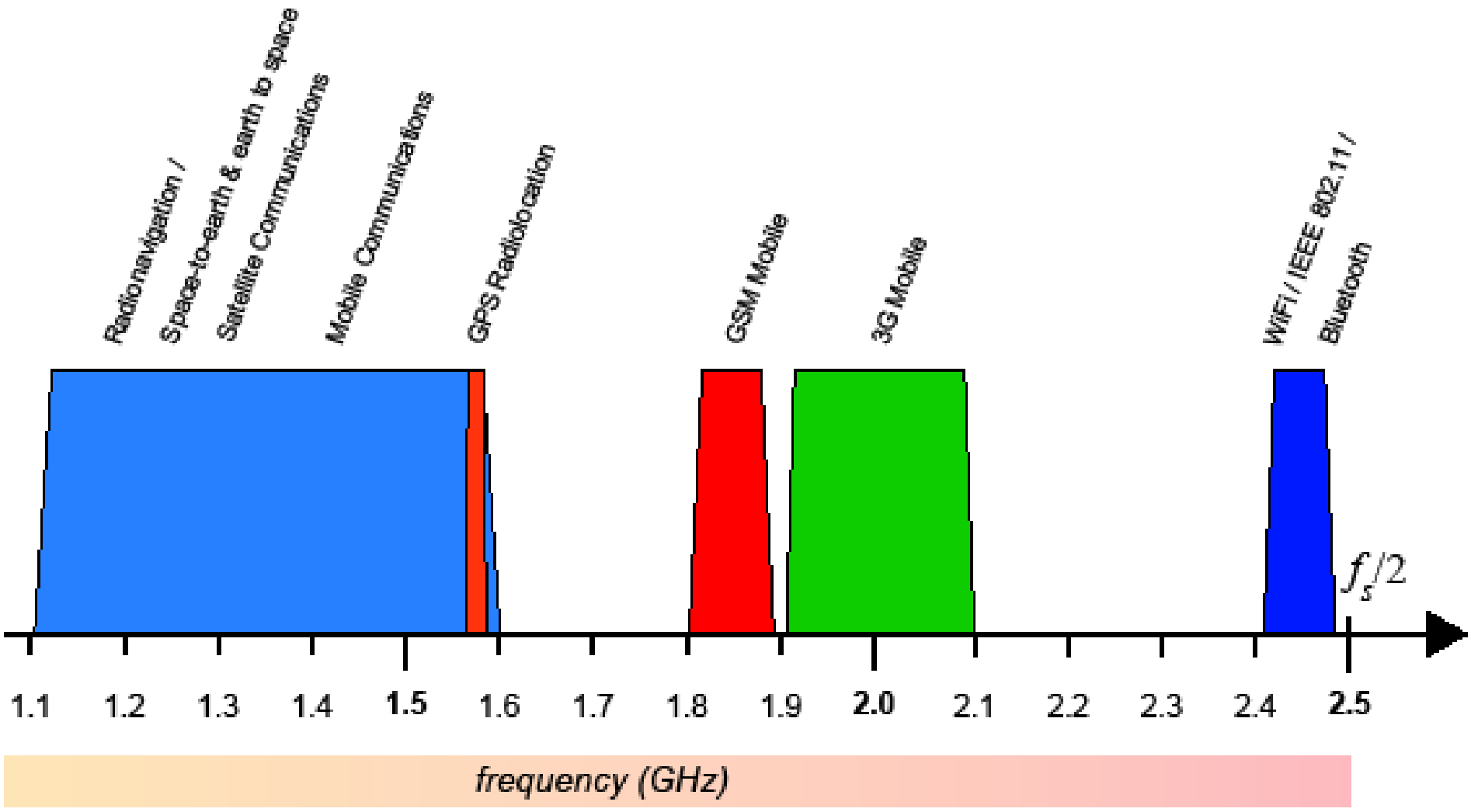
- **Dynamic Spectrum and SDR**
  - Versatile cognitive radios
  - Secondary spectrum users
  - Spectrum databases



Spectrum (UK)… 50MHz to 1GHz



Spectrum (UK)… 1GHz to 2.5Hz



Software Defined Radio – 'White Space' Networks

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  (Part of UK OfCom Pilot Programmes: http://media.ofcom.org.uk/news/2015/tvws-statement/)

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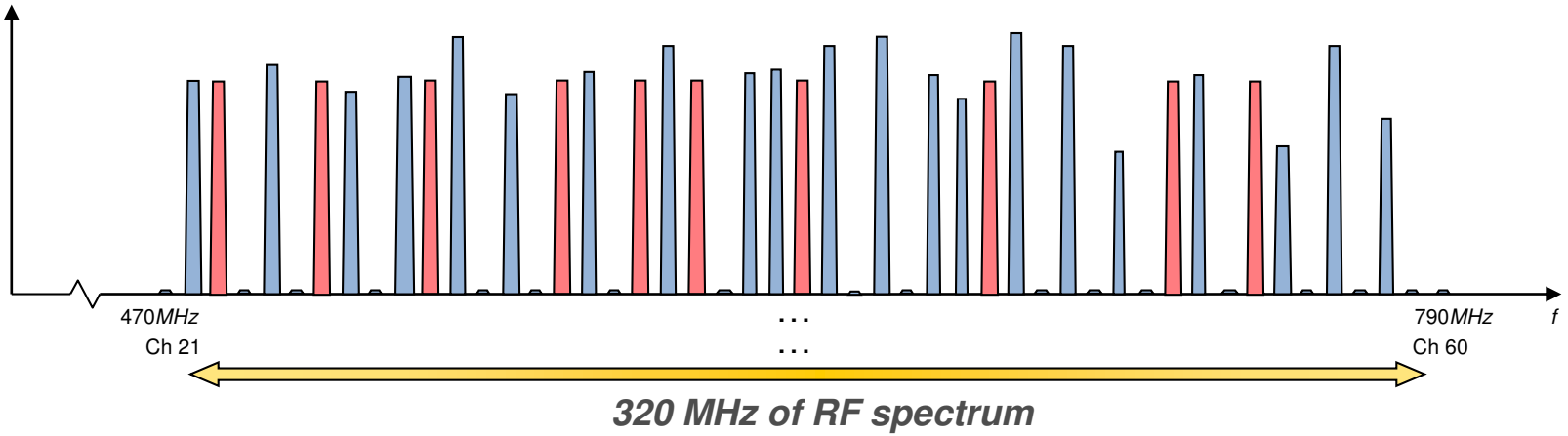
What are the TV 'White Space' frequencies?

- Up to **40 channels** of **8MHz** each from **470MHz to 740MHz.**
- Depends where you are as to available frequencies.
- In UK TV white space (TVWS) you are a **secondary user**

  … the primary users are the terrestrial TV broadcasters.
- If you *transmit* on TVWS then do by the *rules.*
- Requests go to the TVWS database.



TV White Space – Dynamic Spectrum Access

- Regulators around the world are recognizing the importance of TV white space and have been progressing towards the creation of regulatory frameworks
  - Licence-exempt
  - Access controlled by regulator-approved database
- US regulator (FCC) was first to legalize licence-exempt access to TV white spaces in the US, in 2008, and revised in 2010.
- UK regulator (Ofcom) has proposed a more ambitious and more flexible approach, which will increase the efficiency with which this spectrum can be harnessed – *access opened January 2016*
- Many other regulators are also progressing towards regulation.

Ofcom

FCC

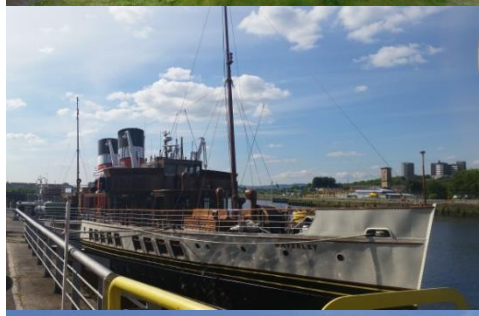
Glasgow TVWS Pilot: Testing & Demonstrating

- Testing TVWS performance in built-up urban areas
- Demonstrating applications:
  - Video Camera
  - Sensor Networks

- Contributing to OfCom regulatory activities:
  - Ofcom test team visits
  - Contributing to Ofcom consultations
  - Working with industry partners and Government

Glasgow TVWS Pilot Activities

- Helping Ofcom to validate its proposed dynamic access framework
- Demonstrating higher-level benefits of using White Space spectrum
  - Outdoor webcams
  - Wi-Fi internet access in campus garden areas
- Helping to assess new technologies
  - e.g: IEEE 802.11af (Wi-Fi in TVWS)
  - Protoyping and proof of concept of other standards
  - LTE implementation



Glasgow White Space Network

- Phase 1: 2014/15 : PTMP TVWS network:
  - Wi-Fi internet access in outdoor garden areas
  - Outdoor webcams
  - Deployed at Strathclyde University City Campus

Radios used in Glasgow TVWS Pilot

- TVWS Pilot used 3 different radios from vendors:
  - ***Adaptrum*** (Proprietary Standard)
  - ***6 Harmonics*** (based on IEEE 802.11)
  - ***MediaTek*** (IEEE 802.11af based)
  - (Also test radios; ***Ubiquity*** XR7)

- But what if we want to test **LTE** in White Space frequencies – there is no radio available (*at present*!)?

- So we achieve with fast SDR LTE TVWS prototyping using ***Model Based Design*** to target FPGA SDR platforms.

Prototyping for SDR in TV White Spaces

Simulation

DSP/Comms Design & Verification

Simulate DSP baseband and IF/RF systems

Protoype

Fixed Point HDL implementation & LTE

LTE Tx and Rx and TVWS Channeliser/Modulator

Production

Prototyping and Implementation

Deploy algorithms onto target FPGA / SDR system

Model Based Design of SDR for LTE in TVWS

Floating Point Simulation	• **MathWorks *DSP System* & *Comms* Toolbox** • Design 470-740 MHz TVWS Filter Bank
Fixed Point Optimisation	• **MathWorks *Fixed Point Designer*** • Implement TVWS Filter Bank in Fixed Point
VHDL Implementation	• **MathWorks *HDL Coder*** • Design verified HDL code for TVWS Filter Bank
LTE Baseband	• **MathWorks *LTE Systems Toolbox*** • Implement LTE Transmit and Receive
FPGA SDR Implementation	• **MathWorks *Zynq SDR Support Package*** • Implement Tx and Rx TVWS Filter banks

So what do we need for the TVWS LTE SDR?

Software:

- MATLAB & Simulink
- DSP Systems Toolbox
- Communications System Toolbox
- LTE Systems Toolbox
- Fixed Point Designer
- HDL Coder
- Zynq SDR Hardware Support Package

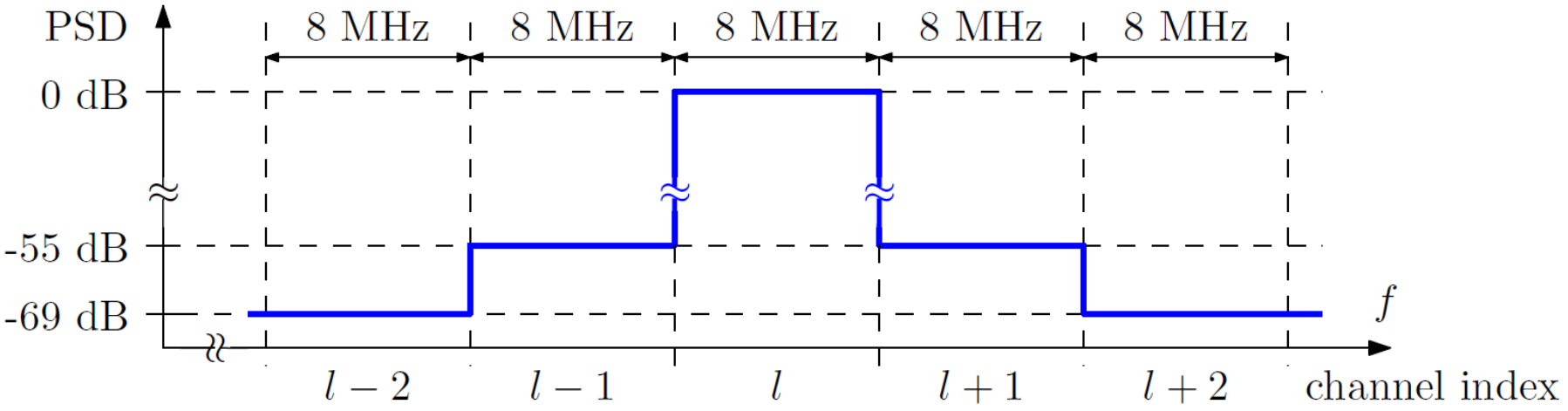
Hardware

- Xilinx Zynq FPGA Board & ADI FMComms RF Tx/Rx Card
- Radio front ends/amplifier and antennas

Floating Point Simulation

- **MathWorks DSP System & Comms Toolbox**
- Design 470-740 MHz TVWS Filter Bank

- Need a 40 channel agile filter bank
- First design prototype FIR filter using **DSP System Toolbox**
- Compliant with TVWS 8MHz channel mask
- TVWS Transmit design satisfies the spectral mask below

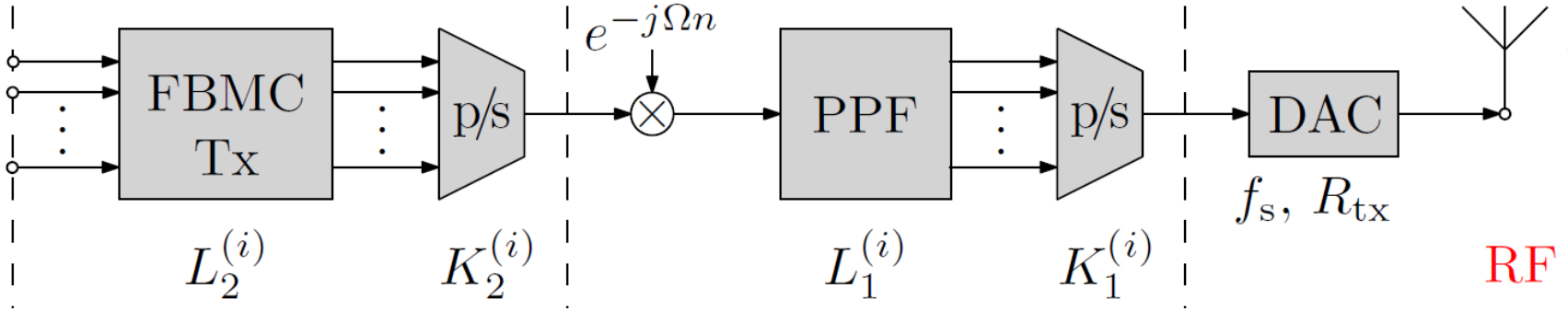


Floating Point Simulation

- **MathWorks DSP System & Comms Toolbox**
- Design 470-740 MHz TVWS Filter Bank

- Filter Bank Multicarrier (FBMC) synthesis bank combines 40 TVWS baseband channels each of 8MHz.
- Polyphase filter (PPF) and complex frequency correction translates the baseband to TVWS 470MHz to 790MHz.

(Full paper on design at: R. A. Elliot, M. A. Enderwitz, K. Thompson, L. H. Crockett, S. Weiss and R. W. Stewart, "Wideband TV White Space Transceiver Design and Implementation," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 1, pp. 24-28, Jan. 2016.)



Floating Point Simulation

- **MathWorks DSP System & Comms Toolbox**
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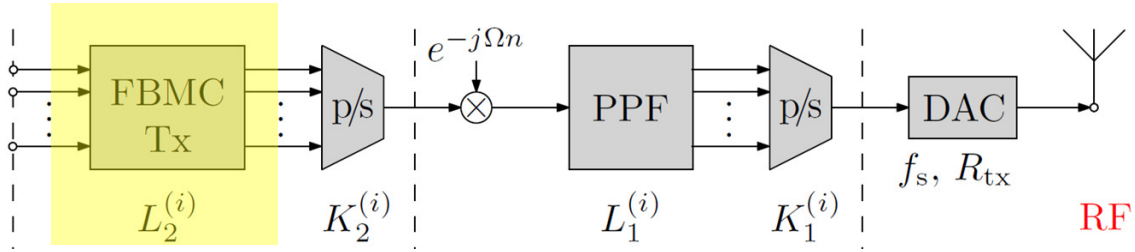
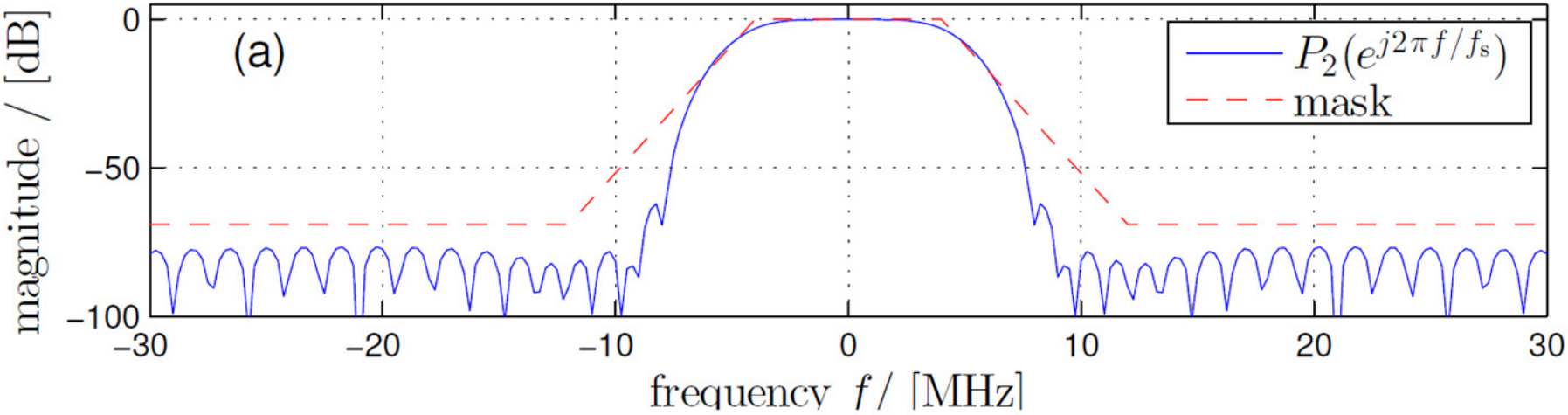
- Prototype Filter Design – Nyquist Root Raised Cosine with adjacent channel leakage of -69dB.

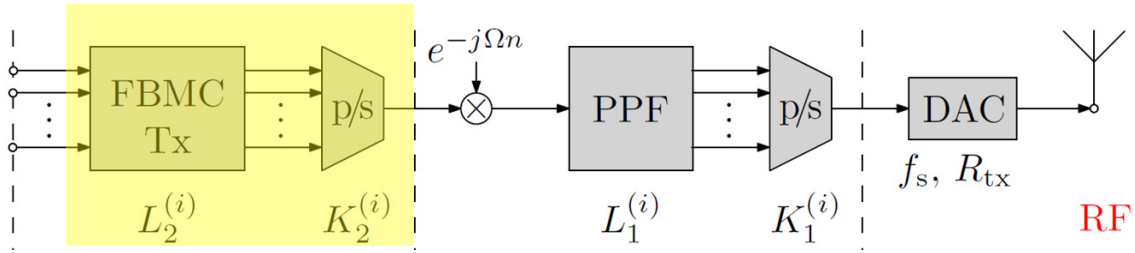


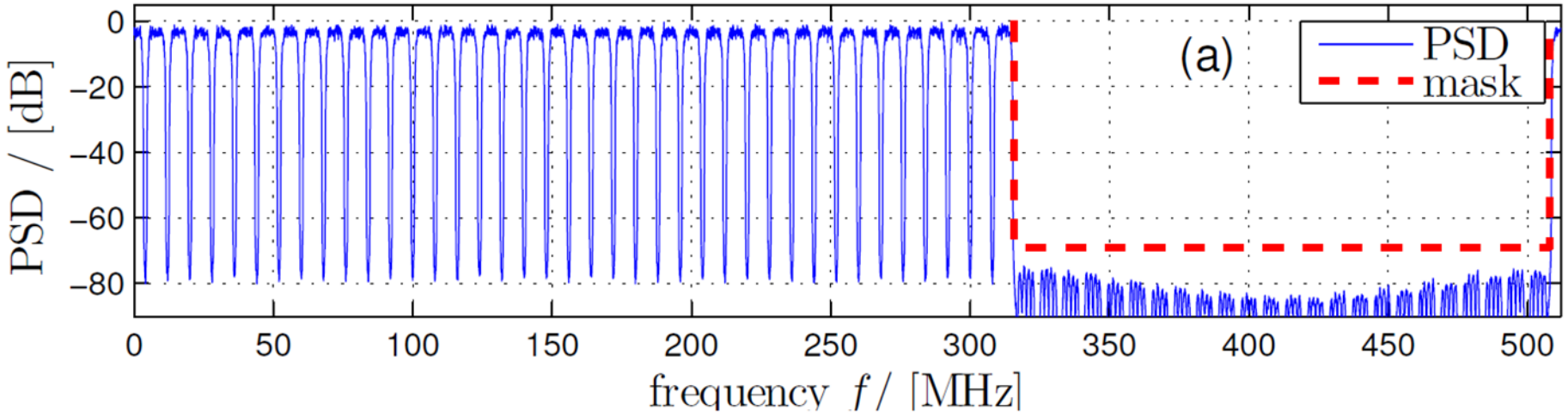


Floating Point Simulation

- **MathWorks DSP System & Comms Toolbox**
- Design 470-740 MHz TVWS Filter Bank

- Power spectral densities (PSD) after 40 x 8MHz filter bank (each TVWS channel loaded here with a 5.33MHz signal).

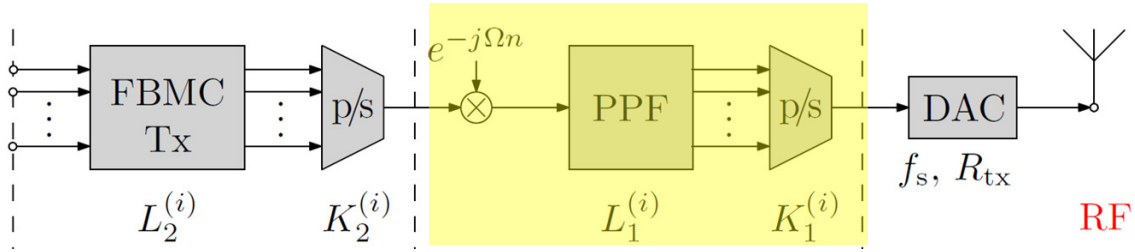


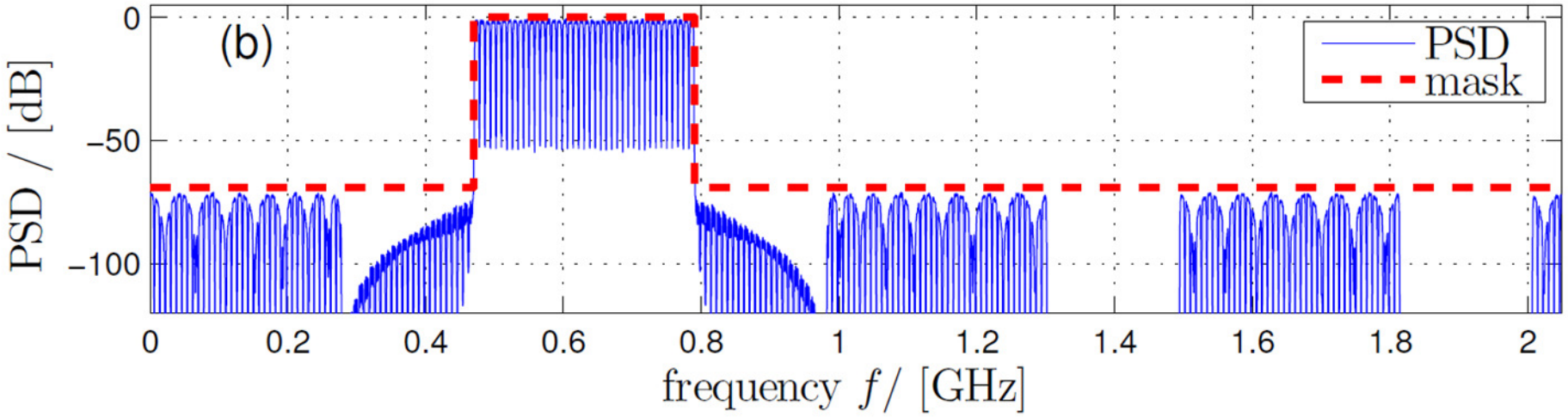


Floating Point Simulation

- **MathWorks DSP System & Comms Toolbox**
- Design 470-740 MHz TVWS Filter Bank

- Modulation of 320MHz baseband of 40 channels to centre frequency at 630MHz, with f_s = 2.048 GHz



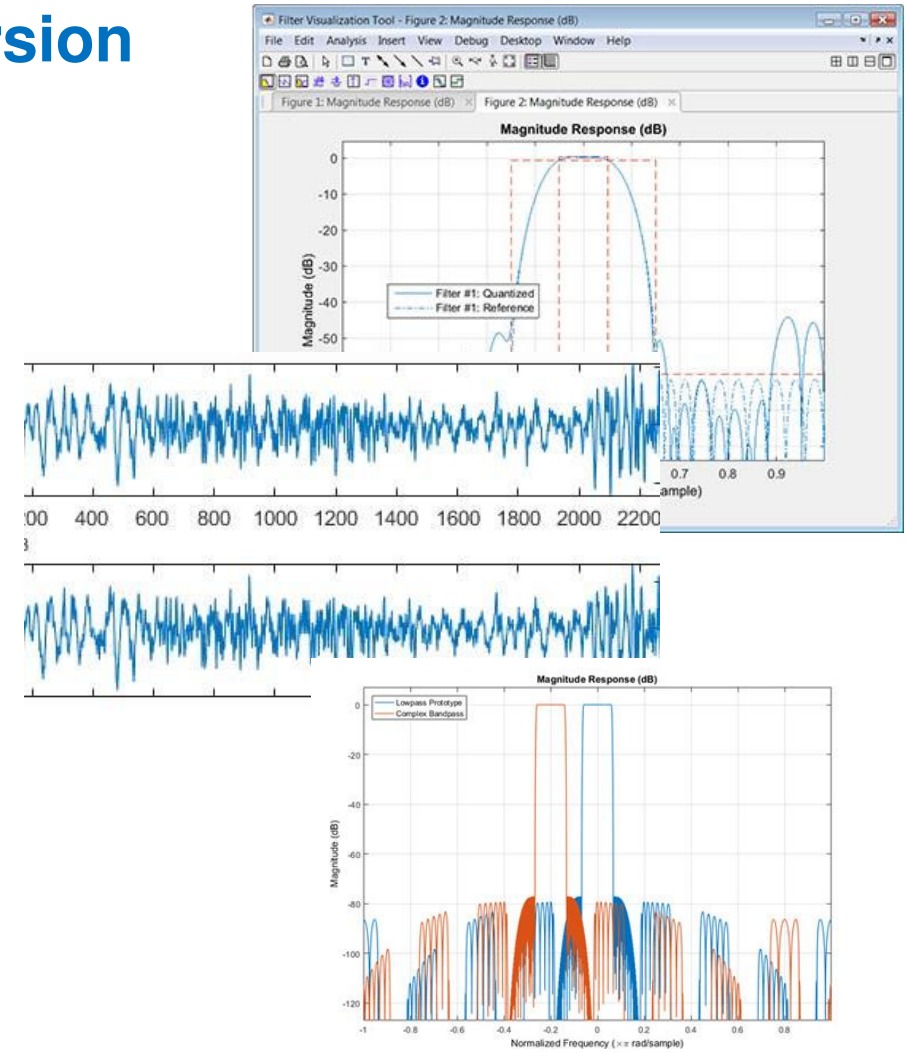


Fixed Point Optimisation

- **MathWorks Fixed Point Designer**
- Implement TVWS Filter Bank in Fixed Point

Floating to Fixed Point Conversion

- Fixed-point data type specification for:
  - MATLAB
  - Simulink
- Bit-true accelerated simulation
- Recommendations for word length and scaling
- Floating to fixed-point results comparison



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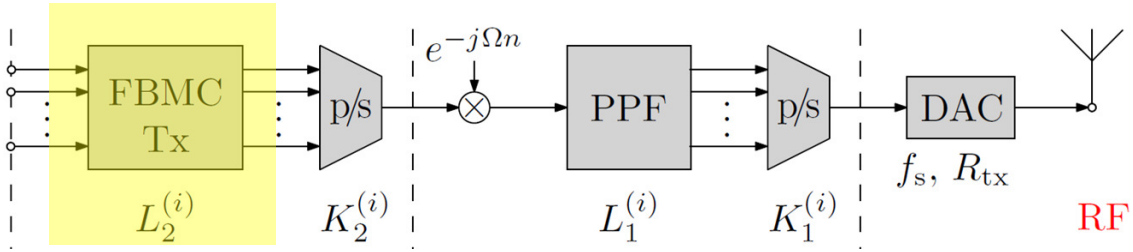

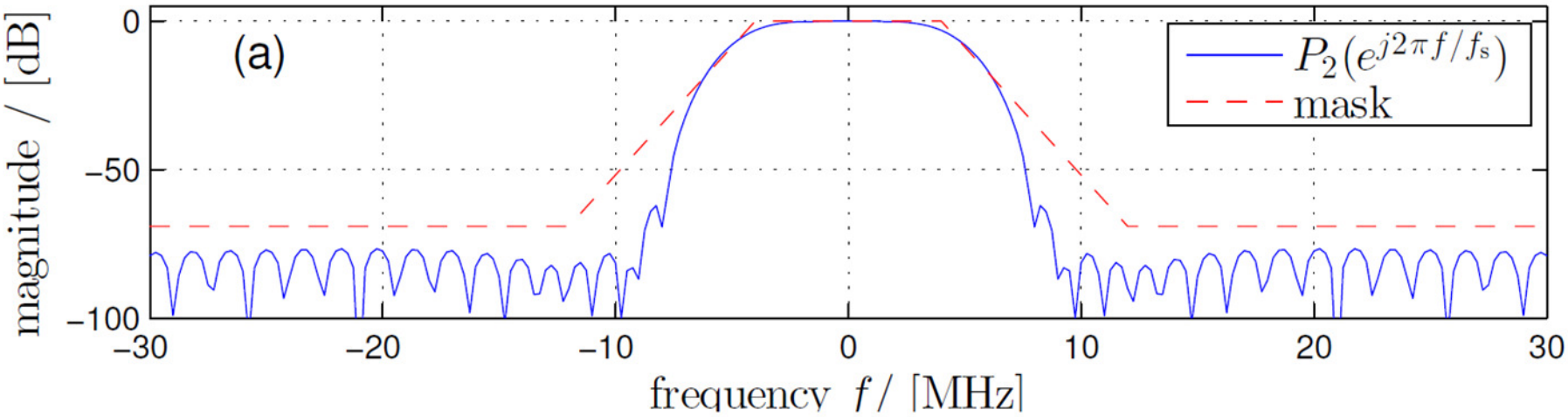

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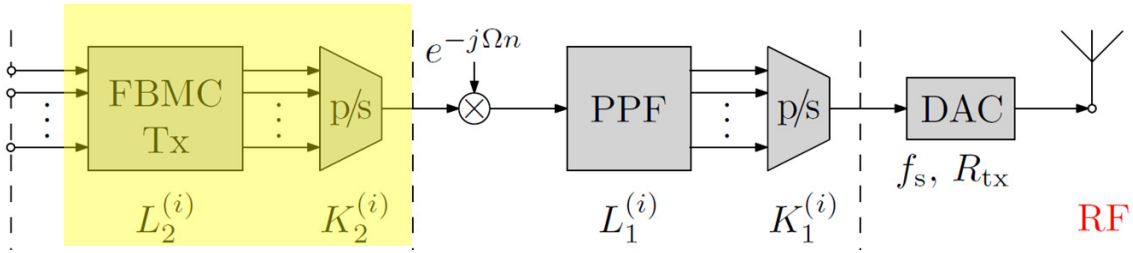

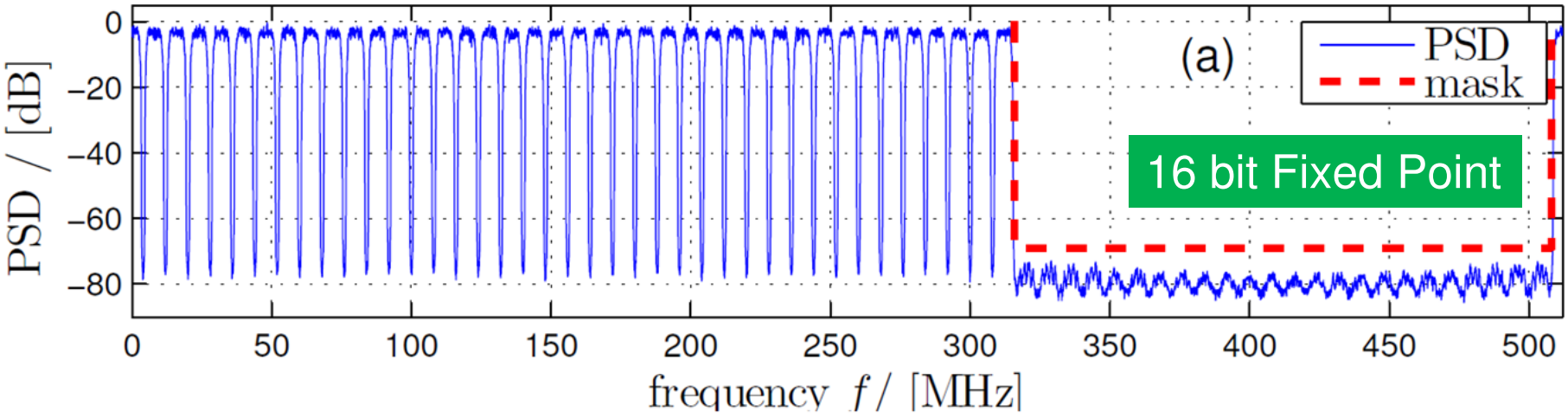

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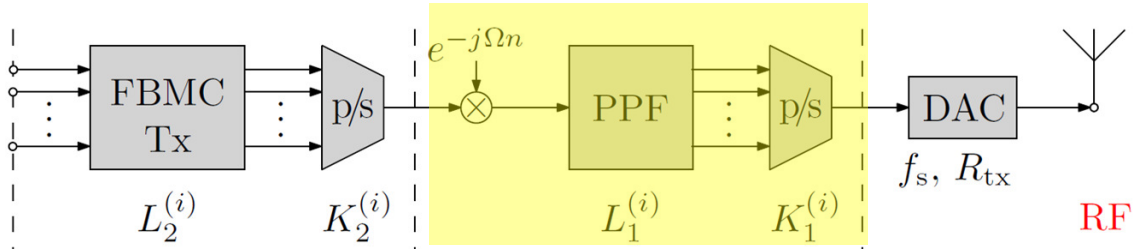
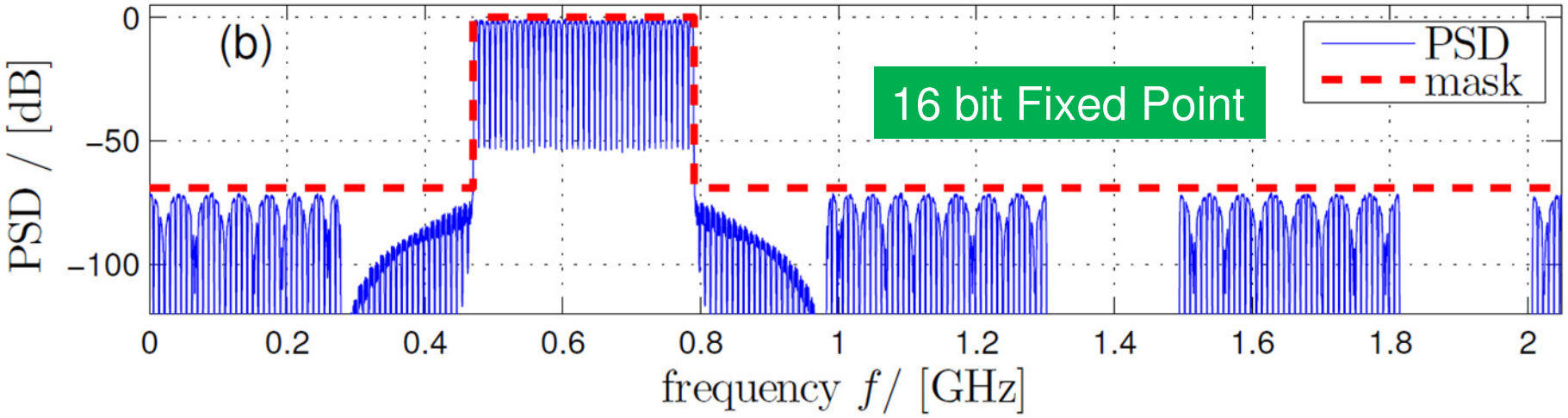
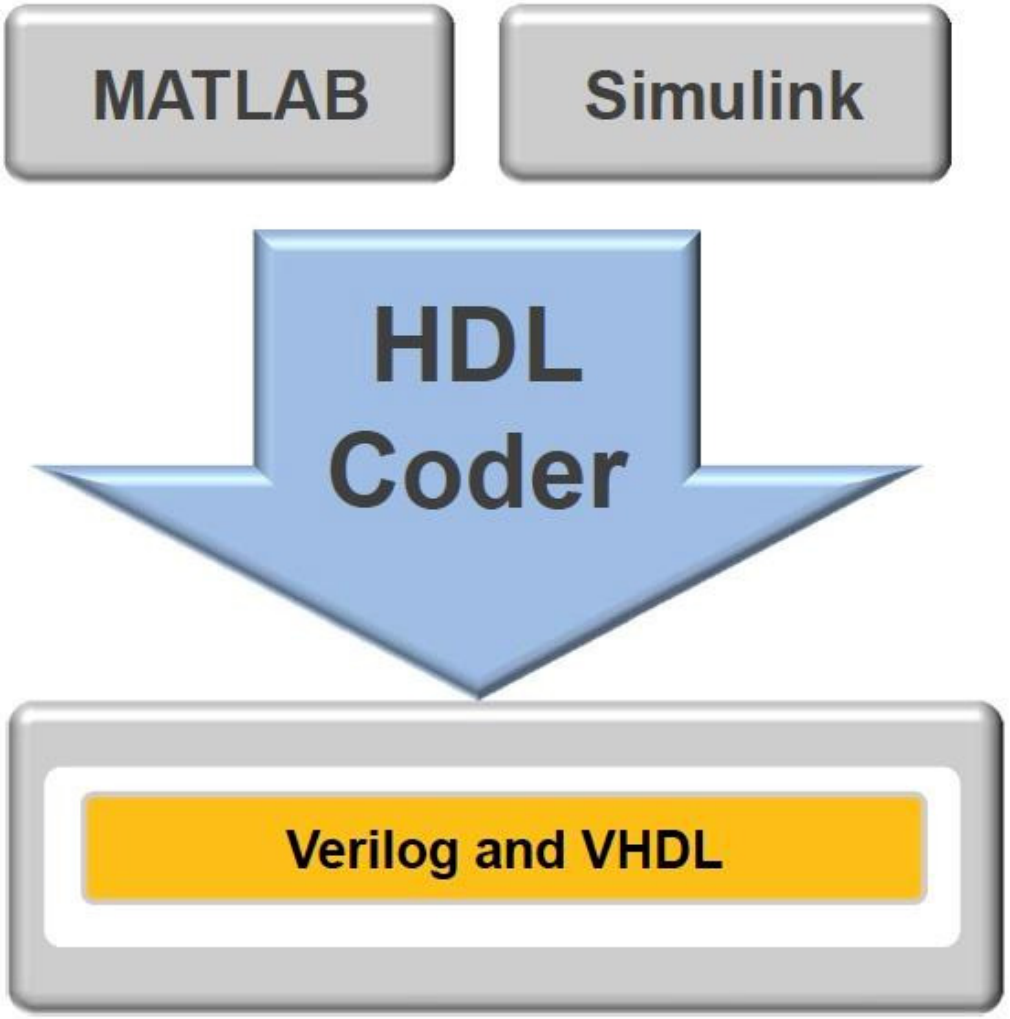




VHDL Implementation

- **MathWorks HDL Coder**
- Design verified HDL code for TVWS Filter Bank



VHDL Implementation

- **MathWorks HDL Coder**
- Design verified HDL code for TVWS Filter Bank

HDL Coder *generates portable, synthesizable VHDL and Verilog code from MATLAB functions, Simulink models*.

- The generated HDL code can be used for **FPGA programming** or ASIC prototyping and design.
- Provides a **workflow advisor** for working with Xilinx and Altera software tools and design flows.
- Controls architecture and implementation and highlight **critical timing paths** limiting clocking frequencies.
- Generate **hardware resource utilization** estimates for designs to target FPGA hardware.
- Provides **traceability** between Simulink model and the generated Verilog and VHDL code.

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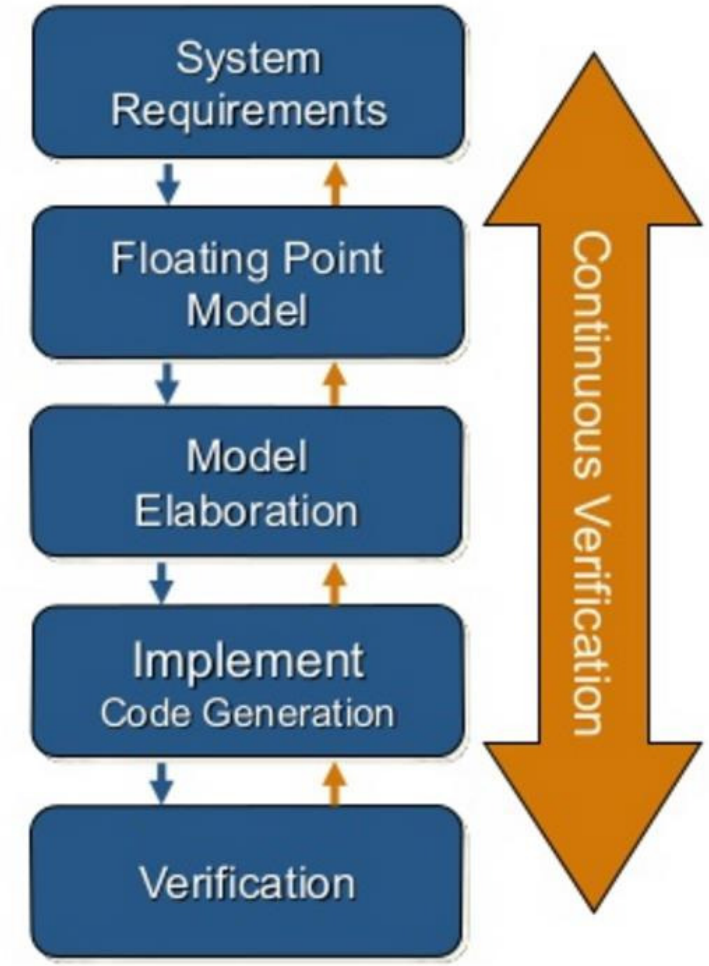

VHDL Implementation

- **MathWorks HDL Coder**
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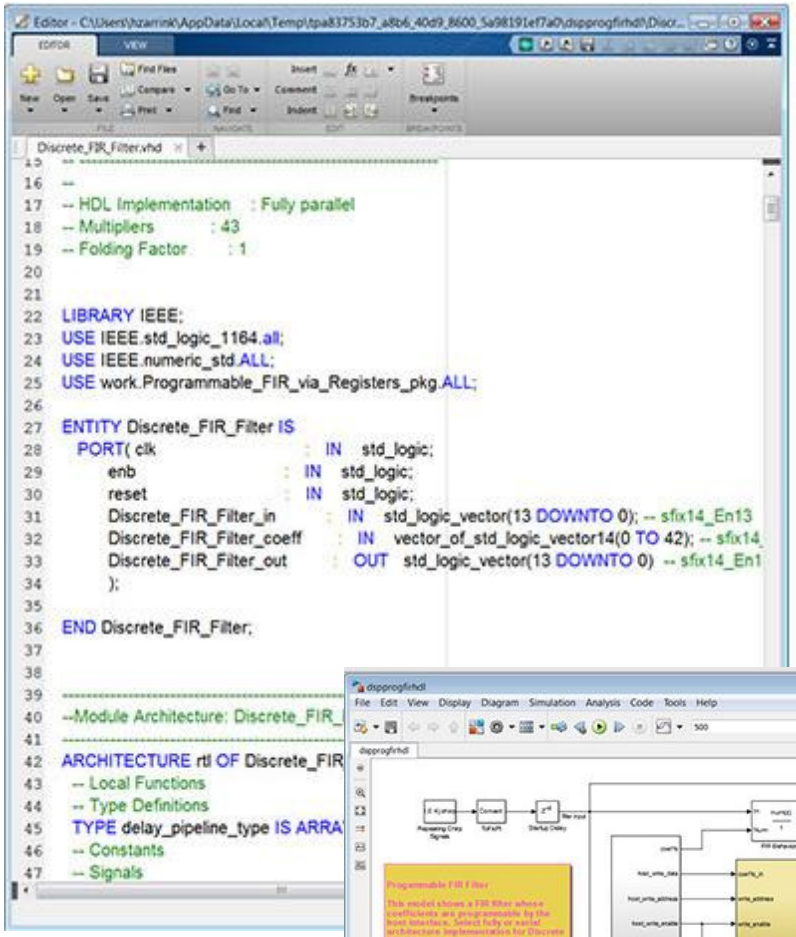
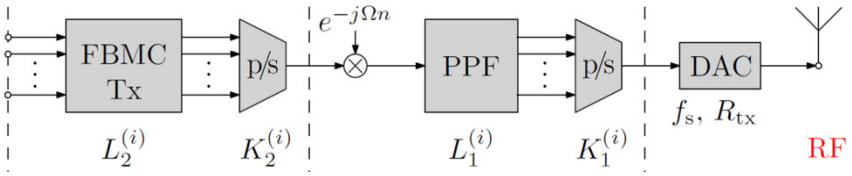
- Generation of VHDL for filter bank design and modulator design.
- VHDL verification and design of fixed point bit true Simulink model.
- FBMC, PPF and modulator





VHDL Implementation

- **MathWorks HDL Coder**
- Design verified HDL code for TVWS Filter Bank

- From fixed point design, we can use the HDL Coder workflow to verify design and review implementation achievable on FPGA devices.
- **Transmit** and **Receiver** Costs integrated on one table from Xilinx VIVADO tools.
- Design is *viable* and implementable on FPGA target

VIRTEX7-XC7VX550T FPGA DEVICE.

logic utilisation	number used	available	percentage used
LUTs	83566	346400	24%
FFs	63108	692800	9%
slices	26297	86600	30%
DSP48E1 units	1748	2880	60%

LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

LTE Systems Toolbox

- Simulates the physical layer of LTE and LTE-Advanced wireless communications systems.
- Standard-compliant functions and apps for the design, simulation, and verification of LTE and LTE-Advanced.
- Accelerates LTE algorithm and physical layer (PHY) development, supporting golden reference verification.
- Conformance testing, and also enabling test waveform generation, suitable for our TVWS links.
- Can configure, simulate, measure, and analyze end-to-end communications links.

LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

LTE Systems Toolbox

- Physical Signals
- Physical Channels
- Transport Channels

Coding/decoding

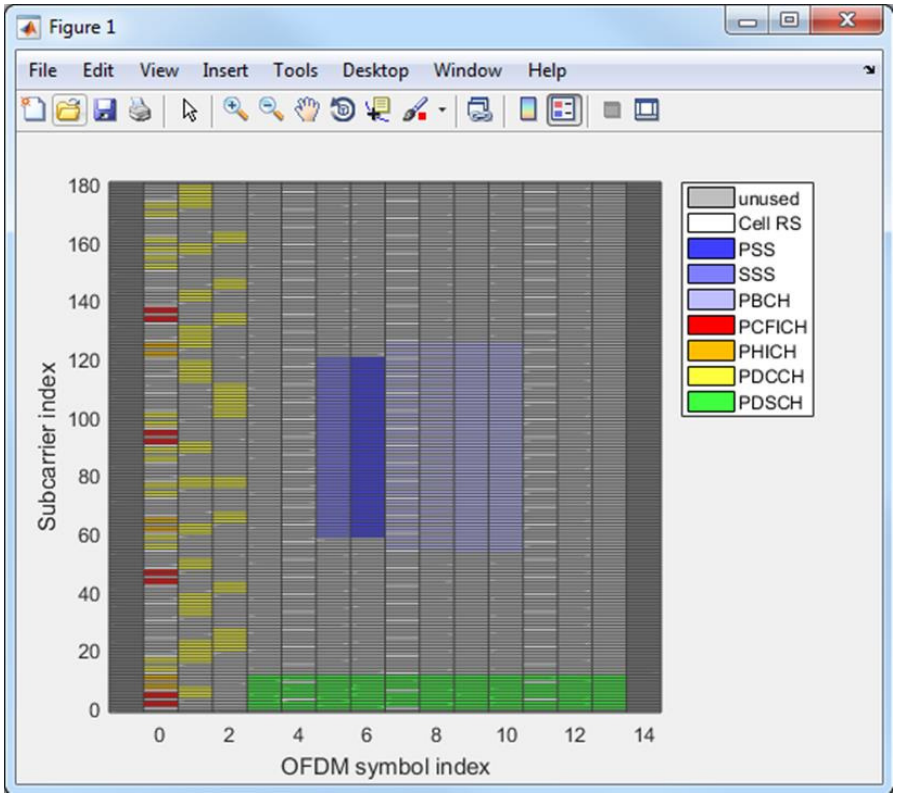
- Control Information
- OFDM/SC-FDMA; Modulation/Demodulation
- Reception and recovery:
  - Synchronisation
  - Channel Estimation
  - Equalisation
  - Cell search procedure
- Channel Models
- Functions for Test and Measurement

LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

LTE Systems Toolbox

- Standard-compliant **physical layer** models in MATLAB: Releases 8, 9, 10, 11 and 12
- Scope:
  - FDD / TDD
  - Uplink / Downlink
  - Transmitter / Receiver
  - Conformance tests
  - link level simulation
- More than 200 functions for physical layer modelling



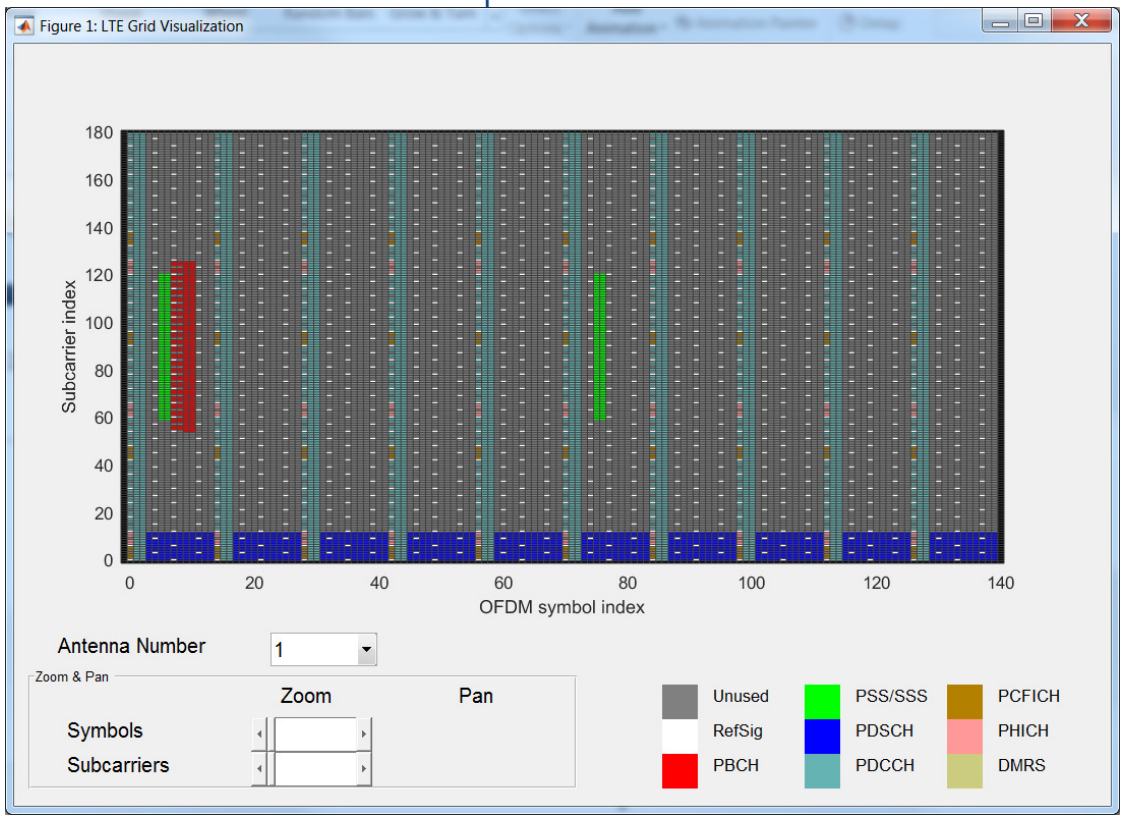
LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

Easy LTE Signal Generation from MATLAB code lines:

Command Window

```
>> enb = lteRMCDL('R.0');
>> [wave,grid]=lteRMCDLTool(enb,[1 0 0]);
>>
```



LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

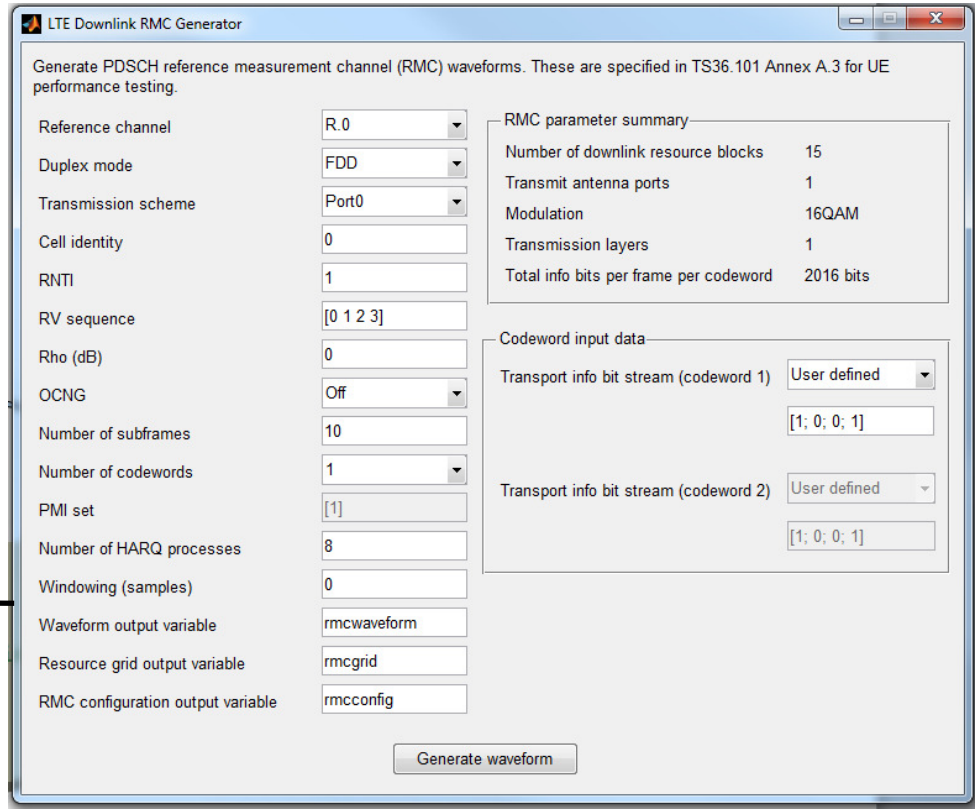
LTE Systems Toolbox has high level signal generators.

```
% Establish the number of component carriers.
numCC = length(NDLRB);

% Create transmission for each component carrier
enb = cell(1,numCC);
for i = 1:numCC
    enb{i} = lteRMCDL('R.5');
    enb{i}.NDLRB = NDLRB(i);
```

MATLAB function

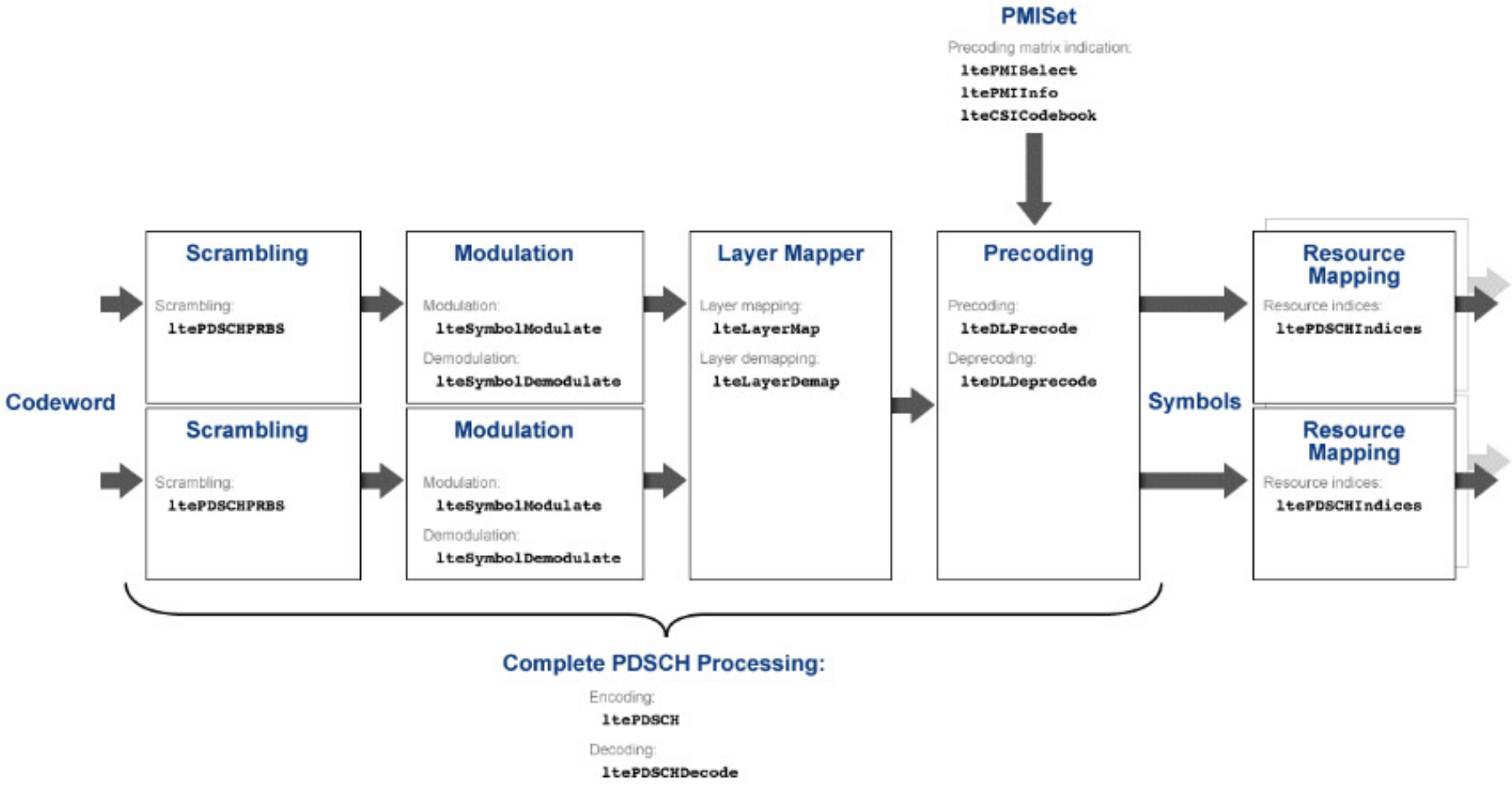
GUI Based



LTE Baseband

- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

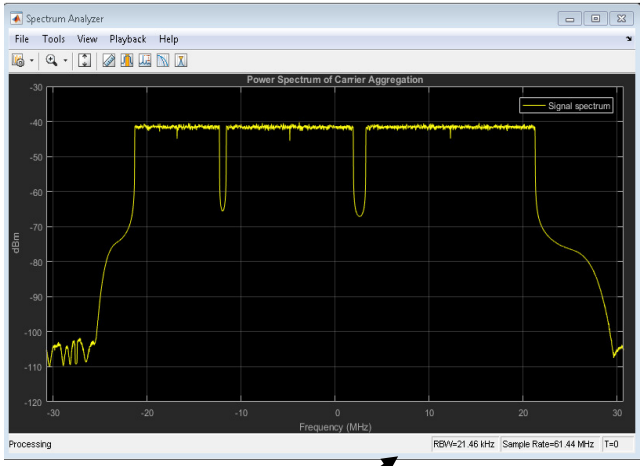
LTE Systems Toolbox gives granular design options

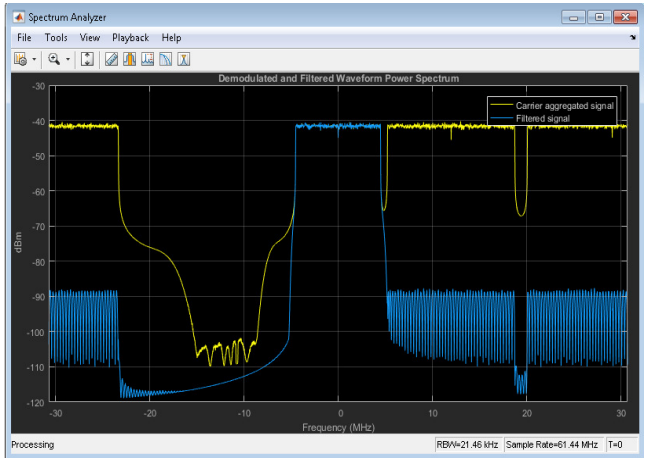


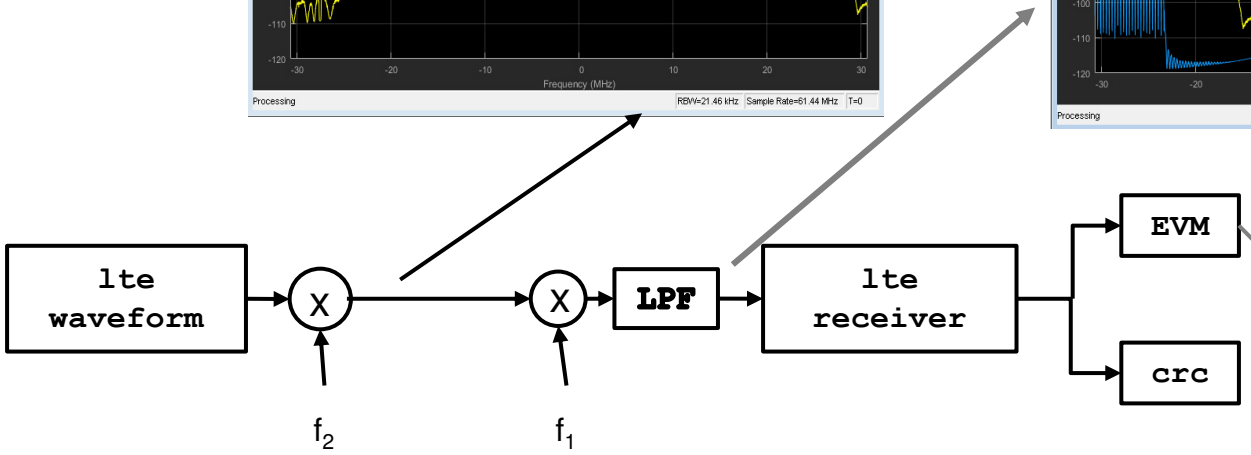
LTE Baseband

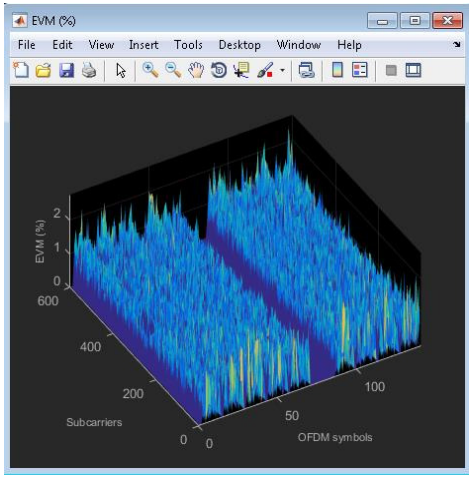
- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

LTE Systems Toolbox: Full transmit and receive chain.









LTE Baseband

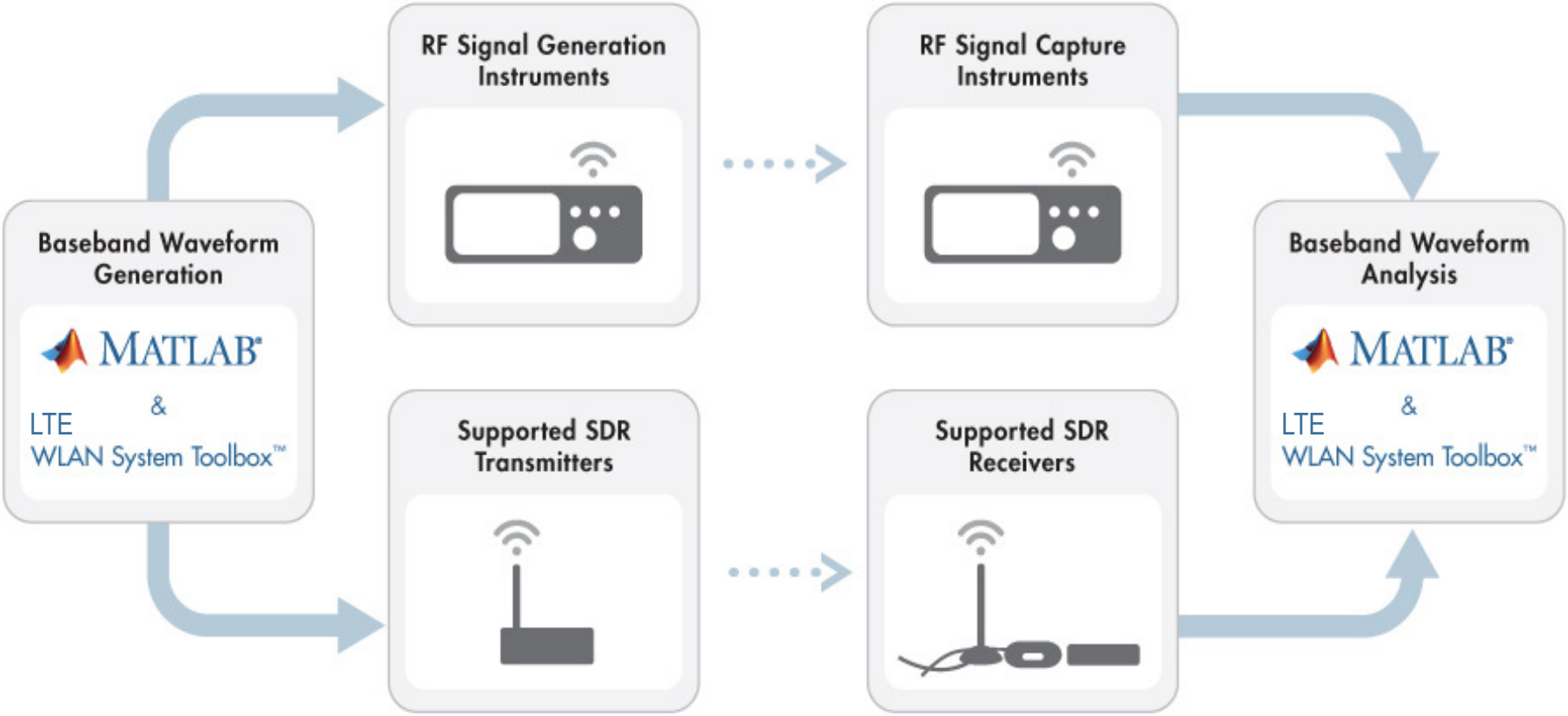
- **MathWorks LTE Systems Toolbox**
- Implement LTE Transmit and Receive

LTE System Toolbox: using TDD for TVWS:

- **Bandwidth:** 5 MHz
- **Modulation:**
  - BPSK / QPSK / 16QAM / 64QAM
  - BPSK : Control
- **64QAM:** data channel
- **Duplex method:** TDD / FDD

FPGA SDR Implementation

- **MathWorks Zynq SDR Support Package**
- Implement Tx and Rx TVWS Filter banks



FPGA SDR Implementation

- **MathWorks Zynq SDR Support Package**
- Implement Tx and Rx TVWS Filter banks

Hardware

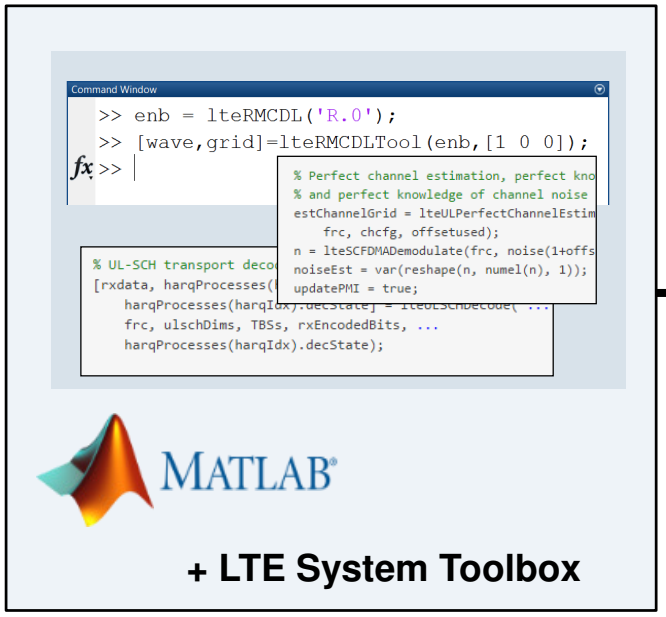
- ***Xilinx Zynq ZC706 Development Board***
  - Featuring Zynq-7045 AP SoC,
    900 DSP48E1 slices; 350K Logic Cells
  - 2 FMC Expansion Slots

- ***ADI FMCCOMMS3 FMC Card***
  - AD9361 Agile RF Transceiver
    2 x 2 transceiver with integrated
    12-bit DACs and ADCs
    Band: 70MHz to 6.0GHz
    Channel Bandwidth: < 200kHz to 56MHz
- ***RF amplifier stage / Yagi Antenna***

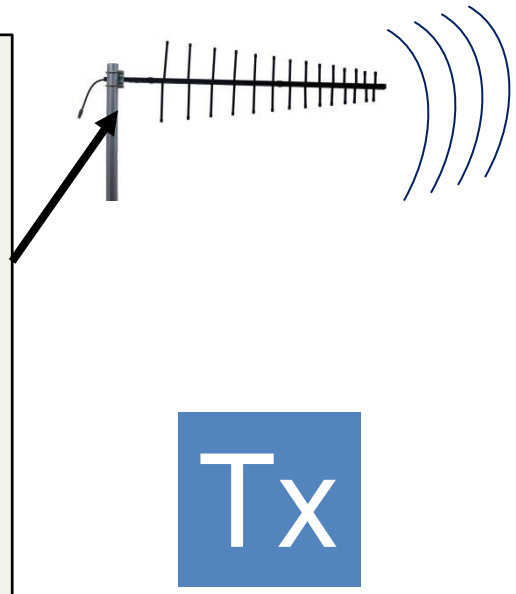
FPGA SDR Implementation

- **MathWorks Zynq SDR Support Package**
- Implement Tx and Rx TVWS Filter banks

LTE Baseband Signal Transmitter and Waveform Generation



RF Signal Capture + TVWS FBMC Transmitter

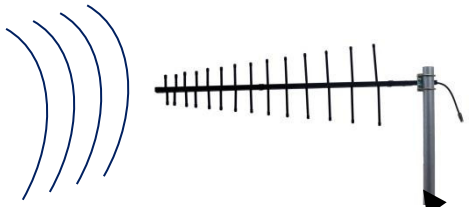


FPGA SDR Implementation

- **MathWorks Zynq SDR Support Package**
- Implement Tx and Rx TVWS Filter banks

RF Signal Capture
+ TVWS Receiver Bank

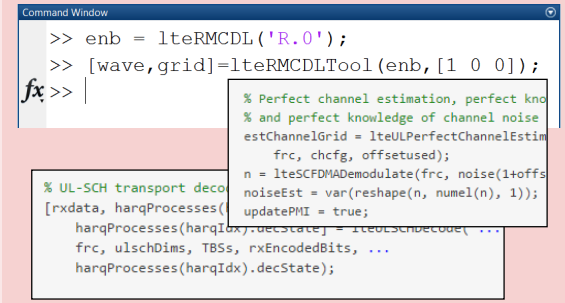
LTE Baseband Signal Receiver and Waveform Analysis



Rx

Zynq SDR Platform

+ HW Support package



MATLAB

+ LTE System Toolbox

Model Based Design of SDR for LTE in TVWS

Floating Point Simulation	• **MathWorks *DSP System* & *Comms* Toolbox** • Design 470-740 MHz TVWS Filter Bank
Fixed Point Optimisation	• **MathWorks *Fixed Point Designer*** • Implement TVWS Filter Bank in Fixed Point
VHDL Implementation	• **MathWorks *HDL Coder*** • Design verified HDL code for TVWS Filter Bank
LTE Baseband	• **MathWorks *LTE Systems Toolbox*** • Implement LTE Transmit and Receive
FPGA SDR Implementation	• **MathWorks *Zynq SDR Support Package*** • Implement Tx and Rx TVWS Filter banks

Conclusions

- Model Based Design of ***LTE-SDR-TVWS-FPGA*** protoype!
- Floating Point DSP Filter Bank and modulator design
- Fixed point optimisation of DSP system
- HDL implementation of DSP system
- LTE Systems toolbox signal generator (Tx) & receiver (Rx)
- Implementation of LTE Tx and Rx on host
- Implement HDL of DSP System using Zynq SDR support
- Test over the TVWS air!

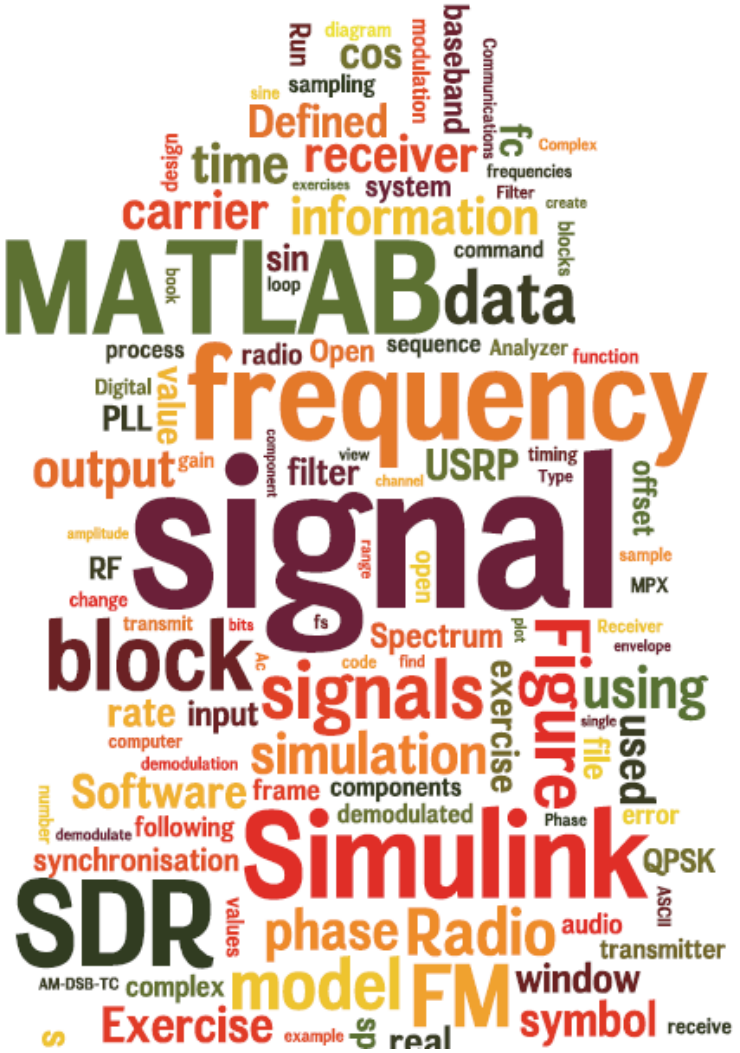
Acknowledgements

- Iain Chalmers, Sarunas Kalade, David Crawford, David Northcote, Dani Anderson, Stephan Weiss

  at University of Strathclyde

- Daniel Garcia-Alis, Neil MacEwen, Ken Karnoksky

  at MathWorks



Additional Reserve Slides

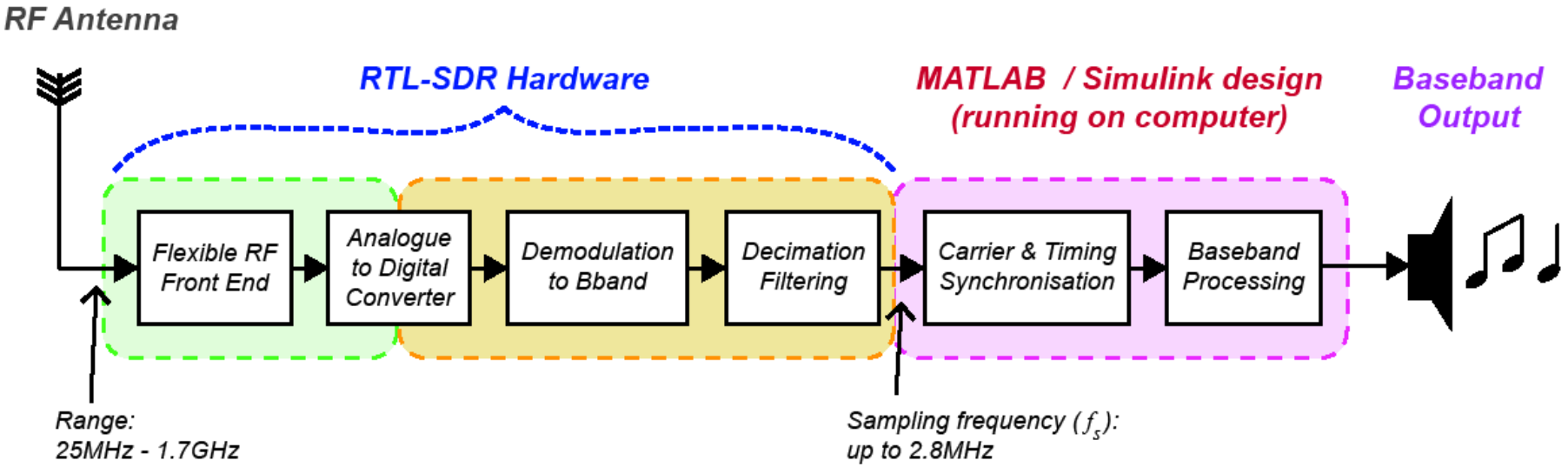
670 Page Textbook

+ more than 100 MATLAB & Simulink examples…

Download e-book and examples from:

www.desktopSDR.com

RTL-SDR *DSP enabled Radio*

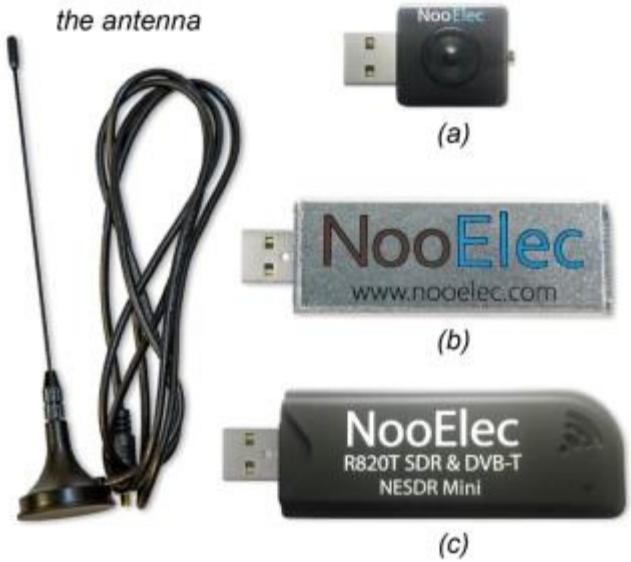


Hardware Setup for Real World SDR

- Windows, Linux or Mac Computer
- An RTL-SDR + Antenna

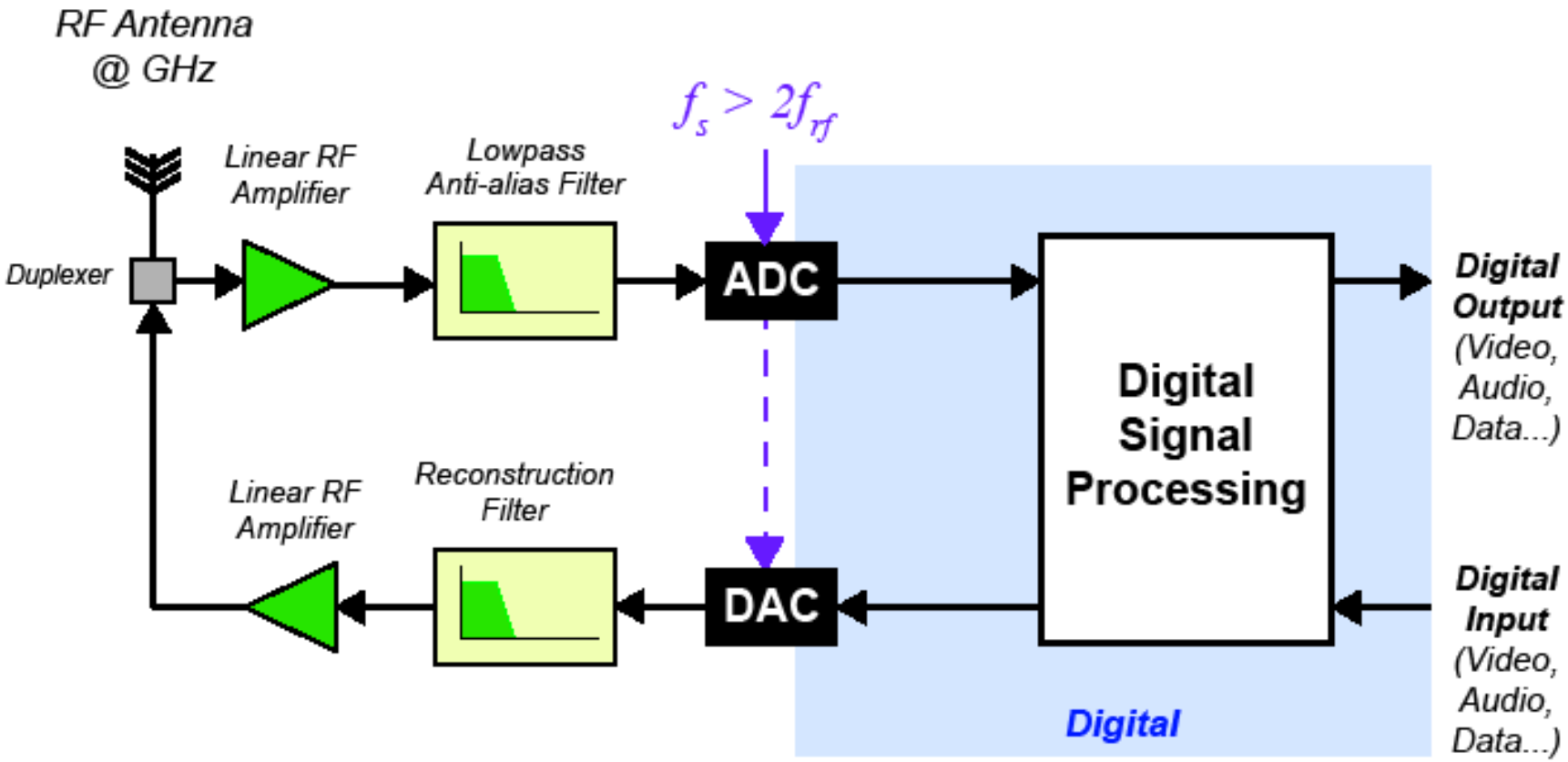
- A few RTL-SDR devices available…

(same hardware different packaging and component tolerances.)



The Ultimate (DSP enabled) Software Defined Radio

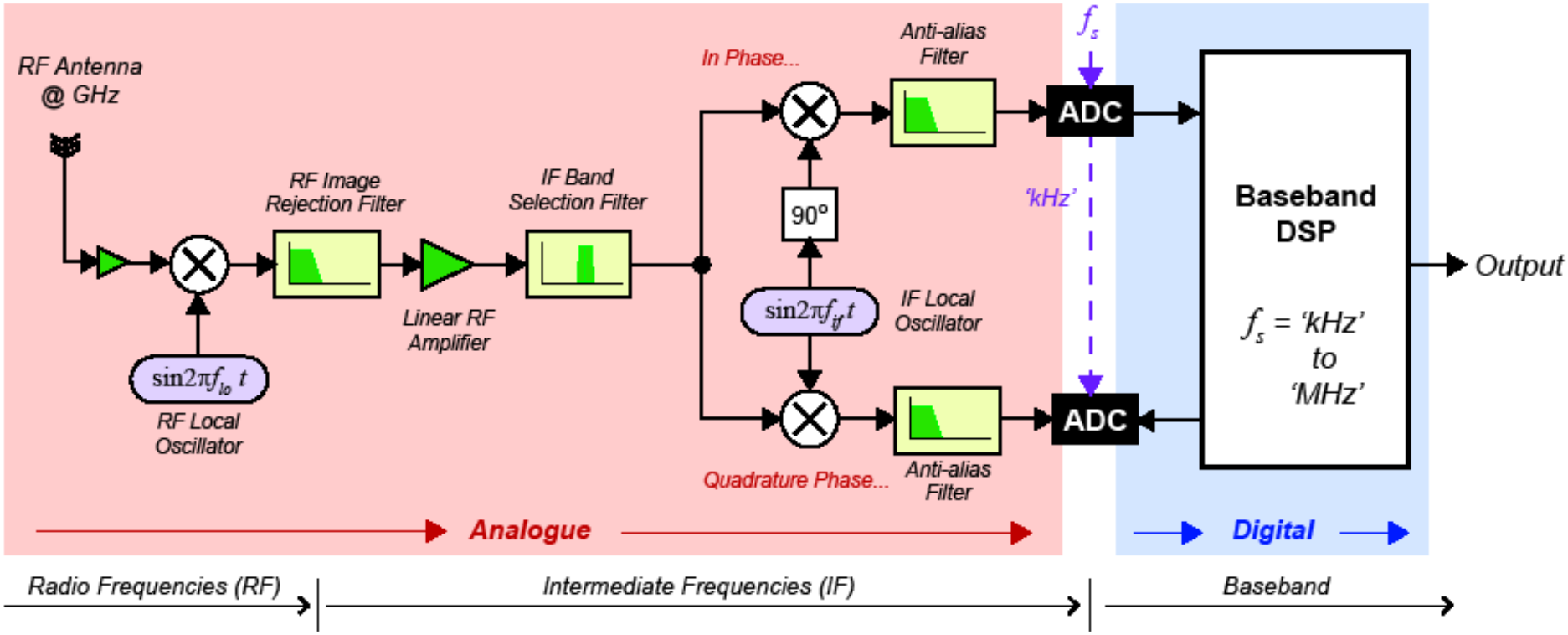
20MHz to 6GHz range



ASICs, FPGAs, DSP Cores

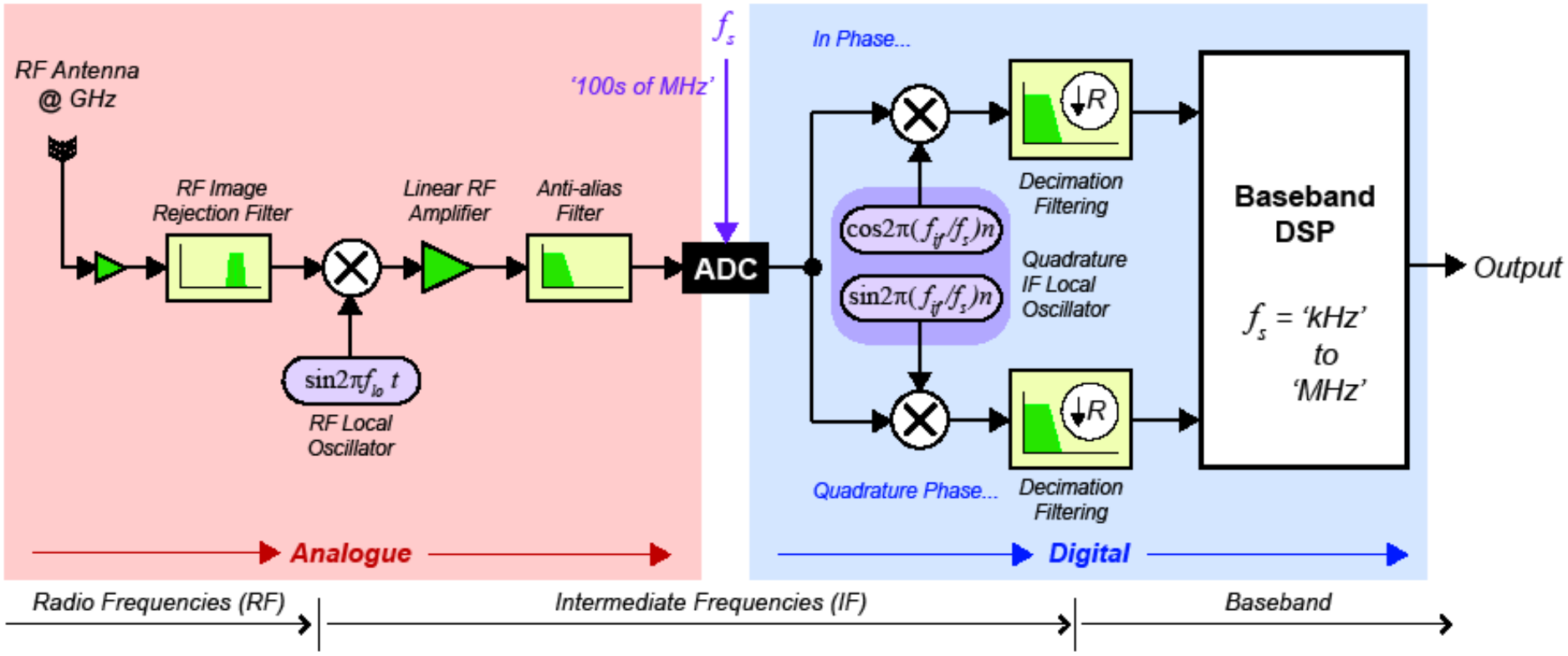
First Generation Digital Radio (around 1995):

- ADC Sampling Rates at baseband up to 100's kHz



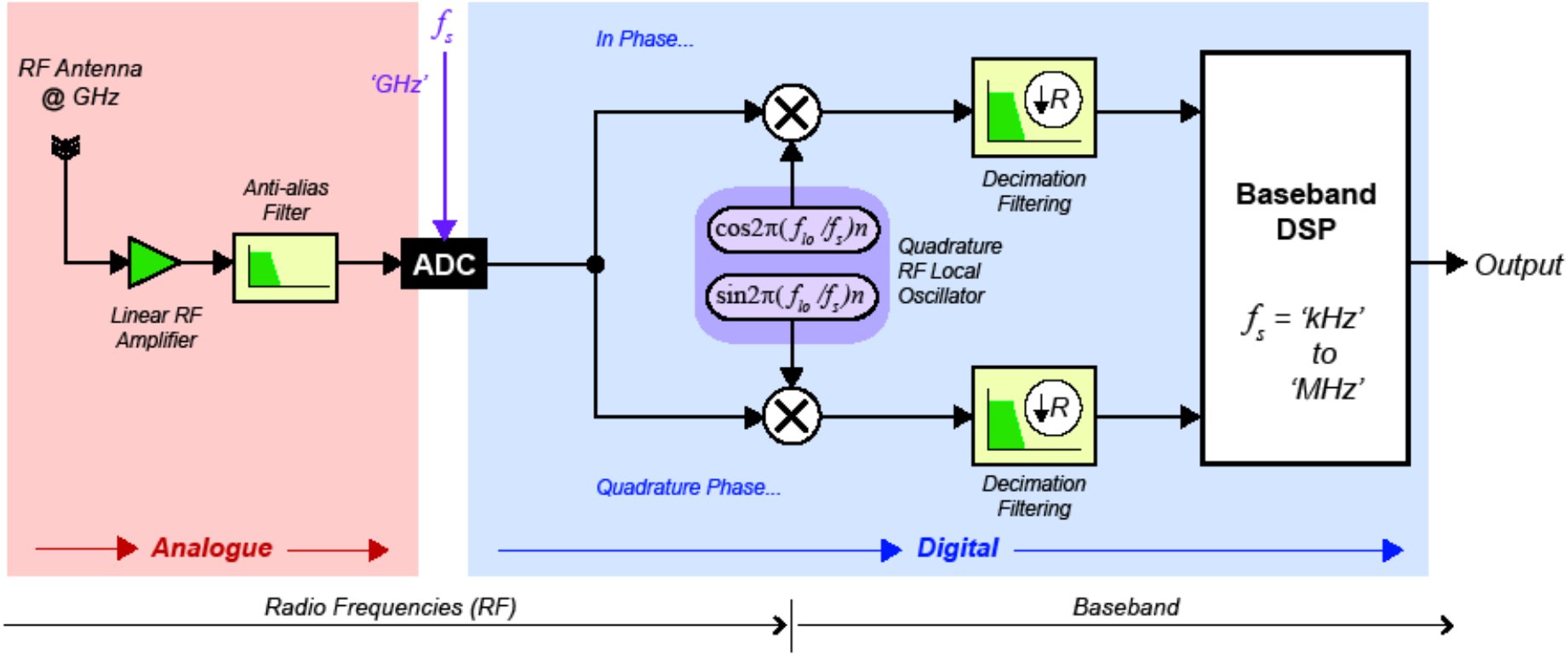
Intermediate Frequency (IF) Digital Radio (2000s)

- ADC Sampling Rates up to a few 100MHz



The RF Sampled (zero-IF) Digital Radio (2012…)

- ADC Sampling Rates of a GHz and (getting) higher.



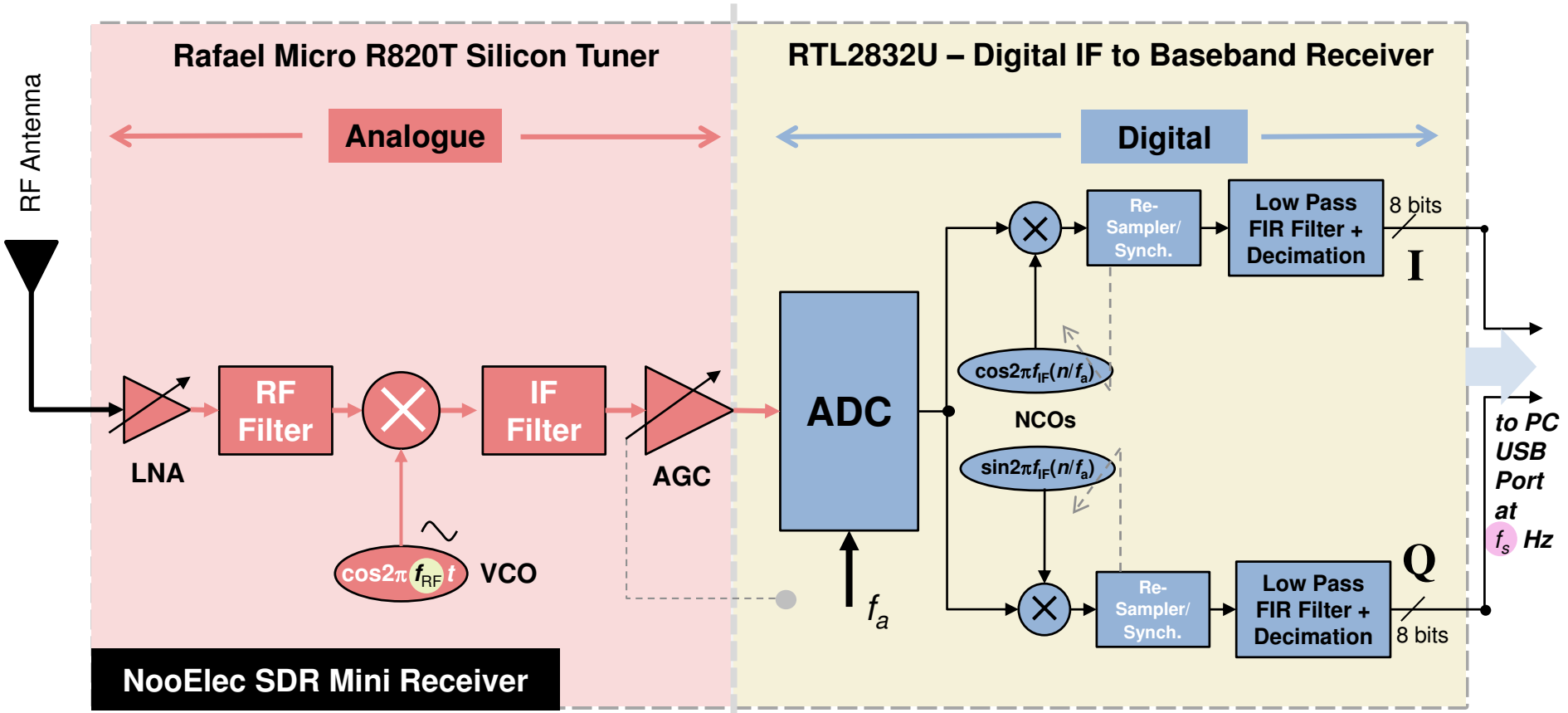
The RTL-SDR USB RF Receiver

Configuring SDR parameters (*via USB port*)

- f_{RF} - RF Center frequency
- f_s – I/Q Data Sampling Frequency
- Gain Control Parameters
- Frequency Correction

An *IF* Software Defined Radio

(IF – Intermediate Frequency)



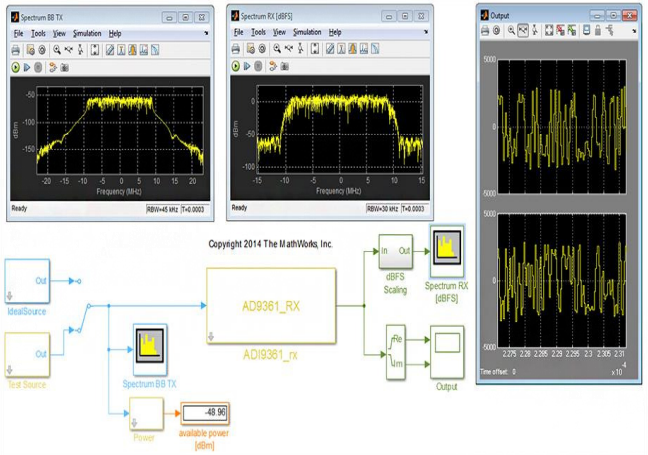
f_{RF} RF VCO Frequency (50MHz to 1.4 GHz)

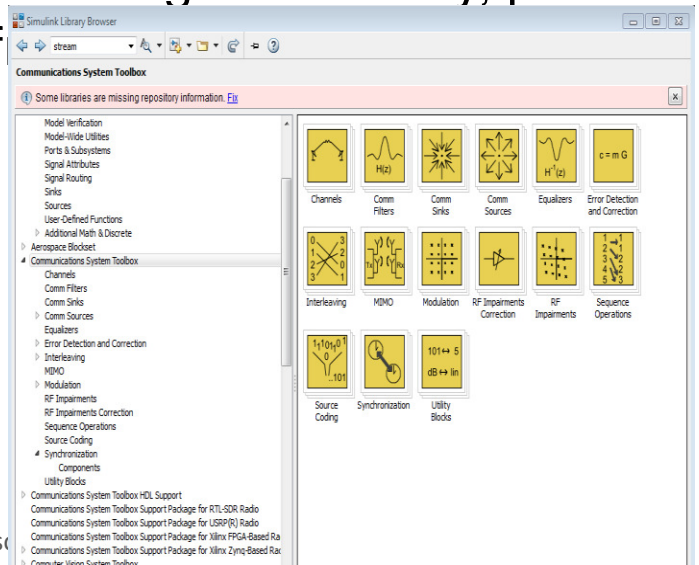
LNA/AGC Tuner Gain Control
VCO Voltage Controlled Oscillator

f_s I/Q Data sampling frequency (up to 2.8MHz)
f_a Sampling rate of ADC (28.8MHz)
ADC Analogue to Digital Converter
I / *Q* In-phase & Quadrature-phase Channel
FIR Finite Impulse Response
NCO Numerically Controlled Oscillator

Integration with MathWorks toolboxes

- Back up your modelling with the full strength of MW tools.
  - Communications, Phased Array, LTE, WLAN, SimRF
  - Analysis tools and measurement scopes, including a bit-error-rate app, constellation diagrams, and eye diagrams
  - Channel models, including AWGN, multipath Rayleigh fading, Rician fading, MIMO multipath fading, and LTE MIMO multipath fading
  - Basic RF impairment models, including nonlinearity, phase noise, thermal noise, and phase and f





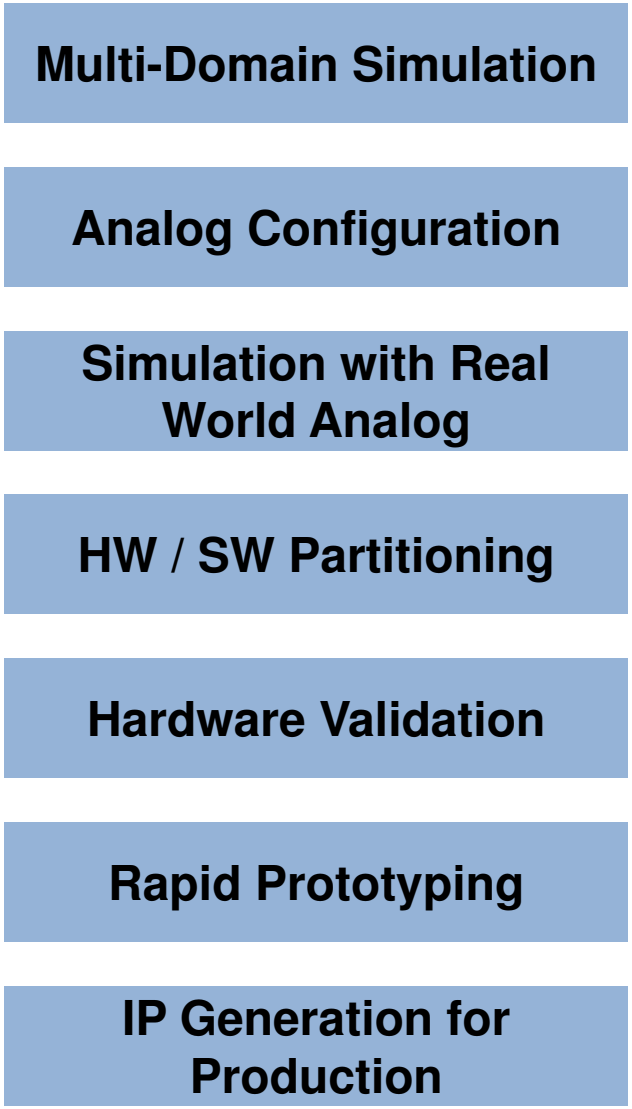
SDR Examples

- Full prototyping flow
  - Repeating transmitter mode
  - QPSK Tx/Rx + FPGA targeting + HW/SW co-desig

- Advanced communications standards
  - LTE using LTE System Toolbox
  - 802.11 using WLAN System Toolbox

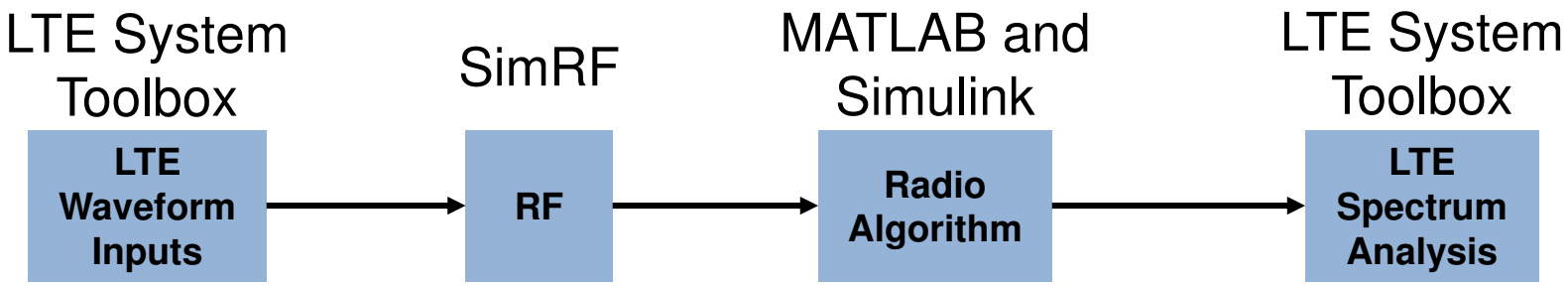
Radio Design Framework

- Quickly develop radio algorithms from customer requirements in MATLAB® and Simulink®
- Common environment used by design teams for system modeling through to production
- Accelerate development with code generation and continuous verification
- Validate, prototype and deploy in hardware



Radio Design Framework

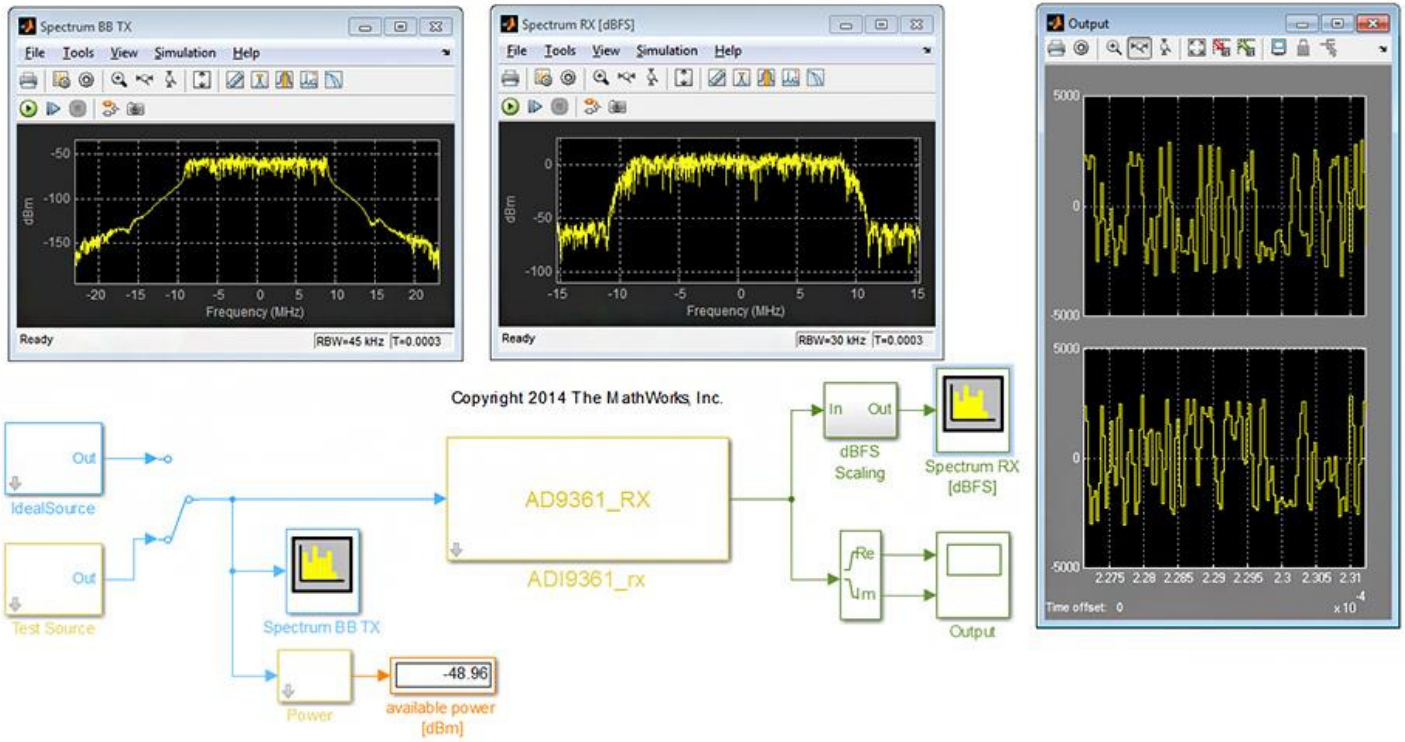
Multi-Domain Simulation



- LTE System Toolbox™ provides advanced waveform generation and spectrum analysis
- Model both the RF and DSP
  - AD9361 simulation model available from MathWorks
- Rapidly explore radio algorithms to meet customer requirements in simulation

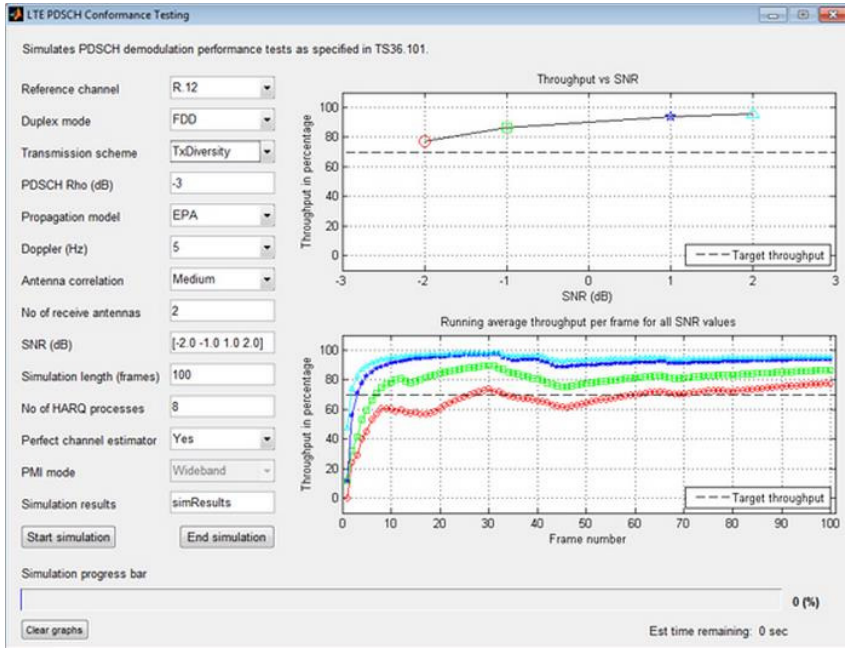
Multi-Domain Simulation Example

- Model RF transceivers using MATLAB and Simulink
  - Built from device functional specification
  - Tested with LTE-compliant waveforms
  - Verified by vendor to match silicon behavior



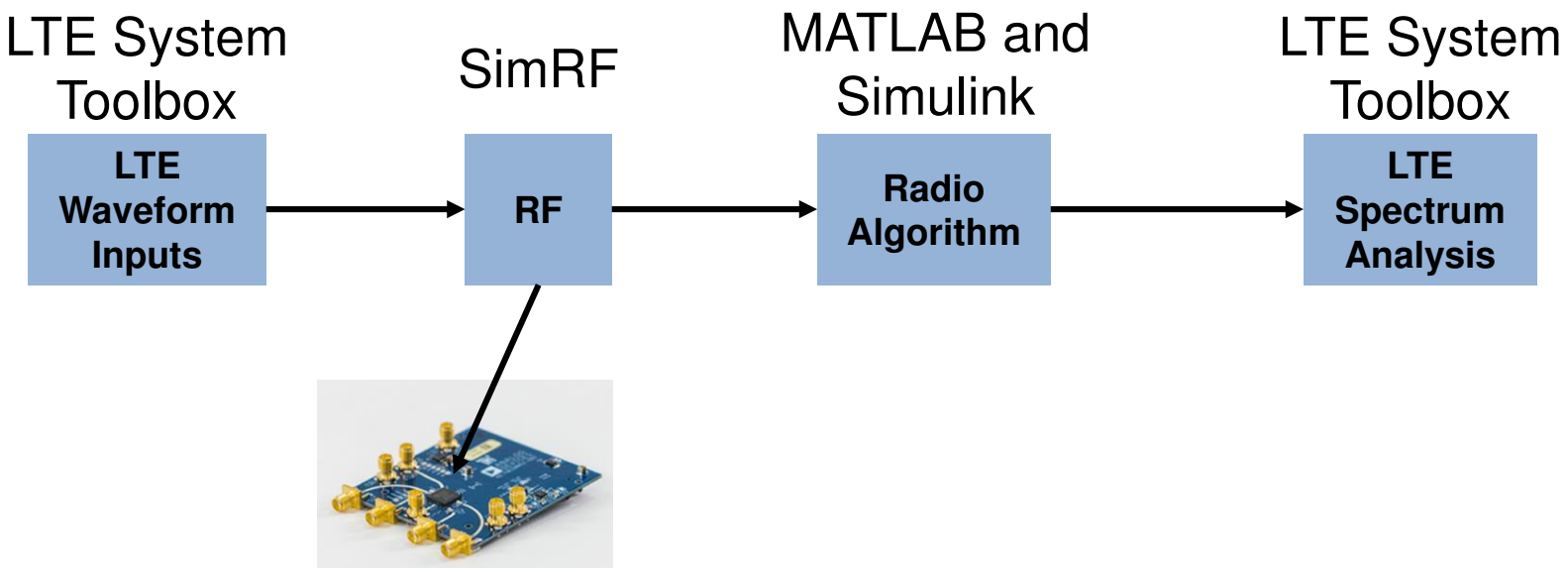
LTE System Toolbox

- Standard-compliant models for LTE and LTE-Advanced
- End-to-end physical layer transmit and receive processing functions
- Test models and reference measurement channel waveform generators



Radio Design Framework

Analog Configuration

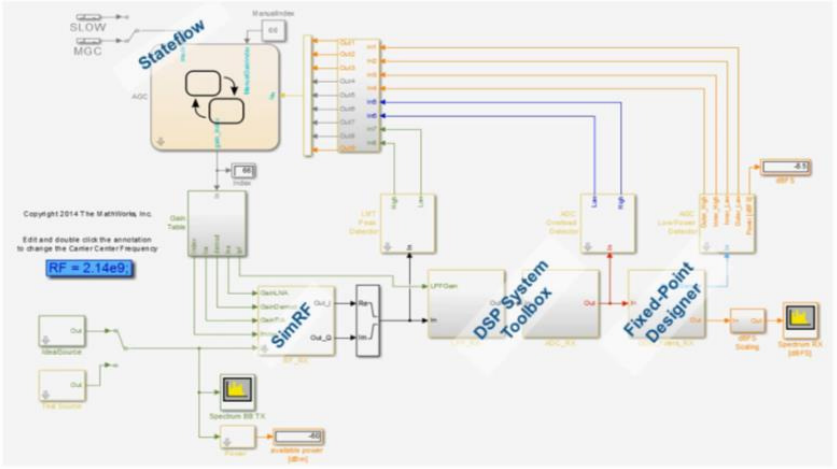


- Tune and Configure Analog Front End in Simulink
  - Simulation model for AD9361 built using Simulink and SimRF™
  - Supports device configuration

AD9361 Simulation Model

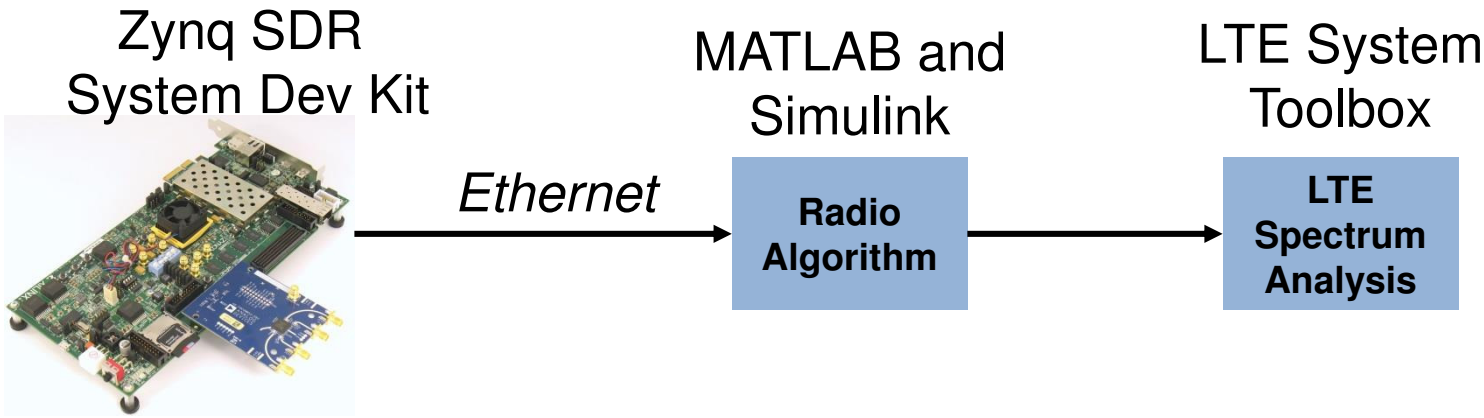
- Predict the impact of RF Imperfections in test signals
- Use reference tones and LTE Signals
- Evaluate the effects of nonlinearity, noise, gain and phase imbalance
- Generate AD9361 configuration file

AD9361 Agile RF Transceiver



Radio Design Framework

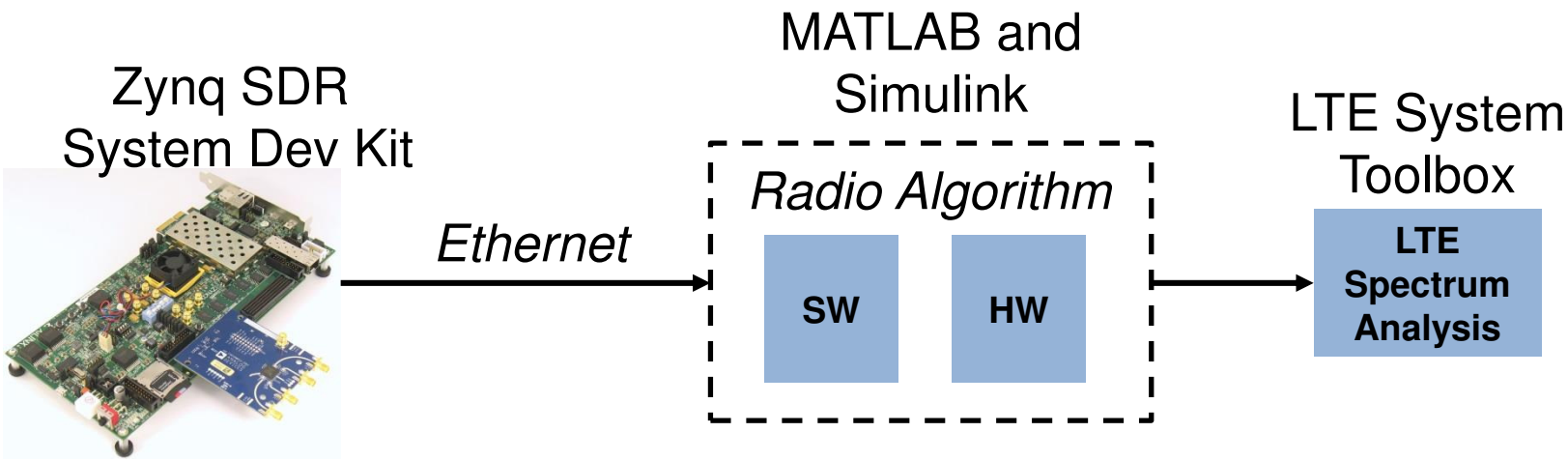
Simulation with Real World Analog



- Validate and tune algorithms with real world analog data through analog interface
  - Zynq SDR System Development Kit supports analog capture and export to Simulink

Radio Design Framework

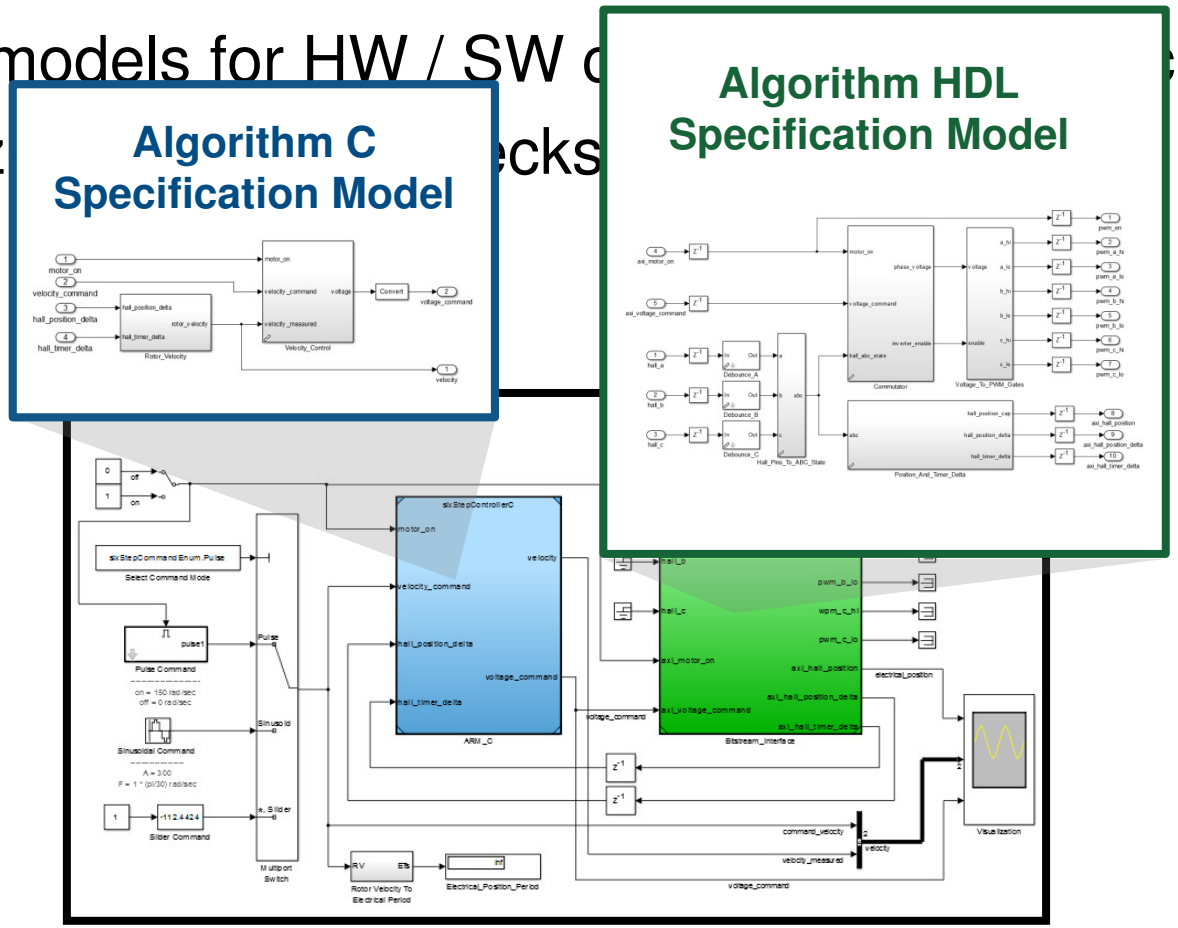
HW / SW Partitioning



- Use Simulink to partition algorithm into HW and SW
  - Cycle Accurate System Simulation
  - Validate system performance
  - Specify system concurrency

System Partitioning

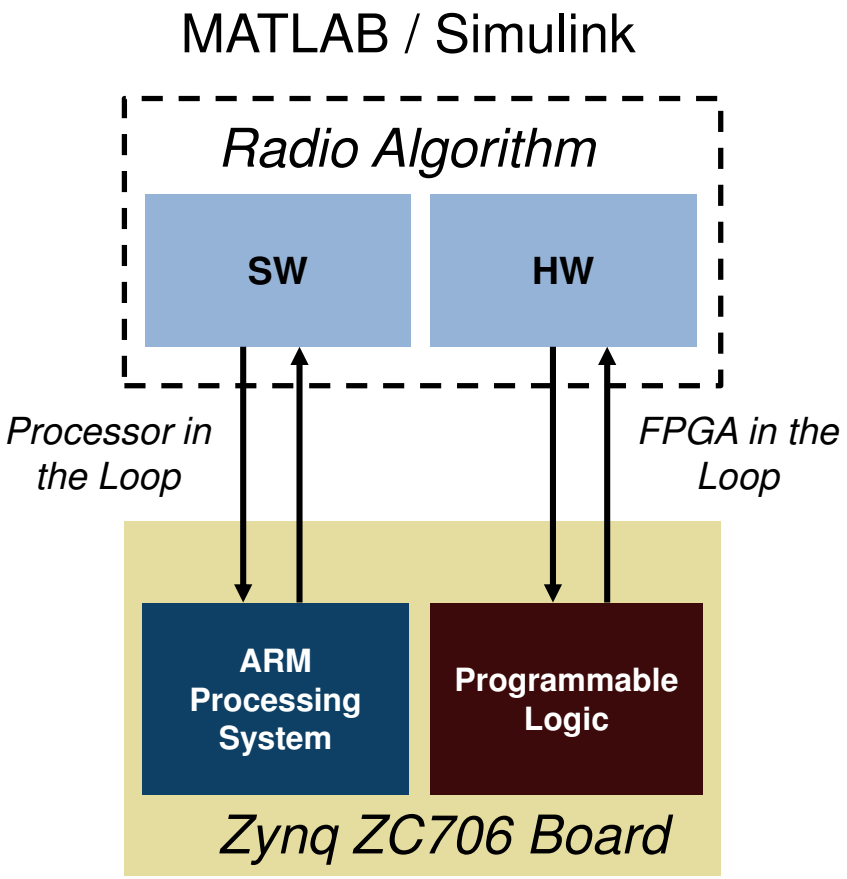
- Hardware / Software system partitioning using Simulink
  - User-defined system partitioning
- Tailor models for HW / SW c iency
- Analyz cks



Radio Design Framework

Hardware and Software Hardware Validation on Zynq

- Processor in the Loop
  - Monitor data and tune parameters on hardware in real time from Simulink
  - External Mode enables Simulink control of software execution
- FPGA in the Loop
  - Generate and download bitstream to Zynq programmable logic
  - Validate design in hardware from Simulink



Radio Design Framework

Rapid Prototyping

- Simulink Zynq Workflow for Rapid Prototyping
  - Automatic code generation
  - Embedded Coder generates NEON optimized code for Zynq ARM
  - HDL Coder Generates AXI IP Core for Zynq Programmable Logic
- Visualize results using LTE Spectrum Analysis