Modular input-parallel output-series DC/DC converter control with fault detection and redundancy

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Abstract: Large offshore wind farms require extensive sub-sea cables within the collection network. Present solutions are based around medium-voltage AC collection networks. Recent studies have highlighted the potential benefits of DC collection networks. However, achieving DC/DC conversion at the required voltage and power levels presents a significant challenge for wind-turbine power electronics. This paper proposes an alternative DC collection network based around a modular DC/DC converter with input-parallel output-series (IPOS) connection. This modular topology can overcome the limitations imposed by semiconductor voltage ratings and provides fault-tolerant operation. Small-signal analysis of the converter is presented to be used to facilitate controller design for the converter input and output stages. A new master-slave control scheme and distributed voltage sharing controllers are proposed that ensure power sharing under all operating conditions, including during failure of a master module. This control scheme achieves fault-tolerant operation by allowing the status of master module to be reallocated to any healthy module. The proposed control scheme is validated using simulation and experimentation, considering active power sharing between modules with parameter mismatch.

1 Introduction

Today, onshore wind energy is regarded as a viable technology to reduce climate-change effects and meet national renewable energy targets in Europe and around the world [1]. In recent years, there has been a movement to increase output from wind generation by exploiting the offshore wind energy resource. A typical offshore wind farm consists of two networks: a collection network within the wind farm and a transmission network to the onshore grid. In comparison to an AC collection network, a DC collection network offers a number of potential benefits. The use of DC can improve cable utilisation, since there is no charging current associated with DC power transfer as there is in AC systems. These issues may become of increasing importance as the capacity and area of offshore wind farms increase. A medium-voltage DC collection grid also has the potential to reduce losses through the use of medium-voltage converters and better optimisation of conversion stages. Additionally, a DC collection grid may reduce the size and weight of the required offshore

platform by replacing the heavy line-frequency transformers in an AC grid with high- or medium-frequency transformers that feature in recent, advanced DC/DC converters [2-7]. Optimising these collection architectures presents an opportunity for significant cost and efficiency savings.

Realising MVDC offshore networks requires efficient and reliable DC/DC converters to step up the wind generator output voltage (e.g. 5kV DC) to a level compatible with an efficient wide area network connection (e.g. 33kV DC). Presently, there is uncertainty regarding the architectures and control approaches needed to enable such high-capacity DC/DC power conversion, considering the limitations of available power semiconductor devices [8]. In such a collection network, this may require complex circuit topologies to achieve power sharing between multiple devices. Modular topologies, which replace a single high-voltage converter with a set of low-voltage converter modules, can overcome the limitations imposed by semiconductor voltage ratings and provide fault-tolerant operation. One possible solution is to use modular multilevel DC/DC converter (MMC) technology, which is effective in high-voltage power conversion such as HVDC applications. However, the effectiveness of such techniques in DC/DC converters is limited by insulation and isolation requirements [8-10]. Instead, a more compact and lighter design that uses a few modules arranged in a parallel-series topology could provide an excellent solution for realising scalable DC/DC converters to enable operation at the required level. Since the IPOS modular DC/DC converter exposes its modules to high DC voltage stresses, the use of insulation grading in combination with symmetrical monopole arrangement offers a practical method for reducing modules' insulation requirements, without significant cost penalties or compromise to system modularity.

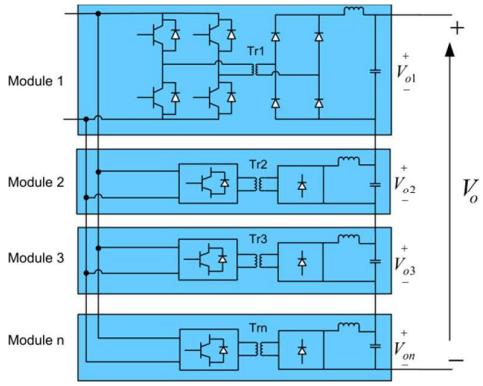


Fig.1. *IPOS converter topology with full-bridge DC/DC modules*

Input-parallel output-series (IPOS) connection is suitable for high input current and high output voltage, as required for interfacing wind turbine generators to MVDC collection

networks. Input-parallel connection ensures current sharing between modules, and improves dynamic performance and fault-tolerant operation, whilst the output-series connection of the high-voltage side has the capability of supporting the collection network voltage and reducing voltage stress per device, thereby avoiding the need for high-voltage diodes with short recovery times [11, 12]. Fig.1 represents a generic isolated full-bridge DC/DC converter with n modules and IPOS connection. Connection of multiple low-power rated modules as in an IPOS DC/DC converter provides an excellent solution for this application, with improved robustness and the possibility of fault-tolerant operation as a result of (n+k) designed redundancy. Such a modular structure allows even distribution of power amongst modules, thereby reducing thermal and electrical stresses in the switching devices and passive components of individual modules. Moreover, the use of power electronic building blocks reduces production and deployment costs [13, 14].

In typical applications, reliable operation of the IPOS modular DC/DC converter requires a control mechanism that ensures equal power sharing amongst the constituent modules under all conditions, including cases when module components have noticeable mismatch [14-16]. At present, the open literature contains few publications in the field of the IPOS converter and its control strategy. One topology uses the same duty cycle, generated from one outer voltage loop and one inner current loop, for all modules [17]. Although this approach offers a simple control structure, it cannot ensure power sharing between modules. This approach is not therefore suitable for medium-voltage applications, as modules may be exposed to the risk of damage from over-voltages during transients. The main weaknesses of this approach are addressed by use of a common output voltage loop, inner current loops and an output voltage sharing loop to achieve power sharing for a DC/AC converter [18]. Issues related to fault-tolerance control are not addressed. Uniform output voltage distribution across several modules has been realised using an output voltage distributed control scheme [19], but additional circuitry is required to provide fault-tolerant performance. In this paper, the overall output voltage controller builds on the Lyapunov stability law to make the system asymptotically stable. Additionally, this paper proposes a new master-slave control scheme and a distributed voltage sharing controller that ensure power sharing under all operating conditions, including during failure of the master module. To further improve performance, each module has its own sawtooth carrier, phase shifted by ±360°/n from adjacent modules.

Small-signal modelling of the IPOS DC/DC converter, based on the response of the converter to small perturbations, is introduced in Section 2 to enable study of the stability of the proposed system. The Lyapunov control design approach is introduced in Section 3. In

Section 4, the overall control topology with fault detection and redundancy is proposed. The proposed control scheme is validated using simulation and experiment under conditions of parameter mismatch and module failure. The main conclusions drawn from this study are summarised in Section 5.

2 Small-Signal Modelling of an IPOS-Connected DC/DC Converter

The efficiency of each module is assumed to be 100% and there are n modules in total. The relationship between input and output power can be obtained for each module as (1)

$$\begin{cases} V_{in}I_{in1} = V_{o1}I_o \\ V_{in}I_{in2} = V_{o2}I_o \\ \quad \cdots \\ V_{in}I_{inn} = V_{on}I_o \end{cases} \tag{1}$$

where V_{in} is the DC input voltage, I_{in1}, I_{in2}, …, I_{inn} are the module input currents, V_{o1}, V_{o2}, …, V_{on} are the module output voltages, and I_o is the load current. In the steady-state condition, output filter inductor currents are identical except for a small ripple component. In typical applications modules are not identical, exhibiting inherent component mismatches such as differences in transformer turns-ratios, capacitances and semiconductor devices nonlinearities, and these may cause unequal power distribution between modules. System reliability may suffer because the modules that contribute a greater portion of the power are thermally overstressed, and this may lead to unequal voltage sharing between individual modules [20, 21]. If output voltage sharing (OVS) is achieved, however, then, $V_{o1}=V_{o2}=\ldots=V_{on}$. Substituting this result for OVS into (1) gives (2).

$$I_{in1} = I_{in2} = \ldots = I_{inn} \tag{2}$$

It should be noted that input current sharing (ICS) is automatically achieved as long as OVS is achieved. Alternatively, if all modules share the same input current, then output voltage sharing is also achieved. In this paper, OVS is applied to achieve power balancing.

The small-signal model of the proposed converter is deduced by linearising about a given steady-state operating point, and used to design the control scheme. The small-signal equivalent circuit of two IPOS connected phase-shift full-bridge converters, which builds on a single module converter model [15], is shown in Fig.2, where k_1 and k_2 are the transformer turns-ratios, L_r is the transformer leakage inductance, D_e is the effective duty cycle per module, and L_{f1}, L_{f2}, C_{f1} and C_{f2} are the filter inductances and capacitances for modules 1 and 2 respectively. Input voltage perturbation is represented by Δv_{in}, input current perturbations for the two modules are Δi_{in1} and Δi_{in2} respectively, and filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δv_{o1} and Δv_{o2} respectively. Δd_1 and Δd_2

are duty cycle perturbations, and Δd_{v1}, Δd_{v2}, Δd_{i1} and Δd_{i2}, which respectively represent duty cycle perturbations due to input voltage and output current, are defined in (3).

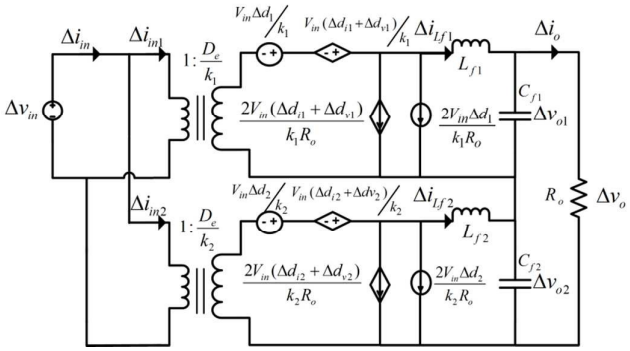


Fig.2. *Small-signal equivalent circuit of the IPOS connected two-module system*

$$\begin{cases} \Delta d_{v1} = \Delta d_{v2} = \dfrac{8L_r D_e f_s}{k^2 V_{in} R_o}\Delta v_{in} \\ \Delta d_{i1} = -\dfrac{4L_r f_s}{kV_{in}}\Delta i_{lf1} \\ \Delta d_{i2} = -\dfrac{4L_r f_s}{kV_{in}}\Delta i_{lf2} \end{cases} \tag{3}$$

To reduce the complexity of the small-signal transfer functions based on the feature of modularity [22], it is assumed that two modules have the same effective duty cycle, transformer turns-ratios, and capacitor and inductor values, i.e. $k_1=k_2=k$, $L_{f1}=L_{f2}=L_f$, and $C_{f1}=C_{f2}=C_f$. From Fig.2, application of Kirchhoff's voltage and current laws yields (4).

$$\begin{cases} \dfrac{D_e\Delta v_{in}}{k} + \dfrac{V_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = sL_f\Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e\Delta v_{in}}{k} + \dfrac{V_{in}}{k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = sL_f\Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{k}{D_e}\Delta i_{in1} = \dfrac{2V_{in}}{kR_o}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) + \Delta i_{lf1} \\ \dfrac{k}{D_e}\Delta i_{in2} = \dfrac{2V_{in}}{kR_o}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) + \Delta i_{lf2} \end{cases} \tag{4}$$

Module voltage perturbations are given by (5), which highlights the interaction between modules.

$$\begin{cases} \Delta v_{o1} = \dfrac{1}{sC_f}\left(\Delta i_{lf1} - \dfrac{\Delta v_{o1} + \Delta v_{o2}}{R_o}\right) \\ \Delta v_{o2} = \dfrac{1}{sC_f}\left(\Delta i_{lf2} - \dfrac{\Delta v_{o1} + \Delta v_{o2}}{R_o}\right) \end{cases} \tag{5}$$

This can be rewritten as (6).

$$\begin{cases} \Delta v_{o1} = \dfrac{1+sC_fR_o}{s^2C_f{}^2R_o+2sC_f}\Delta i_{lf1} - \dfrac{1}{s^2C_f{}^2R_o+2sC_f}\Delta i_{lf2} \\ \Delta v_{o2} = -\dfrac{1}{s^2C_f{}^2R_o+2sC_f}\Delta i_{lf1} + \dfrac{1+sC_fR_o}{s^2C_f{}^2R_o+2sC_f}\Delta i_{lf2} \end{cases} \tag{6}$$

Rearranging (6), the transfer function between module output voltages and currents can be obtained in the matrix form (7)

$$\begin{bmatrix} \Delta v_{o1} \\ \Delta v_{o2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} \tag{7}$$

where

$$\begin{cases} G_{11} = G_{22} = \dfrac{1+sC_fR_o}{s^2C_f{}^2R_o+2sC_f} \\ G_{12} = G_{21} = -\dfrac{1}{s^2C_f{}^2R_o+2sC_f} \end{cases} \tag{8}$$

Addition of the first two equations in (4) gives (9).

$$\begin{aligned} &\frac{2D_e\Delta v_{in}}{k} + \frac{V_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1} + \Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) \\ &= sL_f\Delta i_{lf1} + \Delta v_{o1} + sL_f\Delta i_{lf2} + \Delta v_{o2} \end{aligned} \tag{9}$$

Assuming that Δv_{in}=0, and Δd_k=0 (k=1, 2 and $k\neq j$), the relationship between load voltage and duty cycle, derived from (5) and (9), is used to design the system output voltage PI controller.

$$G_{ovd} = \frac{\Delta v_o}{\Delta d_j} = \frac{V_{in}/k}{L_fC_fs^2 + [\dfrac{2L_f}{R_o} + \dfrac{4L_rf_s}{k^2}C_f]s + \dfrac{8L_rf_s}{k^2R_o} + 1} \tag{10}$$

Substituting (3) and (6) into (4), assuming Δv_{in}=0, yields (11).

$$\begin{cases} \dfrac{V_{in}}{k}\Delta d_1 = [L_fs + \dfrac{1+C_fR_os}{C_f{}^2R_os^2+2C_fs} + \dfrac{4L_rf_s}{k^2}]\Delta i_{lf1} - \dfrac{1}{C_f{}^2R_os^2+2C_fs}\Delta i_{lf2} \\ \dfrac{V_{in}}{k}\Delta d_2 = -\dfrac{1}{C_f{}^2R_os^2+2C_fs}\Delta i_{lf1} + [L_fs + \dfrac{1+C_fR_os}{C_f{}^2R_os^2+2C_fs} + \dfrac{4L_rf_s}{k^2}]\Delta i_{lf2} \end{cases} \tag{11}$$

Rearranging (11), the relationship between duty cycle and inductor current can be represented as (12), highlighting that the current controllers for each module (shown in Fig.4) are designed independently.

$$\begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \tag{12}$$

where

$$\begin{cases} g_{11}=g_{22}=\dfrac{\mathrm{V}_{in}(s\mathrm{L}_f+\dfrac{1+sC_fR_o}{s^2C_f{}^2R_o+2sC_f}+\dfrac{4L_rf_s}{k^2})}{k(s\mathrm{L}_f+\dfrac{R_o}{s^2C_f{}^2R_o+2sC_f}+\dfrac{4L_rf_s}{k^2})\times(s\mathrm{L}_f+\dfrac{2+sC_fR_o}{s^2C_f{}^2R_o+2sC_f}+\dfrac{4L_rf_s}{k^2})} \\ g_{12}=g_{21}=-\dfrac{\mathrm{V}_{in}(\dfrac{-1}{s^2C_f{}^2R_o+2sC_f})}{k(s\mathrm{L}_f+\dfrac{R_o}{s^2C_f{}^2R_o+2sC_f}+\dfrac{4L_rf_s}{k^2})\times(s\mathrm{L}_f+\dfrac{2+sC_fR_o}{s^2C_f{}^2R_o+2sC_f}+\dfrac{4L_rf_s}{k^2})} \end{cases} \tag{13}$$

The transfer function between module output voltage and duty cycle is given in (14), and provides the basis for design of the output voltage sharing controller.

$$\begin{aligned} \begin{bmatrix}\Delta v_{o1}\\ \Delta v_{o2}\end{bmatrix}&=\begin{bmatrix}G_{11} & G_{12}\\ G_{21} & G_{22}\end{bmatrix}\begin{bmatrix}\Delta i_{lf1}\\ \Delta i_{lf2}\end{bmatrix} \\ &=\begin{bmatrix}G_{11} & G_{12}\\ G_{21} & G_{22}\end{bmatrix}\begin{bmatrix}g_{11} & g_{12}\\ g_{21} & g_{22}\end{bmatrix}\begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix} \\ &=\begin{bmatrix}G_{11}g_{11}+G_{12}g_{21} & G_{11}g_{12}+G_{12}g_{22}\\ G_{21}g_{11}+G_{22}g_{21} & G_{21}g_{12}+G_{22}g_{22}\end{bmatrix}\begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix} \end{aligned} \tag{14}$$

The controller is then designed by considering the phase margin of the closed-loop system, deduced from the small-signal model of the proposed system.

3 Lyapunov Design Approach to Closed-Loop Output Voltage Control

DC/DC converters are inherently nonlinear systems whose behaviour is set by circuit parameters which are subject to measurement uncertainty and variation due to ageing and thermal effects. The outer control loop of the IPOS DC/DC converter acts to regulate the total output voltage achieved by the constituent modules which must operate as single composite converter. Established linear control techniques, such as PI control, provide a simple implementation. However, this approach may limit converter performance. Non-linear techniques may be employed which have the capability to obtain a more accurate representation of the system dynamic, and to provide a robust response to parameter variations and enhanced transient response [23]. In this paper, the output voltage controller is developed using the Lyapunov stability law to ensure asymptotic stability of the system [24]. The stability of the closed-loop system can be tested by a control-Lyapunov function, i.e. for a scalar smooth positive definite and radially unbounded function $v(x)$ for control system $\dot{x}=f(x,u)$ there exists $u(x)$ such that $\frac{\partial v(x)}{\partial x}f(x,u(x))<0 \ \ \forall x\neq 0$ [25].

A reduced equivalent linearisation model which reduces a single full-bridge converter to an equivalent output filter model is employed to simplify the control design process [16]. The equivalent model of the IPOS DC/DC converter incorporating closed-loop output voltage control is presented in Fig.3 (a), which provides a linear representation of large-signal converter behaviour. The control input signal v_c is equal to the steady-state voltage before the rectifier bridge (as shown in Fig.1) [16]. The control-to-output transfer function is therefore approximated by (15)

$$G_{oc} = \frac{V_o(s)}{v_c(s)} \approx 2 \times \frac{2}{\pi} \frac{V_o(s)}{\bar{v}_{rec}(s)} = \frac{4}{\pi} \frac{1}{L_f C_f s^2 + 1} \tag{15}$$

where $\bar{v}_{rec}$ is the average value of the voltage across the input to the LC filter tank, as shown in Fig.3 (a). From Fig.3 (a), and using (16) and (17) obtained from the equivalent model, the control variable v_c is expressed in a second order transfer function of the output voltage as (18).

$$\frac{di_{lf1}}{dt} = \frac{1}{L_f}\left(\frac{2}{\pi} v_c - V_{o1}\right) = \frac{1}{L_f}\left(\frac{2}{\pi} v_c - \frac{1}{2} V_o\right) \tag{16}$$

$$\frac{dV_{o1}}{dt} = \frac{1}{2}\frac{dV_o}{dt} = \frac{1}{C_f}\left(i_{lf1} - i_o\right) = \frac{1}{C_f}\left(i_{lf1} - \frac{V_o}{R_o}\right) \tag{17}$$

$$\ddot{V}_o = \frac{1}{C_f}\left(\frac{4v_c}{L_f \pi} - \frac{V_o}{L_f} - \frac{2\dot{V}_o}{R_o}\right) \tag{18}$$

A function $r = \dot{e} + ae$ is defined, where e is the output voltage error between output voltage reference v_o^* and measured output voltage V_o, and α is an arbitrary real constant. A control-Lyapunov function $v(x)$ is defined as $v = \frac{1}{2} r^2$, which is positive definite for all $v_o^* \neq 0$ and $V_o \neq 0$. The time derivative of this function should be negative according to the Lyapunov stability law. To achieve a negative derivative, $\dot{v}$ is made to equal to $-bv$, where b is strictly a positive constant. The derivative is then negative definite under all system dynamic conditions and the closed-loop system will be globally stable. Substituting $-bv$ into the control-Lyapunov function and its derivative yields (19).

$$\ddot{v}_o^* - \ddot{V}_o + \alpha \dot{e} = -\frac{1}{2} b(\dot{e} + \alpha e) \tag{19}$$

Substituting (18) into (19) gives (20) which, when solved for v_c, yields the control law (21). Assuming v_o^* to be constant, $\dot{e} = -\dot{V}_o$ and $\dot{e} = -\ddot{V}_o$. Substituting (18) into (21) yields (22).

$$\left(\ddot{v}_o^* + \frac{V_o}{L_f C_f} - \frac{4v_c}{\pi L_f C_f} + \frac{2\dot{V}_o}{C_f R_o} + \alpha \dot{e}\right) = -\frac{1}{2} b(\dot{e} + \alpha e) \tag{20}$$

$$v_c = \frac{L_f C_f \pi}{4}(\ddot{v}_o^* + \frac{V_o}{L_f C_f} + \frac{2\ddot{V}_o}{C_f R_o} + \alpha\dot{e} + \frac{b}{2}r) \tag{21}$$

$$v_c = \frac{\alpha k C_f L_f \pi}{8}(v_o^* - V_o) - \frac{C_f L_f \pi}{4}(\frac{b}{2} + \alpha - \frac{2}{C_f R_o})\dot{V}_o + \frac{\pi}{4}V_o \tag{22}$$

Notice that the first and second terms of (22) imply that a PD controller is sufficient to ensure stability of the overall output voltage, where 'e' will decay to 0 as the system output voltage V_o converges to its reference set point. The $\pi V_o/4$ feed-forward term improves the start-up speed and helps to stabilise the controller. Therefore, (22) can be rewritten as (23).

$$v_c = k_p e + k_d \dot{e} + \frac{\pi}{4}V_o \tag{23}$$

Using the Routh-Hurwitz stability criterion [26], the system is stable if proportional and derivative gains k_p and k_d are both positive. By designing the damping ratio and natural frequency from the system characteristic equation (24), the required closed-loop performance can be achieved.

$$s^2 + \frac{4k_d}{L_f C_f \pi}s + \frac{4k_p}{L_f C_f \pi} = 0 \tag{24}$$

Thus, the closed-loop output voltage controller obtained using the Lyapunov approach is shown in Fig.3 (b). This is compared with a linear PI output voltage closed-loop controller shown in Fig.3 (c) based on the small-signal model transfer function (10). The robustness of the Lyapunov based controller to circuit parameter variations and its superior performance are shown by comparing the system bandwidth of the two controllers. Fig.3 (d) shows that the system bandwidth achieved using PI control is 620Hz, whilst that achieved using the Lyapunov controller is 1.83kHz. According to the comparison, the Lyapunov controller, which features faster dynamic response at start-up and higher disturbance rejection capability, is applied to produce the main control signal Δi (current command) to track the output voltage reference. The overall control system with power sharing ability and redundancy is described in Section 4.

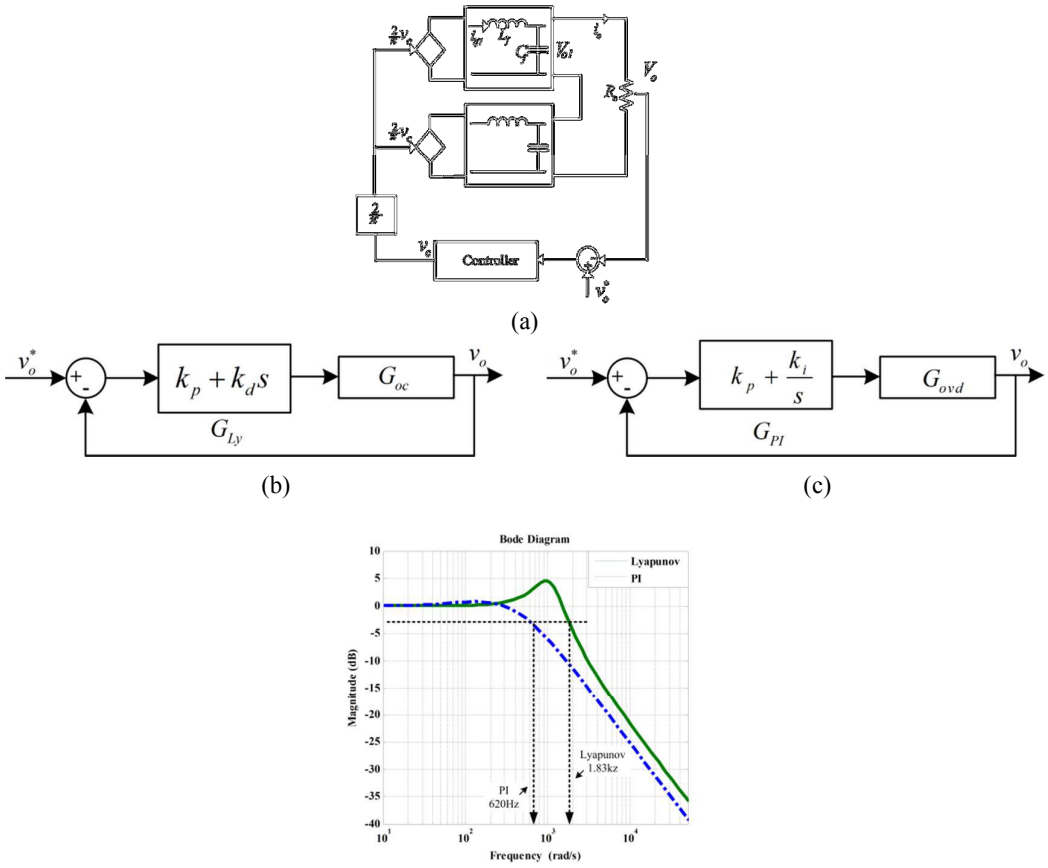


Fig.3. *(a) Equivalent model for the IPOS DC/DC converter (b) Lyapunov closed-loop controller (c) conventional PI closed-loop controller (d) closed-loop bandwidth comparison*

4 Overall Control Performance with Fault Detection and Redundancy

4.1 Overall Control System

The overall output voltage controller was designed using the Lyapunov approach. For power sharing control, the average active sharing method or master-slave sharing method is normally employed to provide a conventional means of solving the power sharing issue with mismatched components amongst the modules, and other challenging conditions such as inconformity of the transfer function, switching delay and discontinuity caused by the switching time delay, and input voltage disturbance [27]. In the master-slave control method, the master module is responsible for load regulation whilst the slaves ensure equal current or voltage sharing amongst the modules. Compared to the average active sharing method, fault-ride-through under slave module failure may be achieved more simply using master-slave control, with input current and output voltage being evenly shared amongst the remaining healthy modules to avoid module overload that could lead to cascade failure of the entire system.

The proposed control system builds on the conventional master-slave scheme with one master module controlled by the PD controller to produce control signal Δi (current command), and uses the procedure outlined in Section 3 to control the output voltage, (n-1) slave modules to produce the voltage balancing current reference quantities Δi_i (i=1, 2,…, n-1), and individual inner current loops for each module. The Lyapunov function is used to establish a structure for the load voltage controller that ensures global system stability, and has resulted in a PD controller. The modular output voltage controller balances the slave module output voltages and compensates for any disturbance by minimising the differences between the slave output voltages and the voltage reference signal to generate the inductor current contributions Δi_1, Δi_2, Δi_3 and Δi_{n-1} through the PI controller. In this case, each slave module output voltage controller tracks the set-point, $V_{o1}^{*} = V_{o2}^{*} = V_{o(n-1)}^{*} = V_o/n$ (under normal condition), with zero steady-state error. The sum of the current references $\sum_{i=1}^{n-1} \Delta i_i$ produced by all of the slave modules is subtracted from the current reference for the master module (the n^{th} module in Fig.1), and Δi is added to the current reference of each slave module. During steady-state operation, the integral term in the modular output voltage controller contributes the majority of the current demand to the inner current control loop. It should be noted, however, that the PD controller plays the most crucial role during start-up and other major transient events such as module failure. A third current control loop, which is designed according to (12), is added for each module in order to improve performance. The resulting control structure is shown in Fig.4 (a).

The multi-module DC/DC converter has internal fault management capability, in that faulty modules may be bypassed in order to allow continued system operation without any performance degradation [28]. Such a feature is normally achievable by incorporating redundant modules to allow re-configuration of the power circuit and bypassing of the faulty modules. The modularity feature allows (n+k) redundancy, where n is the number of modules required to ensure that each module operates within its voltage rating, and k is the number of redundant modules that can be used to replace k faulty modules and maintain uninterrupted operation. (n+1) redundancy is introduced in this paper.

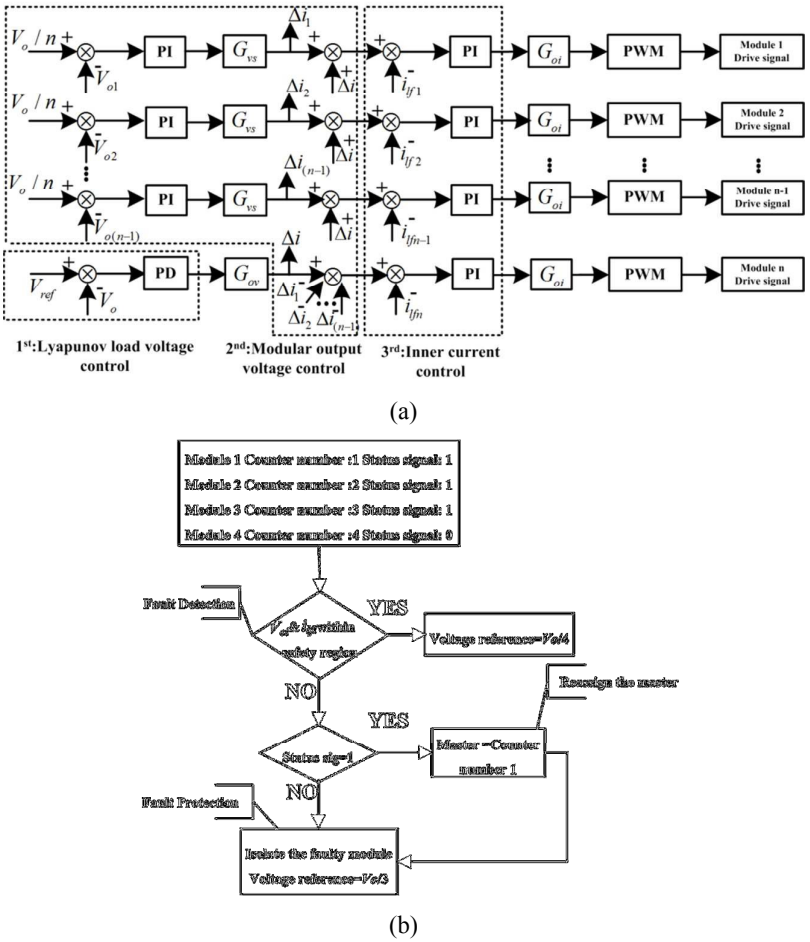


Fig.4. *(a) Overall control scheme and (b) flow chart for the 'non-dedicated master' control scheme*

The modular structure facilitates identification of fault location and bypassing of the faulty modules. The failure of a single or multiple modules is detected by monitoring their output voltages and currents so that they can be compared with predefined limits such as $[0.2V_o<V_{oi}<0.3V_o]$, for $i=1,...,n$ ($n=4$ in this paper). The faulty modules are isolated by blocking their front-end H-bridge converters and their corresponding output diode bridges are bypassed using a combination of bypass switches and bleed resistors to dissipate the energy stored in their DC-side filter capacitors. When any slave module fails, it is identified and bypassed while the system remains operational. In this case, the voltage reference to the slave modules must be changed. For an example, when 'k' modules from n modules have failed, the reference voltage for all slave modules must be changed from V_o/n to $V_o/(n-k)$. The commonly used master-slave scheme, however, has difficulty ensuring $(n+1)$ redundancy in the event of a fault in the master module, which is a consequence of the 'fixed master' characteristic. Consequently, malfunction of the master module will lead the overall system failure [29]. Using such a control scheme for the modular DC/DC converter being studied is

less attractive from the system reliability point of view. In order to avoid system collapse, a 'non-dedicated master' approach is proposed, which enables the role of 'master' to be reallocated to another healthy module when the original master module fails. Because each module has the ability to become a master if required, any module may malfunction without affecting the operation of the whole system. The failure flow graph for a four-module DC/DC converter is shown in Fig.4 (b).

For an n module converter, each module is assigned with a specific numerical identifier between 1 and n. The control system assigns the status signal '0' to a master module and '1' to the remaining modules, which are slaves. The fault detection and protection function will be actived when the affected modules' output voltages or currents are outside the predefined limits. When 'k' slave modules fail the voltage reference for the remaining healthy slave modules is updated to $V_o/(n\text{-}k)$. The master module will remain the same. When the master module fails, one of the healthy slave modules will be assigned to become the new master module (the module with the next counter number to the previous master module) and the voltage reference for the slave modules must be updated. The faulty master module must be isolated immediately.

4.2 Simulation Validation

In order to assess the effectiveness of the proposed control scheme for the IPOS DC/DC converter, the system in Fig.5 (a) that consists of a generator connected to an uncontrolled diode rectifier and an IPOS DC/DC converter with rated output power of 5MW is simulated. Generator output voltage is 2500V at 50Hz, the medium-frequency transformer operates at 5kHz and has a turns-ratio of 2500:8250V, and the load voltage is maintained at 33kV. Module 1 is initially chosen as the master module. To test the effectiveness of the power balancing function when parameter mismatch is considered, the following mismatches are assumed: +10% in module 1 transformer turns-ratio, and +10% in module 2 output filter capacitance. To show enhanced system reliability when the master module fails, a permanent short-circuit fault is applied at the output terminals of the master module (module 1) at t=50ms. Selected simulation results obtained for this case are summarised in Fig.5 (b) to (d).

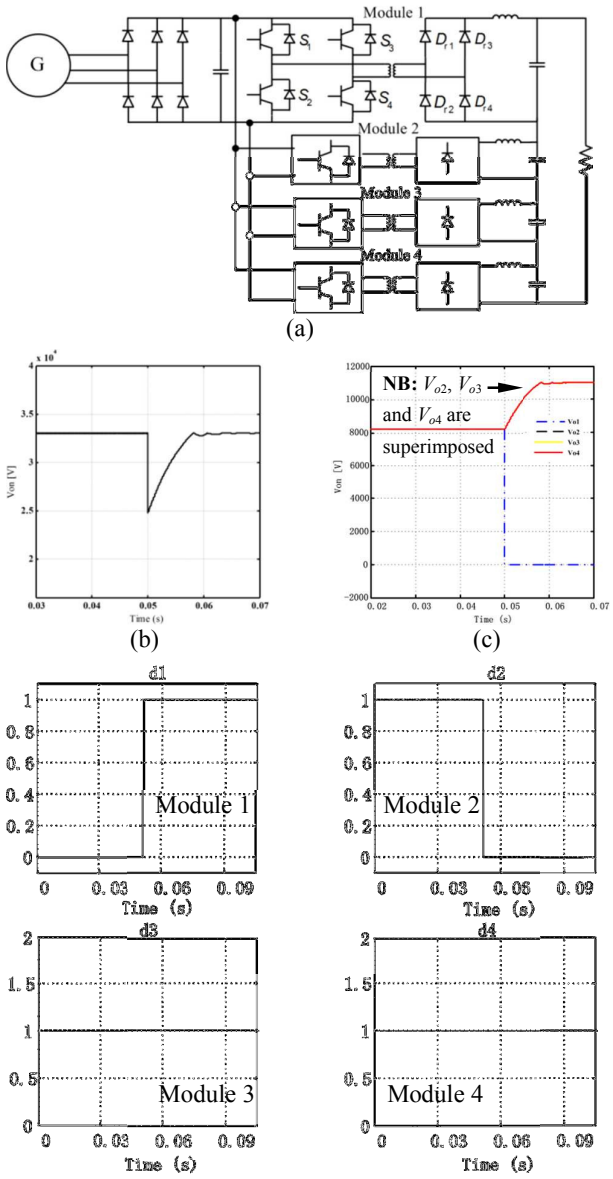


Fig.5. *(a) High-power system used in fault study (b) load voltage response (c) module output voltage response (d) allocation of 'master' and 'slave' roles*

Fig.5 (b) shows the converter output voltage V_o and Fig.5 (c) shows the individual module output voltages V_{o1}, V_{o2}, V_{o3} and V_{o4}. Observe that in the pre-fault condition the proposed control scheme is able to ensure equal output voltage sharing amongst the modules, despite the presence of substantial parameter mismatch in various modules. Following the fault at t=50ms, the faulty module is isolated and the output voltages of the remaining healthy modules have increased to compensate the lost module (i.e. to maintain the output voltage at the pre-fault value). These results show that the proposed control scheme manages failure of the master module, whilst ensuring continuous operation and equal voltage sharing amongst the remaining healthy modules. Following the fault, the 'non-dedicated master' control

function reallocates the role of 'master' to a healthy module, which in this case is module 2. This process is illustrated in Fig.5 (d) which shows the signals that define the 'master' and 'slave' status of the modules. The i^{th} module is defined as 'master' or 'slave' when d_i=0 or d_i=1 respectively. It can be seen that, following the fault, module 1 is deselected as 'master' module and module 2 is selected as the new 'master'.

4.3 Experimental Validation

To validate the proposed control scheme, a prototype four-module IPOS DC/DC converter rated at 200W was built. Its proposed control system was implemented using an Infinoeon Technology Tricore TC1796 microcontroller. Fig.6 and Table I resectively show the experimental test rig and its main parameters.

Fig.6. *ISIPOS connected full-bridge DC/DC converter test rig*

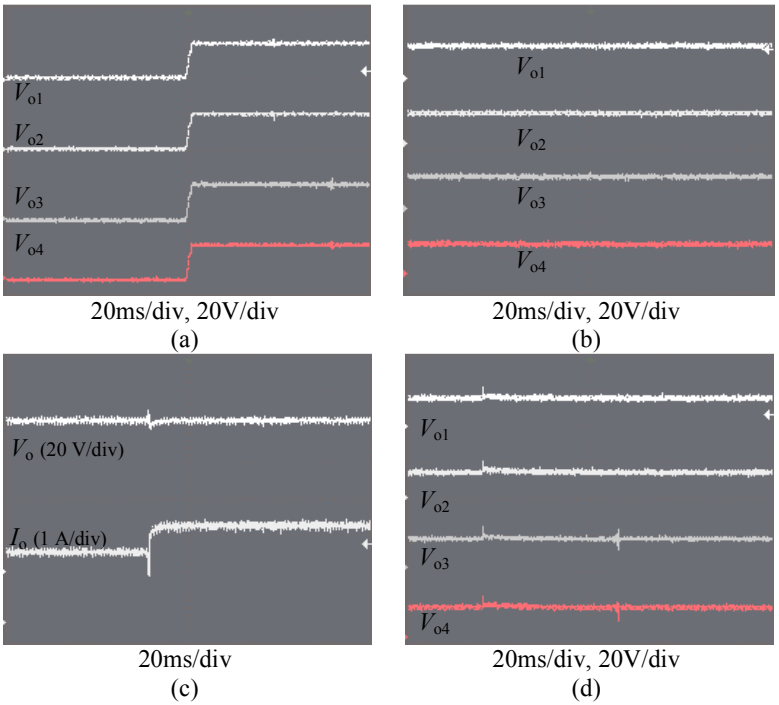
TABLE I. EXPERIMENTAL SYSTEM PARAMETERS

Item	*Value*
DC/DC Converter Rated Power	200W
Input DC Voltage	20V
Number of Modules	4
Input Capacitance	C_{d1}=45 μF, C_{d2}=40 μF
Transformer Turns Ratio	T_1=1:1.4, T_2=1:1.2, T_3=1:1.3, T_4=1:1.2
Output Inductance	L_1=6.8mH, L_2=5mH, L_3=5.9mH, L_4=6.3mH
Output Capacitance	C_1=160 μF, C_2=160μF, C_3=200μF, C_4=200μF
PWM Carrier Frequency	5kHz

To demonstrate the robustness of the power (output voltage) sharing that the proposed control strategy offers, Fig.7 (a) and (b) present individual module output voltages (V_{o1}, V_{o2}, V_{o3} and V_{o4}) during start-up and steady-state operation of the four-module DC/DC converter. Observe that the experimental output voltages of all four modules are tightly regulated during start-up, when the output voltage reference is ramped from 0 to 80V within 5ms, and during steady-state. These results are achieved despite the noticeable mismatch in the transformer turns-ratios, filter capacitances and inductances of the modules as detailed in Table I.

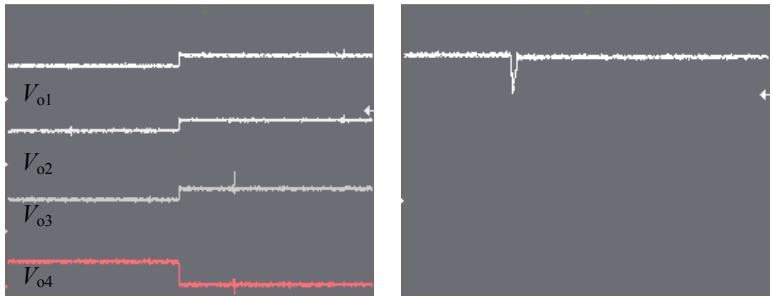
Fig.7 (c) and (d) show selected experimental results obtained when load resistance is decreased to illustrate the dynamic response of the IPOS modular DC/DC converter when the proposed control scheme is employed. Fig.7 (c) shows that the overall output voltage (V_o) is

regulated exactly at the desired set-point before and after the change in load resistance, and that output current (I_o) is increased as the load resistance is decreased. Observe that the output voltage and current in Fig.7 (c) and the individual module output voltages (V_{o1}, V_{o2}, V_{o3} and V_{o4}) in Fig.7 (d) only exhibit minimal transients following the increase in load (decrease of the load resistance from 40Ω to 32Ω).



20ms/div, 20V/div (a)
20ms/div, 20V/div (b)
20ms/div (c)
20ms/div, 20V/div (d)

Fig.7. *Experimental results with the proposed control strategy (a) module output voltages during start-up, (b) module output voltages during steady-state (c) output voltage and current response during load transient (d) module output voltages during load transient*



100 ms/div, 20V/div (a)
10 ms/div, 20V/div (b)

Fig.8. *Experimental results with the proposed control strategy (a) module output voltages (b) output voltage response during master-module fault transient*

To demonstrate the fault-tolerant capability of the proposed 'non-dedicated master' control scheme, a short-circuit fault is applied at the output terminal of the master module (module 4 in the experimental test rig). During the pre-fault condition, the load voltage is

equally shared amongst the modules. Following detection of the fault, module 4 is isolated and its output voltage falls to zero, as shown in Fig.8 (a). Meanwhile, the 'non-dedicated master' control function reallocates the role of master to module 1 and the output voltages of the remaining healthy modules are boosted to $⅓V_o$ to compensate for the lost contribution of the faulty module. Output voltage V_o is therefore maintained at its pre-fault value, after a short duration voltage dip, and is shared equally between the healthy modules, as shown in Fig.8 (b). These results show that the proposed control scheme is capable of managing a master module fault, whilst ensuring continuous operation of and equal voltage sharing amongst the remaining healthy modules.

The dedicated master-slave control strategy can respond appropriately only to slave module faults. In comparison, these experimental results with the proposed 'non-dedicated master' control scheme show that it enables the converter being investigated to ride through fault conditions by permitting reallocation of the role of 'master' to a healthy module. This is achieved without any compromise to power sharing between the modules. However, to ensure the voltage and current stresses in each module, for constant load voltage, remain within the permissible range for continuous operation, both control strategies rely on the use of 'k' redundant modules to replace up to 'k' faulty modules from a total of 'n+k' modules.

5. Conclusions

This paper presented a robust control strategy suitable for MVDC applications that ensures equal power sharing between modules of an IPOS modular DC/DC converter when modules have parameter mismatches and during failure of some modules. A comparative study of output voltage control approaches shows that the non-linear controller has an advantage over a linear PI controller in terms of improved transient response and robustness to parameter variations. With regard to (n+1) redundancy, in comparison to previous dedicated master-slave schemes which responds appropriately to slave module faults only, the proposed controller permits reallocation of the master role to any healthy module when the original master module fails. This allows fault ride-through to be achieved independent of fault location. The viability of the control scheme has been confirmed through simulation and experimentation, where the results show that the converter system being studied exploits true (n+1) redundancy to maintain power balance amongst the remaining healthy modules during internal faults. The converter topology and control strategy can be readily extended to converters composed from any number of modules.

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