Zero-Voltage-Switching Buck Converter with Low Voltage Stress using Coupled Inductor

Abstract–This paper presents a new design of zero-voltage-switching (ZVS) buck converter. This new converter utilizes a coupled inductor to implement the output filter inductor as well as the auxiliary inductor which is commonly employed to realize ZVS for switches. Additional magnetic core for the auxiliary inductor in traditional designs is removed and hence manufacture cost is reduced. Moreover, thanks to the series connection between the input and output, the switch voltage stress in the steady-state is reduced and thus the ZVS operation can be easier achieved. Then the leakage inductor current circulating in the auxiliary switch is decreased, contributing to reduced conduction losses. Especially, low voltage rating devices with low on-state resistance can be adopted to further improve efficiency in the application with non-zero output voltage all the time, such as the battery charger. Furthermore, the reverse-recovery problem of the diode is significantly alleviated by the leakage inductor of coupled inductor. In the paper, operation principle and steady-state analysis of the proposed converter are presented in detail. Meanwhile, design considerations are given to obtain circuit parameters. Finally, the simulation and experimental results of a 200W prototype circuit are demonstrated to validate the advantages and effectiveness of the proposed converter.

None of the material in this paper has been published or is under consideration for publication elsewhere.

I. INTRODUCTION

DC-DC converters have been widely utilized in the industrial applications, such as voltage regulator module (VRM), power factor correction (PFC), renewable energy system, power supply and so on. In DC-DC converters, high density and high efficiency are the main focus of attention [1]. To achieve higher density, a simple yet effective solution is to increase switching frequency, which allows for considerable size reduction of the passive component. However, higher switching frequency results in deteriorated switching loss and lower efficiency in the conventional hard-switching converters. In order to overcome the conflicts between high

switching frequency and low efficiency, zero-voltage-switching (ZVS) techniques [2-27] including quasi-resonant ZVS, multi-resonant ZVS, zero-voltage-transition (ZVT) and active-clamping ZVS, have been employed to eliminate the turn-on loss which is mainly concerned in the high frequency application with majority carrier device such as MOSFET.

Quasi-resonant converters (QRCs) in [2-5] use *LC* resonant components to create a zero-voltage turn-on condition for the switching device. Therefore, the switching loss is greatly reduced. However, the switch is subjected to high voltage stress which is proportional to the load. Besides, a wide switching frequency range is required for the converter to operate with a wide input voltage and load range due to the variable frequency control. As a consequence, the suitable application of QRCs is limited. Moreover, severe parasitic oscillation between the junction capacitance of the diode and the resonant inductor increases the switching noise and the converters instability. Though the oscillation is eliminated in the multi-resonant converters (MRCs) through absorbing all parasitic capacitances of switch and diode into the resonance process, severe drawbacks of high voltage stress and variable frequency remain [6,7].

Compared to the QRCs and MRCs, the merit of ZVS operation is retained while the voltage stress is reduced in the ZVT converters because the resonant inductor is removed out of the main circuit [8-19]. Moreover, the converter is controlled by pulse-width modulation instead of variable frequency, which simplifies the circuit design. However, extra switching loss occurs in the auxiliary switch as a result of zero-current-switching (ZCS) turn-on and ZVS turn-off [12-14]. The soft-switching characteristic of the auxiliary switch is improved in the self-commutated auxiliary circuit, which achieves ZCS turn-on and turn-off for the auxiliary switch in [15]. Although the switching loss of the auxiliary switch is improved, the auxiliary circuit is complicated. In [16,17], a simple ZCS auxiliary circuit only consisting of a unidirectional switch and an auxiliary inductor is proposed. But the ZVS of main switch will lose under improper voltage conversion ratio [18]. In [19], a slave output was utilized to effectively improve the ZVS characteristic but also with the penalty on the increased auxiliary circuit complexity. Therefore, compromise should be made between the main switch and the auxiliary circuit.

The active-clamping DC-DC converters can achieve ZVS for both main switch and auxiliary switch in [20-26]. Besides, the oscillation induced by the diode junction capacitor is suppressed by simply adding a clamping diode and a resonant capacitor [27]. However, switches suffer from high voltage stresses in these converters. Moreover, non-isolated converters in [20-21,27] need additional magnetic cores to implement the auxiliary inductors, which are also demanded in QRCs, MRCs and ZVT converters. Therefore, the volume and the cost are increased.

In order to eliminate the requirement of additional magnetic cores, non-isolated ZVS DC-DC converters with coupled inductors are proposed to implement the auxiliary inductor by the leakage inductor and utilize the magnetizing inductor to acts as a filter inductor [28-31]. The elimination of the additional magnetic core results in reduced volume and improved power density. However, disadvantages of high voltage stress on the auxiliary diode and increased dc-bias of magnetizing current degrade the improvement.

From above, ZVS converters with merits of low voltage stress and reduced magnetic component are considerably desired. In the paper, an improved non-isolated ZVS buck converter with a coupled inductor is proposed in Fig.1. The voltage across junction capacitors of the main switch S_1 and the auxiliary switch S_2 are discharged to zero before turn-on by the leakage inductor and magnetizing inductor of the coupled inductor, respectively. ZVS operation is realized for both switches and hence reduced switching loss and EMI noise are achieved. Moreover, two switches are series connected between the input and the output. Therefore, the switches voltage stresses in the steady-state are decreased. Furthermore, benefit of reduced magnetic component is retained with the coupled inductor. Also, the dc-bias of magnetizing current is decreased, which can further achieve efficiency improvement.

The paper is organized as follows. The operation principle of the proposed ZVS buck converter is presented in detail in section II. Steady-state analysis is illustrated in section III and design considerations are shown in section IV. The simulation and experimental results of a 200W prototype circuit are demonstrated in section V to validate the effectiveness of the converter. Finally, conclusion is given in the section VI.

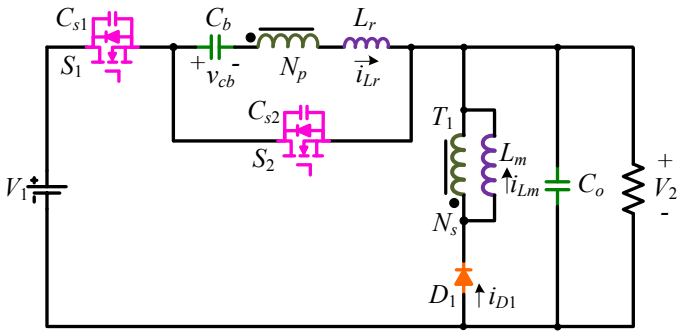


Fig.1. The proposed ZVS buck converter.

II. Operation Principle

The proposed converter is shown in Fig.1. It consists of two switches S_1-S_2 with parasitic capacitors C_{s1}-C_{s2}, a diode D_1, a blocking capacitor C_b and a coupled inductor T_1. The coupled inductor T_1 is modelled as a magnetizing inductor L_m, a leakage inductor L_r and an ideal transformer T_1 with turns ratio of N_p:$N_s = n$:1.

Key operating waveforms of the proposed converter is shown in Fig.2. Switches S_1 and S_2 are operated with the asymmetrical pulse-width modulation. The operation is composed of 7 different stages in a switching period, and equivalent circuits in different stages of a switching cycle are illustrated in Fig.3.

To simplify the analysis of operation principle, some assumptions are made.

(1) The magnetizing inductance L_m is much larger than the leakage inductance L_r.

(2) The parasitic capacitances C_{s1}-C_{s2} are constant in the switching process and the sum of them is denoted as C_{ds}.

(3) All components are ideal except for the parasitic parallel capacitors of switches.

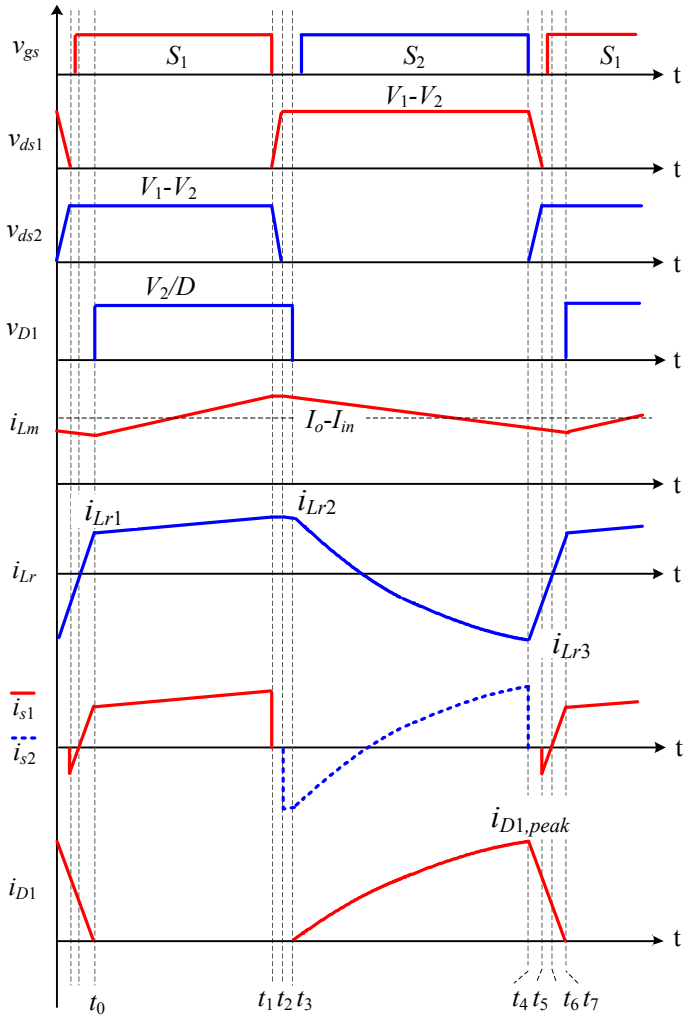


Fig.2. Key operating waveforms of the proposed converter.

Prior to t_0, S_1 is on and S_2 is off. D_1 is forward biased. The leakage current i_{Lr} is increased while the diode current i_{D1} is decreased.

Stage 1 (t_0-t_1): At t_0, the diode current i_{D1} decays to zero. Therefore D_1 is reverse biased. In this stage, the blocking capacitor C_b, the leakage inductor L_r and the magnetizing inductor L_m are charged by V_1-V_2, which is the difference between the input and the output. Energy is transferred from the input to the magnetizing and leakage inductors, the blocking capacitor and the output. Therefore, the leakage current i_{Lr}, the magnetizing current i_{Lm} and the blocking capacitor voltage v_{cb} are increased.

$$i_{Lr}(t) = i_{Lr}(t_0) + \frac{V_1 - V_2 - v_{cb}(t)}{L_r + n^2 L_m}(t - t_0) \tag{1}$$

$$i_{Lm}(t) = n i_{Lr}(t) \tag{2}$$

$$v_{cb}(t) = v_{cb}(t_0) + \frac{i_{Lr}(t)}{C_b}(t - t_0) \tag{3}$$

Stage 2 (t_1-t_2): S_1 is turned off at t_1. The parasitic parallel capacitors C_{s1} and C_{s2} are charged and discharged by the combination of the magnetizing inductor L_m and the leakage inductor L_r. The voltage across C_{s1}, which is denoted as v_{ds1}, rises from 0 to V_1-V_2. i_{Lr} and i_{Lm} are nearly constant in this stage since the magnetizing inductance is large.

$$v_{ds1}(t) \approx \frac{i_{Lr}(t_1)}{C_{ds}}(t-t_1) \tag{4}$$

Stage 3 (t_2-t_3): The drain-to-source voltage across S_1 rises to V_1-V_2 and the drain-to-source voltage across S_2 decays to zero at t_2, thus the current commutes to the anti-parallel diode of S_2. In this stage, C_b resonates with L_r and L_m. The blocking capacitor voltage v_{cb} is increased and the voltage across the magnetizing inductor L_m reaches to the output voltage V_2 at t_3. Then the diode D_1 starts to conduct.

$$\frac{i_{Lm}(t)}{n} = i_{Lr}(t) = i_{Lr}(t_2) - \frac{v_{cb}(t)}{L_r + n^2 L_m}(t-t_2) \tag{5}$$

$$v_{cb}(t) = v_{cb}(t_2) + \frac{i_{Lr}(t)}{C_b}(t-t_2) \tag{6}$$

The average voltage V_{cb} across the blocking capacitor C_b nearly equals to nV_2 as given in (7) when the fluctuation of capacitor voltage is small enough to be neglected.

$$V_{cb} \approx nV_2 \tag{7}$$

Stage 4 (t_3-t_4): In this stage, D_1 is forward biased and the magnetizing inductor L_m is clamped by the output. Therefore, the blocking capacitor C_b resonates with the leakage inductor L_r. The leakage current i_{Lr} is decreased while the diode current i_{D1} is increased. To achieve ZVS operation, the active switch S_2 should be turned on before i_{Lr} turns to negative. In this stage, energy is transferred from magnetizing inductor to the output.

$$i_{Lr}(t) = i_{Lr}(t_3) + \frac{nV_2 - v_{cb}(t)}{L_r}(t-t_3) \tag{8}$$

$$i_{Lm}(t) = i_{Lm}(t_3) - \frac{V_2}{L_m}(t-t_3) \tag{9}$$

$$i_{D1}(t) = i_{Lm}(t) - ni_{Lr}(t) \tag{10}$$

Stage 5 (t_4-t_5): S_2 is turned off at t_4. The voltage across the magnetizing inductor L_m remains unchanged because the diode D_1 is still conducting. Therefore, the parasitic parallel capacitors C_{s1} and C_{s2} are resonant with the leakage inductor L_r. The voltage across C_{s2}, which is denoted as v_{ds2}, rises from zero to V_1-V_2.

$$i_{Lr}(t) = i_{Lr}(t_4) + \frac{v_{ds2}(t) + nV_2 - v_{cb}(t)}{L_r}(t-t_4) \tag{11}$$

$$v_{ds2}(t) = -\frac{i_{Lr}(t)}{C_{ds}}(t - t_4) \tag{12}$$

Stage 6 (t_5-t_6): The voltage across S_2 rises to V_1-V_2 and the voltage across S_1 decays to zero at t_5. Then the leakage current i_{Lr} flows through the anti-parallel diode of S_1. Therefore, S_1 is ZVS turned on. In this stage, the leakage current i_{Lr} is increased while the diode current i_{D1} is decreased.

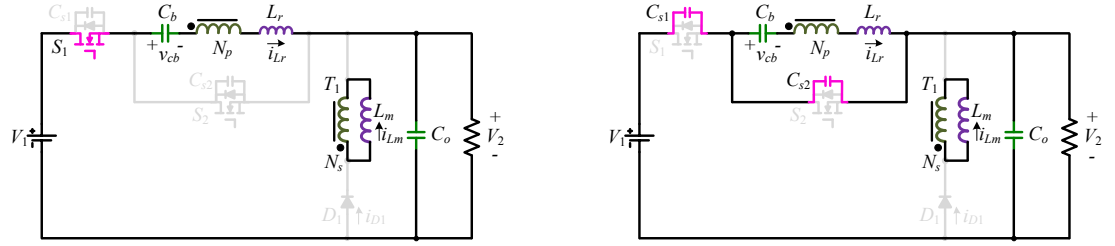
$$i_{Lr}(t) = i_{Lr}(t_5) + \frac{V_1 + (\text{n-1})V_2 - v_{cb}(t)}{L_r}(t - t_5) \tag{13}$$

$$i_{D1}(t) = i_{Lm}(t) - n i_{Lr}(t) \tag{14}$$

Owing to the leakage inductor L_r and magnetizing inductor L_m, the falling rate of the diode current i_{D1} is small. It is mainly determined by L_r as shown in (15) since L_m is so large that di_{Lm}/dt can be neglected.

$$\frac{di_{D1}(t)}{dt} = \frac{di_{Lm}(t)}{dt} - n\frac{di_{Lr}(t)}{dt} \approx -n\frac{V_1 + (n-1)V_2 - V_{cb}}{L_r} \tag{15}$$

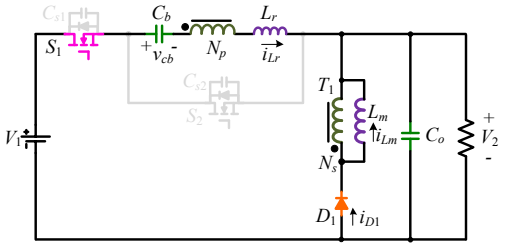
Stage 7 (t_6-t_7): The leakage current i_{Lr} increases to zero at t_6. The state of this stage is the same as the stage 6 except that i_{Lr} is positive. The switching period ends at t_7 when the diode current i_{D1} drops to zero.



(a) t_0-t_1 (b) t_1-t_2

(c) t_2-t_3 (d) t_3-t_4

(e) t_4-t_5 (f) t_5-t_6



(g) t_6-t_7

Fig.3. Equivalent circuits of the proposed converter in different stages. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (b) Stage 5. (c) Stage 6. (d) Stage 7.

III. Steady-State Analysis

A. Voltage Transfer Ratio

From the flux balance of the magnetizing inductor L_m, (16) is derived when the dead-time between S_1 and S_2 is ignored and the effect of the leakage inductor L_r is neglected.

$$\frac{D(V_1 - V_2 - V_{cb})}{n} = (1-D)V_2 \tag{16}$$

where D is the duty cycle of S_1.

Substituting (7) into (16), the voltage transfer ratio M of the proposed converter is calculated in (17). The relationship between M and D with different value of n is depicted in Fig.4. To achieve same voltage transfer ratio M, the duty cycle D is increased in the proposed converter compared with the conventional buck converter. Therefore, the ripple current of the inductor L_m in (18) is decreased. But the maximum transfer ratio is smaller than that of the conventional buck converter, which may result in slower transient response.

$$M = \frac{V_2}{V_1} = \frac{D}{n+D} \tag{17}$$

$$\Delta i_{Lm} = \frac{(1-D)V_2 T_s}{L_m} \tag{18}$$

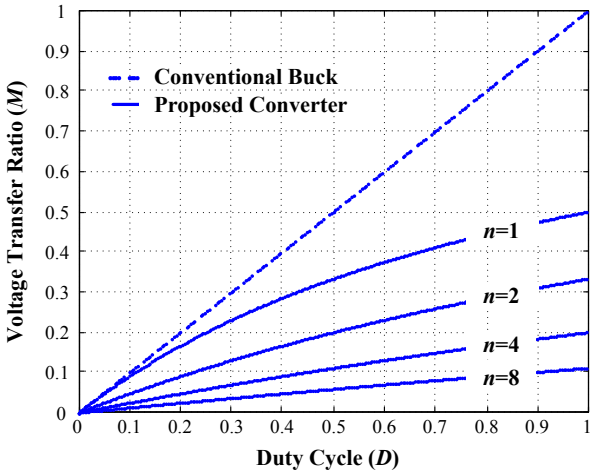


Fig.4. Relationship between M and D in the proposed converter and conventional buck converter.

It is noteworthy that the effective duty cycle D_{eff} is a little smaller than D. The loss of duty cycle, which is denoted as ΔD, is mainly caused by the leakage inductor L_r. As shown in Fig.2, the diode current i_{D1} is linearly decreased in the interval t_4-t_7 and hence the voltage across magnetizing inductor L_m keeps unchanged. The duration of the interval t_4-t_7 is mainly determined by the falling rate of diode current di_{D1}/dt and the peak diode current $i_{D1,peak}$. In (19), $i_{D1,peak}$ is approximately derived from the average output current I_o and the average input current I_{in}. Then ΔD is derived in (20) from (15) and (19), and the voltage transfer ratio M is revised in (21), where $D_{eff} = D - \Delta D$.

$$i_{D1,peak} \approx \frac{2(I_o - I_{in})}{1-D} = \frac{2(1-M)I_o}{1-D} = \frac{2(V_1 - V_2)^2 I_o}{V_1(V_1 - (n+1)V_2)} \tag{19}$$

$$\Delta D = \frac{-i_{D1,peak}}{T_s}\frac{dt}{di_{D1}(t)} = \frac{2L_r I_o(1-M)}{n(V_1 - (n+1)V_2)T_s} \tag{20}$$

$$M = \frac{V_2}{V_1} = \frac{D_{eff}}{n + D_{eff}} \tag{21}$$

B. ZVS Performance of Switches and Reverse-Recovery Problem Alleviation of Diode

The ZVS operation of S_2 can be easily achieved as long as the dead-time between S_1 and S_2 is appropriate because the energy needed is provided by the combination of the magnetizing inductor L_m and the leakage inductor L_r. S_1 is ZVS turned on when the energy stored in L_r is large enough to discharge the parallel capacitor C_{ds} as shown in (22) and the dead-time t_d between S_2 and S_1 satisfies the relationship in (23). From (22), the ZVS operation in the proposed converter is easier to achieve since the turn-off voltage of switches is reduced to V_1-V_2 and hence less energy is required to store in L_r. Therefore, the conduction loss in the auxiliary switch caused by the leakage inductor current is reduced.

$$L_r i_{Lr}(t_4)^2 > C_{ds}(V_1 - V_2)^2 \tag{22}$$

$$(t_5 - t_4) < t_d < (t_6 - t_4) \tag{23}$$

As shown in Fig.2 and (15), the diode current i_{D1} is decreased in the interval t_4-t_7 with the falling rate determined by the leakage inductor L_r. Thus, the output diode reverse-recovery problem is greatly reduced.

C. DC-Bias of Magnetizing Current

As illustrated in Fig.1 that the magnetizing current i_{Lm} is always equal to the sum of the reflected leakage current ni_{Lr} and the diode current i_{D1}, as given in (24). The average leakage current I_{Lr} is zero because L_r is series connected with the blocking capacitor C_b. Therefore, the dc-bias of the magnetizing current I_{Lm} derived in (25) is equal to the difference between the average output current I_o and the average input current I_{in}. From (25), I_{Lm} is decreased with the increase of voltage transfer ratio M and can be much smaller than I_o when M is large.

$$i_{Lm}(t) = ni_{Lr}(t) + i_{D1}(t) \tag{24}$$

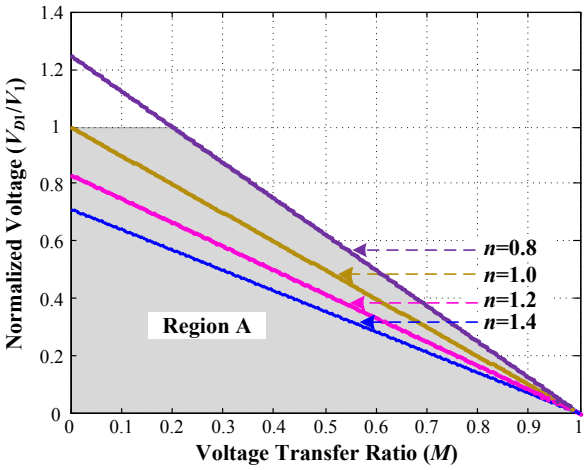
$$I_{Lm} = I_{D1} = I_o - I_{in} = (1 - M)I_o \tag{25}$$

D. Voltage Stress

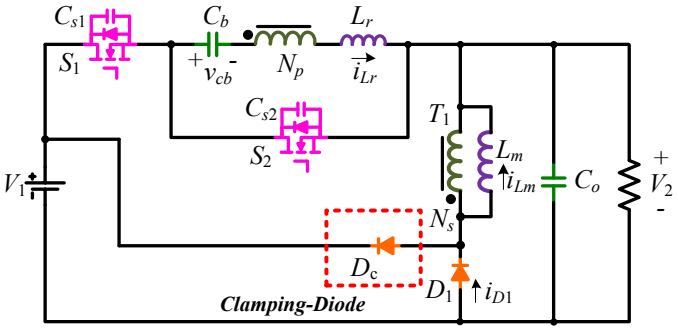
The turn-off voltage across switches S_1 and S_2 is equal to V_1-V_2 because they are in series connection between the input and the output. Thus, lower voltage stress is achieved in the steady-state. Especially, in the battery charger application with non-zero output voltage, lower voltage rating switches with lower on-resistance can be used, contributing to a reduction of cost and conduction loss.

The diode D_1 is reverse biased in the interval t_0-t_3 as shown in Fig.3 and thus the turn-off voltage across D_1 is derived in (26). The relationship between the normalized voltage stress of D_1 and voltage transfer ratio M is depicted in Fig.5(a). The turn-off voltage V_{D1} is lower than the input voltage V_1 when M with different turns ratio n satisfies in the region A. However, in practical application, higher turn-off voltage appears owing to the resonance between the leakage inductor L_r and the junction capacitor of D_1. Therefore, conventional RCD snubber is usually desired to suppress the spike voltage at the expense of increased conduction loss. A simple but effective alternative solution is illustrated in Fig.5 (b) that only one clamping-diode D_c is utilized to clamp the diode D_1 to the input. The efficiency is improved since the conduction loss of additional resistance in the RCD snubber is avoided.

$$V_{D1} = V_2 + \frac{V_1 - V_2 - V_{cb}}{n} = \frac{V_2}{D} = \frac{V_1}{n}(1 - M) \tag{26}$$



(a) The relationship between V_{D1}/V_1 and M with different turns ratio n.



(b) With clamping-diode.

Fig.5. Voltage-clamping of diode D_1.

E. *Comparison of Proposed ZVS Buck Converter and Other ZVS Buck Converters*

Comparison between the proposed ZVS buck converter and other ZVS buck converters is illustrated in TABLE I. In the proposed converter, the switch and diode voltage stresses in the steady-state are lowest. Besides, reduced magnetic component is achieved because of the additional magnetic core elimination and the reduced DC bias of inductor current. Moreover, ZVS is also realized for the auxiliary switch, which is similar

with the active-clamping ZVS converters. Therefore, the proposed converter is expected to achieve improvement on cost and power density while retaining ZVS for switches in comparison with other ZVS buck converters.

TABLE I. Comparison of proposed ZVS buck converter and other ZVS buck converters

	Voltage Stress		DC Bias of Inductor Current	Magnetizing Core	Auxiliary Switch
	Switches	Diodes			
QRC[4]	$V_1 + I_o\sqrt{L_r/C_{ds}}$	V_1	I_o	2	---
ZVT[12]	V_1	V_1	I_o	2	ZCS-on ZVS-off
Active-clamping[21]	$\frac{V_1}{1-D}$	V_1	I_o	2	ZVS
Coupled-inductor[28]	V_1	$(1+\frac{1-D}{n})V_1$	$I_o+\frac{1}{n}I_D$	1	---
Proposed Converter	$V_1 - V_2$	$\frac{V_1-V_2}{n}$	$\frac{V_1-V_2}{V_1}I_o$	1	ZVS

IV. Design Considerations

In this section, the design considerations of the proposed converter are illustrated in detail based on the analysis in Section II and III. The specifications of the prototype circuit are shown as following:

1) Input voltage V_1=156 V;

2) Output voltage V_2=48 V;

3) Maximum output power P_o=200 W;

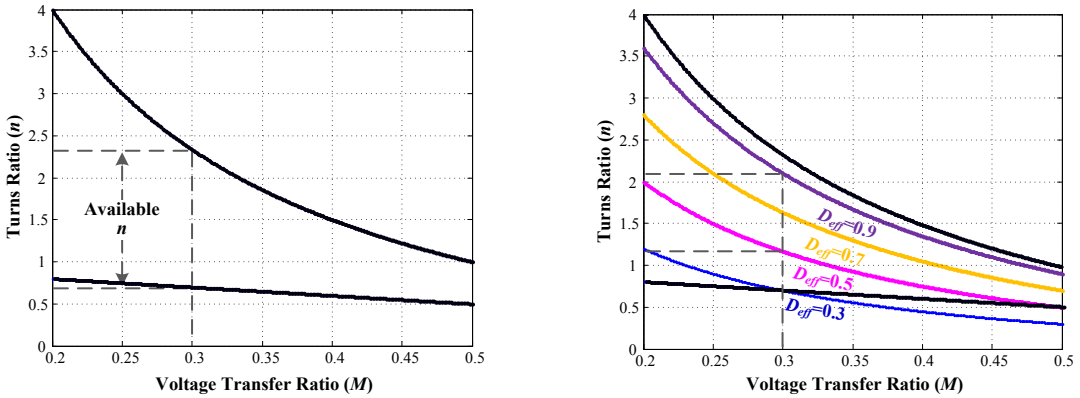
4) Switching frequency f_s=50 kHz.

A. Turns Ratio and Duty Cycle

The maximum n can be derived from (21) with the consideration that effective duty cycle D is less than 1, as shown in (27). And the minimum n is calculated in (28) to clamp the turn-off voltage of diode at the input voltage according to (26). The available range of turns ratio n with voltage transfer ratio M=0.308 is shown in Fig.6 (a). From (26), the larger n is, the lower voltage stress of diode D_1 is. However, with a larger n, the corresponding duty cycle D increases as illustrated in Fig.6 (b). Therefore, the peak diode current in (19) and the duty cycle loss in (20) are increased. Therefore, both factors should be taken into consideration to determine an appropriate value of n. In practical application, the diode D_1 is clamped to the input V_1 by the clamping diode D_c. Hence the turns ratio n is set to 0.9, which is around the minimum n to achieve low peak diode current and duty loss.

$$n = D_{eff}\left(\frac{1}{M}-1\right) < \frac{1}{M}-1 \tag{27}$$

$$n > 1-M \tag{28}$$



(a) Available range of turns ratio n. (b) Available turns ratio n with different D_{eff}.

Fig.6. Relationship between turns ratio n and voltage transfer ratio M.

After the determination of turns ratio n, the effective duty cycle D_{eff} can be derived from (21).

$$D_{eff} = \frac{n}{1/M - 1} = \frac{0.9}{1/0.308 - 1} = 0.4 \tag{29}$$

B. Magnetizing Inductance

The magnetizing inductor is charged in the interval t_0-t_1 and is discharged in the rest of a switching period, as shown in Fig.2. From (18), the magnetizing inductance is derived in (30) with the assumption that $\Delta i_{Lm} = 0.2 I_{Lm} = 0.2(I_o - I_{in})$.

$$L_m = \frac{(1 - D_{eff}) V_2 T_s}{\Delta i_{Lm}} = \frac{(1 - D_{eff}) V_2 T_s}{0.2(I_o - I_{in})} = 998 \mu H \tag{30}$$

C. Active Switches and Diodes

As discussed in Section III, the voltage stress of the main switches is V_1-V_2. Considering the output voltage V_2=0 at start-up with the resistance load, the maximum turn-off voltage $V_{ds1,max}$=$V_{ds2,max}$=V_1=156V is achieved. And the turn-off voltage of diode D_1 is clamped at the input voltage with the clamping diode D_c, thus the maximum turn-off voltage $V_{d1,max}$=$V_{Dc,max}$= V_1=156V.

The leakage current i_{Lr} flows through switches S_1-S_2 when the switch is on, as shown in Fig.2. The leakage current i_{Lr} at different time is derived in (31). Then the RMS current of the switches S_1-S_2 is approximately calculated in (32) and (33), respectively. And the average current of diode D_1 is approximately derived in (34). Since the diode D_c conducts only when the turn-off voltage of D_1 exceeds the input voltage, the current stress is very low.

From above, mosfet IRF630 (200V/5.7A@T_c=100°C) is chosen as active switches. MUR620CT (200V/6A@T_c=130°C) is chosen for the diode D_1 and SK1200 (200V/1A) operates as the clamping diode D_c.

$$\begin{cases} i_{Lr1} = \dfrac{I_{Lm} - 0.5\Delta i_{Lm}}{n}, t = t_0 \\ i_{Lr2} = \dfrac{I_{Lm} + 0.5\Delta i_{Lm}}{n}, t = t_2 \\ i_{Lr3} = \dfrac{I_{Lm} \text{-} 0.5\Delta i_{Lm} \text{-} i_{D1,peak}}{n}, t = t_4 \end{cases} \tag{31}$$

$$I_{S1,RMS} \approx \sqrt{\frac{D}{3}(i_{Lr1}^2 + i_{Lr1}i_{Lr2} + i_{Lr2}^2)} \approx 2.03A \tag{32}$$

$$I_{S2,RMS} \approx \sqrt{\frac{1\text{-}D}{3}(i_{Lr2}^2 + i_{Lr2}i_{Lr3} + i_{Lr3}^2)} \approx 3.02A \tag{33}$$

$$I_{D1,avg} = I_o - I_{in} \approx 2.89A \tag{34}$$

D. *Leakage Inductance and Blocking Capacitance*

From (22), in order to achieve the ZVS of S_1, the energy stored in the leakage inductor must be greater than that of the parasitic capacitor. Therefore, the leakage inductance has to satisfy in (35). Substituting i_{Lr3} in (31) to (35), the relationship between the ZVS region and the leakage inductance is depicted in Fig.7. In the experiment, the leakage inductance of the coupled inductor is 7.6 μH, thus the ZVS can be achieved around 15% load condition with the parasitic capacitance C_{ds}=1000pF from Fig.7.

$$L_r > \frac{C_{ds}(V_1 - V_2)^2}{i_{Lr3}^2} \tag{35}$$

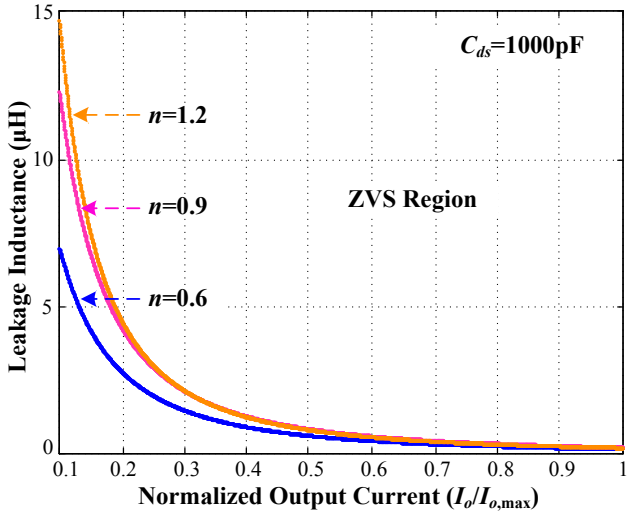


Fig.7. ZVS region of proposed converter with C_{ds}=1000pF.

From Fig.2 and Fig.3, the blocking capacitor C_b is charged by the leakage inductance current i_{Lr} in the interval t_0-t_2. The voltage increment can be obtained in (36). Then $C_b \geq 5.94\mu F$ can be derived assuming $\Delta V_{cb} = 0.01V_{cb}$. In the experiment, a 10μF capacitor is used and thus the voltage variation of blocking capacitor is small enough to be neglected.

$$\Delta V_{cb} = \frac{\int_{t_0}^{t_2} i_{Lr}(t)dt}{C_b} \approx \frac{I_{Lm} / n \times D_{eff} T_s}{C_b} \tag{36}$$

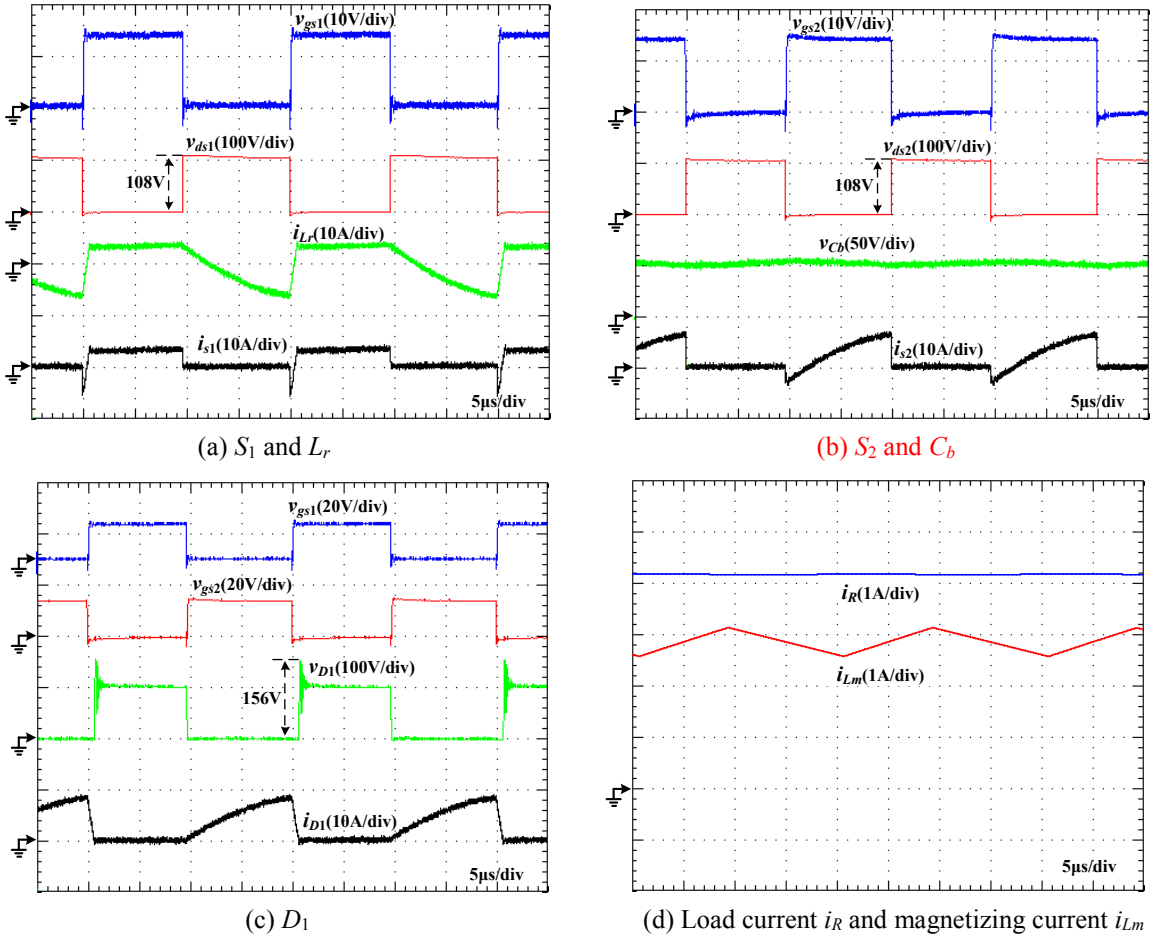
E. Summary of Design Results

From above, the design results of topology parameters are concluded in TABLE II. The simulation and experiment are implemented with the parameters to verify the correctness of the design and to validate the effectiveness of the proposed converter.

TABLE II. Topology Parameters

Parameter	Symbol	Value	Units
Turns ratio	n	0.9	
Magnetizing inductance	L_m	1000	μH
Leakage inductance	L_r	7.6	μH
Blocking capacitance	C_b	10	μF
Switches	S_1–S_2	IRF630	
Diode	D_1	MUR620CT	
Diode	D_c	SK1200	

V. Experiment and Simulation Results



(a) S_1 and L_r (b) S_2 and C_b

(c) D_1 (d) Load current i_R and magnetizing current i_{Lm}

Fig.8. Key operating waveforms of the proposed converter from experiment results (a), (b), (c) and simulation results (d).

Key operating waveforms of the proposed converter from experiment and simulation are shown in Fig.8. The experiment and simulation results coincide well with the theoretical analysis. In Fig.8(a) and Fig.8(b), the turn-off voltage of switches S_1 and S_2 is clamped at 108V, which is nearly equal to the differential voltage between the input and the output. Therefore, the voltage stress of switches is reduced to near two thirds of the input voltage in the steady state. Furthermore, with the clamping diode D_c, the peak turn-off voltage of diode D_1 shown in Fig.8(c) is equal to the input voltage. Because no additional resistance is needed, the voltage-clamping scheme is simpler and more efficient compared with conventional RCD snubber. In addition, the falling rate of the diode current is limited by the leakage inductor L_r so that the reverse-recovery characteristic is effectively improved. Since the magnetizing current can't be practically measured, Fig.8(d) demonstrates the simulation results with PSIM. It shows that the dc-bias of magnetizing current is much smaller than the load current because it is decreased to the difference between load current and average input current.

Fig.9 depicts gate-to-source voltage, drain-to-source voltage and drain-to-source current of S_1 and S_2 at 20% load condition. Before turn-on, the current i_{s1} and i_{s2} flow through the body diodes of S_1 and S_2, respectively. Therefore, both switches can achieve ZVS even under light load condition. As a result, switching loss can be drastically reduced and EMI noise is significantly alleviated.

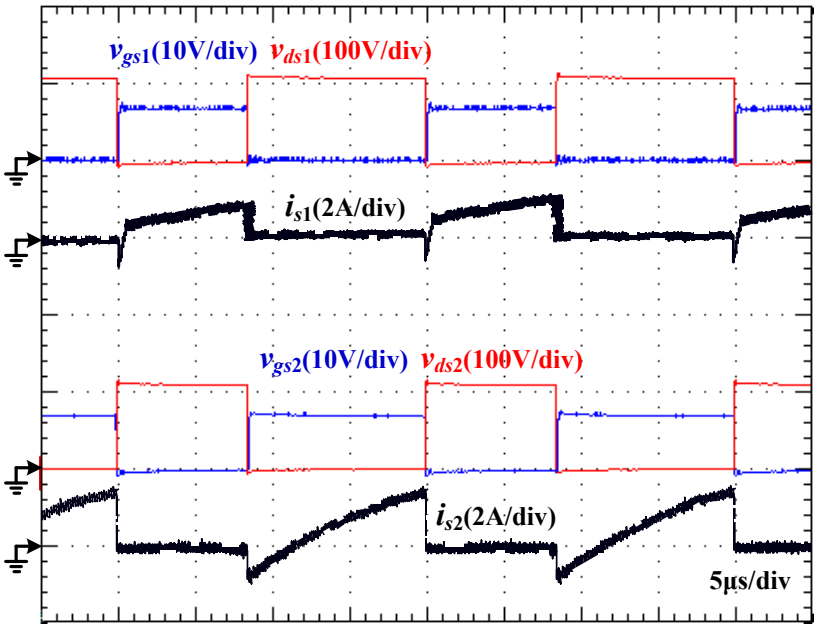
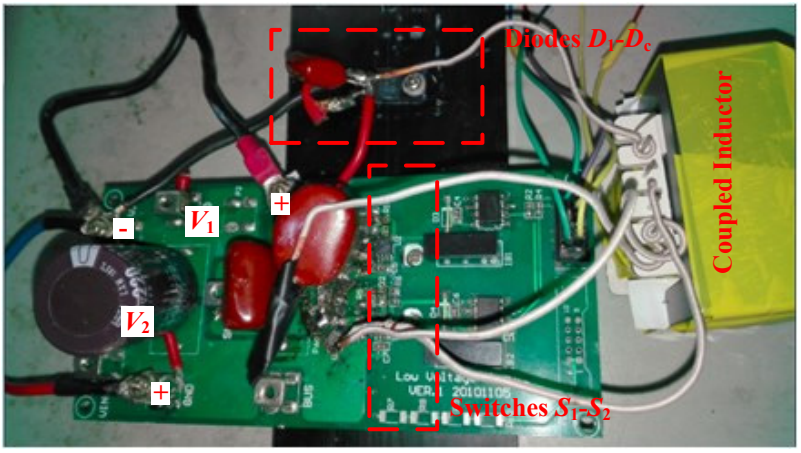
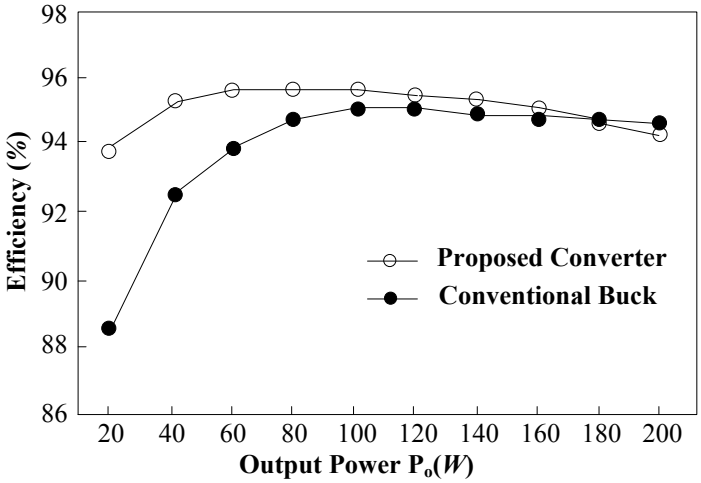


Fig.9. Experiment wavefoms of gate-to-source voltage, drain-to-source voltage and drain-to-source current of switches S_1 and S_2.

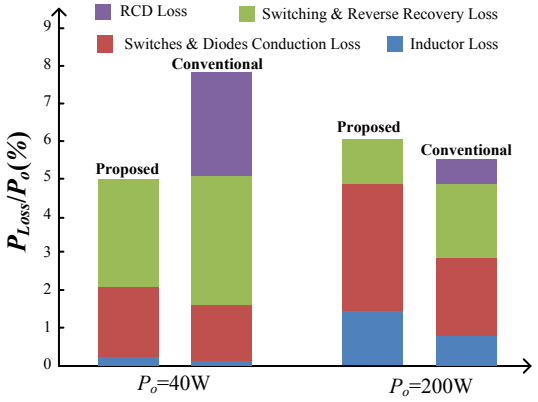
The photograph of the proposed converter is shown in Fig.10 (a) and the measured efficiency as a function of the output power is illustrated in Fig.10 (b). Owing to the merits of ZVS operation, high efficiency is achieved for the proposed converter over the whole power range. At 30% load condition, the efficiency is the highest because the ZVS is achieved while the circulating leakage inductor current is low. Therefore, both switching loss and conduction loss are low and maximum efficiency of 95.68% is achieved. The conventional buck converter with same switch, diode and switching frequency is built for comparison. It is noteworthy that additional RCD snubbers are required to suppress the spike turn-off voltage induced by the resonance between parasitic inductor and parallel capacitors of the switch and diode with the hard-switching operation. From the loss distribution depicted in Fig.10 (c), the conduction loss of the switches, diode and inductor is always higher in the proposed converter, resulting from the extra conduction loss in the auxiliary circuit. But the switching loss is lower owing to the ZVS operation. Moreover, the loss is further reduced because of the RCD snubbers elimination. At low load (e.g. P_o=40W), the conduction loss occupies a small proportion of the total loss, hence the efficiency of the proposed converter is much improved. The proportion enlarges with the increment of output power, resulting in increased loss in the proposed converter. Nevertheless, the efficiency is improved in the proposed converter at most load condition except for the full load condition, as shown in Fig.10 (b). Besides, with higher frequency, the efficiency and EMI characteristic can be further improved in comparison with the conventional buck converter owing to the ZVS operation.



(a) Photograph of the proposed converter.



(b) Measured efficiency.



(c) Loss distribution under output power P_o=40W and P_o=200W

Fig.10. Photograph, measured efficiency and loss distribution.

VI. Conclusion

In this paper, a novel ZVS buck converter is introduced. With the incorporation of filter inductor and leakage inductor into the coupled inductor, the converter has reduced magnetic component while retaining the merit of ZVS. Meanwhile, the turn-off voltage of switches is reduced to the differential voltage between the input and output in the steady-state. Therefore, easier ZVS realization are achieved for switches since the energy required to discharge the switches parallel capacitors is decreased. Then the circulating leakage inductor current can be reduced, which saves conduction loss in the auxiliary circuit. In addition, the turn-off spike voltage of the output diode is effectively clamped to the input with a single diode, which makes the proposed converter more efficient. Moreover, the leakage inductor limits the diode current decreasing rate and thus improved reverse-recovery characteristic of the diode is achieved. The feasibility and advantages of the proposed ZVS buck converter are verified by simulation and experimental results based on a 200W prototype circuit with a maximum efficiency of 95.68%.

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