Controlled Transition Full-bridge Hybrid Multilevel Converter with Chain-links of Full-bridge Cells

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Abstract—This paper proposes a controlled transition full-bridge (CTFB) hybrid multilevel converter (HMC) for medium and high voltage applications. It employs a full-bridge cell chain-link (FB-CL) between the two legs in each phase to generate multilevel bipolar output voltage. The CTFB-HMC has twice DC voltage utilization or power density of conventional converters due to the bipolar capability of its full-bridge configuration. Hence, for the same power rating and same voltage level number, its total cells per phase are quarter that in MMC, which reduces the hardware installation volume. Also, in the proposed converter, the total device number in the conduction paths is the same as in the HB-MMC, leading to low conduction losses. The FB-CL current of the CTFB converter has no DC component, which offers the potential to enhance the transient response. Comparative studies between the CTFB and other multilevel topologies are carried out to clarify its main features. The modulation strategies and parameter sizing of the proposed converter are investigated using a generic case. Simulation and experimental results are used to verify the effectiveness of the proposed approach.

Index Terms—Hybrid multilevel converter; full-bridge cell chain-link; controlled transition process; improved DC voltage utilization; low conduction losses; zero DC chain-link current.

I. INTRODUCTION

With increasing penetration of voltage source converter (VSC) techniques into high-voltage high-power applications such as machine drives, integration of large scale distributed energy source and power system control, the multilevel converter has attracted research attention due to its reduced emission of electro-magnetic interference (EMI) and improved voltage wave shaping ability compared with the two-level converter [1-9].

Amongst the various multilevel topologies, the modular multilevel converter (MMC) contributes advantages of modularity, redundancy, hardware simplification and less modulation complexity than the cascaded full-bridge converter and clamping technique based solutions including diode and flying capacitor clamped converters [6, 8, 10-14]. The basic MMC has half-bridge (HB) cells, and when extended to a full-bridge (FB) cell MMC is able to offer ride-through ability during DC voltage collapse but with doubled the power switch losses. As a compromise, the mixed cell MMC employs both kinds of cells in the arm, facilitating reverse blocking capability with lower conduction losses than the FB-MMC [15, 16].

In general, the conventional MMCs require a large number of cells to synthesize a voltage waveform with high number of voltage levels; thus, their footprints may be large due to the array of cell capacitors and power switching devices. To combine the advantages of the two-level VSC (low device number) and the MMC (less EMI and switching losses), several new topologies have evolved and are termed hybrid multilevel converters (HMCs).

The alternate arm multilevel converter (AAMC) presented in [17] employs a directing switch made up of series connected power switches in each arm to alternatively use the upper or lower full-bridge cell chain-link (FB-CL) for voltage synthesis. In this way, the number of cells can be halved compared with conventional MMCs. To ensure energy balancing of the cell capacitors, directing switch AC voltage zero-crossing commutation is utilized. This overlap region of the upper and lower arms allows energy exchange between two arms. Another method is to inject a zero-sequence current component, which offers a path for power compensation between the cell stacks and the DC-link [18].

The HMC with AC side cascaded FB cells offers an even smaller footprint with half the cell number of the AAMC by placing the chain-links of FB cells and inductance in series with the AC side load [19]. In this topology, the two-level converter is modulated by selective harmonic elimination (SHE), facilitating fundamental voltage control and improve DC-link voltage utilization; while its AC side FB-CL behaves like an active filter that attenuates low order voltage harmonics. The energy balancing of cell capacitors can be fulfilled by modulating the cells according to the reference signal, capacitor voltage sorting and phase current polarity. Practically, the FB-CL needs a small fundamental voltage to compensate for internal losses. The main shortcoming of this converter is high power losses due to the hard-switched power devices in the two-level converter stage and the increased total device number in the conduction paths.

Another topology with a HB cell based chain-link wave-shaping circuit and phase directing switches in parallel has been reported in [20]. The three phases are in series to support the full DC-link voltage.

In [21], a HMC scheme with DC side cascaded FB cells is analysed, where a FB two-level converter is used as a phase director and the FB-CL is located in the DC side for each

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phase. It is able to decouple the power flow control from the energy balancing of cell capacitors by using the bipolar voltage capability of the FB cells in the chain-link. The total required cell number for this converter is the same as the AAMC topology. However, its disadvantage of high power semiconductor losses persists, as in the AC side FB cascaded converter.

In this paper, a novel HMC topology using the controlled transition full-bridge (CTFB) configuration is proposed for medium and high voltage applications such as flexible AC transmission system (FACTS) devices. It has twice the DC utilization and a quarter the cells of the HB-MMC for the same power rating, thus high power density and small footprint are expected. The device number in the conduction path in the CTFB-HMC is equal to that in the HB-MMC and significantly less than other MMCs and HMCs; thus, conduction losses are minimized. It also has zero DC current in the chain-link, which may bring advantages over the MMC in terms of dynamic performance. The remainder of this paper is organized as follows: section II interprets the operating principles of the CTFB topology and its potential advantages; its energy balancing scheme and converter dimensioning are analysed in section III and IV; next, section V compares the proposed converter and other MMCs. The control strategy for a grid-tied three-phase CTFB-HMC is clarified in section VI; simulation and experimentation are presented in section VII and VIII to verify its feasibility as an independent VSC under various conditions. Finally, the main conclusions are summarised and highlighted in section IX.

II. Proposed Controlled Transition Full-bridge (CTFB) Hybrid Multilevel Converter (HMC)

The schematic of the single-phase CTFB-HMC is shown in Fig. 1, where the FB-CL is employed to dynamically clamp the voltage between two leg terminals "x" and "y" to synthesize a true multilevel output voltage waveform v_{xy} as shown in Fig. 2. The maximum AC side peak voltage is equal to the DC-link voltage with 2N+1 voltage levels when the FB-CL has N cells. Therefore, to generate the same voltage levels as the conventional MMC, the cell number per phase in the CTFB-HMC is a quarter and both polarities of its FB cells are utilized; besides, the DC utilization is twice of that with MMCs, AAMC and the AC side cascaded FB topologies, which indicates a higher power density and smaller footprint for the CTFB-HMC. The power switch voltage stress V_{cell} in the CTFB-HMC is expressed as (1).

$$V_{cell} = V_{dc} / N \quad (1)$$

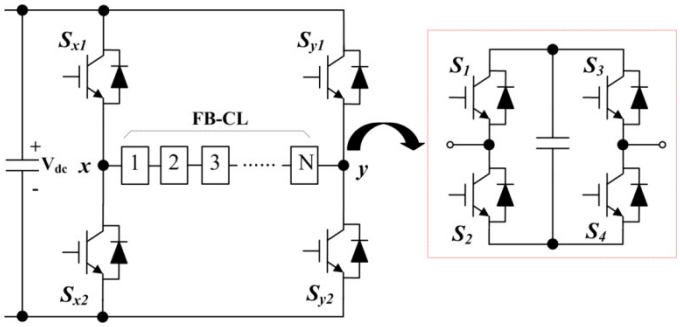


Fig. 1. The topology of single-phase CTFB-HMC and cell structure.

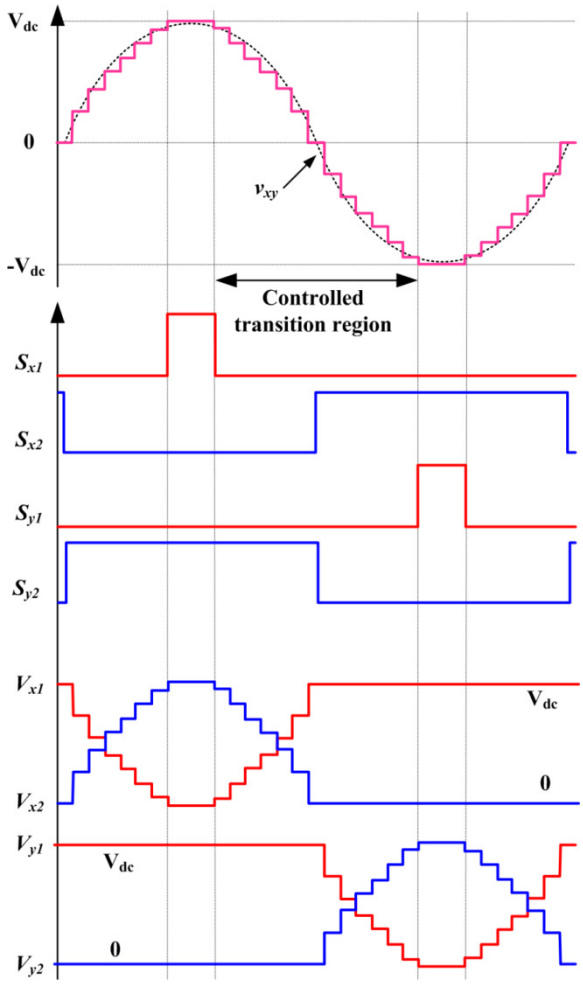


Fig. 2. Maximum synthesized multilevel voltage and key waveforms of the main directing switches for the single-phase CTFB-HMC.

A. Converter Operation Analysis

To generate a true multilevel output from the CTFB-HMC, its FB-CL should be activated to dynamically clamp the two leg terminals "x" and "y" to track the reference, while the main directing switches $\{S_{x1}, S_{x2}\}$ and $\{S_{y1}, S_{y2}\}$ are operated diagonally when the output voltage is clamped to $\pm V_{dc}$; thus allowing the energy exchange between the DC-link and FB-CL. The gate signals and sustained voltage of the main directing switches are interpreted in Fig. 2, where the transitions of S_{x1} and S_{y1} occur when there blocked voltage is equal V_{cell} in (1), thus the switching losses and dv/dt can be largely reduced. The conditions for S_{x2} and S_{y2} are further improved, since they operate at zero voltage and current condition, which means they do not create any switching losses. Also the directing switches only turn on and off at a low frequency, thus their switching losses are minimal and the low switching frequency high efficiency power switches such as the gate turn-off thyristor (GTO) and the integrated gate commutated thyristor (IGCT) become viable for the directing switches to reduce the losses. According to Fig. 2, the FB-CL is responsible for voltage synthesis during the controlled transition region, while the main directing switches are activated for rail-to-rail voltage clamping.

This time-division mode of the main directing switches and FB-CL is able to reduce the device number in the conduction paths, thus minimizing the conduction losses. As an illustration, the HB-MMC can generate the same AC voltage and power rating as the proposed converter when its dc link voltage is $2V_{dc}$ and with 2N cells in each arm (4N per phase). So the total device and conduction path device numbers for HB-MMC are 8N and 2N respectively, which are the same as for the CTFB-HMC. Alternatively, if same DC-link V_{dc} and number of cell per arm N are employed, the power rating of HB-MMC is half of that in CTFB-HMC when the same load current is assumed, and the total device and conduction path device numbers become 4N and N. This means the total conduction loss percentage of the CTFB-HMC is generally the same as that in the HB-MMC. Since HB-MMC offers lower losses than the FB-MMC, AAMC and FB cell cascaded HMCs, it is expected that the proposed CTFB-HMC is also superior in terms of efficiency [22]. In fact, from Fig. 1, the chain-link current in the CTFB converter has no DC component. This implies that dynamic response for the proposed converter is better than the HB-MMC at high power factor high modulation index conditions when the total active power increases and the DC component of the MMC arm current reaches its maximum.

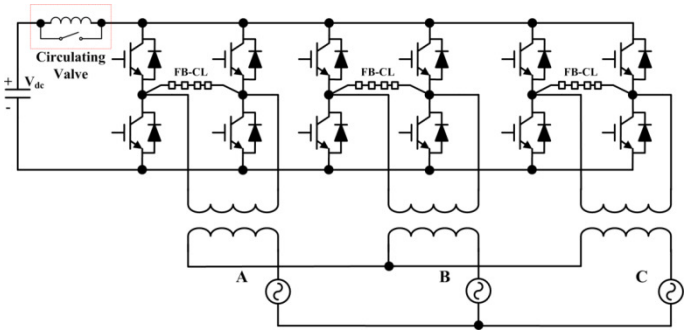


Fig. 3. Grid-tied three-phase CTFB-HMC with DC side circulating valve for current limiting.

In practise, the HMC with AC side cascaded FB cells in [19] can avoid additional arm inductance for current limiting due to the series connection of the chain-link with the load but at the expense of increasing the total conduction losses. For non-cascaded topologies, the inductance is necessary to limit the potential inrush current during energy exchange between DC-link and the cells. Also, the two-level configuration of the directing switches in the CTFB-HMC determines the discontinuous current waveform in the DC side. Therefore, a circulating valve with parallel combination of inductance and clamping switch is introduced into its DC path as in Fig. 3. The clamping switch is triggered when the energy exchange paths between the DC-link and FB-CL are cut-off. This switch could be a diode in unidirectional power flow applications such as renewable energy source integration without storage; however, to ensure the current limit function under four-quadrant operation, a bidirectional switching device is employed. The voltage stress of this device is low, leading to the negligible switching losses. To minimize the circulating losses, an IGCT with a smaller forward voltage drop is suggested. Compared to conventional MMCs with a pair of inductors in each phase, the proposed converter uses the DC side inductor and circulating device to limit the inrush current, thus reducing the overall size and weight.

B. Modulation Schemes

Since the main directing switches and FB-CL operate alternatively except during short period, the energy balancing of the cell capacitors relies on the DC-link conduction path, which means the modulation index is critical for voltage balancing realization. To overcome this constraint, the triplen components are injected to guarantee enough time for the reference signal to touch the boundaries defined by $\pm V_{dc}$. These triplen components can be neutralized in a three-phase system. The voltage reference for each phase is expressed in (2), where m is the required fundamental modulation index, ω is the fundamental angular frequency, θ_0 is the phase angle relative to the phase-locked-loop (PLL) reference system and $\omega t+\theta_0$ represents the real-time angle of the fundamental voltage. The waveform of output voltage in the converter AC side is shown in Fig. 4. For typical three-phase system in Fig. 3 with $\{0, -2/3\pi, 2/3\pi\}$ phase differences, the triplen components cannot propagate and the secondary side line-to-line voltage between phase 'A' and 'B' is calculated by (3), where n_t is the turns-ratio of the adopted interfacing transformer.

$$v_{xy} = V_{dc} \cdot m\cos(\omega t + \theta_0) - V_{dc} \cdot (m-1) \cdot \cos[3(\omega t + \theta_0)] \quad (2)$$

$$v_{AB} = \sqrt{3} n_t V_{dc} \cdot m\cos(\omega t + \theta_0 + \tfrac{1}{6}\pi) \quad (3)$$

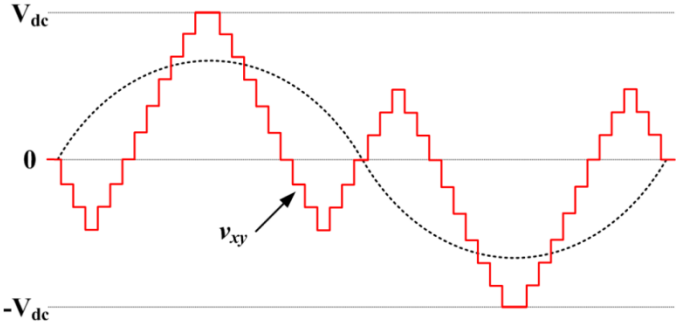


Fig. 4. AC side phase voltage waveform with triplen components injection.

With the modulation scheme in Fig. 4, the injected triplen components can guarantee the energy exchange between DC-link and the chain-link cells within short duration, which is several sampling period. In low power factor applications such as grid reactive power controller, there is theoretically zero energy exchange between the chain-link capacitors and DC-link except for the internal losses. Thus, the inrush current superposed to the directing switches is minor. However, for the cases with large amount of active power transfer, the chain-link capacitors need to exchange energy with DC-link, leading to the inrush current through directing switches and chain-link when the modulation reference reaches '±1'.

The inrush current can cause extra power losses. By extending the clamping duration of the chain-link voltage to '±1', more active power is transferred through the directing switches, thus reducing the voltage deviation of the cell capacitors. Also for fixed energy exchange, a longer period reduces the inrush current RMS. Therefore, the inrush current

power losses can be effectively limited by the clamping time increase. Such techniques are found in the literature such as trapezoidal modulation but with low order harmonic emergence [23]. To optimize the amount of low order harmonics due to the voltage clamp (saturation), multi-slope trapezoidal modulation is presented in [23, 24]. Although the maximum AC voltage can be increased with these methods, their modulation control range is limited due to the narrowed wave-shaping ability. In attempt to further reduce the low order harmonics and extend the available modulation index control range, a new triplen component injection scheme is introduced in Fig. 5.

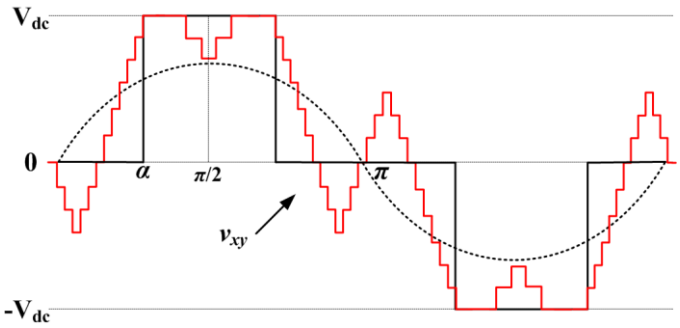
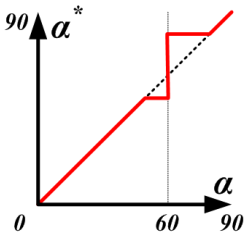


Fig. 5. Modified modulating waveform for high active power applications.

If the targeted modulation index is m (fundamental voltage is mV_{dc}), in Fig. 5, the width-variant rectangular wave can be employed to represent the equivalent fundamental voltage, where α is the angle of the rectangular waveform. Thus, (4) is obtained from its Fourier series. At $\omega t=\alpha$, the normalized fundamental voltage plus the injected triplen harmonic is set to 1pu to ensure that the equivalent modulating signal always touches 1 and -1 (which are equivalent to $+V_{dc}$ and $-V_{dc}$). As α approaches 60°, the triplen component value (3α is around 180°) asymptotes to zero (represents a point of discontinuity), making the desired amplitude of triplen injection high thus reducing the actual fundamental voltage in the clamped modulating signal. To overcome this, a dead-zone is inserted to calibrate the angle for triplen amplitude calculation as in Fig. 6.

$$m = \frac{4}{\pi}\cos\alpha, \quad \alpha \in [0^\circ, 90^\circ] \tag{4}$$



$$\alpha^* = \begin{cases} \alpha, \alpha \in [0^\circ, 50^\circ) \cup (80^\circ, 90^\circ] \\ 80^\circ, \alpha \in [60^\circ, 80^\circ] \\ 50^\circ, \alpha \in [50^\circ, 60^\circ) \end{cases}$$

Fig. 6. Modified clamping angle for triplen component injection.

Then, with α^* known (in Fig. 6) and solving (5), the amplitude of triplen injection for different m can be achieved as m_t, which is used to replace the term (m -1) in (2).

$$m\sin\alpha + m_t \sin 3\alpha^* = 1 \tag{5}$$

By applying reasonable saturation to the superposed signal, the staircase voltage waveform results are shown as in Fig. 5, which extends the AC side peak voltage beyond V_{dc} and more precisely tracks the sinusoidal waveform on the slope and peak areas than trapezoidal methods, thus reducing the lower harmonics. Although the dead zone being adopted may introduce inaccuracies at lower modulation indices, this region is only used briefly during system start-up. Otherwise, for practical reasons associated with power loss and waveform quality, the entire P-Q and Q-V envelopes of the proposed converter, when connected to grid as FACTS devices or inverters, is usually designed to be realised with modulation index above 0.8, which is beyond the imposed dead zone.

Notice that, the modulation method in Fig. 5 is recommended to be used in high active power applications, and it decreases the cell capacitor size and DC side inrush current by reducing the angle α. However, since the clamping area may have overlap period between phases if α is smaller than 60°, the inrush current limiting inductor should not be centralized in the DC-link as in Fig. 3. On the contrary, the inductor should be distributed into each phase to limit the current exchanges between phases and DC link. In this application, the modified modulation scheme extends clamping period of each phase leg, leading to significant reduction in the cyclic cell energy wane. Despite the current limiting inductor is distributed into each phase, overall footprint of the CTFB converter is expected to smaller than MMCs with two arm inductors per phase.

In summary, all voltage clamping methods can increase the power rating (DC voltage utilization) and reduce the power losses as illustrated. These attributes are achieved with the penalty of emerging low order harmonics in the AC side, which may require a relatively small tuned-filter in order to satisfy the grid code.

Since the focus of this converter is as a candidate for FACTS devices involving small amounts of active power (low power factor), the sinusoidal modulation scheme in Fig. 4 is employed here after, unless otherwise stated.

III. Cell Capacitor Voltage Balancing Algorithm

The algorithm for cell capacitor voltage balancing of the CTFB-HMC is presented in this section. During intermediate voltage levels, the FB-CL uses both polarities as well as zero-state to synthesize the AC side voltage and self-adjust the charging and discharging status of each cell capacitor according to the voltage sorting and load current polarity. When the reference reaches the DC-link, energy exchange occurs between the cell capacitors and DC-link, where the power exchange can be in either direction depending on the operational quadrant of the converter.

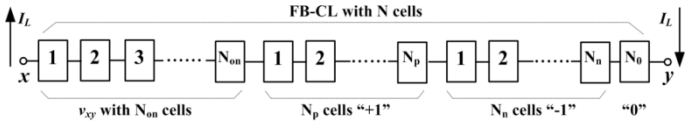


Fig. 7. Cell status distribution in the FB-CL during intermediate voltage levels.

Each CTFB-HMC phase with N cells in the FB-CL uses the reference in (2) to synthesize the multilevel voltage waveform in Fig. 4. Considering high voltage situations where the cell number N≥10, the resolution of the cell voltage in (1)

to approximate a sinusoidal waveform becomes acceptable, Thus, staircase modulation using nearest voltage levels to directly track the reference can be implemented, which avoids extra switching action and saves the switching losses compared to carrier based pulse width modulation (CB-PWM). The cell number required to generate the target voltage is calculated from (6), where the negative N_{on} represents the negative polarity of the AC side voltage. Then, the rest of the cells should produce a net zero output voltage. To better utilize these redundant switching cells for energy balancing, the strategy in Fig. 7 is adopted, where the outmost pairs of positive and negative statuses are employed to facilitate maximum energy exchange between cell capacitors. The number of positive and negative pairs is obtained from (7), and the zero-state cell number is either zero or one as shown in (8). The summation of these cell numbers in difference states is equal to N, viz., (9).

$$N_{on} = \text{round}(v_{xy} / V_{cell}) \in \{-N, N\} \quad (6)$$

$$N_p = N_n = \text{floor}[\tfrac{1}{2}(N - |N_{on}|)] \quad (7)$$

$$N_0 = \text{mod}[\tfrac{1}{2}(N - |N_{on}|)] \quad (8)$$

$$|N_{on}| + N_p + N_n + N_0 = N \quad (9)$$

Considering the load current polarity during intermediate voltage levels, the three voltage states of each FB cell are exploited to maintain the desired output voltage and achieve energy balance by adjusting the behavioural polarities of the cells in the conduction path. With proper arrangement, the cell capacitor voltage errors can be limited to a marginal range via charging or discharging processes with the AC side. When the staircase waveform approaches the peak of $\pm V_{dc}$, energy is exchanged between the FB cells and DC-link through the DC side inductor. In this way, the net active power exchange over one fundamental period for the FB-CL is compensated to zero. The generalized algorithm for cell capacitor voltage balancing of the CTFB-HMC is summarized as follows:

- At the beginning of each sampling period, the capacitor voltages of N cells are sorted in ascending order as in (10). The input data $\mathbf{V_{CN}}$ contains the sampled instantaneous cell voltage values; while $\mathbf{I_xA}$ and $\mathbf{V_cA}$ are the vectors of the index and value for each cell capacitor voltage after ascending sort.

$$[\mathbf{I_xA}, \mathbf{V_cA}] = \text{sort}(\mathbf{V_{CN}}, \text{'ascend'}) \quad (10)$$

- Based on the voltage reference value in each sampling period, the number of cells with different states $\{N_{on}, N_p, N_n, N_0\}$ are obtained from (6) to (8).
- Considering the load current polarity and the cell voltage sorting results, the capacitors with smaller values are assigned to be charged by the AC side current while the higher ones should be discharged. If $\mathbf{S_x}[N]$ is the array of switching states for all the FB cells and each element has possible values of {'+1', '-1', '0'} to identify the polarity, the generic code for cell voltage balancing can be interpreted in Fig. 8(a). An illustrative example with 11 cells per chain-link is presented in Fig. 8(b), where the numbers of cells inserted with different polarities (positive, negative and bypassed) are displayed.

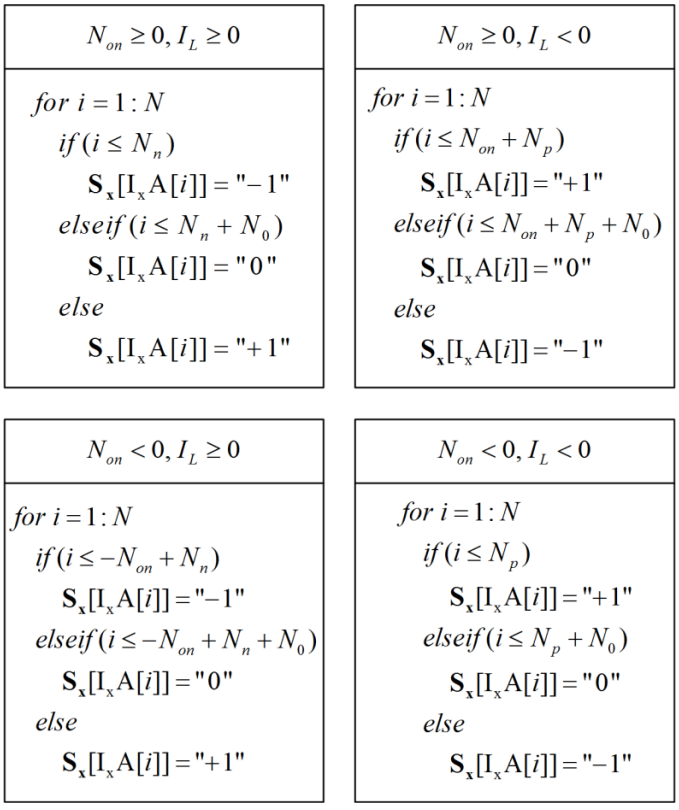


Fig. 8. The energy balancing scheme: (a) generic code for CTFB converter cell voltage balancing and (b) number of cells in each state over a fundamental period (11 cells).

IV. Converter Hardware Dimensioning

The FB-CL inserts a variable number of cell capacitors into the power path according to the predefined modulating signal. This modulating signal is derived from the voltage reference in (2). To simplify the analysis and estimation processes for the chain-link component interaction and passive device sizing, the following prioritized assumptions are made:

- Sufficient FB cells are located in the chain-link to ensure enough resolution for each cell voltage over the full AC side voltage so that a direct reference tracking method can be used for voltage synthesis.
- Sufficiently high sampling frequency is used by the controller so that the each cell status can be recognized and changed effectively; also, the reference signal in (2) is proportional to the effective duty cycle for the FB-CL.

- All internal losses due to the non-ideal parameters are neglected to establish a lossless system model.

With these assumptions and based on (2), the equivalent duty ratio of the duration when FB-CL cell capacitors are inserted into the conduction path linearly changes with the voltage reference and is calculated by (11).

$$d_{eq} = m\cos(\omega t + \theta_0) + (1-m)\cdot\cos[3(\omega t + \theta_0)] \tag{11}$$

Since in typical three-phase system, the triplen components do not contribute to the current, the AC side line current is pure fundamental and expressed in (12), where I_m is the line current amplitude and θ_1 is the phase-shift angle relative to the PLL reference. The effective current for the cell capacitor charging or discharging can be achieved by (13).

$$i_L = I_m \cos(\omega t + \theta_1) \tag{12}$$

$$\begin{aligned} i_c &= d_{eq}\cdot i_L \\ &= I_m \cdot \{m\cos(\omega t + \theta_0) + (1-m)\cos[3(\omega t + \theta_0)]\}\cdot\cos(\omega t + \theta_1) \\ &= \frac{I_m}{2}\cdot[m\cos(\theta_0 - \theta_1) + m\cos(2\omega t + \theta_0 + \theta_1) \\ &\quad + (1-m)\cos(2\omega t + 3\theta_0 - \theta_1) + (1-m)\cos(4\omega t + 3\theta_0 + \theta_1)] \end{aligned} \tag{13}$$

Consequently, the averaged voltage fluctuation of each cell capacitor is obtained by manipulation of (14), since the cell capacitors are assumed to be balanced.

$$v_c = -\frac{1}{C_{ce}/N}\int i_c dt \cdot \frac{1}{N} = -\frac{1}{C_{ce}}\int i_c dt \tag{14}$$

From (11) to (14), the expanded expression for cell capacitor voltage is shown in (15) with a constant term T_c. The function of cell capacitor voltage v_c of (15) should be discontinuous in the time-domain due to step changes of the equivalent topology at conduction instances of the main directing switches. From (11), when d_{eq}=1 or d_{eq}=-1, the instantaneous value of the FB-CL voltage v_{xy} reaches $\pm V_{dc}$ and the main switches start to conduct and transfer energy between the DC-link and FB-CL. Thus, the cell capacitor voltage values at these points are both clamped to V_{dc}/N, then, substituting these relations into (15), (16) is obtained.

$$\begin{aligned} v_c = -\frac{I_m}{2C_{ce}}[&\frac{1-m}{4\omega}\sin(4\omega t + 3\theta_0 + \theta_1) + \frac{1-m}{2\omega}\sin(2\omega t + 3\theta_0 - \theta_1) \\ &+ \frac{m}{2\omega}\sin(2\omega t + \theta_0 + \theta_1) + m\cos(\theta_0 - \theta_1)t] + T_c \end{aligned} \tag{15}$$

$$\begin{cases} \frac{V_{dc}}{N} = -\frac{I_m}{2C_{ce}}[\frac{1-3m}{4\omega}\sin(\theta_0 - \theta_1) + \frac{2k\pi - \theta_0}{\omega}m\cos(\theta_0 - \theta_1)] + T_c^+ \\ \frac{V_{dc}}{N} = -\frac{I_m}{2C_{ce}}[\frac{1-3m}{4\omega}\sin(\theta_0 - \theta_1) + \frac{(2k+1)\pi - \theta_0}{\omega}m\cos(\theta_0 - \theta_1)] + T_c^- \end{cases} \tag{16}$$

By solving for $\{T_c^+, T_c^-\}$ from (16), the final equation for v_c can be derived as (17) with definitions in (18). Expression (17) becomes continuous only at the case of θ_0=θ_1 when the AC power factor is zero and the converter exchanges zero active power with both the AC and DC sides, which is in accordance with the energy conservation law for converter operation.

$$v_c = \begin{cases} \frac{V_{dc}}{N} - \frac{I_m}{2C_{ce}}[A_W(t) + B_W(t) + C_W + \frac{\pi}{2\omega}m\cos(\theta_0 - \theta_1)] \\ \qquad (\omega t + \theta_0 \in [2k\pi, (2k+1)\pi], k \in \mathbb{Z}) \\ \frac{V_{dc}}{N} - \frac{I_m}{2C_{ce}}[A_W(t) + B_W(t) + C_W - \frac{\pi}{2\omega}m\cos(\theta_0 - \theta_1)] \\ \qquad (\omega t + \theta_0 \in [(2k+1)\pi, (2k+2)\pi], k \in \mathbb{Z}) \end{cases} \tag{17}$$

$$\begin{cases} A_W(t) = \frac{1-m}{4\omega}\sin(4\omega t + 3\theta_0 + \theta_1) + \frac{1-m}{2\omega}\sin(2\omega t + 3\theta_0 - \theta_1) \\ B_W(t) = \frac{m}{2\omega}\sin(2\omega t + \theta_0 + \theta_1) + m\cos(\theta_0 - \theta_1)t \\ C_W = -\frac{1-3m}{4\omega}\sin(\theta_0 - \theta_1) - \frac{(4k+1)\pi - 2\theta_0}{2\omega}m\cos(\theta_0 - \theta_1) \end{cases} \tag{18}$$

Based on (17), the magnitude percentage of the cell capacitor voltage ripple over its nominal DC value (V_{dc}/N) is generally determined by the DC-link voltage level (V_{dc}), number of cells in the FB-CL (N), AC side current amplitude (I_m) and the cell capacitance (C_{ce}). For CTFB converter design with known V_{dc} and I_m, N is selected according to the rated voltage of the power switching devices and the value of the C_{ce} is calculated to fulfil the demanded voltage ripple percentage. In (17), the cell capacitor voltage of CTFB converter oscillates around the nominal DC value without a fundamental frequency component for any power factor in contrast to HB-MMC.

Recall (17) and (18), the total chain-link cell capacitor voltage deviation from V_{dc} before turn-on of directing switches (at the discontinuous points) is given by (19), where τ is the radian duration in one fundamental period that the directing switches are enabled. V_{err} can be either positive or negative depending on the sign of the term $\cos(\theta_0$-$\theta_1)$ (the direction of active power flow); and its absolute value is mainly determined by the power factor and directing switch conduction period (τ, radian). In low power factor conditions, the voltage error is almost zero and minimal current is exchanged between the DC-link and cell capacitors; while at high power factors, the longer the directing switches are enabled, the smaller the voltage deviation and exchanging current are. Besides, the magnitude of V_{err} determines the rising slope of inrush current when the directing switches are turned on, and the incremental current during charging time can be estimated by (20), where L_{dc} denotes the current limiting DC side inductance. Based on this equation and the rated pulse current for the selected power semiconductor devices, an optimized value of DC side inductance can be obtained.

$$V_{err} = \frac{(\pi - \tau)NI_m}{2\omega C_{ce}}m\cos(\theta_0 - \theta_1) \tag{19}$$

$$\Delta I_{dc} = \frac{\tau\,|V_{err}|}{\omega L_{dc}} = \frac{m\tau(\pi - \tau)NI_m}{2\omega^2 L_{dc}C_{ce}}|\cos(\theta_0 - \theta_1)| \tag{20}$$

The net energy exchange from the FB-CL in the time-domain is derived and shown in (21). Based on (17), due to the incorporation of the energy exchange with DC side at

certain instances, E_{CL} over one fundamental period is zero as in (22). In further, the root-mean-square (RMS) value of E_{CL} can be calculated by (23), which represents the total energy exchange between the chain-link capacitors and the AC side when directing switches are disabled.

$$E_{CL}(t) = \int i_L \cdot v_{xy} dt = V_{dc} \int i_L \cdot d_{eq} dt = V_{dc} \int i_c dt = C_{ce} V_{dc} v_c \quad (21)$$

$$E_{CL}(t)\Big|_0^T = 0 \quad (22)$$

$$RMS[E_{CL}(t)]\Big|_0^T = 2C_{ce} V_{dc} v_c \Big|_0^{T/2} = \frac{(\pi - \tau) m V_{dc} I_m |\cos(\theta_0 - \theta_1)|}{\omega} \quad (23)$$

V. Performance Analysis of the CTFB-HMC

The operating principle, energy balancing algorithm and main element sizing of the CTFB-HMC have been discussed in previous sections. To reveal certain aspects of its behaviour, a comparative study which involves the CTFB-HMC as well as typical MMC and HMC topologies is presented at first.

On the assumption of fixed apparent power, fixed AC side voltage (thus, same line current) and same type of power switching devices (voltage and current ratings) for each candidate, the converters including CTFB-HMC, HB-MMC, FB-MMC, AAMC are investigated in Table 1, where the number of devices in the conduction path carrying per unit current reflects the percentage of conduction losses. Based on Table 1, following summary can be made:

- Compared to conventional HB-MMC, the proposed CTFB topology requires half DC-link voltage per unit power (thus, doubled power density); also, it uses a quarter number of cell capacitors (smaller footprint) to synthesize same number of voltage levels on AC side without discount in efficiency.
- Similar conclusions hold between the CTFB-HMC and FB-MMC except that the latter employs twice the number of total device for reverse-blocking ability but at the expense of doubled conduction losses.
- The proposed CTFB-HMC also contributes lower conduction losses, doubled power density and fewer cell number than the AAMC.
- The main limitation of the CTFB-HMC (as with the HB-MMC) is the lack of reverse-blocking capability compared with other converters such as FB-MMC and AAMC. However, this is not critical for the applications where there is no long distance DC cable such as FACTS devices.

A. Conduction Losses of CTFB-HMC

To quantitatively show the efficiency performance for the proposed converter, its loss calculation is exploited. Assuming the insulated gate bipolar transistor (IGBT) modules are used to build each converter, the total on-state losses are the summation of IGBT and diode losses. The forward voltage drop of IGBT and its anti-parallel diode are calculated from (24), where $\{V_{CE}, V_D\}$ are the voltage drop in conduction mode; $\{I_C, I_D\}$ are the instantaneous value of the device current; $\{V_{CEO}, V_{DO}\}$ represent the device threshold voltages; $\{R_V, R_D\}$ define the equivalent resistances for IGBT and diode respectively, and can be further obtained by (25) according to the nominal device operation points $\{V_{CEN}, I_{CN}\}$ and $\{V_{DN}, I_{DN}\}$ from the manufacturer datasheet [25, 26].

$$\begin{cases} V_{CE} = R_V \cdot I_C + V_{CEO} \\ V_D = R_D \cdot I_D + V_{DO} \end{cases} \quad (24)$$

$$\begin{cases} R_V = \dfrac{V_{CEN} - V_{CEO}}{I_{CN}} \\ R_D = \dfrac{V_{DN} - V_{DO}}{I_{DN}} \end{cases} \quad (25)$$

For the proposed CTFB-HMC, the FB cells are utilized to generate bipolar voltage. Thus, although the total amount of device in conduction path is constant, the number of IGBTs or diodes that are used to carry current becomes continuously time-variant according to the modulation reference. Since the line current is pure fundamental in the three-phase CTFB-HMC, the injected 3rd order modulating signal has marginal influence on the conduction losses. Therefore, with the AC side current defined in (12), (26) represents the effective fundamental reference signal for the proposed CTFB-HMC. Recall its voltage balancing strategy in Fig. 8, during the half cycle with positive chain-link current, the numbers of on-state IGBT and diode are calculated by the first and second equations in (27) respectively, where the total number of devices in conduction path per phase is F_{con}=2N in Table 1. Considering the symmetrical operation between the two half cycles with different current polarities, the conduction losses

Table 1. Comparisons between CTFB-HMC and other typical multilevel converters.

The same power, AC side voltage/current and same type power switches for each candidate						
Converter type	DC-link required	Cell number per phase	Voltage level number	Total devices per phase	On-state devices per phase (1p.u. current)	Efficiency
CTFB-HMC	V_{dc}	N	2N+1	8N	2N	High
HB-MMC	$2V_{dc}$	4N	2N+1	8N	2N	High
FB-MMC	$2V_{dc}$	4N	2N+1	16N	4N	Low
AAMC	$2V_{dc}$	2N	2N+1	10N	3N	Moderate

of IGBT and diode created by the energy exchange between DC and AC sides in one phase of the CTFB topology can be achieved by (28), and in further to be (29).

$$M_{eq} = m\cos(\omega t + \theta_0) \tag{26}$$

$$\begin{cases} n_T = \tfrac{1}{2}(1 + M_{eq}) \cdot F_{con} \\ n_D = \tfrac{1}{2}(1 - M_{eq}) \cdot F_{con} \end{cases} \tag{27}$$

$$\begin{cases} P_{IGBT} = 2 \times \dfrac{1}{2\pi} \displaystyle\int_{-\theta_1 - \pi/2}^{-\theta_1 + \pi/2} (R_V \cdot i_L + V_{CEO}) i_L n_T \, d\omega t \\ P_D = 2 \times \dfrac{1}{2\pi} \displaystyle\int_{-\theta_1 - \pi/2}^{-\theta_1 + \pi/2} (R_D \cdot i_L + V_{DO}) i_L n_D \, d\omega t \end{cases} \tag{28}$$

$$\begin{cases} P_{IGBT} = \dfrac{I_m F_{con}}{12\pi} [3\pi R_V \cdot I_m + 12 V_{CEO} + (8 R_V \cdot I_m + 3\pi V_{CEO}) m\cos\varphi] \\ P_D = \dfrac{I_m F_{con}}{12\pi} [3\pi R_D \cdot I_m + 12 V_{DO} - (8 R_D \cdot I_m + 3\pi V_{DO}) m\cos\varphi] \end{cases} \tag{29}$$

Provided the power factor is not zero, the cell voltage will deviate from the rated value, causing energy exchange between the DC-link and the chain-link capacitors. Due to the use of the DC side inductor, the current from the DC-link can be assumed constant during the directing switch enabled period ($T_\Delta = \tau/\omega$). For energy balance, (30) is fulfilled; and from (19), is simplified to (31). Then, the power path conduction losses for energy exchange between the DC-link and the chain-link in one phase can be estimated by (32), where it is concluded that:

- In low power factor conditions, P_{ex} is small due to the marginal voltage errors between the DC-link and the chain-link capacitors.
- In high power factor conditions, the directing switch increased enable-time (through the modulation method in Fig. 5) reduces power losses due to the reduced voltage error and DC side RMS current.

$$\frac{1}{2}\frac{C_{ce}}{N}[{V_{dc}}^2 - (V_{dc} - V_{err})^2] \approx I_{dc}(V_{dc} - \tfrac{1}{2}V_{err})T_\Delta \tag{30}$$

$$\begin{cases} I_{dc} T_\Delta = \dfrac{V_{err} C_{ce}}{N} = \dfrac{(\pi - \tau) I_m}{2\omega} m\cos(\theta_0 - \theta_1) \\ I_{dc} = \dfrac{(\pi - \tau) I_m}{2\tau} m\cos(\theta_0 - \theta_1) \end{cases} \tag{31}$$

$$P_{ex} = \frac{\omega}{\pi} F_{con} |I_{dc}| T_\Delta [(R_V \cdot |I_{dc}| + V_{CEO}) + (R_D \cdot |I_{dc}| + V_{DO})] \tag{32}$$

Therefore, the unified expression for the CTFB-HMC per phase conduction losses under arbitrary power factor and modulation scheme is obtained using (33). A case study using 4.5kV IGBT T1800GB45A for the CTFB-HMC is shown in Table 2.

$$P_{con} = P_{IGBT} + P_D + P_{ex} \tag{33}$$

As explained above, the proposed CTFB-HMC topology has virtually the same efficiency performance as HB-MMC for low power factor applications such as the FACTS devices by evaluation the number of devices in conduction path. Also, in the proposed converter, the chain-link current is pure AC component, which differs from that in HB-MMC.

Table 2. The case study of conduction losses for CTFB-HMC

Three-phase apparent power rating 57MVA and AC voltage 25kV (line-to-line RMS), N=11, V_{dc}=25kV.			
Converter Type	Three-phase total conduction losses		
	P=50MW, Q=0	P=0, Q=50MVA	P=50MW, Q=25MVAr (lagging)
CTFB-HMC	0.39MW (0.78%)*	0.26MW (0.52%)	0.43MW (0.86%)*

* Data is achieved with modified triplen injection modulation in Fig. 5 for active power transfer.

B. Switching Losses of CTFB-HMC

In this analysis, both the chain-link device and directing switches are considered. However, it is noticed that the directing switches operate with very low switching frequency and dv/dt (as in Fig. 2) using both modulation methods in Fig. 4 and Fig. 5. Thus, the switching losses of the directing switches are ignorable. This implies that the directing switches of the proposed CTFB converter can be implemented by GTO or IGCT in engineering practise; which means the conduction losses in Table 2 can be significantly decreased, especially for high power factor conditions with more occupation of the directing switches [24]. In order to keep the simplicity, the same IGBT is assumed for loss analysis throughout this paper.

The switching losses of the proposed converter can be calculated using the real-time method in [25, 26]. By recording the switching instance current for each device on-line, the IGBT turn-on/off energy and the diode reverse-recovery energy are obtained using curve-fitting or look-up table methods as in (34), where a_1-a_2, b_1-b_3 and c_1-c_3 are the fitted polynomial coefficients based on the device datasheet from manufacturer. Then, by accumulating the total switching energy for all semiconductor devices during one fundamental period, the average converter switching power losses can be achieved.

$$\begin{cases} E_{on}(I_C) = \dfrac{V_{CE}}{V_{CEN}} (a_1 \cdot {I_C}^2 + b_1 \cdot I_C + c_1) \\ E_{off}(I_C) = \dfrac{V_{CE}}{V_{CEN}} (a_2 \cdot {I_C}^2 + b_2 \cdot I_C + c_2) \\ E_{rev}(I_D) = \dfrac{V_D}{V_{DN}} (b_3 \cdot I_D + c_3) \end{cases} \tag{34}$$

Table 3. The case study of switching losses for CTFB-HMC

Three-phase apparent power rating 57MVA and AC voltage 25kV (line-to-line RMS), N=11, V_{dc}=25kV.			
Converter Type	Three-phase total switching losses		
	P=50MW, Q=0	P=0, Q=50MVA	P=50MW, Q=25MVAr (lagging)
CTFB-HMC	0.14MW (0.28%)*	0.19MW (0.37%)	0.16MW (0.31%)*

* Data is achieved with modified triplen injection modulation in Fig. 5 for active power transfer.

A case study with 4.5kV IGBT T1800GB45A for the proposed converter is shown in Table 3. In low power factor conditions, the switching losses are 50% of the total converter losses; while in high power factor, 30% of the semiconductor losses are contributed by the switching losses. This is in accordance with the engineering experience for high power multilevel converters as in [27].

C. Conduction Losses Comparison

Since the HMC directing switches usually operate at low frequency with multi-step voltage transitions, the switching losses for multilevel converters are much smaller than conduction losses [27, 28]. Therefore, the conduction losses are adopted for power efficiency comparison and all harmonic components in the arm current are neglected.

Table 4. Total conduction losses comparison between CTFB-HMC and other typical multilevel converter topologies.

Three-phase apparent power rating 57MVA and AC voltage 25kV (line-to-line RMS), N=11, V_{dc}=25kV.			
Converter Type	Three-phase total conduction losses		
	P=50MW, Q=0	P=0, Q=50MVA	P=50MW, Q=25MVAr (lagging)
CTFB-HMC	0.39MW (0.78%)*	0.26MW (0.52%)	0.43MW (0.86%)*
HB-MMC	0.22MW (0.45%)	0.20MW (0.39%)	0.24MW (0.47%)
FB-MMC	0.45MW (0.90%)	0.39MW (0.78%)	0.47MW (0.95%)
AAMC	0.37MW (0.74%)	0.37MW (0.74%)	0.40MW (0.80%)

* Data is achieved with modified triplen injection modulation in Fig. 5 for active power transfer.

Using (29) to (33) and the method in [29] for MMC and AAMC, based on the 4.5kV IGBT T1800GB45A parameters, the calculated conduction losses for HB-MMC, FB-MMC, AAMC and CTFB-HMC are summarized in Table 4. These results assume a 57.3MVA three-phase power rating and a line-to-line RMS 25kV AC side for all the converters; thus, the DC link voltage of the proposed CTFB converter V_{dc} is set to 25kV and N equals 11 with a maximum voltage stress of 2.25kV (50% of full rating) for the employed IGBT. This means the other converters must use a 50kV DC-link voltage and 4N=44 cells in each phase (22 per arm) to transfer the same power, as explained in Table 1. From Table 4, for low power factor conditions, the proposed converter has a similar efficiency performance as the HB-MMC with sinusoidal modulation. But for high power factor applications, with the modified modulation scheme in Fig. 5, the efficiency of the CTFB-HMC is virtually the same as the AAMC. As is mentioned above, in the proposed CTFB converter, GTO or IGCT can be employed for the directing switches to significantly reduce the conduction losses, especially in high active power applications. The FB-MMC has the highest on-state losses due to a higher number of power devices in the conduction paths.

VI. Control System Design

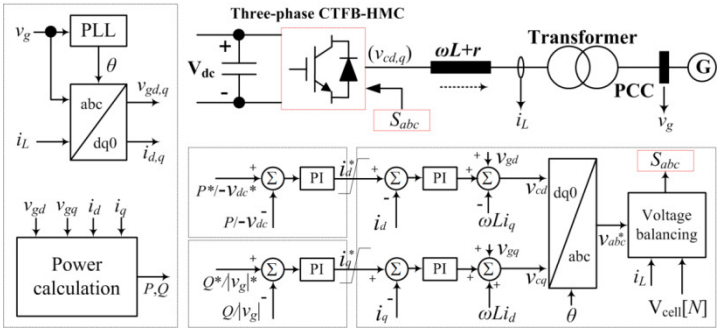


Fig. 9. The control strategy for grid-connected three-phase CTFB-HMC in d-q frame.

The d-q frame control diagram of the proposed three-phase CTFB-HMC under grid-tied mode is summarized in Fig. 9. With this synchronous-reference-frame (SRF) method, the critical variables become time-invariant. Therefore, the basic proportional-integral (PI) controller is sufficient for zero-steady-state reference tracking.

If $v_{cd,q}$ represents the output pole voltage of the CTFB converter, its d-q frame AC side differential equations are obtained in (35), where i_{dq} is the AC side line current; $v_{gd,q}$ is the voltage at the point-of-common-coupling (PCC); L and r represent the parameters of interfacing reactor.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = -\frac{r}{L}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega\begin{bmatrix} i_q \\ -i_d \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{35}$$

The reference signal for converter output voltage is set according to (36), where $\gamma_{d,q}$ is the output of the inner layer current PI controller. With the voltage and current polarity defined in Fig. 9, the outer layer controllers that are used to generate the reference signals for i_d and i_q can be expressed by (37) and (38) respectively.

$$\begin{cases} v_{cd}^* = \gamma_d + v_{gd} - \omega L i_q \\ v_{cq}^* = \gamma_q + v_{gq} + \omega L i_d \end{cases} \tag{36}$$

$$\begin{aligned} & i_d^* = -[k_{dcp}(v_{dc}^* - v_{dc}) + k_{dci}\int (v_{dc}^* - v_{dc})dt] \\ \text{or} \quad & i_d^* = k_{Pp}(P^* - P) + k_{Pi}\int (P^* - P)dt \end{aligned} \tag{37}$$

$$\begin{aligned} & i_q^* = k_{acp}(|v_g^*| - |v_g|) + k_{aci}\int (|v_g^*| - |v_g|)dt \\ \text{or} \quad & i_q^* = k_{Qp}(Q^* - Q) + k_{Qi}\int (Q^* - Q)dt \end{aligned} \tag{38}$$

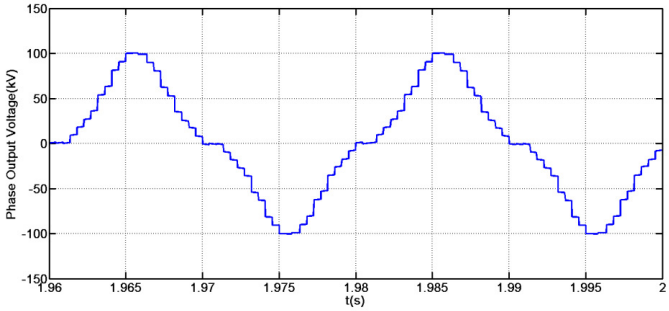
For the current controller, DC voltage controller and active power controller designs, the PI parameters can be arranged by state space analysis that incorporates the local converter feedback and feedforward. In reality, due to the uncertainty and randomness of some grid parameters, the tuning process of reactive power and PCC voltage PI controllers are usually achieved by the trial-and-error indexing method to find the proper gain combinations for the best time domain response.

VII. Simulation Analysis

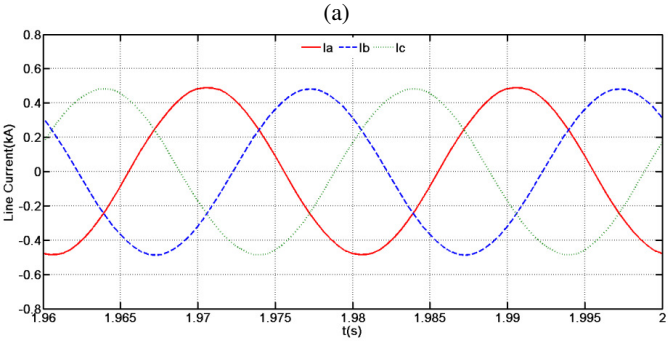
A. CTFB-HMC with 11 Cells in Staircase Mode

A three-phase CTFB-HMC with 11 cells in the chain-link and staircase modulation is tested in Matlab/Simulink with following specifications: DC-link voltage: 100kV; operational power: 60MVA, cell capacitance: 2.2mF; current limiting inductance: 10mH; modulation index: 0.82.

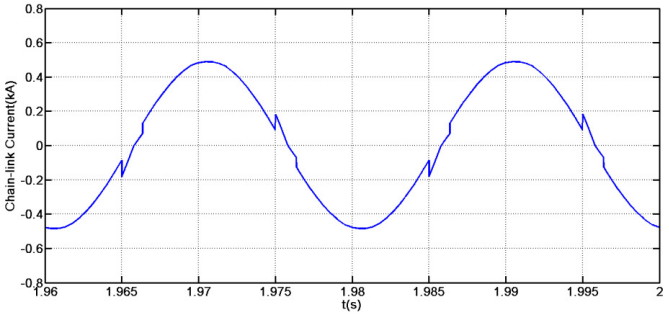
If the power factor is set to about zero and the sinusoidal modulation in Fig. 4 is employed, the phase output voltage and line current quality are shown in Fig. 10(a) and (b). The inrush current in this condition is near zero since the active power exchange is minimal, see Fig. 10(c). Thus, from Fig. 10(d), the cell capacitor voltage ripple is also decreased. In low power factor conditions, the DC side current is insignificant relative to the AC side current; and the three-phase centralized DC side inductor and circulating current waveforms are shown in Fig. 10(e). In the proposed CTFB topology, the DC inductor is located in the DC side and shared by multiple phases, which reduces the total weight and cost compared to conventional MMCs.



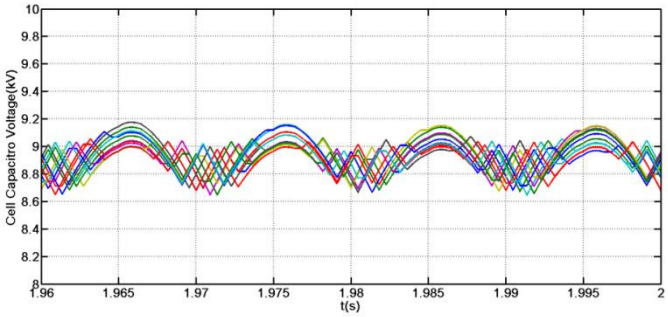
(a)



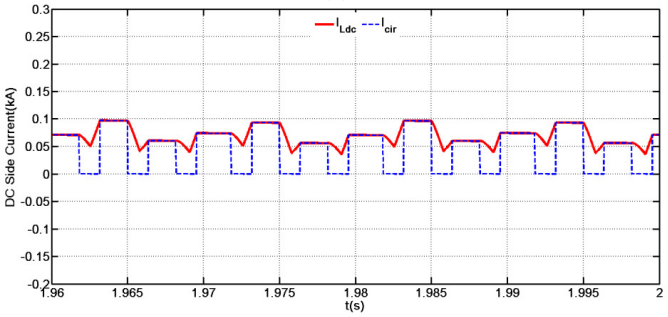
(b)



(c)



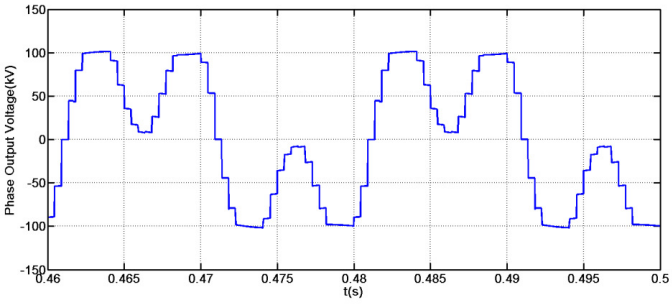
(d)



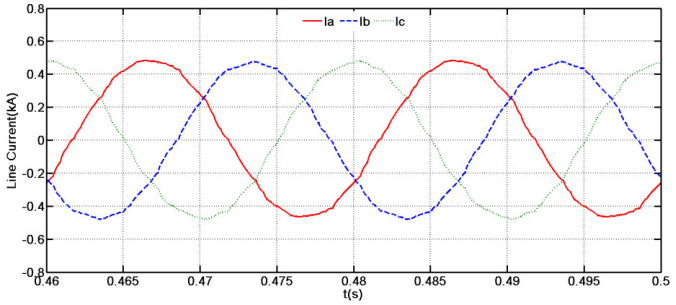
(e)

Fig. 10. Waveforms under zero power factor: (a) converter phase 'a' output voltage with triplen component; (b) three-phase line current in fundamental frequency; (c) chain-link current of phase 'a'; (d) cell capacitor voltage balancing results; (e) DC side inductor and circulating device current.

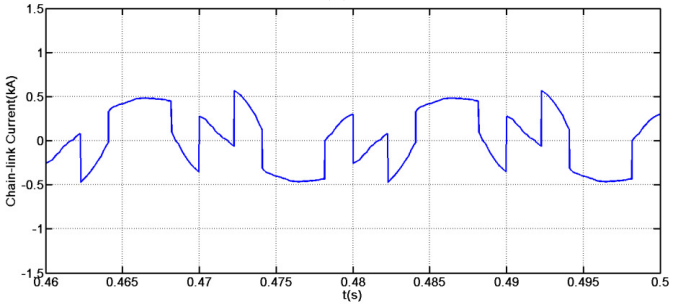
For high power factor conditions, the energy exchange time between the chain-link and the DC-link is short and concentrated in the voltage peak area if the modulation scheme of Fig. 4 is used. This effect increases the power losses and requires large DC side inductance to limit any inrush current in each phase. As in Fig. 5, the modified triplen injection modulation is assessed in another simulation. By extending the voltage level clamping duration and decentralize the inductance into the DC input of each phase, the cell capacitor voltage deviation and inrush current can both be well limited as in Fig. 11(c) and (d). With the modulation in Fig. 5, a small amount of low order harmonics emerge in the phase voltage waveform of Fig. 11(a) [23, 24]. In this simulation, a tuned-filter for the 7^{th} order harmonic is used to limit the current distortion, where the total harmonic distortion (THD) of line current in Fig. 11(b) is 2.1%. To further improve the power quality, a double-tuned filter with minimal reactive power consumption can be investigated [30, 31]. The DC side inductor and circulating current waveforms for phase 'a' is demonstrated in Fig. 11(e).



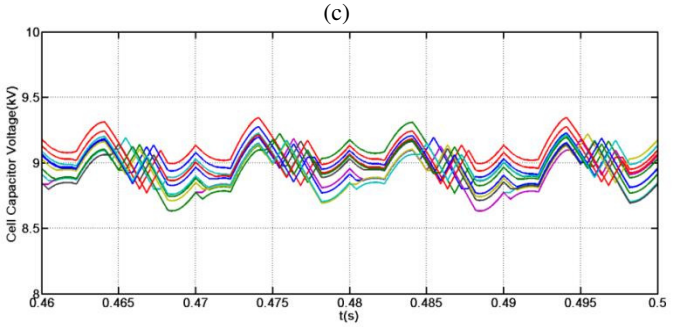
(a)



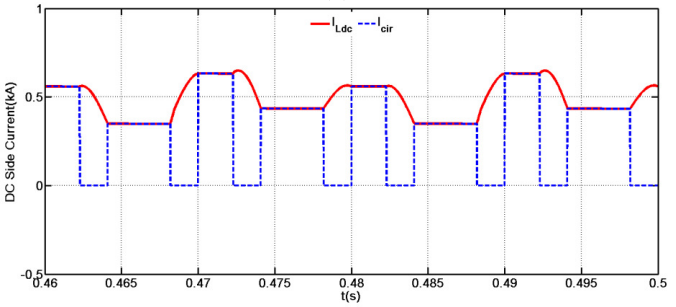
(b)



(c)



(d)



(e)

Fig. 11. Waveforms for unity power factor with modified triplen injection modulation: (a) converter phase 'a' output voltage with triplen component; (b) three-phase line current in fundamental frequency; (c) chain-link current of phase 'a'; (d) cell capacitor voltage; (e) DC side inductor and circulating device current.

From these two cases that cover the full power factor variation range, it is concluded that, with proper modulation schemes, the proposed CTFB-HMC is able to maintain energy balance of its cell capacitors, while synthesizing the desired voltage under various operational conditions.

B. Operation of CTFB-HMC based STATCOM

The grid-connected CTFB-HMC model with 3 FB cells using PWM method is built and tested in Matlab/Simulink to demonstrate two aspects:

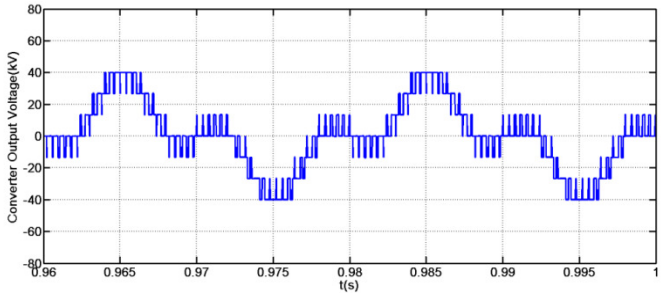
- For a small number of cells per chain-link, operation in PWM mode is able to achieve high quality output voltage with a modest increase on the average switching frequency for each device.
- The proposed converter is suitable for FACTS devices and its control strategy in Fig. 9 is verified with typical STATCOM operation.

Table 5. Specifications of CTFB-HMC model as STATCOM.

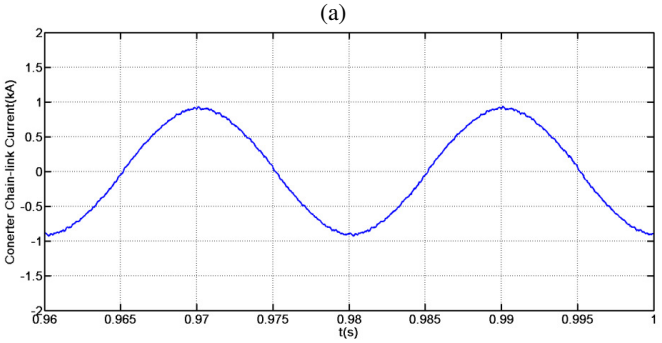
CTFB-HMC with 3 cells per phase	
Apparent power rating S_{con}	60MVA
DC link voltage V_{dc}	40kV
DC link capacitor C_d	470μF
Cell capacitor C_{cell}	2000μF
DC centralized inductor	3.3mH
Shunt inductor L_{sh}	12mH
Converter switching frequency f_{sw}	2.5kHz
Three-phase independent shunt transformer	
Power capacity	60MVA
Voltage ratio	63.5kV/21.2kV
Per unit impedance	(0.002+j0.03)
Grid parameters for shunt compensation	
Nominal line-to-line voltage	110kV(RMS)
Short-circuit power rating	2GVA
X/R ratio	20

The parameters for the tested CTFB converter, interfacing transformer and the grid are listed in Table 5.

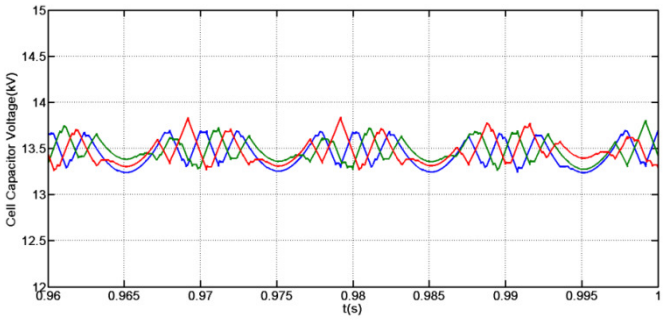
Waveforms of the CTFB-HMC with PWM mode are presented in Fig. 12, where the converter phase synthesized voltage with triplen components and chain-link current are shown by Fig. 12(a) and (b) respectively. The inrush current in the chain-link is minor due to the low power factor in typical STATCOM. Fig. 12(c) is the cell capacitor voltage balancing results under PWM operation.



(a)



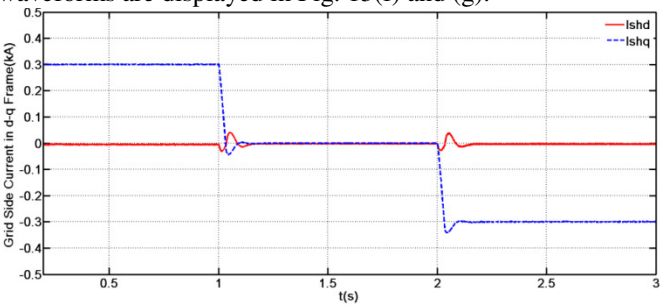
(b)



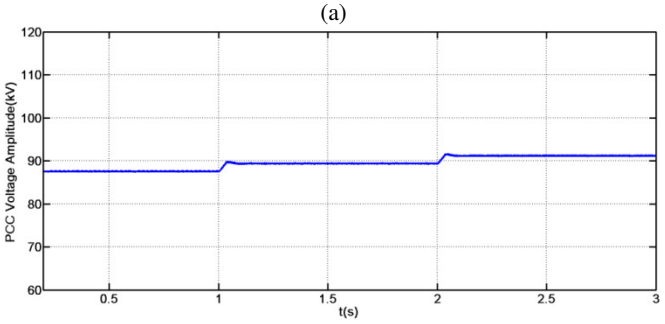
(c)

Fig. 12. Waveforms of the PWM mode CTFB converter: (a) converter phase voltage with triplen component; (b) converter chain-link current; (c) cell capacitor voltage.

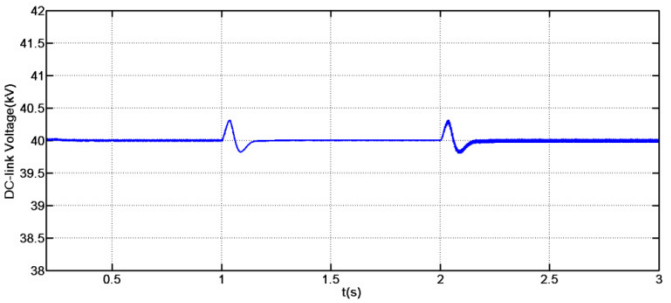
As illustrated in Fig. 9, the direct axes controller is employed to maintain the DC-link voltage in this illustration, while the quadrature controller regulates the reactive power exchange with the grid. With the reference command shift, in Fig. 13(a), the grid side quadrature current i_q is controlled to step from +300A to 0 at t=1s and then to -300A at t=2s. Correspondingly, the reactive power exchanged with the grid will increase, leading to a noticeable change in the PCC phase voltage magnitude as shown in Fig. 13(b). Then, Fig. 13(c) and (d) manifest the DC-link voltage and converter side current responses with the modulation index self-adjustment in Fig. 13(e) for the CTFB converter, where it is observed that the proposed converter can easily achieve a symmetrical reactive power rating without exhausting its linear modulation range. This is because the CTFB topology is able to double the DC-link utilization of other three-phase three-leg solutions. In further, the zoomed-in PCC voltage and shunt current waveforms are displayed in Fig. 13(f) and (g).



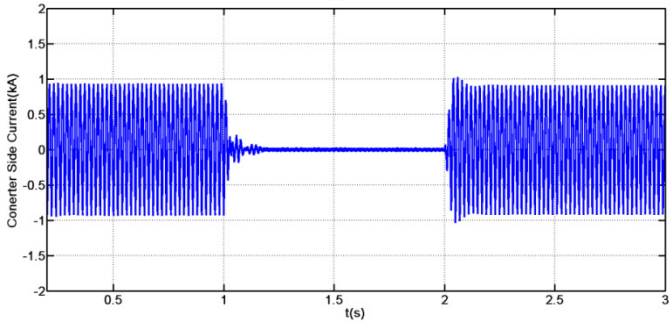
(a)



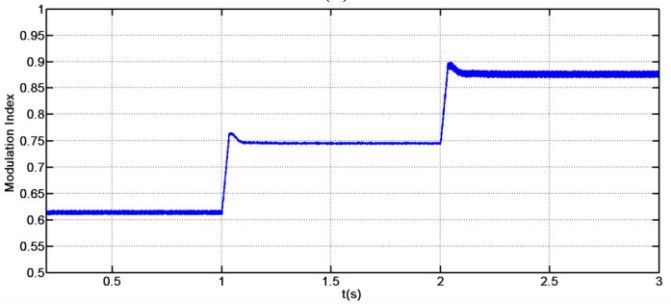
(b)



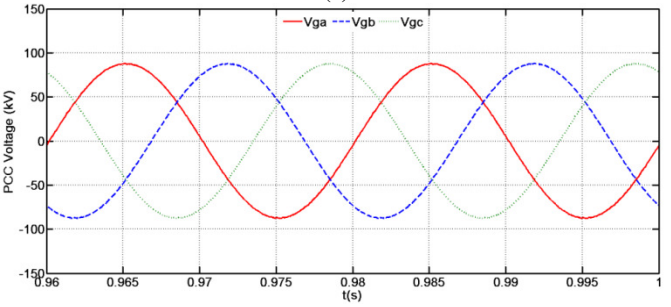
(c)



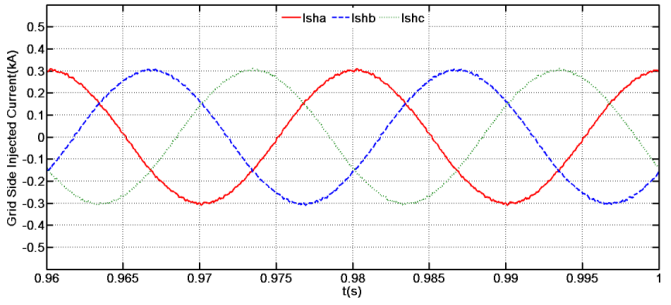
(d)



(e)



(f)



(g)

Fig. 13. Transient processes for three-phase CTFB-HMC based STATCOM: (a) grid side shunt current in d-q frame; (b) PCC voltage amplitude; (c) DC-link voltage response; (d) converter side current transient response; (e) modulation index self-adjustment of the CTFB converter; (f) PCC phase voltage; (g) grid side shunt current.

VIII. EXPERIMENTAL VERIFICATION

The single-phase CTFB-HMC converter with three cells in the chain-link is tested under standalone operation as in Fig. 14. Since the number of cells is limited, conventional CB-PWM method is used for voltage synthesis in this experiment. Due to the unidirectional DC side current, the circulating valve for chain-link current limit is implemented by the parallel combination of an inductor and diode. Also, in order to imitate the three-phase CTFB converter from a single-phase bridge operation, a third order harmonic trap is installed in the AC side to remove the triplen current component from load current. The harmonic trap consists of an inductor in parallel with a capacitor, and the overall impedance seen by the 3rd harmonic voltage component is infinite with proper tuning of the passive element parameters [32]. In this way, the line current will contain no 3rd order harmonic current as in the typical three-phase system case.

The detailed converter specifications for this prototype are as follows: nominal power rating: 1kVA; DC-link voltage: 200V; DC-link capacitance: 470μF; FB cell capacitance: 2200μF; DC side circulating valve: 3.3mH inductor and diode; AC side L-C filter: 10mH inductor and 33μF capacitance; third order harmonic trap: 10mH inductance and 110μF capacitance. To realize the modulation scheme in Fig. 4 as well as the cell capacitor voltage balancing algorithm in Fig. 8, the Infineon DSP Tricore TC1796 is employed as the controller in Fig. 14 to generate the IGBT switching signals.

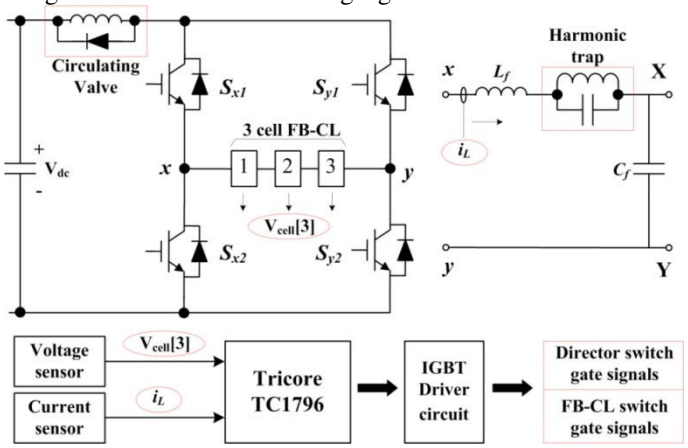
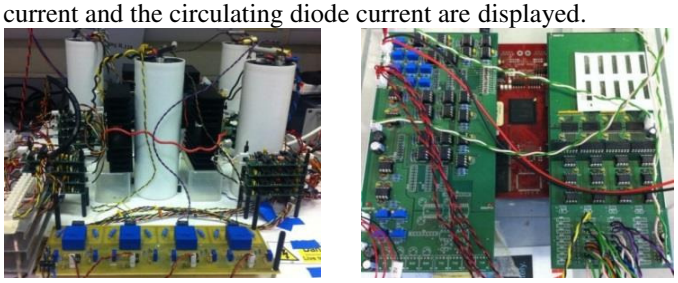


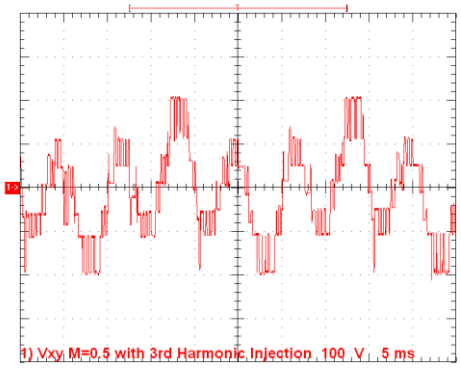
Fig. 14. The experiment setup of single-phase 3 cells CTFB-HMC with harmonic trap.

The hardware installation photograph is in Fig. 15. In order to overcome the energy balancing constraint for the CTFB-HMC with low modulation index, the triplen component signal is inserted as illustrated in (11). If the required modulation index is set to be 0.5, the multilevel output voltage across the FB-CL in this case is shown in Fig. 16(a), and the line current is presented in Fig. 16(b). The current contains predominantly fundamental frequency due to the 3rd order harmonic trap. In further, the current waveform of the FB-CL is displayed by Fig. 16(c), where the current direction is reversed to charge the cell capacitors during the effective conduction time of directing switches. With the injection of triplen component in reference signal, the chain-link output voltage is able to maintain the peak phase voltage value as $\pm V_{dc}$; thus, the energy balancing for cell capacitors in the FB-CL can be implemented for low modulation index condition as presented in Fig. 16(d). Also, in Fig. 16(e) and (f), the DC side inductor current and the circulating diode current are displayed.

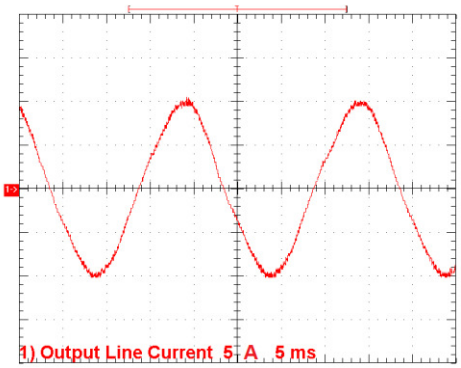


(a) (b)

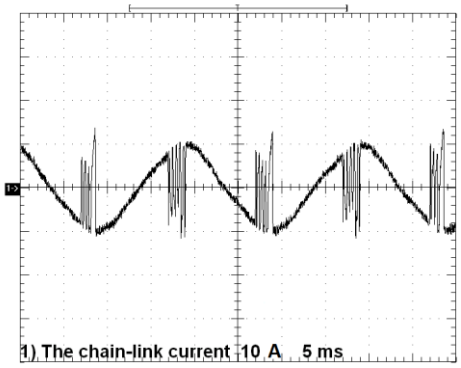
Fig. 15. The picture of experimental installation: (a) CTFB converter and (b) DSP controller.



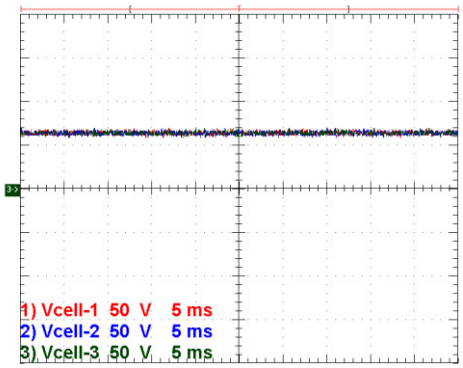
(a)



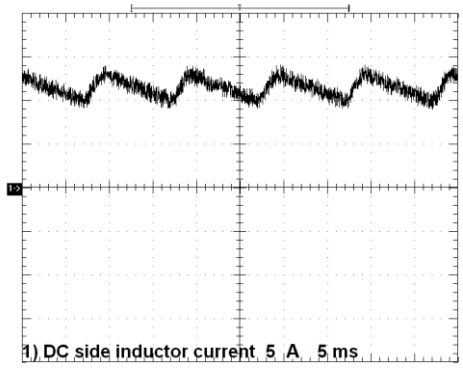
(b)



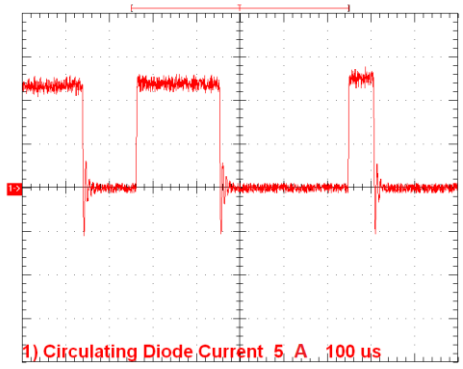
(c)



(d)



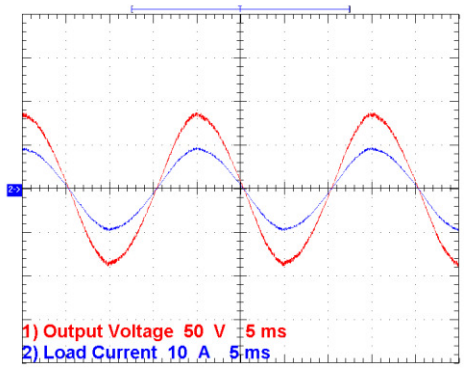
(e)



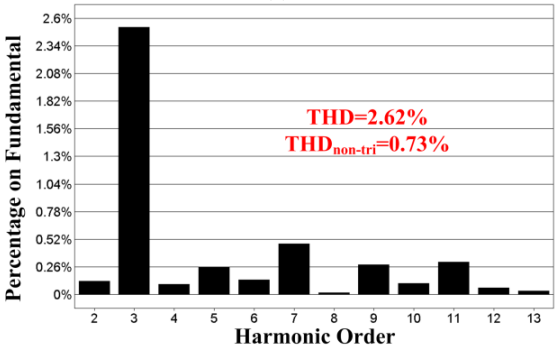
(f)

Fig. 16. Waveforms of the CTFB-HMC with 0.5 modulation index and triplen component injection: (a) voltage waveform on the converter output pole; (b) AC side current with 3rd order harmonic trap; (c) the FB-CL current; (d) cell voltage balancing results; (e) DC inductor current; (f) zoomed-in circulating valve current.

Keeping the pre-set 0.5 modulation index and triplen component reference signal, the post-filter output voltage and current feeding a 9.2Ω resistive load are demonstrated by Fig. 17(a), where the CTFB converter can generate the desired fundamental voltage with the modulation method in (11) provided the triplen component is eliminated. Particularly in this experiment, a certain amount of residual 3rd order harmonics is observed in the base-band spectrum in Fig. 17(b) due to the non-ideal parameters in the harmonic trap design. It is expected that in a real three-phase CTFB-HMC, these harmonics can be fully cancelled in line-to-line voltage. On this basis, the THD values with or without triplen harmonics are calculated as in Fig. 17(b). Similar conclusions for inductive load (9.2Ω, 5mH) and capacitive load (9.2Ω, 100μF) conditions can be concluded from Fig. 18 and Fig. 19, respectively. Therefore, the proposed CTFB-HMC topology is verified to be able to operate under various power factor conditions with the proposed modulation schemes.

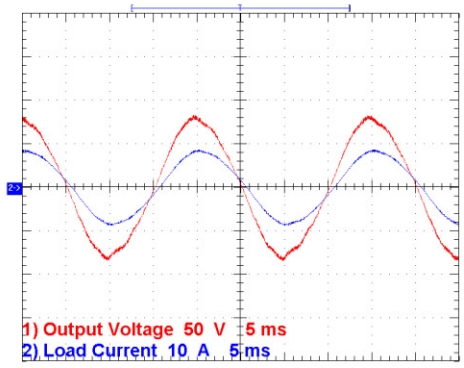


(a)

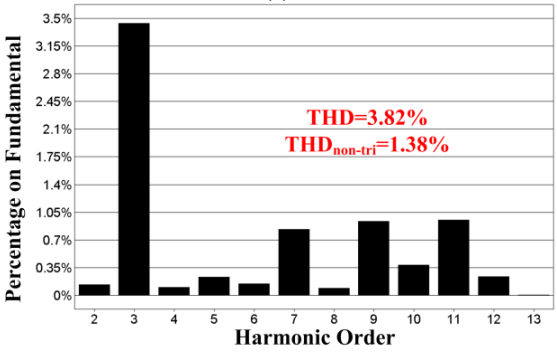


(b)

Fig. 17. The post-filter voltage and current with resistive load: (a) time-domain waveforms; (b) base-band voltage harmonic distribution.



(a)



(b)

Fig. 18. The post-filter voltage and current with inductive load: (a) time-domain waveforms; (b) base-band voltage harmonic distribution.

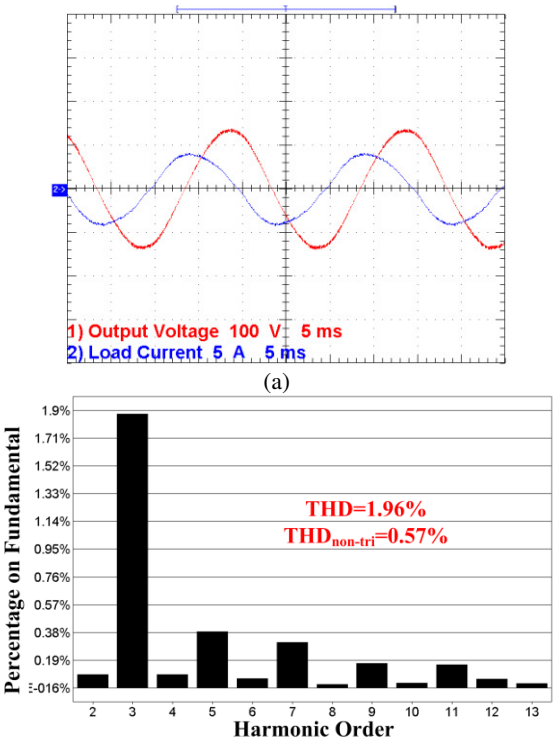


Fig. 19. The post-filter voltage and current with capacitive load: (a) time-domain waveforms; (b) base-band voltage harmonic distribution.

IX. CONCLUSIONS

The controlled transition full-bridge hybrid multilevel converter (CTFB-HMC) has been proposed in this paper. The main features are summarized as follows:

- The CTFB-HMC uses a full-bridge (FB) cell chain-link that dynamically clamps the output poles to synthesize multilevel voltage. Thus, the transformer avoids high dv/dt, which reduces the insulation design demand.
- Due to the two-leg configuration per phase in the proposed topology, its DC voltage utilization and power density are doubled the conventional MMC and hybrid multilevel converters (HMC). Therefore, the number of cell capacitors (footprint) can be minimized when transferring the same power.
- The conduction path device number of the CTFB-HMC is minimized to be same as the half-bridge (HB) cell MMC for per unit power, which leads to better efficiency performance over other topologies including the mixed cell MMC, the FB-MMC and the alternate arm multilevel converter (AAMC).
- The proposed CTFB topology has no DC current in its chain-link, which makes the cell capacitor voltage fluctuate without fundamental frequency and benefits the converter dynamic performance.
- In the proposed CTFB-HMC, a common DC side inductor can be shared by multiple phases, while the conventional MMC has a pair of inductors in each phase for inrush current limiting. A single inductor will reduce converter volume and weight.
- Energy balancing for the cell capacitors in the proposed CTFB converter is implemented utilizing the bipolar voltage output ability of FB cells. To ensure the net energy exchange on the chain-link is zero during each fundamental period, a triplen component signal is injected to realize full range adjustment of the modulation index, which can be neutralized in three-phase systems.
- Comparison between the CTFB-HMC and other multilevel converters shows its attributes including doubled power density, improved efficiency and reduced total costs.
- The control strategy is illustrated in the d-q frame. Then, simulation and experimentation showed the feasibility of the proposed approaches.

The main limitation of the proposed converter is the lack of reverse-blocking capability as with the typical HB-MMC. Therefore, in this paper, the CTFB-HMC is suggested for applications without long distance DC cables, such as fractionally connected FACTS devices.

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