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Active Power Sharing in Input-Series-Input-Parallel Output-Series Connected DC/DC Converters

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Abstract—A high-capacity DC/DC converter with novel input-series-input-parallel output-series connection and with autonomous power sharing between modules is proposed. The proposed scheme is well suited for large-scale wind farm DC collection networks, as it avoids the charging current issues associated with its AC counterpart, and offers lower losses and reduced size and weight when a medium- or high-frequency transformer is used. Small-signal analysis is used to derive the control structures for the converter input and output stages. The proposed control scheme is validated through simulation and experimentation, including demonstration of autonomous power sharing between modules under several operating conditions.

Keywords—DC/DC converter, ISIPOS connection, Power sharing

I. INTRODUCTION

Large offshore wind farms require substantial sub-sea power network to provide internal interconnection. Present solutions are based around conventional medium-voltage AC architectures. Recent studies have highlighted the potential benefits of DC collection networks. Such DC architectures depend on DC/DC conversion to step up the wind-generator output to a voltage compatible with efficient interconnection. Achieving DC/DC conversion at the required voltage and power levels presents a significant challenge for wind-turbine generator's power electronics. Since voltage levels in medium- and high-voltage systems exceed individual semiconductor device voltage ratings, high-capacity converters often require series connection of power devices.

In this paper, a high-power modular structure DC/DC converter which is realized by input-series-input-parallel output-series (ISIPOS) connection of modules is proposed. Parallel-series architectures can be classified into four categories based on their connection. These categories are input parallel output parallel (IPOP), input parallel output series (IPOS), input series output parallel (ISOP) and input series output series (ISOS) [1]. Currently, the open literature contains no publication in the field of the ISIPOS converter and its control strategy. This structure enables generation of high output voltage with reduced voltage and current stresses at the input side. Moreover, the use of high-frequency (HF) or medium-frequency (MF) for galvanic isolation [2, 3], allows the heavy line-frequency transformer in an AC grid to be eliminated, leading to significant weight and size savings and much less investment in copper and core material. For example, the estimated mass of a 1MVA medium-frequency (4kHz) transformer is 150kg, whereas that of a 1MVA 50Hz transformer is 3 tons [4]. With series-output connection, the turns-ratio of the isolation transformer can be reduced, leading to a reduction in leakage inductance. Additionally, modular DC/DC converters offer more compact and lighter designs in situations where a single high-voltage converter with series connection of switches can be replaced with a set of low-voltage converter modules as being discussed in this paper. It will also solve the problem of additional snubber component and more complex gate drive units caused by the series connection of switches [5]. Compared to DC/DC converter based modular multilevel converter (MMC), re-configurability and potential for interleaved control may make the ISIPOS DC/DC converter an attractive choice in medium-voltage applications. ISIPOS connection of multiple low-voltage modules provides an excellent solution for scalability of DC/DC converters, with improved robustness and possibility of fault-tolerant operation. Modular architectures offer further advantages, including internal fault management and module reconfiguration as a result of 'n+k' designed redundancy and the use of power electronic building blocks (PEBB) to reduce production [6-8].

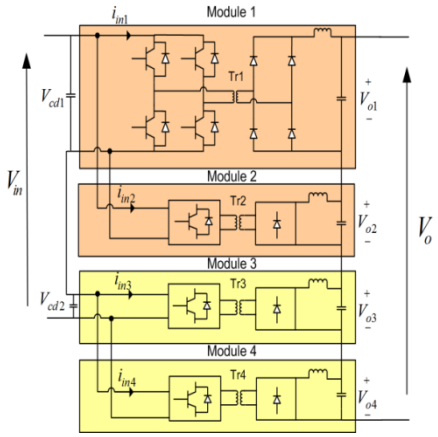

Fig. 1. Four-module ISIPOS DC/DC converter

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Fig.1 shows an illustrative schematic diagram of four-module ISIPOS DC/DC converter that forms the basis of the study. Reliable operation of the ISIPOS modular DC/DC converter requires a control mechanism that ensures equal power sharing among the individual modules, with ability to compensate for any mismatch in the passive components and active switching devices. In this paper, an active input side control scheme for converter power sharing is addressed. Also, the linearized control scheme offered by the Lyapunov control law is applied to provide an improved transient response.

The paper is organized as follows: power sharing in the ISIPOS DC/DC converter is presented in Section 2. In Section 3, the power sharing control strategy for this topology is discussed and the small-signal analyses necessary for controller design are presented. Section 4 presents the simulation and experimental results, and the conclusions are presented in Section 5.

II. POWER SHARING

Assuming all four modules in Fig.1 are lossless, the relationships between the input and output powers of each module can be expressed as (1):

$$\begin{cases} V_{cd1} I_{in1} = V_{o1} I_o \\ V_{cd1} I_{in2} = V_{o2} I_o \\ V_{cd2} I_{in3} = V_{o3} I_o \\ V_{cd2} I_{in4} = V_{o4} I_o \end{cases} \quad (1)$$

where V_{cd1} is the DC input voltage for Modules 1 and 2 due to the parallel connection; V_{cd2} is similarly the DC input voltage for Modules 3 and 4; I_{in1}, $I_{in2}, \ldots, I_{in4}$ are the input currents to Modules 1 to 4, $V_{o1}, V_{o2}, \ldots, V_{o4}$ are the output voltages from Modules 1 to 4; and I_o is the load current. In steady-state condition, the average filter capacitor current is zero, and therefore only a very small filter inductor current ripple is assumed. If output voltage sharing (OVS) is achieved, then $V_{o1}=V_{o2}=V_{o3}=V_{o4}$. Substituting this result into (1) yields (2):

$$V_{cd1} I_{in1} = V_{cd1} I_{in2} = V_{cd2} I_{in3} = V_{cd2} I_{in4} \quad (2)$$

Since $I_{in1}=I_{in3}$ due to the series connection, (2) leads to $I_{in1}=I_{in3}=I_{in2}=I_{in4}$ and $V_{cd1}=V_{cd2}$. It should be noted that input power balancing can be achieved as long as OVS is achieved. Alternatively, if all modules share the same input power, which means Modules 1 and 2 (similarly for Modules 3 and 4) share the same input current and Modules 1 and 3 share the same input voltage, output voltage sharing is achieved.

The common feature revealed for an ISOS system [8-11] is the indispensability of input voltage sharing control. Fig.2 (a) illustrates the equivalent schematic diagram of the output side control strategies for the ISIPOS DC/DC converter. Assuming that OVS is achieved through output side control, modules behave as a constant power sink seen from the input side, with constant output current and equally shared output voltages. Thus, any increase of V_{cd1} leads to a decrease of i_{cin1} and drives the system from equilibrium operating point A to B, as shown in Fig.2 (b). Fig.2 (b) also shows that i_{cin1} at point B is smaller than input current i_{in} and that input filter capacitor current i_{cd1} becomes positive, which will further increase V_{in1}. Thus, the equilibrium point cannot be resumed. An increase in input voltage V_{in1} leads to further increase of itself, eventually leading to a runaway condition between V_{in1} and V_{in2}. This means that any input disturbance may result in an inversely proportional current-voltage relationship. OVS cannot therefore provide input power sharing for the ISIPOS system.

Fig.3 (a) and (b) highlight the consequences of input side control. Modules behave as constant power source seen from the output side, with equally shared input voltage and current. Thus, an increase in V_{o1} leads to a decrease in i_{lf1} which drives the system from the equilibrium operating point A to B, as shown in Fig.3 (b). Now, i_{lf1} is smaller than the load current i_o, current i_{cf1} becomes negative, discharging the capacitor and driving the operating point back to A. Therefore, a dedicated input control loop is indispensable for ISIPOS DC/DC converter stable operation.

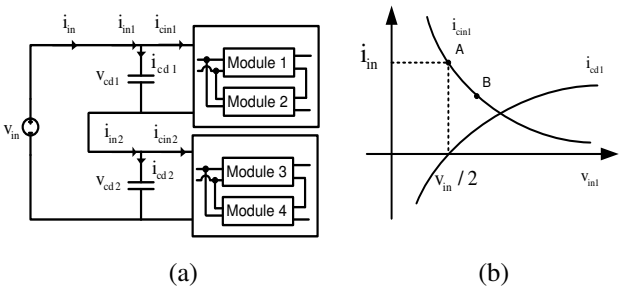


Fig. 2. ISIPOS DC/DC converter (a) output side control and (b) operating point

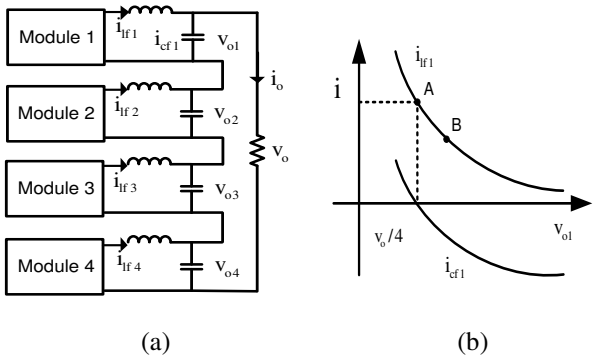


Fig. 3. ISIPOS DC/DC converter (a) input side control and (b) operating point

III. CONTROLLER DESIGN

Converter output voltage control is normally achieved by a linear control technique such as PI control. In comparison, some non-linear techniques can provide improved transient response which is robust to load, input and parameter variations [12]. Most of the non-linear control laws are complex, which makes them difficult to apply, but the linearization schemes have the advantage of reducing the converter model to an equivalent output filter model which

significantly simplifies the control design process, without significant compromise to its robustness. A novel linearized equivalent model of the ISIPOS DC/DC converter incorporating closed-loop output voltage control is presented in Fig.4 [13] which provides a linear representation of converter behavior under large-signal variation which is suitable for faster control response and estimation of the converter state variables. This study applies a large signal Lyapunov controller, with the objective of controlling output voltage error for the ISIPOS DC/DC converter:

$$e = v_o^* - v_o \tag{3}$$

The first order Lyapunov control function v(x) and its derivative are given in (4) and (5), where α is a proportionality constant and β is strictly a positive proportionality constant [13]:

$$v = \frac{1}{2}(\dot{e} + \alpha e)^2 \tag{3}$$

$$\dot{v} = (\dot{e} + \alpha e)(\ddot{e} + \alpha \dot{e}) = -\beta v < 0 \tag{4}$$

$$(\ddot{e} + \alpha \dot{e}) = -\frac{1}{2}\beta(\dot{e} + \alpha e) \tag{5}$$

From Fig.4, (6) and (7) can be derived. Control variable v_c can then be explicitly included in the second order transfer function of the output voltage (8).

$$\frac{di_{lf}}{dt} = \frac{1}{L_f}\left(\frac{1}{\pi}v_c - \frac{1}{4}v_o\right) \tag{6}$$

$$\frac{dv_o}{dt} = \frac{4}{C_f}(i_{lf} - i_o) = \frac{4}{C_f}\left(i_{lf} - \frac{v_o}{R_o}\right) \tag{7}$$

$$\ddot{v}_o = \frac{4}{C_f}\left(-\frac{v_o}{4L_f} + \frac{v_c}{\pi L_f} - \frac{\dot{v}_o}{R_o}\right) \tag{8}$$

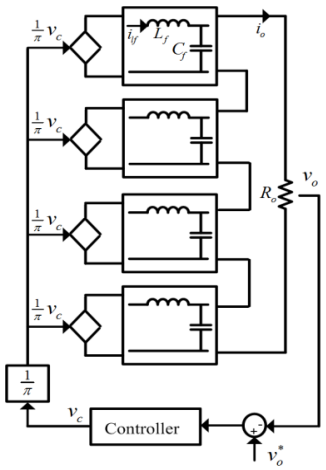


Fig. 4. Simplified large signal control for ISIPOS DC/DC converter

Assuming v_o^* to be constant, $\dot{e} = -\dot{v}_o$ and $\ddot{e} = -\ddot{v}_o$. Based on Fig.4, (9) is deduced. This, in turn, yields (10).

$$\ddot{v}_o = \frac{\alpha\beta}{2}(v_o^* - v_o) - \frac{\beta}{2}\dot{v}_o - \alpha\dot{v}_o = \frac{4}{C_f}\left(\frac{v_c}{L_f\pi} - \frac{v_o}{4L_f} - \frac{\dot{v}_o}{R_o}\right) \tag{9}$$

$$v_c = \frac{\alpha\beta C_f L_f \pi}{8}e + \frac{C_f L_f \pi}{4}\left(\frac{\beta}{2} + \alpha - \frac{1}{R_o C_f}\right)\dot{e} + \frac{\pi}{4}v_o \tag{10}$$

The first and second terms of (10) represent a PD controller, where 'e' will decay to 0 as the system output voltage v_o converges to its reference value. $\pi v_o/4$ is a feed-forward term to speed start-up and to help stabilise the controller. Therefore, (10) can be rewritten as (11):

$$v_c = k_p e + k_d \dot{e} + \frac{\pi}{4}v_o \tag{11}$$

The transfer function between the output voltage and the adjusted output from the load voltage controller can be obtained from Fig.4 and expressed as (12):

$$G_{oc} = \frac{4}{\pi}\frac{1}{L_f C_f s^2 + 1} \tag{12}$$

The resulting closed-loop Lyapunov output voltage controller is shown in Fig.5. The Routh-Hurwitz stability criterion shows that if proportional and derivative gains k_p and k_d are both positive, the system is stable. Thus, by designing the damping ratio and natural frequency from the system characteristic equation, the required closed-loop performance can be achieved.

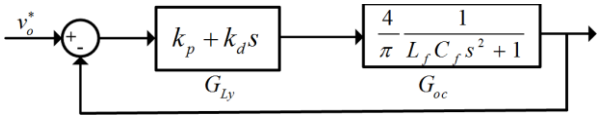


Fig. 5. Lyapunov closed-loop controller

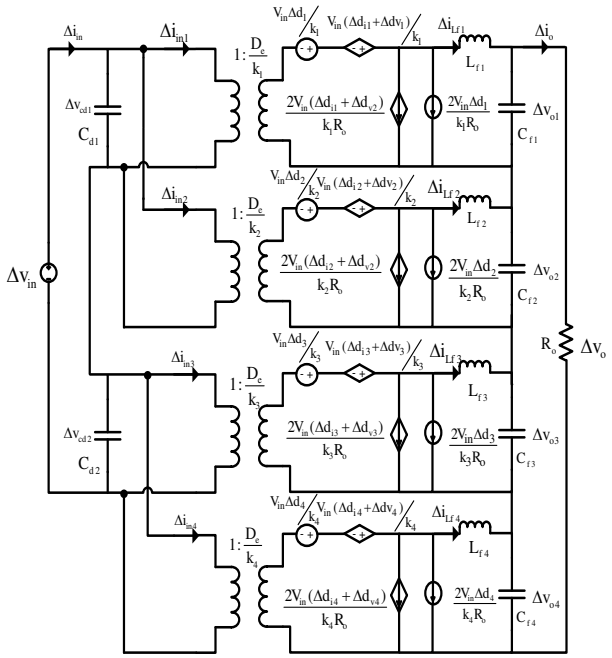


Fig. 6. ISIPOS converter small signal model

The small signal model of four ISIPOS connected DC/DC modules is shown in Fig.6 [7], where k_1, k_2, k_3, k_4 are transformer turns ratios, L_r is the transformer leakage inductance, D_e is the effective duty ratio per module [7], L_{f1}, L_{f2}, L_{f3}, L_{f4}, C_{f1}, C_{f2}, C_{f3} and C_{f4} are filter inductances and capacitances for the four modules. Input voltage perturbation is represented by Δv_{in}, input voltage perturbation components for Modules 1 and 2, and for Modules 3 and 4 are Δv_{cd1} and Δv_{cd2} respectively, input current perturbations for the four modules are Δi_{in1}, Δi_{in2}, Δi_{in3} and Δi_{in4} respectively, and filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δi_{lf3}, Δi_{lf4}, and Δv_{o1}, Δv_{o2}, Δv_{o3} and Δv_{o4} respectively. Δd_1, Δd_2, Δd_3 and Δd_4 are the duty ratio perturbations, and Δd_{v1}, Δd_{v2}, Δd_{v3}, Δd_{v4}, Δd_{i1}, Δd_{i2}, Δd_{i3}, and Δd_{i4} respectively represent perturbations of the duty ratio due to the input voltage and output current, and are defined in (13) [7].

$$\begin{cases} \Delta d_{v1} = \Delta d_{v2} = \dfrac{32 L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{cd1} \\ \Delta d_{v3} = \Delta d_{v4} = \dfrac{32 L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{cd2} \\ \Delta d_{ij} = -\dfrac{8 L_r f_s}{k V_{in}} \Delta i_{lfj} \end{cases} \tag{13}$$

It is assumed that four modules have the same effective duty ratio, transformer turns ratios, and capacitor and inductor values. From Fig.6, equations (14-16) are obtained:

$$\begin{cases} \dfrac{D_e \Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = s L_f \Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e \Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = s L_f \Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{D_e \Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_3 + \Delta d_{v3} + \Delta d_{i3}\right) = s L_f \Delta i_{lf3} + \Delta v_{o3} \\ \dfrac{D_e \Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_4 + \Delta d_{v4} + \Delta d_{i4}\right) = s L_f \Delta i_{lf4} + \Delta v_{o3} \end{cases} \tag{14}$$

$$\begin{cases} \Delta i_{lf1} = s C_f \Delta v_{o1} + \dfrac{\Delta v_o}{R_o} - \Delta i_o \\ \Delta i_{lf2} = s C_f \Delta v_{o2} + \dfrac{\Delta v_o}{R_o} - \Delta i_o \\ \Delta i_{lf3} = s C_f \Delta v_{o3} + \dfrac{\Delta v_o}{R_o} - \Delta i_o \\ \Delta i_{lf4} = s C_f \Delta v_{o4} + \dfrac{\Delta v_o}{R_o} - \Delta i_o \end{cases} \tag{15}$$

Considering the series pair Modules 1 and 3,

$$\begin{cases} \dfrac{k}{D_e}(\Delta i_{in} - s C_d \Delta v_{d1}) = \dfrac{2 v_{in}}{k R_o}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) + \Delta i_{lf1} \\ \dfrac{k}{D_e}(\Delta i_{in} - s C_d \Delta v_{d3}) = \dfrac{2 v_{in}}{k R_o}\left(\Delta d_3 + \Delta d_{v3} + \Delta d_{i3}\right) + \Delta i_{lf3} \end{cases} \tag{16}$$

Based on (16), neglecting duty ratio perturbations due to input voltage and output current, subtraction of the two equations leads to (17). Subtraction of the first and third equations of (14) leads to (18), and from (15) the modular voltage and current relationship can be obtained as (19):

$$\begin{aligned} &\frac{k}{D_e} s C_d (\Delta v_{cd2} - \Delta v_{cd1}) = \\ &\frac{2 v_{in}}{k R_o}\left(\Delta d_1 - \Delta d_3\right) + \Delta i_{lf1} - \Delta i_{lf3} \end{aligned} \tag{17}$$

$$\begin{aligned} &\frac{D_e}{k}(\Delta v_{cd2} - \Delta v_{cd1}) + \frac{V_{in}}{2k}\left(\Delta d_3 - \Delta d_1\right) = \\ &s L_f (\Delta i_{lf3} - \Delta i_{lf1}) + \Delta v_{o3} - \Delta v_{o1} \end{aligned} \tag{18}$$

$$\begin{cases} \Delta v_{o1} = \dfrac{1}{s C_f}\left(\Delta i_{lf1} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o2} = \dfrac{1}{s C_f}\left(\Delta i_{lf2} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o3} = \dfrac{1}{s C_f}\left(\Delta i_{lf3} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o4} = \dfrac{1}{s C_f}\left(\Delta i_{lf4} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \end{cases} \tag{19}$$

Rearranging (19), the relationship between modular voltage output and inductor current can be represented as (20):

$$\begin{cases} \Delta v_{o1} = g_1 \Delta i_{lf1} - g_2\left(\Delta i_{lf2} + \Delta i_{lf3} + \Delta i_{lf4}\right) \\ \Delta v_{o2} = g_1 \Delta i_{lf2} - g_2\left(\Delta i_{lf1} + \Delta i_{lf3} + \Delta i_{lf4}\right) \\ \Delta v_{o3} = g_1 \Delta i_{lf3} - g_2\left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf4}\right) \\ \Delta v_{o4} = g_1 \Delta i_{lf4} - g_2\left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf3}\right) \end{cases} \tag{20}$$

where,

$$\begin{cases} g_1 = \dfrac{R_o + 3}{s C_f (R_o + 4)} \\ g_2 = \dfrac{1}{s C_f (R_o + 4)} \end{cases} \tag{21}$$

Substituting (21) into (18) yields (22):

$$\begin{aligned} &\frac{D_e}{k}(\Delta v_{cd2} - \Delta v_{cd1}) + \frac{V_{in}}{2k}\left(\Delta d_3 - \Delta d_1\right) \\ &= (s L_f + g_1 + g_2)(\Delta i_{lf3} - \Delta i_{lf1}) + \Delta v_{o3} - \Delta v_{o1} \end{aligned} \tag{22}$$

Substituting (22) into (21) yields (23):

$$\frac{\Delta v_{cd1} - \Delta v_{cd2}}{\Delta d_1 - \Delta d_3} = \frac{-\dfrac{2 V_{in}}{k R_o}(g_2 + g_1 + s L_f) - \dfrac{V_{in}}{2k}}{\dfrac{D_e}{k} + s C d \dfrac{k}{D_e}(g_1 + s L_f + g_2)} \tag{23}$$

which can be rewritten as (24):

$$\Delta v_{cd2} = \Delta v_{cd1} + A(s)(\Delta d_3 - \Delta d_1) \tag{24}$$

where,

$$A(s) = -\frac{\frac{2V_{in}}{kR_o}(g_2 + g_1 + sL_f) + \frac{V_{in}}{2k}}{\frac{D_e}{k} + sCd\frac{k}{D_e}(g_1 + sL_f + g_2)} \tag{25}$$

Assuming that $\Delta v_{in}=0$, and $\Delta v_{cd1}=-\Delta v_{cd2}$, the relationship between input capacitor voltage and duty ratio is obtained as (26):

$$\begin{bmatrix} \Delta v_{cd1} \\ \Delta v_{cd2} \end{bmatrix} = \begin{bmatrix} \frac{A(s)}{2} & -\frac{A(s)}{2} \\ -\frac{A(s)}{2} & \frac{A(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_3 \end{bmatrix} \tag{26}$$

The relationship between input current and duty ratio shown in (27) can be obtained by using a similar procedure.

$$\begin{bmatrix} \Delta i_{in1} \\ \Delta i_{in2} \end{bmatrix} = \begin{bmatrix} \frac{B(s)}{2} & -\frac{B(s)}{2} \\ -\frac{B(s)}{2} & \frac{B(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \tag{27}$$

$$\begin{bmatrix} \Delta i_{in3} \\ \Delta i_{in4} \end{bmatrix} = \begin{bmatrix} \frac{B(s)}{2} & -\frac{B(s)}{2} \\ -\frac{B(s)}{2} & \frac{B(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_3 \\ \Delta d_4 \end{bmatrix}$$

where,

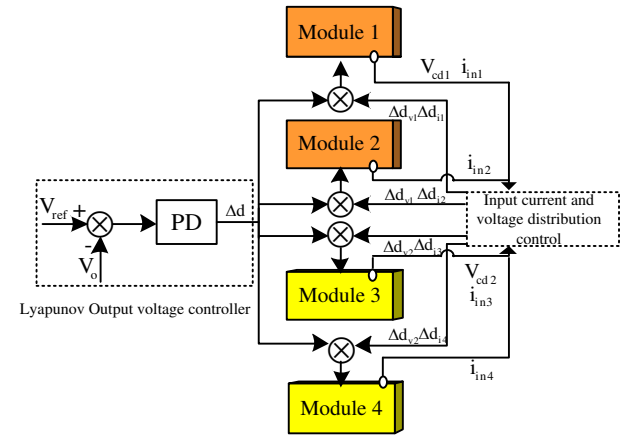
$$B(s) = D_e\left(\frac{2V_{in}}{R_o} + g_3 - g_4\right)$$

$$\begin{cases} g_3 = \dfrac{ac - 2bc}{(a+b)(a-3b)} \\ g_4 = \dfrac{bc}{(a+b)(a-3b)} \end{cases} \tag{28}$$

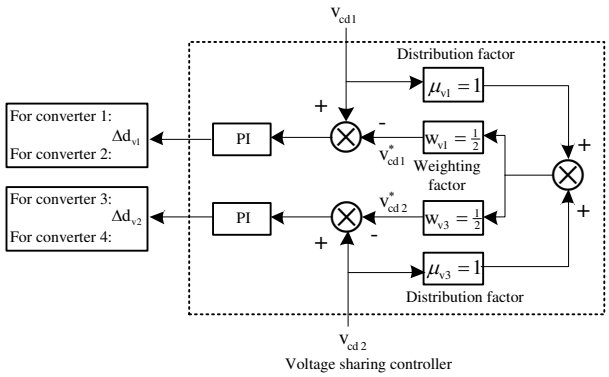
$$\begin{cases} a = sL_f + \dfrac{3 + R_o}{sC_f R_o + 4sC_f} + \dfrac{4L_f f_s}{k^2} \\ b = -\dfrac{1}{sC_f R_o + 4sC_f} \\ c = \dfrac{V_{in}}{2k} \end{cases}$$

The input-series connection requires input voltage balanced while the input-parallel connection requires input current balance. Individual module input voltages and currents are sensed, and average sharing is used to produce correcting error signals to ensure input power sharing.

As shown in Fig.7, the proposed scheme consists of three loops to ensure input voltage and current sharing among the modules. The Lyapunov controller accordingly contributes the main duty ratio signal Δd to all modules, which is then modified by the input current and voltage sharing loops. Average voltage sharing between the two series-connected modules is implemented by correcting the voltage difference signals to generate the duty cycle contributions Δd_{v1} and Δd_{v2} based on (26).



(a)



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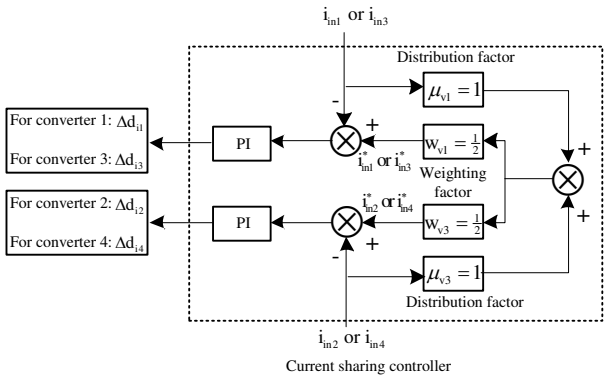

(c)

Fig. 7. Three-loop control for ISIPOS DC/DC converter (a) output voltage loop structure (b) voltage sharing controller (c) current sharing controller

The voltage reference signals for Modules 1 and 3 are generated using distribution factor μ_{v1} and μ_{v3}, and weighting functions W_{v1} and W_{v3}, as shown in Fig.7 (b). Average active sharing is used, therefore $\mu_{v1}=\mu_{v3}=1$ and $W_{v1}= W_{v3}=1/2$.

Master-slave active sharing could also be used, but this is not discussed here. The voltage reference for Modules 1 and 3 is therefore given by (29):

$$v_{ref} = \frac{v_{cd1} + v_{cd2}}{2} \tag{29}$$

Alternatively, a fixed voltage reference of $v_{in}/2$ could be used. The main advantages of using the dynamic input voltage reference in (29) rather than a fixed voltage reference are that it minimizes the interaction among the different control loops and results in better transient performance [1]. Referring to Fig.7, taking Module 1 as an example, the duty ratio contribution of the voltage sharing loop is:

$$\Delta d_{v1} = k_p(v_{cd1} - v^*_{cd1}) + k_i(v_{cd1} - v^*_{cd1}) \tag{30}$$

The current sharing loop corrects differences in input current between the parallel-connected modules, i.e. Modules 1 and 2, and Modules 3 and 4. Similar to the voltage sharing loop, dynamic current sharing is applied to generate the other duty ratio components Δd_{i1}, Δd_{i2}, Δd_{i3} and Δd_{i4} based on (27). Due to its discontinuity, high-cost current transducer is required to provide the high bandwidth. The duty ratios for each module are, therefore:

$$\begin{cases} d_1 = \Delta d + \Delta d_{v1} + \Delta d_{i1} \\ d_2 = \Delta d + \Delta d_{v1} + \Delta d_{i2} \\ d_3 = \Delta d + \Delta d_{v2} + \Delta d_{i3} \\ d_4 = \Delta d + \Delta d_{v2} + \Delta d_{i4} \end{cases} \tag{31}$$

IV. RESULTS

The proposed control strategy is assessed by considering the impact of mismatches among modules, and transient operating conditions in the ISIPOS DC/DC converter. To assess the performance improvement offered when the converter is regulated using the proposed three-loop control scheme, simulation results are compared with those obtained from the widely used common duty-cycle control scheme shown in Fig.8 [14, 15].

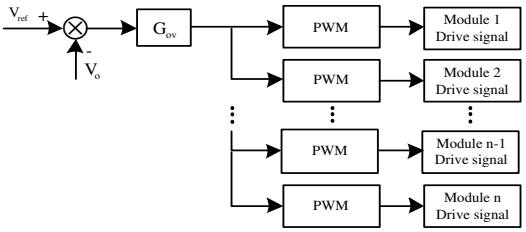

Fig. 8. Common duty-cycle control

The test system, shown in Fig.1, consists of an ISIPOS DC/DC converter with rated output power of 1MW. Mismatched parameters, including input capacitance, transformer turns ratio, output inductance and capacitance, as specified in Table 1, are introduced to test the effectiveness of the power balancing function.

TABLE I. SIMULATION AND EXPERIMENTAL SYSTEM PARAMETERS

Parameter	Values	
	Simulation	**Experiment**
DC/DC Converter Rated Power	1MW	100W
Input DC Voltage	2200V	40V
Number of Modules	4	4
Input Capacitance	C_{d1} = 50μF C_{d2} = 80μF	C_{d1} = 40μF C_{d2} = 10μF
Transformer Turns Ratio	T_1 = 1:6.8 T_2 = 1:6.4 T_3 = 1:6 T_4 = 1:6.4	T_1 = 1:1.4 T_2 = 1:1.2 T_3 = 1:1.3 T_4 = 1:1.2
Output Inductance	L_1 = 0.05H L_2 = 0.06H L_3 = 0.06H L_4 = 0.05H	L_1 = 6.8mH L_2 = 5.0mH L_3 = 5.9mH L_4 = 6.3mH
Output Capacitance	C_1 = 300μF C_2 = 350μF C_3 = 300μF C_4 = 330μF	C_1 = 160μF C_2 = 160μF C_3 = 200μF C_4 = 200μF
PWM Carrier Frequency	2.5kHz	2.5kHz

For the simulation validation, the control schemes are tested by applying a step change in load voltage reference from 21.2kV to 22.5kV at t=0.2ms and back to 21.2kV at t=0.4ms, with system parameter mismatch conditions summarized in Table I. Fig.9 (a) shows the load voltage and individual module output voltages (v_{o1}, v_{o2}, v_{o3} and v_{o4}) under the common duty-cycle control scheme, and Fig.9 (b) shows the performance of the proposed control scheme. The simulation results show that the performance of the common duty-cycle control strategy is significantly affected by the mismatches. With this control scheme the output voltages of all modules exhibit significant voltage ripple, with a worst-case peak voltage ripple value of approximately 14.7% of the average load voltage. Conversely, the proposed control scheme is able to compensate the mismatch, since the sharing loop enables adjustment of the duty ratio of each individual module so that each module can achieve the same output voltage. Output performances can be further improved by interleaving the modules' control systems. These results have demonstrated that with the proposed input power balancing control scheme is able to compensate for any negative influences of system parameters mismatch.

A scaled-down experimental rig of ISIPOS with four modules is built to validate the proposed control scheme. Fig.11 shows the two output voltage being regulated at the desired reference value of 60V with common duty-cycle control and proposed control scheme respectively. It indicates that without the dedicated input voltage and current control, each module operates at different voltages V_{o1}=16.1V, $V_{o1=}$16.9V, $V_{o1=}$12.8V and V_{o1}=14.2V. By virtue of the proposed control loops, it compensates for the mismatch in the module transformer turns ratios and input capacitances by adjustment the phase shift angle of individual module in order to ensure that output voltages are equally shared, see Fig.11 (b). Fig.12 shows that the proposed control the system is able to ensure OVS during start-up transient and load changing transient.

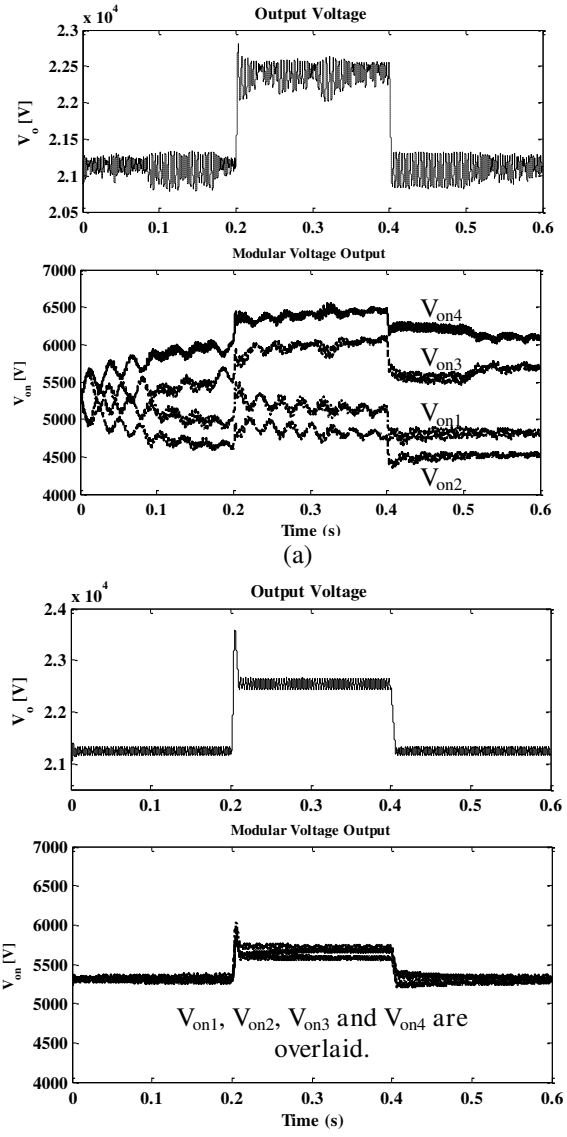

Fig. 9. Simulated response to a step change in load voltage, with mismatched parameters (a) common duty-cycle control (b) proposed control

Fig. 10. ISIPOS connected full-bridge DC/DC converter test rig

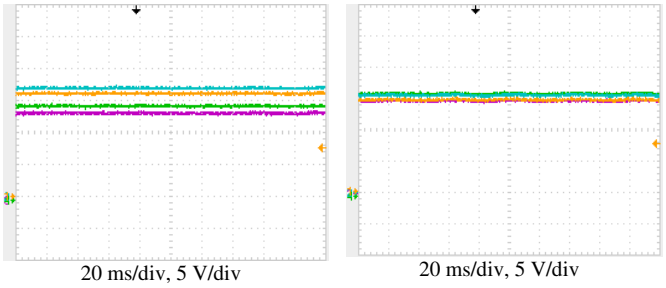

Fig. 11. Experiment resullt (a) with common duty-cycle control and (b) with proposed control

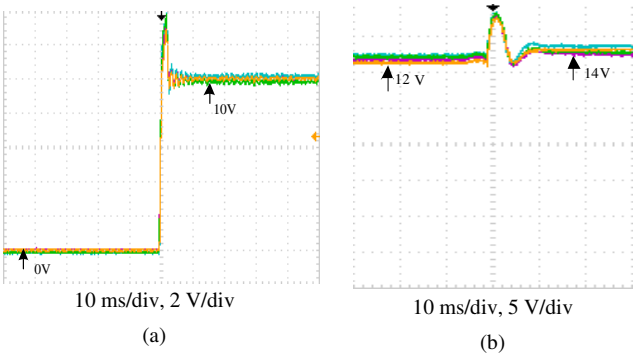

Fig. 12. Experiment resullt with proposed control (a) closed loop start-up transient and open loop load step-up transient

V. CONCLUSIONS

A new modular DC/DC converter with ISIPOS connection is proposed with ability to further expand the benefits of parallel-series connection of low power rating modules. Primarily, an active input side control scheme for converter power sharing is addressed. For the load voltage control, the linearized control scheme offered by the Lyapunov control law reduces complexity and ensures improved transient response which is robust to load and input and parameter variations when compared to a linear control technique. The power sharing loops ensure input current sharing among the series connected modules, and input voltage sharing among the parallel connected modules. System-level simulation and scaled-down experimental validation are performed to verify the modeling and control schemes. It is verified that the proposed control, in ISIPOS DC/DC converter, is reliable for stable control and uniform sharing.

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