A Hybrid Modular Multilevel Converter with Novel Three-level Cells for DC Fault Blocking Capability

Rui Li, John E Fletcher, Senior Member, IEEE, Lie Xu, Senior Member, IEEE, Derrick Holliday, and Barry W. Williams

Abstract—A novel hybrid, modular, multilevel converter is presented that utilizes a combination of half-bridge and novel three-level cells where the three-level cells utilize a clamp circuit which, under dc side faults, is capable of blocking fault current thereby avoiding overcurrents in the freewheel diodes. This dc fault blocking capability is demonstrated through simulation and is shown to be as good as the modular multilevel converter which utilizes full-bridge cells but with the added benefits of: lower conduction losses; fewer diode and semiconductor switching devices, and; fewer shoot-through modes. The semiconductor count and conduction loss of the proposed converter are reduced to around 66.5% and 72% of that of modular multilevel converter based on the full-bridge cells respectively, yielding lower semiconductor cost and improved efficiency. Dc fault ride-through operation is realized without exposing the semiconductors to significant fault currents and overvoltages due to the full dc fault blocking capability of the converter.

Index Terms--dc fault blocking, high-voltage dc (HVDC) transmission system, hybrid multilevel converter, modular multilevel converter (MMC), three-level cell, voltage source converter (VSC).

I. Introduction

Recently, high-voltage dc (HVDC) transmission systems based on modular multilevel converters (MMCs) have developed rapidly due to their significant advantages in comparison with conventional high-voltage ac (HVAC), line commutated converter HVDC (LCC-HVDC) and two-level voltage source converter (VSC) HVDC systems. However, the vulnerability of half-bridge (HB) cell based MMC (HB-MMC) to dc faults is a major issue that constrains its application in HVDC systems. In the event of a dc short circuit, high ac currents flow through the freewheeling diodes from the ac grid to the dc side [1, 2]. Fig. 1 demonstrates that the fault currents reach around 8.5 times rated current due to the low impedance of the short circuit and this may cause serious damage to the converters and associated semiconductors.

Traditionally, ac or dc circuit breakers are required to disconnect the HB-MMC from the ac grid or dc fault point [3].

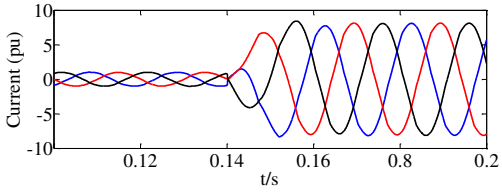

Fig. 1. Three-phase currents of HB-MMC when the pole-to-pole dc fault occurs at 0.14s, all normalized to 2kA. Model based on parameters shown in Table III.

However the response of conventional mechanical circuit breakers is too slow and the semiconductors still endure high current stress during the response time. Presented in [4-7], bypass elements, typically thyristors, are used to protect the anti-parallel diodes of the HB cells. However, the ac circuit breaker and bypass element have to be rated at the full prospective short circuit current. The solid-state dc circuit breaker can achieve fast interruption time but at high capital cost and significant on-state operational losses due to the semiconductors in the main current path [8]. Hybrid dc circuit breakers have been proposed where a mechanical path serves as main conduction path with minimal losses during normal operation, and a parallel connected solid-state breaker is used for dc fault isolation [9-11]. However, it has relatively large footprint and its capital cost is still high [11].

Besides the above dc fault isolation approaches, different topologies based on the conventional MMC are addressed in [4, 12]. Another alternative replaces the HB cells with the full-bridge (FB) cells, thus the capacitors can be inserted into the circuit in either polarity. This feature allows the FB based MMC (FB-MMC) to block dc faults and offers greater controllability [12]. However, this approach requires twice the number of semiconductors in the conduction path, thus higher semiconductor power losses than the equivalent HB arrangement is expected.

Based on active controlled power electronic components, the dc transformer is presented in [4] and [13]. It is mainly used to connect dc links with different voltage levels. However, an additional benefit of the use of the dc transformer is the isolation of dc faults. By blocking the active switches of the dc transformer, the dc fault can be isolated rapidly, thus the remaining healthy parts of the dc grid can still function after the fault. But the above functionalities are achieved at the expense of much higher capital cost and power losses, and a larger footprint compared to the FB-MMC suggested in [12].

Recently, the Hybrid Converter concept has been proposed which combines different topologies in order to optimize

This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) under Grant EP/K006428/1.

R. Li, L. Xu, D. Holliday, and B. W. Williams are with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, G1 1XW UK (e-mail: rui.li@strath.ac.uk, lie.xu@strath.ac.uk, derrick.holliday@strath.ac.uk, b.w.williams@eee.strath.ac.uk).

J. E. Fletcher is with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, N.S.W. 2052, Australia (e-mail: john.fletcher@unsw.edu.au).

converter performances. Based on current source converters and FB-MMCs, the alternate-arm multilevel converter is presented in [14-17]. This topology can block dc faults with reduced semiconductor losses compared to the FB-MMC; however, the director switches, composed of series connected IGBTs, are still required. Furthermore, its ac voltage flexibility is limited and large dc filters are required to eliminate the predominant 6^{th} harmonic in the dc current [17-19]. References [2, 20-22] present the hybrid multilevel converter which uses the two-level converter in series with cascaded FB cells. It can block dc faults but the dc capacitors are still needed to maintain the dc link voltage stable and the active switches of the two-level VSC still suffer high voltage stresses.

References [23, 24] propose the clamp double (CD) sub-module, shown in Fig. 2 (a), to reduce the losses and block the dc fault. By using the clamp circuit, the number of devices in the conduction path is reduced to 3/4 of that for FB-MMC, while it can block an ac fault by connecting the two capacitors in series. However, for the dc fault, the two capacitors are connected in parallel, hence the CD cell only utilizes half of the possible cell capacitor voltages to block dc faults. In addition, during the initial stages of the fault immediately after switches have been disabled, the fault current will only flow through the cell capacitor with lowest voltage until it is charged to the same voltage as the other capacitor. As a result the fault current is not shared between the two parallel circuits.

The cross connected (CC) cells presented in [25, 26] can generate $-2V_c$ to block the dc fault. However, the two clamp switches must tolerate twice the capacitor voltage hence the series connection of two switches is required typically and both dynamic and static voltage balancing techniques are necessary. Additionally, to reduce the cell capacitance in normal operation or operate the converter continuously under dc fault conditions, the CC cells are required to generate negative voltages ($-V_c$ and $-2V_c$). Thus, the clamp switches must operate in a switching mode to change the polarity of the output voltage, resulting in higher switching losses compared to the FB cell.

The mixed cell presented in [26, 27] connects a HB cell with a FB cell in series to obtain the dc fault blocking capability and reduce the losses, Fig. 2 (b). It can generate a negative voltage ($-V_c$), which allows the converter to block the dc fault and offers greater controllability than the HB cell. Besides, its losses are expected to be the same as the CD cell. However, it uses one more IGBT and one less diode compared with the CD cell, thus its device cost is higher. Additionally, it can only provide $-V_c$ to block the dc fault, which is the same with the CD cell. In [28], an improved configuration which removes the IGBT S_6 in Fig. 2 (b) was proposed. Such configuration uses one less diode compared to the CD cell but retains dc fault blocking capability. In [29], a mixed HB and FB configuration was proposed with the ratio between FB and HB cells per arm being higher than one, yielding a slightly lower efficiency though it can transfer more power than the conventional MMC by utilizing the negative output voltage capability of the FB cells.

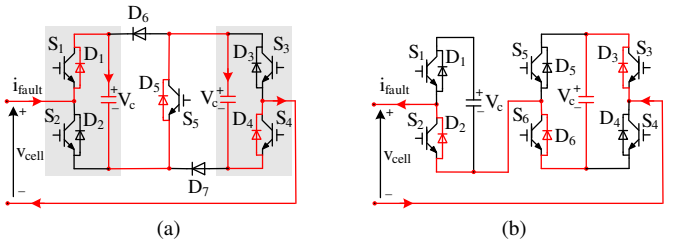

Fig. 2. Alternative blocking cell topologies. (a) Clamp double (CD) cell topology proposed in [23, 24] showing dc fault current direction and generation of only $-V_c$ at its output. (b) Mixed cell topology.

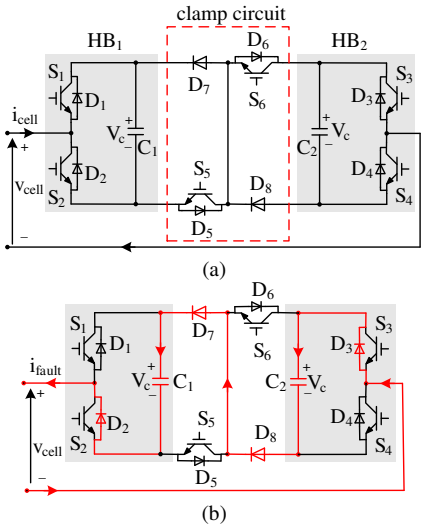

Fig. 3. Three-level (TL) cell with full dc fault blocking capability. (a) Topology, where i_{cell} denotes the positive direction reference of cell current. (b) DC fault conduction path with all switches off to generate $-2V_c$ blocking voltage, where i_{fault} denotes the fault current direction.

TABLE I
Switching Table for the Three-level Cell.

S_1	S_2	S_3	S_4	S_5	S_6	v_{cell}
0	1	1	0	1	1	0
1	0	1	0	1	1	V_c
0	1	0	1	1	1	V_c
1	0	0	1	1	1	$2V_c$
0	0	0	0	0	0	$-2V_c$ (for dc fault blocking)

In order to overcome the above problems, the three-level (TL) cell based hybrid MMC (TL-HMMC) is proposed and its operation including dc fault blocking capability is researched. The proposed TL cell is introduced in Section II along with the converter topology, operating principle and capacitance requirement. In Section III, the switching model of the TL-HMMC is presented and the control strategy is introduced and discussed. The dc fault blocking capability of the TL-HMMC is assessed in Section IV, considering a two-terminal HVDC link. Section V concludes the paper.

II. Three-level Cell Based Hybrid MMC

A. Three-level Cell with Full DC Fault Blocking Capability

To achieve the full dc fault blocking capability with reduced losses and semiconductor costs, the TL cells with two active clamp switches is proposed, Fig. 3 (a). It is effectively

two HB cells connected in series by a clamp circuit. Its switching states are detailed in Table I. In normal operation, the switches S_5 and S_6 are always on. Thus, the positive current, which has the same direction with the reference current i_{cell}, flows through D_5 and D_6, while the negative current would flow through S_5 and S_6. The TL cell is equivalent to two series connected HB cells and can generate three output levels (0, V_c and $2V_c$) under normal operation. Note that the voltages of diodes D_7 and D_8 are both clamped at V_c by switches S_5 and S_6 respectively in normal operation.

The TL cell can fully utilize the cell voltage ($-2V_c$) to suppress the fault current and achieve the dc fault blocking capability, as shown in Fig. 3 (b). Once a fault is detected, all the switches are turned off. Then the dc fault current flows through the diodes D_3, D_8, D_7 and D_2 and charges the capacitors C_1 and C_2. The capacitors C_1 and C_2 are effectively connected in series presenting the sum of C_1 and C_2 voltages to the fault current path hence the output voltage of the cell is $-2V_c$ which acts in opposition to the applied ac line voltages to block the dc fault current. This differs from the parallel capacitors in the dc fault path for the clamp double cell shown in Fig. 2, which only generates $-V_c$ during dc faults. As a result fewer HB sub-modules have to be replaced by TL cells to block the dc fault in the hybrid MMC, as detailed in Section II B. This yields lower losses and semiconductor cost. From the above operating principle, it can be seen all the devices of the TL cell endure the same voltage stress (cell capacitor voltage V_c) during both normal and fault conditions, which standardizes the choice of power devices in both HB and TL cells [23, 24]. Also, the semiconductors of the clamp circuit do not need to operate in the switching mode, thus diodes D_7 and D_8 do not require fast recovery characteristics and the system loss can be reduced by choosing clamp switching devices with low conduction losses.

In the FB-MMC, each pair of switches contributes a shoot-through mode where switches in the same leg could be switched on simultaneously by, for example, EMI noise, causing fault currents. By using the clamp circuit with two switches shown in Fig. 3, fewer shoot-through modes exist whilst still ensuring dc blocking capability yielding potentially higher reliability. Also note that, besides offering full dc fault blocking capability, the proposed TL cells can still isolate ac faults in the same way as HB cells.

Besides connecting two HB cells, the proposed clamp circuit can connect other cells which do not have the dc fault blocking capability, such as the neutral point clamped (NPC) and flying capacitor (FC) based cells, Fig. 4. These alternative configurations can generate five voltage levels (0, V_c, $2V_c$, $3V_c$ and $4V_c$) and only one quarter of the alternative cell modules are required in the stack compared with the conventional HB and FB cell system. Thus, the two alternative topologies significantly reduce the complexity of the control in terms of the number of cells and associated signals, which is often associated with improved reliability of the converter system [30], particularly, if the cell modulation can be made semi-autonomous.

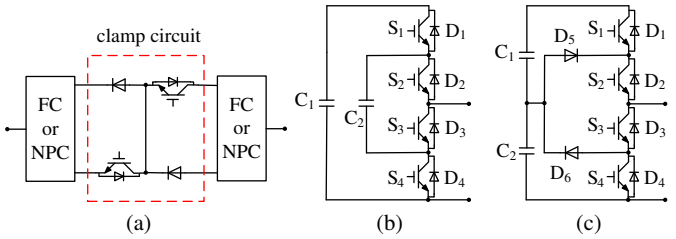

Fig. 4 Other possible cell topologies using the proposed clamp circuit. (a) Five-level cell composed of two FCs/NPCs connected by the presented clamp circuit. (b) Details of FC structure. (c) Details of NPC structure.

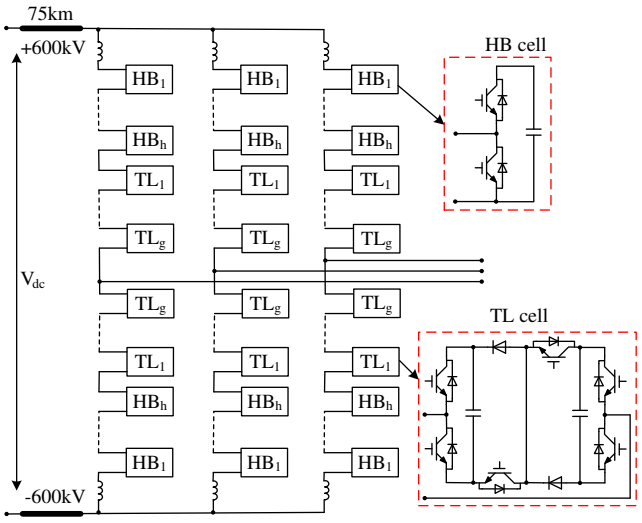

Fig. 5. Three-level cell based hybrid MMC (TL-HMMC) with dc fault blocking and minimized losses.

However, compared with the proposed TL cell, the device voltage stresses of the clamp circuit in Fig. 4 (a) are doubled and series connected semiconductors would be necessary. The same problem applies to the capacitor C_1 for the FC structure in Fig. 4 (b). Although all the devices of the NPC structure in Fig. 4 (c) have the same voltage rating, two more diodes D_5 and D_6 are required, resulting in higher capital cost. Hence, they are not preferable in the practical application, compared with the proposed TL cells.

B. Three-level Cell Based Hybrid MMC

Fig. 5 shows a generic version of the proposed TL-HMMC. Each arm is a combination of novel TL cells and conventional HB cells. All the devices of the TL-HMMC can be arranged to endure the same voltage stresses $V_c = V_{dc}/(2g+h) = V_{dc}/N$, where V_{dc} is the dc link voltage, h and g are the HB and TL cell numbers per arm respectively, and; N is the equivalent cell number per arm where $N=2g+h$. The on-state loss can be minimized by arranging suitable ratio between the TL cell number g and HB cell number h, while still providing adequate reverse voltage to block the dc fault current. The process of choosing g and h is detailed as follows.

Once the dc fault is detected, typically within a few tens of microseconds, all the switches of TL-HMMC are turned off and the fault current flows through the anti-parallel diodes of HB cells. As a result the HB cells on the arms of the TL-HMMC do not contribute any voltage to block the dc fault current forced by the ac line voltages. However, the dc fault

TABLE II
Comparison between MMC and Hybrid MMC Topologies Demonstrating Advantages of the TL-HMMC.

ITEM (per phase)	HB-MMC	FB-MMC	CD-MMC	CC-MMC	TL-MMC	FB-HMMC	CD-HMMC	CC-HMMC	TL-HMMC
IGBTs	4N	8N	5N	8N	6N	5.76N	4.88N	5.76N	4.88N
Diodes	4N	8N	7N	8N	8N	5.76N	6.64N	5.76N	5.76N
Semiconductors	8N	16N	12N	16N	14N	11.52N	11.52N	11.52N	10.64N
Semiconductors in current path	2N	4N	3N	4N	4N	2.88N	2.88N	2.88N	2.88N
Series connection of switches	No	No	No	Required	No	No	No	Required	No
Number of shoot-through modes	2N	4N	2N	4N	2N	2.88N	2N	2.88N	2N

currents can be blocked by the voltage impressed by the series-connected capacitors of the TL cells which are inserted into the fault current path from the ac side to the dc side.

The impressed voltage blocking the dc fault is the sum of the upper arm TL voltages on one phase and lower arm TL voltages on another phase. If this impressed voltage is higher than peak line voltage, the uncontrolled fault current from the ac side will be suppressed and the fault current blocked. If all the HB and TL cells are to have the same voltage stress, the following equation is derived:

$$4gV_c = 4g\frac{V_{dc}}{N} \geq \frac{\sqrt{3}}{2}V_{dc}. \quad (1)$$

The TL cell number per arm required to block the dc fault can then be determined:

$$g \geq 0.22N. \quad (2)$$

Based on the conventional HB-MMC, the proposed converter replaces fewer than half of HB cells (2×0.22=0.44) with TL cells hence a hybrid converter comprising of TL and HB cells. This distribution of TL and HB cells reduces the number of power devices in the conduction path and improves the efficiency; meanwhile the dc fault can still be blocked. The cell structure in Fig. 2 does not guarantee this condition and is a major motivation for adopting the structure in Fig. 3.

The number of TL cells of the TL-HMMC is set at 0.22N and compared with other topologies, Table II. The dc fault blocking capability of the proposed solution is achieved with a penalty of only 44% increase in conduction losses compared to the conventional HB-MMC. It can also be seen that the number of semiconductors (IGBTs and diodes) required for the TL-HMMC is only around 66.5% (10.64N/16N) of that for FB-MMC, yielding lower power device capital cost. Additionally, the conduction loss of the TL-HMMC is reduced to around 72% (2.88N/4N) of that of the FB-MMC with the same power rating, due to fewer power devices in the conduction path. In normal operation, the clamp switching devices, S_5 and S_6, are always on and the switching loss is zero, thus the system loss can be reduced further by choosing clamp switching devices with low conduction losses. As a result the TL-HMMC is expected to be more efficient than predicted by this simple treatment. Table II also compares the TL-HMMC topology with the conventional HB-MMC and demonstrates that the TL-HMMC provides dc fault blocking capability with only a modest increase in semiconductors.

The attributes of the TL-MMC, which is composed of only TL cells per arm, are better than that of FB-MMC and CC-MMC, such as reduced semiconductors in the current path, lower power device capital cost and reduced shoot through modes, but not as good as that of CD-MMC, Table II. However, the CD-MMC only utilizes half of the possible cell capacitor voltages to block dc faults hence the minimum number of CD cells is twice the number of TL, CC and FB cells in the other hybrid MMCs. The TL-HMMC requires the lowest number of semiconductors among all the MMCs and hybrid MMCs with dc fault blocking capabilities, yielding the lowest capital cost and its reliability is potentially improved, as its shoot-through modes are lower and the director switches composed of series connected IGBTs are not required. The TL-HMMC promises the best performance compared with other MMCs and hybrid MMCs.

Notice that a higher voltage rating switch could, if available with suitable ratings, be used as the clamping circuit, but typically the CC cell would need to use series-connected devices to guarantee suitably-rated reverse blocking voltage and current capability. Also, to simplify the comparison, the two clamp switches of the CC cell are both composed of two switches connected in series to block twice the capacitor voltage and the voltage sharing problem is neglected.

C. Capacitance Requirements

The specified maximum capacitor voltage ripple generally determines the capacitance requirement. The following section details the process of choosing the capacitances of the TL and HB cells.

Assuming the converter lossless, the dc side power is equal to the ac power during steady-state operation. Thus, the upper arm power P_u and its average value $\bar{P}_u$ can be obtained:

$$P_u(\omega t) = \frac{V_{dc}I_{dc}}{6}\left[1 - m\sin(\omega t)\right]\left[1 + \frac{2\sin(\omega t - \varphi)}{m\cos\varphi}\right] \quad (3)$$

$$\bar{P}_u = \frac{1}{2\pi}\int_0^{2\pi} P_u d(\omega t) = 0 \quad (4)$$

where m is the modulation index; φ is the phase angle between the phase voltage and current; I_{dc} is the dc current; ω is the angular frequency; u refers to upper arms. Similarly, the average power of lower arm equals zero:

$$\bar{P}_l = 0. \quad (5)$$

This ensures that the capacitor voltages of HB and TL cells are theoretically unchanged at the beginning and at the end of one fundamental period. Thus the capacitor voltage balancing can be achieved by rotating the HB and TL cell capacitors when synthesizing different voltage levels, taking into account arm current polarities, and voltage magnitudes of the cell capacitors, as is conventionally performed in MMCs.

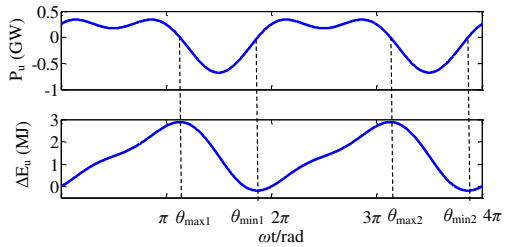

Fig. 6. Upper arm power and energy variation of TL-HMMC, where m=0.8, V_{dc}=1200kV, I_{dc}=1.25kA and φ=0.

According to the upper arm power, (3), the upper arm energy variation is

$$\Delta E_u(\omega t)=\int_0^{\omega t} P_u\,d(\omega t)$$
$$=\frac{V_{dc}I_{dc}}{6}\left\{\begin{array}{l}-\dfrac{2}{m\cos\varphi}\left[\cos(\omega t-\varphi)-\cos\varphi\right]+\\ m\left[\cos(\omega t)-1\right]+\dfrac{1}{2\cos\varphi}\left[\sin(2\omega t-\varphi)+\sin\varphi\right]\end{array}\right\}. \quad (6)$$

Shown in Fig. 6, the angle θ_{maxk} and θ_{mink}, where the upper arm power is zero, are expressed as

$$\left\{\begin{array}{l}\theta_{max\,k}=\arcsin\left[m\cos(\varphi)/2\right]+\varphi+2\pi(k-0.5)\\ \theta_{min\,k}=-\arcsin\left[m\cos(\varphi)/2\right]+\varphi+2k\pi\end{array}\right. \quad k=1,2,3,\cdots. \quad (7)$$

It can be seen from (7) that the θ_{maxk} and θ_{mink} are determined by the modulation index and the phase angle and are independent of the power rating of HVDC system. Then, the maximum energy variation for the upper arm is

$$\Delta E_{u\,max}=\Delta E_u(\theta_{max\,1})-\Delta E_u(\theta_{min\,1})$$
$$=\frac{g}{2}C_T\Delta D_T\left(V_{T\,max}+V_{T\,min}\right)^2+\frac{h}{4}C_H\Delta D_H\left(V_{H\,max}+V_{H\,min}\right)^2 \quad (8)$$

where V_{Hmin}, V_{Hmax}, V_{Tmin} and V_{Tmax} are the minimum and maximum capacitor voltages for HB and TL cells respectively; ΔD_H and ΔD_T is the maximum ripple ratios of HB and TL capacitor voltages:

$$\Delta D_H=\frac{2(V_{H\,max}-V_{H\,min})}{V_{H\,max}+V_{H\,min}},\qquad \Delta D_T=\frac{2(V_{T\,max}-V_{T\,min})}{V_{T\,max}+V_{T\,min}}. \quad (9)$$

Equations (8) and (9) are used to determine the capacitances for the HB and TL cells in Section IV, according to the voltage ripple requirements. Note that the proposed TL cells can operate in a different mode to the HB cells. Thus their capacitance requirements are different but are still dominated by (8) and (9). Also, in the FC based cell shown in Fig. 4, the voltage across C_1 is twice of that of C_2. Hence its capacitance requirement is different to that of the HB cell in the conventional MMC and can be derived with a similar approach to that presented in this section.

III. Control Strategy of TL-HMMC

This section uses the switching function based model to design the control strategy of the proposed TL-HMMC. Shown in Fig. 7, each arm is represented by controlled voltage sources (v_{Huk} and v_{Tuk} or v_{Hlk} and v_{Tlk}) in series with inductance and resistance of the arm reactor [31].

The controlled voltage sources can be described in the abc reference frame by:

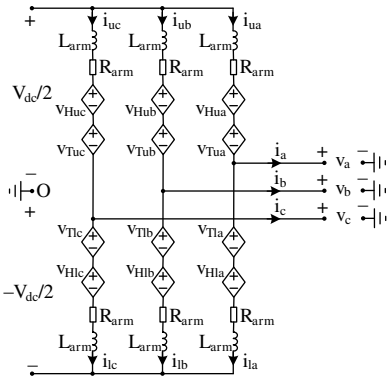

Fig. 7. Equivalent circuit using controlled voltage sources in abc reference frame.

$$v_{Huk}+v_{Tuk}=\sum_{i=1}^{h}\left(s_{Huki}V_{Huki}\right)+\sum_{i=1}^{g}\left(s_{Tuki}V_{Tuki}\right) \quad (10)$$

$$v_{Hlk}+v_{Tlk}=\sum_{i=1}^{h}\left(s_{Hlki}V_{Hlki}\right)+\sum_{i=1}^{g}\left(s_{Tlki}V_{Tlki}\right) \quad (11)$$

where k stands for the converter phases (k=a, b, c); V_{Huki}, V_{Hlki}, V_{Tuki}, and V_{Tlki} are the voltages across i^{th} HB and TL cell capacitors in the upper and lower arms respectively; s_{Huki}, s_{Hlki}, s_{Tuki} and s_{Tlki} are the switching functions of i^{th} HB and TL cells in the upper and lower arms respectively. The above switching functions are defined as

$$s_{Huki}=\begin{cases}0\\1\end{cases},\quad s_{Hlki}=\begin{cases}0\\1\end{cases},\quad s_{Tuki}=\begin{cases}0\\1\,,\\2\end{cases}\quad s_{Tlki}=\begin{cases}0\\1\,.\\2\end{cases} \quad (12)$$

According to equivalent circuit in Fig. 7, the differential equations that describe upper arm, lower arm and ac current dynamics of the proposed TL-HMMC are:

$$L_{arm}\frac{di_{uk}}{dt}+R_{arm}i_{uk}=\frac{V_{dc}}{2}-v_k-\sum_{i=1}^{g}\left(s_{Tuki}V_{Tuki}\right)-\sum_{i=1}^{h}\left(s_{Huki}V_{Huki}\right) \quad (13)$$

$$L_{arm}\frac{di_{lk}}{dt}+R_{arm}i_{lk}=\frac{V_{dc}}{2}+v_k-\sum_{i=1}^{g}\left(s_{Tlki}V_{Tlki}\right)-\sum_{i=1}^{h}\left(s_{Hlki}V_{Hlki}\right). \quad (14)$$

The dynamics of the common mode components of arm currents i_{ck} are obtained from (13) and (14), and are described by the following first-order differential equation:

$$L_{arm}\frac{di_{ck}}{dt}+R_{arm}i_{ck}=\frac{V_{dc}-v_{ck}}{2} \quad (15)$$

$$i_{ck}=\frac{i_{uk}+i_{lk}}{2}=\frac{I_{dc}}{3}+i_{zk} \quad (16)$$

where i_{zk} are the circulating currents among the three-phase legs; v_{ck} are the common mode components of arm voltages, defined as

$$v_{ck}=\sum_{i=1}^{h}\left(s_{Huki}V_{Huki}+s_{Hlki}V_{Hlki}\right)+\sum_{i=1}^{g}\left(s_{Tuki}V_{Tuki}+s_{Tlki}V_{Tlki}\right). \quad (17)$$

Equations (15-17) indicate that the circulating current i_{zk} can be regulated by controlling the common mode component of arm voltages. In the normal operation, the capacitor voltages of HB and TL cells are all balanced and fluctuate around V_H and V_T respectively, thus the following equations are obtained:

$$\left\{\begin{array}{l}V_{Huki}=V_{Hlki}=V_H,\ k=1,2,\cdots h\\ V_{Tuki}=V_{Tlki}=V_T,\quad k=1,2,\cdots g\end{array}\right. . \quad (18)$$

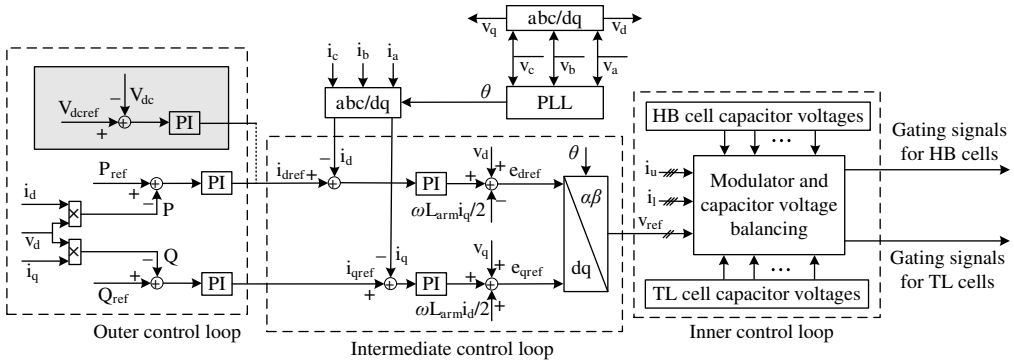

Fig. 8. Control strategy for TL-HMMC detailing inner, intermediate and outer control loops.

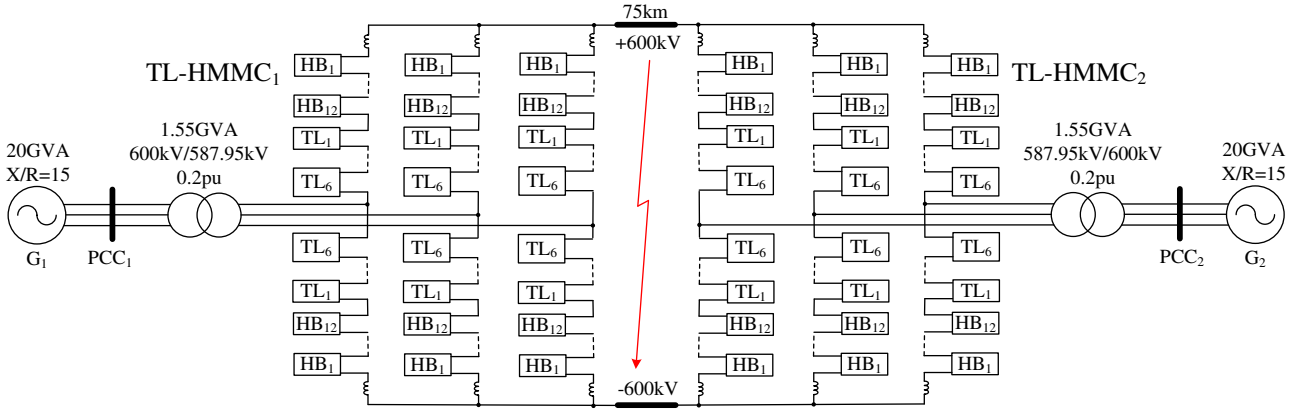

Fig. 9. Point-to-point HVDC link with three-level cell based hybrid MMCs (TL-HMMC$_1$ and TL-HMMC$_2$) where g=6 and h=12.

TABLE III
Nominal Parameters of Modeled Test System.

PARAMETER	Nominal value
dc link voltage	±600kV
capacitor voltage of HB cell	50kV
capacitor voltage of TL cell	50kV
HB cell number per arm	12
TL cell number per arm	6
capacitance of HB cell	595μF
capacitance of TL cell	595μF
arm inductance	76mH
line voltage RMS	600kV
carrier frequency	1350Hz
dc cable length	75km
pi section number of dc cable	10
dc cable resistance	9.5mΩ/km
dc cable inductance	1.43mH/km
dc cable capacitance	0.25μF/km

When (14) is subtracted from (13), the differential equations describing ac current dynamics of the proposed TL-HMMC can be derived:

$$L_{arm}\frac{di_k}{dt}+R_{arm}i_k=\sum_{i=1}^{g}\left(s_{Tlki}V_{Tlki}-s_{Tuki}V_{Tuki}\right)+\sum_{i=1}^{h}\left(s_{Hlki}V_{Hlki}-s_{Huki}V_{Huki}\right)-2v_k. \quad (19)$$

Thus, according to the coordinate transformation [32], the following equation is derived:

$$\begin{bmatrix}v_{cd}\\v_{cq}\end{bmatrix}=L_{arm}\frac{d}{dt}\begin{bmatrix}i_d\\i_q\end{bmatrix}+R_{arm}\begin{bmatrix}i_d\\i_q\end{bmatrix}+2\begin{bmatrix}v_d\\v_q\end{bmatrix}+L_{arm}\begin{bmatrix}0&-\omega\\\omega&0\end{bmatrix}\begin{bmatrix}i_d\\i_q\end{bmatrix} \quad (20)$$

where v_{cd} and v_{cq} are the controlled voltages for d and q axes respectively and can be expressed as:

$$\begin{bmatrix}V_{cd}\\V_{cq}\end{bmatrix}=V_H\begin{bmatrix}\sum_{i=1}^{h}\left(s_{Hldi}-s_{Hudi}\right)\\\sum_{i=1}^{h}\left(s_{Hlqi}-s_{Huqi}\right)\end{bmatrix}+V_T\begin{bmatrix}\sum_{i=1}^{g}\left(s_{Tldi}-s_{Tudi}\right)\\\sum_{i=1}^{g}\left(s_{Tlqi}-s_{Tuqi}\right)\end{bmatrix}. \quad (21)$$

Therefore, by regulating the voltages developed across HB and TL cells, the ac currents of the proposed TL-HMMC can be controlled in a similar manner to that of the conventional MMC. Equations (19)-(21) are required to show the impact of having TL cells on the voltage outputs. As the TL cell can generate three voltage levels, its switching function is different to that of HB cell, depicted by (12). According to (12) in addition with (21), the gating signals for HB and TL cells can be obtained by the inner control loop in Fig. 8. Note that the inner loop includes the circulating current controller and utilizes the phase-disposition (PD) carriers to generate the gating signals.

IV. DC FAULT BLOCKING AND RIDE-THROUGH OPERATION

The performance of the new hybrid MMC in high-voltage applications is assessed using a model of a point-to-point HVDC link with TL-HMMCs in the MATLAB/Simulink® environment. A reduced numbers of cells is modelled (where each cell operates at 50kV) to simplify the complexity of the model, Fig. 9. The parameters of the two converters (TL-HMMC$_1$ and TL-HMMC$_2$) are the same and listed in Table III. The equivalent cell number N is set at 24 in the test model. Thus, according to (2), the minimum TL cell number g=6, while the HB cell number h=12. To simplify the simulation, all HB and TL cells operate in the same condition and their

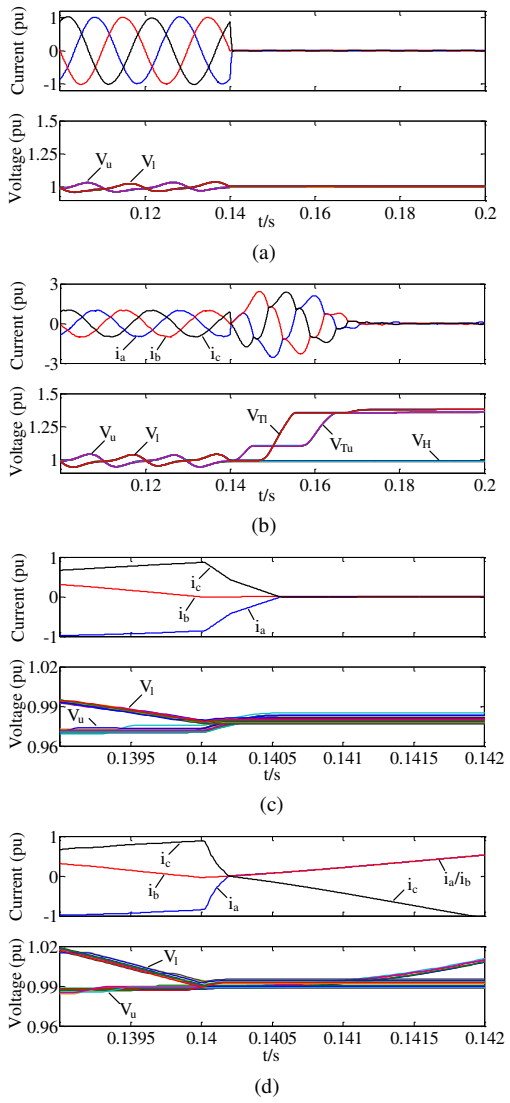

Fig. 10. Three-phase currents and cell voltages of (a) TL-HMMC, and (b) CD-HMMC, normalized to 2kA and 50kV respectively. i_a, i_b, and i_c: three-phase currents; V_u and V_l: upper and lower arm cell voltages; V_{Tu} and V_{Tl}: TL cell voltages in upper and lower arms; V_H: HB cell voltages. (c) and (d) are the expanded plots of (a) and (b) respectively to detail the current response.

maximum ripple ratios are set at 9%. According to (8), the HB and TL cell capacitance can be calculated as 595μF.

The full dc fault blocking capability is the primary advantage of the TL cell compared with the HB and the CD counterpart. DC fault blocking capability allows the system to ride-through the dc fault. Fig. 10 compares the dc fault blocking capability of the TL-HMMC with 6 TL and 12 HB cells, Fig. 10 (a) and (c), with the CD counterpart which uses the same layout (6 CD and 12 HB cells), Fig. 10 (b) and (d). Note that the CD-HMMC is the same as the TL-HMMC other than replacing the 6 TL cells with 6 CD cells. After the permanent pole-to-pole dc fault occurs at 0.14s, all the switches are turned off after 25μs from fault initiation, which is a typical time required for the system to sense the fault and act [11]. The proposed TL-HMMC suppresses the ac currents to zero immediately after the fault, without an increase in cell capacitor voltage, by virtue of the full dc fault blocking capability that the TL cells furnish the system, Fig. 10 (a) and (c). However, the dc fault cannot be fully blocked when the 6 TL cells are replaced by 6 CD cells in the test HVDC link. As shown in Fig. 10 (b) and (d), the fault currents charge the capacitors of CD cells in excess of 1.3pu (V_{Tu} and V_{Tl}) while the HB voltages (V_H) remain stable. With the voltage increases of CD cells, the fault currents eventually reduce to zero but the fault current peaks at ~3pu. The large current and voltage stresses caused by the dc fault may damage the hybrid MMC based on CD cells.

To test the dc fault ride-through operation, the next simulated scenario assumes the system shown in Fig. 9 is subjected to a solid pole-to-pole dc short circuit fault at the mid-point of the dc cable at t=1.3s, and cleared after 280ms. As previously mentioned, the two converters' switches are disabled after 25μs from fault initiation. In the pre-fault condition, TL-HMMC$_1$ transfers 1.5GW of active power from G_2 to G_1, while TL-HMMC$_2$ is set to maintain the dc voltage constant at 1200kV. During the simulation, both the two converters operate with unity power factor and their actions after dc fault depend on their pre-fault control modes. In a practical implementation, the ac circuit breakers are still needed to protect the converters and facilitate normal operation, even though the converters can block the dc faults by themselves. In this simulation, the ac circuit breakers are modelled with delay time of 40ms and the results are shown in Fig. 11.

The dc-link voltage drops to zero when the pole-to-pole dc fault occurs at t=1.3s, Fig. 11 (a). Following the fault, the gating signals of the two converters are inhibited, which activates their inherent dc fault blocking capabilities due to the TL cells in each arm. Thus, the three-phase ac currents are regulated to zero, resulting in zero power exchange between the converters and their corresponding ac grids, Fig. 11 (c-f). At t=1.58s, the dc fault is cleared and the gating signals of TL-HMMC$_2$ will be restored to charge the dc cable and build up the dc voltage. As the two converters are disconnected from the grids by ac circuit breakers, the TL cell capacitors of TL-HMMC$_2$ can be connected to the dc cables of the positive and negative poles successively at predefined intervals. Thus, the dc link voltage is increased in the step of TL cell capacitor voltage to avoid significant inrush currents and dc voltage oscillation as the dc cable capacitance recharges. Once the dc-link voltage has recovered to around rated value, the ac circuit breakers are closed and then TL-HMMC$_2$ is activated to maintain the dc voltage at the rated value. Subsequently, the gating signals of TL-HMMC$_1$ can be restored, thus allowing its active power to be ramped gradually from zero to -1.5GW, over 100ms, thereby avoiding transient oscillations.

Fig. 11 (g) to (j) present upper and lower arm currents of TL-HMMC$_1$ and TL-HMMC$_2$. These arm currents are suppressed to zero after the fault due to the dc fault blocking capability and the power switches do not suffer any overcurrents. When TL-HMMC$_2$ is reactivated at t=1.7s, its arm currents are very small due to no power transfer between ac and dc sides, see Fig. 11 (i) and (j), while the arm currents of TL-HMMC$_1$ are still zero, see Fig. 11 (g) and (h).

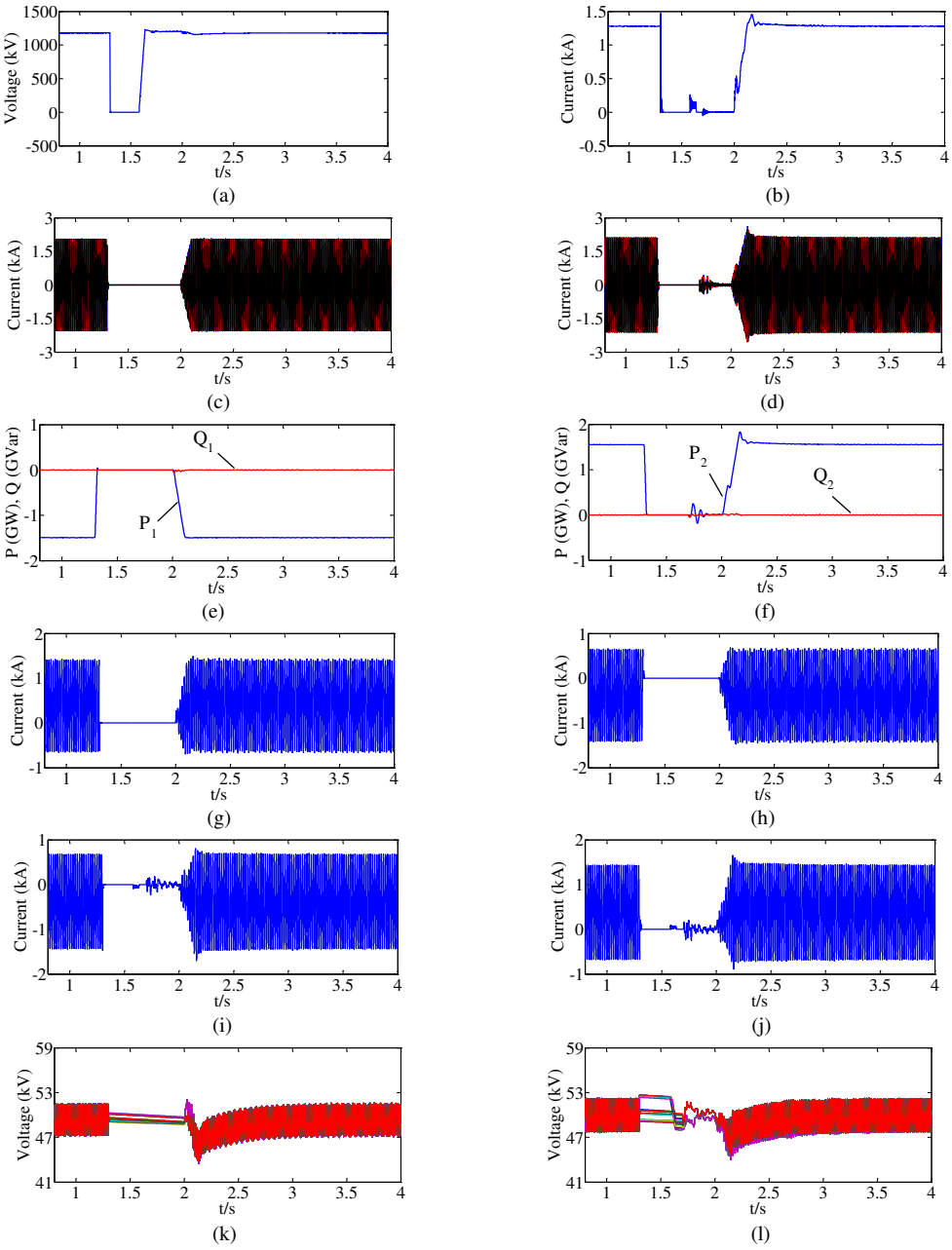

Fig. 11. DC fault ride-through waveforms. (a) DC voltage. (b) DC current. (c) Three-phase currents of TL-HMMC$_1$. (d) Three-phase currents of TL-HMMC$_2$. (e) Active and reactive powers of TL-HMMC$_1$. (f) Active and reactive powers of TL-HMMC$_2$. (g) Upper arm currents of TL-HMMC$_1$. (h) Lower arm currents of TL-HMMC$_1$. (i) Upper arm currents of TL-HMMC$_2$. (j) Lower arm currents of TL-HMMC$_2$. (k) Capacitor voltages of HB and TL cells for TL-HMMC$_1$. (l) Capacitor voltages of HB and TL cells for TL-HMMC$_2$.

Shown in Fig. 11 (k) and (l), all the capacitors of HB and TL cells remain balanced fluctuating around 50kV and the ripple ratios are around 8.92%, which is in agreement with the preset value.

Although the test system is subjected to the most severe type of dc fault (pole-to-pole dc fault), it does not suffer over-currents or over-voltages and can be restored to pre-fault operation conditions, benefitting from the full dc fault blocking capability of TL cells in the proposed TL-HMMC.

V. Conclusion

The novel TL-HMMC achieves the full dc fault blocking capability by using TL cells that utilize a clamp circuit to series-connect capacitors and insert them in the fault current path thereby reducing the fault current from the ac side to the dc side to zero. Compared to the FB counterpart, the TL cell reliability is likely to improve due to fewer shoot-through modes. The TL-HMMC uses the TL cells in combination with HB cells in each arm. Based on the conventional HB-MMC, the TL-HMMC replaces less than half of HB cells with the TL cells. The number of semiconductors and conduction losses are reduced to 66.5% and 72% of that for FB-MMC respectively, yielding lower semiconductor costs and higher efficiency. Meanwhile, the proposed topology can still ride-through the dc fault due to the full dc fault blocking capability of TL cells, which is achieved with a penalty of only 44% increase in conduction losses compared to the conventional

HB-MMC. Simulation results demonstrate the dc fault blocking capability and the improvements compared to the HB-MMC and the CD counterpart. A switching model is developed to control the proposed TL-HMMC by regulating the voltage developed across the HB and TL cells in each arm. The capacitance requirement is derived and the simulation results show that capacitor voltages of the HB and TL cells are all well balanced and within specified voltage ripple. The dc fault ride-through capability, high efficiency, robustness and low capital cost of the proposed TL-HMMC makes it attractive for application in HVDC systems.

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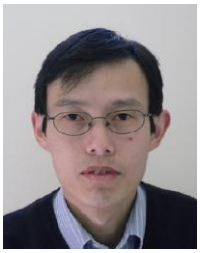
Rui Li received the M.S. and Ph.D degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2008 and 2013, respectively. Since 2013, he has been working as a research associate with University of Strathclyde in Glasgow, UK.

His research interests include HVDC transmiision system, grid integration of renewable power, power electronic converters, and energy conversion.

John E. Fletcher (M'12–SM'14) received the B.Eng. (with first class honors) and Ph.D. degrees in electrical and electronic engineering from Heriot-Watt University, Edinburgh, U.K., in 1991 and 1995, respectively. Until 2007, he was a Lecturer at Heriot-Watt University. From 2007 to 2010, he was a Senior Lecturer with the University of Strathclyde, Glasgow, U.K. He is currently a Professor with the University of New South Wales, Sydney, Australia.

His research interests include distributed and renewable integration, silicon carbide electronics, pulsed-power applications of power electronics, and the design and control of electrical machines. Prof. Fletcher is a Charted Engineer in the U.K. and a Fellow of the Institution of Engineering and Technology.



Lie Xu (M'03–SM'06) received the B.Sc. degree in Mechatronics from Zhejiang University, Hangzhou, China, in 1993, and the Ph.D. degree in Electrical Engineering from the University of Sheffield, Sheffield, UK, in 1999.

He is currently with the Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK. He previously worked in Queen's University of Belfast and ALSTOM T&D, Stafford, UK. His research interests include power electronics, wind energy generation and grid integration, and application of power electronics to power systems.

Derrick Holliday received the Ph.D. degree in electrical and electronic engineering from Heriot Watt University, Edinburgh, U.K., in 1995.

He has held full-time academic posts at the Universities of Bristol and Strathclyde. He has authored or co-authored over 70 academic journal and conference publications. He is currently leading an industrially funded research in the field of power electronics for HVDC applications, and is a coinvestigator on research programs in the fields of photovoltaic systems and the interface of renewable energy to HVDC systems. His research interests include power electronics, and electrical machines and drives.

B. W. Williams received the M.Eng.Sc. degree from the University of Adelaide, Australia, in 1978, and the Ph.D. degree in electrical and electronic engineering from Cambridge University, Cambridge, U.K., in 1980.

After seven years as a Lecturer at Imperial College, University of London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at Strathclyde University, UK. His teaching covers power electronics (in which he has a free internet text) and drive systems.

His research activities include power semiconductor modelling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors to industrial electronics.