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Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems

Grain Philip Adam and Innocent Ewean Davidson

Abstract—This paper presents the theoretical basis of the control strategy that allows the cell capacitor voltage regulation of the full-bridge modular multilevel converter (FB-MMC) to be controlled independent of its dc link voltage. The presented control strategy permits operation with reduced dc link voltage during permanent pole-to-ground dc fault, and controlled discharge and recharge of the HVDC links during shutdown and restart following clearance of temporary pole-to-pole dc faults. Additionally, it allows voltage source converter based HVDC links that employ FB-MMC to be operated with both positive and negative dc link voltages. This feature is well suited for hybrid HVDC networks, where the voltage source converters are operated alongside the line commutating current source converters, without any compromise to the power reversal at any terminals. The usefulness of the presented control strategy is demonstrated on full-scale model of HVDC link that uses FB-MMC with 101 cells per arm, considering the cases of pole-to-ground and pole-to-pole dc faults.

Index-Terms— DC fault reverse blocking, full and half bridge modular multilevel converter, High-voltage dc transmission systems, and multi-terminal high-voltage dc networks.

I. INTRODUCTION

Recently there are several voltage source converter (VSC) topologies being proposed aim to improve dc fault survival of point-to-point and multi-terminal HVDC transmission systems[1-8]. Half-bridge modular multilevel converter (HB-MMC) is widely adopted in recent years; because its distributed cell capacitors do not contribute discharge current to dc fault when converter switches are blocked [7, 9-18]. As a result the magnitude of transient dc fault current is greatly reduced compared to that of conventional VSC topologies with concentrated input dc link capacitors such as two-level and neutral-point clamped converters[3, 4, 6, 9, 19-21]. However, HB-MMC is unable to stop ac grid contribution to the dc fault current through its freewheeling diodes. This makes its dc fault survival is increasingly relies on the availability of fast acting dc circuit breakers as suggested in [9, 22-25]. Otherwise, HB-MMC freewheeling diodes may fail from excessive current stresses. FB-MMC offers an invaluable feature of dc fault current limiting, and shares many other attributes with HB-MMC; but it has been widely dismissed on the ground of high semiconductor losses [22, 26-31].

Mixed cells MMC (50% of the cells are half-bridge and remaining 50% are full-bridge) is suggested as an alternative to FB-MMC in attempt to achieve dc fault current limiting feature at reduced semiconductor losses [5, 32]. This approach is appeared to be attractive because it combines the attributes of both HB-MMC and FB-MMC such as modularity and internal fault management. Alternative arm modular multilevel converter (AA-MMC) discussed in [3, 7, 8, 33, 34] offers dc fault current limiting feature with similar level of semiconductor losses as mixed cells MMC, but with smaller footprint[5, 35]. However, smooth current commutation between upper and lower arms of the AA-MMC is seemed to be challenging, especially when AA-MMC exchanges large reactive power with the ac grid. Additionally, AA-MMC is expected to have large transient dc fault current from discharge of its concentrated input dc link capacitor as dc link voltage collapses during dc short circuit faults. References [4, 5] have shown that the three-level and five-level cells MMCs presented in [23, 36-38] offer dc fault limiting feature, with similar level of semiconductor losses and converter footprint as the mixed cells MMC. But they acquire dc fault current limiting feature at greater complexity of the control and power circuit compared to mixed cells MMC.

This paper explores manipulation of insertion function dc bias to enable reduced dc voltage operation of the HVDC links that employ FB-MMC during permanent pole-to-ground dc faults, and to facilitate controlled discharge and recharge of the dc link during system shutdown and restart following clearance of temporary dc faults. Additionally, this paper uses a generic electromagnetic model of the FB-MMC to demonstrate the benefits of manipulation insertion function dc bias at system level, considering the case of full-scale HVDC link, where each converter terminal is a FB-MMC with 101 cells per arm. It has been shown that the adjustment of the insertion function dc bias improves transient response of the HVDC link being studied, including its dc fault ride through capability.

II. FULL-BRIDGE MODULAR MULTILEVEL CONVERTER (FB-MMC)

A) Theoretical basis of FB-MMC modulation

Figure 1 shows a generic three-phase FB-MMC with ' N ' cells per arm and input dc link voltage of V_{dc} when it is connected to ac grid through an interfacing transformer. Assume the voltage drops in the upper and lower arm reactors are negligible compared to V_{dc} , the output phase voltage at output pole ' a ' relative to supply mid-point ' o '

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can be expressed as: $v_{a0}(t) = \frac{1}{2}V_{dc} - \gamma \sum_{j=1}^N v_{cj}$, where v_{cj}

represents capacitor voltage of cell j^{th} and γ is insertion or modulation function. Insertion function for the FB-MMC upper arm is $\gamma(t) = \frac{1}{2}(\alpha_d - m \sin(\omega t + \delta))$, where ‘ m ’ is the modulation index; ‘ α_d ’ stands for insertion function dc bias; and ‘ δ ’ is the phase shift between phase ‘a’ fundamental voltage at converter terminal ‘ v_{ao} ’ and voltage ‘ v_a ’ at the point of common coupling. Recently, it has been recognized that the cell capacitor voltages of the full-bridge MMC can be regulated independent of the dc link voltage, should bipolar capability of each individual FB cell is fully exploited[22]. This allows insertion function ‘ γ ’ of the FB-MMC and its dc component to be varied over extended range of $-1 \leq \gamma \leq 1$ and $-1 \leq \alpha_d \leq 1$ respectively. When the sum of the cell capacitor voltages in each MMC arm is regulated at ‘ V_{cref} ’, the voltage developed across upper and lower arms of phase ‘a’ are:

$$v_{a1}(t) = \frac{1}{2}V_{dc} - \frac{1}{2}mV_{cref} \sin(\omega t + \delta) = \frac{1}{2}V_{cref} [\alpha_d - m \sin(\omega t + \delta)] \quad \text{and}$$

$$v_{a2}(t) = \frac{1}{2}V_{dc} + \frac{1}{2}mV_{cref} \sin(\omega t + \delta) = \frac{1}{2}V_{cref} [\alpha_d + m \sin(\omega t + \delta)],$$

where $\alpha_d = V_{dc}/V_{cref}$. Observe that when ‘ V_{cref} ’ is regulated close or equal to dc link voltage (V_{dc}) as it will be during normal operation for practical reasons, $\alpha_d \approx 1$ as in HB-MMC case (all cells are inserted with positive polarity); $\alpha_d \approx 0$ when $V_{dc} \approx 0$ during pole-to-pole dc short circuit fault (50% of cells are inserted with positive polarity and remaining 50% with negative polarity); and $\alpha_d = -1$ when polarity of the input dc link voltage is reversed (all cells to be inserted with negative polarity). When the cell capacitor voltage regulation is decoupled from the converter input dc link voltage as being pursued in this paper, the maximum peak fundamental voltage can be synthesized during normal operation is

$$V_{m1} = |v_{a0}(t)| = \left| \frac{1}{2}V_{dc} - \gamma \sum_{j=1}^N v_{cj} \right| = V_{cref} - \frac{1}{2}V_{dc}, \quad \text{with } \gamma = 1 \text{ or } -1$$

(positive γ corresponds to number of cell capacitors to be inserted with positive polarity, and the opposite is true). Notice that when the dc link voltage collapses to zero during pole-to-pole dc fault, insertion function is limited to $-\frac{1}{2} \leq \gamma \leq \frac{1}{2}$; and in this case, the maximum peak fundamental voltage can synthesized is $\frac{1}{2}V_{cref}$, which is almost the same as in normal operation should ‘ V_{cref} ’ is set to be equal to nominal input dc operating voltage ‘ V_{dc0} ’. This shows when cell capacitor voltage regulation of the FB-MMC is decoupled from the input dc link voltage level, the cell capacitors of each arm act as virtual dc link, including during collapse of the actual dc link voltage. This permits ac voltage at converter terminal to be synthesized independent of input dc link voltage. This feature allows FB-MMC to be controllable even when the input dc link is lower than the grid voltage. Notice that the insertion function of each arm varies within $0 \leq \gamma \leq 1$ and $-1 \leq \gamma \leq 0$ during normal operation with positive and negative input dc link voltage respectively. The above discussions have shown that the input dc link voltage of the FB-MMC can be varied from V_{dc0} to $-V_{dc0}$,

without loss of converter control, benefiting of the use of the cell capacitors of each converter arm as a virtual dc link.

B) Converter control

Figure 2 summaries control systems of the FB-MMC being used in this paper. Observe that the loops that regulate AC power/or dc link voltage, reactive power/or ac voltage and ac currents in synchronous reference frame set the insertion function ac component, and provide over-current protection during ac network faults. Whilst the loops that regulate cell capacitor voltages independent of converter dc link and common mode currents that flow in the converter arms set the insertion function dc bias, and provide over-current protection during dc side faults. The most inner loop uses amplitude (staircase) modulation to generate the gating signals for switches of the FB-MMC, with Marquardt capacitor voltage balancing that rotates the cell capacitors based on their voltage magnitudes and polarity of the arm currents. The loops that regulate cell capacitor voltages are designed as follows:

A) Common mode current

Differential equations that describe the dynamics of FB-MMC upper and lower arm currents for phase ‘a’ are:

$$L_d \frac{di_{a1}}{dt} = \frac{1}{2}V_{dc} - v_{a1} - R_d i_{a1} - v_{a0} \quad (1)$$

$$L_d \frac{di_{a2}}{dt} = \frac{1}{2}V_{dc} - v_{a2} - R_d i_{a2} + v_{a0} \quad (2)$$

Where i_{a1} and i_{a2} are phase ‘a’ upper and lower arm currents; v_{a1} and v_{a2} are voltages developed across converter upper and lower arms cell capacitors of phase ‘a’; and R_d and L_d are resistance and inductance of the upper and lower arm reactors. After adding (2) to (1) and recall that v_{a1} and v_{a2} are $v_{a1} = \frac{1}{2}V_c [m_d - m \sin(\omega t + \delta)]$ and $v_{a2} = \frac{1}{2}V_c [m_d + m \sin(\omega t + \delta)]$, equation (3) is obtained:

$$L_d \frac{di_{com}}{dt} = \frac{1}{2}V_{dc} - \frac{1}{2}m_d V_c - R_d i_{com} \quad (3)$$

Where the common mode current i_{com} is: $i_{com} = \frac{1}{2}(i_{a1} + i_{a2})$ and

$$V_c = \frac{1}{2} \left[\sum_{j=1}^N v_{cuj} + \sum_{j=1}^N v_{clj} \right].$$

$u_{com} = \frac{1}{2}V_{dc} - \frac{1}{2}m_d V_c$ and u_{com} will be obtained from proportional-integral (PI) controller as:

$$u_{com} = k_p (i_{com}^* - i_{com}) + k_i \int (i_{com}^* - i_{com}) dt \quad (4)$$

After replacing the integral part of (4) by z_{com} , and further algebraic and Laplace manipulations, the following transfer

function is obtained: $\frac{i_{com}(s)}{i_{com}^*(s)} = \frac{\frac{k_p}{L_d} s + \frac{k_i}{L_d}}{s^2 + \frac{(k_p + R_d)}{L_d} s + \frac{k_i}{L_d}}$. This

transfer function allows the initial controller gains to be selected as $k_i = \omega_n^2 L_d$ and $k_p = 2\xi \omega_n L_d - R_d$ for given time-domain specifications such as settling time or using frequency domain. From the above definition of the u_{com} , m_d is obtained considering the feed-forward term of $\frac{1}{2}V_{dc}$ as: $m_d = 2(\frac{1}{2}V_{dc} - u_{com})/V_c$.

B) Cell capacitor voltage

The differential equations that describe the cell capacitor dynamics of the upper and lower arms of phase ‘a’ as an

example are: $\frac{d}{dt} \sum_{j=1}^N \frac{1}{2} C v_{cu}^2 = i_{a1} \times \gamma_1^a \sum_{j=1}^N v_{cu}$ and

$\frac{d}{dt} \sum_{j=1}^N \frac{1}{2} C v_{cl}^2 = i_{a2} \times \gamma_2^a \sum_{j=1}^N v_{cl}$. With proper control, the cell

capacitor voltages of the upper arm vary together with relatively small errors, and the same is applicable to the lower arm. Thus, above equations can be written as:

$$\frac{d}{dt} \left(N \times \frac{1}{2} C v_{cu}^2 \right) = i_{a1} \times \gamma_1^a \times N \times v_{cu} \Rightarrow C \frac{dv_{cu}}{dt} = i_{a1} \times \gamma_1^a \quad (5)$$

$$\frac{d}{dt} \left(N \times \frac{1}{2} C v_{cl}^2 \right) = i_{a2} \times \gamma_2^a \times N \times v_{cl} \Rightarrow C \frac{dv_{cl}}{dt} = i_{a2} \times \gamma_2^a \quad (6)$$

Recall that $i_{a1} = I_d + \frac{1}{2} i_a$ and $i_{a2} = I_d - \frac{1}{2} i_a$, $i_a = I_m \sin(\omega t + \varphi)$.

With insertion functions of the upper and lower arms of phase ‘a’ (γ_1^a and γ_2^a) defined as $\gamma_1^a = \frac{1}{2}(\alpha_d - m \sin \omega t)$ and

$\gamma_2^a = \frac{1}{2}(\alpha_d + m \sin \omega t)$, $\alpha_d I_d = \frac{1}{4} m I_m \cos \varphi$; thus, equation (7) is obtained by adding (5) and (6):

$$C_e \frac{d}{dt} (V_{c1} + V_{c2}) = i_{a1} \gamma_1^a + i_{a2} \gamma_2^a = \frac{1}{4} m I_m \cos(2\omega t + \varphi) \quad (7)$$

Where $V_{c1} = N \times v_{cu}$ and $V_{c2} = N \times v_{cl}$; and $C_e = C/N$. Observe that the R.H.S of equations (5) and (6) do not contain dc component, and R.H.S of equation (7) that describes dynamic of the upper and lower arms contains only 2nd harmonic. These indicate that the converter cell capacitor voltage balancing can be maintained around the dc link voltage, and but the cell capacitor voltage level is coupled to the dc link voltage. In order to decouple the cell capacitor voltage level from the dc link voltage level, theoretical equation (7) is abandoned in favour empirical equation in (8):

$$C_e \frac{d}{dt} \frac{1}{2} (V_{c1} + V_{c2}) = \frac{1}{2} (i_{a1} + i_{a2}) = i_{com} \quad (8)$$

Where $C_e = C/N$ is the equivalent capacitance per arm, and C is the capacitance per cell. Observe that the R.H.S of equation (8) is a common mode current of the upper and

lower arm of phase ‘a’ that contains dc component, which provides the ability to change the energy (or voltage) level of the cell capacitors independent of the converter input dc link voltage. The reference common mode current i_{com}^* is obtained from PI controller that regulates the cell capacitor voltages as:

$$i_{com}^* = \alpha_p \left[V_{cref} - \frac{1}{2} (V_{c1} + V_{c2}) \right] + \alpha_i \int \left[V_{cref} - \frac{1}{2} (V_{c1} + V_{c2}) \right] dt \quad (9)$$

The initial gains for the PI controller in (9) are obtained from $\alpha_p = 2\xi_1 \omega_{n1} C_e$ and $\alpha_i = \omega_{n1}^2 C_e$, with damping and natural frequency ξ_1 and ω_{n1} are decided based on time domain specification as previously stated.

Based on above discussions, the control structure for the cell capacitor and common mode current regulation depicted in Figure 2 is constructed. The readers are advised to refer to reference [39] for details of the control design for the remaining controllers depicted in Figure 2.

III. PERFORMANCE EVALUATION

Figure 3 shows full-scale symmetrical mono-pole HVDC link that uses FB-MMC, with each converter terminal VSC₁ and VSC₂ is rated at 1000MVA, ± 320 kV dc link voltage, and connected to 400kV ac network through 1000MVA, 300kV/400kV interfacing transformers. Converter terminals VSC₁ and VSC₂ are modelled using FB-MMC electromagnetic transient model described in [39], but in this paper, number of FB sub-modules in each arm is set to 101. Generic control system displayed in Figure 2 is used to control VSC₁ and VSC₂, with no dedicated controller for 2nd harmonic suppression in converter arms is incorporated in attempt to reduce the overall system complexity.

VSC₁ and VSC₂ are configured to regulate active power and dc voltage level at 640kV (pole-to-pole) respectively, with reactive powers at both stations are set to zero. The parameters of the HVDC link in Figure 3 are listed in Table 1. The dc fault survival of the HVDC link in Figure 3 is examined when the cell capacitor voltage balancing of the FB-MMCs used in VSC₁ and VSC₂ is decoupled from the dc link during pole-to-ground and pole-to-pole dc faults (with and without converter blocking).

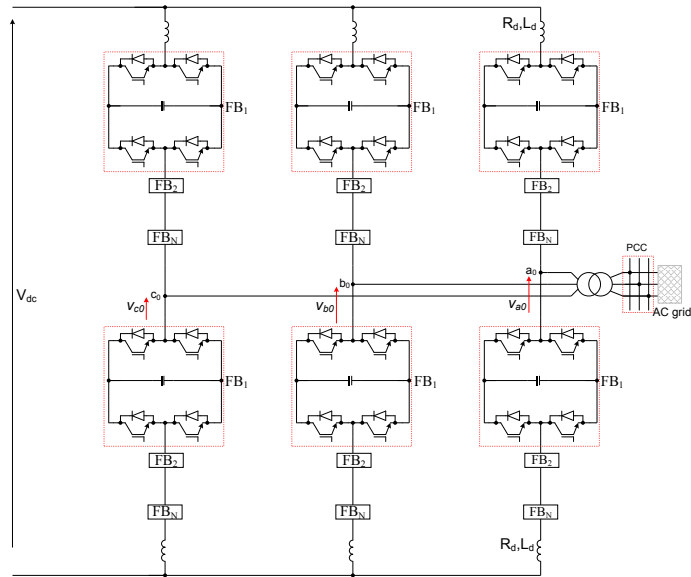


Figure 1: Generic three-phase full-bridge modular multilevel converter

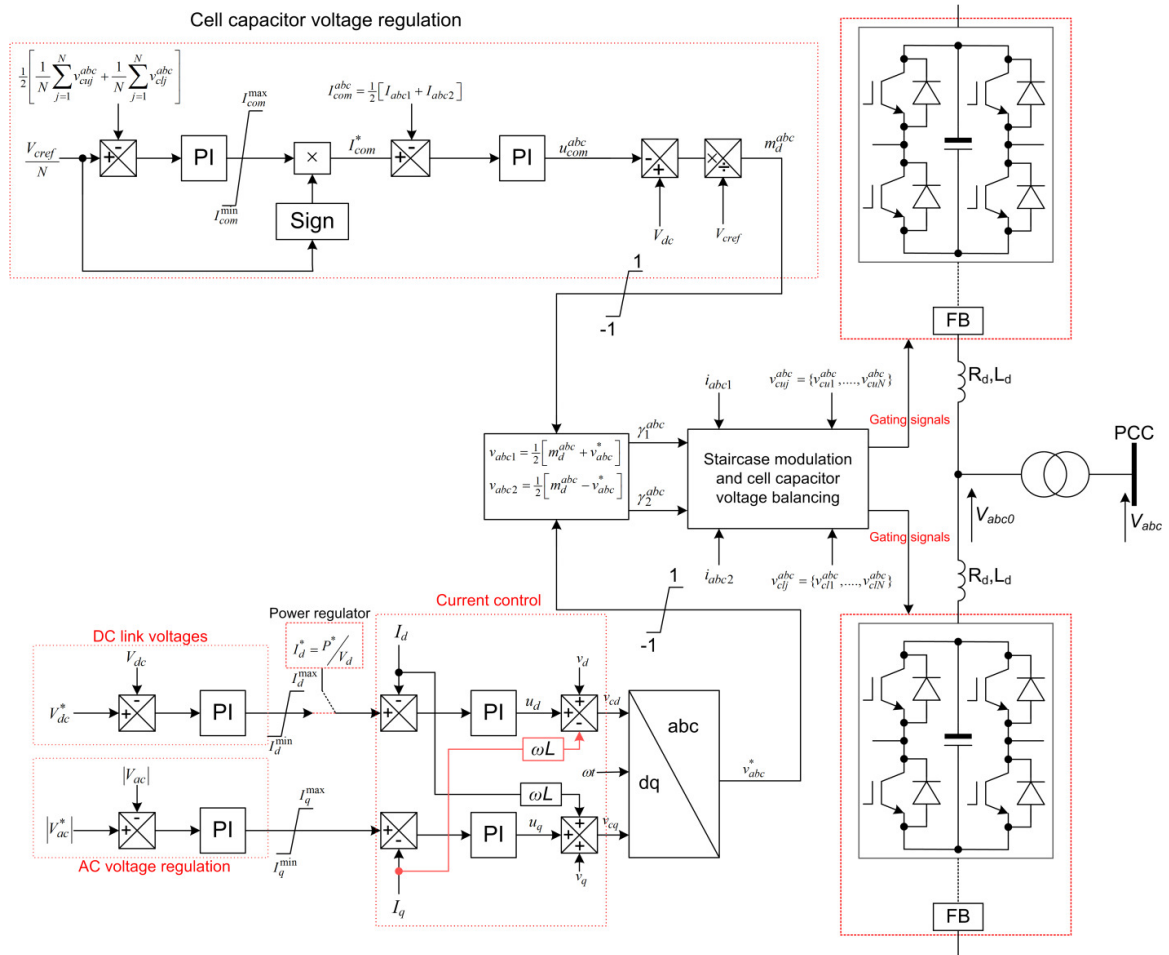


Figure 2: Generic control systems of the FB-MMC

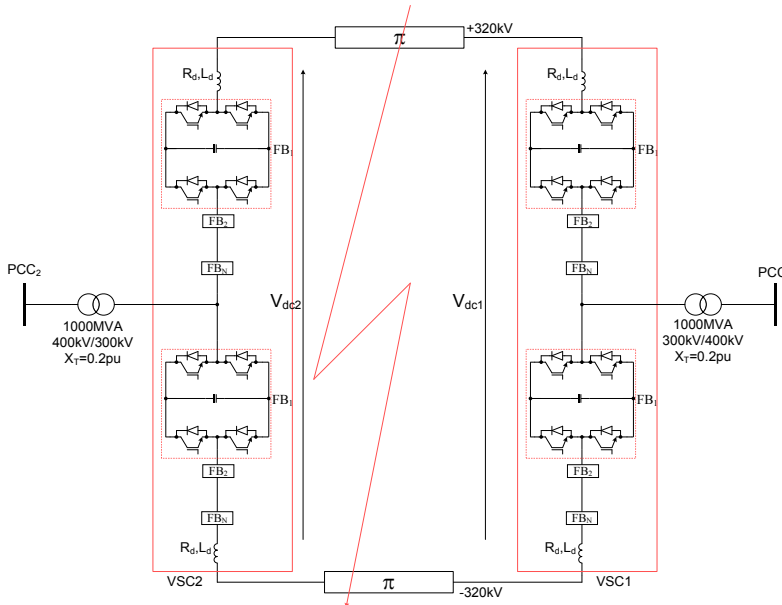


Figure 3: Electromagnetic transient based full-scale model of FB-MMC HVDC link with 101 cells per arm

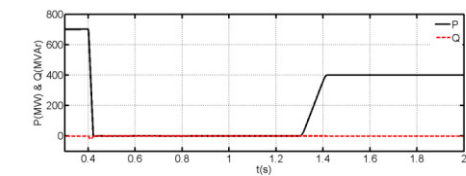
Table 1: Summary of system parameters

Parameter	Value
dc link voltage (Vdc)	±320kV
Converter rated ac side voltage	300kV
Converter rated power	1052MVA
Converter rated active power	±1000MW
Converter rated reactive power	±328MVar
Number of cells per arm	101
Capacitance per cell	4mF
Arm reactance	50mH
Interfacing transformer rated power	1052MVA
Interfacing transformer voltage ratio	300kV/400kV
Interfacing transformer per unit leakage reactance	0.2pu
Interfacing transformer per unit resistance	0.0002pu
DC cable resistance	0.01Ω/km
DC cable inductance	0.8mH/km
DC cable capacitance	0.25μF/km

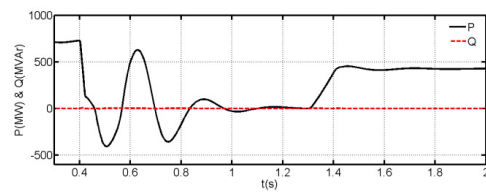
(A) Pole-to-ground dc fault

This section exploits some of the silent features of the FB-MMC discussed in section II to enable continue operation of a symmetrical mono-pole HVDC when it is exposed to a permanent pole-to-ground dc fault. For illustration, the HVDC link in Figure 3 is initially set to export 700MW from the point of common coupling (PCC₁) to PCC₂. At time $t=0.4s$, a permanent dc fault is applied at the middle of the dc cable (positive pole) that connects VSC₁ to VSC₂, and afterward VSC₁ is immediately commanded to reduce the transmitted power from PCC₂ and PCC₁ to zero, and then restored gradually to 400MW after the transients associated with the dc faults have died out. Because the surge arresters being used in such HVDC links are not rated for continuous operation (1.5 to 2 times of the rated voltage for 10ms ~ 20ms in the worse cases), VSC₂ is commanded after 45ms (for illustration only) from the fault initiation to reduce dc link voltage gradually to 320kV, with VSC₁ and VSC₂ remain unblocked. Selected waveforms obtained from this case are displayed in Figure 4. Figure 4 (a) and (b), and (c) and (d) show active and reactive powers VSC₁ and VSC₂

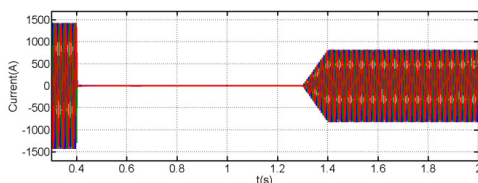
exchange with PCC₁ and PCC₂, and their corresponding ac side currents measured at PCC₁ and PCC₂. Figure 4 (e) and (f) show arm currents of the VSC₁ and VSC₂. Figure 4 (g) and (h) show samples of the dc link voltage (pole-to-pole) and current measured at the terminals of VSC₂. Observe that a successful reduction of the dc link voltage is achieved, with the current stresses in VSC₁ and VSC₂ upper and lower arms and in their ac sides remain fully controllable. This illustrative example has demonstrated the possibility of continuous operation of the FB-MMC HVDC link when one of its positive or negative poles is subjected to permanent pole-to-ground dc fault. Figure 4 (i) and (j) show the cell capacitor voltages of VSC₁ and VSC₂ are decoupled from the dc link voltage and well regulated around (640kV/101≈6.37kV) as in pre-fault condition. The significance of this work is that it addresses the main weakness in all symmetrical mono-pole HVDC links currently in operation (inability to operate during pole-to-ground dc fault as the surge arresters and dc cable insulation of the healthy pole will breakdown from excessive voltage stresses, see Figure 4 (k)).



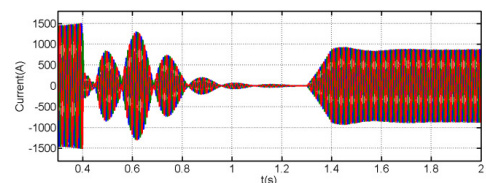
(a) Active and reactive power VSC₁ exchanges with PCC₁



(b) Active and reactive power VSC₂ exchanges with PCC₂



(c) AC currents VSC₁ injects into PCC₁



(d) AC currents VSC₂ injects into PCC₂

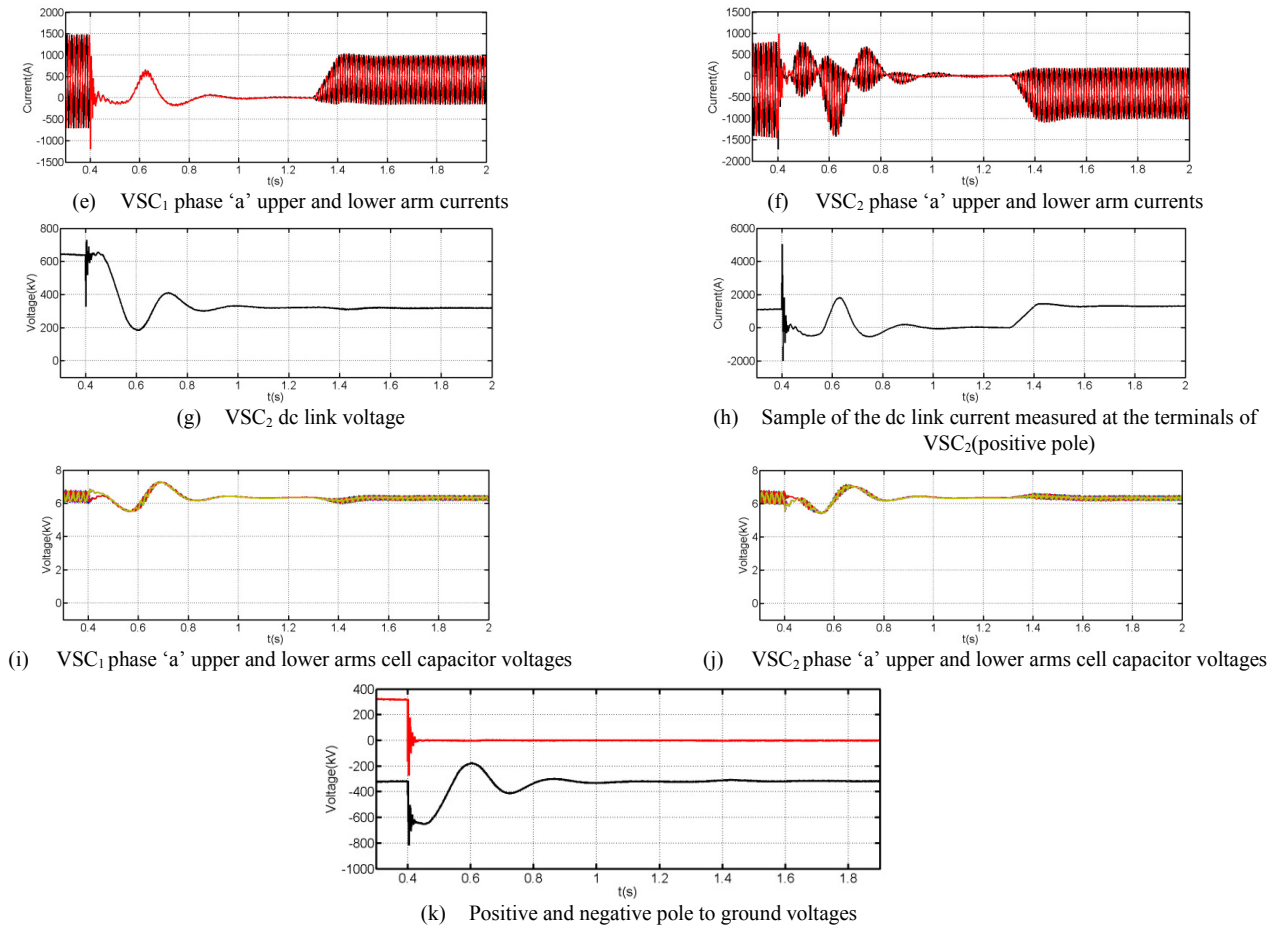


Figure 4: Waveforms obtained when HVDC link based on FB-MMC is subjected to pole-to-ground dc fault at the middle of the link

(B) Pole-to-pole dc fault

(i) When VSC_1 and VSC_2 are blocked during fault

This section exploits the dc fault reverse blocking and controlled recharge capabilities of the FB-MMC to improve dc fault survival of symmetrical mono-pole HVDC link, while keeping the current and voltage stresses on converter stations switching devices and passive components within tolerable limits. For illustration, the HVDC link in Figure 3 is subjected to a temporary pole-to-pole dc fault at the middle of the dc line that connects VSC_1 to VSC_2 at $t=0.4s$, with 100ms fault duration. In pre-fault condition, the HVDC link in Figure 3 is set to export 700MW from PCC_1 to PCC_2 , and the transmitted power is reduced to zero and converter switches are blocked immediately when the fault is detected. After fault clearance at $t=0.5s$, VSC_1 and VSC_2 switches are unlocked, and VSC_2 is commanded to perform a controlled recharge of the dc link to 640kV before power transmission is resumed. At $t=1.3s$, VSC_1 is commanded to restore the power exchange between the two ac networks gradually to pre-fault value.

Figure 5 (a) and (b), (c) and (d), and (e) and (f) show active and reactive powers VSC_1 and VSC_2 exchange with their corresponding ac networks, ac current waveforms measured at PCC_1 and PCC_2 , and arm currents of the VSC_1 and VSC_2 respectively. These waveforms have shown that the link being studied is able to recover from pole-to-pole dc fault, with currents at PCC_1 and PCC_2 , and switching devices of VSC_1 and VSC_2 are tightly regulated within the levels that can be tolerated by the commercially available

IGBTs. Figure 5 (g) and (h) show samples of the dc link voltage and current measured at the terminals of VSC_2 . Observe that the HVDC link being studied briefly lost control due to the transients experienced when converter switches are unblocked promptly and the delay time introduced by the response time of individual controllers, and shortly afterward the link is able to perform a controlled recharge of the link, with the current associated with the recharging of the dc line stray capacitors are tightly controlled, including that in the converter arms. Figure 5 (i) and (j) show the voltage balance of the cell capacitors of VSC_1 and VSC_2 are well maintained, including during controlled recharge of the dc link.

(ii) When VSC_1 and VSC_2 are not blocked during dc fault

This subsection investigates the possibility of riding a temporary pole-to-pole dc fault studied in subsection B-(i) when VSC_1 and VSC_2 are not blocked, and their cell capacitor voltages are exploited in a manner to be seen by their respective ac sides as virtual dc links. Exploiting this feature allows the ac currents VSC_1 and VSC_2 exchange with PCC_1 and PCC_2 to be controllable despite the collapse of their physical dc link voltage. Figure 6 displays selected waveforms obtained when the simulated case in B-(i) is repeated, with VSC_1 and VSC_2 remain unblocked. Figure 6 (a) and (b) show with the control system in Figure 2, the HVDC link being studied is able to ride-through solid pole-to-pole dc fault, with ac currents associated with the discharge and recharge of the dc line stray capacitors are

tightly controlled. But the plots for the upper and lower arm currents of VSC₁ and VSC₂ in Figure 6 (c) and (d) have shown that the current stresses in the converter arms, which will be seen by the semiconductor switches, are dominated by the transient discharge currents of the dc line stray capacitors. Figure 6 (e) and (f) show when VSC₁ and VSC₂ are not blocked, their cell capacitor voltages exhibit large disturbances as result of large unipolar dc fault currents that flow through the sub-module capacitors. Although the

simulated case (B)-(ii) has shown that the semiconductor switches are less likely to survive such excessive current stresses when converters are not blocked, riding dc fault without converter blocking may be possible in relatively short overhead HVDC links, where the line distributed capacitances are negligible. Figure 6 (g) and (h) show sample of the dc link current and dc link voltage measured at VSC₂ terminals.

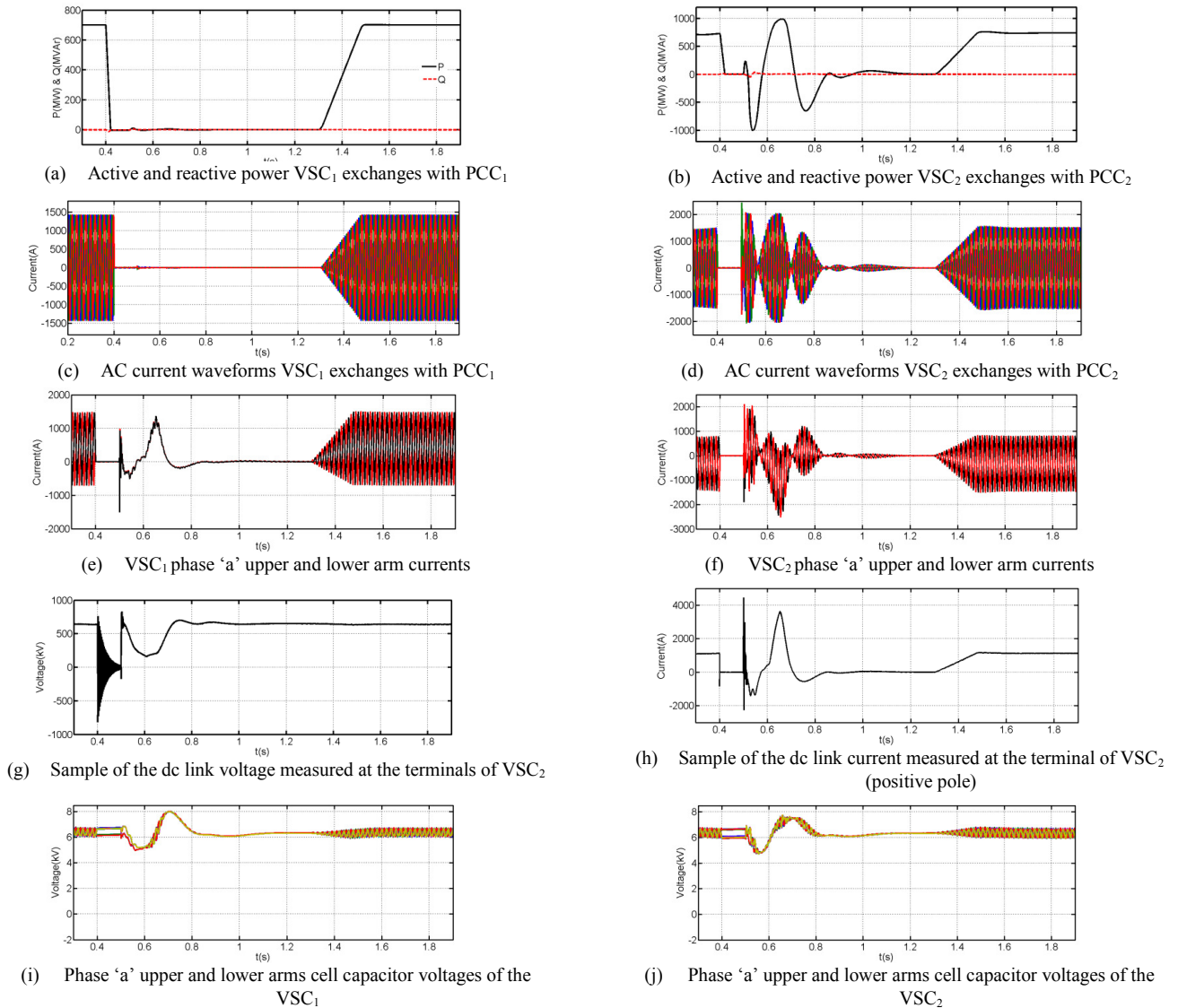
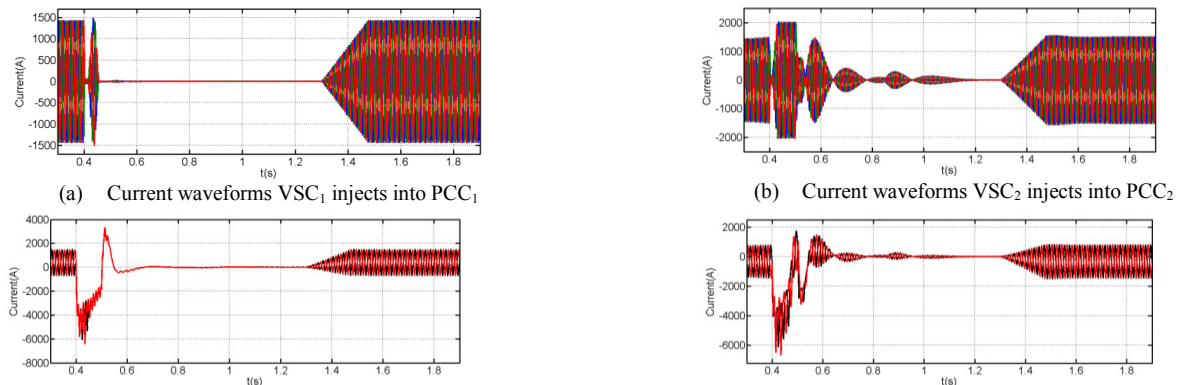


Figure 5: Waveforms obtained when HVDC link based on FB-MMC is subjected to pole-to-pole dc fault at the middle of the link



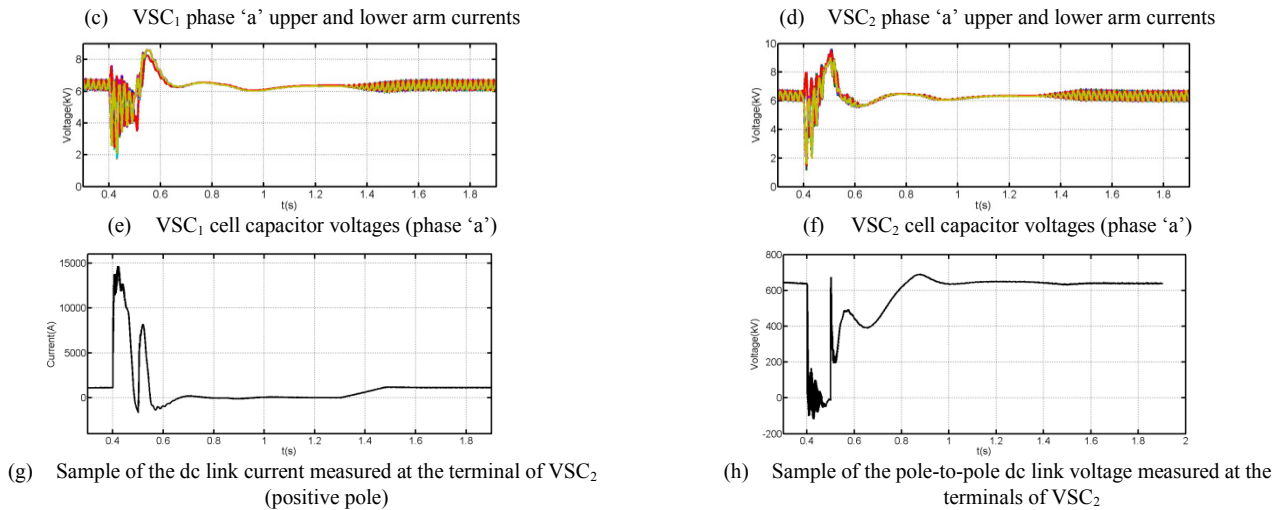


Figure 6: Waveforms obtained when HVDC link based on FB-MMC is subjected to pole-to-pole dc fault at the middle of the link, with VSC1 and VSC2 remain unblocked during fault

IV. CONCLUSIONS

This paper presented comprehensive discussions of the underlying theory, which is later exploited to control FB-MMC when used in a symmetrical mono-pole HVDC link in attempt to improve its dc fault survival. It has been shown that when the regulation of the cell capacitor voltages is decoupled from the converter dc link voltage, converter stations of the HVDC remain controllable even though when its physical dc link voltage is collapsed to zero. Moreover, it has been shown that the number of sub-modules to be inserted in power path with positive and negative polarities is directly link to the dc bias magnitude of the insertion function of each phase, and this feature is exploited to enable operation of FB-MMC HVDC link with variable dc voltage. The theoretical discussions presented in section II have been substantiated using simulation of full-scale HVDC link that uses FB-MMC with 101 sub-modules per arm, considering the cases of pole-to-ground and pole-to-pole dc faults. The presented results have shown that the FB-MMC offers number of invaluable features that are well suited for point-to-point and multi-terminal HVDC transmission systems.

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