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Electrodeposition and characterisation of CdS thin films using thiourea precursor for application in solar cells

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Abstract

CdS thin films have been successfully electrodeposited on glass/FTO substrates using acidic and aqueous solution of CdCl₂.xH₂O and thiourea (SC(NH₂)₂). The electrodeposition of CdS thin films were carried out potentiostatically using a 2-electrode system. The prepared films were characterised using X-ray diffraction (XRD), Raman spectroscopy, Scanning electron microscopy (SEM), Atomic force microscopy (AFM), Photoelectrochemical (PEC) cell measurements, Electrical resistivity measurements and UV-Vis spectrophotometry to study their structural, compositional, morphological, electrical and optical properties, respectively. The structural studies show that the asdeposited and annealed CdS layers are polycrystalline with hexagonal crystal structure and preferentially oriented along (200) planes. The optical studies indicate that the ED-CdS layers have direct bandgaps in the range (2.53-2.58) eV for the as-deposited and (2.42-2.48) eV after annealing at 400°C for 20 minutes in air. The morphological studies show the good coverage of the FTO surface by the CdS grains. The average grain sizes for the as-deposited and annealed layers were in the range \sim (60-225) nm. These grains or clusters are made out of smaller nano crystallites with the sizes in the range \sim (11-33) nm. The electrical resistivity shows reduction as thickness increases. The resistivity values for the asdeposited and annealed layers were in the range $(0.82-4.92)\times10^5 \Omega$ cm. The optimum growth voltage for the CdS thin films was found to be at the cathodic potential of 797 mV with respect to the graphite anode. No visible precipitations of elemental S or CdS particles were observed in the deposition electrolyte showing a stable bath using thiourea during the growth.

Keywords: Electrodeposition, CdS, thin film, semiconductor, window layer, thiourea

1 Introduction

Cadmium sulphide (CdS) is a metal chalcogenide semiconductor with a wide band gap of 2.42 eV at room temperature (300 K) [1]. This material has been widely used in many applications such as optoelectronic devices, semiconductor lasers, sensors and solar cells [2-5]. Different techniques have been used to deposit CdS thin films including close-space sublimation (CSS) [6], metal organic chemical vapour deposition (MOCVD) [7], vacuum evaporation [8], spray pyrolysis [9], chemical bath deposition (CBD) [10] and electrodeposition (ED) [11]. These growth techniques have been used to grow crystalline and polycrystalline CdS thin films. However, some of these growth techniques require expensive and complex equipment. In addition, in solution growth techniques such as CBD, the production of large Cd-containing waste is a disadvantage. Electrodeposition of thin films semiconductor using aqueous solution has attracted lots of attention due to its simplicity, low-cost growth conditions, scalability and manufacturability. Other advantages of electrodeposition technique using aqueous solution can be related to ease of compositional variation of thin films and production of high quality large-area semiconductor materials in a continuous manufacturing process [12].

In the literature, the electrodepositions of CdS thin films have been carried out from acidic and aqueous solutions using 2-electrode and 3-electrode systems. In these reports different sulphur precursors such as sodium thiosulphate $(Na_2S_2O_3)$ [13-16], ammonium thiosulphate $(NH_4)_2S_2O_3$ [17] and thioacetamide (C_2H_5NS) [18] have been used. The CdS thin films grown by these precursors were polycrystalline, homogeneous, transparent and showed good adhesion to the underlying transparent conduction oxide (TCO) substrates. However, the major disadvantages of these precursors are the precipitation of elemental S and CdS particles in the solution during the growth which can affect the quality of the deposited thin films. Electrodeposition of the CdS from acidic and aqueous solutions using thiourea (TU) precursor has been able to overcome this disadvantage. In the literature, there is only one report on the cathodic electrodeposition of CdS thin films from TU precursor using 3-electrode system [19].

This paper presents the cathodic electrodeposition of CdS thin films from acidic and aqueous solution using TU precursor. The electrodeposition of CdS was carried out potentiostatically using 2-electrode system and the main aim of this research is to establish an electrodeposition method with high stability of the electrolyte, without forming precipitation. Such a process has a huge potential in continuous growth process in an industrial manufacturing line.

2 Experimental Details

An aqueous solution of 0.30 M SC(NH₂)₂ (99.995% purity) serving as sulphur source was made in 800 ml of deionised water. Afterwards, 0.20 M CdCl₂,xH₂O (99.995% purity) serving as the cadmium source was added into the TU solution contained in a 1000 ml plastic beaker. The 1000 ml plastic beaker was placed inside a 2000 ml glass beaker containing de-ionised water to achieve homogeneity in heating the solution. Afterward, the pH of the aqueous solution was adjusted to 2.70±0.02 at room temperature using diluted HCl and NH₄OH. The temperature of the deposition electrolyte was increased to ~85°C using a magnetic stirrer hotplate. The TEC-7 glass/FTO (fluorine-doped tin oxide) substrates with a sheet resistance of 7 Ω /square were cut into small pieces with dimensions of 2×2 cm². These substrates were kept in an ultrasonic bath containing detergent solution for 30 min in order to remove any residual particles and contaminants. Afterwards, the glass/FTO substrates were cleaned with organic solvents (methanol and acetone) and subsequently rinsed with de-ionised water. The electrodeposition of CdS thin films were carried out potentiostatically using 2-electrode system. The electrodes used for the electrodeposition of CdS thin films were high purity graphite rod. One electrode serves as the anode while the other electrode serves as the cathode. The cathode was attached to the glass/FTO substrate using insulating polytetrafluoroethylene (PTFE) tape. All the reagent grade chemicals and the glass/FTO substrates were purchased from Sigma Aldrich Ltd (UK). Finally, the computerised GillAC potentiostat (ACM instrument) was used to carry out the electrodeposition work. The approximate ranges of deposition voltages were determined using the cyclic voltammetry. The structural, compositional and morphological properties of the ED-CdS thin films were respectively carried out using X-ray diffraction (XRD), Raman spectroscopy, Scanning electron microscopy (SEM) and Atomic force microscopy (AFM). The electrical and optical properties of the CdS layers were studied using Photoelectrochemical (PEC) cell measurement, DC electrical conductivity and Optical absorption, respectively.

3 Results and Discussion

3.1 Cyclic Voltammograms

Cyclic voltammograms were recorded for the acidic and aqueous solution containing a combination of 0.30 M SC(NH₂)₂ and 0.20 M CdCl₂.xH₂O in 800 ml of deionised water. The pH of the aqueous solution was adjusted to

2.70 \pm 0.02 at room temperature by adding diluted HCl or NH₄OH. The acidic pH was used to prevent the formation of cadmium hydroxide phase and to suppress the homogeneous precipitation of elemental S and CdS particles during the growth [18]. Afterward, the temperature of the aqueous solution was raised to ~85°C. Then, cyclic voltammograms were recorded at the cathodic potentials range (0-900) mV with the scan speed of 3 mVs⁻¹ and result is shown in Figure 1.



Figure 1: A cyclic voltammogram for acidic and aqueous electrolyte containing 0.30 M $SC(NH_2)_2$ and 0.20 M $CdCl_2.xH_2O$ at pH of 2.70±0.02 and temperature of 85°C.

Study on the cyclic voltammograms of the acidic and aqueous solution containing $SC(NH_2)_2$ and $CdCl_2$ using 3-electrode system has been reported in the literature [19]. In these solutions, $CdCl_2$ provides Cd^{2+} ions and the electrochemical reaction of Cd deposition is as follows:

$$Cd^{2+} + 2e^- \to Cd \tag{1}$$

Reports show that when TU and $CdCl_2$ are mixed together in acidic and aqueous solutions, most of the Cd^{2+} ions bond to TU and forms Cd^{2+} -TU complexes. This is due to the high tendency of Cd^{2+} ions to coordinate with TU through S atoms [20]. For this reason, the concentration of Cd^{2+} -TU complexes will be much higher than Cd^{2+} ions in the deposition electrolyte. In this case, the deposition of elemental Cd shown in Equation 1 can only take place at higher cathodic potentials (in this work more than 820 mV) as shown in Figure 1. It should be noted that, the TU is fairly stable in acidic solution but it easily decomposes in alkaline solution. In this case, in acidic and aqueous solution containing Cd^{2+} -TU complexes none of the constituents, Cd^{2+} and TU, can electrochemically reduce to give CdS but the chemical decomposition of Cd^{2+} -TU complex is promoted under increased pH that is generated by electrochemical reduction of hydrogen and/or oxygen as shown in Equations (2) and (3):

$$2H^+ + 2e^- \to H_2 \tag{2}$$

$$O_2 + 2H_2O + 4e^- \to 4OH^-$$
 (3)

These reactions raise pH at the vicinity of the electrode (FTO surface) to promote the chemical decomposition of TU. However, in the bulk solution pH remains low. TU undergoes decomposition when pH is raised as shown in Equation (4) [21]:

$$SC(NH_2)_2 \rightarrow H_2S + NH_2CN$$
 (4)

Then H₂S react with Cd²⁺ to form CdS according to the following electrochemical reaction:

$$Cd^{2+} + H_2S \to CdS + 2H^+ \tag{5}$$

In Figure 1, the gradual increase in the cathodic current from \sim (0-740) mV during the forward scan is due to reactions shown in Equations (2) and (3) which trigger the film growth. Further increase in cathodic current from \sim (740-820) mV results in the CdS layer formation on the FTO surface which agrees with the experimental observations as shown in Equation (5). The sharp increase in the cathodic current at cathodic potential of >820 mV is due to the deposition of elemental Cd.

3.2 Visual appearance

Figures 2a and 2b show the visual appearance of the as-deposited and annealed CdS layers grown at cathodic potential ranges of 740 to 820 mV. For this experiment, all CdS layers were grown on glass/FTO substrates for 2 hours duration. This growth voltages range was selected from cyclic voltammograms study and experimental observations. The visual appearance can give some qualitative information about the electrodeposited CdS layers.

Results show the light yellowish-green colours for the samples grown at lower growth voltages. The light yellowishgreen colour is due to the S-richness of the CdS layers. This is because S (with standard reduction potential $E^{\circ} = -0.14$ V vs. NHE) deposits first since it has a more positive standard reduction potential than Cd ($E^{\circ} = -0.40$ V vs. NHE) [22]. As the growth voltage increases gradually, more elemental Cd is deposited and therefore layers gradually become darker in colour.

From the visual appearance of as-deposited CdS layers, it is obvious that the as-deposited CdS layers require post deposition annealing in order to improve their microstructural and optical properties suitable for device fabrication. After annealing at 400°C for 20 minutes in air, the CdS layers become uniformly orange-yellowish colour as shown in Figure 2b. The CdS formation is also possible by combining excess elemental S and Cd upon heat treatment. CdO formation is also possible by oxidation of elemental Cd due to heat treatment in air. The energy bandgap of CdO is $\sim 2.28 \text{ eV}$ [23] very close to that of CdS ($\sim 2.42 \text{ eV}$) and therefore layers become uniformly orange-yellowish colour.



Figure 2: Variation of visual appearance as a function of growth voltage for (a) the as-deposited and (b) annealed CdS layers.

3.3 Structural analysis

3.3.1 X-ray Diffraction

The XRD measurements were carried out with a diffractometer (Philips PW 3710 X'pert) using the Cu-K_{α} monochromator of wavelength λ =1.542 Å over the interval 10-70°/2 Θ . The X-ray generator voltage and current were set to 40 kV and 40 mA respectively.

Figure 3a shows the XRD patterns of the as-deposited CdS layers grown on glass/FTO substrates at different cathodic potential ranges of 740 to 820 mV. This investigation was carried out in order to find the optimum growth voltage by observing the most intense XRD peaks for the CdS layers. The growth durations for all the as-deposited CdS layers were 2 hours. Among all the CdS samples, the layers grown in the vicinity of 800 mV showed better crystallinity as shown in Figure 3b.

According to the results presented in Figure 3a, all CdS layers were polycrystalline with hexagonal crystal structure. Three small XRD peaks observed at 20 values in the range $(24.88-24.95)^{\circ}$, $(28.21-28.57)^{\circ}$ and $(48.01-48.41)^{\circ}$ represent the diffractions from (100), (101) and (103) hexagonal planes, respectively. The preferred orientation peak was observed at 20 values in the range $(26.53-26.59)^{\circ}$ representing the diffraction from (002) hexagonal plane which overlaps with the underlying FTO peak. For this reason, the analysis were mainly focused on the (101) XRD peak which is the second intense peak next to the (002) peak. In this work, the experimentally observed XRD peaks are in a good agreement with JCPDS file number: 01-080-0006 for the hexagonal CdS.



Figure 3: (a) The XRD patterns of the as-deposited CdS layers grown at the cathodic potentials range (740-820) mV, and (b) the intensity variation of (101) peak as a function of growth voltage.

The similar hexagonal crystal structure has been reported by Yamaguchi et al for the electrodeposited CdS layers grown on the ITO substrates from the combination of TU and CdCl₂ in acidic and aqueous solution [19]. In their reports, the (002) peak is clearly shown to be preferred orientations due to non-overlapping (002) with underlying ITO peaks. In other reports, the similar hexagonal structure or mixture of hexagonal and cubic crystal structures have been reported for the as-deposited CdS layers grown from different precursors including Na₂S₂O₃ [15], (NH₄)₂S₂O₃ [17], C₂H₅NS [18]. In these reports, the hexagonal phases were shown to be more stable than cubic phases at high temperatures for the electrodeposited CdS layers as the cubic phases were completely vanished after annealing at 400°C for 20 minutes in air.

The optimisation of the growth voltage was narrowed down by growing the CdS layers close to the cathodic potential of 800 mV. For this reason, the CdS layers were grown at the cathodic potential ranges of 793 to 801 mV with 2.0 mV potential step difference while keeping other growth parameters constant. All CdS layers again were grown on glass/FTO substrates for 2 hours. Afterwards, the as-deposited CdS layers were annealed at 400°C for 20 minutes in air and results are shown in Figures 4a and 4b.



Figure 4: The XRD patterns of (a) as-deposited, (b) annealed CdS layers, and (c) the intensity variation of (101) peak as a function of growth voltage for the as-deposited and annealed CdS layers. All CdS layers were grown at growth voltage ranges of 793 to 801 mV for 2 hours duration and then annealed at 400°C for 20 minutes in air.

In order to find the best growth voltage for the CdS layers, the intensities of (101) peaks were plotted against the growth voltages for both as-deposited and annealed CdS layers as shown in Figure 4c. The best crystallinities were observed for the CdS layers grown at the growth voltage of 797 mV before and after annealing. This growth voltage is related to the stoichiometric point (V_i) where the ratio of Cd/S is close to unity. The lower peak intensities were observed for the layers grown away from the growth voltage of 797 mV due to non-stoichiometric properties (S-richness or Cd-richness) of the deposited layers (see later EDX results for compositions). The (101) peak intensities of all as-deposited layers were improved after annealing as shown in Figure 4c. This is due to enhancement in crystallinity, grain growth and recrystallisation in the CdS layers after annealing. This shows that in the low temperature solution growth techniques such as electrodeposition and CBD, the post-deposition annealing is an essential step to improve the material quality of the CdS layers.

Table 1 shows the variation of the FWHM and the corresponding crystallite sizes as a function of growth voltages for the as-deposited and annealed CdS layers. The FWHM and crystallite size calculations were based on diffraction from CdS (101) XRD peaks. The crystallite sizes were estimated using the Scherrer's formula as given by Equation (6) [24]:

$$D = \frac{0.94\lambda}{\beta\cos\theta} \tag{6}$$

Where, D is the crystallite size in (nm), λ is the X-ray wavelength in (Å), β is the full width at half maximum (FWHM) in degrees and θ is the Bragg angle in degrees. For the as-deposited CdS layers grown at the growth voltage ranges of 793 to 801 mV, the crystallite size values were in the range ~(11-22) nm. After annealing, the crystallite sizes were improved with the values in range ~(26-33) nm. This is due to the recrystallisation and coalescence of crystallites, reduction in stress/strain and improvement in the structural properties of CdS layers after annealing. It should be noted that, depending on the growth techniques and growth conditions, the crystallite sizes of the CdS thin films can be different. In electrodeposition growth technique, the crystallite sizes can also be different depending on the precursor, growth temperature and pH values used for the growth of thin films [15, 17, 25]. Reports show that, CdS layers grown by high temperature growth techniques produce larger crystallites and larger grains as compared to the low temperature growth techniques such as CBD and electrodeposition [26, 27].

Growth	20		FWHM		Crystallite size	
voltage	(°)		(°)		(nm)	
(mV)	As-deposited	Annealed	As-deposited	Annealed	As-deposited	Annealed
793	28.44	28.28	0.519	0.259	16	33
794	28.25	28.28	0.779	0.324	11	26
795	28.21	28.32	0.519	0.324	16	26
796	28.27	28.57	0.519	0.324	16	26
797	28.41	28.26	0.389	0.259	22	33
798	28.38	28.26	0.779	0.324	11	26
799	28.49	28.41	0.779	0.259	11	33
800	28.41	28.27	0.779	0.324	11	26
801	28.39	28.26	0.519	0.259	11	33

 Table 1: Variation of crystallite size as a function of growth voltage for the as-deposited and annealed CdS layers

 based on (101) peak.

3.3.2 Raman Spectroscopy

Raman spectroscopy as a non-destructive technique can be used to identify the molecular finger print, crystallinity, strain and stress of the solid-state materials. The Raman spectra of the CdS thin films were measured using Renishaw's Raman microscope. The excitation laser used was an Argon ion laser with the wavelength of 514.0 nm.

In this experiment, CdS layers were grown on glass/FTO substrates at growth voltage of 797 mV for 2 hours duration. Then, the as-deposited layers were divided into two parts; the first part remained as-deposited and second part was annealed at 400°C for 20 minutes in air. Raman study was carried out on the as-deposited and annealed layers and results are shown in Figure 5.

In the as-deposited sample, two Raman peaks were observed at 232.1 cm⁻¹ and 304.9 cm⁻¹ which are related to the TO and 1LO phonon peaks of CdS, respectively. After annealing, the TO phonon peak disappears and the intensity of the 1LO peak increases drastically as compared to the 1LO peak of the as-deposited sample. Also, the second Raman peak

appeared at 601.1 cm⁻¹ after annealing which is corresponding to the 2LO phonon peak of the CdS. An increase in the intensity of 1LO peak and appearance of the 2LO peak after annealing indicate the improvement in the crystallinity and material quality of the CdS layers. The 1LO and 2LO peaks position for the bulk CdS crystal are 305 cm⁻¹ and 610 cm⁻¹, respectively [28]. Obviously, as observed in this work, 1LO and 2LO peaks for the as-deposited and annealed samples have red shifted as compared to the bulk CdS crystal. The red shift in Raman peaks can arise due to the tensile stress in CdS thin films [29].

In a production line, Raman spectroscopy can be used as a fast and non-destructive method to check the material quality of the deposited thin films as a quality control technique.



Figure 5: Raman spectra of as-deposited and annealed CdS layers grown on glass/FTO substrates. The CdS layers were grown at cathodic potential of 797 mV and annealed at 400°C for 20 minutes in air.

3.4 Optical absorption studies

Optical absorption measurements were carried out using a Carry 50 scan UV-visible spectrophotometer (Varian Australia Pty. Ltd.). This experiment was carried out to study the effect of different growth voltages on the optical properties of the CdS layers. For this experiment, the CdS layers were grown on glass/FTO substrates for 2 hours

duration. Afterwards, CdS samples were cut into two parts; the first parts were remained as-deposited and the second parts were annealed at 400°C for 20 minutes in air for comparison.

Figure 6a and 6b shows the $(ahv)^2$ vs. photon energy (hv) for the as-deposited and annealed CdS layers grown at the cathodic potential ranges of 793 to 801 mV, in the vicinity of V_i = 797 mV. For the as-deposited CdS layers shown in Figures 6a, as the growth voltage increases the gradient of the optical absorption also increases gradually while the energy bandgaps reduce. The gradual reduction in energy bandgaps is due to the incorporation of more elemental Cd in the CdS layers as the growth voltage increases as shown in Table 2 and Figure 7. It should be noted that Cd is a metallic element, therefore, incorporation of more elemental Cd in the CdS layers lead to the reduction in energy bandgap. Also, experimental observations show that as the amount of elemental Cd increases in the as-deposited CdS layers, the layers become darker in appearance showing the reduction in energy bandgaps.

The estimated energy bandgap values for the as-deposited samples grown at cathodic potential ranges of 793 to 801 mV were in the range (2.53-2.58) eV as shown in Table 2. The higher energy bandgap values at lower growth voltages can be due to the S-richness of the layers or nano crystalline nature of the electrodeposited CdS layers. Also, presence of pinholes or gaps in between grains in CdS layers can provide easy path for UV-vis light to pass during optical absorption measurement which can lead to the increase in energy bandgap.

After annealing, as the growth voltage increases gradually the gradient of the optical absorption also increases gradually and reaches its maximum values at 797 mV as shown in Figure 6b. Above 797 mV, the gradient of optical absorption reduces again. Results show that, after annealing the energy bandgap values of the as-deposited samples were shifted towards the lower energy in the range (2.42-2.48) eV as shown in Table 2. It should be noted that, the lowest energy bandgap value ($E_g = 2.42 \text{ eV}$) were observed at $V_i = 797 \text{ mV}$, which coincide with that of bulk CdS. When the growth voltage deviate from V_i , the energy bandgap increases due to the non-stoichiometric effect, and expose of gaps between the grains as shown in Table 2 and Figure 7. Also, reports show that incorporation of oxygen in the CdS during annealing can increase the optical bandgap of CdS layers and hence, increases the photocurrent in the fabricated solar cells [30].



Figure 6: Optical absorption spectra of (a) as-deposited and (b) annealed CdS layers at 400°C for 20 minutes in air. The CdS layers were grown on glass/FTO substrates at different cathodic potential ranges of 793 to 801 mV for 2 hours duration.

Growth voltage	Energy bar	$dgap \pm 0.01$	
(mV)	(eV)		As-deposited CdS
	As-	Annealed	2.58 X
	deposited		
793	2.58	2.46	
794	2.57	2.45	
795	2.56	2.44	Annealed CdS
796	2.56	2.43	2.46
797	2.55	2.42	
798	2.55	2.44	2.42
799	2.54	2.45	
800	2.53	2.46	
801	2.53	2.48	Growth voltage (mV)

 Table 2 and Figure 7: Variation of energy bandgap with growth voltage for the as-deposited and annealed CdS layers at 400°C for 20 minutes in air. The CdS layers were grown on glass/FTO substrates for 2 hours duration.

Figures 8a and 8b, respectively show the transmittance spectra of the as-deposited and annealed CdS layers grown on glass/FTO substrates at the cathodic potential ranges of 793 to 801 mV for 2 hours durations. Results show the large scatter in the transmittance spectra of the as-deposited samples as compared to the annealed samples. In the as-deposited sample, as the growth voltage increases transmittance reduces gradually. The gradual reduction in transmittances can be due to the gradual increase in the amount of elemental Cd as the growth voltage increases as shown in Figure 8a.

Experimental observations show that the transmittances were in the ranges of (8-80)% at the wavelength ranges of (530-800) nm for the as-deposited samples. After annealing, the transmittances of the CdS layers were improved and absorption edges became sharper. Also, annealing brought the transmittance spectra closer together and narrow them down to the ranges of (68-89)% within the same wavelength ranges of (530-800) nm as shown in Figure 8b. The highest transmittance was observed for the annealed sample grown at $V_i = 797$ mV. When the growth voltage deviates

from V_i , the transmittances show reduction due to non-stoichiometric properties of the layer. The CdS layers with higher transmittances and sharper absorption edges are more suitable for solar cells application.



Figure 8: Transmittance spectra of (a) as-deposited and (b) annealed CdS layers grown for 2 hours at different cathodic potential ranges of 793 to 801 mV.

3.5 Microstructure and morphological studies

3.5.1 Scanning electron microscopy (SEM)

The surface morphology of the CdS thin films were studied using FEI Nova 200 NanoSEM. This experiment was carried out in order to study surface morphology of the ED-CdS layers. For this work, CdS layers were grown on glass/FTO substrates at growth voltage of 797 mV for 2 hours duration. Part of the as-deposited CdS samples was annealed at 400 for 20 minutes in air for comparison of SEM images.

Figure 9a and 9b, respectively shows the SEM and cross section images of the as-deposited CdS thin films grown at optimum growth voltage of 797 mV for 2 hours duration. At the 650,000x magnification, the SEM image of asdeposited CdS thin films show that the layers contain nano crystallites in the range of $\sim(11-22)$ nm. The agglomeration of these nano crystallites produces small clusters/grains with the sizes in the range $\sim(60-225)$ nm as shown in Figure 9a. In this figure, the gaps in-between the grains can be clearly observed. The presence of these gaps can be due to the nature of the electrodeposition technique and the substrate used. The FTO is known to have rough and spiky surface as shown in Figure 9b. During the electrodeposition, the electric field at these spikes are higher than that of the valleys. In this case, the nucleation starts at these spikes first and tends to grow upwards perpendicular to the FTO surface. This will create columnar-like growth for the electrodeposited thin films which can be seen in Figure 9a and 9b. The columnar growth behaviour has some advantages and disadvantages. The disadvantages of columnar growth are pinholes formation and creation of non-uniformity in the electrodeposited layers. These pinholes are known as shunting paths and should be treated otherwise they will drastically reduce the efficiency of the fabricated thin film solar cells due to short-circuiting of front and back contacts after metallisation. The advantages of the columnar growth are the high crystallinity and high electrical conductivity along the columnar shape grains. In this case it is easier for charge carries to flow normal to the FTO surface during the PV action of CdS/CdTe solar cells with higher mobility through this path with minimized scattering from the grain boundaries [31].

The SEM cross section image of the as-deposited CdS layers with magnification of 200,000x show the good coverage of FTO surface by the CdS grains. However, the non-uniformity at the surface of the CdS thin films can be due to the high surface roughness of the underlying glass/FTO substrate and also can be due to upward growth nature of the electrodeposited layers. The average thickness of the as-deposited CdS layer estimated from SEM image was ~120 nm. In addition, some voids were observed at FTO/CdS interface. These voids can be originated from the columnar type growth, incomplete cleaning or introduced during the sample preparation for SEM experiment.



Figure 9: (a) Surface and (b) cross section SEM images of the as-deposited CdS layers grown at the growth voltage of 797 mV for 2 hours duration with 650,000x and 200,000x magnifications, respectively. The thickness of CdS layer is estimated close to 120 nm.

Figures 10a and 10b, respectively shows the SEM images of the as-deposited and annealed CdS layers with the lower magnification of 120,000x. The SEM images of as-deposited and annealed layers approximately show the uniform coverage of the FTO surface by CdS grains. However, presences of pinholes or gaps between grains are clear in the layers. The estimated grain sizes obtained from the SEM image of the as-deposited CdS layers were in the range \sim (60-225) nm. After annealing, no noticeable changes were observed in the grain sizes of the as-deposited CdS layers as shown in Figures 10b. After annealing, the number of gaps in between the grains has reduced due to the coalescence of these grains. It also can be due to slight increase in crystallite sizes of the CdS layers from the \sim 22 nm for the as-deposited to \sim 33 nm after annealing as shown in Figure 10b and Table 1.



Figure 10: The SEM images of the CdS layers grown on glass/FTO substrates for (a) the as-deposited and (b) the annealed layers. The CdS layers were grown at cathodic potential of 797 mV for 2 hours duration.

3.5.2 Atomic force microscopy (AFM)

The AFM studies were carried out using JSPM-5200 system (JEOL, Tokyo, Japan) and Nanoscope IIIa multimode atomic force microscope in order to evaluate the crystallite and grain sizes. For this experiment CdS samples were grown on glass/FTO substrates at cathodic potential of 797 mV for 2 hours duration. As-deposited CdS layers were divided into two parts; the first part was left as-deposited and the second part was annealed at 400°C for 20 minutes in air.

Figures 11a, 11b and 11c show the 2D and 3D-AFM images of the as-deposited CdS layers. The AFM images of the asdeposited CdS layers show coverage of FTO surface by CdS grains with some gaps in-between the grains. The 2D-AFM image shows that the as-deposited CdS layers contain nano crystallites with the sizes in the ranges of ~(10-25) nm as shown in Figure 11a. These results are in a good agreement with the results obtained from SEM images. The non-uniformity at the surface of the as-deposited CdS layers can be observed in the 3D-AFM images CdS thin film shown in Figure 11b. These non-uniformities are due to high surface roughness of the underlying FTO substrate and upward growth nature of the electrodeposition technique. The upward or columnar-like growth leaves some gaps/pinholes in between the grains as can be seen in Figure 11c.



CdS S1



Figure 11: (a, b, c) 2D and 3D-AFM images of the as-deposited CdS grown on glass/FTO substrates for 2 hours (courtesy: Inst. of Org. Catalysis & Electrochem., Kazakhstan).

3.6 Compositional characterisation

The EDX measurements were carried out on in order to study the composition and atomic percentage of the deposited CdS layers. For this experiment, CdS layers were deposited on glass/FTO substrates for 2 hours duration. The first layer was grown at the stoichiometric growth voltage of 797 mV. The next four layers were grown at 787, 792, 802 and 807 mV respectively.

The EDX spectrum of the sample grown at stoichiometric growth voltage of 797 mV is shown in Figure 12. All the EDX spectra clearly show the presence of Cd and S atoms in the deposited films. The other two peaks, Sn and O, are related to the underlying glass/FTO substrates. The atomic percentages calculated from EDX measurement are shown in Table 3. The EDX work show that the samples deposited at growth voltages lower than 797 mV are S-rich, whereas samples grown at growth voltages higher than 797 mV are Cd-rich. The samples deposited at the growth voltage of 797 mV were approximately stoichiometric with the Cd/S ratio close to unity as shown in Table 3.



Figure 12: EDX spectra of the Stoichiometric CdS. The CdS layer was grown on glass/FTO substrate for 2 hours duration at growth voltage of 797 mV.

Table 3: Atomic percentages and Cd/S ratio of the CdS layers grown at 787, 792, 797, 802 and 807 mV respectively.All as-deposited CdS layers were grown on glass/FTO substrates for 2 hours duration.

Growth voltage	Atomic percentage (at%)			Cd/S ratio	Conditions
(mV)	Cd	S	Sn		
787	28.1	33.1	38.8	0.84	S-rich
792	29.8	31.1	39.1	0.95	S-rich
797	30.0	30.4	39.6	0.98	Stoichiometric
802	31.7	29.0	39.3	1.09	Cd-rich
807	33.0	24.2	42.8	1.36	Cd-rich

3.7 Electrical properties

3.7.1 Photoelectrochemical (PEC) cell Analysis

The PEC cell measurements were carried out to determine the electrical conductivity type of the CdS thin films. In PEC cell measurements, a semiconductor/liquid junction is formed by immersing glass/FTO/CdS into 0.10 M $Na_2S_2O_3$ aqueous solution. The voltage of the semiconductor/liquid junction is measured under both light (V_L) and dark (V_D)

conditions and the difference (V_L-V_D) represents the magnitude of PEC signal. The sign of the PEC signal shows the electrical conductivity type of the semiconductor. In this work, the Hall Effect measurement cannot be applied to glass/FTO/CdS layers due to the presence of lower resistance path of the underlying FTO substrate.

For PEC cell measurements, CdS layers were grown on glass/FTO substrates at different growth voltage ranges of 793 to 801 mV for 2 hours duration and PEC signals were measured. Then, the as-deposited samples were annealed at 400°C for 20 minutes in air for comparison and results are shown in Figure 13. For both as-deposited and annealed samples, the negative PEC signals were observed which represents the n-type electrical conductivity. After annealing, the values of negative PEC signal increases as compared to the as-deposited samples. This shows an enhancement in electrical properties and material quality of the CdS layers upon annealing. The n-type conductivity nature of CdS layers arises due to the presence of S vacancies and Cd interstitials in the crystal lattice of this material. The S vacancies and Cd interstitials are generally known as intrinsic donor defects [30].



Figure 13: The PEC signals of the as-deposited and annealed CdS layers grown at the cathodic potential ranges of 793 to 801 mV. The CdS layers were annealed at 400°C for 20 minutes in air. All CdS layers were grown on glass/FTO substrates for 2 hours duration.

3.7.2 Electrical resistivity measurements

The resistivity measurements were carried out at room temperature (300 K) for the CdS layers grown on glass/FTO substrates with different thicknesses. Circular indium metal contacts of 2 mm diameter were evaporated on glass/FTO/CdS structures using EDWARDS 306 vacuum coater (metalliser). The pressure of the evaporation chamber during the evaporation of indium metal contacts was 10⁻⁵ Pa. The average resistances of the glass/FTO/CdS/In structures were then measured under dark condition using a computerised I-V system including a Keithley 619 electrometer and a multimeter. Table 4 and Figure 14 show the variation of CdS resistivity as a function of thickness for the as-deposited and annealed layers at 400°C for 20 minutes in air. In this experiment, all the CdS layers were grown at optimised cathodic potential of 797 mV.

Results show that as the thickness of CdS layers increases the resistivity decreases as shown in Table 4 and Figure 14. The reduction in resistivity can be attributed to improvement of all properties due to formation of improved crystallites in CdS layers. It should be noted that in CdS thin films, sulphur vacancy and Cd interstitial defects act as electron donor. Therefore, as the thickness of the layers increases, the free electron concentration in the CdS thin film also increases due to increase in the sulphur vacancy and Cd interstitial defects thus leading to the reduction of the resistivity [32]. The other possible reason of reduction in CdS resistivity can be due to the increase in grain size as the thickness increases. It should be noted that as the grain size increases, the grain boundaries reduces. The grain boundaries act as electron traps or scattering centres. Therefore, larger grains mean less scattering centres, and as a result electrons can move easily within the CdS crystal [33].

In this work, annealing of the CdS layers were shown to have lower resistivity than those of the as-deposited layers. The reduction in CdS resistivity indicates an improvement in electrical and structural properties. This can be due to recrystallisation, increase in grain size, carrier concentration and mobility of free electrons in the CdS thin films and reduction in lattice defect sites after annealing. The resistivity values observed in this work are in agreement with resistivity values reported in the literature [32, 17].

Table 4: Variation of resistivity with thickness for the as-deposited and annealed CdS layers grown at cathodic potential of 797 mV. The CdS layers were grown on glass/FTO substrates and then annealed at 400°C for 20 minutes in air.

Thickness	$\mathrm{R}_{\mathrm{av}}\left(\Omega ight)$		Resistivity $\times 10^5$ (Ω cm)	
(nm)	As-deposited	Annealed	As-deposited	Annealed
335	525	495	4.92	4.63
393	494	452	3.94	3.61
465	424	385	2.86	2.59
483	291	268	1.89	1.74
500	274	236	1.72	1.48
550	180	145	1.02	0.82



Figure 14: Variation of electrical resistivity as a function of thickness for the as-deposited and annealed CdS layers grown at the cathodic potential of 797 mV. The CdS layers were grown on glass/FTO substrates and then annealed at 400°C for 20 minutes in air.

3.7 Thickness Measurement

Thickness measurement is an important step in thin film solar cells development. The CdS thickness can directly affect the performance of the solar cells. In the device application, CdS thin films are usually used as a window or buffer layers. Reports show that CdS with a thickness of ~100 nm can absorb about 63% of the incident photons with energy greater than the bandgap (E_g) due to its high absorption coefficient of about 10⁴ to 10⁵ cm⁻¹ [34, 35]. For this reason, in order to increase the photocurrent in the solar cells, the CdS thickness should be as low as possible about 50 to 80 nm [36]. It should be noted that by lowering the thickness of CdS, the possibility of creation of pinholes in the layer also increases. These pinholes create shunting paths between the front and back contact during metallisation in the thin film solar cells which will affect the performance of the solar cells. However, reducing the thickness of CdS can adversely affect the open circuit voltage (V_{oc}) and fill factor (FF) of fabricated solar cells [37]. The ability to grow pinholes-free CdS layers with low thicknesses depends on the growth technique and substrate used.

In this work, the CdS layers thicknesses were measured experimentally using UBM microfocus optical depth profilometer (UBM, Messetecknik GmbH, Ettlingen, Germany). The theoretical thicknesses were estimated using Faraday's law of electrolysis for comparison as shown in Equation 7 [38]:

$$\Gamma = \frac{JtM}{nF\rho}$$
(7)

Where T is the thickness of the CdS layer, J is the average deposition current density, M is the molecular weight of the CdS, n is the number of electrons transferred in the reaction for formation of one mole of CdS (n = 2), F is the Faraday's constant and ρ is the density of CdS.

Figure 15 shows the variation in CdS thicknesses as a function of growth time. Both theoretical and experimental values show approximately linear increase in film thickness with deposition time. The difference in the theoretically estimated and experimentally measured thickness values is due to the loss of some electronic charges in the electrolyte during electroplating.

The two dotted lines show the extrapolation to the point of zero (t = 0). This simply means when no current passes through the deposition electrolyte, no deposition will take place. In this experiment, the error in thickness measurement was about ± 50 nm.



Figure 15: Theoretical and experimental thickness variation with growth time for the as-deposited CdS layers grown at cathodic potential of 797 mV.

4 Conclusions

CdS thin films have been successfully electrodeposited using 2-electrode system. All CdS layers presented in this work were deposited at temperature of ~ 85° C and pH of 2.70±0.02. The precursors used were aqueous solutions containing 0.30 M SC(NH₂)₂ and 0.20 M CdCl₂.xH₂O. The deposited CdS thin films showed good adhesion to the glass/FTO substrates. Based on the experimental observations, the best cathodic potential for the deposition of stoichiometric CdS thin films is identified as 797 mV. From the XRD results, all the deposited layers were identified as polycrystalline in nature with hexagonal crystal structure and preferentially oriented along (002) plane. Improvements in the crystallinities of the CdS layers were observed after annealing at 400°C for 20 minutes in air. All deposited CdS layers grown at different cathodic potential showed n-type electrical conductivity. Also, optical absorption results showed the bandgap values in the range (2.42-2.48) eV after annealing.

Observation from SEM and AFM images revealed the columnar-like growth for the CdS grains. SEM and AFM images also show that the CdS grains contain nano crystallites with the sizes in the range \sim (11-33) nm. The EDX spectra show that the layers grown at the growth voltage of 797 mV were approximately stoichiometric. The CdS layers grown below

and above the growth voltage of 797 mV were found to be S-rich and Cd-rich respectively. The electrical resistivity show a reduction as the CdS layer thickness increases. The resistivity values for as-deposited and annealed CdS were in the range $(0.82-4.92)\times10^5 \Omega$ cm. No visible precipitations of elemental S or CdS particles were observed in the deposition electrolyte showing a stable bath using TU during the growth.

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References

- [1] S.M. Sze, Physics of Semiconductor Devices, 2nd edn. (John Wiley & Sons, New York, 1981) pp 849.
- [2] K. Deng and L. Li, Adv. Mater., **26**, 2619-2635 (2014).
- [3] Q.H. Li, T. Gao, and T.H. Wang, Applied Physics Letters, 86, 193109 (2005).
- [4] E. Sorokin, D. Klimentov, M.P. Frolov, Yu.V. Korostelin, V.I. Kozlovsky, Yu.P. Podmarkov, Ya.K. Skasyrsky,
 I.T. Sorokina, Appl. Phys. B, 117, 1009-1014 (2014).
- [5] D. Lincot, Thin Solid Films, **487**, 40-48 (2005).
- [6] N.R. Paudel, C. Xiao, Y. Yan, J. Mater. Sci: Mater. Electron., 25, 1991-1998 (2014).
- [7] R.A Berrigan, N. Maung, S.J.C Irvine, D.J Cole-Hamilton, D. Ellis, Journal of Crystal Growth, 195, 718-724 (1998).
- [8] Z. He, G. Zhao, W. Weng, P. Du, Ge. Shen, G. Han, Vacuum, 79, 14-18 (2005).
- [9] M.C. Baykul, A. Balcioglu, Microelectronic Engineering, 51-52, 703-713 (2000).
- [10] Junfeng Han, C. Spanheimer, G. Haindl, Ganhua Fu, V. Krishnakumar, J. Schaffner, Chunjie Fan, Kui Zhao,
 A. Klein, and W. Jaegermann, Solar Energy Materials & Solar Cells, 95, 816-820 (2011).
- [11] S.J. Lade, M.D. Uplane, C.D. Lokhande, Materials Chemistry and Physics, 53, 239-242 (1998).
- [12] I.M. Dharmadasa and J. Haigh, J. Elechtrochem. Soc., **153**(1), G47-G52 (2006).
- [13] G. Sasikala, R. Dhanasekaran, C. Subramanian, Thin Solid Film, **302**, 71-76 (1997).
- [14] J. Nishino, S. Chatani, Y. Uotani, Y. Nosaka, Journal of Electroanalytical Chemistry, 473, 217-222 (1999).
- [15] D.G. Diso, G.E. A. Muftah, V. Patel and I.M. Dharmadasa, Journal of The Electrochemical Society, 156(6), H647-H651 (2010).
- [16] K. Zarebska, M. Skompska, Electrochimica Acta, 56, 5731-5739 (2011).
- [17] N.A. Abdul-Manaf, A.R. Weerasinghe, O.K. Echendu, I.M. Dharmadasa, J. Mater. Sci: Mater. Electron., 26, 2418-2429 (2015).
- [18] K. Yamaguchi, T. Yoshida, T. Sugiura, and H. Minoura, J. Phys. Chem. B, 102, 9677-9686 (1998).
- [19] K. Yamaguchi, P. Mukherjee, T. Yoshida, and H. Minoura, Chemistry Letters, 9, 864-865 (2001).
- [20] A.V. Naumov, V.N. Semenov, and E.G. Goncharov, Inorganic Materials, 37(6), 647-652 (2001).
- [21] V.P. Timchenko, A.L. Novozhilov, and O.A. Slepysheva, **74**(7), 1046-1050 (2004).
- [22] P. Vanysek, Electrochemical Series Table 1 Alphabetical, CRC press LLC (2000).

- [23] P.H. Jefferson, S.A. Hatfield, T.D. Veal, P.D.C. King, C.F. McConville, J. Zuniga-Perez and V. Munoz-Sanjose, Applied Physics Letters, 92, 022101 (2008).
- [24] A.L. Patterson, Physical Review, 56, 978-982 (1939).
- [25] R. Dharmadasa, I.M. Dharmadasa and T. Druffel, Advanced Engineering Materials, 16(11), 1351-1361 (2014).
- [26] A.I. Oliva, R.C. Rodriguez, O.S. Canto, V. Sosa, P. Quintana, J.L. Pena, Applied Surface Science, 205, 56-64 (2003).
- [27] H.R. Moutinho, D. Albin, Y. Yan, R.G. Dhere, X. Li, C. Perkins, C.-S. Jiang, B. To, M.M. Al-Jassim, Thin Solid Films, 436, 175-180 (2003).
- [28] R. Litrán, R. Alcantára, E. Blanco, and M. Ramirez-del-solar, Journal of Sol-Gel Science and Technology, 8(1-3), 275-283 (1997).
- [29] P. Nandakumar, C. Vijayan, M. Rajalakshmi, A.K. Arora, Y.V.G.S. Murti, Physica E, 11, 377-383 (2001).
- [30] C. Wu, J. Jie, L. Wang, Y.Yu, Q. Peng, X. Zhang, J. Cai, H. Guo, D. Wu and Y. Jiang, Nanotechnology, 21, 505203 (7pp) (2010).
- [31] I.M. Dharmadasa, P.A. Bingham, O.K. Echendu, H.I. Salim, T. Druffe, R. Dharmadasa, G.U. Sumanasekera,
 R.R. Dharmadasa, M.B. Dergacheva, K.A. Mit, K.A. Urazov, L. Bowen, M. Walls and A. Abbas, Coating, 4, 380-415 (2014).
- [32] K.S. Balakrishnan and A.C. Rastogi, Solar Energy Materials, 20, 417-434 (1990).
- [33] E. Bertran, J.L. Morenza and J. Esteve, Thin Solid Film, **123**, 297-306 (1985).
- [34] W.J. Danaher, L.E. Lyons and G.C. Morris, Solar Energy Materials, 2, 137-148 (1985).
- [35] T.L. Chu, S.S. Chu, Prog. Photovoltaics: Res. Appl., 1, 31-42 (1993).
- [36] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Progress in Crystal Growth and Characterization of Materials, 52, 247-279 (2006).
- [37] X. Wu, Sol. Energy, 77, 803-814 (2004).
- [38] A.K. Mokhopadhyay, A.K. Chakraborty, A.P. Chatterjee and S.K. Lahiri, Thin Solid Film, 209, 92-96 (1992).