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Synchronization of a renewable energy inverter with the grid

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The design, mathematical analysis, and testing results of the architecture of a new all-digital phase-locked loop system for synchronizing a voltage source DC-AC single-phase inverter with the low voltage utility grid are presented. The system which is based on the time-delay digital tanlock loop was simulated using MATLAB/SIMULINK and was tested by subjecting the grid voltage to various perturbations similar to those which can occur in a real power system, such as voltage sags and nonlinear distortion of the grid voltage waveform. Results indicate that even in the presence of such perturbations the system achieved and/or re-gained synchronization within 100 ms. The proposed system is all-digital and can be readily implemented using a field programmable gate array and easily embedded into a power inverter. © *2012 American Institute of Physics*.
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I. INTRODUCTION

Due to their unsustainability and harmful effects on the environment, fossil fuels no longer stand as attractive sources of energy. International agreements and commitments for reducing carbon and other harmful emissions to the environment have recently been the driving force behind renewed interests in renewable energy sources (RES) such as wind and solar.[1–3] RES are clean and sustainable; they never run out and present no threat to the environment. Many power electronic systems have been described in the literature for harvesting renewable energy and converting into a useable form.[4,5] However, RES are intermittent because their output energy depends on weather conditions and consequently cannot be relied upon for continuous supply of electricity. To compact this problem, the harvested energy from a RES, such as a photovoltaic (PV) generator, may be used to charge a bank of batteries which is then used to feed a voltage source DC-AC inverter (VSI) to provide the AC voltage with the required amplitude and frequency. Such a "standalone" system depicted in Figure 1(a) is commonly used for lighting and water pumping in remote areas where a utility grid is not available. When a grid is available, the utilization of the above PV system may be enhanced by integrating it with the grid as depicted in Figure 1(b). In this grid-connected system, when the weather conditions are not conducive for energy generation and if the batteries are not fully charged, the load can be met by the grid. On the other hand, when the harvested renewable energy is in excess of the load demands, the excess energy can be fed back "sold" to the grid. However, before the inverter can be connected to the grid, its output voltage waveform must be synchronized with the grid voltage. Furthermore, because the grid voltage may occasionally be subjected to sudden and unpredicted perturbations such as voltage sag and/or a phase change, which may lead to loss of synchronization, the inverter must be able to re-establish synchronization.

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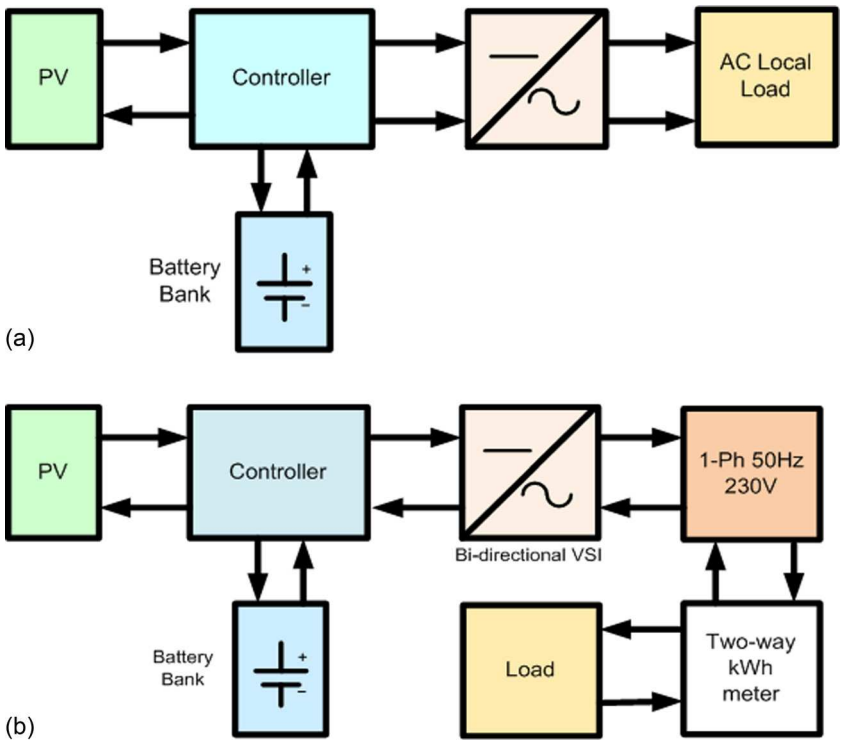

FIG. 1. (a) Standalone single-phase PV system. (b) A grid-connected single-phase PV system.

In addition, a grid-connected inverter must conform to some legal regulations set out by national regulatory bodies in order to regulate the penetration of external power into the grid.[6–8] Many circuits have been described in the literature for synchronizing an inverter to the grid.[9–12] They all implement one form or another of the well-known phase-locked loop (PLL) circuit which was invented in the early 1930s and has since then evolved into many different forms and types.[13–15]

In this paper, a new all-digital circuit topology for synchronizing a VSI to the grid is presented. The circuit not only can synchronize an inverter to the grid but also can re-gain synchronization whenever it is lost such as after an unanticipated perturbation in the phase, amplitude, or distortion of the grid voltage. The proposed circuit is based on the digital phase lock loop (DPLL) which has been extensively used in communications and signal processing systems that require phase tracking and synchronization.[15,16]

There are many types and forms of DPLLs, however, because sampling is a major operation in any DPLL, DPLLs are normally classified according to the nature of the sampling process they use as either uniform or non-uniform DPLLs. The non-uniform type of DPLLs offers better acquisition time and less circuit complexity compared to the uniform type, and hence attracted much of the research attention.[16]

There are two main types of non-uniform DPLLs; the zero crossing DPLL (ZCDPLL) and the digital tanlock loop (DTL).[16–18] Despite its simplicity and ease of implementation, the ZCDPLL has a major drawback due to its sensitivity to variation in the input signal power, which degrades its performance. This paved the way for the DTL to stand as an attractive alternative. Although, the DTL has many good attributes such as linearity and insensitivity to variation in the input signal power, its adoption has been hindered due to the fact that it uses a Hilbert Transformer (HT) which made its implementation fairly complex. This problem was later alleviated by replacing the HT with a fixed time-delay unit as proposed in the time-delay digital tanlock loop (TDTL).[16] In particular, the proposed system makes use of a variant of the TDTL due to the aforementioned advantages.[16–18] The system, depicted in Fig. 2, has been

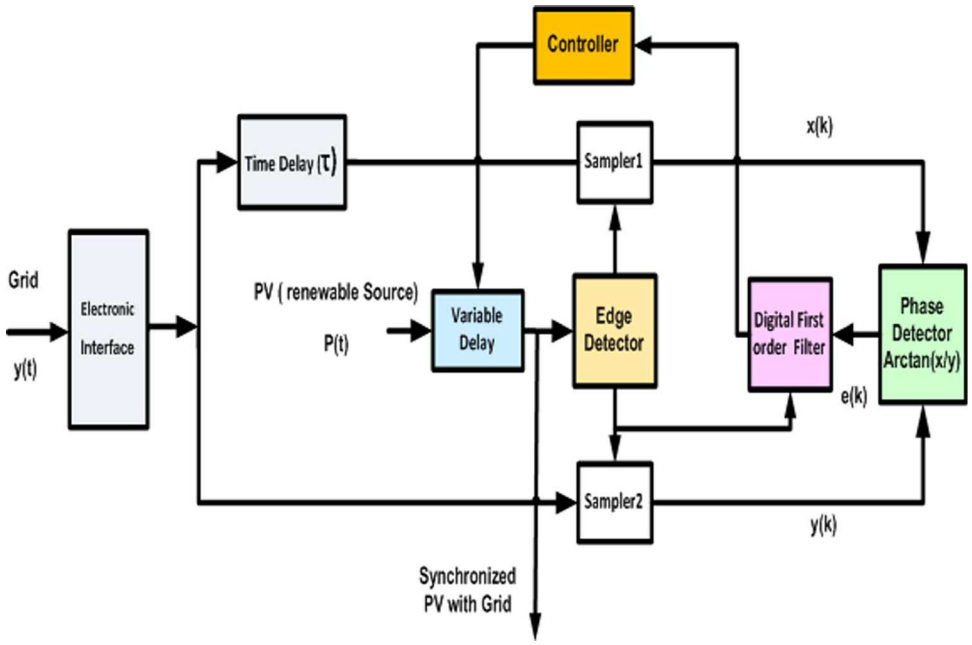

FIG. 2. Block diagram of the proposed synchronization system.

tested by simulation using MATLAB/SIMULINK software. A comprehensive set of testing results under various simulated conditions of the grid voltage are also presented. These include testing the system with phase step changes, voltage sags, and with harmonic distortion induced in the grid voltage. In addition, the system has the ability to re-establish synchronization even in the presence of nonlinear distortion which can considerably falsifies the zero-crossing points.

The design and mathematical modeling of the system are presented in Sec. II, whilst Sec. III presents the results of testing the system using the MATLAB/SIMULINK software. Section IV briefly highlights the implementation issues of the systems, whilst Sec. V presents the conclusions of the work.

II. ANALYSIS OF THE SYSTEM

The architecture of the proposed TDTL-based second-order digital synchronization system is depicted in the block diagram of Figure 2. The system consists of an arctan unit which is used as a phase detector, two sample-and-hold blocks, a first-order digital filter "the loop filter" and a fixed time delay module τ which is used to provide the required 90° phase shift for the 50 Hz grid voltage. In addition, the system has a controllable variable time delay module which is used in conjunction with the PV source voltage to emulate the functionality of the digital controlled oscillator (DCO) used in the conventional TDTL system.[16–18]

A continuous sinusoidal signal $y(t)$, representing the grid voltage, as defined by Eq. (1) with a phase offset $\omega(t - t_o)$ relative to the PV voltage waveform $P(t)$ is received by the proposed system, through an appropriate interface, as depicted in Figure 2. The times t and t_o are the times measured from the instant the two signals $y(t)$ and $P(t)$ are received by the system, respectively, and $\omega\,(\mathrm{rad/s})$ is the angular frequency. This is converted to a phase shift of the grid voltage $y(t)$ relative to the PV voltage $P(t)$ as demonstrated below.

$$\mathrm{y(t)} = \mathrm{Asin}(\omega \mathrm{t}), \tag{1}$$

where A is the input signal amplitude. The incoming signal $y(t)$ is passed through a fixed time delay unit τ which introduces a phase shift in $y(t)$. As a result, a phase shifted signal $x(t)$ of the input signal is generated and this is expressed as

$$\mathrm{x(t)} = \mathrm{Asin}(\omega \mathrm{t} - \psi). \tag{2}$$

The input signals $y(t)$ and its phase-shifted version $x(t)$ pass through their own individual sample-and-hold blocks. Consequently, they are sampled by the digitized PV source voltage $p(k) = A\sin[\omega_o t(k)]$, as illustrated in Figure 2, and sampled versions both signals (1) and (2) can be written as

$$\mathrm{y(k)} = \mathrm{Asin}[\omega \mathrm{t(k)}] \tag{3}$$

and

$$\mathrm{x(k)} = \mathrm{Asin}[\omega \mathrm{t(k)} - \psi]. \tag{4}$$

The sampling interval between the sampling instants $t(k)$ and $t(k-1)$ is given by

$$\mathrm{T(k)} = \mathrm{T} - \mathrm{c(k-1)}, \tag{5}$$

where $T = 2\pi/\omega$ is the period of the PV source and $c(i)$ is the output of the digital filter at the ith sampling instant that is used to drive the variable time delay unit in order to provide the required phase shift which is simply emulating the DCO in the conventional TDTL. By assuming $t(0) = 0$, the elapsed time up to the kth sampling instant is given by

$$\mathrm{t(k)} = \sum_{\mathrm{i=1}}^{\mathrm{k}} \mathrm{T(i)} = \mathrm{kT} - \sum_{\mathrm{i=0}}^{\mathrm{k-1}} \mathrm{c(i)}. \tag{6}$$

As a result, both $\mathrm{y(k)}$ and $\mathrm{x(k)}$ are written as

$$\mathrm{y(k)} = \mathrm{Asin}\left[-\omega \sum_{\mathrm{i=0}}^{\mathrm{k-1}} \mathrm{c(i)}\right] \tag{7}$$

and

$$\mathrm{x(k)} = \mathrm{Asin}\left[-\omega \sum_{\mathrm{i=0}}^{\mathrm{k-1}} \mathrm{c(i)} - \psi\right]. \tag{8}$$

Therefore, the phase error between the input grid signal $y(t)$ and the PV signal $P(t)$ can be defined as

$$\phi(\mathrm{k}) = -\omega \sum_{\mathrm{i=0}}^{\mathrm{k-1}} \mathrm{c(i)} - \psi. \tag{9}$$

Both Eqs. (7) and (8) can be expressed in term of phase error as

$$\mathrm{y(k)} = \mathrm{Asin}[\phi(\mathrm{k}) + \psi] \tag{10}$$

and

$$\mathrm{x(k)} = \mathrm{Asin}[\phi(\mathrm{k})]. \tag{11}$$

Therefore, the loop error signal $e(k)$ produced by the phase detector can be expressed as

$$e(k) = f\left[\tan^{-1}\left(\frac{\sin[\phi(k)]}{\sin[\phi(k)+\psi]}\right)\right], \tag{12}$$

where $f(\gamma) = -\pi + [(\gamma + \pi) \bmod (2\pi)$. This error signal $e(k)$ represents the nonlinear phase error whose effect on the nonlinearity of the system worsens as the value of the phase shift ψ departs away from $\pi/2$ radians. The digital loop filter with a transfer function $D(k)$ receives the error signal $e(k)$ and produces the signal $c(k)$ that drives the variable time-delay through the controller to the required phase shift for synchronizations purpose. Consequently and by assuming that the grid has the same frequency as that of the PV source, the system difference equation can be derived from Eqs. (6) and (9) as

$$\phi(k+1) = \phi(k) - \omega c(k). \tag{13}$$

The second-order loop utilizes a proportional plus accumulation digital filter transfer function $D(k)$ which is given as

$$D(z) = G_1 + G_2/(1 - z^{-1}), \tag{14}$$

where G_1 and G_2 are positive constants. From Eqs. (13) and (14), the system difference equation of the second-order TDTL can be achieved as

$$\phi(k+2) = 2\phi(k+1) - \phi(k) - rK_1 h[\phi(k+1)] + K_1 h[\phi(k)], \tag{15}$$

where $r = 1 + G_2/G_1$ and $K_1 = G_1\omega$. Following the same procedure with a fixed-point analysis as in Refs. 15–17, the second-order TDTL lock range is defined by the inequality

$$0 < K_1 < \frac{4}{1+r}\sin(\psi_o), \tag{16}$$

where ψ_o is the nominal phase lag induced in the incoming signal by the time delay unit. If the phase shift is $\psi_o = \pi/2$, then the lock range of the system depends only on the filter coefficients

$$0 < K_1 < \frac{4}{1+r}. \tag{17}$$

For the system to be stable the value of K_1 must be selected so that inequality (17) is satisfied.

III. RESULTS

The synchronization system presented in this paper has been thoroughly tested to evaluate its suitability for locking. The test was carried out with an input signal voltage which has an amplitude of 325 V and frequency of 50 Hz. The TDTL parameters were as follows: $K_1 = 1$, $r = 1.2$, $G_1 = 0.00318$, and $G_2 = 0.000635$. The tests involved synchronizing the PV source with the grid voltage under normal and abnormal conditions. The system was subjected to abnormal disturbances in the grid voltage which led to loss of synchronization in order to evaluate its ability to re-gain lock after each disturbance. This section presents some of these tests which all indicate that the synchronization system is capable of achieving the desired locking state following adverse changes in the grid voltage waveform. Although, in practice the inverter has to be isolated from the grid in such conditions,[6–8] the ultimate objective of the tests was to demonstrate the versatility of the system.

In one test, a positive phase step with additive white Gaussian noise (AWGN) as shown in Figure 3(a) was induced in the grid voltage with a signal-to-noise ratio (SNR) of 20 dB. The phase error, Figure 3(b), and the phase plane of Figure 3(c) indicate that synchronization was successful even in the presence of this AWGN.

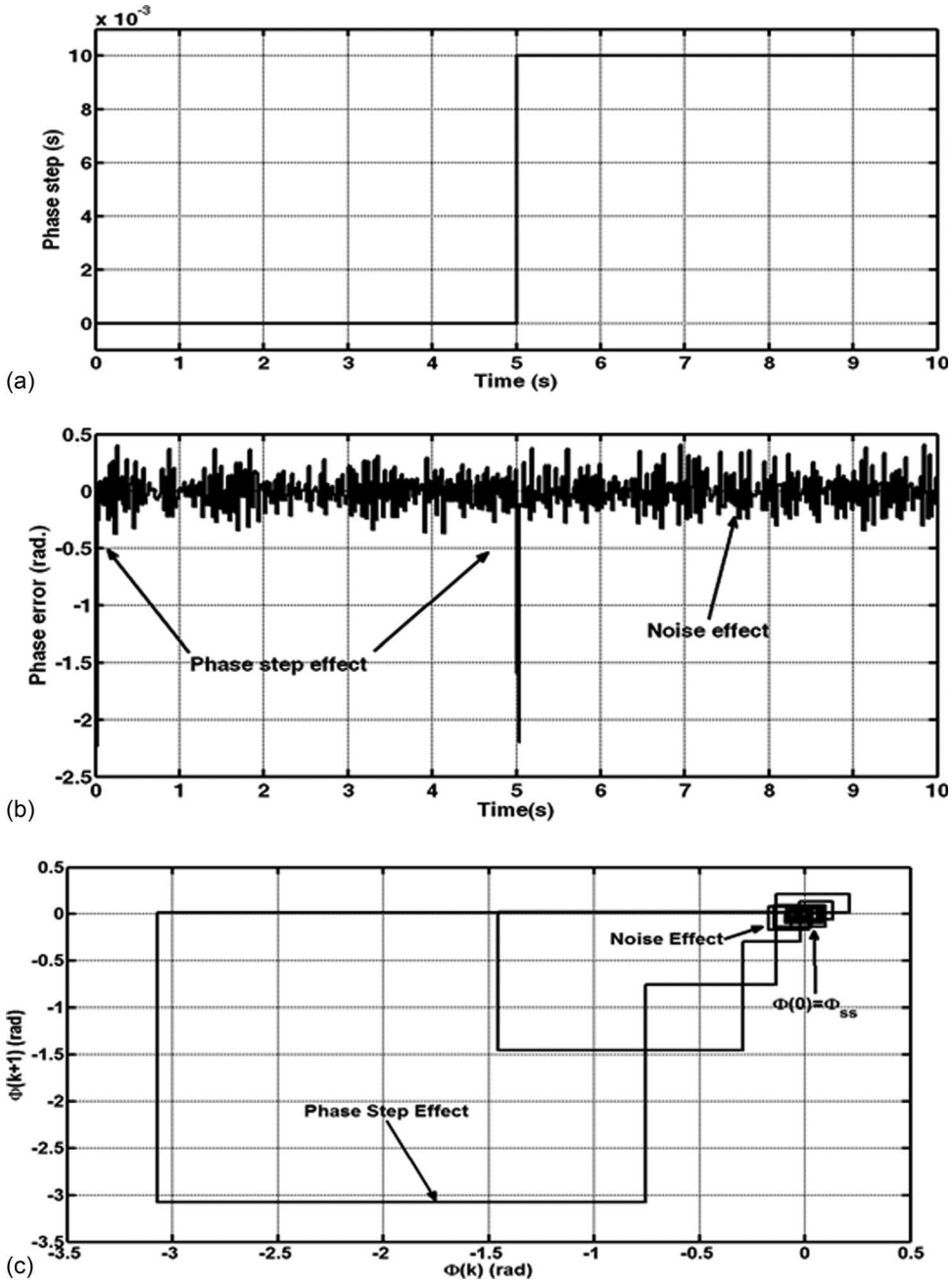

FIG. 3. (a) Input phase step. (b) Phase error for phase step input. (c) Phase plane for phase step.

Another test involved injecting the grid waveform with a positive step input with a very high total-harmonic distortion (THD) of 80% as illustrated in Figure 4(a). The phase error of Figure 4(b) indicates that the system achieved synchronization within 200 ms. Such an adverse condition is, however, unlikely to occur in practice. In a similar test but without the distortion the system achieved synchronization within 100 ms as shown in Figure 4(c).

The synchronization ability of the system to deal with consecutive input steps with a THD of 35% is shown in Figure 5. The distorted grid voltage is shown in Figure 5(a) and the injected train of input phase steps is shown in Figure 5(b). The transient response and associated phase plane plots, for the distorted grid signal, are shown in Figs. 5(c) and 5(d),

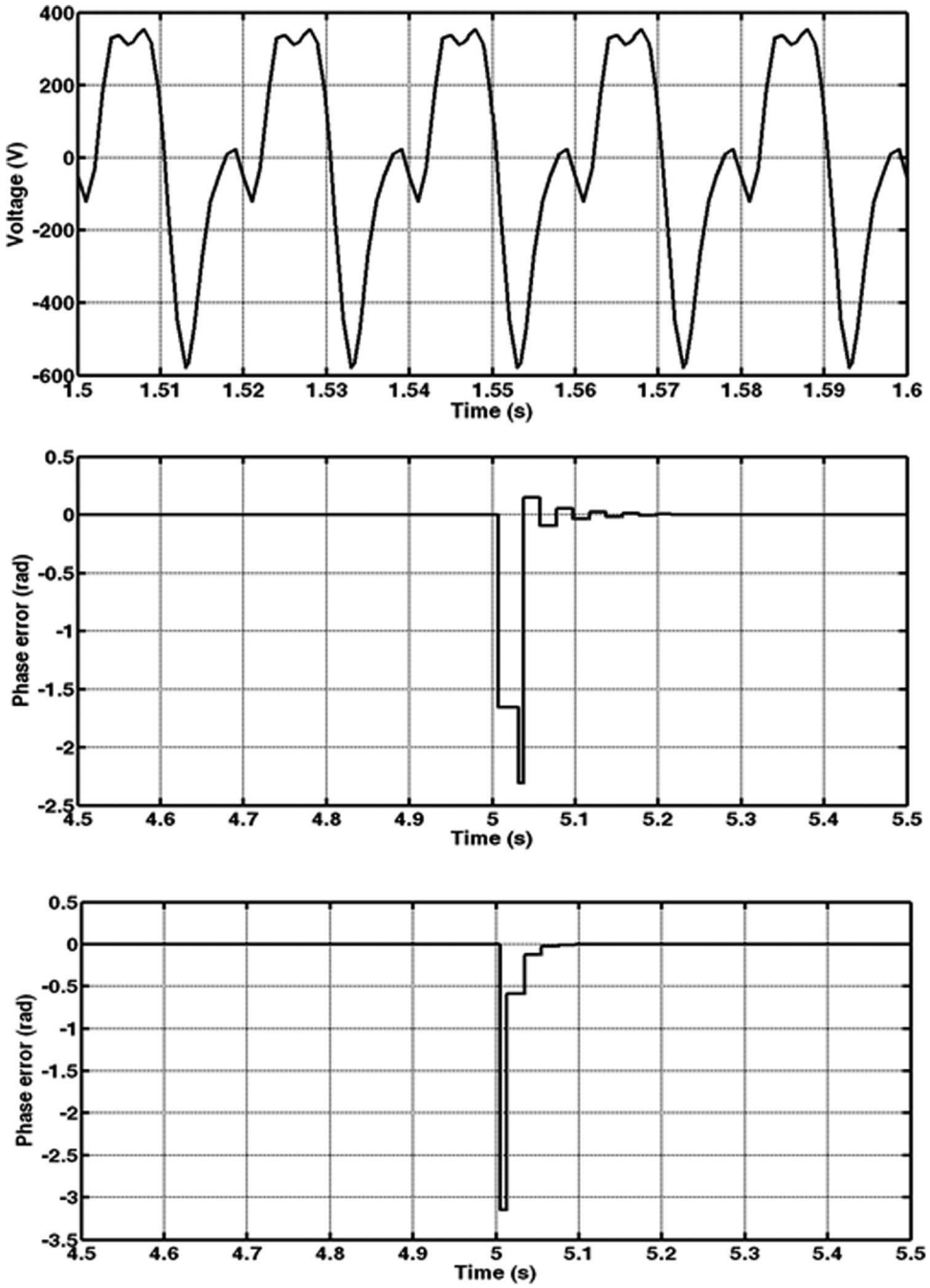

FIG. 4. (a) Grid signal with 80% THD. (b) Phase error for input phase step with 80% THD. (c) Phase error for input phase step without distortion.

respectively. This is in comparison with consecutive input steps without grid distortion signal which are shown in Figs. 5(e) and 5(f), respectively. The results show that the system achieves locking when subjected to consecutive phase error steps even with a distorted grid voltage.

The response of the synchronization system to variations in the input signal phase in the form of a ramp is shown in Figure 6. The results shown in Figs. 6(b) and 6(c) illustrate that the system achieves locking. However, the locking in this case includes a very small residual constant shift that is not enabling convergence to exactly zero as obviously desired. This is basically attributed to the selection of the filter parameters and value of the variable delay. Both of

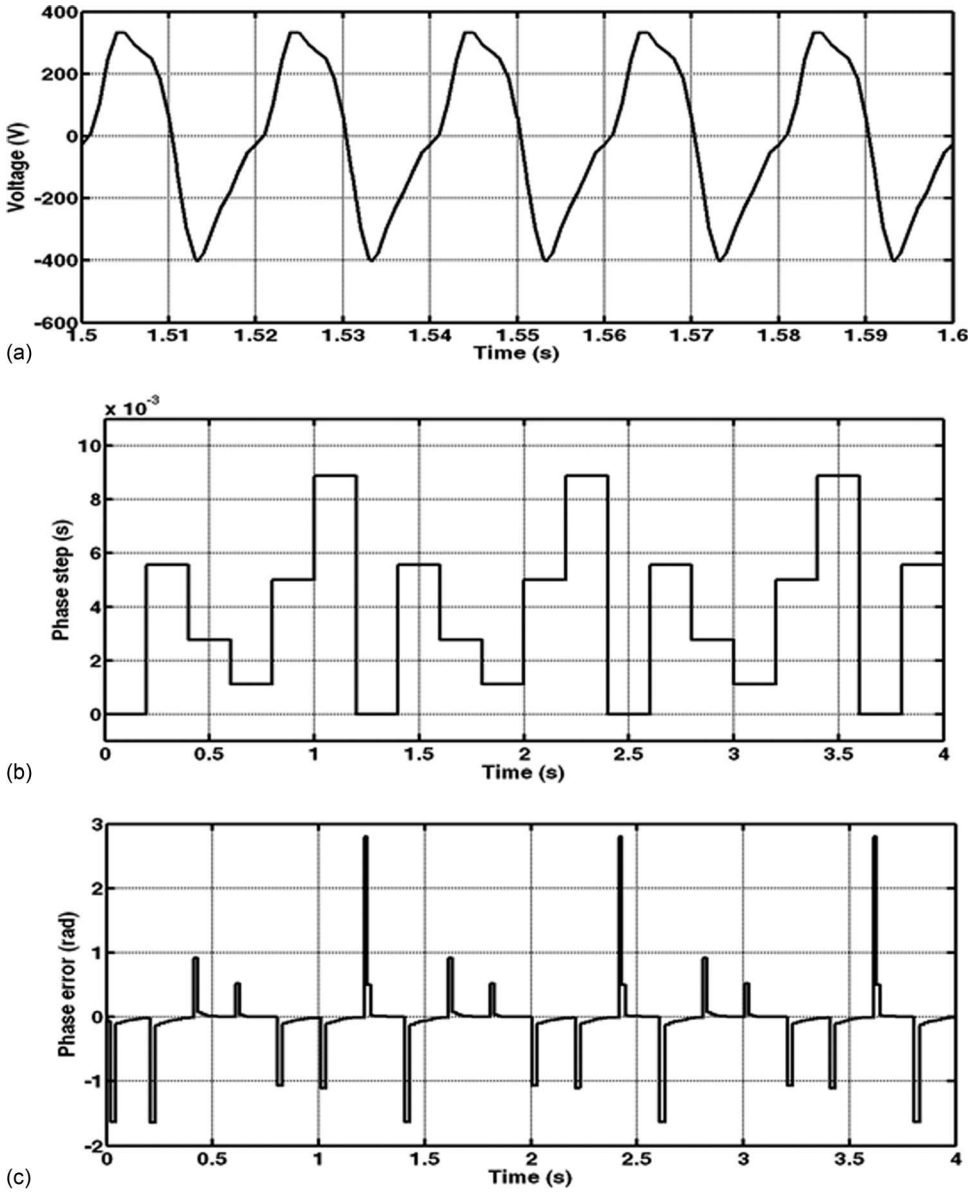

FIG. 5. Grid signal with 35% THD. (b) Consecutive input phase step. (c) Phase error for consecutive input phase step with 35% THD. (d) Phase plane for consecutive phase steps with 35% THD. (e) Phase error for consecutive input phase step without distortion. (f) Phase plane for consecutive phase steps.

these can be refined depending on the actual implementation conditions. The fact that the constant shift is very small indicates that successful locking has been achieved.

Finally, the synchronization system was tested after inducing a voltage sag in the grid voltage as depicted in Figure 7(a). The phase error plot and the phase plane error for this test shown in Figures 7(b) and 7(c) indicate that the system was successful in achieving synchronization in less than 200 ms.

IV. IMPLEMENTATION

The feasibility and practical circuit implementation of the system using a field programmable gate array (FPGA) was performed and assessed in an earlier work using a similar

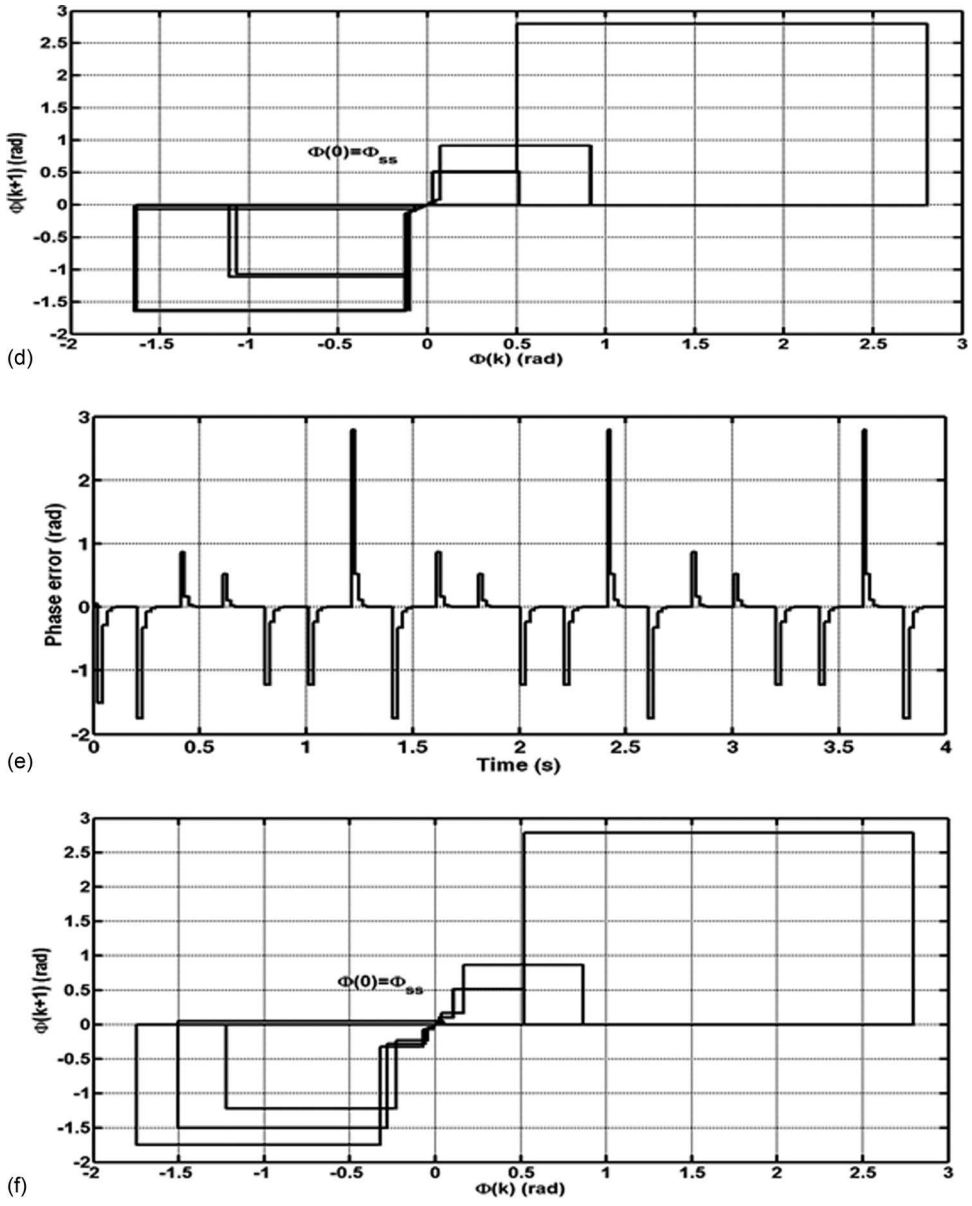

FIG. 5. (*Continued*).

system.[17,18] It is shown that the real-time performance of the TDTL compares favorably with the simulation results obtained from the MATLAB/SIMULINK model. The synthesis process of the prototype system used Xilinx System Generator to generate the necessary hardware description language (HDL) for the device-optimized block-set from within SIMULINK.

V. CONCLUSION

The architecture of a new circuit topology of a digital phase-locked loop based on the TDTL has been presented. The system does not require a DCO and is all-digital which simplifies its implementation. The system was constructed and tested using MATLAB/SIMULINK. Synchronization between the grid and PV source was achieved by the proposed system. The system

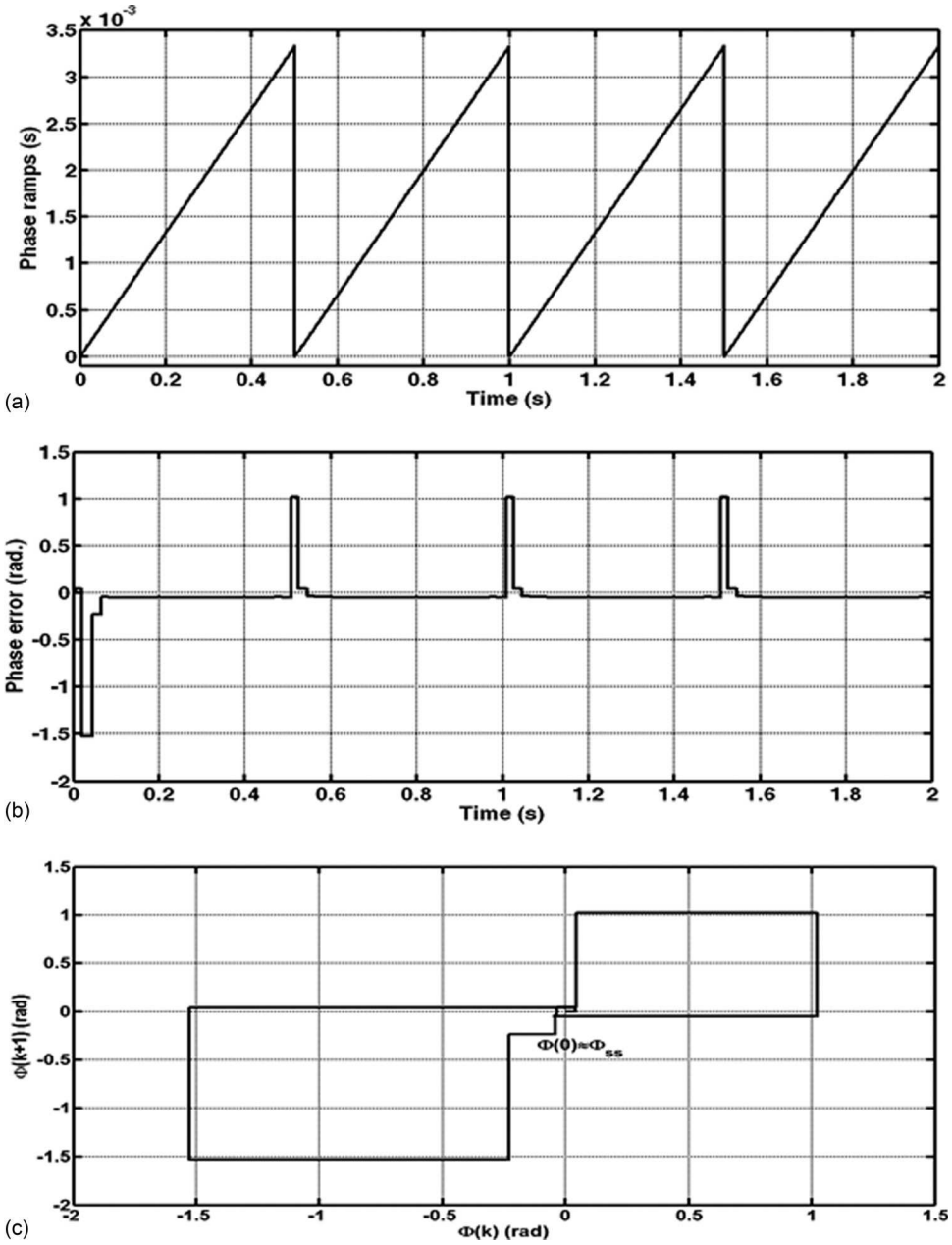

FIG. 6. (a) Consecutive input ramp phase. (b) Phase error for the input consecutive ramp phase step. (c) Phase plane for the input consecutive ramp phase step.

was tested by applying a single phase step and consecutive phase steps to the grid with and without AGWN. The system achieved synchronization in less than 100 ms. Tests were also performed with simulated voltage sags and with noise injection into the grid voltage. Adequate response was observed even when the grid voltage was distorted by noise, and/or the harmonic distortion which consequently falsifies the zero-crossings of the grid voltage. This doubled the time taken to achieve synchronization compared to the case without harmonic distortion. However, the severity of the simulated conditions, e.g., 80% harmonic distortion, is unlikely to occur in practice due to various strict national regulations on the quality of the grid voltage waveform.

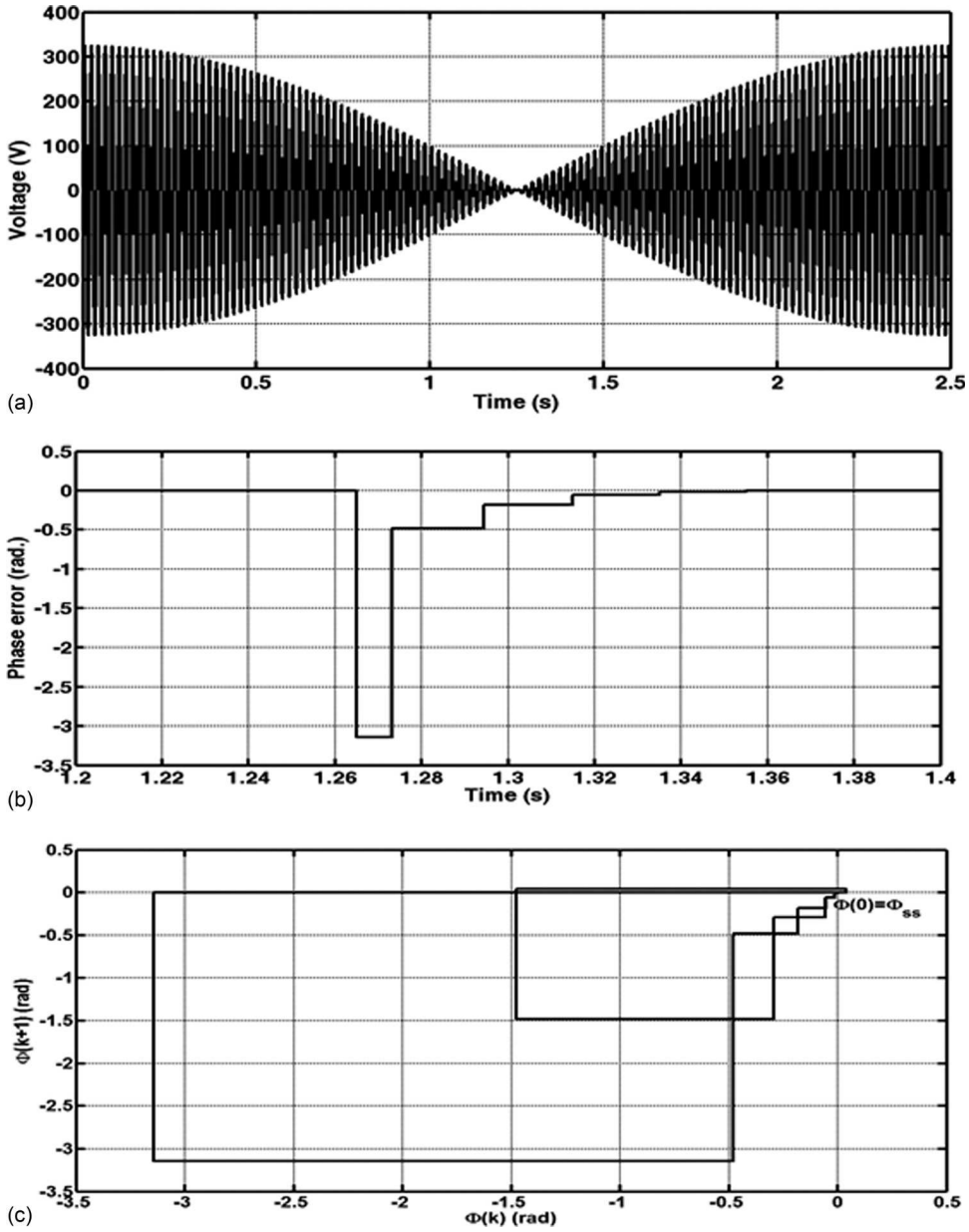

FIG. 7. (a) Input ramp phase. (b) Phase error for voltage sag. (c) Phase plane for the Input consecutive ramp phase step.

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