Real-Time Grid Parameter Estimation methods using Model based Predictive Control for Grid-Connected Converters

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Abstract

In recent years, renewable and distributed generation (DG) systems have contributed towards an efficient and an economic way of transporting electricity to end-users as the generation sources are in general located nearer the loads. DG and renewable energy systems are modifying the old concept of distribution network by instigating a bi-directional power flow into the grid, facilitated through the use of power electronic grid-connected converters.

A challenge associated with grid-connected converters arises when they are interacted with a grid that is not stiff, like weak micro grids. Small grid parameter variations in these systems can considerably affect the performance of the converter control and lead to higher values in current total harmonic distortion (THD) and loss of control and synchronization. Thus, the control of grid-connected power converters needs to be regularly updated with latest variation in grid parameters.

Model Predictive Direct Power Control (MP-DPC) has been chosen as the control strategy for the work presented in this thesis due to its advantages over traditional control techniques such as multivariable control, no need of phase-locked loops (PLLs) for grid synchronization and avoidance of cascaded control loops.

Two novel methods for estimating the grid impedance variation, and hence the grid voltage, are presented in this thesis along with a detailed literature review on control of grid-connected converters with special emphasis on impedance estimation techniques. The first proposed estimation method is based on the difference in grid voltage magnitudes at two consecutive sampling instants while the second method is based on a model-fitting algorithm similar to the concept of cost-function optimization in model

predictive control. The proposed estimation methods in this thesis are integrated within the MP-DPC, therefore updating the MP-DPC in real-time with the latest variation in grid impedance. The proposed algorithms provide benefits such as: quick response to transient variations, operation under low values of short-circuit-ratio (SCR), robust MP-DPC control, good reference tracking to grid parameter variations and operation under unbalanced grid voltages. The thesis also presents the advantages and drawbacks of the proposed methods and areas where further improvement can be researched.

The work presented has been tested on a three phase two-level grid-connected converter prototype, which is connected to a low voltage substation highly dominated by inductive component of grid impedance. It can be adapted and modified to be used for general grid impedance estimation, medium or high voltage applications, in case of multilevel grid-connected converter topologies or photo-voltaic (PV) grid-connected applications.

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Table of Contents

Abstract i
Acknowledgement iii
Table of Contents iv
List of Figures ix
List of Tables xx
Nomenclature xxi
Chapter 1: Background and motivation 1
1.1 Introduction 2
1.1.1. Background and motivation 2
1.1.2. Weak Grid 6
1.2. Objectives of the project 7
1.3. Thesis structure 9
1.4. Contribution of thesis 11
1.5. Conclusion 13
Chapter 2: Introduction to converters, control techniques, modulation techniques and grid impedance estimation techniques 14
2.1. Introduction 15
2.2. Grid Connected Converters 15
2.2.1. Two-level Converter 18
2.2.1.1. AC-DC 20
2.2.1.2. DC-AC 21
2.2.1.3. AC-AC 21
2.3. Control of 3-phase 2-level grid-connected converter 22
2.3.1. Transformation and Angle Calculation - A 23
2.3.1.1. SRF-PLL 24
2.3.1.2. P-PLL 27
2.3.1.3. DSOGI-PLL 31
2.3.2. Control Techniques - B 34
2.3.2.1. DQ control 34
2.3.2.2. PR Control 35
2.3.2.3. Hysteresis Control 37
2.3.3. Modulation Strategies - C 39

Table of Contents

2.3.3.1. SPWM 39
2.3.3.2. SVM 40
2.3.4 Summary 42
2.4. Grid impedance estimation techniques 44
2.4.1. Estimation using a controlled voltage disturbance 45
2.4.2. Estimation based on active power variations 46
2.4.3. Estimation based on Virtual-Flux-Based Predictive Direct Power Control 49
2.4.4. Estimation based on active and reactive power samples before and after a commutation 51
2.5. Conclusion 53
Chapter 3: Predictive Control 56
3.1. Introduction 57
3.2. Predictive control for power converters 57
3.3. Deadbeat Control 59
3.4. Model Predictive Control 62
3.4.1. General concept of MPC 62
3.4.2. Sampling intervals in MPC 63
3.4.3. FCS-MPC Current Control 64
3.4.3.1. Measurements at instant k - A 64
3.4.3.2. Predictions at instant k+1 - B 65
3.4.3.3. Delay compensation - C 66
3.4.3.4. Cost-function optimization - D 67
3.4.4. Application of MPC 68
3.4.5. Comparison between CCS-MPC and FCS-MPC 71
3.5. Conclusion 74
Chapter 4: Model Predictive Direct Power Control with online Grid Inductance estimation methods 75
4.1. Introduction 76
4.2. Model Based Predictive Direct Power Control 78
4.2.1. Current Predictions 81
4.2.2. Converter voltage calculations 82
4.2.3. DC-Link Voltage Prediction 86
4.2.4. Two sample-ahead prediction 87
4.2.5. Active and Reactive Power Predictions 89

Table of Contents

4.2.6. DC-Link voltage reference calculation 90
4.2.7. Active and Reactive Power reference calculation 92
4.2.8. Cost-function optimization 95
4.3. Dead-time Compensation 99
4.3.1. Methodology 101
4.4. Grid Impedance Estimation Algorithm 102
4.4.1. Background 102
4.4.2. Inductance Estimation Algorithm – Method 1 104
4.4.2.1. Working Principle 104
4.4.2.2. Grid Voltage Estimation 110
4.4.2.3. Integration of grid inductance and voltage estimation with MP-DPC 111
4.4.3. Inductance Estimation Algorithm – Method 2 112
4.4.3.1. Working Principle 112
4.4.3.2. Cost function optimization 114
4.4.4. Remarks 118
4.5. Conclusion 121
Chapter 5: Simulation Results 123
5.1. Introduction 124
5.2. Simulation tests platform 124
5.3. Model based Predictive Direct Power Control on a 3-Phase 2-Level AFE 128
5.3.1. Model Predictive Direct Power Control: Past, Present and Future sampling intervals 128
5.3.2. DC-link voltage with different values of N* 129
5.3.3. Active and reactive power response to a step in DC-Link voltage reference 130
5.3.4. Reactive power variation 132
5.3.5. Effect on MP-DPC with Grid inductance variation 135
5.4. Predictive Direct Power Control with presence and online estimation of Grid inductance 139
5.4.1. Online estimation using Method 1 139
5.4.2. Online inductance estimation for a step in reactive power 146
5.4.3. Online estimation for a large variation in grid inductance 148
5.4.4. Online estimation and presence of Dead-Time for converter switches 149
5.4.5. Online estimation in the presence of a grid capacitance 150
5.4.6. Online estimation with unbalanced grid voltages 151
5.4.7. Effect of measurement noise 155

Table of Contents

5.5. Model based Predictive Direct Power Control with online predictive model fitting algorithm for online grid inductance estimation 157
5.5.1. Online estimation using Method 2 157
5.5.2. Frequent step variation in grid inductance 158
5.5.3. Online estimation in case of a large step in grid inductance 160
5.5.4. Online estimation with reactive power variation 161
5.5.5. Online estimation in the presence of a grid capacitance 162
5.5.6. Online estimation with unbalanced grid voltages 163
5.5.7. Effect of measurement noise 167
5.6. Conclusion 169
Chapter 6: Experimental Setup and Results 171
6.1. Introduction 172
6.1.1 Experimental setup 173
6.1.1.1. Voltage and Current measurement 173
6.1.1.2. System Parameters 174
6.1.2. Control board and AFE 175
6.2. Experimental Results using a Programmable Voltage Source 178
6.2.1. DC-Link voltage regulation procedure 180
6.2.2. Step in dc-link voltage reference 181
6.2.3. Step in reactive power reference 184
6.3. Experimental Results using a VARIAC 186
6.3.1. Model Predictive Control with grid inductance estimation in the presence of a step of supply voltage 186
6.4. Comparison between the simulation and experimental results using estimation method 1 192
6.5. Comparison between the simulation and experimental results using estimation method 2 199
6.6. Conclusion 202
Chapter 7: Discussion, Conclusion and Further Work 204
7.1. Background 205
7.2. Grid impedance estimation techniques 207
7.3. Further work suggestions 210
References 214
Appendix A: Short Circuit Ratio (SCR) Calculations 225
Appendix B: Mathematical model of the system 229
Appendix C: Clarke's Transformation 232

Table of Contents

Appendix D: Dead-Time block in MATLAB/SIMULINK 233
Appendix D.1: Dead-Time generation code 233
Appendix E: Experimental results from oscilloscope for MP-DPC with estimation methods 235

List of Figures

Figure 1.1	*Classical electrical grid structure*	*3*
Figure 1.2	*Contribution of renewable energy generation in the total electrical energy demand*	*4*
Figure 1.3	*Present electrical grid structure with distributed generation systems*	*5*
Figure 1.4	*Equivalent grid impedance model*	*6*
Figure 2.1	*Equivalent representation of a grid connected converter*	*16*
Figure 2.2	*Operation points of grid-connected converters in their P and Q representation*	*18*
Figure 2.3	*Three phase two-level converter*	*18*
Figure 2.4	*Block diagram for Voltage Oriented Control of a two-level converter*	*22*
Figure 2.5	*Basic scheme of a PLL*	*23*
Figure 2.6	*Three phase SRF-PLL structure*	*24*
Figure 2.7	*SRF-PLL, K_p = 100, K_i = 500*	*26*
Figure 2.8	*SRF-PLL, K_p = 10, K_i = 50*	*27*
Figure 2.9	*P-PLL block diagram*	*28*
Figure 2.10	*P-PLL, K_p=100, K_i = 500*	*29*
Figure 2.11	*P-PLL, K_p=10, K_i = 50*	*30*
Figure 2.12	*SOGI filter*	*32*
Figure 2.13	*Three phase dual SOGI-PLL structure*	*32*
Figure 2.14	*DSOGI-PLL, $K_{p=}$500, K_i=100*	*33*
Figure 2.15	*d-q representation of supply side of the rectifier*	*35*

List of Figures

Figure 2.16	*Proportional Resonant Controller*	*36*
Figure 2.17	*Basic scheme of hysteresis current control*	*37*
Figure 2.18	*Switching signal generation in Hysteresis Control*	*38*
Figure 2.19	*PWM generation*	*39*
Figure 2.20	*PWM generation using SPWM*	*40*
Figure 2.21	*PWM generation using SVM*	*41*
Figure 2.22	*Switching Pulse Pattern for Sector I*	*42*
Figure 2.23	*Grid impedance representation for a three-phase grid-connected converter*	*44*
Figure 2.24	*Grid impedance estimation from* [1]	*45*
Figure 2.25	*Working principle of* [63]	*48*
Figure 2.26	*Experimental validation of grid impedance estimation in* [63]	*48*
Figure 2.27	*Working principle of* [61]	*50*
Figure 2.28	*Inductance estimation for* [61]	*51*
Figure 2.29	*Working principle of* [64]	*52*
Figure 2.30	Percentage of error in inductance estimation [64]	53
Figure 3.1	*Characteristics of power converters and modern control systems demands*	*58*
Figure 3.2	*Basic scheme of digital deadbeat current control*	*59*
Figure 3.3	*Basic operation of deadbeat current control*	*60*
Figure 3.4	*General working principle of model predictive control*	*62*
Figure 3.5	*Sampling intervals for MPC*	*63*

List of Figures

Figure 3.6	*Basic FCS-MPC current control scheme for power converters*	*64*
Figure 3.7	*Switching state selection principle for FCS-MPC*	*67*
Figure 3.8	*Contribution of MPC in 4 respective areas from 2007-2014*	*69*
Figure 3.9	*Increasing trend of MPC research work in 4 respective areas from 2007-2014*	*70*
Figure 3.10	*Steady state switching state, THD and current ripple comparison between CCS1, CCS2, FCS* [99]	*71*
Figure 3.11	*Comparison between (a) CCS1, (b) CCS2 and (c) FCS to a step variation in current reference* [99]	*73*
Figure 4.1	*Grid-connected active front end (AFE) rectifier*	*77*
Figure 4.2	*Past, Present and Future (Prediction) sample instants*	*82*
Figure 4.3	*Three phase two-level voltage source converter*	*82*
Figure 4.4	*Equivalent AFE model in α-β reference frame*	*87*
Figure 4.5	*Past, Present, future[1] and future[2] sampling instants*	*88*
Figure 4.6	*Simplified explanation on importance of N**	*91*
Figure 4.7	*Equivalent representation of a 3-phase Active Front End*	*92*
Figure 4.8	*Active Power Predictions for the eight switching combinations and its reference*	*97*
Figure 4.9	*Block Diagram of the MP-DPC*	*98*
Figure 4.10	*Basic Configuration of one leg of three phase AFE during dead-time*	*99*
Figure 4.11	*Dead-time in upper and lower switch of leg-A in a 3-phase 2-level AFE*	*100*

List of Figures

Figure 4.12	*Grid voltage representation in α-β*	*104*
Figure 4.13	*Current and converter voltage terms used in the inductance estimator*	*107*
Figure 4.14	*Block Diagram of MP-DPC with Inductance Estimator method 1*	*109*
Figure 4.15	*Relation between number of iterations and accuracy of inductance estimation*	*116*
Figure 4.16	*Block Diagram of MP-DPC with Inductance Estimator method 2*	*117*
Figure 4.17	*Case 1 of grid capacitance presence*	*119*
Figure 4.18	*Case 2 of grid capacitance presence*	*120*
Figure 5.1	*Matlab SIMULINK schematic*	*125*
Figure 5.2	*Three phase Two-level grid connected converter on PLECS*	*127*
Figure 5.3	*Current samples future[2], future[1], present and past*	*128*
Figure 5.4	*DC-Link voltage with different values of N**	*129*
Figure 5.5	*DC-Link voltage with reference N* = 150*	*131*
Figure 5.6	*Active and reactive power with reference*	*131*
Figure 5.7	*Supply current and Grid Voltage in synchronization*	*132*
Figure 5.8	*Active and reactive power with reference to variation in reactive power reference*	*133*
Figure 5.9	*DC-Link voltage to variation in reactive power reference*	*133*
Figure 5.10	*Supply current and Grid Voltage before step in reactive power reference from 0VAR to +2kVAR*	*134*
Figure 5.11	*Supply current and Grid Voltage after step in reactive power reference from 2 kVAR to -1*	*134*

List of Figures

	kVAR	
Figure 5.12	*Grid connected converter with supply impedance*	*135*
Figure 5.13	*Supply current and Grid Voltage with L_S= 10%L_C without grid impedance compensation. THD_i = 7.6%, THD_{Vpcc} = 5.9%*	*135*
Figure 5.14	*Corresponding active and reactive powers for L_S= 10%L_C*	*136*
Figure 5.15	*Corresponding DC-link voltage for L_S= 10%L_C*	*137*
Figure 5.16	*Supply current and Grid Voltage with L_S= 30%L_C without estimation. THD_i = 24.36%, THD_{Vpcc} = 16.17%*	*137*
Figure 5.17	*Corresponding active and reactive powers for L_S= 30%L_C*	*138*
Figure 5.18	*Corresponding DC-link voltage for L_S= 30%L_C*	*138*
Figure 5.19	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 10%L_C value (i.e. L_S = 0.45mH) as compared to L_C. THD_{Vpcc}=5.56%, THD_{Vg-est}=0.51%, THD_i=5.52%*	*139*
Figure 5.20	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 30%L_C (i.e. L_S = 1.35mH) as compared to L_C. THD_{Vpcc}=13.7%, THD_{Vg-est}=0.73%, THD_i=4.82%*	*140*
Figure 5.21	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 50%L_C (i.e. L_S = 2.25mH) as compared to L_C. THD_{Vpcc}=21%, THD_{Vg-est}=1.0%, THD_i=4.15%*	*140*
Figure 5.22	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 100%L_C (i.e. L_S = 4.5mH) as compared to L_C. THD_{Vpcc}=30.9%, THD_{Vg-est}=1.4%, THD_i=3.2%*	*141*

List of Figures

Figure 5.23(a)	*Total Inductance estimation with a frequent variation in grid inductance*	*143*
Figure 5.23(b)	*Active and reactive power response to a frequent variation in grid inductance*	*144*
Figure 5.24	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 200%L_C (L_S = 9mH) as compared to L_C. THD_{Vpcc}=42.5%, $THD_{Vg\text{-}est}$=1.89%, THD_i=2.87%*	*144*
Figure 5.25	*Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= ~400%L_C (i.e. L_S = 17.5mH) as compared to L_C. THD_{Vpcc}=43%, $THD_{Vg\text{-}est}$=2.05%, THD_i=2.53%*	*144*
Figure 5.26	*Short Circuit Ratio to grid inductance comparison*	*145*
Figure 5.27	*Active and Reactive powers with steps in reactive power reference and estimated total inductance with L_S= 300%L_C (i.e. L_S = 13.5mH) to L_C*	*146*
Figure 5.28	*Supply current, PCC voltage, grid Voltage estimation with L_S= 300%L_C (13.5mH) as compared to L_C and step in reactive power reference*	*147*
Figure 5.29	*Total Inductance estimation, supply current, PCC voltage, and grid voltage estimation with 67% step in L_S value (L_S = 0.5mH to 3.0mH)*	*148*
Figure 5.30	*Comparison of total inductance estimation with and without the dead-time compensation*	*149*
Figure 5.31	*Equivalent model with grid capacitance*	*150*
Figure 5.32	*Total inductance estimation with a presence of 100µF grid capacitance*	*151*
Figure 5.33	*Effect of unbalanced grid voltages*	*154*
Figure 5.34	*Estimation method 1, effect of noise on total estimation*	*156*

List of Figures

Figure 5.35	*Grid voltage estimation, PCC voltage, supply current and grid inductance estimation with L_S=50%L_C (L_S = 2.25mH) as compared to L_C*	*157*
Figure 5.36	*Grid voltage estimation, PCC voltage, supply current and grid inductance estimation with L_S=100%L_C*	*158*
Figure 5.37	*Grid inductance estimation with frequent variation*	*159*
Figure 5.38	*Active and reactive powers, DC-link voltage with references to a frequent variation in L_S*	*160*
Figure 5.39	*Grid inductance estimation for high grid inductance values*	*160*
Figure 5.40	*L_S estimation, supply current, PCC voltage, and grid voltage estimation with 67% step in L_S value (L_S = 0.5mH – 3.0mH) when L_C = 4.5mH*	*161*
Figure 5.41	*Active and Reactive powers with steps in reactive power reference and L_S inductance with L_S=100%L_C*	*162*
Figure 5.42	*Grid inductance estimation with a presence of 100µF grid capacitance*	*163*
Figure 5.43	*3-phase unbalance grid voltages and respective supply currents*	*164*
Figure 5.44	*Total inductance estimation for unbalance grid voltage condition*	*165*
Figure 5.45	*Grid voltage estimation, PCC voltage and supply current*3 for phase A with unbalanced grid voltage condition and L_S=100%L_C, L_S=4.5mH, L_C = 4.5mH*	*165*
Figure 5.46	*Active and reactive powers with their respective references for unbalanced grid voltage condition*	*166*
Figure 5.47	*Estimation method 2 effect of measurement noise*	*168*
Figure 6.1	*Experimental arrangement circuit diagram*	*172*

List of Figures

Figure 6.2	*Experimental Set-up*	*174*
Figure 6.3	*Three phase two-level active rectifier set-up*	*175*
Figure 6.4	*Block diagram of the control implementation*	*177*
Figure 6.5	*PCC voltage, supply current and grid voltage estimation – phase A*	*179*
Figure 6.6	*Total Inductance estimation – L_S = 3.0mH, L_C = 4.5mH*	*179*
Figure 6.7	*DC-Link Voltage with reference*	*180*
Figure 6.8	*Active and Reactive power with reference*	*180*
Figure 6.9	*DC-link voltage with a step of 35V in dc-link voltage reference*	*181*
Figure 6.10	*Active power and reactive power with their respective references with a step of 35V in dc-link voltage reference*	*182*
Figure 6.11	*PCC voltage, supply current and grid voltage estimation for a step of 35V in dc-link voltage reference– phase A*	*183*
Figure 6.12	*Total Inductance estimation with a step in dc-link voltage reference, L_S = 3.0mH, L_C = 4.5mH*	*183*
Figure 6.13	*Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference*	*184*
Figure 6.14	*PCC voltage, supply current and grid voltage estimation – phase A for a step of 500VAR in reactive power reference*	*185*
Figure 6.15	*Total Inductance estimation with a step of 500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH*	*185*
Figure 6.16	*DC-Link voltage with reference for a step of 500VAR in reactive power reference*	*186*

List of Figures

Figure 6.17	*Equivalent representation of a VARIAC* [108]	*187*
Figure 6.18	*Step from ~33V to ~100V PCC voltage, supply current and grid voltage estimation – phase A*	*188*
Figure 6.19	***A*** *- ~33V in VARIAC. PCC voltage, supply current and grid voltage estimation – phase A*	*189*
Figure 6.20	***B*** *- ~100V in VARIAC. PCC voltage, supply current and grid voltage estimation – phase A*	*189*
Figure 6.21	*Step from ~33V to ~100V in VARIAC, Inductance estimation,* $L_{estimation} = L_S + L_{VARIAC}$	*190*
Figure 6.22	*Step from 33V to 100V in VARIAC, DC-Link Voltage*	*191*
Figure 6.23	*Step from ~33V to ~100V in VARIAC, Active and Reactive Power with reference*	*192*
Figure 6.24	*DC-link voltage response to 35V step in DC-link voltage reference – experimental result using a programmable voltage source*	*194*
Figure 6.25	*DC-link voltage response to 35V step in DC-link voltage reference – simulation result*	*195*
Figure 6.26	*Total Inductance estimation with 35V step in dc-link voltage reference – experimental result using a programmable voltage source.* $L_S = 3.0mH$, $L_C = 4.5mH$	*195*
Figure 6.27	*Total Inductance estimation with 35V step in dc-link voltage reference – simulation result.* $L_S = 3.0mH$, $L_C = 4.5mH$	*196*
Figure 6.28	*Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference – experimental result using a programmable voltage source*	*197*
Figure 6.29	*Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference – simulation result*	*197*
Figure 6.30	*Total Inductance estimation with a step of*	*198*

List of Figures

	500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH – experimental result using a programmable voltage source	
Figure 6.31	*Total Inductance estimation with a step of 500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH – simulation result*	*198*
Figure 6.32	*Total Inductance estimation with a 0.5mH step in grid inductance, L_S = 0.5mH, L_C = 4.5mH – experimental result using a programmable voltage source*	*199*
Figure 6.33	*Total Inductance estimation with a 0.5mH step in grid inductance, L_S = 0.5mH, L_C = 4.5mH – simulation result*	*200*
Figure 6.34	*Total Inductance estimation, L_S = 3.0mH, L_C = 4.5mH, experimental result*	*201*
Figure 6.35	*Grid voltage estimation, supply current and PCC voltage, L_S = 3.0mH, L_C = 4.5mH, experimental result*	*201*
Figure A1	*Equivalent circuit diagram of a weak grid*	*225*
Figure C1	*Three phase to α-β voltage transformation*	*232*
Figure D1	*Dead-time generation block in Matlab/Simulink*	*233*
Figure E1	*Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage (blue) using PVS using method 1*	*235*
Figure E2	*Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage with a step (blue) using PVS using method 1*	*235*
Figure E3	*Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage (blue) with a variation in reactive power reference using PVS using method 1*	*236*
Figure E4	*Oscilloscope results for supply voltage (yellow) and supply current (pink) using PVS using method 2*	*236*

List of Figures

Figure E5	*Experimental results for supply voltage, supply current and dc-link voltage using PVS using method 2*	*237*

List of Tables

Table 2.1	*Switching combinations and converter voltage – Two-Level*	*19*
Table 4.1	*Converter Voltage levels*	*85*
Table 4.2	*Relation Between Integer Steps and Required Accuracy Of Grid Inductance Estimation*	*115*
Table 5.1	*Simulation Parameters*	*127*
Table 5.2	*Comparison of THD values for different variations in L_S*	*142*
Table 5.3	*SCR for different values of L_S*	*145*
Table 5.4	*Estimation method 1 - Effect of measurement noise on supply current THD*	*156*
Table 5.5	*Estimation method 2 - Effect of measurement noise on supply current THD*	*168*
Table 6.1	*THD values for 2 VARIAC operating conditions*	*191*
Table 6.2	*Comparison of THD values between simulation results and experimental results using programmable voltage source*	*193*

Nomenclature

$\hat{L}_{EST}$	*Total estimated inductance*
λ_i	*Weighting factor for cost function*
$\hat{\theta}$	*Grid phase angle*
AFE	*Active front end*
BPF	*Band pass filter*
C	*DC-link capacitance*
CCS-MPC	*Continuous control set MPC*
CSC	*Current source converter*
DG	*Distributed Generation*
d-q	*Direct-quadrature*
DSOGI-PLL	*Dual econd order generalized integrator PLL*
DSP	*Digital signal processing*
FACTS	*Flexible AC transmission systems*
FCS-MPC	*Finite control set MPC*
FFT	*Fast Fourier transform*
FLL	*Frequency locked loop*
FPGA	*Field programmable gate array*
g	*Cost function*
GaN	*Gallium Nitride*
GPC	*Generalized MPC*
IGBT	*Integrated bi-polar transistors*
Ki	*Integral gain of PI*
Kp	*Proportional gain of PI*
L_C	*Converter input filter inductance*

Nomenclature

LPF	*Low pass filter*
L_S	*Grid inductance*
MPC	*Model predictive control*
MP-DPC	*Model Predictive Direct Power Control*
N*	*Reference prediction horizon*
PCC	*Point of common coupling*
PI	*Proportional Integral*
PLL	*Phase Locked Loop*
P-PLL	*Instantaneous power PLL*
PR	*Proportional resonant*
PV	*Photo-voltaic*
PWM	*Pulse-width-modulation*
R	*Load resistance*
r_C	*Converter input filter resistance*
RES	*Renewable energy sources*
SCR	*Short circuit ratio*
SiC	*Silicon Carbide*
SOGI-PLL	*Second order generalized integrator PLL*
$S_{optimum}$	*Optimum switching signal obtained from cost function optimization*
SPWM	*Sinusoidal pulse-width modulation*
SRF-PLL	*Synchronous reference frame PLL*
STATCOM	*Static compensators*
SVM	*Space vector modulation*
t_d	*Dead-time of* 2μs

Nomenclature

THD	*Total harmonic distortion*
t_s	*Sample time of 50*μs
UPFC	*Unified power flow conditioner*
UPS	*Uninterrupted power supply*
VCO	*Voltage controlled oscillator*
VOC	*Voltage Oriented Control*
VSC	*Voltage source converter*
α-β	*Alpha-beta*
ω_{ff}	*Feed forward frequency*
ω	*Angular frequency*

Chapter 1: Background and motivation

1.1 Introduction

This chapter starts by giving a brief introduction about the background and motivation of the research work presented in this thesis; highlighting the emergence of distributed generation (DG) and micro-grids systems in the recent past. The chapter also mentions the limitations associated with such systems and objectives of the presented research work. The chapter is concluded by giving an outline of the thesis and a list of publications resulting from this thesis.

1.1.1. Background and motivation

Classical grid structures, similar to the one shown in figure 1.1, have been in use for decades. The electricity in such structures is mostly generated from large and centralized power stations such as thermal, nuclear or hydro power plants. These power sources are usually located far from the consumer side and transport electricity via long transmission cables, high and medium voltage substations [7], [8].

The power transmitted through these cables is monitored at the substations in order to maintain the voltage and frequency levels [7]. Such classical grid structures need a major upgrade as they present drawbacks that include inefficiencies, power losses, old, lengthy and overloaded transmission lines. Furthermore, the classical grid structure need to be modified with a decentralized energy system (distributed generation) that includes small-scale energy sources to meet a rising demand of electricity.

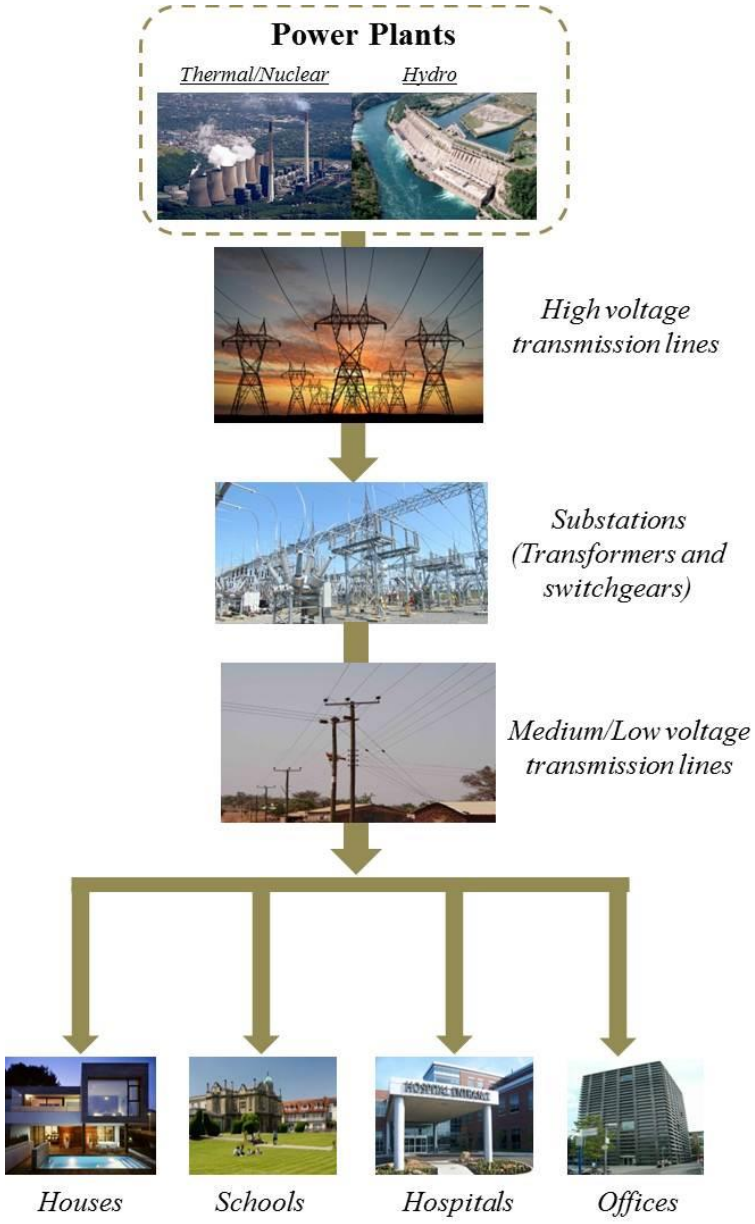


Figure 1.1: Classical electrical grid structure

In the recent past, the fast emergence of DG systems using renewable and traditional energy sources is widely contributing to modify the old concept of electrical distribution network towards an active grid model through the use of power electronic converters [9]. Figure 1.2 shows the contribution of generated renewable energy in Europe according to surveys carried out between 1998 and 2012 [10], [11]. The increasing trend in renewable energy generation has demanded an improvement in power electronics

systems and their control in order to implement systems grid interface, effective and intelligent power flow control and to avoid grid instability [7].

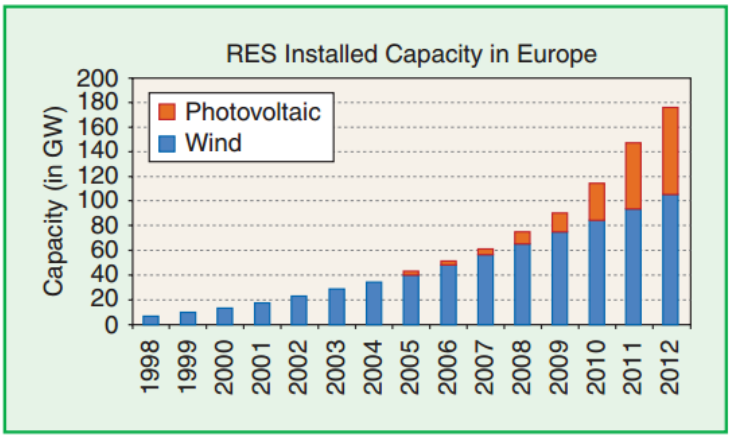


Figure 1.2: Contribution of renewable energy generation in the total electrical energy demand of Europe [10][11]

In order to overcome issues related to the classical grid networks, a more sustainable grid structure is in the making where through DG systems, the renewable energy sources like wind power plants, solar plants or small scale thermal power plants are being situated near the end-users, thus providing more protection, security, less congestion on the transmission line and a smart grid operation [12]–[14]. Moreover, due to location of renewable energy sources near the end-users and also due to a large number of smaller generation sources, it reduces the chances of power failure as compared to cases of large centralized power plants [7], [15], [12], [16]–[19]. An equivalent model of present grid structure with inclusion of distributed generation sources is illustrated in figure 1.3.

Such grid structures can have large scale distribution networks and also small-scale where renewable energy sources can be connected centrally or locally to the electrical grid, respectively. A DG system consists of power transformers, linear loads, non-linear loads and other distributed energy sources [20]–[22] . While distributed generation has

many advantages as mentioned earlier, there are also some drawbacks. These drawbacks that affect the power quality in the distributed generation network and the grid-connected converter control performance include harmonic interaction between a large number of distributed power converters, transient load variations, connection or disconnection of individual energy sources, grid impedance variations, to name a few [7], [20]–[23].

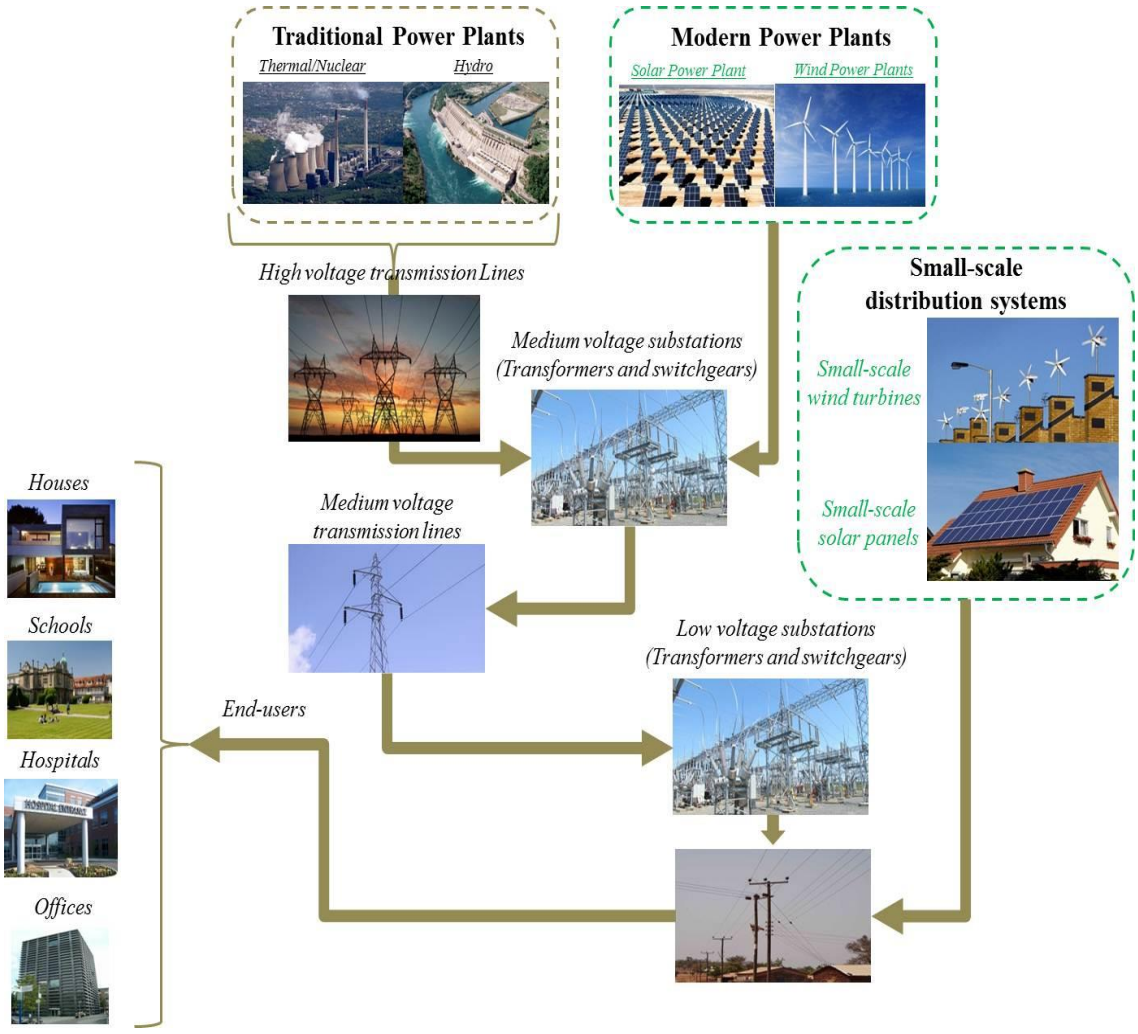


Figure 1.3: Present electrical grid structure with distributed generation systems

Thus, the grid needs to be continuously monitored in order to provide a stable power quality and converter control by considering these variations in grid interconnections

according to the IEEE standards mentioned in [23]–[25]. The next section briefly explains the concept of a weak grid system that is largely dominated by harmonics and grid impedance; affecting the control of power converters.

1.1.2. Weak Grid

A weak grid refers to a grid network that is heavily dominated by distortions present at the PCC. This distortion, usually referred as grid impedance, can be classified as having inductive-resistive characteristics as explained through several measurement studies performed on power distribution networks [21], [26]. With respect to figure 1.4, the grid impedance Z_{grid} can, therefore, be represented as:

$$Z_{grid} = r_S + j\omega L_s \tag{1.1}$$

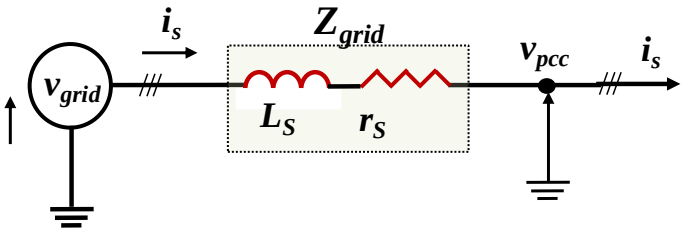


Figure 1.4: Equivalent grid impedance model

Where, r_s, L_s and ω refer to the grid resistance, grid inductance and the grid frequency with a fundamental value of 50 Hz, respectively. The determination of a grid to be weak or strong is based on its Short-Circuit-Ratio (SCR) value calculated using the grid impedance values as explained with the help of examples in Appendix A [27]. The SCR is a unit less quantity and is the ratio between the short circuit power at the PCC in a three phase system and the rated power of the active load connected to the grid [27].

Small values of grid impedance result in a strong (stiff) grid with a high SCR value (greater than 20), whereas, a large value in grid impedance results in a weak grid with a

low SCR value (less than 10) [28]–[30]. While r_s mostly affects the amplitude of the voltage at the PCC, a large variation in L_s not only affects the amplitude of the voltage at PCC, it also introduces a phase shift, hence affecting the phase synchronization between the voltage and the phase current at the PCC. As the grid impedance is an addition in series to the converter input filter impedance, a large value of grid impedance (if not known) can significantly affect the performance of the converter current control which is usually tuned only on the basis of the known converter impedance. To improve the power quality of a grid-connected converter, it can be advantageous to know the correct value of the grid impedance.

The value of grid impedance in grid-connected converter applications is either 'assumed' as a fixed value or mostly estimated using offline/online methods [7]. However, the grid impedance does not remain consistent and can have variations that can affect the converter control performance, especially for SCR values less than or equal to 5. To have an intelligent converter control with a good power quality, a fast and continuous estimation of grid impedance in real-time under SCR values less than 5 can add additional features on operation of grid-connected converters.

1.2. Objectives of the project

This project investigates the potentiality of MPC to realize grid connected power converters capable of grid self-synchronization, eliminating the need of a PLL to measure supply frequency and phase. The method is studied and tested for a conventional three phase two level active front end with dc-link voltage control. Moreover, the control performance is also studied in presence of grid impedance variation in cases of a low SCR grid. Methods to estimate the variation in grid

impedance are proposed in this thesis that update the MPC in real-time thus, giving a reliable control performance and improved power quality. This project includes modeling, simulation and experimental work. The project objectives and solutions are highlighted as:

Use a control technique for grid connected converters that have a single control structure instead of having cascaded control loops as used in Voltage Oriented Control (VOC) techniques, for example, for converter control. Advanced control techniques, like MPC, are fast emerging in the field of power electronics because of its advantages that include multivariable control in a single control structure, model representation of the system, quick response to transient variations, inclusion of nonlinearities and system constraints within the control algorithm, to name a few [31]. Hence, the MPC has been chosen as the control strategy for the work carried out in this thesis.

For low SCR grid connections, the *PLL* tuning can be challenging since the integral gain (*Ki*) and proportional gain (*Kp*) parameters need to be retuned frequently with the latest value of grid parameters [32]. To avoid retuning the *PLL* every time a variation in grid parameters takes place, the task at hand was to find a technique that avoids the use of *PLL* and keeps the grid voltage and current synchronized without the need of retuning frequently. Continuation of this task was to propose and develop methods that estimate the variation in grid impedance in real-time thus updating the predictive controller in real-time as well. To solve these issues, firstly a Direct Power Control incorporated within the MPC has been used [33]–[35]. The active and reactive powers are directly controlled to maintain a close to unity power factor and provide phase synchronization between the grid voltage and current. Thus, by using a Model based

Predictive Direct Power Control (MP-DPC) the need of a *PLL* for phase synchronization is hence avoided. Secondly, two online grid impedance estimation methods have been proposed in this thesis that are integrated within the MP-DPC described as *method 1* and *method 2* in chapter 4. *Method 1* estimates the variation in grid impedance such that a constant grid voltage magnitude at two consecutive sampling instants is assumed. *Method 2* on the other hand estimates the variation in grid impedance based on an estimated grid current and an optimization algorithm that determines the variation in grid impedance by minimizing the error between the estimated and actual line currents at every sampling interval.

The advantage of using these two proposed estimation algorithms lies in the fact that the estimation is carried out in real-time and also the model impedance value in the predictive controller is updated in real-time with the latest value of grid impedance. Simulation and experimental results support the proposed methodologies for low SCR values where the grid condition is weak, thus providing an improved power quality and a robust converter control performance.

1.3. Thesis structure

The thesis is organized as follows:

- Chapter 1 gives background, motivation and objectives of the research project with emphasis on problems associated with the current grid structure. Moreover, the chapter gives a guideline of thesis structure and contribution of the thesis work in form of international publications.
- Chapter 2 gives an overview of the most popular *PLL* techniques used for phase synchronization in grid-connected converters and highlights the basic working

principle of the mentioned *PLL* strategies. Moreover, the chapter describes the popular VOC technique used for control of power converters using modulation strategies. The chapter also discusses the widely applied grid impedance estimation techniques using both online and offline methods and mentions the advantages and drawbacks of each approach.

- In Chapter 3, a literature review of predictive control techniques like dead-beat control and MPC is carried out with regards to their advantages and disadvantages. The working principle of MPC using an MPC-Current Control as an example is explained with emphasis on cost-function optimization and switching signal generation.
- Chapter 4 presents the MP-DPC strategy along with the two proposed grid impedance estimation techniques applied to a three phase two-level AFE. The discrete-time modeling, cost-function optimization, switching state selection, sample-ahead predictions, dead-time compensation method, grid impedance estimation algorithms used in conjunction with the MP-DPC are respectively explained in detail in this chapter.
- Simulation results, using MATLAB/SIMULINK and PLECS environment on three phase two-level AFE, for the methods proposed in Chapter 4 are presented in Chapter 5 to analyze the performance of the predictive control to variations in dc-link voltage reference, active power and reactive power references. As the control performance gets disturbed due to parameter mismatches, simulation results with an unknown variation in grid impedance are presented that validate the importance of knowing the value of grid impedance. Simulation results for the two proposed

estimation algorithms with a frequent variation in grid impedance, a large step in grid impedance, variation in active and reactive powers are shown. The results support the proposed methodologies and provide a robust performance to the predictive controller to variations in grid impedance as the controller is updated in real-time with the latest estimation of grid impedance value. Also, estimation algorithm performance with unbalanced grid voltages is presented and the importance of dead-time compensation is highlighted in this chapter as well.

- Chapter 6 gives a description of the experimental setup that uses a three phase two-level AFE. It also presents MP-DPC experimental results using the methods proposed in Chapter 4 to a presence of unknown grid impedance value and also with variations in active and reactive powers. The experimental tests have been conducted using a three phase programmable voltage source manufactured by CHROMA and also by using an autotransformer referred as VARIAC. The control platform uses a DSKC6713DSK digital signal processing (DSP) board and an Actel ProASIC3 A3P400 field programmable gate array (FPGA).
- Detailed discussion and concluding remarks for the thesis are presented in Chapter 7 with suggestions on areas where improvements can be made. This chapter also presents suggestions for further work on the proposed topic.

1.4. Contribution of thesis

The work presented in this thesis has resulted in three international conference publications and one journal publication for Transactions on Industrial Applications. The work published in these papers is presented in chapters 4, 5 and 6, respectively. The key contributions of this thesis includes development, design, simulation testing and

practical verification of two novel grid impedance estimation algorithms for grid-connected power converters that can be applied to Weak AC systems where the transmission line parameters can have a significant value as compared to the usually known converter input filter impedance value. The published papers are:

Journal publication:

- B. Arif, L. Tarisciotti, P. Zanchetta, J. Clare, M. Degano, *"Grid Parameter Estimation using Model Predictive Direct Power Control"*, **IEEE Transactions on Industrial Applications, July 2015**.

Conference publications:

- B. Arif, L. Tarisciotti, P. Zanchetta, J. Clare, *"Finite Set Model Predictive Control with a Novel online grid inductance estimation technique"*, Power Electronics Machines and Drives (PEMD 2014), 7th IET International Conference, IET CONFERENCE PUBLICATIONS, April 2014
- B. Arif, L. Tarisciotti, P. Zanchetta, J. Clare, M. Degano, *"Integrated grid inductance estimation technique for Finite Control Set Model Predictive Control in grid connected converters"*, Energy Conversion Congress and Exposition (ECCE 2014) IEEE, IEEE CONFERENCE PUBLICATION, September 2014.
- B. Arif, L. Tarisciotti, P. Zanchetta, P. Wheeler, *"Online predictive model fitting algorithm for supply inductance estimation"*, Energy Conversion Congress and Exposition (ECCE 2015) IEEE, IEEE CONFERENCE PUBLICATION, September 2015.

1.5. Conclusion

This chapter gave an introduction about the project motivation and objectives by highlighting the advancement of DG systems and the challenges associated with them. The chapter presented the structure of the thesis and also contribution of the work carried out in this project that resulted in international publications.

The next chapter presents the literature review on grid-connected converters with emphasis on their control techniques and the most popular grid impedance estimation methods.

Chapter 2: Introduction to converters, control techniques, modulation techniques and grid impedance estimation techniques

2.1. Introduction

Over the last two decades, there has been a sharp growth in the usage of power electronic systems, where through highly-networked collaborations several companies and businesses are working together to develop world-leading solutions in this field [36]. According to a report from the UK based Department for Business Innovation and Skills, power electronics is believed to be contributing towards almost all sectors of industry that include aerospace, automotive, renewable energy generation, energy networks and industrial processes [36]. Furthermore, one of the main objectives of the use of power electronics based equipment is also the reduction of CO_2 emissions by means of, for example, the capability of building more efficient system or to interface renewable energy system [36]. By 2016, IHS in [37] estimates that the global market in the field of power electronic devices would be around $18 billion, increasing at a growth rate of 10% per annum [36]. Power electronics also has a pivotal role in the Renewable Energy Sources (RES) sector and plays an important role in the development, improvement, reliability and stability of the future electrical grid through its contribution as grid connected converters [38].

This chapter gives a literature review and a state of the art of grid connected converters and their topologies. Also the chapter highlights the classical control strategies for grid connected converters in addition to grid impedance estimation techniques.

2.2. Grid Connected Converters

Due to advancements in power semiconductor devices and in DSP and microcontroller computational power in recent years, application of power electronic systems has gained more attention in many different fields, and in particular in power systems. Power

electronic converters are thus increasingly being employed in power conditioning, compensation, grid connections and active filtering applications [8]. Power converters can be categorized as Voltage Source Converters (VSCs) [39] and Current Source Converters (CSCs) [40]. However, VSCs are more widely applied compared to CSCs above all when used as active front ends (AFE) for high-performance drives, rectifiers, for integration of renewable energy sources like wind energy, PV and other energy storage systems [41]–[43]. The term active front end refers to a controllable rectifier that provides bi-directional power flow between the AC side and the DC side of the rectifier. Grid-connected converters are used in flexible AC transmission systems (FACTS) devices such as static compensators (STATCOMs), active power filters to eliminate harmonics produced due to non-linear loads, unified power flow controller (UPFC) and unified power quality conditioner [44]–[47].

Figure 2.1 shows an equivalent representation of a general three phase grid connected converter with an input inductive filter and a resistive load at the output. The AC voltage generation point is referred to as v_{grid} and the AC current that flows in the transmission line are referred to as i_s.

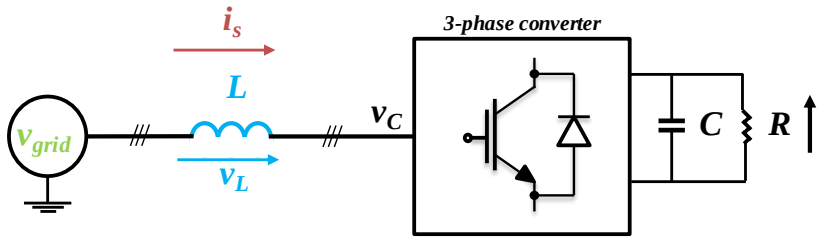


Figure 2.1: Equivalent representation of a grid connected converter

The different operating points of the grid connected converter in figure 2.1 are shown in figure 2.2 with respect to their vectorial representation. Each of the cases, *1-6,* mentioned in figure 2.2 are explained as:

1) For a case when the transmission line has inductive characteristics, the grid voltage has a leading phase shift as compared to the line current, therefore the reactive power is positive.

2) On the contrary to case 1, a transmission line having capacitive characteristics results in the supply current leading the grid voltage. The case presented shows a negative reactive power thus a lagging power factor.

3) This is a purely inductive case. Though not actively applied in grid connected converters, this case is applied for a purely positive reactive power control such that the reactive power is absorbed. The grid voltage leads the supply current by an angle of 90°.

4) In case of a negative reactive power control where purely capacitive characteristics are reflected, the supply current leads the grid voltage by an angle of 90°.

5) Case 5 depicts the case where a unity power factor regeneration mode is required; the grid voltage and supply current have 180° phase shift between them.

6) In case of a unity power factor rectification mode, where the reactive power is zero or negligible, the grid voltage and the line current are maintained to be in phase with each other, thus achieving phase synchronization.

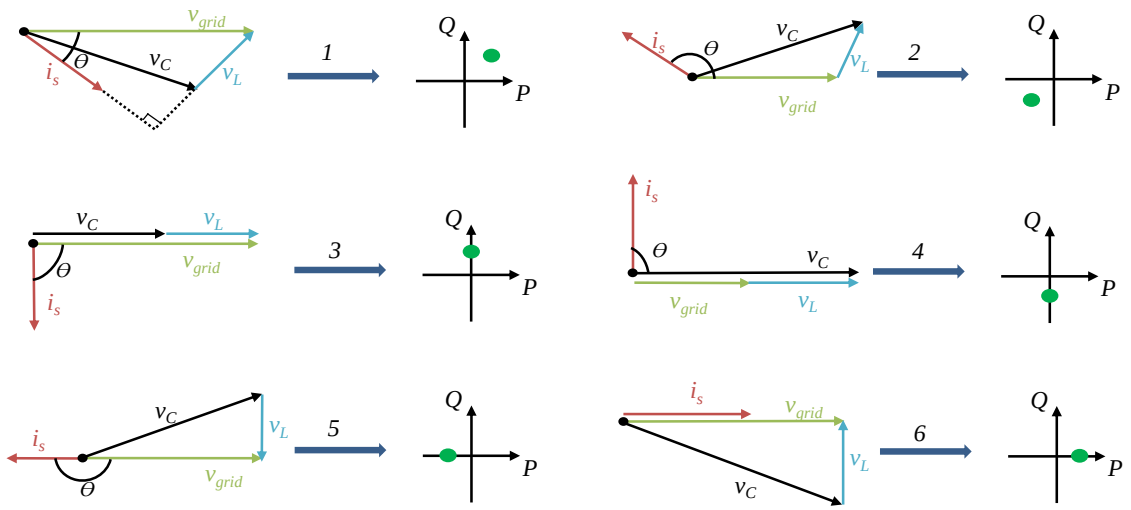


Figure 2.2: Operation points of grid-connected converters in their P and Q representation

2.2.1. Two-level Converter

Figure 2.3 shows the representation of a three phase grid connected two-level converter that consists of 2 IGBTs per leg, 6 IGBTs in total which will be used in this work to validate the proposed impedance estimation algorithms and control. In figure 2.3, v_{ca}, v_{cb} and v_{cc} are the voltages with respect to the ground of the dc-link. Using leg *A* of the converter, table 2.1 shows the switching combinations to achieve the desired voltage levels.

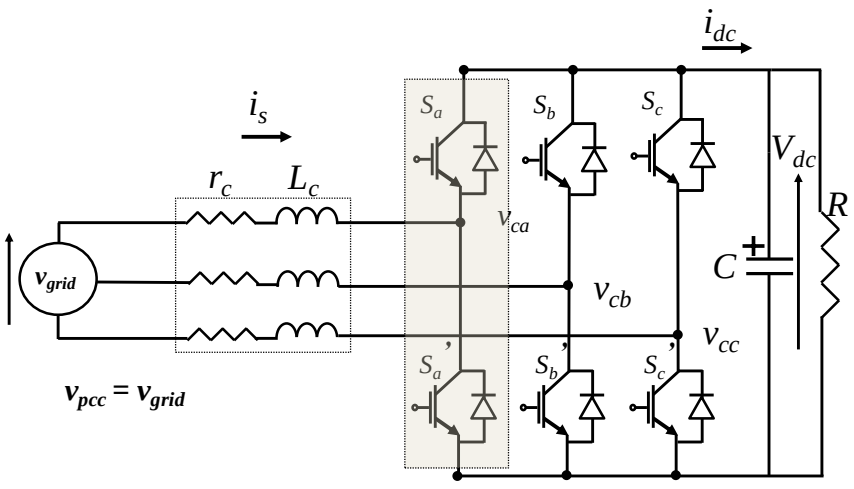


Figure 2.3: Three phase two-level converter

Table 2.1: Switching combinations and converter voltage – Two-Level

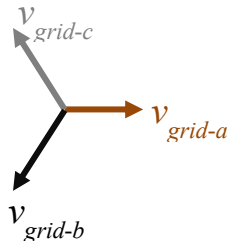
S_a	S_a'	v_{ca}
1	*0*	V_{dc}
0	*1*	*0*

Therefore, with respect to the ground of the dc-link only two levels can be obtained for each leg, V_{dc}, *0*. In order to avoid short-circuit in the leg a dead-time is introduced while turning ON the switches in each leg. The dead-time works in such way that at the instant switch S_a is turned OFF, S_a' takes some defined time to turn ON. The drawback associated with dead-time is the voltage loss, [48], that needs to be compensated. Several methods for dead-time compensation have been proposed in the literature that calculate the voltage drop due to dead-time [49]–[51]. These methods are based on the direction of current in each leg every time dead-time occurs, using average sampling methods to sample the current in the middle of the switching interval or by calculating the difference between the reference converter voltage and the actual converter voltage that has effect of dead-time. Modeling of the three phase two-level converter and an online implementation of dead-time compensation method that takes into account the voltage loss during the turning ON of the switches in each leg and modifies the control algorithm with an average value of the converter voltage during this time is explained in Chapter 4 of this thesis.

Using this basic converter structure, it is possible to implement the following controlled power conversion types.

2.2.1.1. AC-DC

The controlled AC-DC converters are called *Active Rectifier* or *Active Front End (AFE)*. Normally, the operating AC voltage for the rectifiers is 240V, 50Hz in the UK and 120V, 60Hz in the United States. Using PWM control techniques as explained in section 2.3, the AC input voltages are converted into a unidirectional DC voltage that is used to supply power to a DC load. The three phase input AC voltages are determined as:



$$v_{grid-a} = \hat{V}\sin(\theta)$$
$$v_{grid-b} = \hat{V}\sin(\theta - 120°) \quad (2.1)$$
$$v_{grid-c} = \hat{V}\sin(\theta + 120°)$$

Where, $\hat{V}$ is the peak of the input voltage and the grid phase angle θ is calculated using PLL techniques as explained in section 2.3A.

Referring to figure 2.1, in grid-connected applications the AC voltage is obtained from low voltage distribution systems that may include renewable energy sources like photo-voltaic, wind turbines or non-renewable energy generation systems. The rectifier is widely used for power factor correction to achieve a unity power factor condition. Moreover, the DC voltage produced at the output is mostly used for batteries, DC-motor operation, as a supply voltage for DC-AC converters or other DC power sources. For the work carried out in this project, a three phase two-level rectifier has been used as a

front-end where the converter is connected to an AC grid, provides unity power factor and supplies active power to a dc-load [52].

2.2.1.2. DC-AC

The DC-AC converters are called *Inverters* that take as input a DC signal and convert it to an AC signal to be utilized as an input signal for AC motors and drives or for AC grid connections. The inverter source voltage includes batteries, solar panels, fuel cells or DC voltage generated from a rectifier [53]. Moreover, DC-AC inverters are also used as STATCOMs where they support the electricity networks by improving the power factor and provide voltage stability [54].

2.2.1.3. AC-AC

These types of converters consist of an AC-DC and a DC-AC converter connected together through a common DC bus with a dc-link capacitor and are controlled using pulse-width-modulation schemes. Applications of these converters include light dimmers, variable speed drives, AC grid interconnections, electric power generation, to name a few [54].

2.3. Control of 3-phase 2-level grid-connected converter

This section gives an insight into the control strategies adapted for grid-connected converters with emphasis on α-β control, dq-control and PLL techniques used for gird phase angle synchronization. Figure 2.4 shows a block diagram of voltage oriented control of a two-level converter.

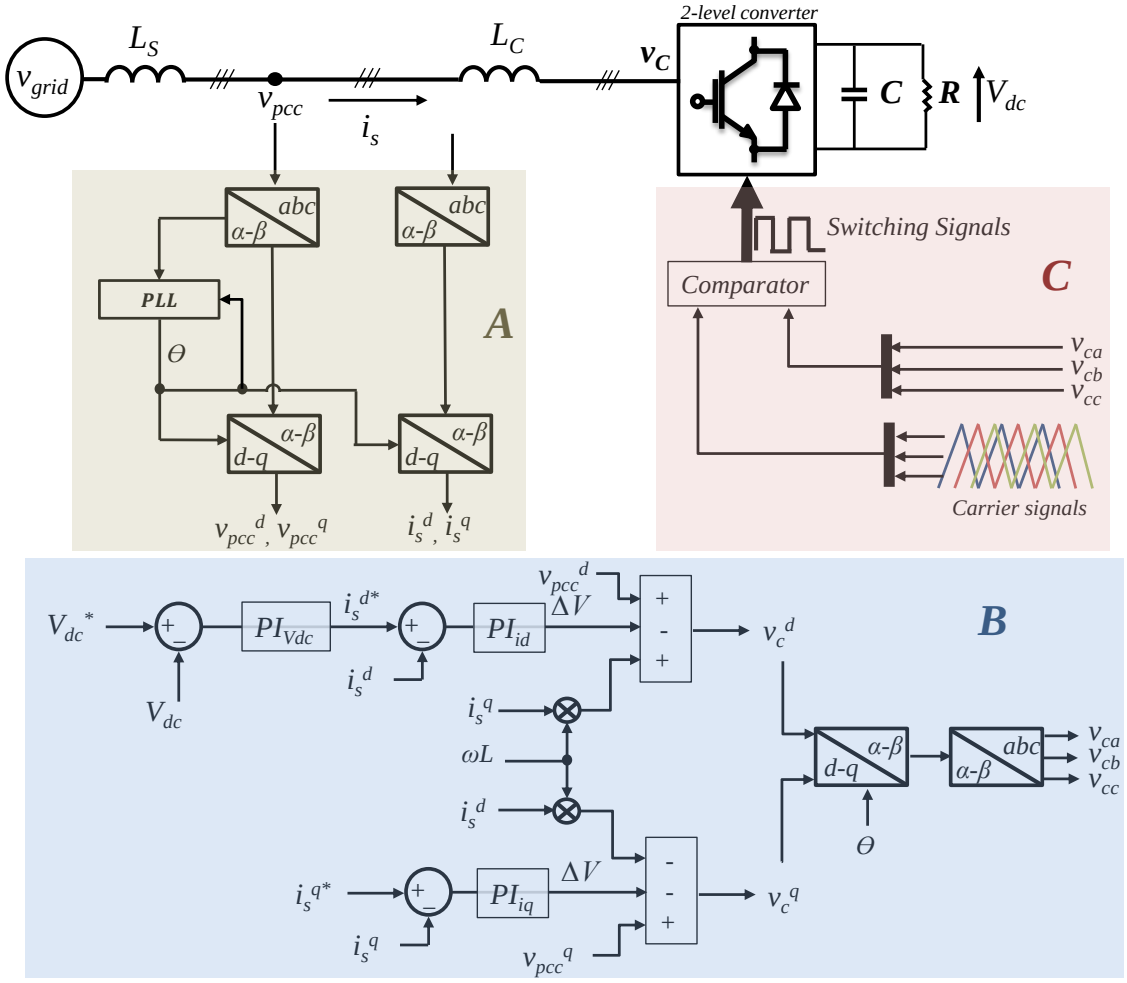


Figure 2.4: Block diagram for Voltage Oriented Control of a two-level converter

The explanation of blocks *A*, *B* and *C* in figure 2.4 are reported in sections 2.3.1, 2.3.2 and 2.3.3 where they are referred as the *Transformation and Angle Calculation* block, *Control Techniques* block and *Modulation Strategies* block.

2.3.1. Transformation and Angle Calculation - A

The three phase voltages and supply currents at the point of common coupling (PCC) are transformed into their respective α and β components using Clarke's transformation [55]. The stationary α-β components are later changed into their respective rotating d and q components, synchronous to the supply voltage, using the Park's transformation[55]. Therefore, for a proper operation of grid-connected converters, knowledge of the utility voltage, phase and frequency become vital [56]. PLLs are used to provide this information. The main objective of a PLL, that operates in a feedback loop, is to provide the phase angle that can be used to synchronize the supply current with the voltage at the PCC [7]. The basic topology of a PLL is shown in figure 2.5 with three building blocks that comprise a phase detector for the d-q components calculations of the input signal, a PI controller to minimize the phase error and to provide a driving signal for the voltage controlled oscillator (VCO) [57] and the VCO that, with an initial value of the fundamental frequency, generates a phase angle Θ to control the angular position of the d-q rotating reference frame in the phase detector block and also for control variable reference calculations.

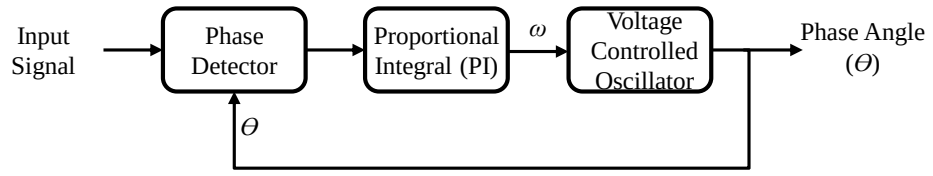


Figure 2.5: Basic scheme of a PLL

A few PLL techniques are explained in the following sections with respect to their response to different values of SCR:

2.3.1.1. SRF-PLL

Figure 2.6 shows a Synchronous Reference Frame PLL (SRF-PLL) that consists of a Clarke-Park transformation to achieve the d-q components of the input voltage signal.

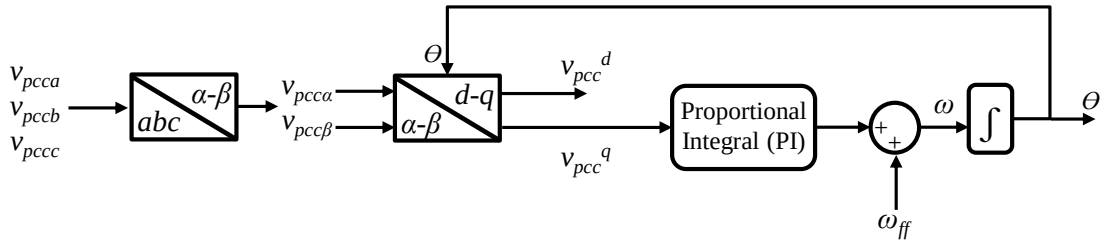


Figure 2.6: Three phase SRF-PLL structure

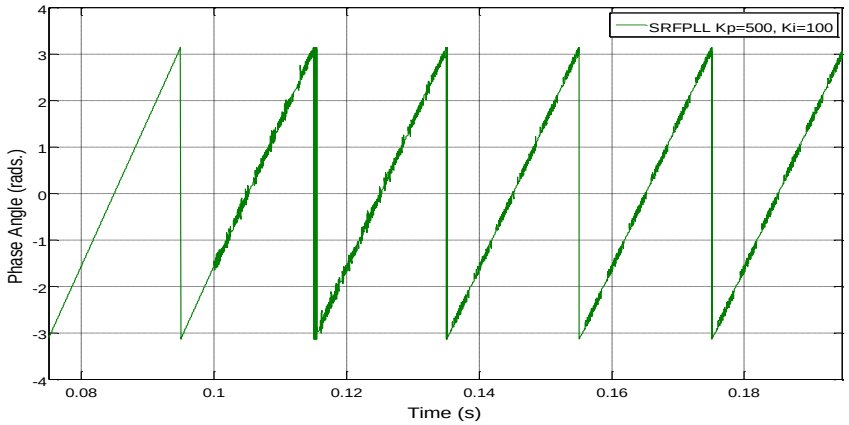
SRF-PLL is perhaps the most widely applied PLL technique for the phase angle generation in a three phase grid connected converter. An initial frequency, ω_{ff}, also referred as a feed-forward frequency is used to provide a better dynamic response of the PLL every time it resets [7]. For a system fundamental frequency of 50 Hz the ω_{ff} is equal to $2\pi 50 = 100\pi$ rads^{-1}. As mentioned in [56], the two most important characteristics while designing a PLL are the tracking precision and the dynamic response to transient variations. The PI controller, also referred as a filter, determines the dynamics of the PLL by careful tuning of its gains as represented in (2.2):

$$PI = K_p + K_i \cdot \frac{1}{s} \tag{2.2}$$

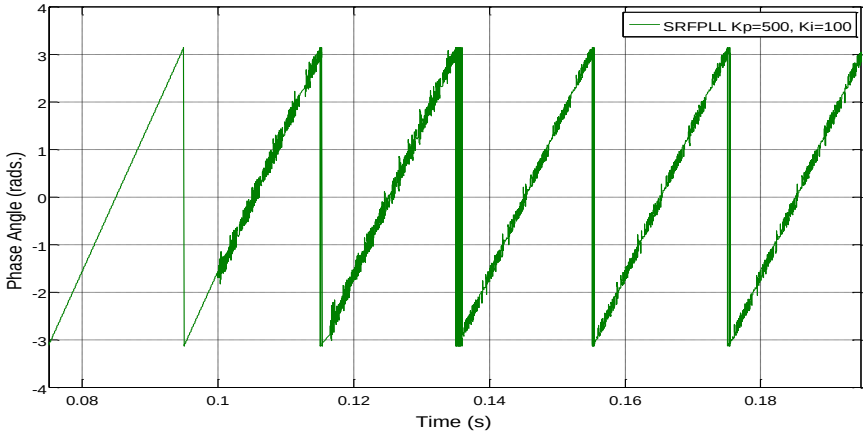
Where, K_p, K_i and $\frac{1}{s}$ are the proportional gain, integral gain and the integrator respectively.

While the SRF-PLL gives fast and precise voltage amplitude and phase angle in an undistorted transmission line, in case the transmission line has a significant distortion on it the generated phase angle shows superimposed ripple. Figure 2.7-2.9 shows the response of the SRF-PLL under three SCR scenarios using three different set of

parameters for the SRF-PLL. In figure 2.7, the proportional and integral gains have been tuned to 100 and 500 respectively while in figure 2.8 the tuning parameters have been reduced by a factor of 10 to observe the PLL performance when its gains are reduced. The values of K_p and K_i in the results presented are empirically designed to show their effect on the generated phase angle when their values are large or small for different values of SCR.



(a)



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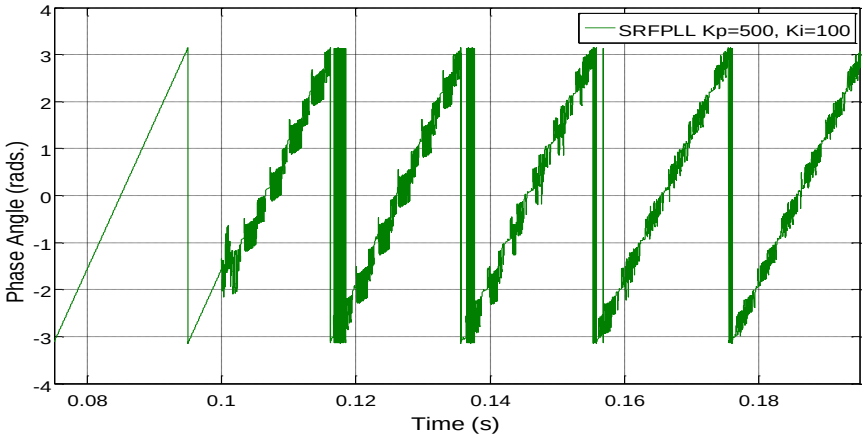
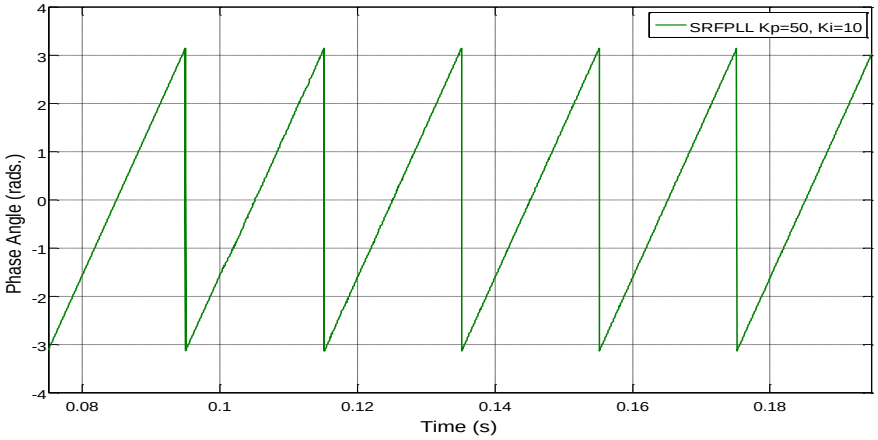


(c)

Figure 2.7: SRF-PLL, K_p = 100, K_i = 500, (a) SCR = 20, (b) SCR = 10, (c) SCR = 3.5

As can be observed, as the SCR reduces the presence of angle distortion gets more dominant; the reason being a highly distorted PCC voltage.



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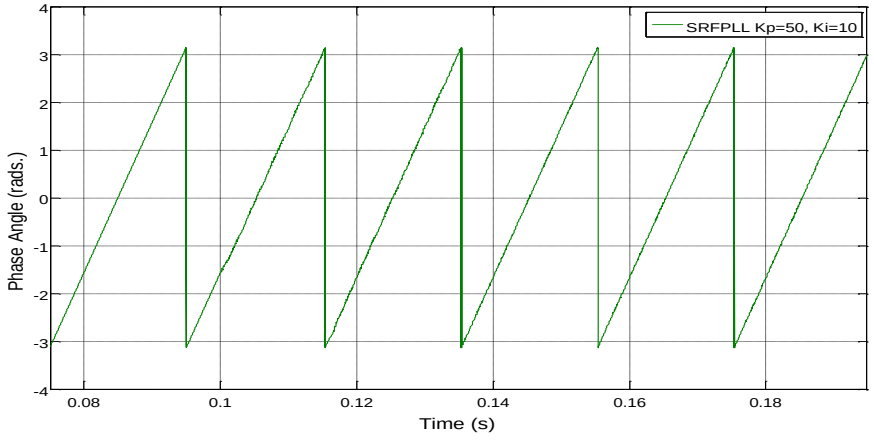

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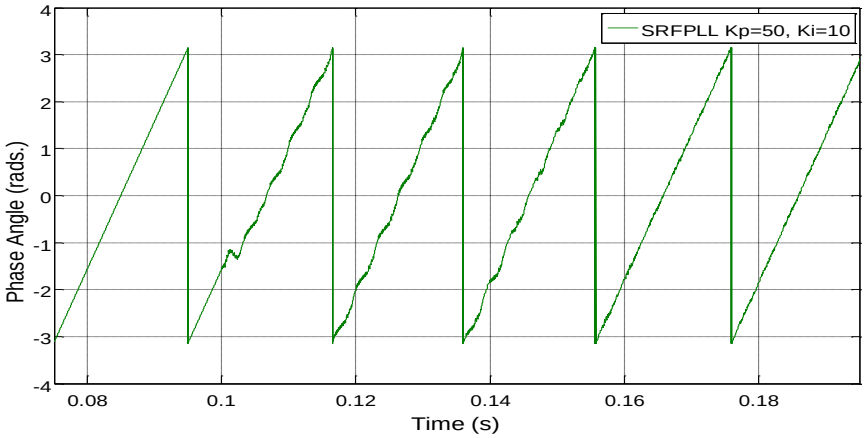

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Figure 2.8: SRF-PLL, K_p = 10, K_i = 50, (a) SCR = 20, (b) SCR = 10, (c) SCR = 3.5

The phase angle is estimated correctly for SCR value till 10. However, for lower values the estimated phase angle becomes distorted. To improve its performance, the PLL gains would need to be reduced furthermore.

Therefore, to conclude, the SRF-PLL works very well under ideal grid conditions. However, in low SCR values where the grid is no longer stiff the performance of the PLL gets significantly affected. The tuning of the PLL gains can be re-adjusted to estimate the phase angle correctly, though that may not be a suitable option under low SCR conditions as the grid impedance may not remain consistent, thus giving variable SCR values.

2.3.1.2. P-PLL

This section presents an instantaneous Power-PLL used for phase synchronization referred as *P-PLL*. The working principle of a P-PLL is based on regulation of the three phase instantaneous power that is calculated using the voltages at the PCC and the phase currents estimated using the estimated phase angle value, $\hat{\theta}$, as shown in the block diagram of figure 2.9 [32], [58]. Figure 2.10 shows the performance of a P-PLL to SCR

values of 20, 10 and 3.5 using proportional and integral gains of 100 and 500 respectively. Figure 2.11 shows P-PLL performance with lower Kp and Ki gains of 10 and 50, respectively. The active power *P* is calculated as shown in (2.3):

$$P = (v_{pcca} - v_{pccb})i_a + (v_{pccc} - v_{pccb})i_c \tag{2.3}$$

Where, i_a and i_c are the supply currents calculated using the estimated phase angle $\hat{\theta}$ with a peak current value of *I*:

$$i_a = I\cos(\hat{\theta}), \qquad i_c = I\cos\left(\hat{\theta} + \frac{2\pi}{3}\right) \tag{2.4}$$

The error between *P** and *P* is taken as input for the *PI* controller to generate the angular frequency, ω. A feed forward frequency, ω_{ff}, is used to improve the initial dynamics of the P-PLL. The integrator, as shown in figure 2.9, is used to calculate the phase angle $\hat{\theta}$.

As can be observed from the results in figures 2.10 and 2.11, the performances of the SRF-PLL and the P-PLL are not significantly different from each other for the same gain values. For both the cases, the performance of the PLL highly depends on retuning of its gains for lower SCR values in order to have a correct estimation of the grid phase angle. Thus, P-PLL may also not be a suitable option under low SCR conditions.

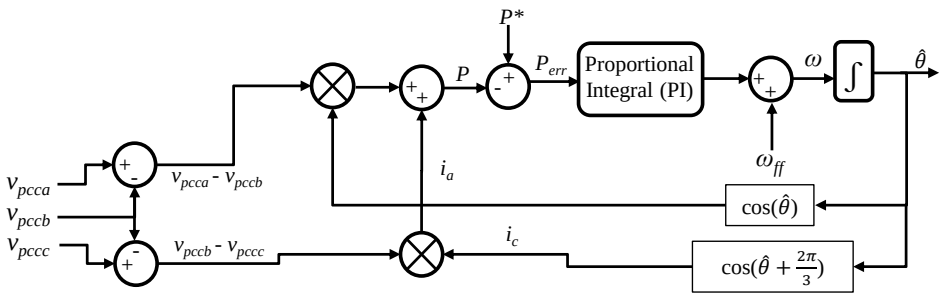
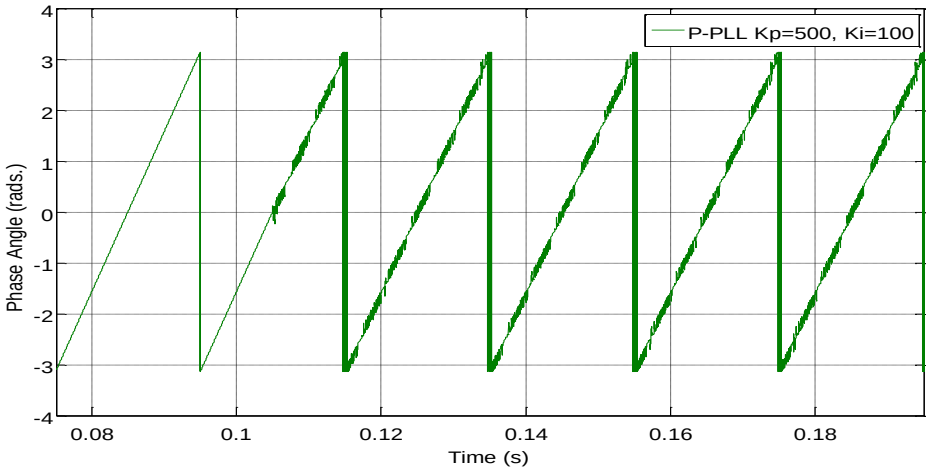


Figure 2.9: P-PLL block diagram



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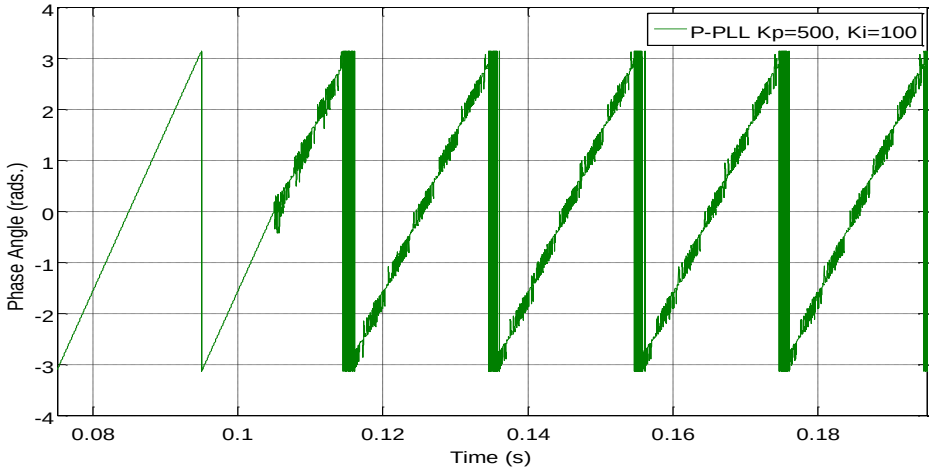

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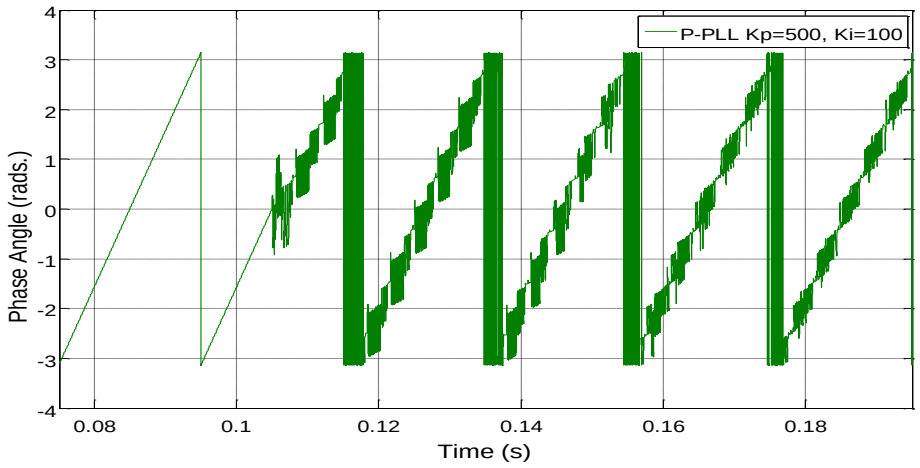

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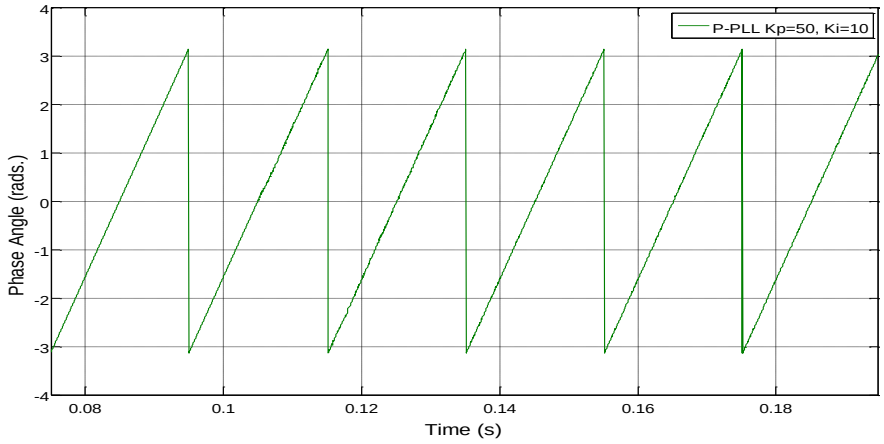
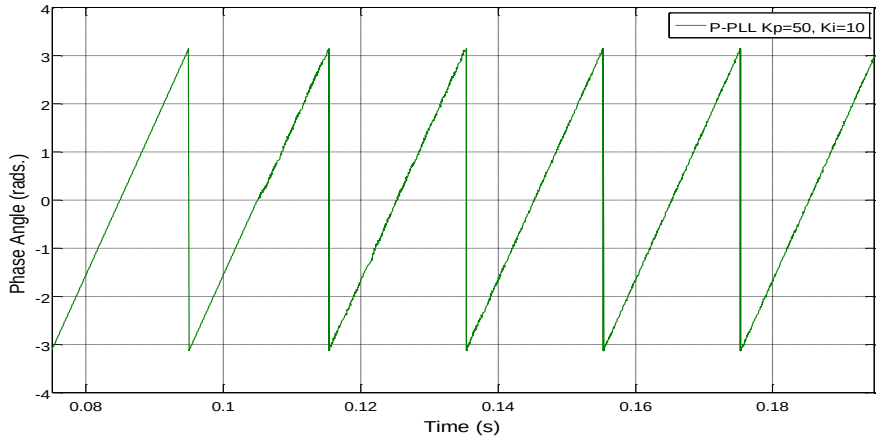
Figure 2.10: P-PLL, K_p=100, K_i = 500, (a) SCR = 20, (b) SCR = 10, (c) SCR = 3.5



(a)



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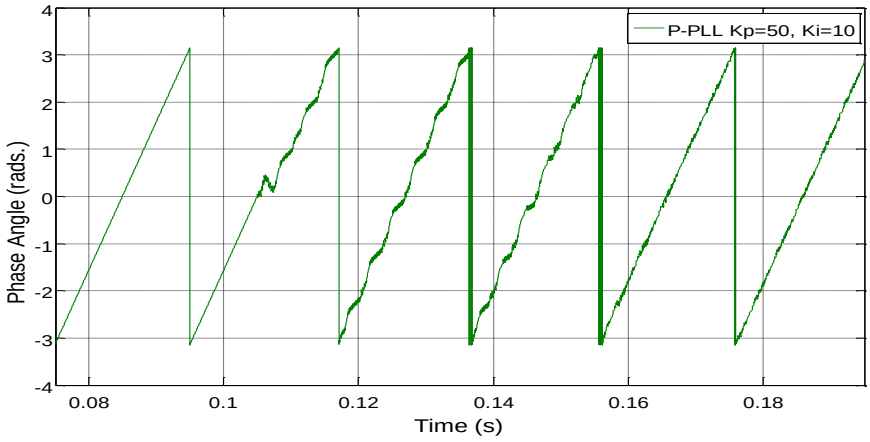


(c)

Figure 2.11:P-PLL, K_p=10, K_i = 50, (a) SCR = 20, (b) SCR = 10, (c) SCR = 3.5

2.3.1.3. DSOGI-PLL

To improve the performance of the SRF-PLL and P-PLL a Second Order Generalized Integrator (SOGI) is applied on the *α-β* input voltage signals to obtain clean signals, hence modifying the classical SRF-PLL to a dual SOGI-PLL (DSOGI-PLL) as shown in figure 2.13, where the term dual stands for two SOGI filters for the respective stationary *α-β* voltage reference frames.

Figure 2.12 shows the structure of the SOGI filter and figure 2.13 shows a block diagram of a three phase DSOGI-PLL. The SOGI consists of a combination of a band-pass filter (BPF) and a second-order low pass filter (LPF), as shown in (2.5) and (2.6) respectively, that provides harmonic filtering capabilities and 90° phase shift to the *α-β* signals for generation of their quadrature signals [59]:

$$BPF(s) = \frac{v_{pcc}{}'}{v_{pcc}} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{2.5}$$

$$LPF(s) = \frac{qv_{pcc}{}'}{v_{pcc}} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{2.6}$$

Where, *k* is the gain of the filter and *ω* is the angular frequency calculated from the PLL. The rest of the structure of a DSOGI-PLL is similar to the SRF-PLL and P-PLL and consists of a Park Transformation and a PI controller similar to (2.2). Figure 2.14 shows the response of the DSOGI-PLL for SCR values of 20, 10 and 5 for K_p and K_i gains of 500 and 100, respectively.

The SOGI filter relies on information of the angular frequency, *ω*, generated from the output of the PI controller as shown in figure 2.13. In case of an error in calculation of *ω* the performance of the SOGI filter may get disturbed. Therefore, a Frequency Locked

Loop (FLL) is integrated with a SOGI filter that monitors the error between the angular frequency ω instead of the phase angle Θ [60].

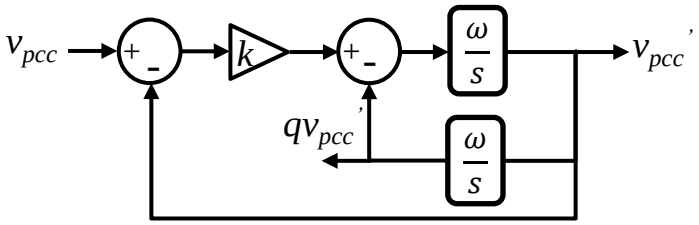


Figure 2.12: SOGI filter

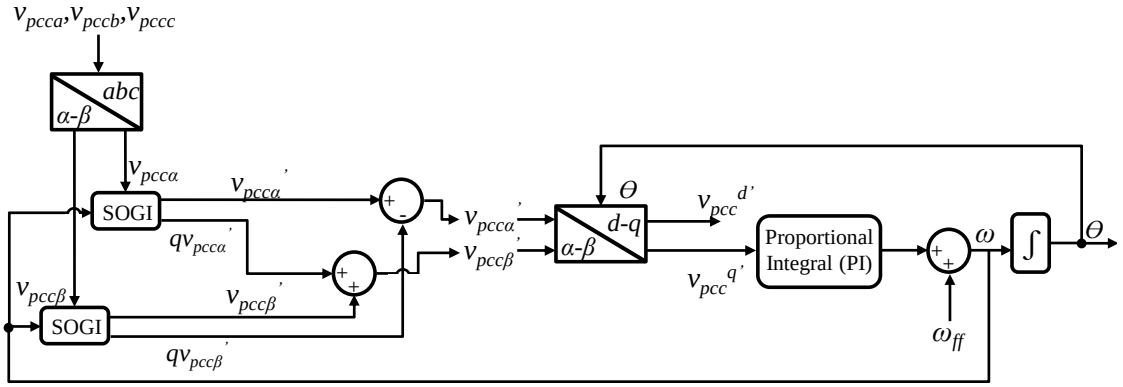
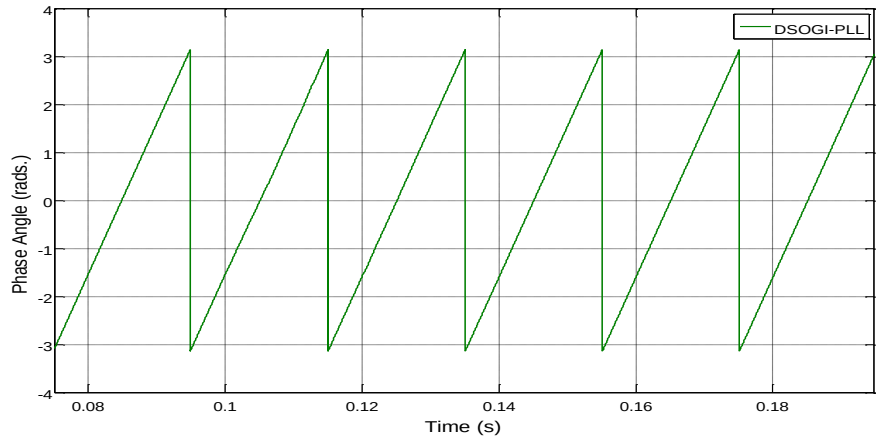


Figure 2.13: Three phase dual SOGI-PLL structure



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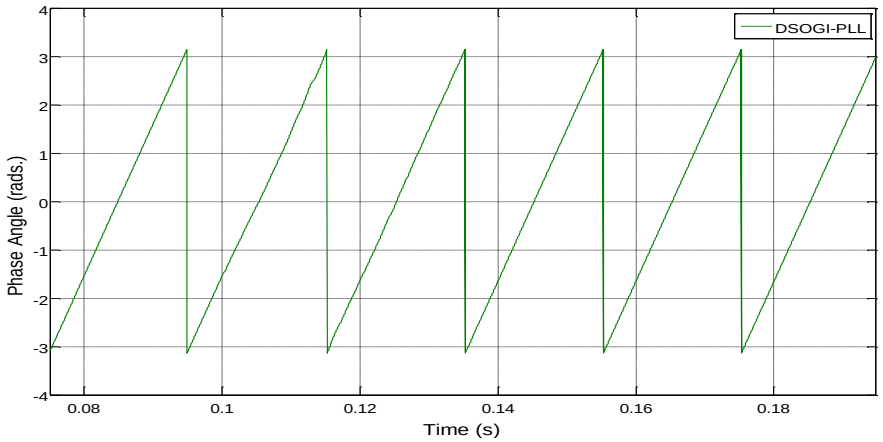

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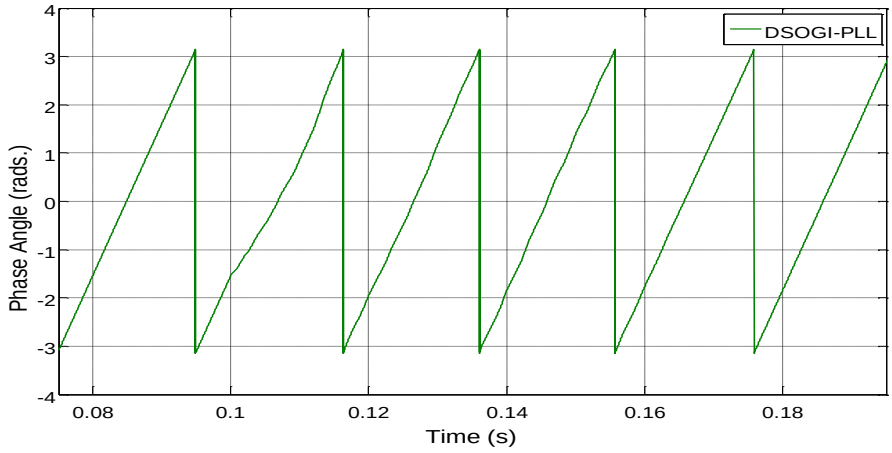


(c)

Figure 2.14: DSOGI-PLL, K_p=100, K_i=500, (a) SCR = 20, (b) = 10, (c) = 3.5

The results show that as compared to SRF-PLL and P-PLL, DSOGI-PLL provides a faster and more precise response to different values of SCR.

2.3.2. Control Techniques - B

The three most common classical control strategies applied for AC current and DC voltage control of grid-connected power converters are d-q Proportional Integral (PI) based control, Proportional Resonant (PR) controller and hysteresis controller applied in a per-phase configuration (or α-β).

2.3.2.1. DQ control

With respect to figure 2.4, the d-q control technique, also commonly known as a Voltage Oriented control (VOC), controls the dc-link voltage and the supply currents by transforming the input AC signals into their respective d-q rotating components with respect to the angular rotation of the grid voltage. Using 2 PI controllers as shown in figure 2.4, 1 for the d-axis and 1 for the q-axis, the current references and the actual current in the d-q rotating reference frames, the converter modulation signals are generated. These represent the modulating signal for the chosen modulation strategy, like Sinusoidal Pulse-Width-Modulation and Space Vector Modulation, to generate the PWM signals for the converter switches.

Another external PI controller is designed for the dc-link voltage that generates an active current reference. The 2 inner PI controllers are designed to regulate the active and reactive currents that are used for generation of converter voltages in their respective *d-q* components. The calculation of *d-q* converter voltage components, v_c^d and v_c^q, can be explained from its equivalent representation of the supply side of the rectifier in *d-q* reference frame as shown in figure 2.15.

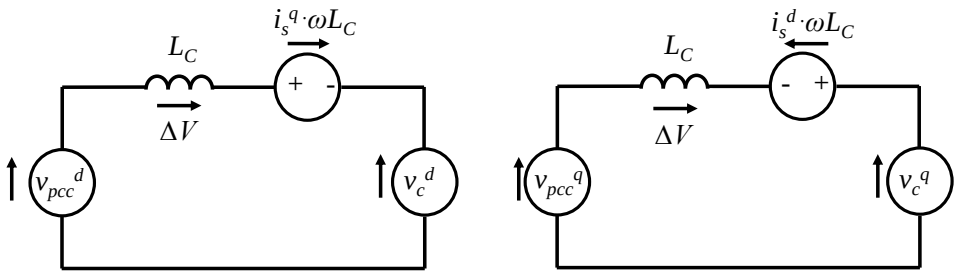


Figure 2.15: d-q representation of supply side of the rectifier

ΔV represents the voltage drop across the converter input filter. The converter voltages are thus equated as:

$$v_C{}^d = v_{pcc}{}^d - \Delta V + i_S{}^q \cdot \omega L \tag{2.7}$$

$$v_C{}^q = v_{pcc}{}^q - \Delta V - i_S{}^d \cdot \omega L \tag{2.8}$$

Using the phase angle Θ obtained from the PLL mentioned in section 2.3.2, the d-q converter voltages are transformed into their respective three phase components $v_{ca,}$ v_{cb} and v_{cc} using inverse Clarke and Park transformation to be used as modulation signals for PWM switching signals generation [55]. As shown through results in section 2.3.1 for different PLL performances under low SCR values, if the calculated phase angle shows oscillation or an incorrect estimated angle value, the PI d-q control performance in turn gets affected since the same calculated angle is used for converter modulation signals generation. Moreover, in case of phase jump, frequency unbalance and unbalanced supply voltage the performance of PLL gets affected and results in phase angle error in addition to harmonics that are represented as additional oscillations in the d-component [55], [58], [59].

2.3.2.2. PR Control

The working principle of a Proportional-Resonant (PR) control is similar to that of the d-q based PI controller with the exception that the control operates in stationary α-β or natural reference frames instead of rotating d-q reference frames. This will allow to use

the converter also in the presence of grid unbalance (in case of natural reference frame) [61]. As opposed to the PI d-q current control of figure 2.4, figure 2.16 shows a block diagram of a PR current controller that takes as input the α-β currents and the current references generated using the phase angle obtained from PLL and outputs the converter modulation signals.

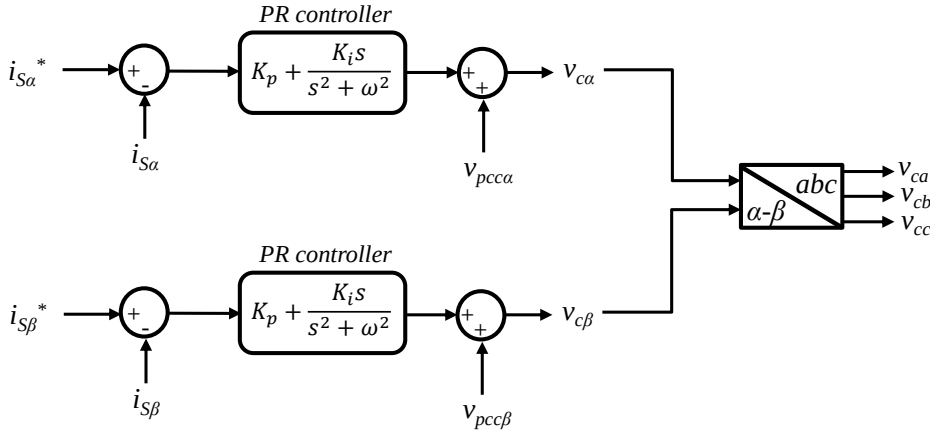


Figure 2.16: Proportional Resonant Controller

The PR controller is represented as the sum of a proportional gain, K_p and a resonant controller gain, K_i, combined with a resonant function as:

$$PR = K_p + \frac{K_i s}{s^2 + \omega^2} \qquad (2.9a)$$

The operating frequency of the PR controller is tuned on the system natural frequency, i.e. 50 Hz in this project for example. If the resonant frequency matches the operating grid fundamental frequency (50Hz), the PR controller gives a high gain and a narrow frequency band that is centered on the resonant frequency of 50Hz, thus giving a good control performance just for that frequency. On the other hand, if the grid frequency shows a variation as compared to fundamental 50Hz frequency, the control performance becomes low and the resonant frequency band becomes wide [62]. In order to improve the control performance, the proportional and integral gains can be re-tuned such that a

low integral gain leads to a narrow frequency band while a high integral gain results in a wider frequency band. The PR control as shown in (2.9a) is ideal and has an infinite gain at the frequency of ω. In order to avoid stability problems due to infinite gain, the ideal PR control in (2.9a) is modified to a non-ideal PR control as shown in (2.9b):

$$PR = K_p + \frac{K_i \omega_c s}{s^2 + 2\omega_c s + \omega^2} \qquad (2.9b)$$

2.3.2.3. Hysteresis Control

The hysteresis control strategy generates the switching signals based on upper and lower boundary limits set on the system control variables. For example, the generated converter switch signal is ON when the control variable reaches the upper boundary limit and is OFF when it reaches the lower limit, thus, restricting the amplitude of the control variable between these two limits, referred as the hysteresis area [63], [64].

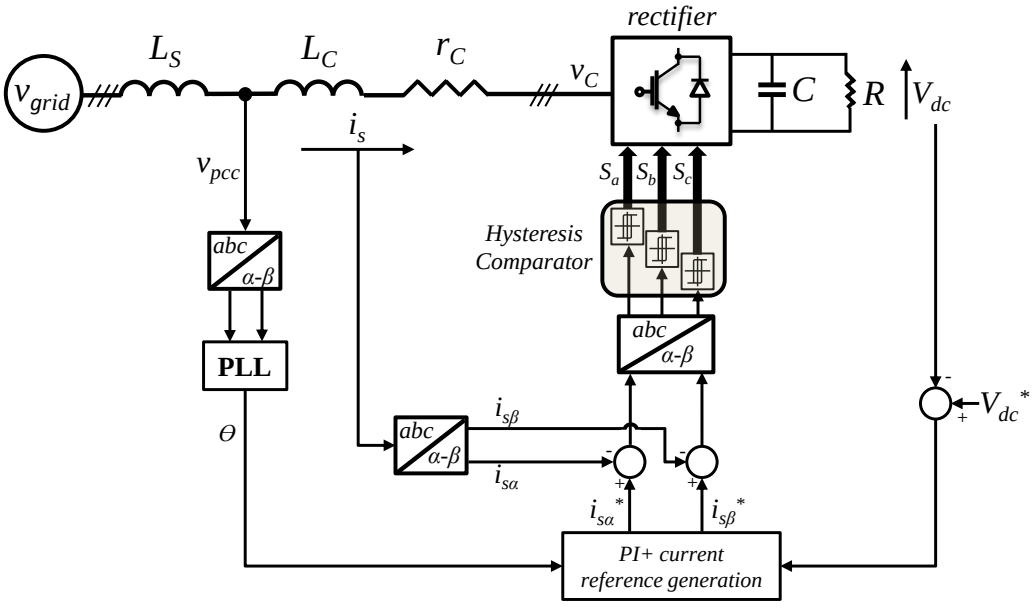


Figure 2.17: Basic scheme of hysteresis current control

The basic block diagram of a hysteresis current controller for a grid-connected converter is presented in figure 2.17. The three phase converter input currents are compared with their respective references in the hysteresis comparator to generate the switching signals for the converter switches such that the converter currents do not exceed the upper and lower boundary limits set in the hysteresis area. The PI controller for the voltage loop is designed in the same way as mentioned in (2.2). Since a modulation strategy is not used and the ripple on the current varies according to the load conditions, the resultant converter switching frequency is variable as the upper and lower boundary limits in the hysteresis area remain unchanged. Figure 2.18 shows the generation of switching signals.

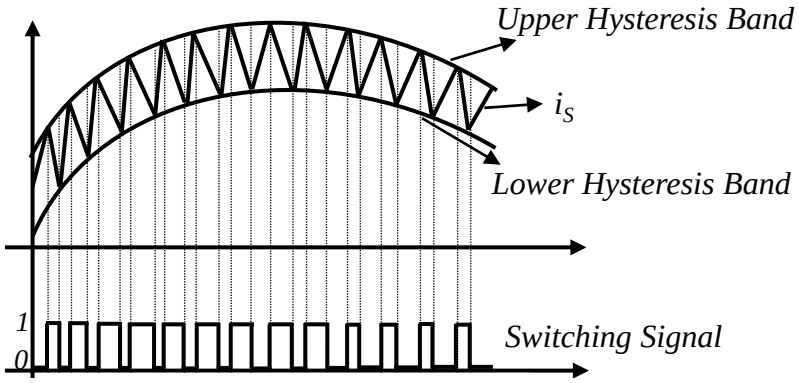


Figure 2.18: Switching signal generation in Hysteresis Control

It is important to mention here that the switching frequency for a hysteresis control also depends on the width of the hysteresis band. The wider the hysteresis bandwidth is, the smaller is the switching frequency, and vice versa. The implementation of a hysteresis controller is theoretically simple and provides a good dynamic performance in addition to providing a variable switching frequency [64]. Unlike the PI d-q controller, the hysteresis controller like the PR controller does not require information of the PLL

phase angle for synchronous reference frame transformations but requires the phase angle for current reference generation. An error in the phase angle generation may result in generating erroneous current references especially under low SCR values as validated through simulation results in [29], thus affecting the control performance.

2.3.3. Modulation Strategies - C

The three modulation signals v_{ca}, v_{cb} and v_{cc} generated from block ***B*** using either PI d-q control as shown in figure 4 or the PR controller are used to generate Pulse-Width-Modulation (PWM) signals for the converter power switches. Popular modulation strategies include Sinusoidal Pulse-width modulation (SPWM) and Space vector modulation (SVM) that are explained in the following sections [53], [54], [65].

2.3.3.1. SPWM

The basic functioning principle of SPWM is presented in figure 2.19 where the modulation signal and the carrier signal for each phase are compared with each other to generate the desired PWM signal. For digital implemtation this is usually done internally by a specific hardware unit in the DSP of FPGA using a comparator as shown in figure 2.19. The carrier signal is generated by a timer that runs independently from the central processing unit (CPU).

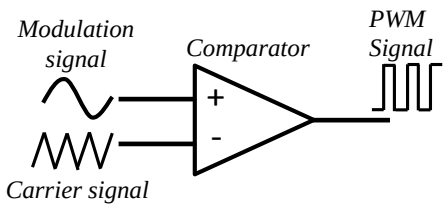


Figure 2.19: PWM generation

The frequency of the carrier signal is fixed and defined by the user, thus giving the converter a fixed switching frequency as opposed to the case in hysteresis controller where the switching frequency is variable.

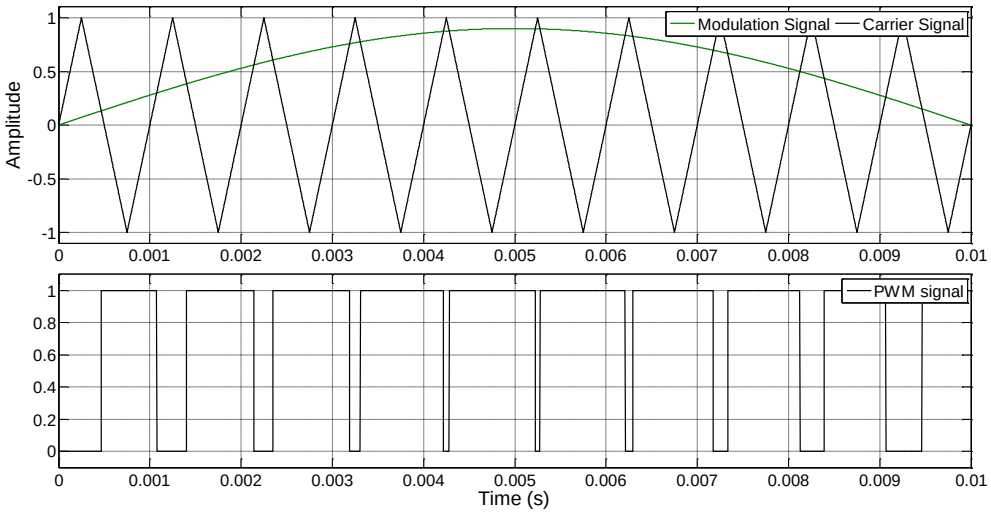


Figure 2.20: PWM generation using SPWM

The generated PWM signal shown in p.u. in figure 2.20 defines the turning ON and OFF of the power converter switches.

2.3.3.2. SVM

The space vector modulation (SVM) works on a sector-by-sector basis and is specifically developed for digital implementation in 3-phase converters. For example, in figure 2.21, the sector allocation (*I-VI*) of a three phase two-level converter is shown while its voltage levels are shown in table 4.1 in chapter 4.

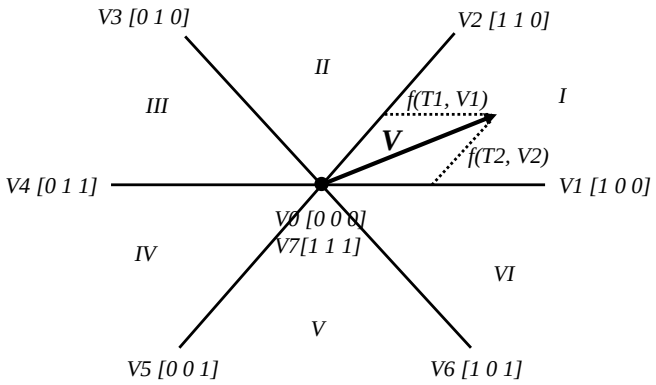


Figure 2.21: PWM generation using SVM

If $\boldsymbol{V}$ is the desired voltage vector for the converter output to generate for sector *I* in figure 2.21. It can be synthesized by the sum of the two active vectors, *V1* and *V2*, with respect to their application times as shown in equation (2.10):

$$\boldsymbol{V} = T_1 \cdot \boldsymbol{V}1 + T_2 \cdot \boldsymbol{V}2 \tag{2.10}$$

T_1 and T_2 signify the active vector application times and are calculated as explained in [53] for two-level rectifiers using classical control algorithm or using advanced predictive control methods that rely on the information of the optimized switching sequence [66], thus calculating the duty cycles for the applied space voltage vectors for each sector. Based on the information of the active vectors application times, the application time for the zero vector can be calculated such as:

$$T_0 = T_S - (T_1 + T_2) \tag{2.11}$$

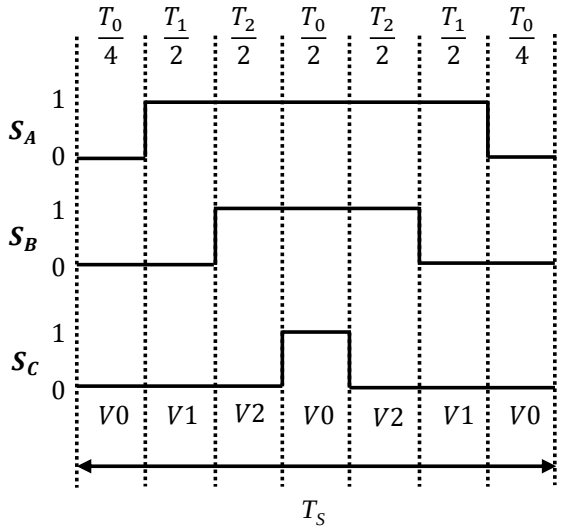


Figure 2.22: Switching Pulse Pattern for Sector I

Figure 2.22 shows a three phase representation of a two level converter switching sequence in sector 1 of figure 2.21 that applies the switching signals S_A, S_B and S_C for the calculated times T_1, T_2 and T_0. In order to reduce switching losses and harmonic content, the switching signals are applied in a symmetrical way such that between the transitions from one sector to another the zero vectors are always present [53]. As the application times are fixed in SVM technique, the converter switching frequency is fixed.

2.3.4 Summary

To summarize, this section explained the commonly applied PLL techniques for phase angle estimation used for phase synchronization between the supply voltage and current. A comparison between the SRF-PLL, P-PLL and DSOGI-PLL under three different SCR scenarios was presented.

Moreover, a brief insight into the commonly used grid connected converter control strategies has also been given. While the PI d-q based control strategy is the most widely applied control strategy, its performance under a weak grid scenario gets

affected due to an inaccurate phase angle generation which results in an unsatisfactory synchronous reference frame transformation and control variable reference generation. On the other hand the PR controller provides a better steady state error response as compared to a classical PI controller and has better harmonic filtering capability due to its resonant filter. However, under low SCR values, due to an incorrect phase angle generation the control variable reference can show an unsatisfactory response. Similarly, though the hysteresis control is fairly simple to compute, under low SCR values its performance gets significantly affected due to irregularities in the phase angle generation that results in an inaccurate current reference generation and therefore in a poor current control. The performance of these controllers can be improved by re-tuning the gains of the PLL; however, that may not present as an optimal solution since the grid impedance variation may not remain consistent and also smaller gains slow down the performance of a PLL, resulting in a larger settling time to a transient variation. The classical modulation strategies like SPWM and SVM used for PWM signal generation for power converter switches have been briefly explained as well.

As explained in section 2.3.2, when the SCR value is less than 10 the phase angle generated by the PLL shows an unsatisfactory behavior to presence of grid impedance. This gives rise to incorrect phase synchronization between voltage and phase current at the point of common coupling. Therefore, knowledge of grid impedance value becomes of a paramount importance in low SCR values to provide better control performance. Hence, the next section explains a few of the commonly applied grid impedance estimation techniques for three phase two-level grid connected converters.

2.4. Grid impedance estimation techniques

Figure 2.23 shows an equivalent representation of a three phase grid-connected converter where grid impedance is represented as an inductive-resistive (L_S, r_S) circuit [67].

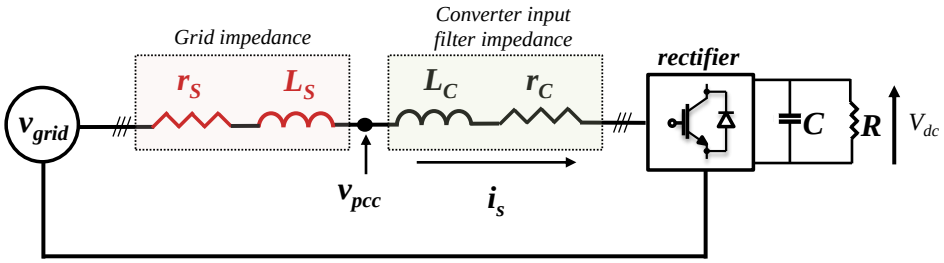


Figure 2.23: Grid impedance representation for a three-phase grid-connected converter

When the power converter is connected to a grid that is not stiff, also referred as Weak Grid where the SCR value is less than 10 [68], not knowing the value of grid impedance represents a big problem. Grid impedance can also commonly vary due to environmental changes, long distance transmission cables or due to presence of harmonics from non-linear loads connected on the transmission line [67]. Several authors have suggested different methods to estimate the grid impedance:

In [69] authors propose variation in active and reactive power and perform signal processing techniques like Fast-Fourier-Transform (FFT) on the voltage and current harmonic magnitudes at the PCC to calculate the grid impedance; [70] suggests injecting a transient in the supply current at the PCC and then measuring the voltage response. The impedance is obtained in function of frequency by

$$Z = \frac{FFT\ (V)}{FFT(I)}$$

Impedance estimation has also been implemented using model based identification methods [15] or using the estimated virtual-flux to estimate the line impedance [3].

2.4.1. Estimation using a controlled voltage disturbance

The authors have proposed an estimation method for grid impedance in a grid connected converter, [1], through injection of a controlled voltage transient at the point of common coupling. The principle of operation is such that the frequency of the transient signal is 6.25Hz. This choice allows a sufficient resolution in order to obtain an accurate behavior of supply impedance magnitude and phase in function of frequency. It is important to note that the frequency of transient injection should be different than the fundamental frequency of the voltage and current so the calculations are not affected by the fundamental frequency and its harmonics. The transient is injected through modification in PWM generation, where the voltage references are varied for a period of 160ms (6.25Hz). The voltage and current data is first recorded for 160ms before the transient injection and is then recorded after the transient injection for a period of 160ms.

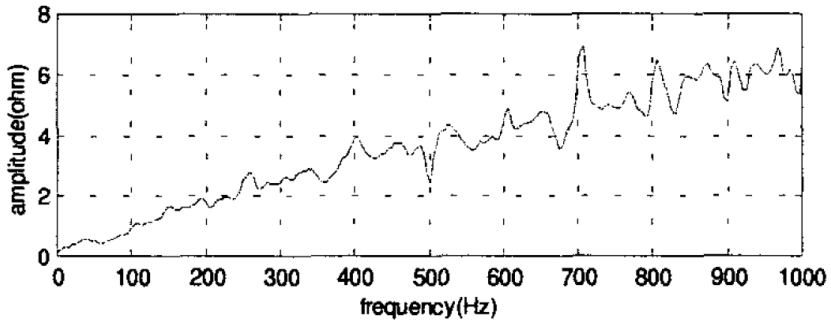


Figure 2.24: Grid impedance estimation from [1]

The data to be analyzed is obtained by subtraction of the information before and after the transient injection. The resultant data is used to achieve the harmonic magnitudes

and phases of the voltage and current at the PCC. Equation 2.8 explains the calculation of the grid impedance:

$$|Z(i)| = \frac{v_{pcc}(i)}{i_S(i)} \qquad \angle Z(i) = \frac{\angle v_{pcc}(i)}{\angle i_S(i)} \tag{2.12}$$

Where, *i* denotes the number of harmonic magnitudes considered over a wide frequency range. Results obtained in [1] for the estimation of grid impedance magnitude in function of frequency are reported in figure 2.24. The harmonic magnitudes are imported from the DSP to MATLAB using a Host PC so the data can be processed using a MATLAB built-in block referred as Transfer Function Estimation (TFE). Once all the data is recorded, the resulting estimated grid impedance is plotted through calculation in equation (2.12) as shown in figure 2.24.

Though the method proposed is mathematically feasible, it requires a high computational effort required due to signal processing (FFT). Moreover, since the FFT based methods are usually carried out in a standalone environment, the controller in this case is not updated in real-time with the latest variation in grid impedance. However, the authors of this method have proposed further suggestions to estimate the grid impedance in real-time and their work is on-going in this aspect.

2.4.2. Estimation based on active power variations

The method proposed by authors in [2] estimates the grid impedance based on variation in the active power at two different points and recording the voltage and current obtained at the PCC for these two points. The variation in power is not at two sampling instants; instead it takes place at regular time intervals of approximately 0.25s. The

operating principle is such that grid impedance, Z_g, is calculated as shown in the set of equations below with reference to figure 2.23:

$$v_{pcc1} = v_{grid1} + Z_g \cdot i_{S1} \tag{2.13a}$$

$$v_{pcc2} = v_{grid2} + Z_g \cdot i_{S2} \tag{2.13b}$$

Where, v_{pcc1}, v_{pcc2}, i_{s1} and i_{s2} are the measured voltages and currents at the PCC at two time instants, Z_g is the grid impedance (L_S, r_S) and v_{grid1} and v_{grid2} are the grid voltages at two time instants. Considering the variation in Z_g is not significant and that the grid voltage at the two operating points remains consistent, by solving equations (2.13a) and (2.13b) simultaneously Z_g is equated:

$$Z_g = \frac{\Delta v_{pcc}}{\Delta i_S} \tag{2.14}$$

Where,

$$\Delta v_{pcc} = v_{pcc1} - v_{pcc2}$$

$$\Delta i_S = i_{S1} - i_{S2}$$

are the voltage and current variations at the point of common coupling. The inductive and resistive parts of Z_g in (2.14) are obtained by transforming the above equations into their respective synchronous reference frames as shown in equations (2.15a) and (2.15b) [2].

$$R = \frac{(v_{q1} - v_{q2}) \cdot (i_{q1} - i_{q2}) + (v_{d1} - v_{d2}) \cdot (i_{d1} - i_{d2})}{(i_{q1} - i_{q2})^2 + (i_{d1} - i_{d2})^2} \tag{2.15a}$$

$$\omega L = \frac{(v_{d1} - v_{d2}) \cdot (i_{q1} - i_{q2}) - (v_{q1} - v_{q2}) \cdot (i_{d1} - i_{d2})}{(i_{q1} - i_{q2})^2 + (i_{d1} - i_{d2})^2} \tag{2.15b}$$

Where, v_{d1}, v_{d2}, v_{q1}, v_{q2}, i_{d1}, i_{d2}, i_{q1} and i_{q2} are the voltages and supply current at the point of coupling represented in synchronous reference frame. The working principle is also explained in figure 2.25 for two operating points P1,Q1 and P2,Q2:

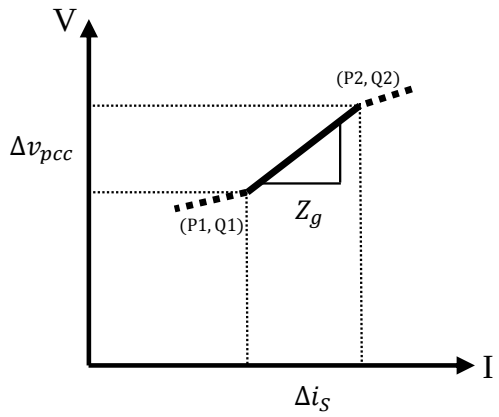


Figure 2.25: Working principle of [2]

The method proposed estimates grid impedance in real-time. Figure 2.26 shows the experimental result of the proposed grid impedance estimation. As can be observed, the experimental results presented in [2] show a steady error more than 20% on the grid inductance estimation while the resistive estimation has a lesser steady state error of less than 10% on average.

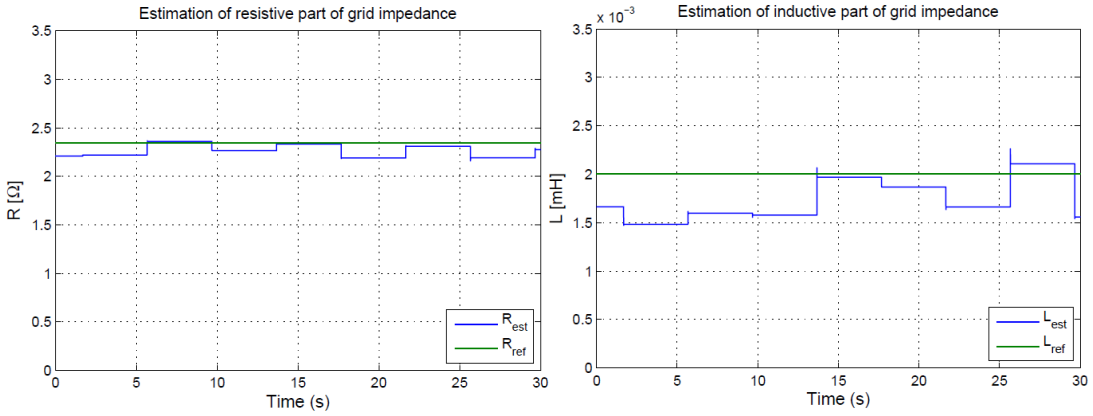


Figure 2.26: Experimental validation of grid impedance estimation in [2]

The method uses a simple arctangent of the synchronous reference frame voltages to obtain the grid phase angle. The results show that under low values of grid impedance where the grid has a high SCR, the estimation algorithm may not show significant errors. While under low SCR of value less than 10, the proposed estimation algorithm may loose its performance and more advanced PLL techniques need to be used for angle generation.

2.4.3. Estimation based on Virtual-Flux-Based Predictive Direct Power Control

The authors in [61] propose a converter line inductance estimation method using a predictive direct power control to improve the traditional voltage oriented control (VOC) technique by avoiding the use of a PLL and instead control the power factor close to unity by directly controlling the active and reactive power flow. For variations in the converter line inductance as compared to the model inductance value, the control performance can get affected. The grid connected converter as shown in figure 2.23 is represented in its synchronous reference frame coordinates for the voltage and current under unity power factor in figure 2.27 that is used for line inductance estimation method in [61].

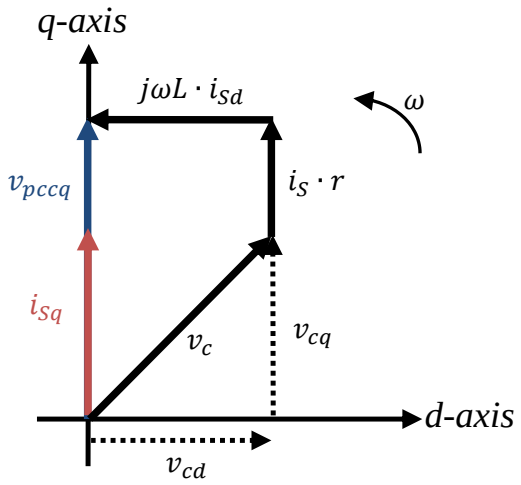


Figure 2.27: Working principle of [61]

The converter voltage *d-q* components, v_{cd} and v_{cq}, are calculated by using the switching signals and the dc-link voltage after transformation from the stationary reference frame in *α-β*. Solving the vectorial representation of figure 2.27, the following sets of equations describe the inductance estimation algorithm:

$$v_{cd} = j\omega L \cdot i_{Sd} \tag{2.16}$$

An absolute value of (2.16) is taken such that it results in:

$$|v_{cd}| = \omega L \cdot |i_{Sd}| \tag{2.17}$$

Therefore, the estimated inductance is equated as:

$$L = \frac{|v_{cd}|}{\omega \cdot |i_{Sd}|} \tag{2.18}$$

Where, $|v_{cd}|$ represents the converter voltage magnitude, $|i_{Sd}|$ represents the AC current magnitude and the term ω is the angular frequency fixed at 50Hz. The approach in [61] provides the estimation of line inductance, referred as the choke inductance, in real time and updates the controller in real time. Instead of estimating the variation in grid inductance, the method estimates the value of the converter line inductance in case there is a mismatch between the model value and the actual value. The results in figure

2.28 for [61] show the estimated inductance, L_{est}, response to a large step in line inductance.

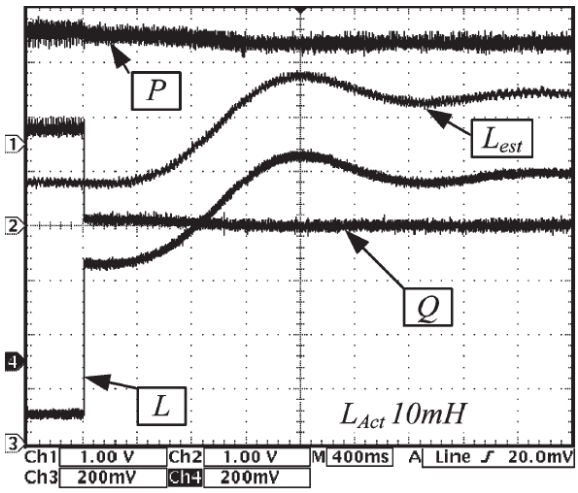


Figure 2.28: Inductance estimation for [61]

However, the dynamic response to a transient variation takes greater than 2s to reach a steady state value, i.e. approximately more than 100 fundamental cycles since the fundamental frequency is 50Hz. Once the steady state is reached, the proposed method estimates the variation accurately with a steady error less than 5% and gives a quasi-sinusoidal current waveform with a THD value less than 5%. The practical implementation using a DSP is simple and uses a second order low pass filter on the estimated inductance to filter out the high frequency harmonics due to converter switching that may slow down the dynamics of the estimator.

2.4.4. Estimation based on active and reactive power samples before and after a commutation

The inductance estimation method proposed in [4] is based on the active and reactive power calculations before and after a commutation instant as shown in equations (2.19) and (2.20).

$$P_t - P_t{}' = 0 \tag{2.19}$$

$$Q_t - Q_t{}' = 0 \tag{2.20}$$

Where, P_t and $P_t{}'$, Q_t and $Q_t{}'$, stand for the active and reactive power samples before and after a sampling period, respectively, as shown in figure 2.29.

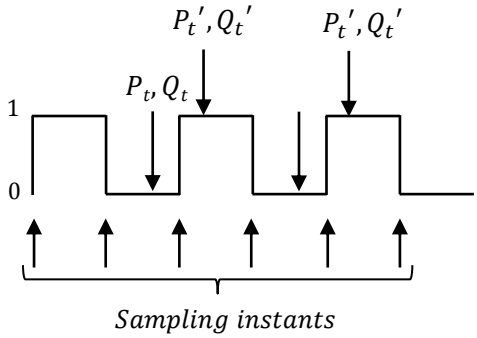


Figure 2.29: Working principle of [4]

The active power and reactive power for one instant are formulated in three phase representation as:

$$P = v_{pcca}i_{Sa} + v_{pccb}i_{Sb} + v_{pccc}i_{Sc} \tag{2.21}$$

$$Q = \frac{1}{\sqrt{3}}\Big((v_{pcc} - v_{pccc})i_{Sa} + (v_{pccc} - v_{pcca})i_{Sb} + (v_{pcca} - v_{pccb})i_{Sc}\Big) \tag{2.22}$$

Where, for phase *A*, the supply voltage, v_{pcca}, is represented by the voltage drop across the line inductance, *L*, plus the converter input voltage, v_{ca}.

$$v_{pcca} = L\frac{di_{Sa}}{dt} + v_{ca} \tag{2.23}$$

Equation (2.23) is replicated for phases *b* and *c* to be substituted in (2.21) and (2.22), respectively for active and reactive power calculations. Thus, the active and reactive powers before and after the sampling instants are calculated. Solving equations (2.21) and (2.22) simultaneously for the two sampling instants, the estimated inductance is equated as:

$$L = -\frac{V_{dc}\big(i_{Sa}(S_{at} - S_{at}{}') + i_{Sb}(S_{bt} - S_{bt}{}') + i_{Sc}(S_{ct} - S_{ct}{}')\big)}{i_{Sa}\left(\frac{di_{Sa}}{dt_t} - \frac{di_{Sa}}{dt_t{}'}\right) + i_{Sb}\left(\frac{di_{Sb}}{dt_t} - \frac{di_{Sb}}{dt_t{}'}\right) + i_{Sc}\left(\frac{di_{Sc}}{dt_t} - \frac{di_{Sc}}{dt_t{}'}\right)} \tag{2.24}$$

Where,$S_{at}, S_{bt}, S_{ct}, S_{at}', S_{bt}'$ and S_{ct}' are the switching signals to be defined for the three phases before and after a commutation occurs. V_{dc} is the dc-link voltage and the three phase currents are represented by i_{Sa}, i_{Sb} and $i_{Sc.}$ The method proposed in [4] estimates the effect of mismatch in the coupling inductance in real-time and updates the controller in real-time. Figure 2.30 shows the percentage of error in the proposed estimation algorithm when tested for a non-ideal grid condition. The results show the percentage error of estimated inductance is less than ±1% for the different non-ideal conditions. Though the results presented in [4] show a good response of the estimator to a mismatched inductance value, they do not show the performance of the estimator under low SCR values and for transient variations in case of Weak grid operation.

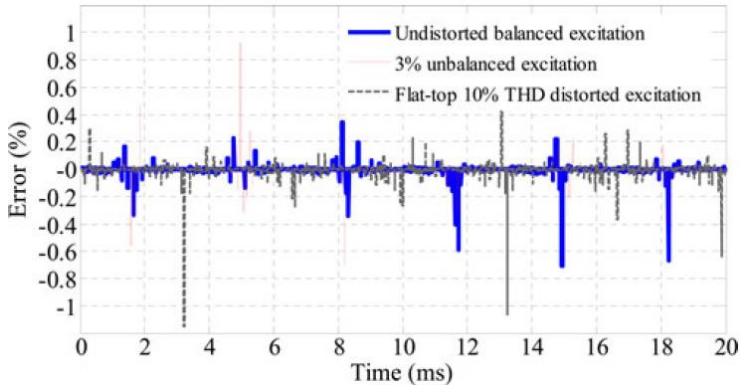


Figure 2.30: Percentage of error in inductance estimation [4]

2.5. Conclusion

This chapter started by giving an introduction about the operating points for a grid connected converter under different power conditions. The converter topology used for the project, a three phase two-level rectifier, thus having and AC-DC configuration, has also been introduced. This converter topology has been chosen due to its lesser

complexity and easy implementation as compared to other structures like multilevel converters.

The performance of commonly used PLL techniques was explained under presence of grid impedance, in particular for low SCR values where the PLL takes a longer time to reach an accurate estimated value of the phase angle.

Three control strategies for grid-connected converters, d-q PI, PR and hysteresis control were explained with emphasis on their performance under presence of grid impedance as explained in the researched literature.

The two most widely applied modulation strategies, SPWM and SVM, were briefly explained as well.

The performance of the grid-connected converter control gets affected in the presence of substantial grid impedance. Therefore, a comprehensive literature research was presented for various methods used for estimation of grid impedance using both online and offline methods.

The goal of the project was to develop a grid impedance estimation algorithm that estimates grid impedance in real-time and updates the converter controller in real-time even for cases when the SCR is less than 5, i.e. a Weak Grid operation. To achieve the task, a Model Based Predictive Direct Power Control (MP-DPC) was chosen due to its ability of providing a close to unity power factor control by directly controlling the active and reactive powers without requiring any cascaded control loops or PLLs for phase synchronisation. Two grid impedance estimation techniques have been proposed in this work and are presented in chapter 4.

Chapter 2: Introduction to converters, control techniques, modulation techniques and grid impedance estimation techniques

Before explaining the proposed methodology in chapter 4, a brief background on predictive control is presented in chapter 3.

Chapter 3: Predictive Control

3.1. Introduction

The previous chapter gave a literature review on different converter topologies used for grid connection in addition to a literature review on techniques for grid impedance estimation. This chapter gives a general understanding of the predictive control strategy and its demand as a control strategy to be used in the power electronic converters with emphasis on the modern day control requirements. The chapter also highlights different types of control approaches that belong to the same family.

3.2. Predictive control for power converters

Predictive control techniques have been widely applied in recent decades for different power electronic converter applications [31], [71]–[74]. Research in literature shows it to be a promising alternative to already applied popular concepts, like Voltage Oriented Control (VOC), vector control and direct torque control, for example [47].

The advantages of using predictive control over traditional control techniques in power electronics include its ability for including constraints and nonlinearities; easier concept and implementation, fast dynamic response, provides a multivariable control thus multiple variables can be controlled within a single control loop, as depicted in figure 3.1. In addition, the main characteristic of predictive control is that it relies on the model of the system to make predictions of the future behavior of the controlled variables and using a predefined optimization criteria selects the optimal actuation [63]. With the advancement in the field of modern high speed and high precision microprocessors, for instance, faster DSPs and FPGAs can facilitate the application of predictive control, solving complex calculations at a high speed [75]. Moreover, predictive control

provides an advantage of avoiding the use of cascaded control loops, like in the case of VOC for example, and also achieves fast response to transient variations [74], [76].

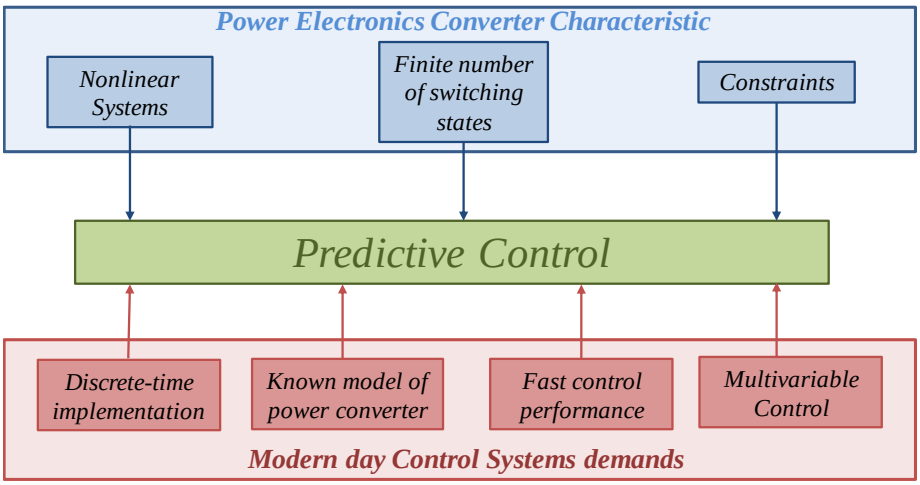


Figure 3.1: Characteristics of power converters and modern control systems demands

Different types of predictive control techniques applied in power electronics converters include hysteresis-based predictive control, dead-beat control and model predictive control [63], [71], [77]–[81]. In hysteresis-based predictive control the control variables are restricted within a tolerance band to generate the switching functions and results in a variable switching frequency, while in dead-beat control the optimization takes place at the next sampling instant with the aim of achieving zero error between the control variable and the reference value [74], [76]. On the contrary, a model predictive control technique is divided into further two types; continuous control set model predictive control (CCS-MPC) and finite control set model predictive control (FCS-MPC) [72], [74], [76], [82], [83]. The CCS-MPC uses a modulator to generate the respective switching signals for the power converter switches, whereas the FCS-MPC relies on minimization of an optimization function to generate the required switching signals. Since both dead-beat control and CCS-MPC use a modulator, the switching frequency is

fixed. For FCS-MPC, however, the switching frequency is variable. The commonly used predictive control techniques, dead-beat control and MPC, are addressed in the following sections.

3.3. Deadbeat Control

Deadbeat control, proposed about two decades ago, is a well-known predictive control technique, [84]–[87], that uses the system model at every sampling interval to calculate the required voltage reference for the PWM in order to track the controlled variable reference value in the next sampling interval [63]. A general deadbeat current control scheme for a grid-connected converter is presented in figure 3.2.

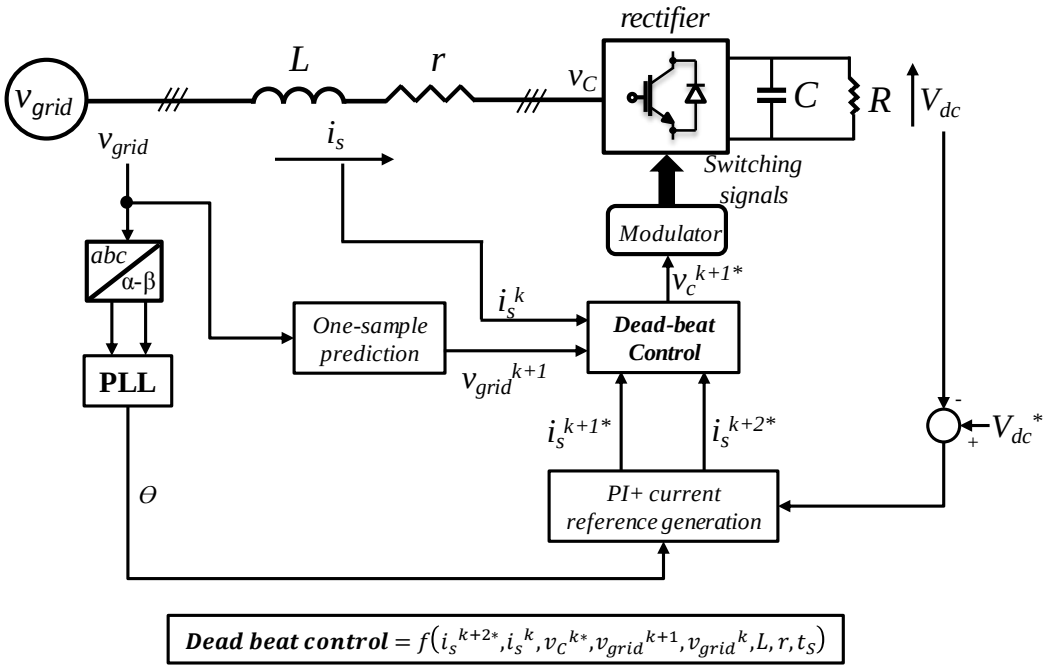


Figure 3.2: Basic scheme of digital deadbeat current control.

The current references used for the dead-beat controller are generated by means of a dc-link voltage PI controller and information about the phase angle from the PLL (as explained in chapter 2) [88]. Using phase *A* from figure 3.2, the mathematical

explanation of the dead-beat algorithm is presented below [38] to define the continuous-time AC model of the grid-connected converter:

$$v_{grida}(t) = L\frac{di_{Sa}(t)}{dt} + r \cdot i_{Sa}(t) + v_{Ca}(t) \tag{3.1}$$

Where, v_{grida} is the supply voltage, i_{sa} is the supply current, v_{ca} is the converter input voltage and L and r are the converter input filter inductance and its equivalent series resistance. The first order Euler approximation method is used to obtain the discrete-time model of (3.1) for implementation as [74]:

$$v_{grida}{}^{k} = \frac{L}{t_s}\left(i_{Sa}{}^{k+1} - i_{Sa}{}^{k}\right) + r \cdot i_{Sa}{}^{k} + v_{Ca}{}^{k} \tag{3.2}$$

(3.2) can be re-arranged as:

$$\left(v_{grida}{}^{k} - v_{Ca}{}^{k}\right) = \frac{L}{t_s}\left(i_{Sa}{}^{k+1} - i_{Sa}{}^{k}\right) + r \cdot i_{Sa}{}^{k} \tag{3.3}$$

Where, the terms *k* and *k+1* mean the present and one-sample ahead sampling instant, t_s is the sample time and the supply current prediction for phase *A* is hence given by:

$$i_{Sa}{}^{k+1} = \frac{t_s}{L}\left(v_{grida}{}^{k} - v_{Ca}{}^{k}\right) + \left(1 - r\frac{t_s}{L}\right) i_{Sa}{}^{k} \tag{3.4}$$

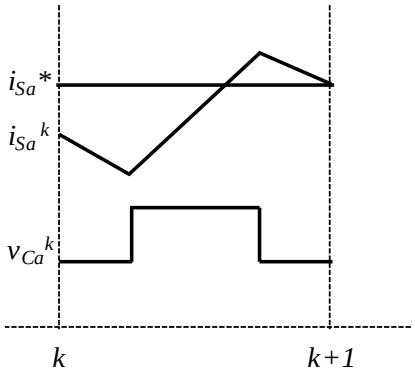


Figure 3.3: Basic operation of deadbeat current control

With reference to figure 3.3, which explains the basic working principle of a deadbeat current control, at instant *k* the current ($i_{sa}{}^{k}$) is different from the reference current ($i_{sa}{}^{*}$). At instant *k+1*, the aim is to have the current prediction to be equal or very close to the reference value (error equal to zero) [63]. Hence, the error between the reference value of the current at *k+1* ($i_{sa}{}^{k+1*}$) and the measured value at *k* is used to generate the converter voltage reference at *k* as shown in (3.5):

$$v_{Ca}{}^{k*} = v_{grida}{}^{k} - \left(\frac{L}{t_s}\left(i_{Sa}{}^{k+1*} - i_{Sa}{}^{k}\right) + r \cdot i_{Sa}{}^{k}\right) \tag{3.5}$$

For practical implementation, however, to compensate for the computational delay introduced due to the processing time required by the DSP or a microcontroller [38] the converter voltage reference of (3.5) is generated at *k+1* while the current prediction at *k+2* is set equal to the reference value of the current [88].

The voltage reference calculation of (3.5) is similarly carried out for phases *b* and *c* as well. Using modulation strategies like SPWM or SVM, these voltage references are then used to generate the converter switching signals.

The dead-beat control has a fast dynamic response thus responding to transient variations quickly and provides an advantage of using modulation strategies like SPWM and SVM, for example, thus providing a fixed converter switching frequency. However, for grid-connected converters where the grid impedance can have significant variations, it can become challenging to use dead-beat current control as it relies on the phase angle for current reference generation in addition to grid synchronization and hence the PLL needs to be regularly tuned.

3.4. Model Predictive Control

3.4.1. General concept of MPC

Figure 3.4 shows a general working principle of MPC for a power converter with the help of a block diagram while the calculation of a state-space model used in MPC can be seen in Appendix B. The predictive control model in figure 3.4 takes as input measurements from the load, *x(k)*, to calculate predictions *x(k+1)* of the control variable at the next sampling instant. These predictions are calculated for the possible switching combinations used in the power converters. For example, for a three phase two level converter the number of switching combinations are 8 while for a three phase 3 level converter the number of switching combinations are 27, and so on. The number of sample-ahead predictions of the control variable is determined by the prediction horizon N_p. The predicted values along with their respective reference values are optimized using a cost-function optimization criterion to generate the optimum switching signal *S* for the power converter. This process repeats every sampling interval to calculate prediction values and the optimum switching signals [74].

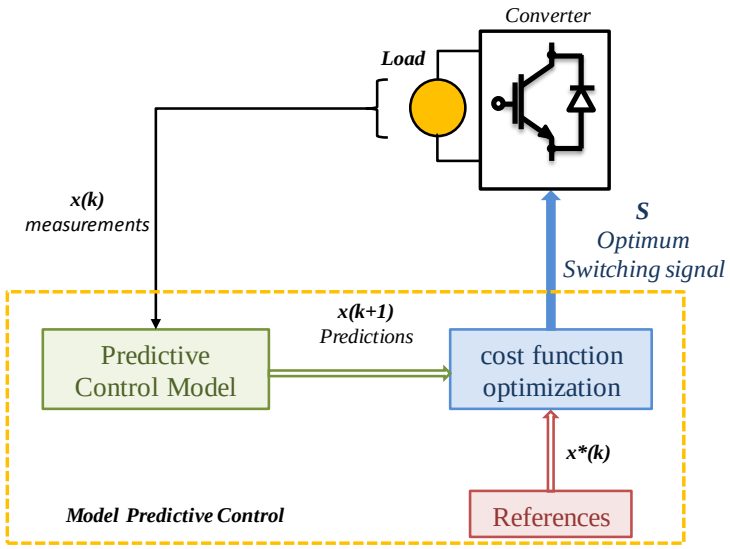


Figure 3.4: General working principle of model predictive control

3.4.2. Sampling intervals in MPC

Figure 3.5 explains the concept of general MPC working principle of figure 3.4 with respect to sampling intervals.

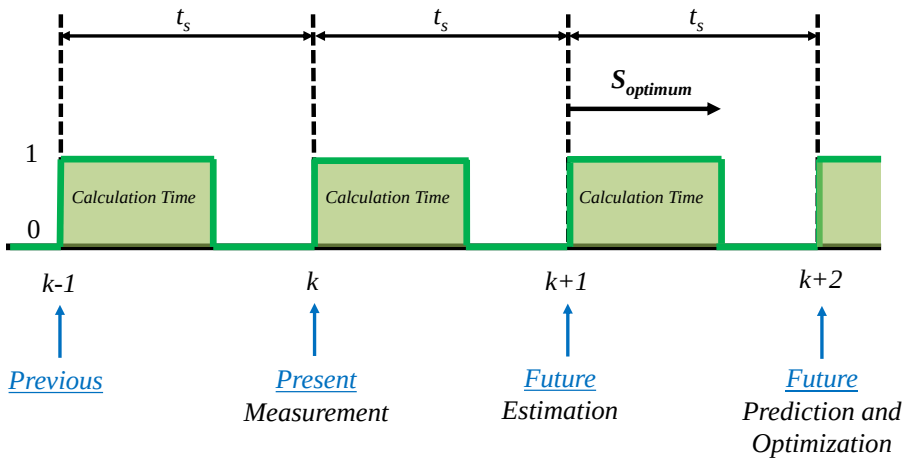


Figure 3.5: Sampling intervals for MPC

In figure 3.5, four sampling instants are shown as *k-1*, *k*, *k+1* and *k+2* that represent the *previous*, *present*, *one-sample-ahead prediction* and *two-sample-ahead prediction* instants while t_s is the sampling interval, respectively. The measurements of the currents and the voltages for the predictive control process are taken at instant *k*. Utilizing these measurements at *k* and the optimum switching signals, estimations or predictions at instant *k+1* are calculated. These predictions are further used to predict the future behavior of the control variable for all the possible switching combinations at the instant *k+2*. The reason to calculate predictions at instant *k+2* is to compensate for the delay due to practical system calculation times. At *k+2*, using cost-function optimization the control reference is compared with each of the possible calculated predictions. At this instant, the switching combination that gives the minimum difference between reference value and the predicted value is selected as the optimum switching signal and is applied

to the converter switches, referred as $S_{optimum}$ in figure 3.5. The basic block scheme of FCS-MPC for a three-phase grid connected converter is explained with the help of a simplified FCS-MPC current controller in section 3.4.3.

3.4.3. FCS-MPC Current Control

With the help of figure 3.5 and the sub-blocks *A*, *B*, *C* and *D* in figure 3.6, the basic FCS-MPC operating principle for a current control is explained in this section, whereas, a FCS-MPC Direct Power Control is explained in chapter 4.

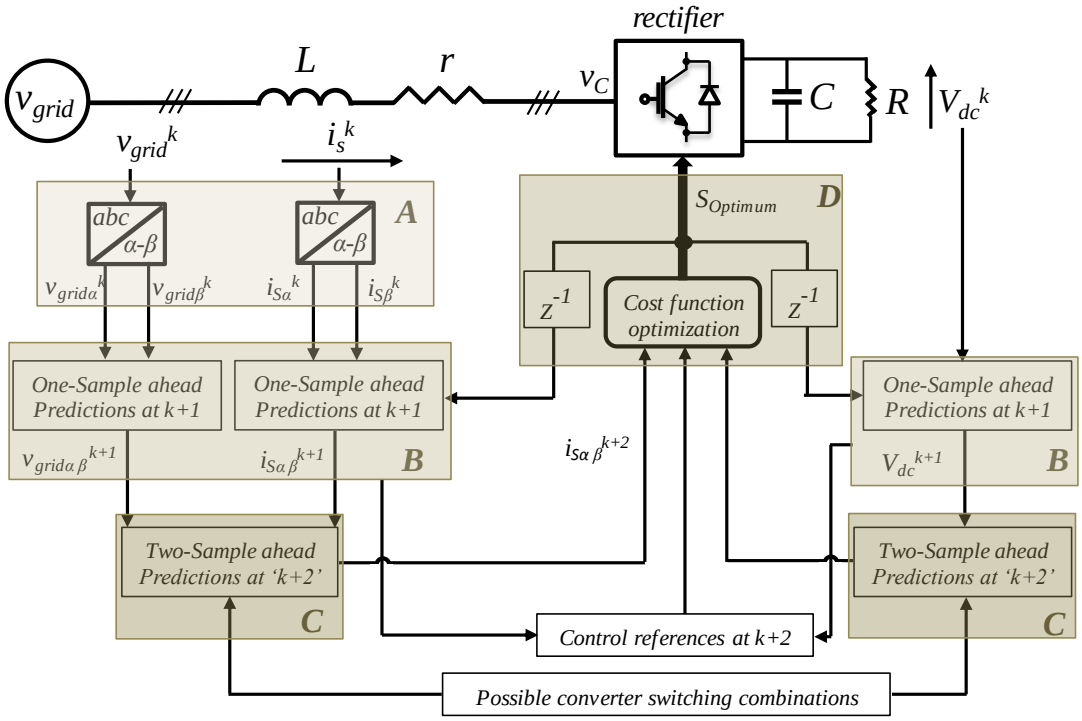


Figure 3.6: Basic FCS-MPC current control scheme for power converters

3.4.3.1. Measurements at instant k - A

The grid voltages (v_{grid}^{k}), supply currents (i_s^{k}) and the dc-link voltage (V_{dc}^{k}) are sampled at the present instant *k* as measurements for the FCS-MPC. For simplification of the control algorithm, the three phase coordinates are transformed into the respective two-

phase α-β coordinates as $v_{grid\alpha\beta}^{\ k}$ and $i_{s\alpha\beta}^{\ k}$ using the Clarke's transformation as shown in Appendix C [55]. Normally for a current controlled FCS-MPC, the voltage stationary reference frame coordinates or rotating frame coordinates are used to calculate the phase angle with the help of PLL techniques as mentioned in chapter 2.3. For a Direct Power Control MPC, however, the need of PLLs is avoided by directly controlling the active and reactive powers, as will be explained in Chapter 4.

3.4.3.2. Predictions at instant k+1 - B

This block estimates the controlled variables at the future sampling instant *k+1* using information provided at the present sampling instant *k*. The grid voltage estimation at *k+1* is calculated using the popular Lagrange Interpolation, [38], while the supply current and the dc-link voltage control relies on the information of the optimized switching signals obtained from the cost-function optimization block (*block D*). Moreover, the estimations at *k+1* are used for calculation of the control variables references at the instant *k+2*. Equation (3.6) shows the continuous time domain model of the AC side in figure 3.6 for a lossless converter using the Kirchoff's Voltage Law (KVL).

$$\frac{di_{\alpha\beta}(t)}{dt} = \frac{1}{L} \cdot \left(v_{grid\alpha\beta}(t) - v_{C\alpha\beta}(t)\right) - i_{S\alpha\beta}(t) \cdot \frac{r}{L} \tag{3.6}$$

Where, L, r and $v_{c\alpha\beta}$ represent the AC side line inductance, resistance and the converter input voltage. Using the Euler Approximation method as shown in (3.7), the AC current derivative in (3.6) is discretized to obtain prediction for supply current at the instant *k+1* as shown in (3.8).

$$\frac{di_x(t)}{dt} = \frac{{i_x}^{k+1} - {i_x}^{k}}{t_s} \tag{3.7}$$

Where, *x* represents the control variable. Therefore,

$${i_{S\alpha\beta}}^{k+1} = \frac{t_s}{L} \cdot \left({v_{grid\alpha\beta}}^{k} - {v_{C\alpha\beta}}^{k}\right) + {i_{S\alpha\beta}}^{k} \cdot \left(1 - \frac{r \cdot t_S}{L}\right) \tag{3.8}$$

The converter voltage ${v_{C\alpha\beta}}^{k}$ is calculated using the optimized switching signal (explained in section D) and the DC-link voltage at the instant *k*.

3.4.3.3. Delay compensation - C

The delay caused by the calculation time of the DSP/FPGA in the practical implementation, if not compensated, affects the performance of MPC [89]. Therefore, in order to compensate this delay the control variables are predicted at two-sample instants in advance, i.e. at *k+2*. Equation (3.9) shows the supply current predictions at the instant *k+2* for the 8 switching combinations.

$${i_{S\alpha\beta}}^{k+2}(i) = \frac{t_s}{L} \cdot \left({v_{grid\alpha\beta}}^{k+1} - {v_{C\alpha\beta}}^{k+1}(i)\right) + {i_{S\alpha\beta}}^{k+1} \cdot \left(1 - \frac{r \cdot t_S}{L}\right) \tag{3.9}$$

Where, ${v_{grid\alpha\beta}}^{k+1}$ is obtained using the Lagrange Interpolation of ${v_{grid\alpha\beta}}^{k}$, the converter voltage is calculated using the DC voltage at *k+1* for the 8 switching combinations and ${i_{S\alpha\beta}}^{k+1}$ is represented in (3.8). The index *i* represents the 8 switching combinations as shown in sector representation of figure 2.21 of chapter 2 as *[000,100,110,010,011,001,101,111]*.

Since the predictions using the 8 switching combinations are carried at *k+2*, it becomes important to calculate the control references at the same instant *k+2* as well [79], [90].

The predictions and the respective references are used in the cost-function optimization block *D* to generate the optimum switching signal for the power converter.

3.4.3.4. Cost-function optimization - D

For an easier understanding, figure 3.7 explains the cost-function optimization criterion by showing variation of the control variable, i_S, using only three switching (S_1, S_2 and S_3) combinations instead of the 8 combinations (S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7), as it is for a two-level converter, and the control reference, $i_{S\alpha\beta\text{-}ref}$.

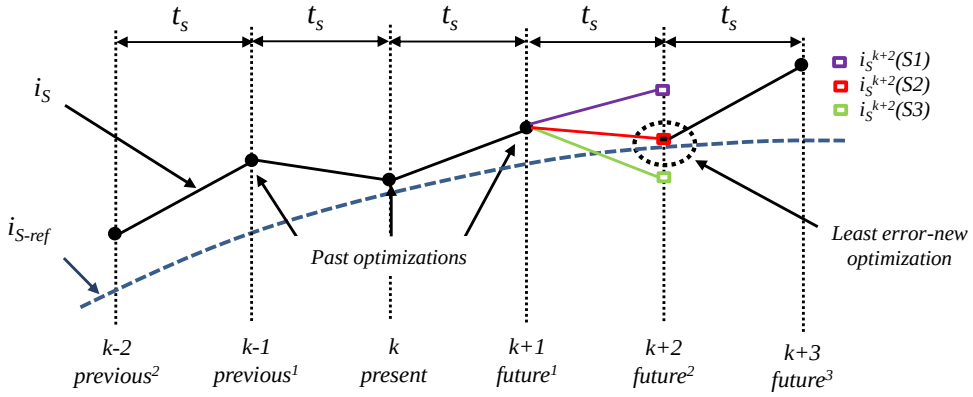


Figure 3.7: Switching state selection principle for FCS-MPC

The cost function, also referred as an error or objective function, is expressed in per-unit values and calculates the difference between the reference value and the predicted values [31], [72]–[74]:

$$g(i) = \lambda_\alpha \left| {i_{S\alpha-ref}}^{k+2} - {i_{S\alpha}}^{k+2}(i) \right| + \lambda_\beta \left| {i_{S\beta-ref}}^{k+2} - {i_{S\beta}}^{k+2}(i) \right| \quad (3.10)$$

Where, g defines the cost function. ${i_{S\alpha-ref}}^{k+2}$ and ${i_{S\beta-ref}}^{k+2}$ are the reference values. ${i_{S\alpha}}^{k+2}(i)$ and ${i_{S\beta}}^{k+2}(i)$ refer to the predicted values for the controlled variables. λ_α and λ_β are the weighting factors that are normally empirically designed or depending on which control variable in the cost-function needs more importance the weighting factor

accordingly has a high or low value [74]. The index *i* stands for the number of times the control variable need to be predicted for, which is usually the same as the number of converter switching combination. For each combination, at each sampling interval the error between the reference value and the prediction is calculated and the combination that gives the minimum value is selected and applied to the converter, referred as $S_{optimum}$ in figure 3.5. For example, in figure 3.7, the switching combination S2 used for the prediction $i_S^{k+2}(S2)$ gives the closest supply current prediction to the reference signal, hence *S2* is selected to be applied as the optimum signal. Similarly, this process is then repeated for the next sampling interval (referred as *receding horizon strategy*), generating the optimum switching signal for the converter each time. It is also possible that the same switching combination maintains closest to the reference signal for two or more consecutive sampling intervals, resulting in a variable switching frequency. However, several methods have been proposed in recent years that integrate a modulation strategy within the FCS-MPC to provide a fixed converter switching frequency to reduce the harmonic distortion and provide an improved current THD as compared to the FCS-MPC [91]–[93]. These methods will be used along with the proposed grid impedance estimation methods as future work for continuation of this project.

3.4.4. Application of MPC

To understand the application of MPC in different areas of power electronics, a vast literature research was carried out on the best scientific sources. This search addressed 4 areas of predictive control application: rectifiers, grid impedance estimation, motor

drives and inverters. The usage of MPC in these 4 areas has been summarized in the form a pie chart and a graph as shown in figures 3.8 and 3.9, respectively.

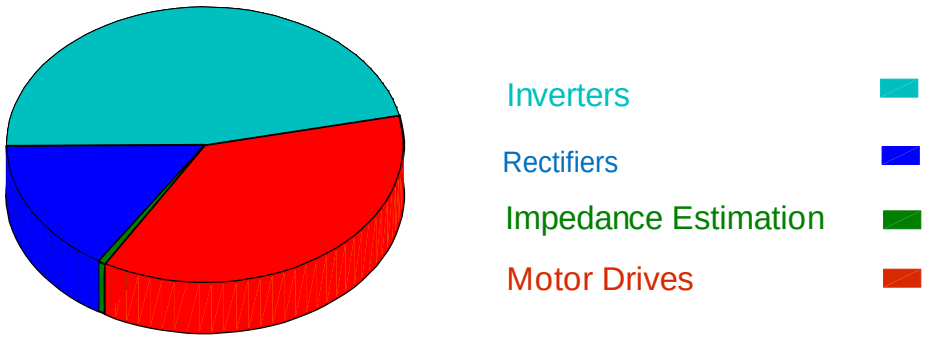


Figure 3.8: Contribution of MPC in 4 respective areas from 2007-2014.

The pie chart in figure 3.8 shows that even though MPC has been in use for power electronic converters for a few years now, the research work has been mostly focused on inverters and motor drives. Amongst these two areas, inverters that have been used for grid-connections, battery connections, uninterruptible power supplies, for example, have been the top priority for MPC implementation [94]–[96]. The second most applied predictive control area is in the field of high performance motor drives that provides, for example, torque control, speed and current control [97], [98]. On the other hand, rectifiers that use either model predictive current control or model predictive direct power control have only recently started to attract much attention of researchers [33], [67], [99], [100]. When a rectifier or an inverter is connected to a non-stiff grid, the unknown and high value of grid impedance with respect to the rectifier or inverter one generates mismatch between the model and the real system and therefore can affect the performance of the predictive controller, [3], [67], [101], [102]. For a robust operation of FCS-MPC in presence of parameter variations, it becomes vital to estimate these values if they are significant and compensate for them within the predictive controller to

make it work efficiently [67]. However, in the pie chart of figure 3.8 it can be observed that the application of MPC for grid impedance estimation has not been able to grab much attention as this concept is challenging and relatively new in MPC.

Figure 3.9 shows the amount of published work about MPC application in the 4 respective areas as mentioned earlier. As can be seen, MPC for grid connected converters has recently started to attract attention from researchers due to easier and less complex modeling, real-time implementation, fast integration, robust performance due to a fast dynamic response [3], [67], [103].

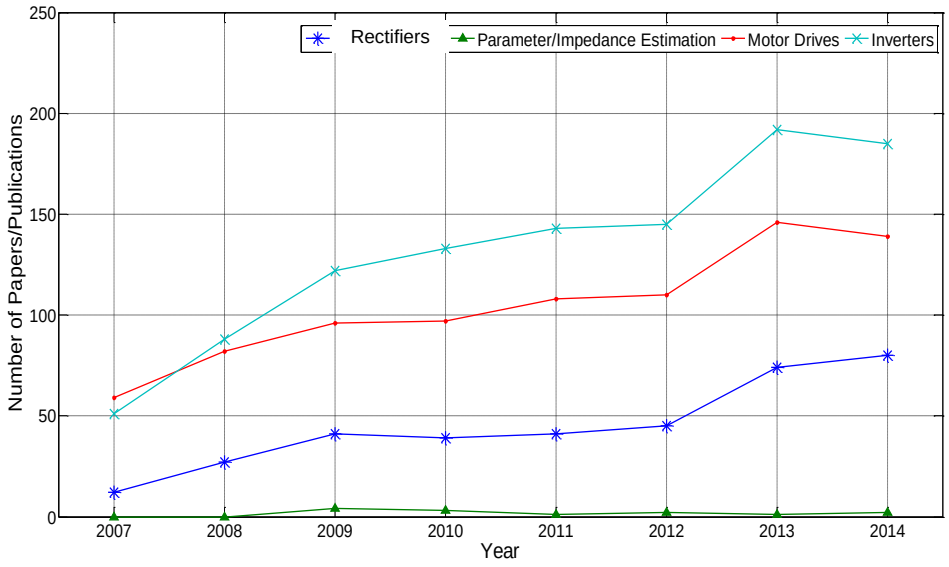


Figure 3.9: Increasing trend of MPC research work in 4 respective areas from 2007-2014.

This trend makes the research carried out in this project all the more significant as it may open opportunities for researchers to expand on the idea proposed in this work for using MPC to estimate grid impedance variations in grid connected converters.

In contrast to the above mentioned advantages of the FCS-MPC, a drawback of the FCS-MPC for grid-connected converters is the variable switching frequency that occurs

due to an absence of a modulation strategy; thus, resulting in a large ripple on the system waveforms. Therefore, normally smaller sample times are used for FCS-MPC application in order to provide a good power quality and a small value of THD.

3.4.5. Comparison between CCS-MPC and FCS-MPC

The authors in [99] have carried out a comparison between CCS-MPC and FCS-MPC for a current control in a three phase two level inverter feeding an inductive-resistive load with respect to their switching frequency, current THD, ripple in current to modulation index variation and their respective dynamic behavior to a step variation in current reference value when applied on a three phase two-level converter.

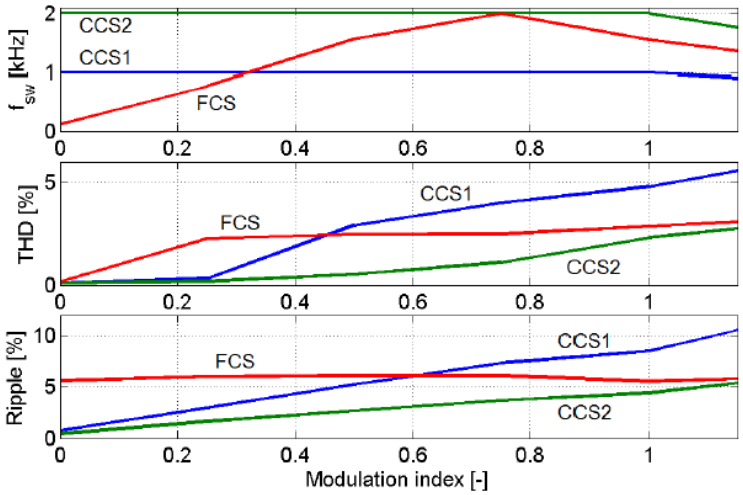
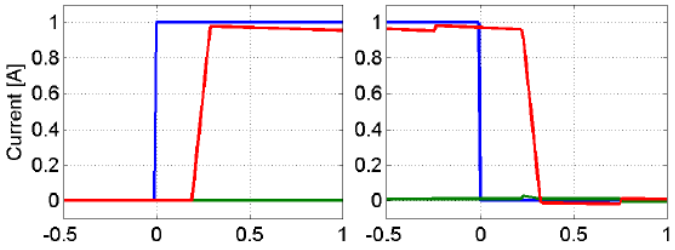


Figure 3.10: Steady state switching state, THD and current ripple comparison between CCS1, CCS2, FCS [99]

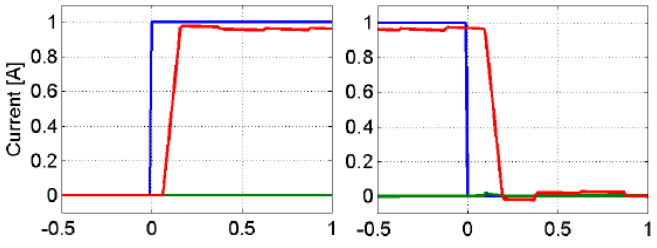
Figure 3.10 and 3.11 show these results where CCS1 refers to a CCS-MPC approach with 1kHz switching frequency, CCS2 refers to a CCS-MPC approach with 2kHz switching frequency and FCS refers to a FCS-MPC with a variable switching frequency averaging around 2kHz for a modulation index of 0.75 for the three respective approaches.

In figure 3.10, the CCS approaches show a constant switching frequency for variations in modulation indexes, however, an increase in the current THD and ripple is observed to an increase in the modulation index. On the contrary, the FCS shows a variable switching frequency to different operating points, however, a consistent value of THD and a constant value of current ripple quality were observed due to a smaller sampling time. Figure 3.11 shows the dynamic behavior of the three control approaches to a step variation of 1A in current reference value. Figure 3.11(a) and (b) present a slow dynamic performance for the CCS-MPC techniques due to larger sampling times at low switching frequencies, while the FCS in figure 3.11(c) shows a faster dynamic response to transient variations and a better current quality as it operates with a smaller sampling time.



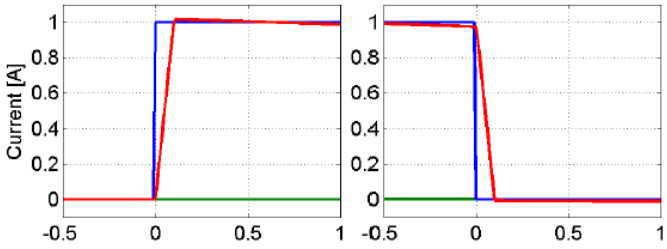
Time (s)

(a)



Time (s)

(b)



Time (s)

(c)

Figure 3.11: Comparison between (a) CCS1, (b) CCS2 and (c) FCS to a step variation in current reference [99]

3.5. Conclusion

This chapter gave an insight into an increasing demand of predictive control in the field of power electronics and addressed the commonly used predictive control strategies that include Deadbeat Control and FCS-MPC.

MPC provides several advantages like inclusion of nonlinearities and constraints within the control system. Moreover, it also provides a multi-variable control within a single control structure thus avoiding the use of cascaded control loops like internal and external PI controllers in case of voltage oriented control. Using different switching combinations for control variable predictions, MPC chooses the optimum switching signal for the power converter switches according to the minimization of a cost function.

However, according to the system demand and requirement, the performance of the predictive control varies. For example, for a grid-connected converter with presence of grid impedance, due to sensitivity of parameter mismatch the FCS-MPC performance may get affected. On the other hand, due to its flexible control structure and better dynamic response to transient variations, FCS-MPC provides a better platform to integrate grid impedance estimation methods within the controller.

The next chapter presents the model based predictive direct power control for a grid connected converter and presents in detail the control algorithm. The chapter will also present two novel grid impedance estimation algorithms that are used in real-time to update the FCS-MPC, thus providing a robust performance.

Chapter 4: Model Predictive Direct Power Control with online Grid Inductance estimation methods

4.1. Introduction

Chapter 3 gave a general description of the model based predictive control technique. A brief history of the control topology and the characteristics that make model predictive control a suitable choice for control of modern day converters has also been explained. This chapter focuses on a finite set Model Predictive Control (MPC) approach for a three-phase two-level active front end rectifier. The advantages of MPC for power converters lies in the fact that it does not require cascaded control loops or PWM modulators, provides a multivariable control and also provides fast dynamic response to transient variations, to name a few.

As any model based control technique, MPC is sensitive to model parameter variations. Since the supply impedance is generally an unknown parameter any significant variation in it can cause remarkable errors in the MPC control action, in case its value is not negligible compared to the converter input filter impedance. Therefore, in addition to explaining the model based predictive control strategy used in this work, the chapter also proposes two methods for estimating value of grid impedance. The grid impedance has been estimated such that it is used in conjunction with the MPC approach, updating the controller every sampling time with the estimated value of the grid impedance. For grid-connected applications it is common to use LCL filters at the point of common coupling instead of the conventional L filters. For simplicity of the proposed predictive control model and estimation algorithms in this work, L filter is used at the input of the power converter. For further work of this project where LCL filters can be used, the predictive control model needs to be modified such that the parameters of LCL filters are included in the predictive equations. This would also require for LCL filter parameters to be included in the estimation algorithms.

Looking at figure 4.1 while converter filter inductance, L_c, and its parasitic resistance, r_C, are usually known, the grid resistance, r_s, and the grid inductance, L_s, are unknown with values that vary depending on grid load conditions at the point of connection of the converter to the grid. Several methods have been proposed in literature for estimation of the supply impedance, with both offline and online implementations as explained in chapter 2 that include using a Fast Fourier Transform (FFT) to calculate different harmonic impedances [100] by injecting a voltage transient at the PCC resulting in a transient variation in current and voltage at the PCC. Taking the current and voltage harmonics magnitudes at different frequencies, the grid harmonic impedance was calculated using Ohm's Law. However, as mentioned earlier the use of an online FFT algorithm requires a high computational effort. Other grid impedance estimation methods include variations of active and reactive power, [59], or use a Virtual-Flux based control method to estimate inductance, [61]. An analytic approach for estimation of the coupling inductance in direct power control of active rectifiers is also proposed in [4] and [103].

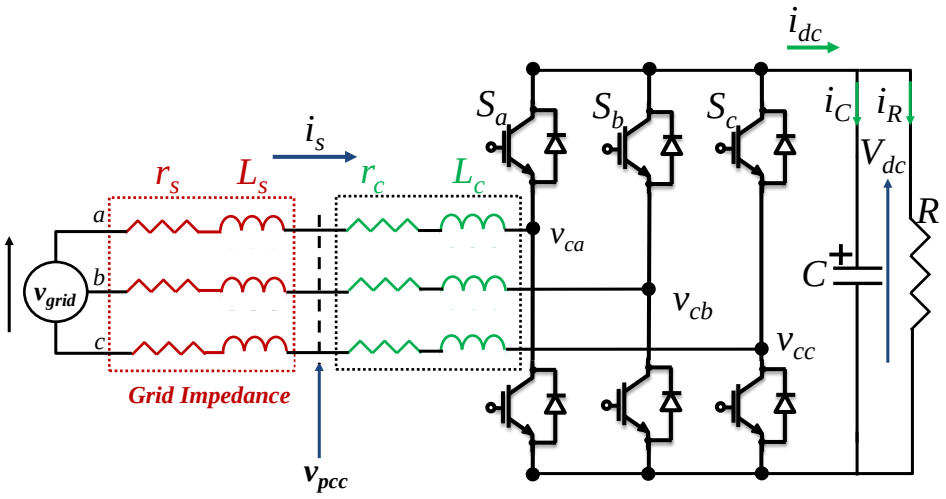


Figure 4.1: Grid-connected active front end (AFE) rectifier

Many argue that because the variation in the grid resistance and voltage drop across it is negligible as compared to the voltage drop across the inductance, therefore, for grid impedance estimation purposes grid resistance can be neglected. Hence, the grid impedance can be mainly inductive [3]. Using this phenomenon, the grid impedance estimation method proposed in this work focuses on estimation of the grid inductance. However, the estimation method can be expanded by including the grid resistance and an eventual capacitance terms as well. Though, inclusion of these parameters would make the algorithm more complex.

The proposed predictive control model together with grid impedance estimation methods has been implemented for a single converter connected to an equivalent model of a weak AC system. Moreover, the effect of grid resistance and grid capacitance are considered to have negligible effect thus estimation of these parameters are excluded from the estimation algorithms and predictive control. For expansion of the proposed methods, effect of more loads connected at the PCC, LCL filters and estimation of resistive and capacitive grid parameters can be taken into account. This would need modification of the predictive control model and estimation algorithms.

4.2. Model Based Predictive Direct Power Control

Model predictive control for grid connected converters can be implemented by means of two strategies: Model Predictive Current Control (MP-CC) and Model Predictive Direct Power Control (MP-DPC). MP-CC uses a Phase Locked Loop (PLL) for grid synchronization and regulates the grid voltage and current phase shift. Whereas, MP-DPC regulates the voltage and current phase shift by monitoring the power factor (PF) achieved by controlling the active and reactive powers directly. Therefore, for MP-

DPC, the use of a PLL for grid synchronization is avoided. Under low SCR values, the tuning of the PI controller used inside a PLL may get significantly affected, hence introducing an irregularity in grid synchronization. Therefore, MP-DPC presents suitable option since the knowledge of grid phase angle is not necessary for reference calculation and grid synchronization.

The MP-DPC uses the finite number of possible converter switching states to control the AFE rectifier. Since a 3-phase 2-level converter is used in this work, the total number of switching states are 8 (n^p =>2^3; n = number of levels, p = number of phases). The method used here controls the active power, reactive power and the dc-link voltage using predictions of the supply current and the dc-link voltage, respectively.

Referring to figure 4.1, the continuous-time representation of the AC-side at the PCC for each phase is expressed as:

$$v_{PCCa}(t) = i_{Sa}(t) * r_C + L_C * \frac{di_a(t)}{dt} + v_{Ca}(t) \tag{4.1}$$

$$v_{PCCb}(t) = i_{Sb}(t) * r_C + L_C * \frac{di_b(t)}{dt} + v_{Cb}(t) \tag{4.2}$$

$$v_{PCCc}(t) = i_{Sc}(t) * r_C + L_C * \frac{di_c(t)}{dt} + v_{Cc}(t) \tag{4.3}$$

Where, $v_{PCCa}(t)$, $v_{PCCb}(t)$, $v_{PCCc}(t)$ and $i_{Sa}(t)$, $i_{Sb}(t)$, $i_{Sc}(t)$ are the measured voltages and currents at the PCC and $v_{Ca}(t)$, $v_{Cb}(t)$, $v_{Cc}(t)$ are the converter input voltages. The terms r_c and L_c refer to the inductive and resistive parameters of the converter input filter.

Bringing the current derivatives to the left hand side of equations (4.1)-(4.3) for ease of discretizing the system model results in:

$$\frac{di_a(t)}{dt} = \frac{v_{PCCa}(t)}{L_C} - \frac{r_C}{L_C} * i_{Sa}(t) - \frac{v_{Ca}(t)}{L_C} \tag{4.4}$$

$$\frac{di_b(t)}{dt} = \frac{v_{PCCb}(t)}{L_C} - \frac{r_C}{L_C} * i_{Sb}(t) - \frac{v_{Cb}(t)}{L_C} \tag{4.5}$$

$$\frac{di_c(t)}{dt} = \frac{v_{PCCc}(t)}{L_C} - \frac{r_C}{L_C} * i_{Sc}(t) - \frac{v_{Cc}(t)}{L_C} \tag{4.6}$$

Similarly, the continuous-time representation for the DC-side of the converter in figure 4.1 is expressed as

$$i_{dc}(t) = i_C(t) + i_R(t) \tag{4.7}$$

Where, $i_{dc}(t)$ is the output dc current of the converter calculated from the supply currents from the AC side and the converter switching vectors, $i_C(t)$ is the current flowing through the capacitor and $i_R(t)$ is the current flowing through the load resistor. Solving (4.7),

$$i_{dc}(t) = C * \frac{dV_{dc}(t)}{dt} + \frac{V_{dc}(t)}{R} \tag{4.8}$$

$$\frac{dV_{dc}(t)}{dt} = \frac{i_{dc}(t)}{C} - \frac{V_{dc}(t)}{R * C} \tag{4.9}$$

Where, $V_{dc}(t)$ is the measured dc-link voltage and the terms R, C are the load resistor and dc-link capacitor respectively.

4.2.1. Current Predictions

Since the predictive control works in discrete-time, using the Euler forward approximation method [74], the current derivatives for each phase model, (4.4)-(4.6), and the dc-link voltage derivative, (4.9), are hence approximated to obtain the current and dc-link voltage predictions at the future instant, *k+1*. So, solving (4.4)-(4.6) for current predictions by approximating current derivative as

$$\frac{di_x}{dt} = \frac{{i_{Sx}}^{k+1} - {i_{Sx}}^{k}}{t_s} \qquad ; \qquad x \in \{a, b, c\}$$

Therefore:

$${i_{Sa}}^{k+1} = \boldsymbol{K_1} * ({v_{PCCa}}^{k} - {v_{Ca}}^{k}) + \boldsymbol{K_2} * {i_{Sa}}^{k} \tag{4.10}$$

$${i_{Sb}}^{k+1} = \boldsymbol{K_1} * ({v_{PCCb}}^{k} - {v_{Cb}}^{k}) + \boldsymbol{K_2} * {i_{Sb}}^{k} \tag{4.11}$$

$${i_{Sc}}^{k+1} = \boldsymbol{K_1} * ({v_{PCCc}}^{k} - {v_{Cc}}^{k}) + \boldsymbol{K_2} * {i_{Sc}}^{k} \tag{4.12}$$

Where,

$$\boldsymbol{K_1} = \frac{t_s}{L_C}; \qquad \boldsymbol{K_2} = \left(1 - \frac{r_C * t_s}{L_C}\right)$$

$$t_s = sampling\ time\ between\ two\ consecutive\ instants$$

$$\begin{Bmatrix} {i_{Sa}}^{k} \\ {i_{Sb}}^{k} \\ {i_{Sc}}^{k} \end{Bmatrix} = Current\ measurements\ at\ present\ instant\ k$$

$$\begin{Bmatrix} {i_{Sa}}^{k+1} \\ {i_{Sb}}^{k+1} \\ {i_{Sc}}^{k+1} \end{Bmatrix} = Current\ predictions\ at\ future\ instant\ k+1$$

$$\begin{Bmatrix} {v_{PCCa}}^{k} \\ {v_{PCCb}}^{k} \\ {v_{PCCc}}^{k} \end{Bmatrix} = PCC\ Voltage\ at\ present\ instant\ k$$

$$\begin{Bmatrix} {v_{Ca}}^{k} \\ {v_{Cb}}^{k} \\ {v_{Cc}}^{k} \end{Bmatrix} = Converter\ input\ voltage\ at\ present\ instant\ k$$

Past, *present* and one-sample ahead (*future*) instants are as shown in figure 4.2:

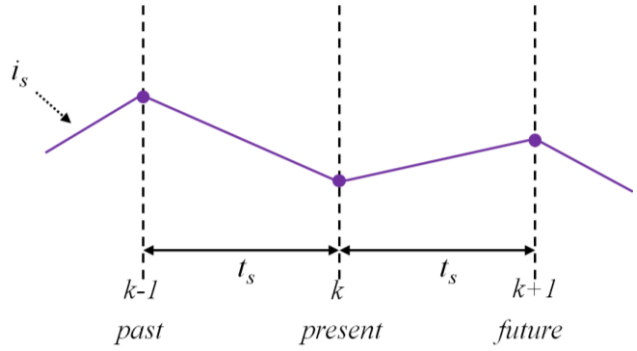


Figure 4.2: Past, Present and Future (Prediction) sample instants

4.2.2. Converter voltage calculations

Figure 4.3 shows the voltage source converter which implements our active front end (AFE).

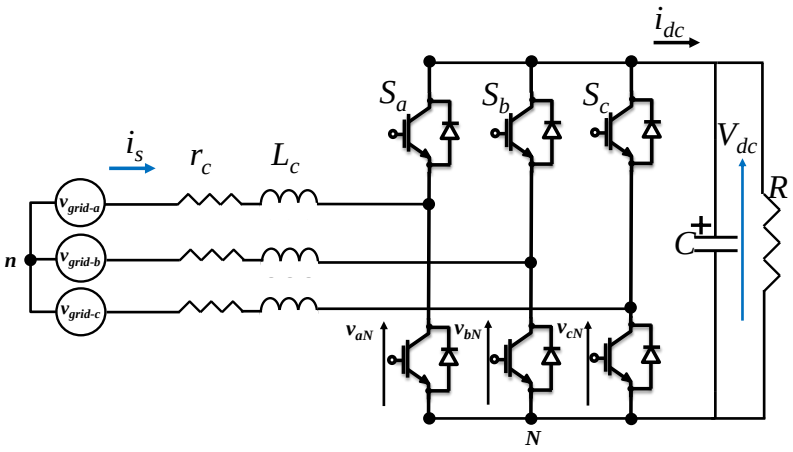


Figure 4.3: Three phase two-level voltage source converter

With reference to figure 4.3, the quantities S_a, S_b and S_c represent the converter switching functions and can be defined based on the status of each converter leg, respectively. When the top switch of each converter leg is turned ON (the low one is OFF) the switching function has a value of 1, otherwise it is zero. These switches operate in a complementary way such that the two switches in one leg cannot be turned ON or OFF at the same time as it would result in a short-circuit of the supply. S_a, S_b and S_c are used to calculate the converter voltages with respect to the dc-link voltage, V_{dc} that acts across the switch as:

$$v_{CaN} = S_a V_{dc} \qquad v_{CbN} = S_b V_{dc} \qquad v_{CcN} = S_c V_{dc} \tag{4.13}$$

In order to take into account the 120° phase displacement between the three phases, the converter voltage vector is referred as [74], [105]:

$$\boldsymbol{v_C} = \frac{2}{3}(v_{CaN} + \mathbf{a} v_{CbN} + \mathbf{a}^2 v_{CcN}) \tag{4.14}$$

Where, **a** is the 120° phase displacement term $\mathbf{a} = e^{j\left(\frac{2\pi}{3}\right)}$. Substituting (4.13) in (4.14) gives:

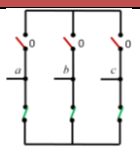
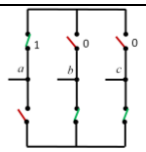
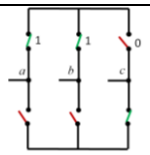
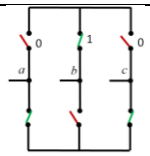
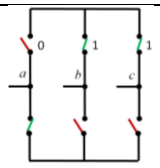
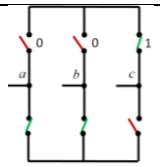
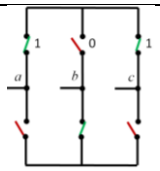
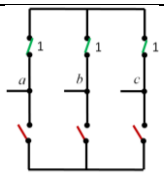
$$\boldsymbol{v_C} = \frac{2}{3}(S_a V_{dc} + \mathbf{a}\, S_b V_{dc} + \mathbf{a}^2\, S_c V_{dc}) \tag{4.15}$$

The expression $\mathbf{a} = e^{j\left(\frac{2\pi}{3}\right)}$ can be expanded as $\mathbf{a} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$. For the chosen 3-phase 2-level converter topology, the 8 switching combinations generate converter voltages as explained in table 4.1 for figure 4.3. Table 4.1 shows the phase to converter neutral (N) voltages represented in (4.13) and converter voltage vector with respect to the ac-side neutral point, *n*, represented in (4.15) in its complex notation (as used in the predictive

controller) as further explained in [74]. The term S in table 4.1 represents the state of the converter and is described as:

$S = \{S_a, S_b, S_c\}$ ➔ {0 0 0}, {1 0 0}, {1 1 0}, {0 1 0}, {0 1 1}, {0 0 1}, {1 0 1}, {1 1 1}

TABLE 4.1. CONVERTER VOLTAGE LEVELS

	S	v_c
0		0
1		$\frac{2V_{dc}}{3}$
2		$V_{dc}\left(\frac{1}{3}+j\frac{\sqrt{3}}{3}\right)$
3		$V_{dc}\left(-\frac{1}{3}+j\frac{\sqrt{3}}{3}\right)$
4		$-\frac{2V_{dc}}{3}$
5		$V_{dc}\left(-\frac{1}{3}-j\frac{\sqrt{3}}{3}\right)$
6		$V_{dc}\left(\frac{1}{3}-j\frac{\sqrt{3}}{3}\right)$
7		0

4.2.3. DC-Link Voltage Prediction

Similarly, the dc-link voltage is predicted as:

$$V_{dc}{}^{k+1} = \boldsymbol{K_3} * \left(i_{dc}{}^{k}\right) + \boldsymbol{K_4} * V_{dc}{}^{k} \tag{4.16}$$

Where,

$$\boldsymbol{K_3} = \frac{t_s}{C}; \qquad \boldsymbol{K_4} = \left(1 - \frac{t_s}{R * C}\right)$$

$i_{dc}{}^{k} = converter\ output\ current\ at\ instant\ k$

$V_{dc}{}^{k} = DC - link\ voltage\ measurement\ at\ instant\ k$

$V_{dc}{}^{k+1} = DC - link\ voltage\ prediction\ at\ future\ instant\ k+1$

$i_{dc}{}^{k}$ is calculated using the supply currents and the switching combinations used for converter operation as:

$$i_{dc}{}^{k} = i_{Sa}{}^{k} * S_a + i_{Sb}{}^{k} * S_b + i_{Sc}{}^{k} * S_c \tag{4.17}$$

In case the load resistance, *R*, changes it may have an influence on the control performance as the actual value and model value will be different. In order to take the variation of *R* into account it is advisable to have an estimation algorithm that can estimate the *R* value in real-time and thus update the predictive model with the estimated *R* value. For algorithm simplification, the AC-side of the grid connected converter in figure 4.1 is transformed into its *α-β* equivalent circuit, shown in figure 4.4 using the Clarke's transformation reported in the Appendix C [55].

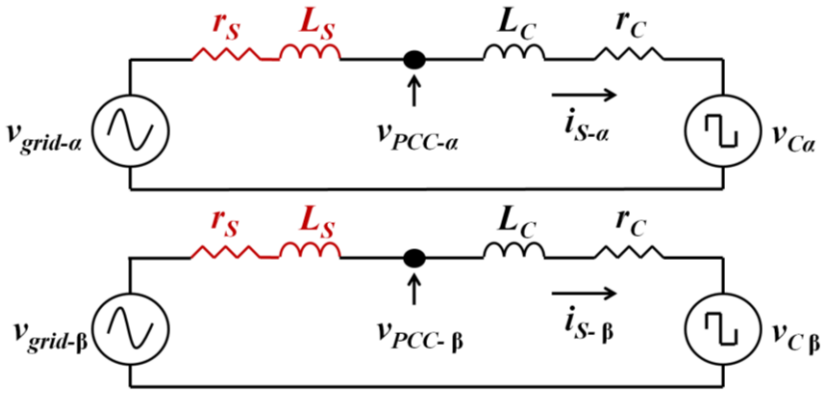


Figure 4.4: Equivalent AFE model in α-β reference frame

Thus, the current predictions, (4.10)-(4.12), in a-b-c representation are transformed to *α-β* as

$$i_{S\alpha}{}^{k+1} = \boldsymbol{K_1} * (v_{PCC\alpha}{}^{k} - v_{C\alpha}{}^{k}) + \boldsymbol{K_2} * i_{S\alpha}{}^{k} \tag{4.18}$$

$$i_{S\beta}{}^{k+1} = \boldsymbol{K_1} * \left(v_{PCC\beta}{}^{k} - v_{C\beta}{}^{k}\right) + \boldsymbol{K_2} * i_{S\beta}{}^{k} \tag{4.19}$$

The converter output current, $i_{dc}{}^{k}$, is modified as:

$$i_{dc}{}^{k} = i_{S\alpha}{}^{k} * S_\alpha + i_{S\beta}{}^{k} * S_\beta \tag{4.20}$$

Where, S_α and S_β are also calculated using the Clarke's transformation [55].

4.2.4. Two sample-ahead prediction

For predictive control algorithm it becomes of utmost importance that the delays introduced due to control algorithm calculations in the practical system implementation must be compensated. This is carried out such that instead of making one sample-ahead prediction at *k+1*, two sample-ahead predictions are carried out. In other words, predictions at instant *k+2* are carried out for cost-function optimization, as depicted in figure 4.5.

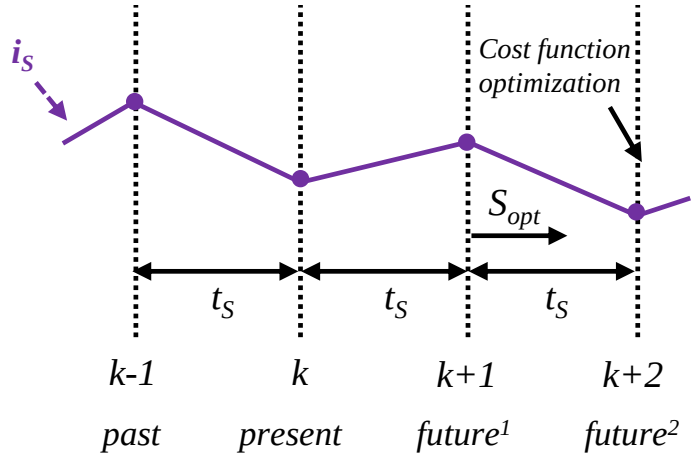


Figure 4.5: Past, Present, future[1] and future[2] sampling instants

In figure 4.5, measurements of voltages and currents for the MP-DPC are taken at the *present* instant *k*. At *future*[1] instant *k+1*, the predictions of the control variable for one-sample ahead instant are calculated using the optimum switching signal calculated through minimization (optimization) of the cost-function. To compensate for the delay caused by calculation times, using the possible switching combinations as explained in table 4.1 the predictions at two-sample instants ahead *k+2*, referred as *future*[2] in figure 4.5, are calculated that relies on information achieved from instants *k+1* and *k*. At the instant *k+2*, the difference between the control variable predictions and their reference values are optimized to generate the optimum switching signal. In this work the supply currents are predicted at instant *k+2*, as shown in (4.21) and (4.22), to calculate active and reactive power predictions at instant *k+2* for cost-function optimization.

$$i_{S\alpha-i}{}^{k+2} = \boldsymbol{K_1} * \left(V_{PCC\alpha}{}^{k+1} - V_{C\alpha}{}^{k+1}\right) + \boldsymbol{K_2} * i_{S\alpha}{}^{k+1} \tag{4.21}$$

$$i_{S\beta-i}{}^{k+2} = \boldsymbol{K_1} * \left(V_{PCC\beta}{}^{k+1} - V_{C\beta}{}^{k+1}\right) + \boldsymbol{K_2} * i_{S\beta}{}^{k+1} \tag{4.22}$$

Where, *i = {0, 1, 2, 3, 4, 5, 6, 7} – eight switching combinations*

$$\begin{Bmatrix} {i_{S\alpha}}^{k+1} \\ {i_{S\beta}}^{k+1} \end{Bmatrix} = Current\ predictions\ at\ future^1\ instant\ using\ S_{opt.}$$

$$\begin{Bmatrix} {V_{C\alpha}}^{k+1} \\ {V_{C\beta}}^{k+1} \end{Bmatrix} = Converter\ input\ voltage\ at\ future^1\ using\ table\ 4.1$$

$$\begin{Bmatrix} {V_{PCC\alpha}}^{k+1} \\ {V_{PCC\beta}}^{k+1} \end{Bmatrix} = PCC\ voltage\ at\ future^1$$

$$\begin{Bmatrix} {i_{S\alpha}}^{k+2} \\ {i_{S\beta}}^{k+2} \end{Bmatrix} = Current\ predictions\ at\ future^2\ \ using\ table\ 4.1$$

Similarly, for the dc-link voltage predictions for the same number of switching combinations as explained in table 4.1 is calculated as:

$${V_{dc-pred-i}}^{k+2} = \boldsymbol{K_3} * \left({i_{dc}}^{k+1}\right) + \boldsymbol{K_4} * {V_{dc}}^{k+1} \quad (4.23)$$

Where,

${V_{dc}}^{k+1} = DC - link\ voltage\ prediction\ at\ future^1$

${i_{dc}}^{k+1} = DC - side\ current\ at\ future^1\ using\ table\ 4.1$

${V_{dc-pred-i}}^{k+2} = DC - link\ voltage\ prediction\ at\ future^2\ using\ table\ 4.1$

4.2.5. Active and Reactive Power Predictions

Using the supply current predictions at the instant *k+2*, the active and reactive power predictions at the same instant are calculated as shown in (4.25) and (4.25) for cost-function optimization.

$${P_{pred-i}}^{k+2} = \left(V_{PCC\alpha} * {i_{S\alpha-i}}^{k+2} + V_{PCC\beta} * {i_{S\beta-i}}^{k+2}\right) * 1.5 \quad (4.24)$$

$${Q_{pred-i}}^{k+2} = \left(V_{PCC\beta} * {i_{S\alpha-i}}^{k+2} - V_{PCC\alpha} * {i_{S\beta-i}}^{k+2}\right) * 1.5 \quad (4.25)$$

Where, $P_{pred-i}{}^{k+2}$ represents the active power predictions for the eight switching combinations, $Q_{pred-i}{}^{k+2}$ represents the reactive power predictions for the eight combinations and the subscript *i* represents the eight switching vectors (refer to Table 4.1).

4.2.6. DC-Link voltage reference calculation

For dc-link voltage reference, the first point to notice is that the capacitor voltage (dc-link voltage) can be adjusted by the capacitor current, i_C, referred in figure 4.1. Since i_C cannot be made arbitrarily large, a reference prediction horizon, N^*, is introduced to have a better dynamic response of the dc-link voltage. The significance of N^* for the dc-link voltage reference calculation is explained in figure 4.6. Considering that the dc-link capacitor value remains constant, if the capacitor current increases, the rate of change of voltage across the capacitor would increase as well. This increase in voltage over a time period can damage the capacitor; hence, a limit needs to be put on the capacitor current. (4.26) shows the current through the capacitor:

$$i_C(t) = C\frac{dV_{dc}(t)}{dt} \tag{4.26}$$

Where, *C* is the dc-link capacitor, V_{dc} represents the dc-link voltage and *dt* represents the time between two consecutive dc-link voltage samples. The dc-link voltage reference at *future*[1] instant *k+1* is, therefore, calculated as

$$V_{dc-ref}{}^{k+1} = V_{dc}{}^{k} + \frac{1}{N^*}\left(V_{dc-ref}{}^{k} - V_{dc}{}^{k}\right) \tag{4.27}$$

Where, $V_{dc\text{-}ref}^{k+1}$ is the dc-link voltage reference, V_{dc}^{k} is the measured dc-link voltage at the *present* instant *k* and $V_{dc\text{-}ref}^{k}$ is the reference for the dc-link voltage at the *present* instant *k*. Since the dc-link voltage reference does not change significantly between two consecutive sampling instants, it is safe to say that

$$V_{dc-ref}^{k+2} \sim V_{dc-ref}^{k+1}$$

for use in optimization of the cost-function [35]. The reference prediction horizon, *N**, serves to trade-off the response time versus the control effort by putting a limitation on the total increment in the capacitor current, i_C. For a faster tracking response of the dc-link voltage, the *N** is set to a small value and for a slower tracking response of the dc-link voltage, the *N** is set to a larger value as seen in figure 4.6 and simulation results shown in chapter 5. Moreover, *N** serves to make dynamics of the voltage slower than the current.

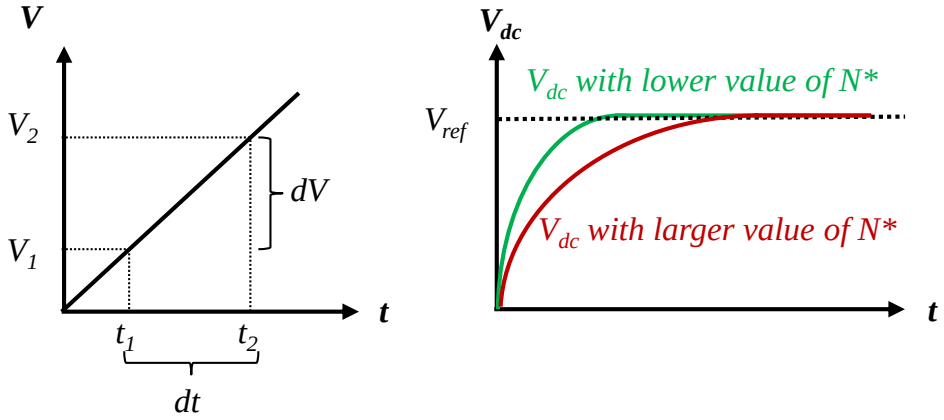


*Figure 4.6: Simplified explanation on importance of N**

This approach generates reference for the dc-link voltage (4.27). The advantages of generating the dc-link voltage reference using this approach are [35]:

- No need for external PI controller to obtain active power reference and control of the dc-link voltage
- High effectiveness to a step change in the control system
- Better dynamics, as depicted in figure 4.6 and simulation results in chapter 5.

4.2.7. Active and Reactive Power reference calculation

The active power reference is calculated using the dc-link voltage reference, the rectifier dc-side current calculated using voltage and current at the PCC and the measured dc-link voltage. The active power reference calculation is based on the following relation of the input power to the output power:

$$P_S = P_r + P_{LOAD} \tag{4.28}$$

Where, P_S is the three phase supply power, P_r corresponds to the power loss across the converter input filter resistor and P_{LOAD} refers to the power loss across the capacitor and resistor at the dc-side. If we neglect the converter switching losses, it can be said that the power at the input of the converter (P_O) is equal to the power at the load (P_{Load}). An equivalent representation of the three phase active front end is shown in figure 4.7.

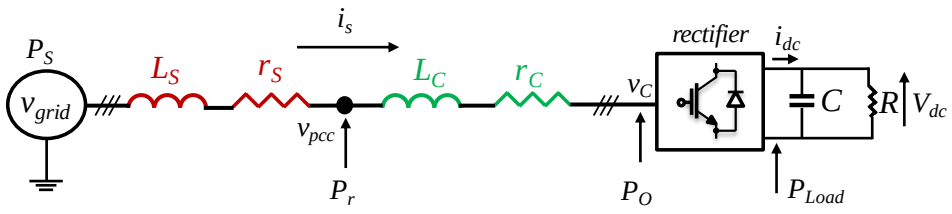


Figure 4.7: Equivalent representation of a 3-phase Active Front End

The following sets of equations explain the derivation for the total active power reference.

$$P_S = 3 * \frac{v_{pcc}}{\sqrt{2}} * \frac{i_s}{\sqrt{2}} = \frac{3}{2} * v_{pcc} * i_s \tag{4.29}$$

$$P_r = 3 * \left(\frac{i_s}{\sqrt{2}}\right)^2 * r = \frac{3}{2} * {i_s}^2 * r \tag{4.30}$$

$${P_{load}}^{k+1} = {i_{dc-ref}}^{k+1} * {V_{dc-ref}}^{k+1} \tag{4.31}$$

Where,

$${i_{dc-ref}}^{k+1} = C\frac{\left({V_{dc-ref}}^{k+1} - {V_{dc}}^{k}\right)}{t_s} + \frac{{V_{dc}}^{k}}{R} \tag{4.32}$$

Therefore, substituting (4.29)-(4.31) in (4.28) to solve for the supply current i_s:

$$\frac{3}{2} * v_{pcc} * i_s = \frac{3}{2} * {i_s}^2 * r \ + P_{load} \tag{4.33}$$

Re-arranging (4.33):

$$\frac{3}{2} * {i_s}^2 * r - \frac{3}{2} * v_{pcc} * i_s + P_{LOAD} = 0 \tag{4.34}$$

$${i_s}^2 - \frac{v_{pcc}}{r} * i_s + \frac{2}{3} * \frac{P_{LOAD}}{r} = 0 \tag{4.35}$$

(4.35) above is solved using the quadratic expression in (4.37)

$$a * x^2 + b * x + c = 0 \tag{4.36}$$

Where, solving for x:

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{4.37}$$

Hence, solving (4.35) in the same manner as (4.36) and (4.37), i_s is equated as:

$$i_s = \frac{1}{2}\left(\left(\frac{v_{pcc}}{r}\right) \pm \sqrt{\left(\frac{v_{pcc}}{r}\right)^2 - 4 * \frac{2}{3} * \frac{P_{load}}{r}}\right) \tag{4.38}$$

$$i_s = \frac{1}{2} * \left(\frac{v_{pcc}}{r}\right)\left(1 - \sqrt{1 - \frac{8}{3} * \frac{P_{load} * r}{v_{pcc}^2}}\right) \tag{4.39}$$

Referring to (4.29), the active power reference is thus equated as:

$$P_{ref} = \frac{3}{2} * v_{pcc} * i_s \tag{4.40}$$

Substituting (4.39) into (4.40),

$$P_{ref} = \frac{3}{2} * v_{pcc} * \frac{1}{2} * \left(\frac{v_{pcc}}{r}\right)\left(1 - \sqrt{1 - \frac{8}{3} * \frac{P_{load} * r}{v_{pcc}^2}}\right) \tag{4.41}$$

Where, v_{pcc} and i_s signify the voltage and supply current, respectively. So, the active power reference in discrete form at the *future*[2] instant *k+2* is expressed in (4.42) as

$$P_{ref} = \frac{3}{4} * \frac{{V_s}^{k+1^2}}{r}\left(1 - \sqrt{1 - \frac{8}{3} * \frac{{P_{load}}^{k+1} * r}{{V_s}^{k+1^2}}}\right) \tag{4.42}$$

The active power reference in (4.42) is used in optimization of the cost-function with each of the eight active power predictions.

The reactive power reference, ${Q_{ref}}^{k+2}$ on the other hand is set quite simply by just setting the desired value. To achieve a unity power factor, as explained in vectorial representation in chapter 2, the reference is set to 0VAR. However, if the reactive power reference is set to a positive value, the source current will lag the source voltage

by a certain phase angle and similarly if the reactive power reference is set to a negative value, the source current will lead the source voltage by a certain phase shift as will be shown in the simulation and experimental results chapters.

To summarize, the dc-link voltage reference, active and reactive power references are used together for cost function optimization at *future*^{2} instant *k+2* for each of the eight switching combinations used to generate their respective predictions. Next section describes the cost function optimization used in the predictive direct power control strategy.

4.2.8. Cost-function optimization

The predictive controller used in this work utilizes the prediction models for the dc-link voltage, active power and reactive powers along with their respective references to choose a switching signal to be sent to the converter switches. At each sampling interval, the eight possible switching combinations (6 active vectors and 2 zero vectors) are used to evaluate the cost function, thus making the control approach fast. Out of the 8 switching combinations the one that gives the minimum value between the reference and the predictions is selected and hence applied as the optimum switching signal S_{opt} (refer to figure 4.5). Though an advantage of using this approach lies in the fact that the use of a modulation strategy to generate the converter switching states is no longer required, however it results in a variable switching frequency.

The cost function, *G*, used for the model predictive direct power control in this work is, hence, described as:

$$G(i) = \frac{\lambda_1}{{V_{dc-rated}}^2}\left({V_{dc-ref}}^{k+2} - {V_{dc-pred}}^{k+2}(i)\right)^2 + \frac{\lambda_2}{{P_{rated}}^2}\left({P_{ref}}^{k+2} - {P_{pred}}^{k+2}(i)\right)^2 + \frac{\lambda_3}{{P_{rated}}^2}\left({Q_{ref}}^{k+2} - {Q_{pred}}^{k+2}(i)\right)^2 \quad (4.43)$$

Where, i, λ_1, λ_2 and λ_3 are the switching states and weighting factors for the three terms in the cost function that have the values 1.5, 1.0 and 1.0 respectively. In [74], the authors emphasize that special attention must be paid while designing the weighting factors; however, there is not a straightforward approach through which an accurate value for these parameters can be selected. Since the weighting factors selection is an on-going research topic, mostly their values are designed based on empirical procedures. However, some methods developed that provide auto-tuning of weighting factors for multi-variable cost-function with different weighting factors include using a Genetic Algorithm (GA) multi-objective optimization approach [115], while authors in [116] provide guidelines on selection of weighting factors based on analytical and empirical methods when applied on different power converters. $V_{dc\text{-}rated}$ and P_{rated} are the normalizing factors since three different variables are used in the cost function.

The cost-function optimization using eight predictions is depicted in figure 4.8 for the active power predictions only. Same procedure is carried out for the reactive power and the dc-link voltage predictions.

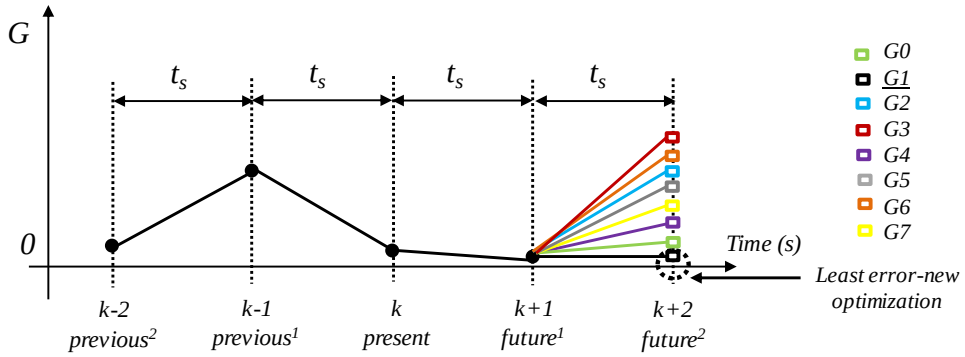


Figure 4.8: Active Power Predictions for the eight switching combinations and its reference

In figure 4.8, *G0* to *G7* depict the cost-functions for the eight switching combinations. Since the cost-function optimization is calculated at *future*^{2}, prediction value that gives the least error value at that instant gets selected. Therefore in figure 4.8, the switching combination *[1 0 0]* used for *G1* would be selected to be applied at the *present* instant to drive the IGBTs in order to achieve minimum error in *k+2*.

The cost function in (4.43) highlights an important feature of the predictive control technique, as mentioned in chapter 3, that it offers a multivariable control using a single control loop. In (4.43), it can be seen that without using any additional PI controllers or modulation strategies, three different variables, i.e. dc-link voltage, active power and reactive power, are being controlled within one equation/function. Thus, providing a much flexible, straightforward and compact control structure. Simulation results in chapter 5 show the results for optimization of the cost function and selection of the optimized switching vector for the converter switches.

Figure 4.9 shows the complete block diagram representation of the model based predictive direct power control.

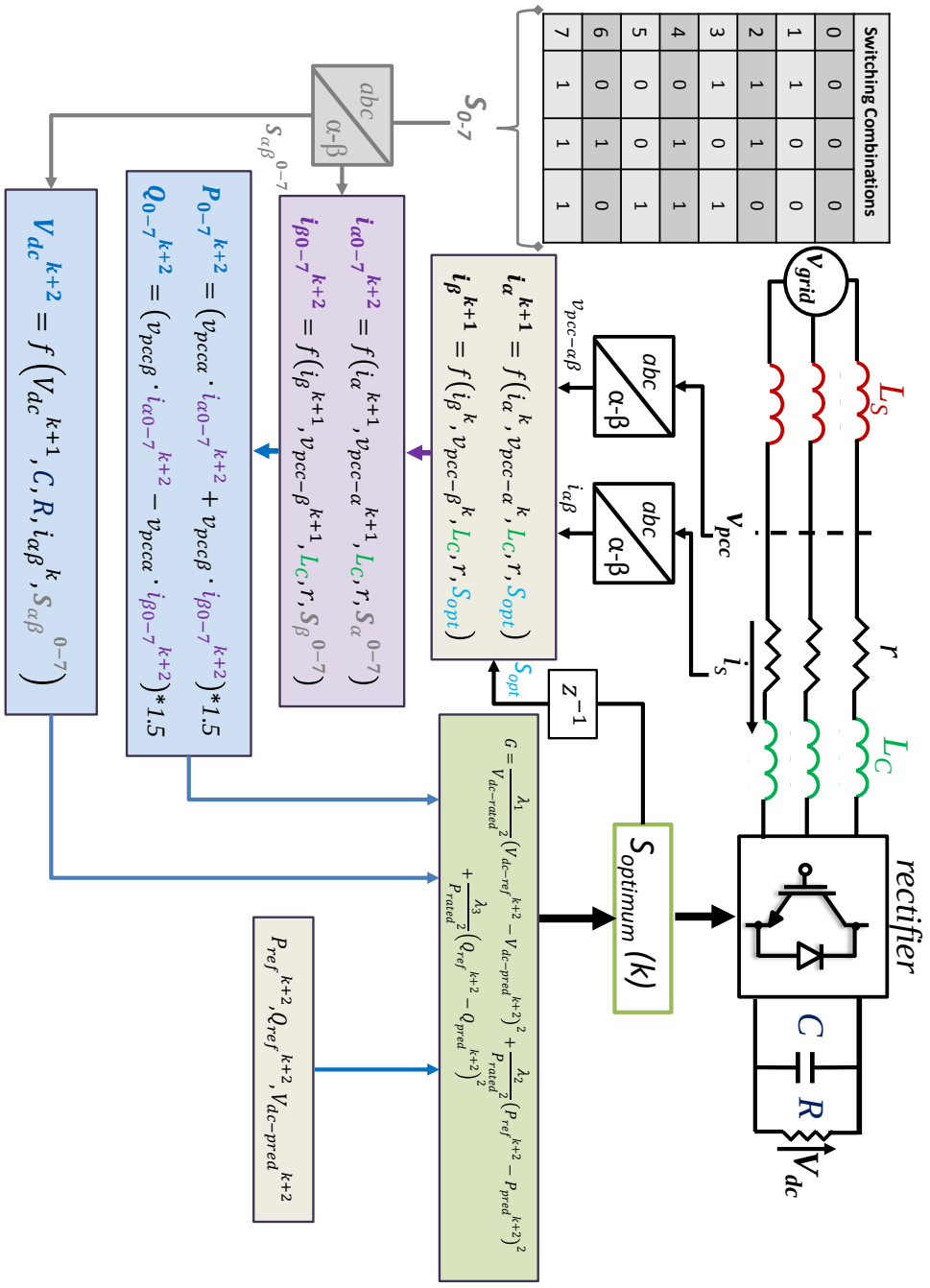


Figure 4.9: Block Diagram of the MP-DPC

4.3. Dead-time Compensation

For the switches used in the converter, like in all power electronics systems, a small delay time is introduced between the two switches in one leg referred as dead-time. Dead-time means that there must be a time delay between the turning OFF and turning ON of the upper and lower switches in each leg of a converter, as shown in figure 4.10 for one leg of the converter. This is done so as to give time to the stored charge in an IGBT (S_a) to disappear before the other device (S_a') is turned ON. If the dead-time is not present, S_a is still able to conduct current even when S_a' turns ON. This results in a short circuit across the dc-link and a failure of the converter leg [48].

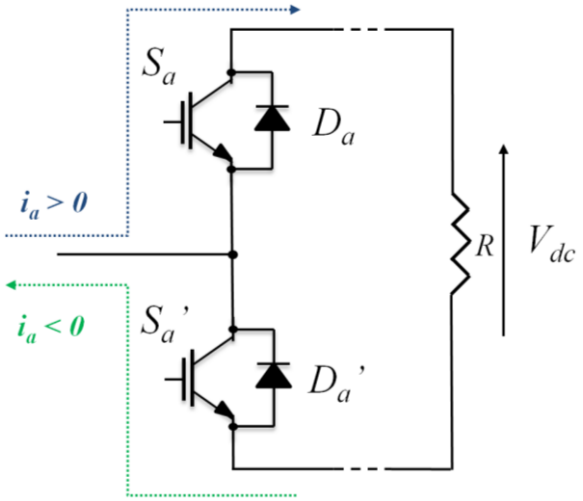


Figure 4.10: Basic Configuration of one leg of three phase AFE during dead-time

Figure 4.11 shows the *Ideal* and *Real* switching patterns for S_a and S_a' for four consecutive sampling intervals, where *k* refers to the *present* sampling instant and *k-2*, *k -1*, k+*1* and *k+2* refer to the past and future sampling instants, respectively. The dead-time is clearly noticeable in the figure and this of course gives protection to the converter leg; however, a small voltage drop due to this dead-time also occurs. If this voltage drop is not compensated, it can considerably affect the control performance.

Moreover, if the converter is being operated at low voltage the ratio of voltage drop in converter leg to the applied voltage would be high as compared to the case if the converter is being operated at a higher voltage where this ratio would be smaller.

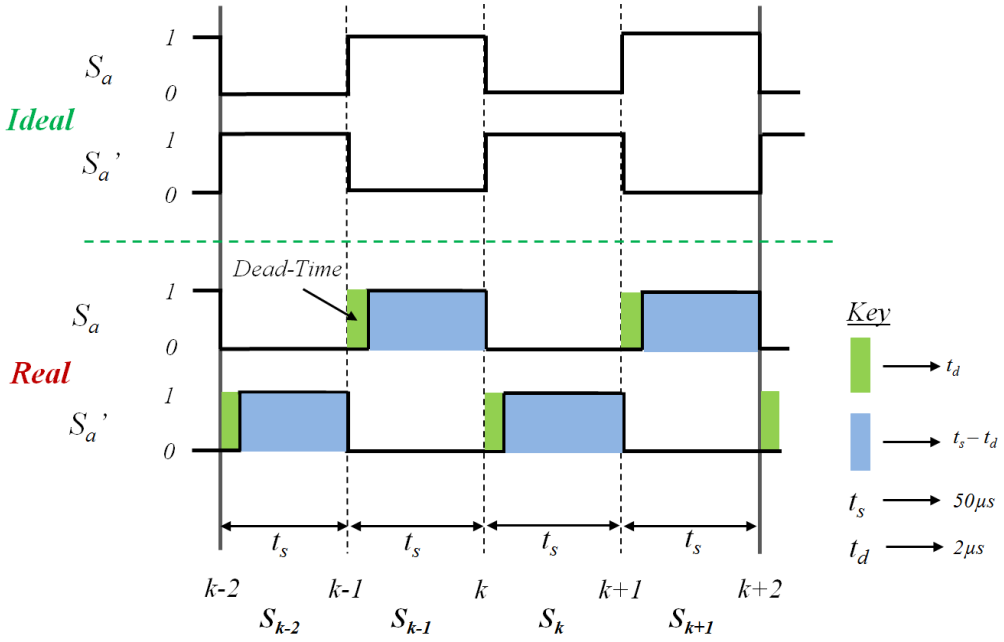


Figure 4.11: Dead-time in upper and lower switch of leg-A in a 3-phase 2-level AFE

There are several methods used to compensate the voltage drop due to dead-time, [49]–[51]. Amongst those, the most popular method calculates the average converter voltages according to the direction of the respective supply currents in each leg and conductivity of the switches in the respective legs [49]. With respect to figure 4.10 and figure 4.11 (between interval *k-2* and *k*), the switching pattern is explained below when the current in the leg is greater than or lesser than zero:

1. *Interval k-2 to k-1*

   If S_a is OFF and the direction of current is positive, then during dead-time D_a conducts until S_a' turns ON and keeps conducting till *k-1*.

2. *Interval k-1 to k*

   If S_a' is OFF and the direction of current is positive, then during dead-time D_a conducts and keeps conducting till *k*.

3. *Interval k-2 to k-1*

   If S_a is OFF and the direction of current is negative, then during dead-time D_a' conducts and keeps conducting till *k-1*.

4. *Interval k-1 to k*

   If S_a' is OFF and the direction of current is negative, then during dead-time D_a' conducts until S_a turns ON and keeps conducting till *k*.

Dead-time compensation becomes all the more significant for our approach since the proposed inductance estimation methods takes into account the converter voltages at two consecutive sampling instants. If not compensated, the converter voltage drop introduces a significant distortion to the estimation methods, thus affecting the control performance as well. The compensation method has been explained in section 4.3.1 with regards to its use for the grid impedance estimation method. Effect of voltage drop due to dead-time has been shown with the help of simulation results in chapter 5.

4.3.1. Methodology

A dead-time compensation method, as proposed in [49], has been included in the model predictive control by incorporating an additive term representing the voltage drop due to the dead time t_d (2µs) for calculation of the converter voltages in one sample period. The voltage loss in the t_d region for interval *k-1* to *k* (figure 4.11) for leg A of the converter (figure 4.10) is expressed as

$$v_{Ca-td} = \frac{1}{3} * Vdc * \frac{t_d}{t_s} * \left(2{S_a}^{k-2} - {S_b}^{k-2} - {S_c}^{k-2}\right) \quad (4.44)$$

And the voltage in the $t_s - t_d$ region for interval *k-1* to *k* is expressed as

$$v_{Ca-ts-td} = \frac{1}{3} * Vdc * \frac{t_s - t_d}{t_s} \cdot \left(2{S_a}^{k-1} - {S_b}^{k-1} - {S_c}^{k-1}\right) \quad (4.45)$$

Therefore, the total voltage for the sample interval *k-1* to *k* is now expressed as

$${v_{Ca}}^{S_{k-1}} = v_{Ca-td} + v_{Ca-ts-td} \quad (4.46)$$

Similarly, (4.44) – (4.46) are applied for the other legs with reference to the direction of the supply currents in the respective legs. The converter voltages are later transformed to their respective α and β components to be used in the current predictions, at instants *k+1* and *k+2*, and in the inductance estimation methods explained in the next section.

4.4. Grid Impedance Estimation Algorithm

4.4.1. Background

This project focuses on model based predictive control performance of a grid connected converter. Due to sensitivity of the predictive control to model mismatches, the control performance of such converters may get largely affected by variations in the grid impedance, especially for systems with a low SCR value. In figure 4.1, while the converter inductance, L_C, and its parasitic resistance, r_C, are usually known, the grid inductance, L_S, and grid resistance, r_S, are unknown and can have highly varying values depending on the grid load conditions. Since MP-DPC is based on the knowledge of model parameters, any small variations in these parameters will disturb performance and stability of the control system.

Variation of transmission line inductance is very common and is due to [67]:

- environmental changes
- long distance transmission cables or
- Presence of harmonics generated by non-linear loads.

This variation in grid impedance also affects the ripple on the measured voltage at the PCC. A mismatched impedance value alongside a distorted PCC voltage, can affect the predictive control performance immensely. Thus, it is important that the variation in grid impedance, mostly inductive, is taken into account in the control implementation. Also, it would be a great advantage if a good online estimation of the supply inductance, L_S, is provided, using that to update the total AC side impedance value in MP-DPC.

There are two grid inductance estimation methods proposed in this work. Method 1, as explained in section 4.4.2, works on the principle of assuming an equal grid voltage magnitude at two consecutive sampling instants [4], and it is integrated within the MP-DPC algorithm. The supply resistance is not considered in this work since its effect can be considered negligible with respect to the supply inductance which heavily affects the magnitude and phase of the grid voltage, thus reducing the performance of predictive control. However, it is always possible to expand the proposed estimation method to include the supply resistance estimation.

Method 2 on the other hand, as explained in section 4.4.3, estimates the variation in grid inductance such that it uses the model based predictive algorithm to estimate the grid currents for different values of grid inductance and, between these values, selects the desired grid inductance estimation as the one which minimizes the error between

the estimated and measured current. The predictive controller is updated in real-time with the latest variation in grid inductance value.

The combination of a finite set MP-DPC and the proposed estimation algorithm results in a high-bandwidth control robust to supply impedance variations without increasing excessively the complexity of the control system. The next sections explain in detail the derivation of the grid inductance estimation algorithms.

4.4.2. Inductance Estimation Algorithm – Method 1

4.4.2.1. Working Principle

The estimation method proposed in this work estimates the total inductance, i.e. grid inductance plus converter inductance, and feeds the estimated value as an update to the model based predictive controller.

Using the total estimated inductance value, referred as $\hat{L}_{EST}$, we can easily find the variation in grid inductance, L_S, and make an estimation of the grid voltage inside the controller, as explained later in section 4.4.2.2.

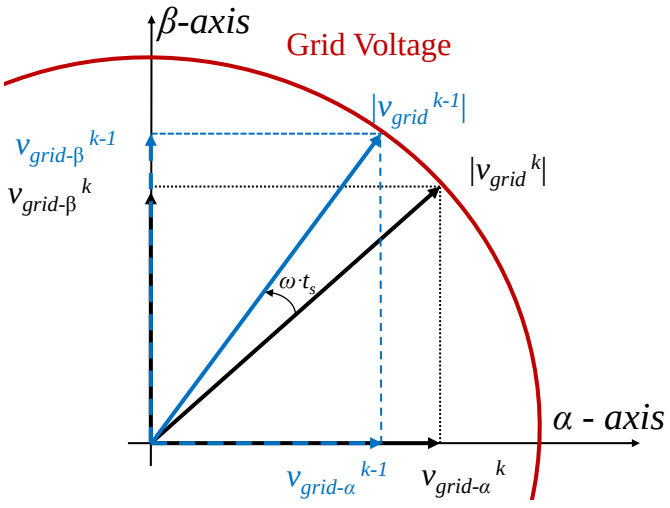


Figure 4.12: Grid voltage representation in α-β

Figure 4.12 presents an equivalent constant grid voltage magnitude representation between two consecutive sampling instants. Although there will be a phase shift of '$\omega \cdot t_s$,' the magnitude of the grid voltage vector will, however, not vary significantly. In *α-β* reference frame, the square of the grid voltage magnitude for instants *k* and *k-1* are expressed as:

$$\left|v_{grid}{}^{k-1}\right|^2 = \left(v_{grid\alpha}{}^{k-1}\right)^2 + \left(v_{grid\beta}{}^{k-1}\right)^2 \tag{4.47}$$

$$\left|v_{grid}{}^{k}\right|^2 = \left(v_{grid\alpha}{}^{k}\right)^2 + \left(v_{grid\beta}{}^{k}\right)^2 \tag{4.48}$$

According to figure 4.4, the grid voltage magnitude at the time instant *k* can be expressed using the value of $v_{grid}{}^{k}$ extracted from the system model in *α-β*:

$$\left(v_{grid\alpha}{}^{k}\right)^2 = \left(L \cdot \frac{di_{s\alpha}}{dt} + r \cdot i_{s\alpha}{}^{k} + v_{C\alpha}{}^{k}\right)^2 \tag{4.49}$$

$$\left(v_{grid\beta}{}^{k}\right)^2 = \left(L \cdot \frac{di_{s\beta}}{dt} + r \cdot i_{s\beta}{}^{k} + v_{C\beta}{}^{k}\right)^2 \tag{4.50}$$

Where, *L* signifies the combined total line inductance (L_S+L_C), $i_{s\alpha}{}^{k}$ and $i_{s\beta}{}^{k}$ are the supply currents in stationary reference frame representation at instant *k*, the converter voltages $v_{c\alpha}{}^{k}$ and $v_{c\beta}{}^{k}$ are calculated using the optimized switching signals obtained from (4.43), the dc-link voltage and using (4.44)-(4.46) that takes into account the effect of voltage drop due to IGBT dead-time. Hence, the square of the grid voltage magnitude at instant *k* is expressed as

$$\left|v_{grid}{}^{k}\right|^2 = \left(L \cdot \frac{di_{s\alpha}}{dt} + r \cdot i_{s\alpha}{}^{k} + v_{C\alpha}{}^{k}\right)^2 + \left(L \cdot \frac{di_{s\beta}}{dt} + r \cdot i_{s\beta}{}^{k} + v_{C\beta}{}^{k}\right)^2 \tag{4.51}$$

Similarly, the square of the grid voltage at the previous instant *k-1* is expressed as

$$\left|{v_{grid}}^{k-1}\right|^2 = \left(L \cdot \frac{di_{s\alpha}}{dt} + r \cdot {i_{s\alpha}}^{k-1} + {v_{C\alpha}}^{k-1}\right)^2 + \left(L \cdot \frac{di_{s\beta}}{dt} + r \cdot {i_{s\beta}}^{k-1} + {v_{C\beta}}^{k-1}\right)^2 \quad (4.52)$$

After discretizing the current derivatives for *past*, *present* and *future* sampling instants using Euler approximation method in [74], (4.51) and (4.52) are solved for the value of the total inductance *L* such that:

$$\left|{v_{grid}}^{k}\right|^2 - \left|{v_{grid}}^{k-1}\right|^2 \approx 0 \quad (4.53)$$

Substituting (4.51) and (4.52) in (4.53):

$$\left(L \cdot \frac{di_{s\alpha}}{dt} + r \cdot {i_{s\alpha}}^{k} + {v_{C\alpha}}^{k}\right)^2 + \left(L \cdot \frac{di_{s\beta}}{dt} + r \cdot {i_{s\beta}}^{k} + {v_{C\beta}}^{k}\right)^2 - \left(L \cdot \frac{di_{s\alpha}}{dt} + r \cdot {i_{s\alpha}}^{k-1} + {v_{C\alpha}}^{k-1}\right)^2 - \left(L \cdot \frac{di_{s\beta}}{dt} + r \cdot {i_{s\beta}}^{k-1} + {v_{C\beta}}^{k-1}\right)^2 \approx 0 \quad (4.54)$$

For a better understanding of the equations coming ahead, the estimation of the total inductance, *L*, is referred as $\hat{L}_{EST}$. Therefore, solving (4.54) for $\hat{L}_{EST}$ results in a quadratic equation as:

$${\hat{L}_{EST}}^2 \cdot A + \hat{L}_{EST} \cdot B + C = 0 \quad (4.55)$$

Where, the terms *A*, *B* and *C* are function of supply current and converter voltages in *α-β* for sampling instants *k*, *k-1* and *k-2* as explained in (4.56) – (4.66):

$$A = (\Delta A_{\alpha 1})^2 + \left(\Delta A_{\beta 1}\right)^2 - (\Delta A_{\alpha 2})^2 - \left(\Delta A_{\beta 2}\right)^2 \quad (4.56)$$

$$B = 2 \cdot \left(\Delta B_{\alpha 1} \cdot \Delta A_{\alpha 1} + \Delta B_{\beta 1} \cdot \Delta A_{\beta 1} - \Delta B_{\alpha 2} \cdot \Delta A_{\alpha 2} - \Delta B_{\beta 2} \cdot \Delta A_{\beta 2}\right) \quad (4.57)$$

$$C = (\Delta B_{\alpha 1})^2 + \left(\Delta B_{\beta 1}\right)^2 - (\Delta B_{\alpha 2})^2 - \left(\Delta B_{\beta 2}\right)^2 \quad (4.58)$$

$$\Delta A_{\alpha 1} = \frac{{i_{s\alpha}}^{k} - {i_{s\alpha}}^{k-1}}{t_s} \quad (4.59) \qquad \Delta A_{\alpha 2} = \frac{{i_{s\alpha}}^{k-1} - {i_{s\alpha}}^{k-2}}{t_s} \quad (4.60)$$

$$\Delta A_{\beta 1} = \frac{{i_{s\beta}}^{k} - {i_{s\beta}}^{k-1}}{t_s} \quad (4.61) \qquad \Delta A_{\beta 2} = \frac{{i_{s\beta}}^{k-1} - {i_{s\beta}}^{k-2}}{t_s} \quad (4.62)$$

$$\Delta B_{\alpha 1} = r \cdot {i_{s\alpha}}^{k-1} + {v_{C\alpha}}^{k-1} \quad (4.63) \qquad \Delta B_{\alpha 2} = r \cdot {i_{s\alpha}}^{k-2} + {v_{C\alpha}}^{k-2} \quad (4.64)$$

$$\Delta B_{\beta 1} = r \cdot {i_{s\beta}}^{k-1} + {v_{C\beta}}^{k-1} \quad (4.65) \qquad \Delta B_{\beta 2} = r \cdot {i_{s\beta}}^{k-2} + {v_{C\beta}}^{k-2} \quad (4.66)$$

The supply current and converter voltage terms at different sampling intervals are shown in simple terms in figure 4.13:

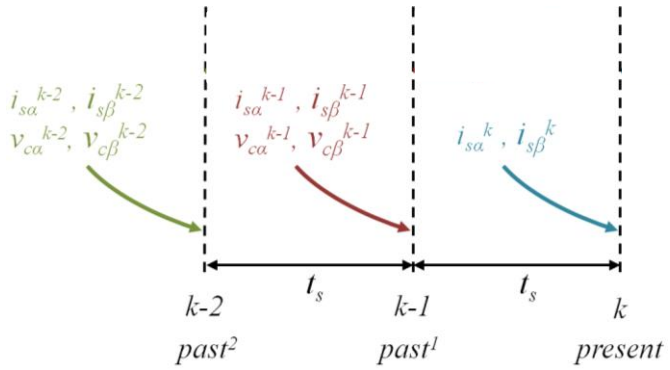


Figure 4.13: Current and converter voltage terms used in the inductance estimator

After substituting (4.56) – (4.66) in (4.55) and equating for estimation of the total inductance using the quadratic equation expression in (4.36), (4.37), estimation of the total inductance, $\hat{L}_{EST}$, is hence equated as:

$$\hat{L}_{EST} = \frac{1}{2} \cdot \frac{B}{A} \cdot \left[-1 + \sqrt{1 - \frac{4 \cdot A \cdot C}{B^2}} \right] \tag{4.67}$$

The total estimated value of inductance in (4.67), once excluded the negative root, is used as an update to the inductance value used in the current predictions in (4.1), (4.19), (4.21) and (4.22). Since the estimation algorithm consists of converter voltages and supply currents, it is important to include some saturation limit that act like a filter to remove high switching frequency component present in the estimation algorithm. The reason for not using Low Pass Filter was as a Low Pass Filter resulted in a slower response of estimation result to a step in grid inductance. The code used for setting up the saturation limit on the estimation result of (4.67) is shown as below:

$if \left\{ \left(\hat{L}_{EST} - \hat{L}_{EST-previous} \right) > 0.0001 \right\}$

$\hat{L}_{EST} = \hat{L}_{EST-previous} + 0.0001;$

end

$if \left\{ \left(\hat{L}_{EST} - \hat{L}_{EST-previous} \right) < -0.00001 \right\}$

$\hat{L}_{EST} = \hat{L}_{EST-previous} if \left\{ \left(\hat{L}_{EST} - \hat{L}_{EST-previous} \right) > 0.0001 \right\}$

$\hat{L}_{EST} = \hat{L}_{EST-previous} + 0.0001;$

end

Where, $\hat{L}_{EST-previous}$ is the one-sample previous stored value of $\hat{L}_{EST}$.

The procedure for grid inductance estimation of method 1 that is integrated within the model predictive direct power control is illustrated in figure 4.14.

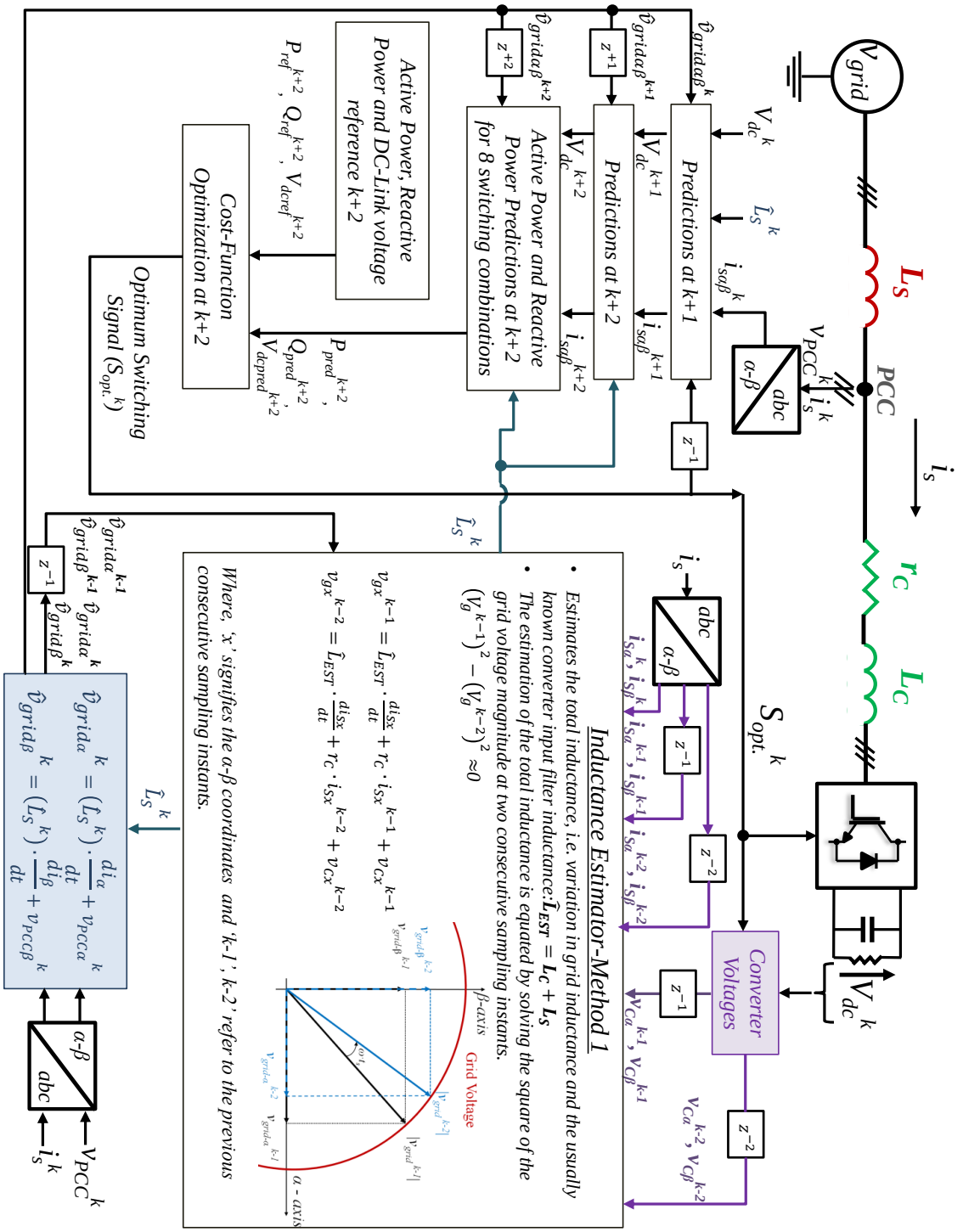


Figure 4.14: Block Diagram of MP-DPC with Inductance Estimator method 1

4.4.2.2. Grid Voltage Estimation

If the voltage at the point of common coupling, v_{pcc}, presents a substantial distortion and it is used in the predictive control model, it will in turn induce distortion on the current predictions. Many authors propose on using Low Pass Filters or Anti-Aliasing Filters for filtering out frequency harmonics from the voltage at the PCC before using it in the control algorithm [69], [106], [107]. Furthermore, for a low SCR value with dominance of grid inductance, a phase shift in v_{pcc} is introduced which can also affect the predictive control performance. The phase shift for the v_{pcc} may not be straightforward to compensate as it may not remain consistent for different variations SCR values. Once the total inductance in (4.67) has been estimated, the supply inductance $\hat{L}_S$ is estimated as:

$$\hat{L}_S = \hat{L}_{EST} - L_C \tag{4.68}$$

Where, L_C corresponds to the converter input filter inductance and its value is usually known. As shown in figure 4.14, the grid voltage estimation is integrated within the MP-DPC to update the current predictions with the latest estimated value of grid inductance and grid voltage instead of using the voltage at the PCC. Therefore, the voltage used for the predictive controller is corrected using the estimation in (4.69) and (4.70) for the respective α-β reference frames:

$$\hat{v}_{grid\alpha}{}^{k} = \hat{L}_S \cdot \frac{i_{S\alpha}{}^{k+1} - i_{S\alpha}{}^{k}}{t_s} + v_{pcc\alpha}{}^{k} \tag{4.69}$$

$$\hat{v}_{grid\beta}{}^{k} = \hat{L}_S \cdot \frac{i_{S\beta}{}^{k+1} - i_{S\beta}{}^{k}}{t_s} + v_{pcc\beta}{}^{k} \tag{4.70}$$

Where, $\hat{L}_S$ is the estimated grid inductance and $v_{pcc\alpha}{}^{k}$, $v_{pcc\beta}{}^{k}$ are the measured PCC voltages and the current derivatives in stationary reference frames are discretized into their respective *future* and *present* sampling instants.

4.4.2.3. Integration of grid inductance and voltage estimation with MP-DPC

Using the estimated grid voltages, the current predictions of (4.18), (4.19) at *future*[1] instant *k+1* are updated as:

$$i_{S\alpha}{}^{k+1} = \boldsymbol{K_1} * \left(\hat{v}_{grid\alpha}{}^{k} - v_{C\alpha}{}^{k}\right) + \boldsymbol{K_2} * i_{S\alpha}{}^{k} \tag{4.71}$$

$$i_{S\beta}{}^{k+1} = \boldsymbol{K_1} * \left(\hat{v}_{grid\beta}{}^{k} - v_{C\beta}{}^{k}\right) + \boldsymbol{K_2} * i_{S\beta}{}^{k} \tag{4.72}$$

Where, ***K1*** and ***K2*** are updated with the total estimation of inductance, i.e. grid inductance plus the converter input filter inductance as:

$$\boldsymbol{K_1} = \frac{t_s}{\hat{L}_{EST}} \qquad \boldsymbol{K_2} = \left(1 - \frac{r_C * t_s}{\hat{L}_{EST}}\right)$$

And current predictions of (4.21) and (4.22) at *future*[2] instant *k+2* are updated for each of the possible switching combinations (*i = {0-7}*) as:

$$i_{S\alpha-i}{}^{k+2} = \boldsymbol{K_1} * \left(\hat{v}_{grid\alpha}{}^{k+1} - v_{C\alpha}{}^{k+1}\right) + \boldsymbol{K_2} * i_{S\alpha}{}^{k+1} \tag{4.73}$$

$$i_{S\beta-i}{}^{k+2} = \boldsymbol{K_1} * \left(\hat{v}_{grid\beta}{}^{k+1} - v_{C\beta}{}^{k+1}\right) + \boldsymbol{K_2} * i_{S\beta}{}^{k+1} \tag{4.74}$$

Where, $\hat{v}_{grid\alpha}{}^{k+1}$ and $\hat{v}_{grid\beta}{}^{k+1}$ are the one sample ahead grid voltage estimations that can be calculated using linear-type predictions or Lagrange extrapolation [89], [108]. However, as the results in chapters 5 and 6 show, since the estimation of inductance is precise and has a steady state error less than 0.5%, the variation in grid voltage estimation between two consecutive sampling instants is less than 1% on average.

Thus, the grid voltage at *k+1* is imposed to be equal to its value at instant *k*. Using the current predictions in (4.73) and (4.74) for each of the possible switching combinations, the active and reactive powers are updated in a way that the resultant control action takes into account grid impedance variations and the system performance does not get affected by parameter mismatches.

4.4.3. Inductance Estimation Algorithm – Method 2

Though inductance estimation method 1 estimates the variation in grid inductance quite accurately, as it will be shown in the next chapter of simulation results, it does not have a good response in case of an unbalanced grid voltage condition, as it relies on a constant magnitude of the grid voltage. For this reason, estimation method 2 is proposed in this section, which even works under unbalanced grid voltages as is shown with the help of simulation results in chapter 5. The integration of the estimation method 2 in the MP-DPC is carried out in the same way as done for method 1 and also takes into account the effect of dead-time since it also relies on the information of the converter input voltages. The working principle is explained in the following sections.

4.4.3.1. Working Principle

Similar to method 1, method 2 estimates the grid inductance in real-time as well and feeds the estimated value as an update to the MP-DPC. The method is implemented in a stationary reference frame and uses the measured current ($i_{S\alpha}$, $i_{S\beta}$), the estimated grid voltages ($\hat{v}_{g\alpha}$, $\hat{v}_{g\beta}$) and the converter input voltages ($v_{C\alpha}$, $v_{C\beta}$) at the previous sampling instants to estimate the grid currents ($\hat{\imath}_{S\alpha}$, $\hat{\imath}_{S\beta}$) at the present sampling instants for several values of the estimated grid inductance ($\hat{L}_S$).

The grid currents are estimated in their stationary α-β reference frames as shown in equations (4.75) and (4.76), respectively.

$$\hat{\imath}_{S\alpha}{}^{k} = \left(\hat{v}_{g\alpha}{}^{k-1} - v_{C\alpha}{}^{k-1}\right) \cdot \frac{t_s}{L_C + \hat{L}_S{}^{k}} - i_{S\alpha}{}^{k-1} \cdot \left(1 - \frac{r_C t_s}{L_C + \hat{L}_S{}^{k}}\right) \tag{4.75}$$

$$\hat{\imath}_{S\beta}{}^{k} = \left(\hat{v}_{g\beta}{}^{k-1} - v_{C\beta}{}^{k-1}\right) \cdot \frac{t_s}{L_C + \hat{L}_S{}^{k}} - i_{S\beta}{}^{k-1} \cdot \left(1 - \frac{r_C t_s}{L_C + \hat{L}_S{}^{k}}\right) \tag{4.76}$$

Where, L_C is the converter input filter inductance, r_C is its parasitic resistance, t_s is the sample time, $i_{s\alpha}{}^{k-1}$ and $i_{s\beta}{}^{k-1}$ are the stationary reference frame grid currents at the previous sampling instant *k-1*, $v_{c\alpha}{}^{k-1}$ and $v_{c\beta}{}^{k-1}$ are the converter voltages at the previous sampling instants, $\hat{v}_{g\alpha}{}^{k-1}$ and $\hat{v}_{g\beta}{}^{k-1}$ are the estimated grid voltages at the previous sampling instant calculated in the same way as done in equations (4.69) and (4.70) and the grid inductance $\hat{L}_S{}^{k}$ is estimated as:

$$\hat{L}_S{}^{k} = \hat{L}_S{}^{k} \pm n \cdot \Delta L_S \tag{4.77}$$

The term ΔL_S represents the accuracy of the estimator and is usually tuned to a small value for a better accuracy. While initiating the estimation algorithm, the user needs to define an initial mean value of supply inductance to set the ΔL_S and n values. Once the process of estimation begins, after a few sampling intervals the estimation algorithm adapts itself to give the right value and thus repeats every sampling interval. For example, in (4.78), ΔL_S is equal to 0.1mH while the mean value of supply inductance was 1.0mH. This signifies that with reference to the mean value of the estimated inductance, the variation in resolution of the inductance is 0.1mH. While n is limited by the computational resources that are available on the practical implementation.

$$\Delta L_S = 0.1mH \tag{4.78}$$

It is not important, however, that ΔL_S is always set to the same value. Depending on the application, the ΔL_S can be increased or decreased. A small value of ΔL_S results in a slower and more affected by noise estimation while a larger value would result in faster convergence.

4.4.3.2. Cost function optimization

Amongst all the considered values of the estimated grid inductance, $\hat{L}_S{}^k$, the correct value is selected based on the one that minimizes the cost function in equation (4.79) consisting of the difference between the measured supply current and the estimated supply current of equations (4.75) and (4.76) at each sampling interval. Therefore, the cost function G_L for the inductance estimator is presented as below:

$$G_L(\pm n) = \sqrt{\left(\hat{\imath}_{S\alpha}{}^k(\pm n) - i_{S\alpha}{}^k\right)^2 + \left(\hat{\imath}_{S\beta}{}^k(\pm n) - i_{S\beta}{}^k\right)^2} \tag{4.79}$$

By defining the upper and lower number of steps, *n*, the user can execute the necessary number of iterations at each sampling interval necessary to execute the algorithm. Moreover, the execution time of the algorithm can be varied by carefully choosing the value of *n* so as to minimize the computational effort of the DSP for algorithm processing. In addition to the aforementioned, *n* and ΔL_S, can be set in order to obtain the required estimation accuracy and response without exceeding practical implementations computational constraints. For example, table 4.2 shows a relation between the number of iterations and the required accuracy of grid inductance when the estimation method 2 was applied on the three phase two level active rectifier of figure 4.1.

TABLE 4.2.RELATION BETWEEN INTEGER STEPS AND REQUIRED ACCURACY OF GRID INDUCTANCE ESTIMATION

No. of iterations per sampling interval	$\Delta L_S(mH)$	**n**
9	0.1	±4
11	0.01	±5
13	0.001	±6

In table 4.2, *i* has been varied from 9 to 13 between the upper and lower boundary limits ±n from ±4 to ±6, respectively. As the number of iterations increases, the current THD gets lower as a better accuracy is achieved and hence gives a good power quality as well, as is shown in results of chapter 5 for estimation method 2. For example, for a high number of iterations, 13, where the boundary limit *n* is ±6, between each step *n* the variation of ΔL_S in table 4.2 has a value of 0.001mH that results in a precise estimation of the grid inductance with a high accuracy. On the contrary, for a smaller boundary limit where *n* is ±3, ΔL_S has a larger variation of 0.1mH and precision of the estimated inductance deteriorates. Therefore, a careful tuning of these parameters is required according to the practical system limitations like computational effort of the DSP and FPGA. However, in case of a variation in inductance, the estimation algorithm can take more than one sampling interval to give the final result. Figure 4.15 shows an equivalent representation highlighting the significance of ΔL_S.

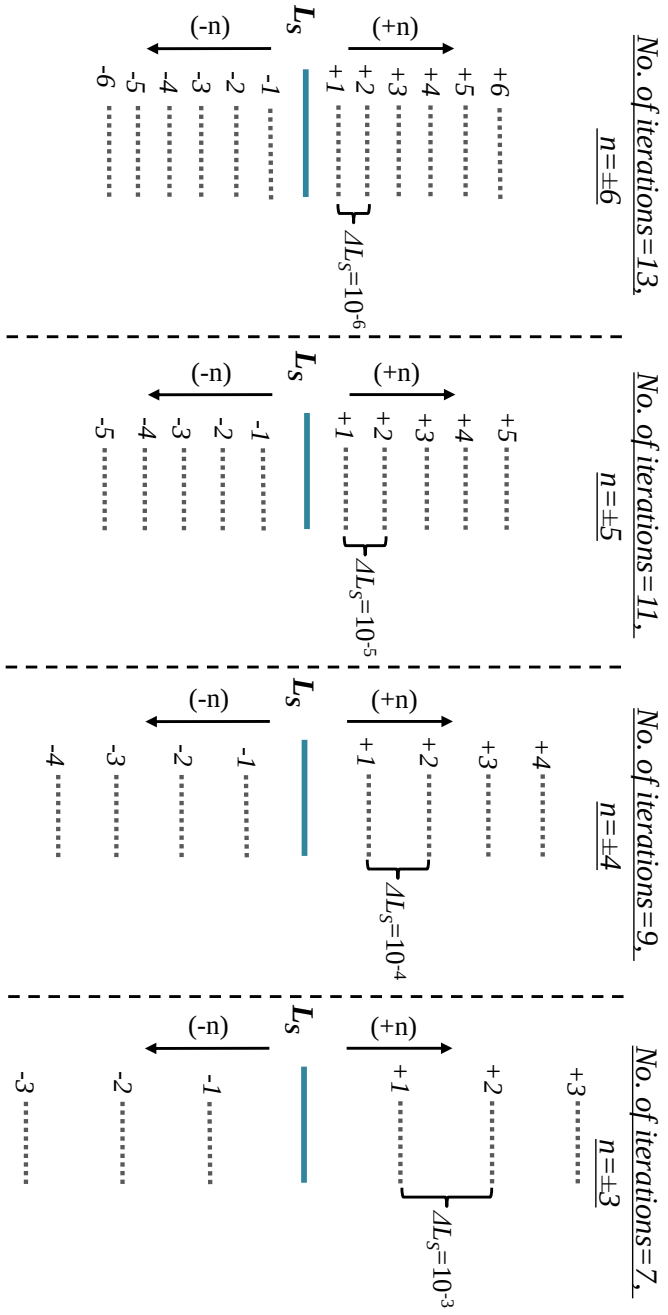


Figure 4.15: Relation between number of iterations and accuracy of inductance estimation

The procedure for grid inductance estimation of method 2 that is integrated within the model predictive direct power control is illustrated in figure 4.16.

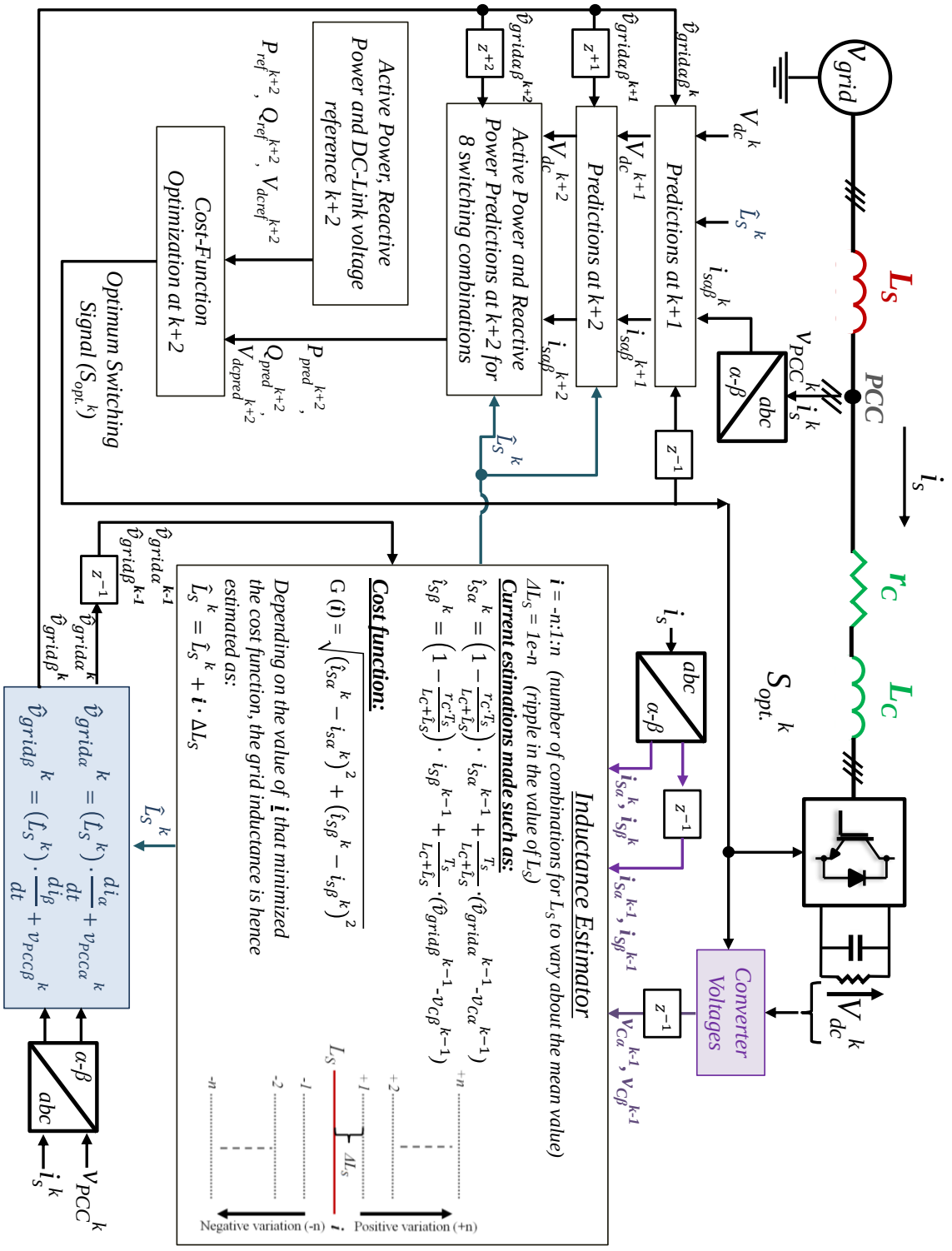


Figure 4.16: Block Diagram of MP-DPC with Inductance Estimator method 2

4.4.4. Remarks

The proposed estimation algorithms have focused on estimation of grid inductance as the effect of grid resistance is not as significant as grid inductance. While variation in grid resistance may affect the amplitude of the voltage at the PCC, the inductance not only affects the amplitude but also introduces a phase shift (larger in case of low SCR values), thus, affecting the control performance significantly. Nevertheless, the variation in grid resistance can also be included in the proposed estimation algorithm such that the grid inductance and grid resistance terms can be collectively estimated in the equation (4.80):

$$v_{grid\alpha\beta} = L_S \cdot \frac{di_{s\alpha\beta}}{dt} + r_S \cdot i_{s\alpha\beta} + L_C \cdot \frac{di_{s\alpha\beta}}{dt} + r_C \cdot i_{s\alpha\beta} + v_{C\alpha\beta} \qquad (4.80)$$

Where, r_S and L_S are the grid resistance and grid inductance terms. Solving (4.80) for the present and past sampling intervals and extracting the inductive-resistive terms would result in a complex algorithm and hence a higher computational time.

Similarly, the grid capacitance can also be included in the estimation algorithm by modifying the predictive model and also the estimation algorithm. The figures below show equivalent representation of grid capacitance for two cases and give a mathematical explanation about significance of the capacitance term for the estimator, one before the grid inductance and the other after the grid inductance such that the effect of the capacitance is seen at the point of common coupling.

Mathematical Analysis for Case 1 of grid capacitance presence:

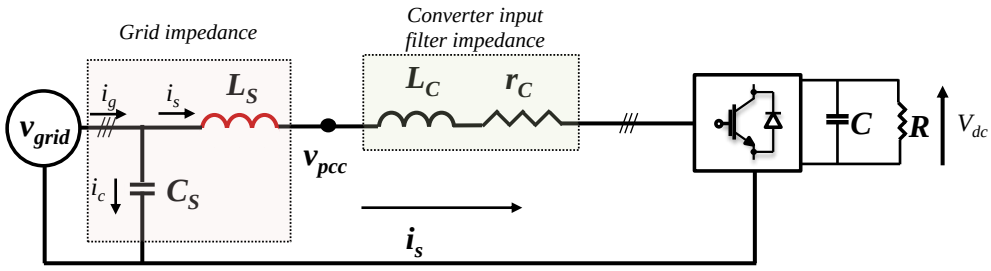


Figure 4.17: Case 1 of grid capacitance presence

Solving the grid side model mathematically:

$$v_{grid} - v_{pcc} = L_S \frac{di_s}{dt} \tag{4.81}$$

Where,

$$i_s = i_g + i_c \tag{4.82}$$

i_c represents the capacitor current and is given by:

$$i_c = C_s \frac{dv_{grid}}{dt} \tag{4.83}$$

Substituting (4.83) in (4.82) and then substituting (4.82) in (4.81) gives:

$$v_{grid} - v_{pcc} = L_S \frac{di_g}{dt} - L_S C_S \frac{d^2 v_{grid}}{dt^2} \tag{4.84}$$

Changing (4.84) in s-domain results in:

$$v_{grid} - v_{pcc} = sL_S i_g - s^2 L_S C_S v_{grid} \tag{4.85}$$

Further simplifying (4.85) to bring the v_{grid} terms on the left hand side:

$$v_{grid}(1 + s^2 L_S C_S) = sL_S i_g + v_{pcc} \tag{4.86}$$

The second order term $s^2 L_S C_S$ in (4.86) has a very minimal effect on the estimation algorithm as the capacitance and inductive terms are in mH or µF respectively. Therefore, this term has values much less than 1. Hence, the effect of $s^2 L_S C_S$ can be ignored and (4.86) can be simplified as:

$$v_{grid} = sL_S i_g + v_{pcc} \tag{4.87}$$

Mathematical Analysis for Case 2 of grid capacitance presence:

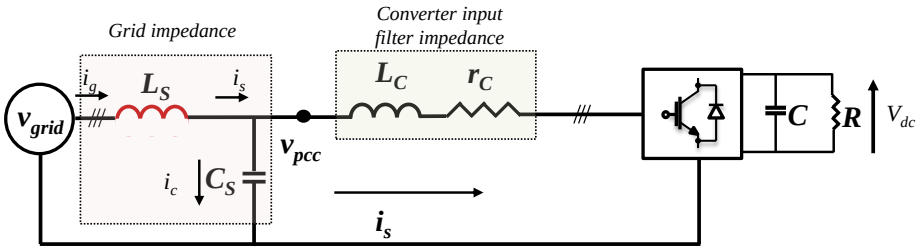


Figure 4.18: Case 2 of grid capacitance presence

Similar to case 1, the grid side model can be solved as well

$$v_{grid} - v_{pcc} = L_S \frac{di_g}{dt} \tag{4.88}$$

Where,

$$i_g = i_c + i_s \tag{4.89}$$

And i_c represents the capacitor voltage at the point of common coupling represented as:

$$i_c = C_s \frac{dv_{pcc}}{dt} \tag{4.90}$$

Substituting (4.90) in (4.89) and then substituting (4.89) in (4.88):

$$v_{grid} - v_{pcc} = L_S \frac{di_g}{dt} + L_S C_S \frac{d^2 v_{pcc}}{dt^2} \tag{4.91}$$

Changing (4.91) in s-domain and bringing the v_{pcc} terms to the same side results in:

$$v_{grid} - v_{pcc}(1 + s^2 L_S C_S) = s L_S i_g \tag{4.92}$$

Similar to the explanation in *Case 1*, the significance of $s^2 L_S C_S$ would be minimal and it can be ignored to give a simplified grid side model as:

$$v_{grid} = s L_S i_g + v_{pcc} \tag{4.93}$$

Therefore, it can be concluded that the effect of grid capacitance may not present a significant threat to the estimation algorithm as variation in grid capacitance is very small. However, it can always be included in the estimation algorithm by modifying the estimation method.

4.5. Conclusion

In the recent past, grid-connected converters have gained popularity, particularly for renewable energy systems integration, where in some cases the grid is not stiff. Small grid parameter variations in these systems can substantially affect the performance of the converter control. This chapter has presented two novel grid inductance estimation methods that are used in real-time in conjunction with the Model Predictive Direct Power Control to update the inductance value in the control system.

The increase in v_{pcc} ripple along with the variation in grid inductance can greatly affect the predictive control performance. Estimating the variation in grid inductance allows the estimation of the grid voltage inside the controller so that the v_{pcc} can be updated at each sampling interval for a better quality operation. The proposed algorithm can be

easily adapted to be used for general grid impedance estimation and in the case of any topology of grid connected converters.

The integration of the estimation methods 1 and 2 in the MP-DPC is carried out in a similar fashion where the total line inductance in the model is updated with the latest estimation of grid inductance. Also, the grid voltage is estimated in the similar manner. Moreover, as compared to the proposed estimation method 1 where the estimation algorithm relies on the grid voltage magnitude, method 2 can work under unbalanced grid voltage conditions as it relies on estimation of the supply current and not the grid voltage magnitude.

The estimation approaches have been integrated within the model based predictive control, thus making the estimation and control effective and efficient. The efficacy of the proposed estimation methods with the Model Based Predictive Direct Power control using a three phase two level active front end are shown with the help of simulation results in the next chapter, Chapter 5, and with the help of experimental results in Chapter 6.

Chapter 5: Simulation Results

5.1. Introduction

This chapter presents simulation results for the MP-DPC and the proposed grid inductance estimation algorithms that are integrated within the predictive control, thus updating the controller in real-time with the latest value in grid inductance.

The chapter is divided into 6 sections and begins by presenting the transient and steady state performance of the MP-DPC for variations of the DC-Link voltage reference and for variation of the reactive power reference, in the first two sections. As mentioned in Chapter 2.3, the converter control performance can get significantly affected to parameter mismatches, like variation in grid impedance. Simulation results for MP-DPC under an unknown variation in grid inductance are presented in section 5.2.3. However, once this variation in grid impedance is estimated, it can be used to update the MP-DPC in real-time and improve its performance. The results for online grid impedance estimation using the two proposed estimation algorithms are presented in sections 5.3 and 5.4, respectively.

5.2. Simulation tests platform

Simulation parameters for the tested 2.4kW three phase two-level grid connected converter are shown in table 5.1. A grid voltage of $100V_{rms}$ has been used, as in the experimental setup, and a sample time of 50μs for the predictive controller. The converter input filter inductance is 4.5mH while a dc-link voltage capacitor of 2200μF is used as in the experimental setup.

The simulation tests have been conducted on Matlab SIMULINK version R2013a that has an integrated PLECS software toolbox, version 3.3.4, used for schematic of the power converter as shown in figure 5.1. Matlab Simulink and PLECS software provides an advantage of designing the power converter switching devices with realistic

parameters like in practical implementation that include on-state resistance and dead-time inclusion, for example, and also implement the control algorithm in a similar manner as it is implemented in the practical system on the DSP.

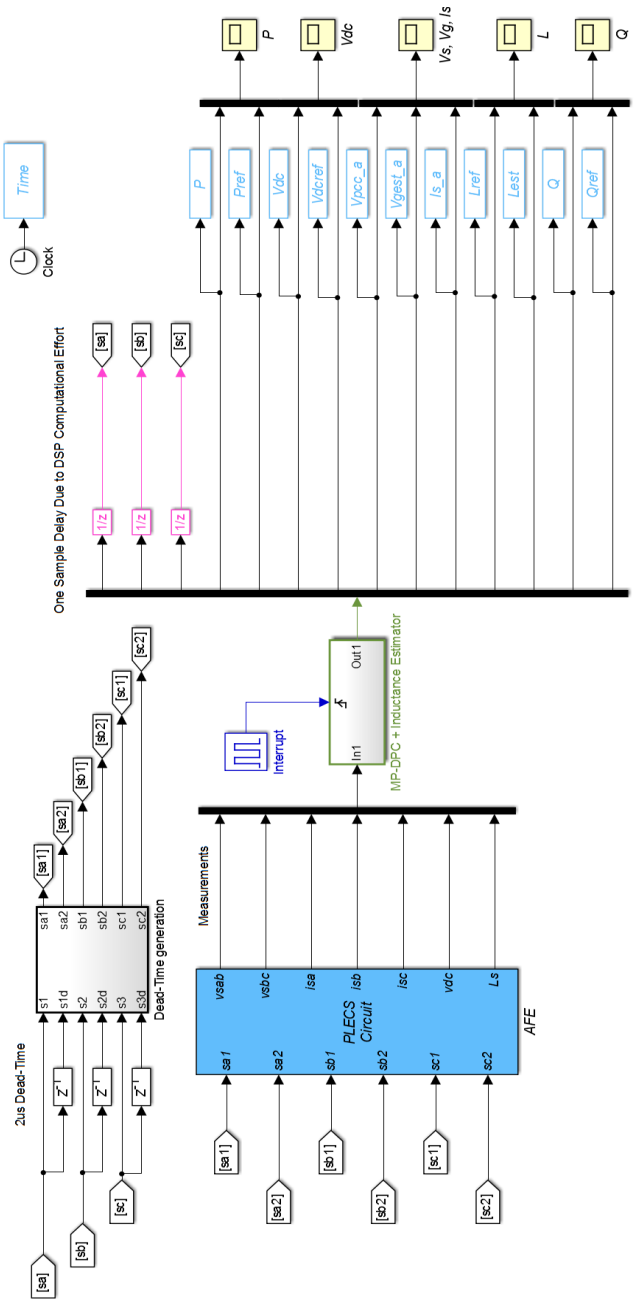


Figure 5.1: Matlab SIMULINK schematic

In figure 5.1, the measurements of the line to line voltages at the PCC, the three phase supply currents and the dc-link voltage are taken as inputs from the AFE of figure 5.2 for control process. Similar to the practical system DSP implementation, the control acquisition takes place at the beginning of every interrupt period, referred as the sample time in table 5.1. The output of the MP-DPC are the three optimized switching signals applied to the IGBT switches in each leg of the AFE that are obtained through cost-function optimization as explained in section 4.2.8. In practical system implementation, due to high computational effort a delay of one-sample is introduced. This is portrayed as a delay block referred as 1/z in figure 5.1. Moreover, dead-time is also introduced in each leg to make sure that the upper and lower switches are not simultaneously turned ON or OFF so as to avoid short-circuit. The input switching signals of the IGBTs in figure 5.2 now consist of dead-time and also one sample delay due to practical system computational effort that have been compensated as explained in chapter 4 within the MP-DPC. A dead-time of 2μs is implemented in the simulation file of figure 5.1 and figure 5.2 in the form of a code. Its implementation is explained in Appendix D and Appendix D.1 and its compensation within the MP-DPC is explained in section 4.3.

The three phase two-level converter in figure 5.2 is constructed in PLECS environment such that it takes as input three sinusoidal voltages with a phase displacement of 120° for each of the respective phases. Variable grid inductance for each phase is modelled that is labelled as Lsa, Lsb and Lsc and the measurements of voltages and currents are taken at the point of common coupling referred as Vpcc_a, Vpcc_b and Vpcc_c, respectively, in figure 5.2. The converter input filter is modelled as an inductive-resistive filter with inductance and resistance for each of the phases labelled as Lca, Lcb, Lcc, ra, rb and rc,

respectively. The converter power switches are modelled as an IGBT with free-wheeling diodes in parallel referred as Da1, Da2, Db1, Db2, Dc1 and Dc2, respectively as shown in figure 5.2. The reason to add a free-wheeling diode is to provide a circulating path to the current during dead-time when one IGBT turns OFF and the other is waiting to be turned ON.

Table 5.1: Simulation Parameters

Parameter	***Symbol***	***Value***
Supply voltage	V_{grid}	$100V_{rms}$
Converter filter inductance	L_C	*4.5mH*
Converter filter resistance	r_C	*0.2Ω*
Load resistance	*R*	*28.8Ω*
DC-link capacitance	*C*	*2200µF*
Active Power	*P*	*2.4kW*
Weighting factors	$\lambda_1, \lambda_2, \lambda_3$	*0.6, 0.2, 0.2*
Sampling time	T_S	*50µs*
Average Switching frequency	F_{SW}	*~9.7 kHz*

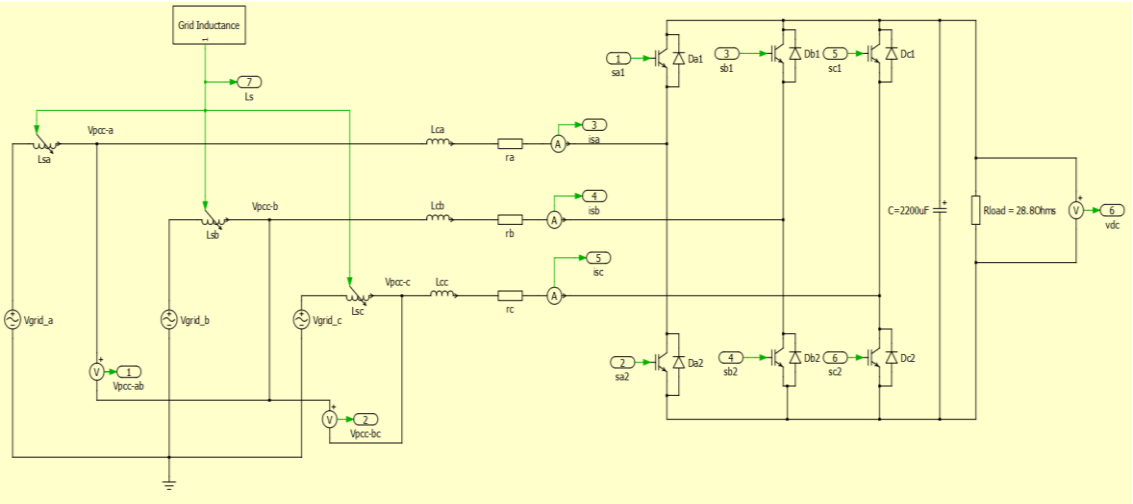


Figure 5.2: Three phase Two-level grid connected converter on PLECS

5.3. Model based Predictive Direct Power Control on a 3-Phase 2-Level AFE

Results in this section present the performance of the MP-DPC to variation in DC-link voltage reference, reactive power reference and in case of unknown variation in grid inductance value.

5.3.1. Model Predictive Direct Power Control: Past, Present and Future sampling intervals

Referring to table 5.1, the sample time used for the presented control system is 50µs. In figure 5.3, results are shown for the supply current referred as $isa_{measured}$ that is then sampled at the *present* instant and referred as isa_k in the figure. Using the optimum switching signals obtained from the cost function minimization, the predictive controller then makes predictions at $future^1$ instant referred as isa_{k+1} in the figure.

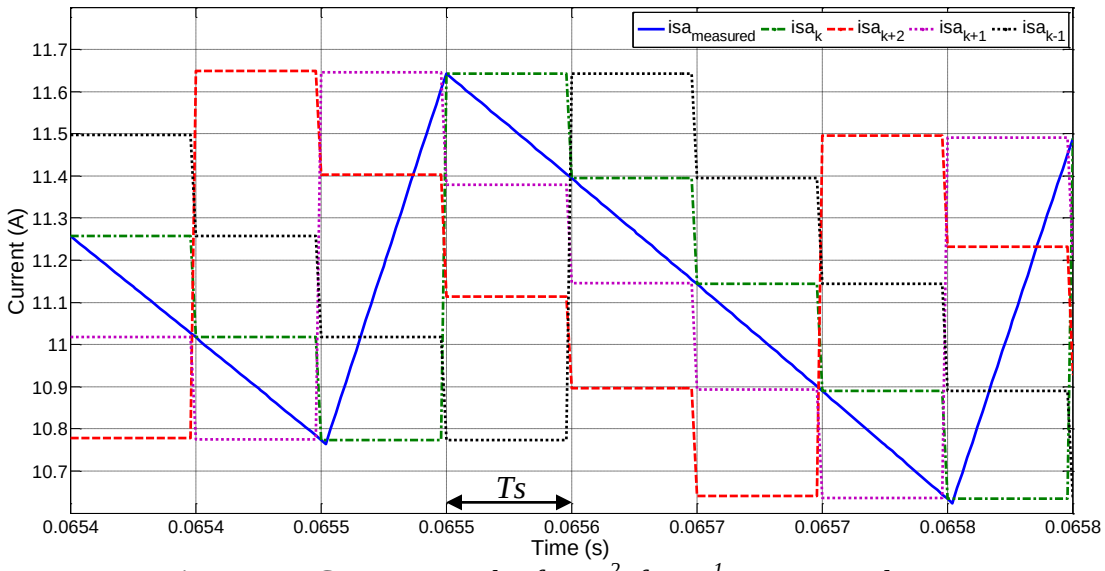


Figure 5.3: Current samples $future^2$, $future^1$, present and past

To compensate for the computational delay present in the practical system implementation due to algorithm calculation times, predictions at $future^2$ instant are carried out, referred as isa_{k+2} in figure 5.3. The current samples at the *previous* sampling

instant are referred as isa_{k-1}. Each division on the *x-axis* in figure 5.2 represents 50µs sampling time.

For the results presented in figure 5.3, the predictive control works with an online inductance estimation and dead-time compensation presented in the following sections. The supply current predictions at *k+1* and *k+2* depend on the value of estimated inductance. A correct estimation value results in an accurate calculation of these samples, as seen in figure 5.3, that show the same amplitude of predicted samples at two consecutive sampling instants and the measured sample at *k*. Therefore, online estimation presents good results for the supply current samples at *past*, *present* at *future* sampling intervals.

5.3.2. DC-link voltage with different values of N*

Classical control strategies, like voltage oriented control for example, use Proportional-Integral (PI) control for regulation of the dc-link voltage. The dc-link voltage reference in this work for MP-DPC is calculated based on the approach explained in section 4.2.6 of chapter 4.

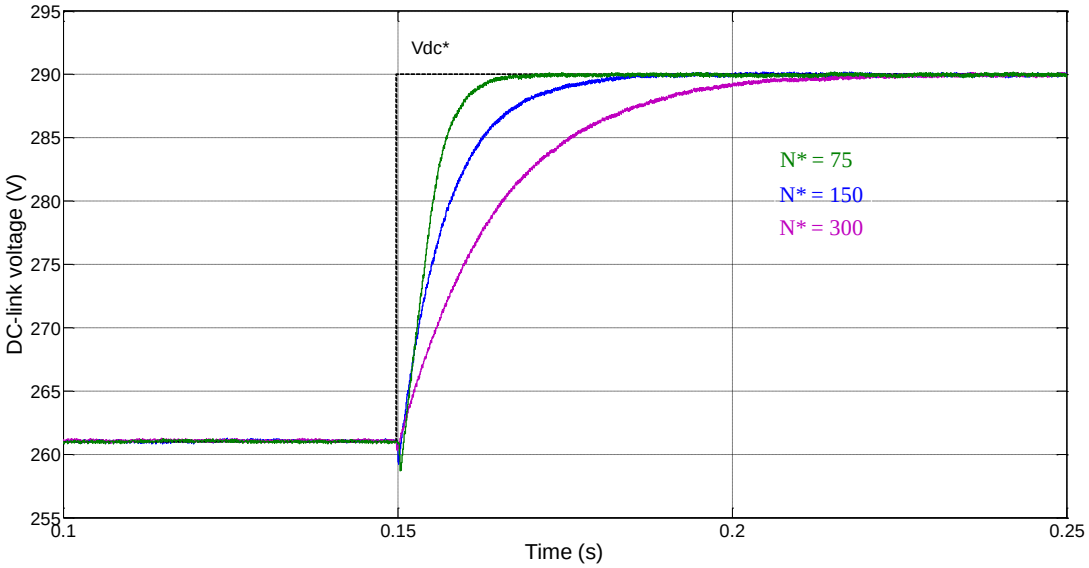


*Figure 5.4: DC-Link voltage with different values of N**

The dynamics of the dc-link voltage tracking can be controlled by adjusting the reference prediction horizon, N^* in equation (4.27). A higher N^* means the dc-link voltage takes longer time to reach its reference value, whereas, a smaller N^* means the dc-link voltage reaches its reference value quickly as shown in figure 5.4. This is done in order to have slower dynamics of the dc-link voltage as compared to the current control since the current control in MP-DPC acts like an inner control and the dc-link voltage control acts like an external controller that depends on the output from the current control.

5.3.3. Active and reactive power response to a step in DC-Link voltage reference

In order to show the adaptability of the AFE predictive controller when the DC load demand has a sudden surge, in this test the dc-link voltage reference is varied from 260V to 290V. As can be observed, the dc-link voltage follows its reference accurately without showing any significant steady state error. Results in figure 5.5 and 5.6 show the dc-link voltage response and active and reactive power response to a variation in dc-link voltage reference. The active power shows an increase from ~2.4kW to ~3.0kW at steady state and the reactive power maintains around its reference value of 0VAR without showing any significant steady state errors. Note also that a saturation limit is put on the active power in order to avoid damage of the power semiconductor switches. A sudden spike in current can exceed the maximum rating of the power devices and precautionary measures should be taken to avoid any damage.

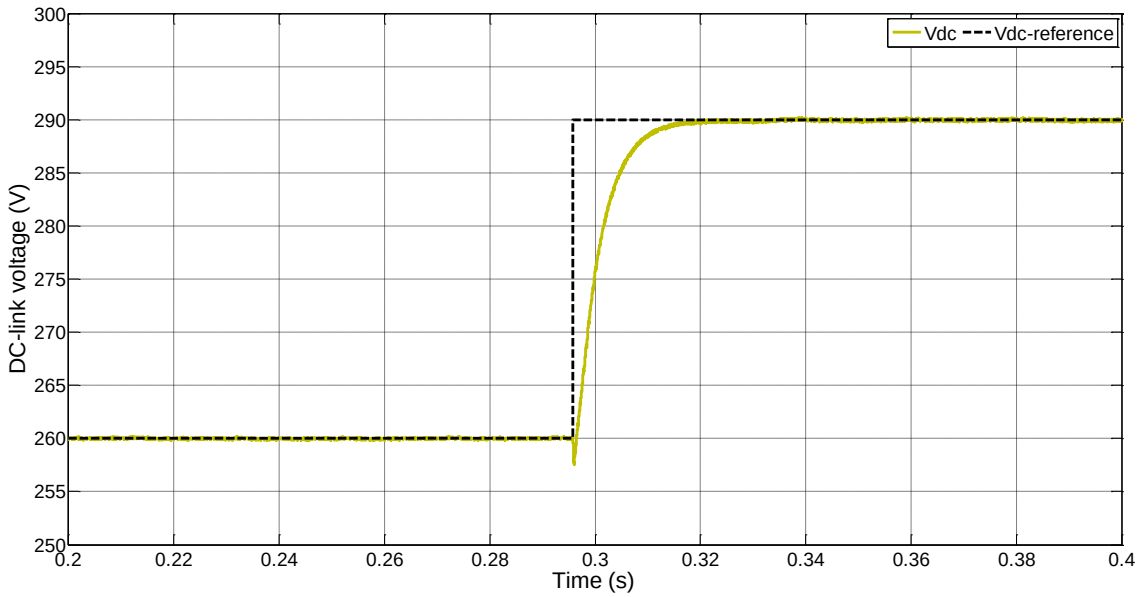


Figure 5.5: DC-Link voltage with reference N = 150*

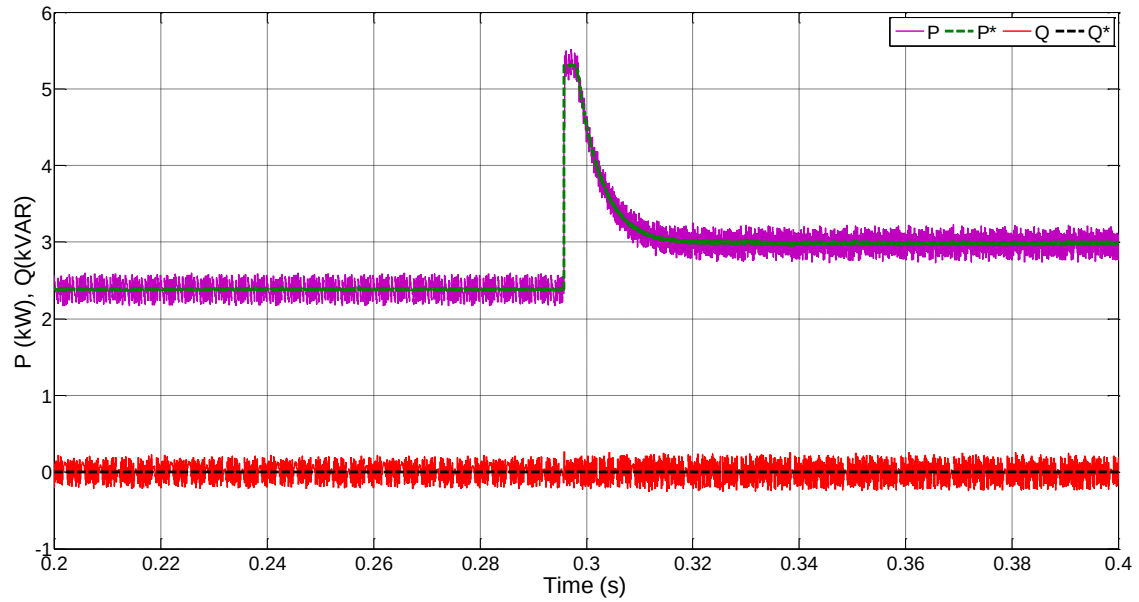


Figure 5.6: Active and reactive power with reference

Figure 5.7 shows the supply current and voltage at the PCC for variation in dc-link voltage reference. As the active power increases the supply current shows an increase in amplitude from 11.3A to 14.14A with a slight decrease in THD value from 6.3% to

5.6% while the modulation index reduces from ~1 to 0.97 where the modulation index is calculated as:

$$m = \frac{2\hat{v}_{pcc}}{V_{dc}} \tag{5.1}$$

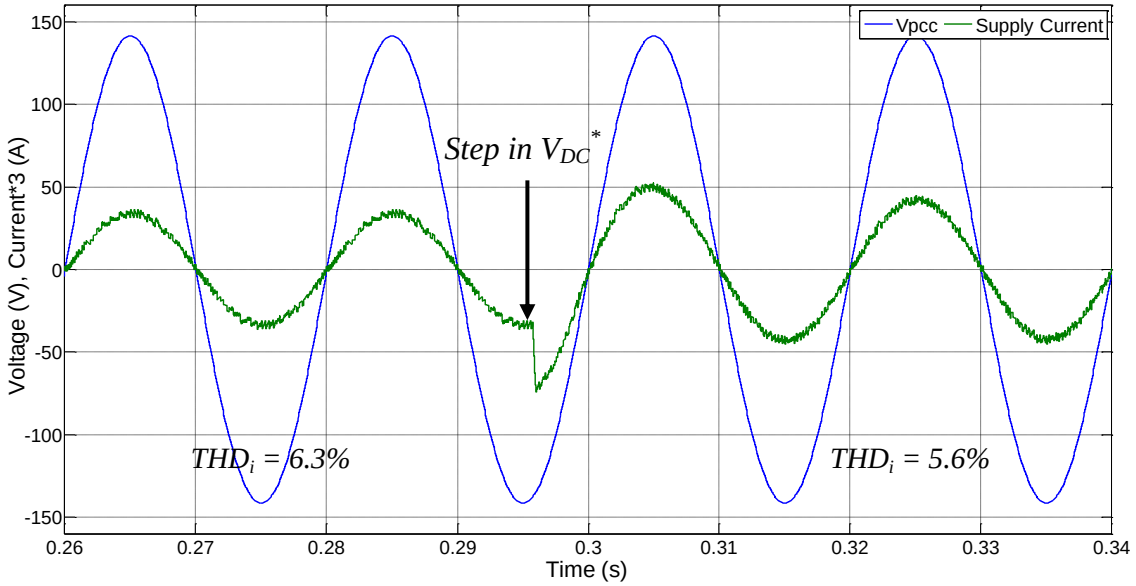


Figure 5.7: Supply current and Grid Voltage in synchronization

5.3.4. Reactive power variation

Figure 5.8 shows a good response of active and reactive power to a variation in reactive power reference from 0 VAR to 2 kVAR and 2 kVAR to -1 kVAR. That means at 0.1s, the power factor varies from approximately unity to 0.76 with a leading current waveform as compared to the voltage waveform. On the other hand, at 0.2s, the power factor varies from 0.76 to 0.92 and the supply current waveform now lags the voltage as the variation in reactive power is negative. A large spike in the active power is seen at the two time instants where a large variation in reactive power takes place. This is due to a sudden change in the supply current amplitude. Figure 5.9 shows instead the response of dc-link voltage to such a large variation in reactive power. The dc-link

voltage shows a steady state error of ±1V to such variations since the apparent power on the AC side changes. Figure 5.10 and figure 5.11 show the supply voltage and current response to such large variations in reactive power reference.

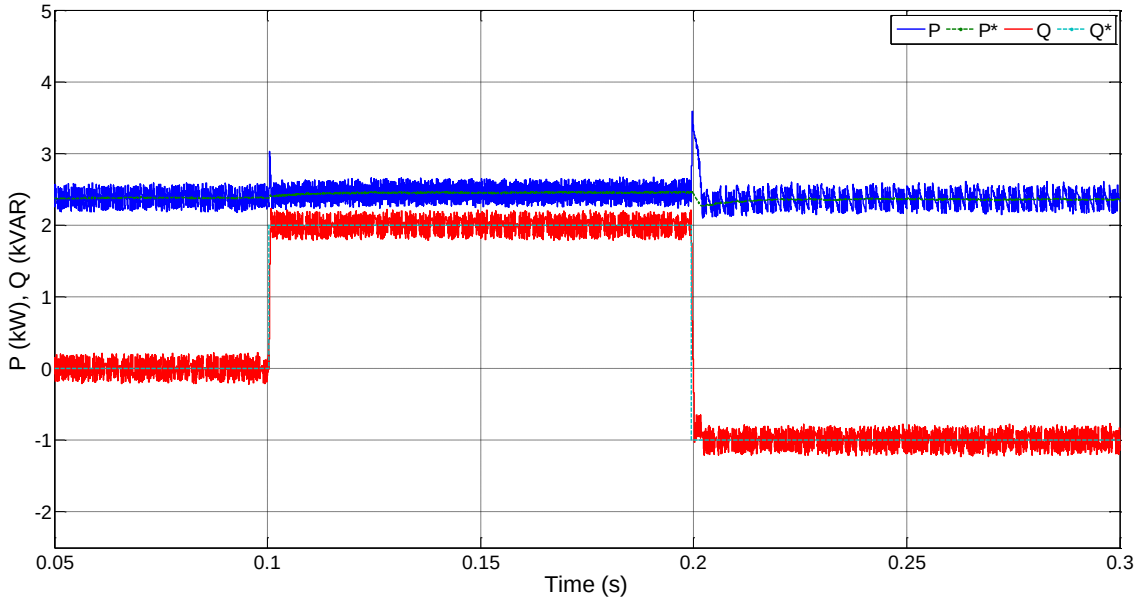


Figure 5.8: Active and reactive power with reference to variation in reactive power reference

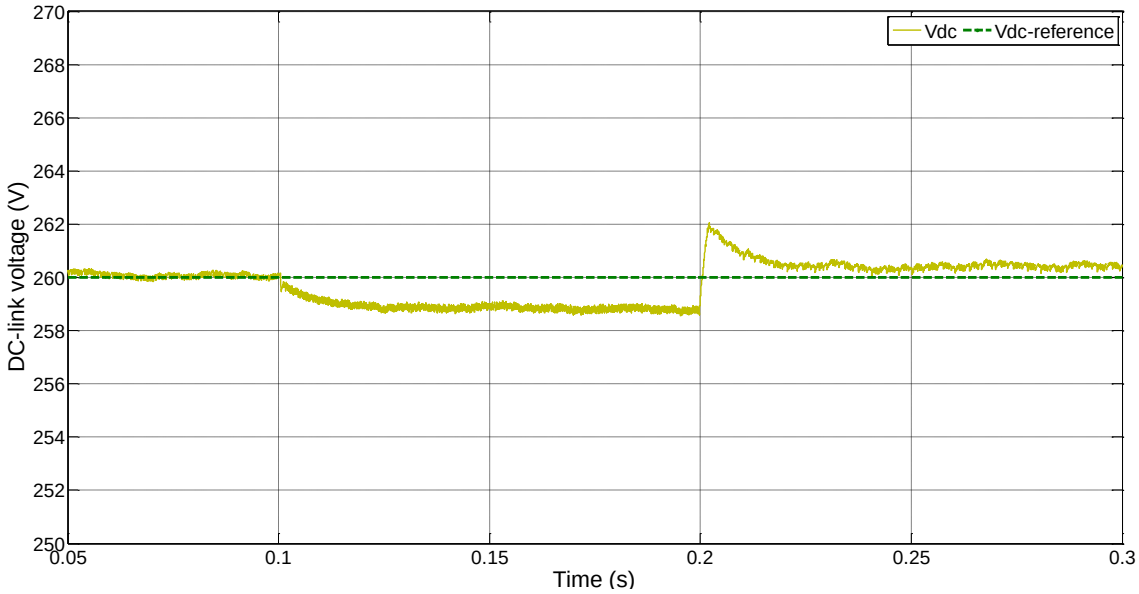


Figure 5.9: DC-Link voltage to variation in reactive power reference

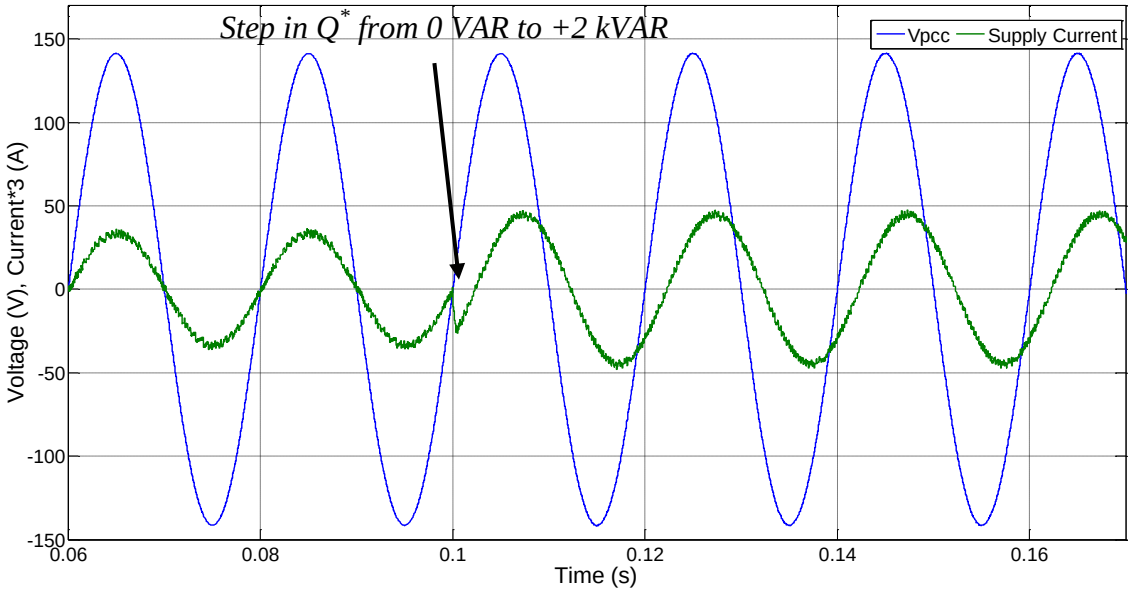


Figure 5.10: Supply current and Grid Voltage before step in reactive power reference from 0VAR to +2kVAR

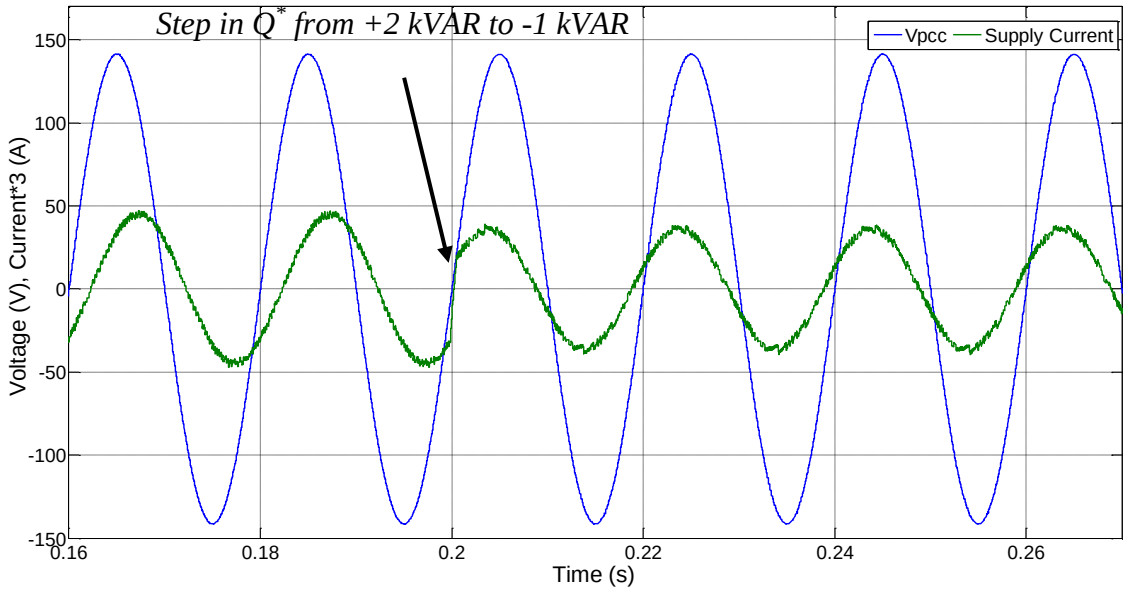


Figure 5.11: Supply current and Grid Voltage after step in reactive power reference from 2 kVAR to -1 kVAR

Therefore, it can be concluded that the MP-DPC responds accurately to variations in reactive power.

5.3.5. Effect on MP-DPC with Grid inductance variation

The presence of grid impedance with a substantial value compared to the converter input impedance as shown in figure 5.12, if not compensated in the predictive control, can cause problems to the control performance. According to the literature review in chapter 2, the grid impedance is mostly considered inductive. As depicted in figure 5.13 showing the PCC voltage and supply current, a value of L_S=10%L_C (where the SCR is greater than 15) results in a significant disturbance to the control.

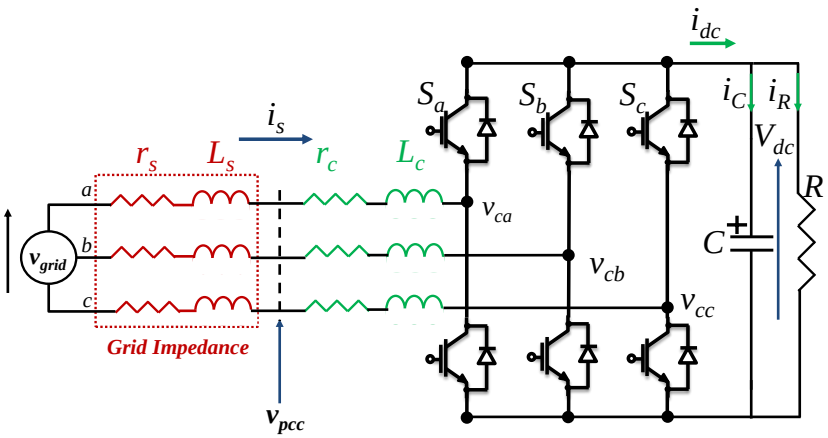


Figure 5.12: Grid connected converter with supply impedance

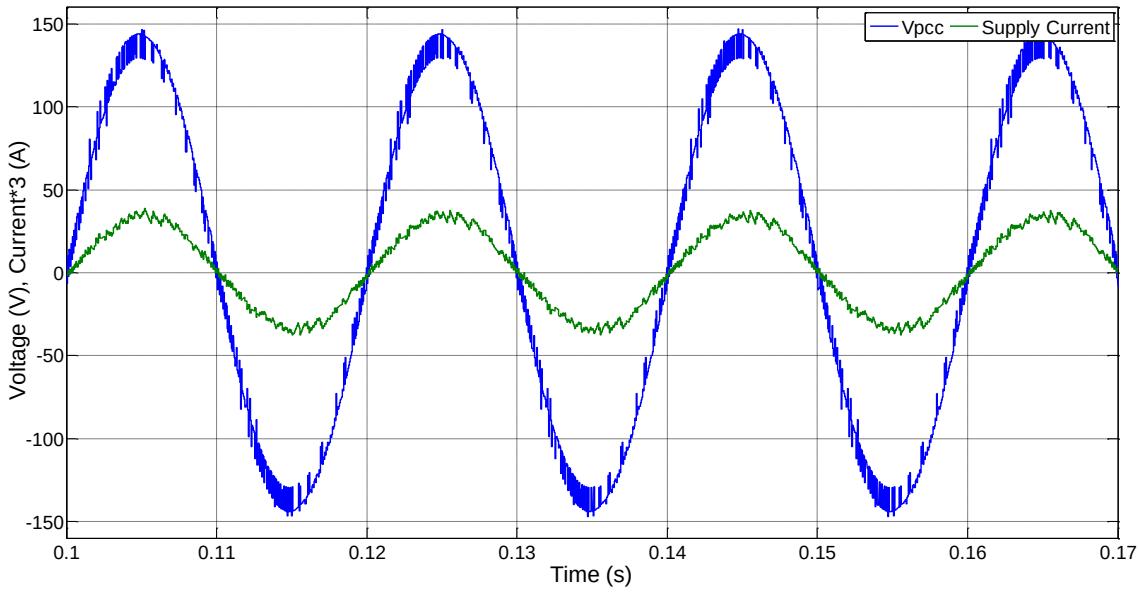


Figure 5.13: Supply current and Grid Voltage with L_S= 10%L_C without grid impedance compensation. THD_i = 7.6%, THD_{Vpcc} = 5.9%

Figure 5.14 shows the response of active and reactive powers with respect to their references for a 10% variation in grid impedance when this is not compensated. As can be observed, due an increase in the ripple and higher THD of supply current and PCC voltage, the ripple on the active and reactive powers also increase.

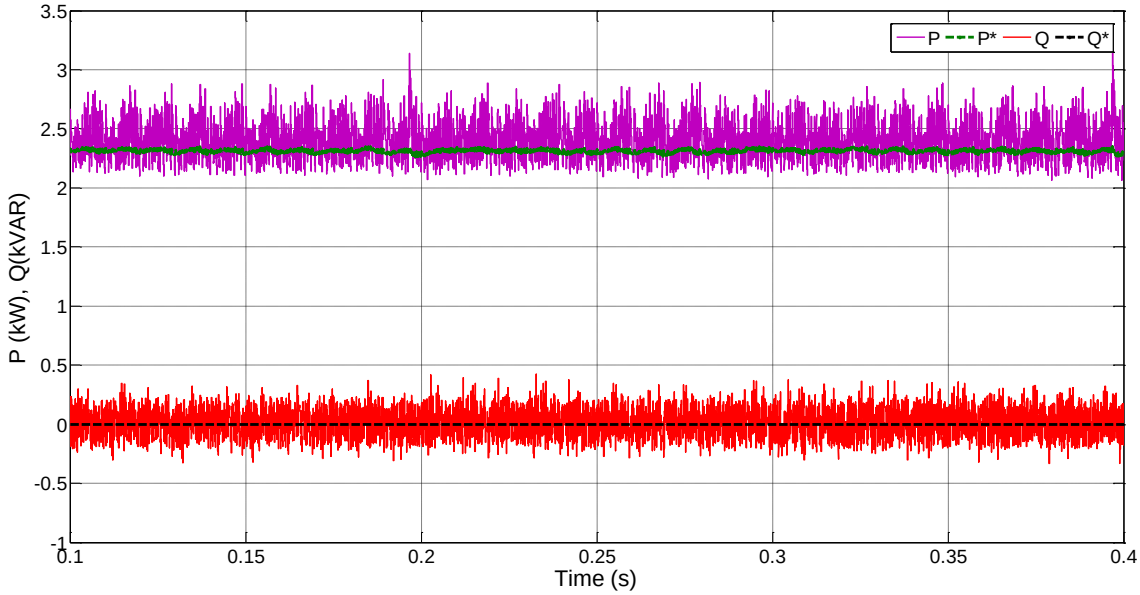


Figure 5.14: Corresponding active and reactive powers for L_S= 10%L_C

In figure 5.15, a steady state error can be observed in the dc-link voltage for supply inductance equal to 10% of L_C. This is due to inaccurate calculations of supply current predictions as the model inductance value is not correct. The dc-link voltage calculations depend on current predictions as shown in sections 4.2.3 and 4.2.4, thus, an incorrect calculation affects the dc-link voltage control.

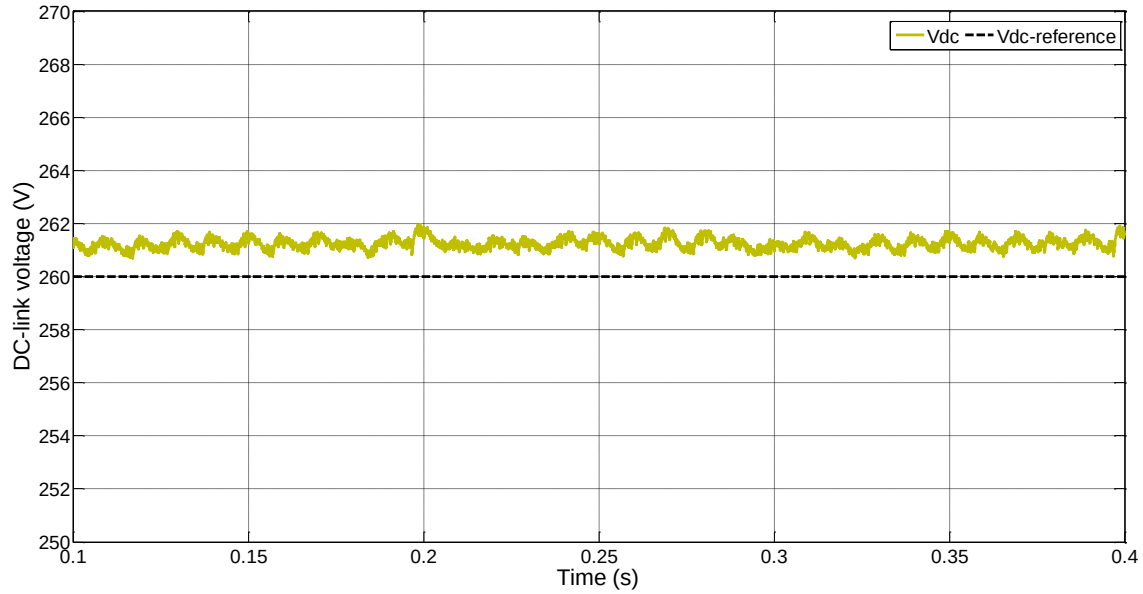


Figure 5.15: Corresponding DC-link voltage for L_S= 10%L_C

For L_S=30%L_C, as shown in figures 5.16-5.18, the predictive control performance further deteriorates giving a very low quality response and supply current THD greater than 20%.

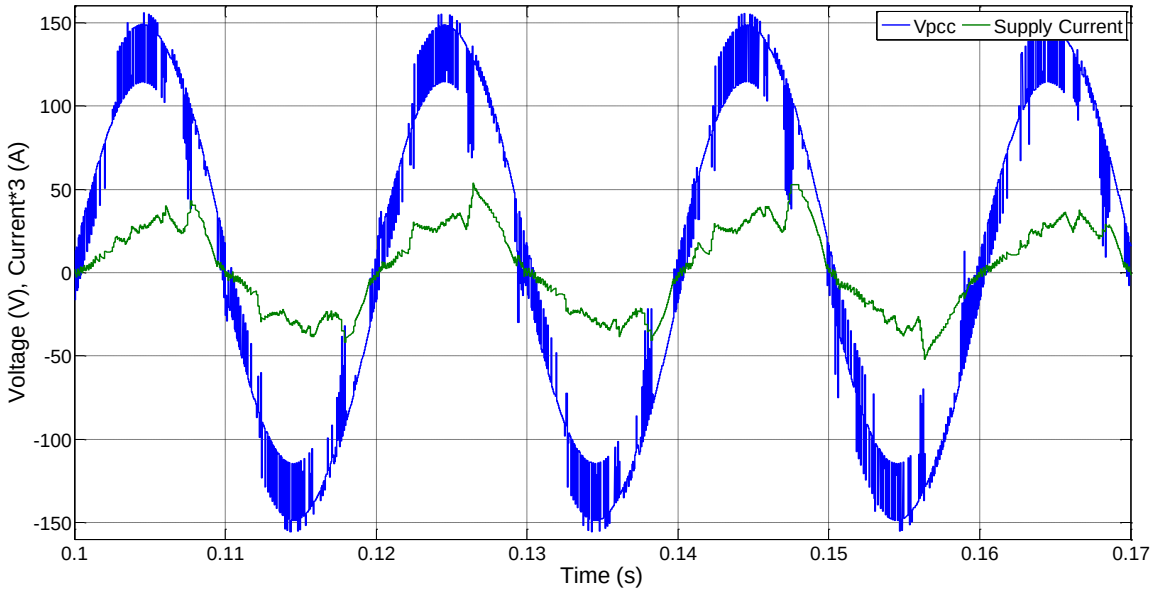


Figure 5.16: Supply current and Grid Voltage with L_S= 30%L_C without estimation. THD_i = 24.36%, THD_{Vpcc} = 16.17%

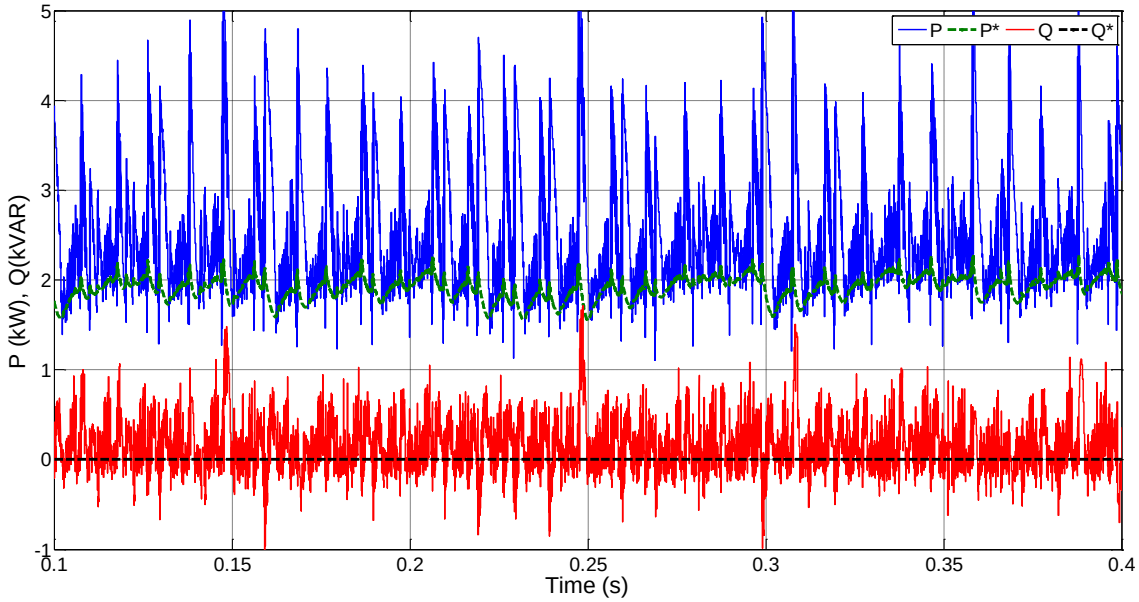


Figure 5.17: Corresponding active and reactive powers for L_S= 30%L_C

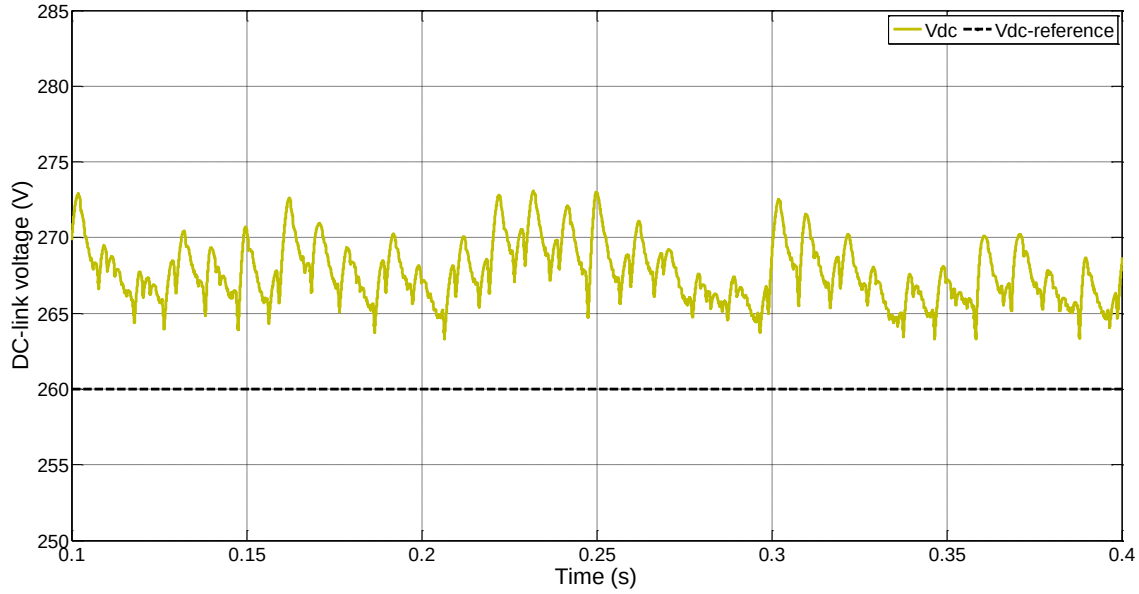


Figure 5.18: Corresponding DC-link voltage for L_S= 30%L_C

Therefore, it becomes of utmost importance to compensate for the variation in grid inductance to provide a robust and accurate performance to the predictive controller.

5.4. Predictive Direct Power Control with presence and online estimation of Grid inductance

5.4.1. Online estimation using Method 1

The results in this section present the estimation of the total inductance (line and converter) using Method 1, as proposed in section 4.4.2 of Chapter 4, that is integrated within the model based predictive controller such that the predictive controller is updated in real-time. Figures 5.19-5.22 show results for grid inductance values from 10% to 100% of the converter inductance value. The results show that, according to section 4.4.2.2, the grid voltage is estimated accurately showing a quasi-sinusoidal waveform for a correct estimation of grid inductance without showing any significant distortions.

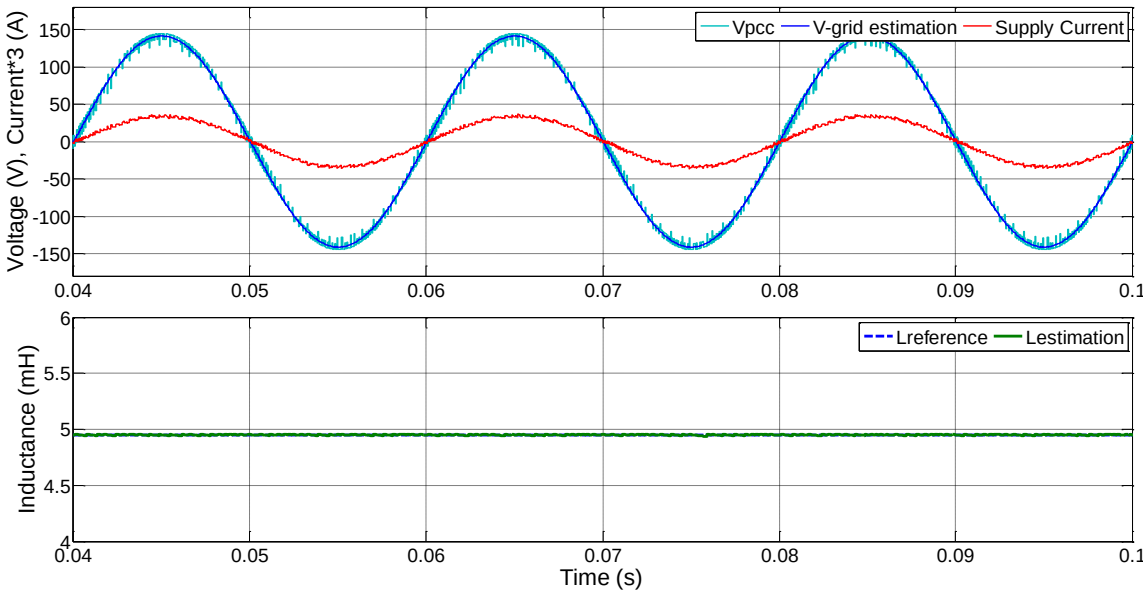


Figure 5.19: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 10%L_C value (i.e. L_S = 0.45mH) as compared to L_C. THD_{Vpcc}=5.56%, $THD_{Vg\text{-}est}$=0.51%, THD_i=5.52%

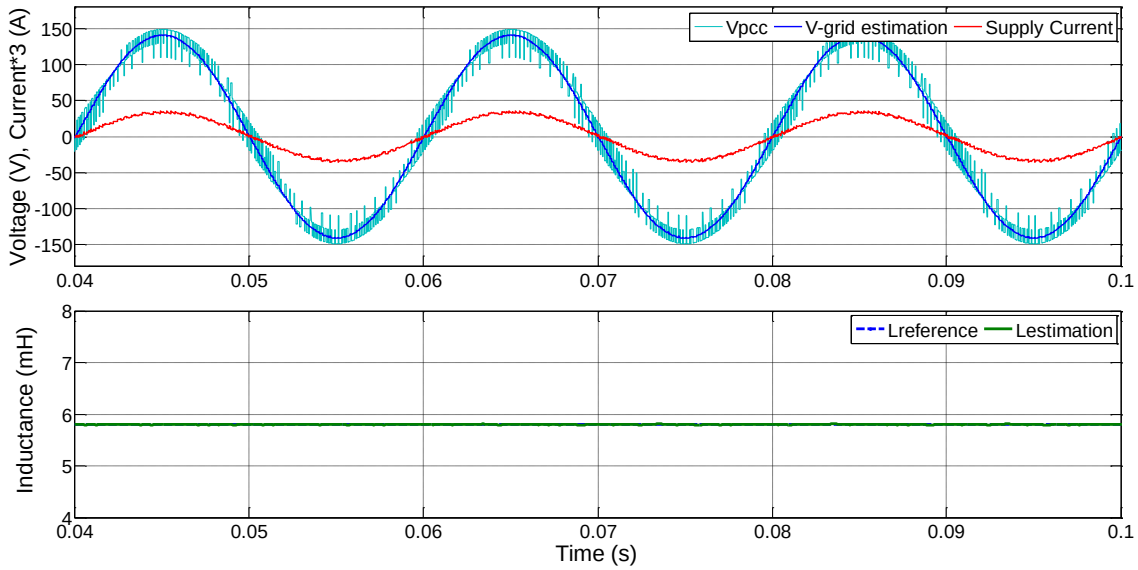


Figure 5.20: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 30%L_C (i.e. L_S = 1.35mH) as compared to L_C. THD_{Vpcc}=13.7%, $THD_{Vg\text{-}est}$=0.73%, THD_i=4.82%

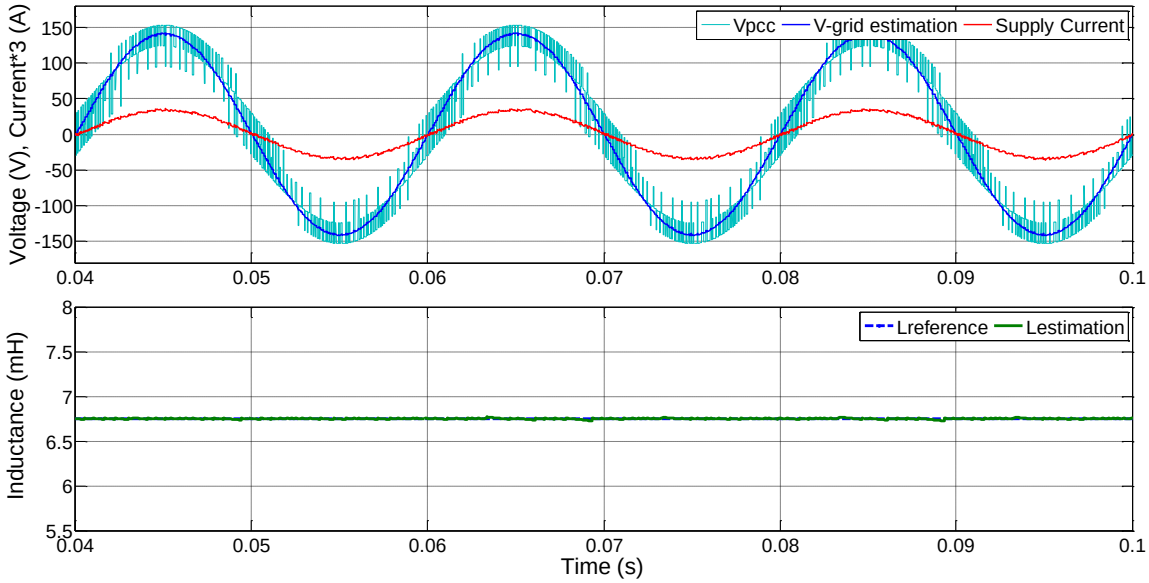


Figure 5.21: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 50%L_C (i.e. L_S = 2.25mH) as compared to L_C. THD_{Vpcc}=21%, $THD_{Vg\text{-}est}$=1.0%, THD_i=4.15%

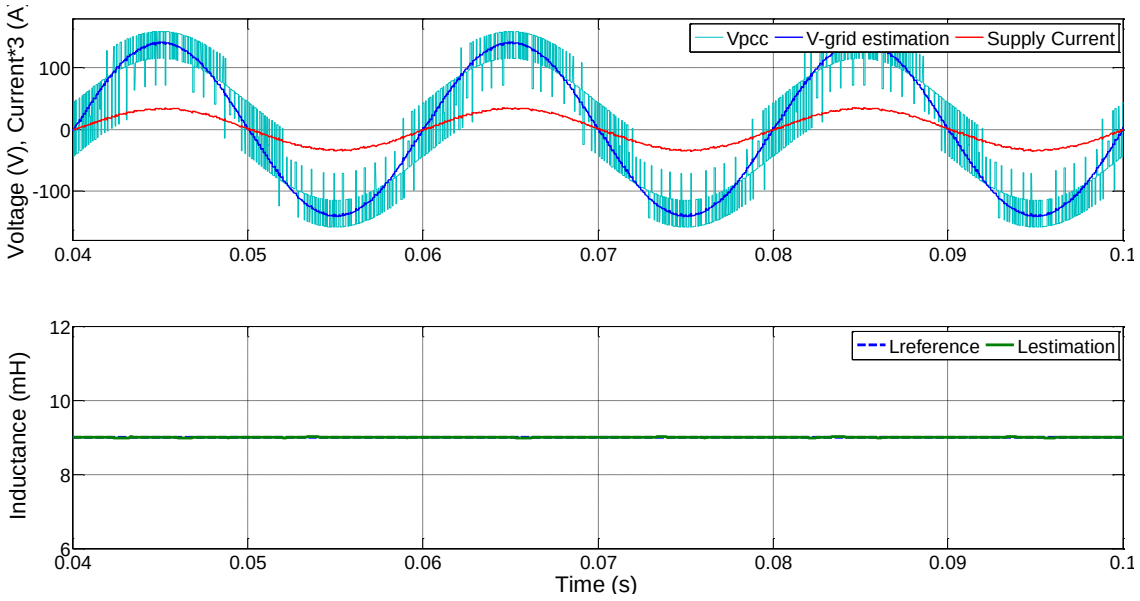


Figure 5.22: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 100%L_C (i.e. L_S = 4.5mH) as compared to L_C. THD_{Vpcc}=30.9%, $THD_{Vg\text{-}est}$=1.4%, THD_i=3.2%

The supply current remains sinusoidal and maintains a THD value less than 4% when the grid inductance is 100% of L_C. The THD values for supply current (i_S), PCC voltage (v_{pcc}) and estimated grid voltage ($v_{g\text{-}est}$) are presented for each L_S case in the respective figures captions as well.

Table 5.2 shows a comparison in the THD values for the 4 respective cases presented in figures 5.19-5.22 when L_S has been tested for 10%, 30%, 50% and 100% as compared to the L_C value. Since the grid inductance is accurately estimated and is used to update the total line inductance value in the predictive controller, as expected, the supply current THD shows a decreasing trend. However, a higher distortion in v_{pcc} as the L_S increases leads to a higher distortion on the estimation of grid voltage as can be seen from the grid voltage THD value for the four respective presented cases.

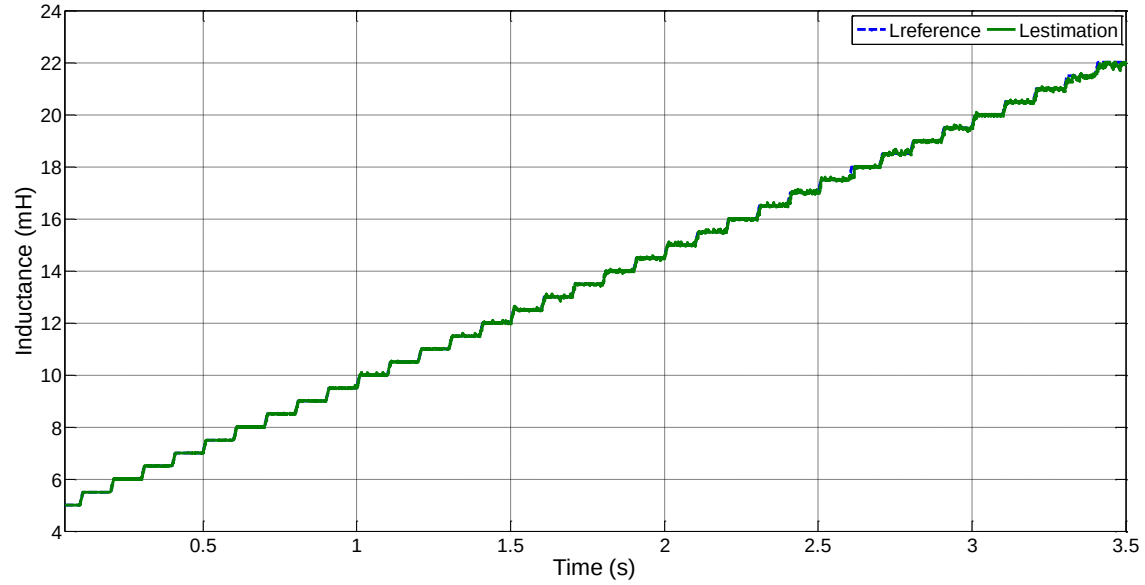
Table 5.2: Comparison of THD values for different variations in L_S

SCR	L_S (mH)	THD_i (%)	THD_{vpcc} (%)	$THD_{vg\text{-}est}$ (%)
88	0.45	5.52	5.56	0.51
30	1.35	4.82	13.7	0.73
18	2.25	4.15	21	1.0
9	4.5	3.2	30.9	1.4
4	9.0	2.87	42.5	1.89
2	17.5	2.53	43	2.05

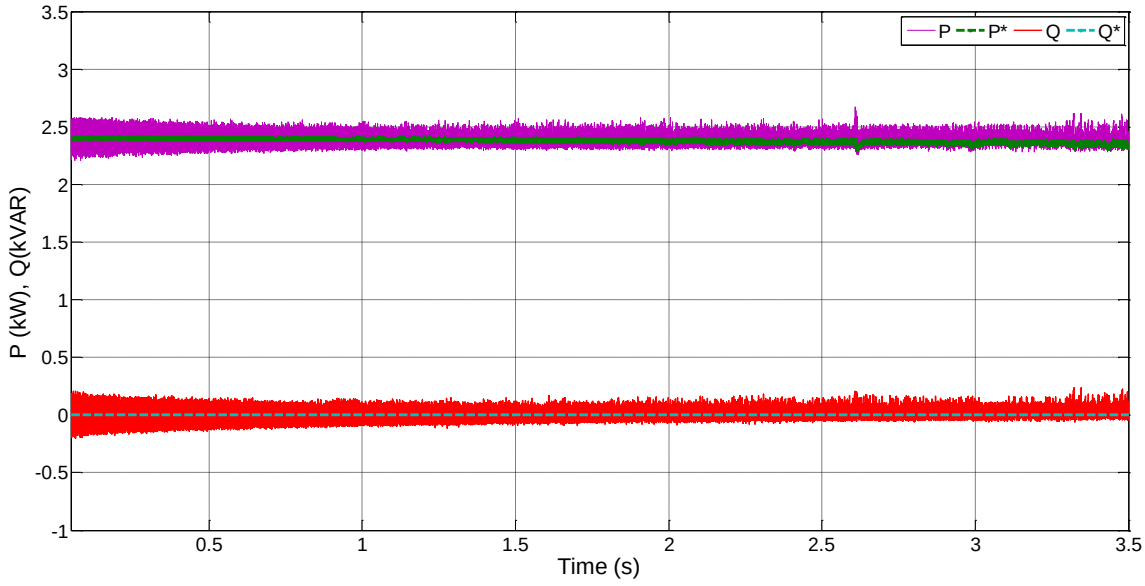
On the other hand, figure 5.23(a) shows the response of the total inductance estimation algorithm to a frequent step variation in the value of grid inductance. The L_S has been varied from 0.5mH (SCR > 20) to ~17.5mH (SCR < 3) while the converter input filter inductance L_C is kept at 4.5mH. As can be observed, hardly any significant steady state error appears and the total inductance estimation shows a fast response to the frequent variation. The method for calculating SCR values are shown in Appendix A.

The active and reactive powers, in figure 5.23 (b), follow their respective references for the frequent step variation in grid inductance from 0.5mH to 17.5mH. Since the ripple on the supply current reduces as the total line inductance increases, reduction in active power and reactive power ripples can also be seen.

Results in figures 5.24 and 5.25 show the total inductance estimation, supply current, PCC voltage and grid voltage estimation when L_S has a value of 200% and ~400% as compared to L_C. Even for such large values of L_S, the estimator and the predictive control performance do not get disturbed - resulting in supply current THD less than 3%.



(a)



(b)

Figure 5.23: (a) Total Inductance estimation with a frequent variation in grid inductance, (b) Active and reactive power response to a frequent variation in grid inductance

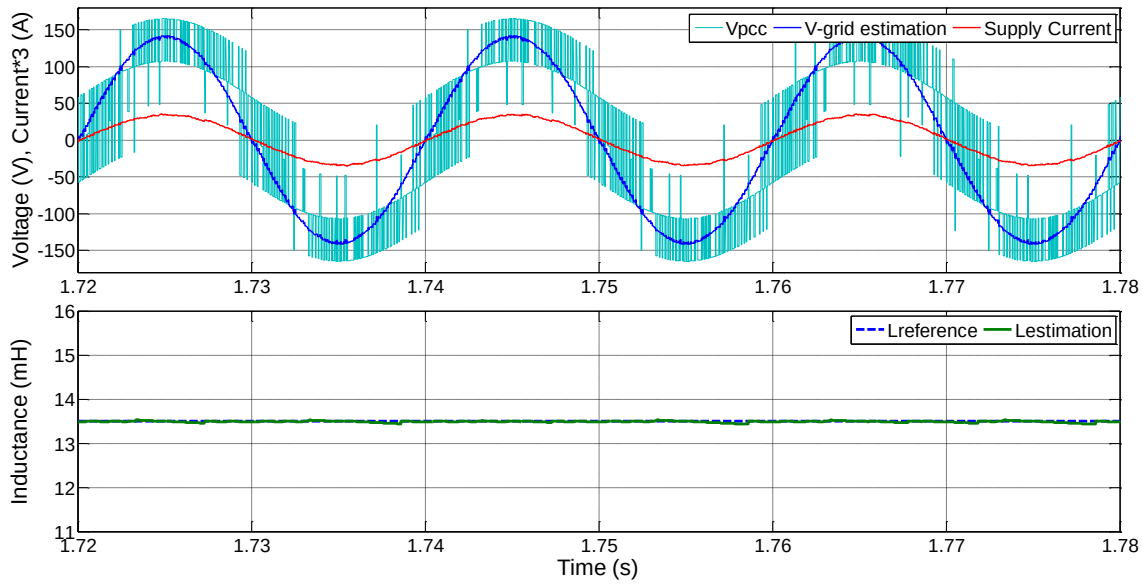


Figure 5.24: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= 200%L_C (L_S = 9mH) as compared to L_C. THD_{Vpcc}=42.5%, $THD_{Vg\text{-}est}$=1.89%, THD_i=2.87%

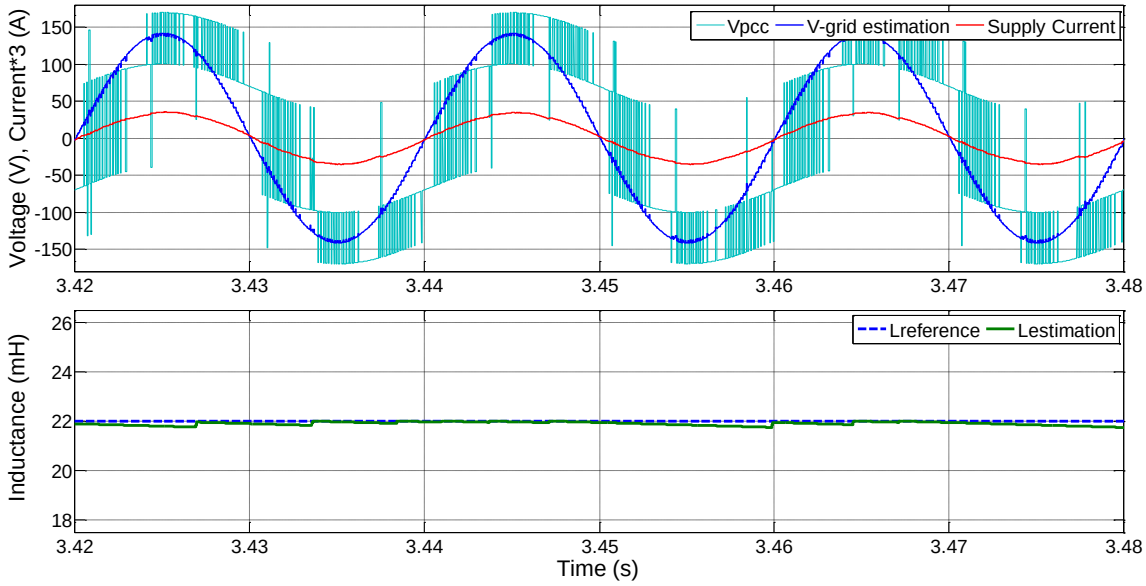


Figure 5.25: Supply current, PCC voltage, Grid Voltage estimation and total inductance estimation with L_S= ~400%L_C (i.e. L_S = 17.5mH) as compared to L_C. THD_{Vpcc}=43%, $THD_{Vg\text{-}est}$=2.05%, THD_i=2.53%

Table 5.3 shows a comparison of the Short Circuit Ratio (SCR) value to a variation in L_S, calculated as shown in Appendix A. For a high value of L_S, the SCR decreases. Figure 5.26 shows the SCR values for all the operating points for L_S considered in figure

5.23. A weak grid with SCR less than 5 can introduce significant problems to the performance of the predictive control, thus fast estimation of the grid inductance and its integration within the predictive control makes the proposed method suitable to be applied in weak grid scenarios.

Table 5.3: SCR for different values of L_S

L_C (mH)	L_S (mH)	Z_S (Ω)	SCP(kVA)	S_{BASE}(kW)	SCR
4.5	2.0	0.628	47.77	2.4	19.9
4.5	4.0	1.257	23.87	2.4	9.95
4.5	6.0	1.885	15.92	2.4	6.63
4.5	8.0	2.513	11.94	2.4	4.98
4.5	10.0	3.142	9.548	2.4	3.98
4.5	12.0	3.77	7.958	2.4	**3.32**
4.5	14.0	4.398	6.821	2.4	**2.84**
4.5	16.0	5.027	5.968	2.4	**2.49**
4.5	18.0	5.655	5.305	2.4	**2.21**

Weak Grid

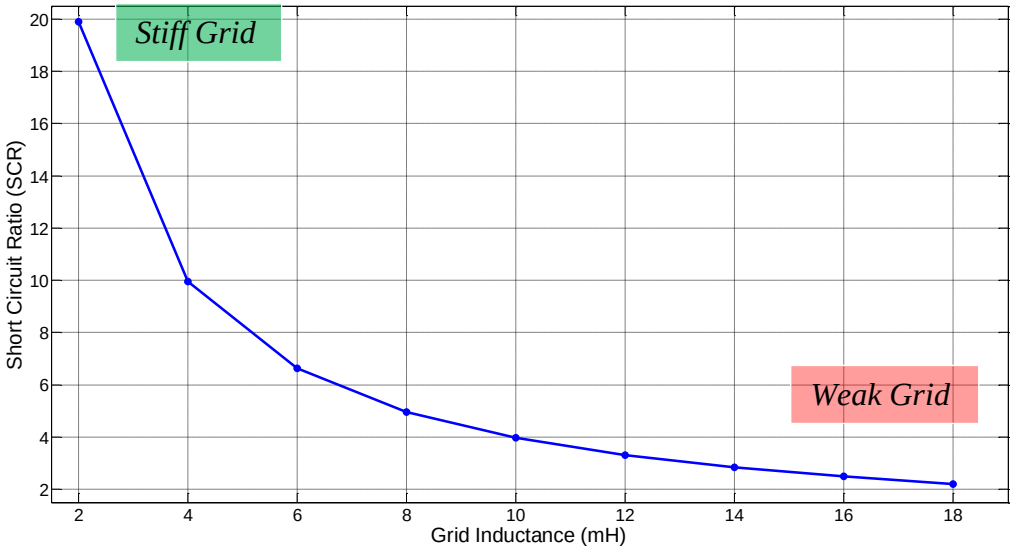


Figure 5.26: Short Circuit Ratio to grid inductance comparison

5.4.2. Online inductance estimation for a step in reactive power

Figure 5.27 shows the adaptability and performance of the inductance estimator to a variation in reactive power from 0VAR to 1 kVAR to 0.5 kVAR and back to 0VAR for L_S=13.5mH. The power factor is, hence, varied from approximately unity to 0.923 to 0.979 and back to unity. The predictive controller performs well by maintaining the active and reactive powers along their respective reference values and so does the inductance estimator.

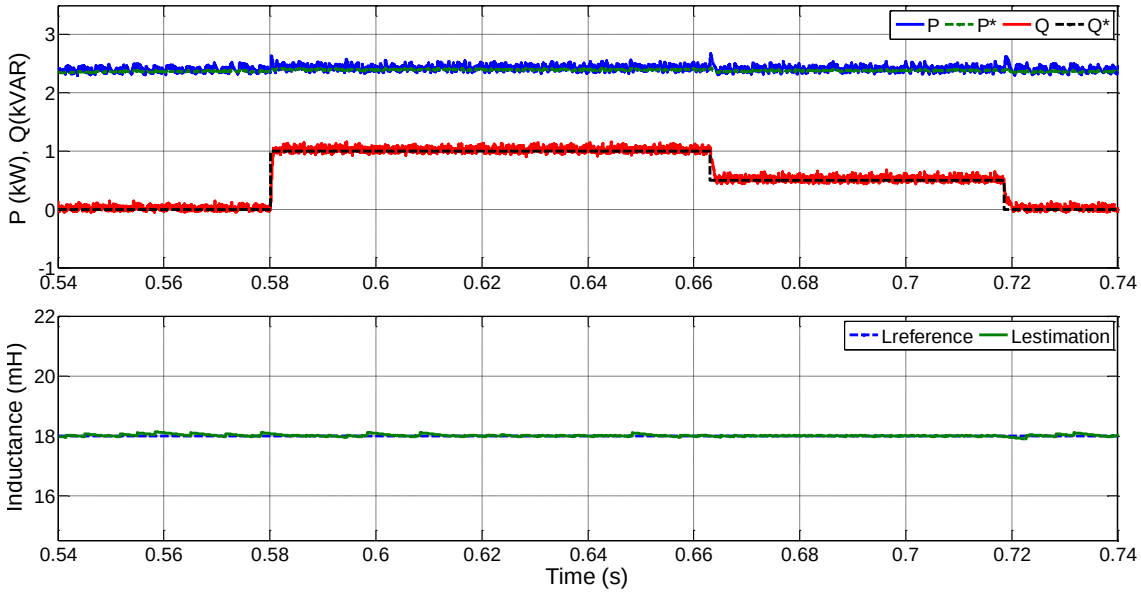


Figure 5.27: Active and Reactive powers with steps in reactive power reference and estimated total inductance with L_S= 300%L_C (i.e. L_S = 13.5mH) to L_C

Figure 5.28 presents the supply current, PCC voltage and the grid voltage estimation for L_S= *300%*L_C when a step of 1 kVAR in reactive power happens at t=0.58s. A leading current phase shift as compared to the grid voltage can be observed.

It is important to talk about the high distortion present on the v_{pcc}. The reason for a high distortion on v_{pcc} for a high L_S value is because of a higher distorted voltage drop across

the grid inductance. This is depicted in equation (5.2) referring to figure 5.12 in case of a purely inductive grid impedance:

$$v_{pcc}(t) = v_{grid}(t) - L_S \frac{di_S(t)}{dt} \tag{5.2}$$

Where, the PCC voltage gets distorted because of a higher voltage drop on $L_S \frac{di_S(t)}{dt}$ which is higher due to a higher value in L_S.

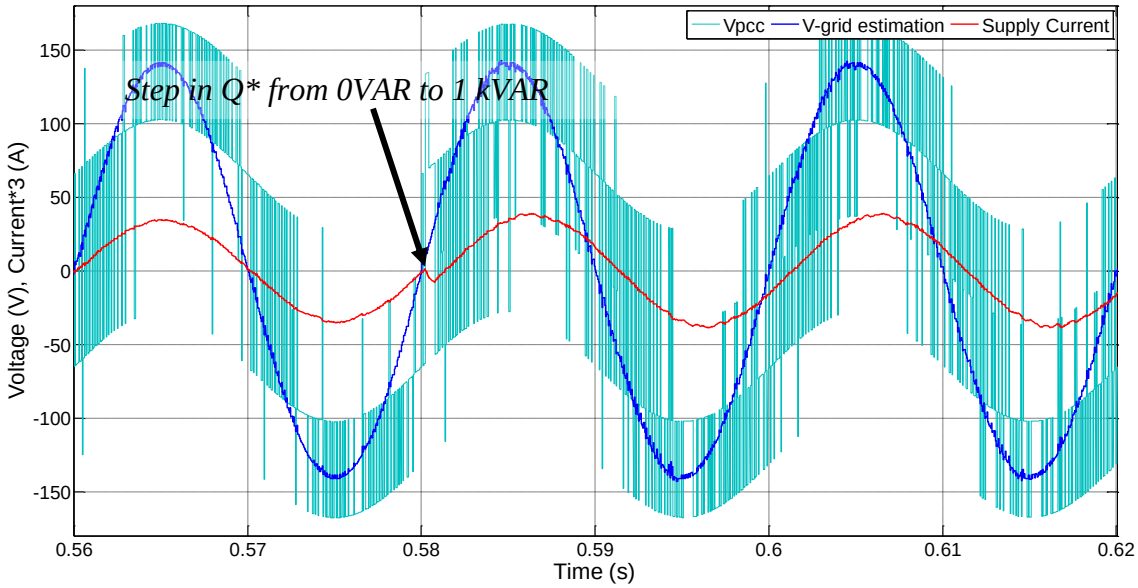


Figure 5.28: Supply current, PCC voltage, grid Voltage estimation with L_S= 300%L_C (13.5mH) as compared to L_C and step in reactive power reference

Moreover, even if the fundamental of the v_{pcc} is used in the predictive controller, the significant delay introduced would be difficult to compensate since the delay may not remain consistent for different values of L_S. Therefore, under these circumstances, it is best to estimate the grid voltage that maintains the phase synchronization with the supply current unless a phase shift is deliberately demanded by increasing or decreasing the reactive power reference value.

5.4.3. Online estimation for a large variation in grid inductance

It is important to monitor the performance of the inductance estimator and the predictive controller to a sudden large variation in L_S. Therefore, figure 5.29 show results for inductance estimation, supply current, PCC voltage and grid voltage estimation for a step of 3.0mH in L_S.

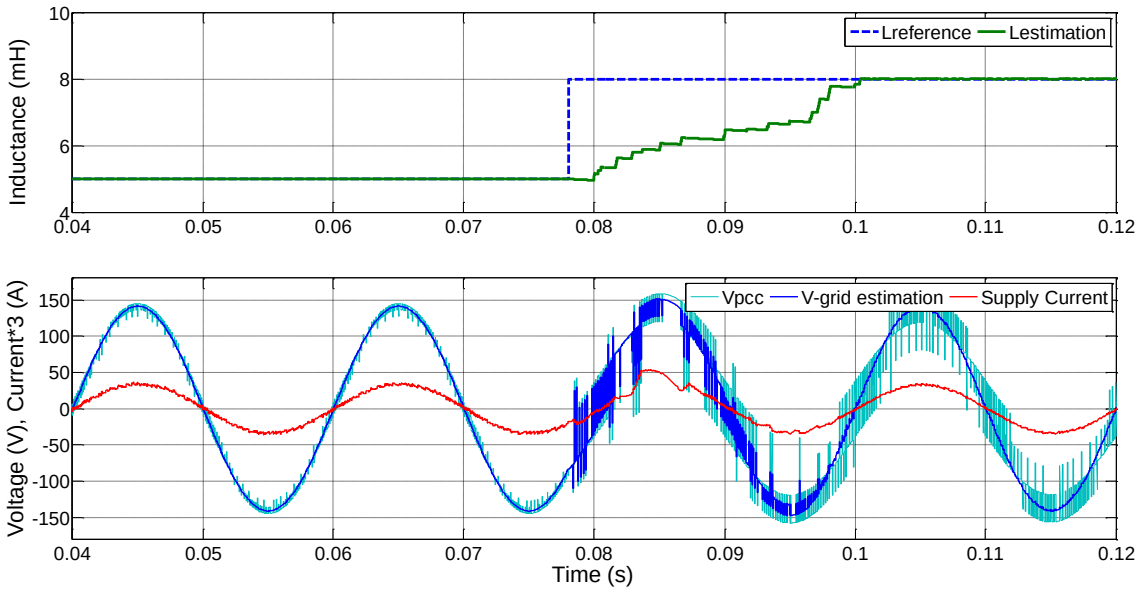


Figure 5.29: Total Inductance estimation, supply current, PCC voltage, and grid voltage estimation with 67% step in L_S value (L_S = 0.5mH to 3.0mH)

From time 0.04s to 0.07s the L_S is 0.5mH giving a supply current THD 5.77%, v_{pcc} THD 6.3% and estimated grid voltage THD 0.5%. However, at ~0.08s a step of 3.0mH is introduced in L_S which greatly disturbs the control performance giving a supply current THD 21.5%, estimated grid voltage THD 18.8% for a v_{pcc} THD 34.7%. Due to the fast response of the estimator, at 0.1s the correct value is accurately estimated after taking approximately one fundamental cycle and greatly improves the supply current THD to 3.6%, estimated grid voltage THD to 1.3% when v_{pcc} THD is 27.1%.

5.4.4. Online estimation and presence of Dead-Time for converter switches

This section briefly talks about the effect of dead-time on the total inductance estimation techniques. The dead-time has been compensated as explained in section 4.3 of chapter 4. Figure 5.30 shows the results of total inductance estimation for a step variation in grid inductance equal to 66.67% of the value of L_C for cases with and without the dead-time compensation. In the figure, 'Lestimation with DT comp.' refers to the estimation of total inductance with dead-time compensation integrated within the MP-DPC while 'Lestimation without DT comp.' refers to total inductance estimation without dead-time compensation. A steady state error of ~0.2mH ~0.4mH can be observed when dead-time is not compensated, whereas when the dead-time is compensated hardly any steady state error can be seen. The reason why dead-time compensation becomes important is due to the inclusion in the inductance estimation algorithm of converter voltages that are dependent on the converter switching signals.

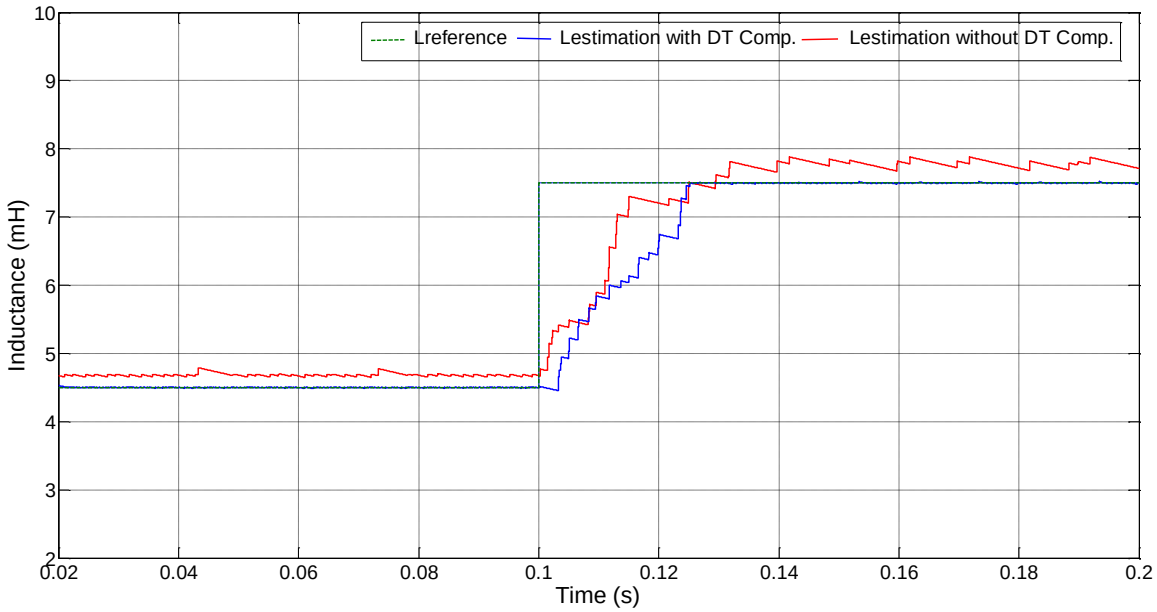


Figure 5.30: Comparison of total inductance estimation with and without the dead-time compensation

Therefore, any delay in the switching signals or converter voltage drop caused by dead-time, if not compensated, can introduce errors to the proposed estimation method. In figure 5.30, the grid inductance L_S is varied from 0mH to 3.0mH while the converter input filter inductance L_C is 4.5mH.

5.4.5. Online estimation in the presence of a grid capacitance

Results in figure 5.32 show the inductance estimation performance in case of a presence of grid capacitance, for an equivalent grid model of figure 5.31. In reality the value of grid capacitance is quite negligible, however, in order to check the robustness of the proposed total inductance estimation, a high value of grid capacitance (100µF) has been used with a step in grid inductance L_S from 0mH to 3.0mH. Despite such a significant presence of grid capacitance, the estimation is not affected and gives a correct total estimation value around 4.5mH in case of 0mH grid inductance and 7.5mH in case of 3.0mH grid inductance without any significant steady state errors, thus showing the robustness of the proposed estimation algorithm.

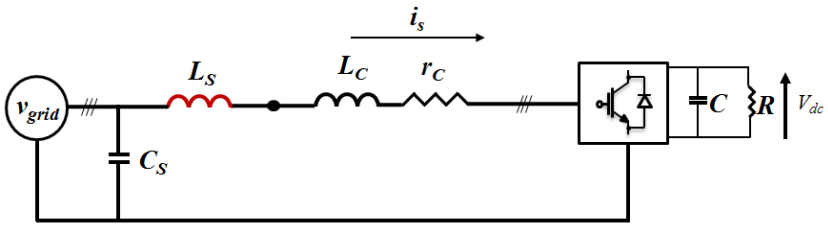


Figure 5.31: Equivalent model with grid capacitance

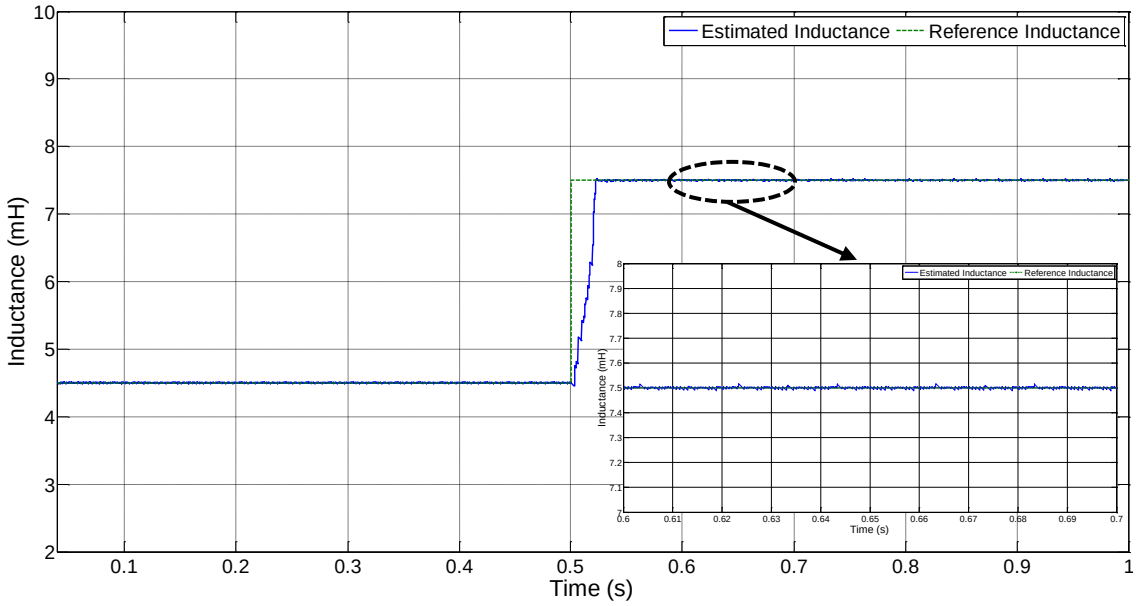
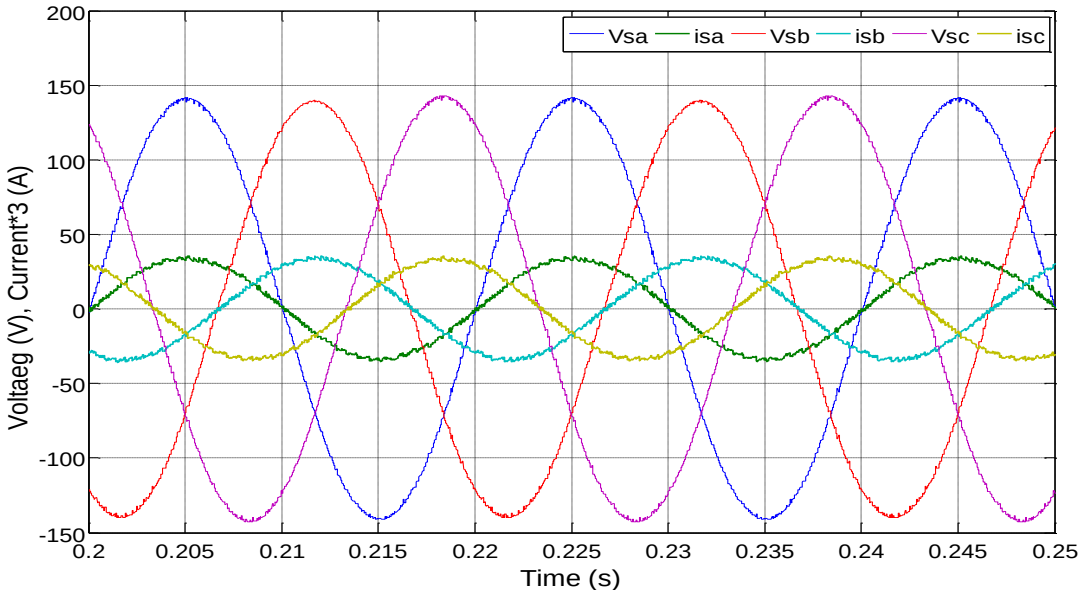


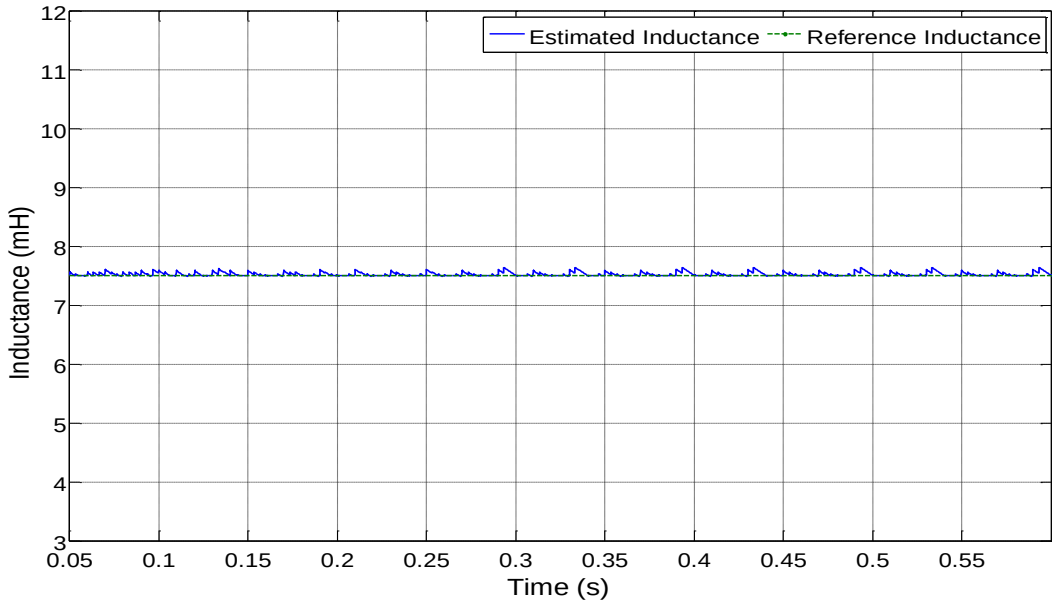
Figure 5.32: Total inductance estimation with a presence of 100µF grid capacitance

5.4.6. Online estimation with unbalanced grid voltages

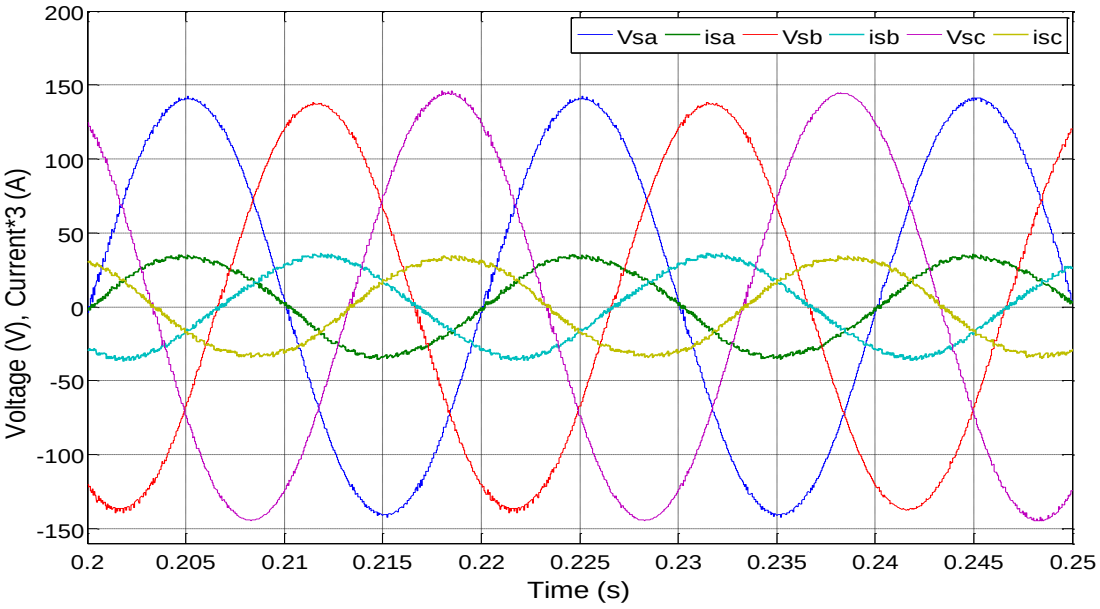
The results presented in the above sections are all based on a balanced grid voltage condition. However, it becomes important to observe the response of estimation method 1 in case there is grid voltage unbalance as presented in figure 5. The presented results are shown for 3 cases of grid voltage unbalance, i.e. when phases *b* and *c* have 2%, 5% and 10% amplitude variation with respect to phase *a*. The presented results also show the respective supply currents for each phase and the estimated total inductance in each test condition.


Vsa
isa
Vsb
isb
Vsc
isc
Voltaeg (V), Current*3 (A)
Time (s)
200
150
100
50
0
-50
-100
-150
0.2
0.205
0.21
0.215
0.22
0.225
0.23
0.235
0.24
0.245
0.25

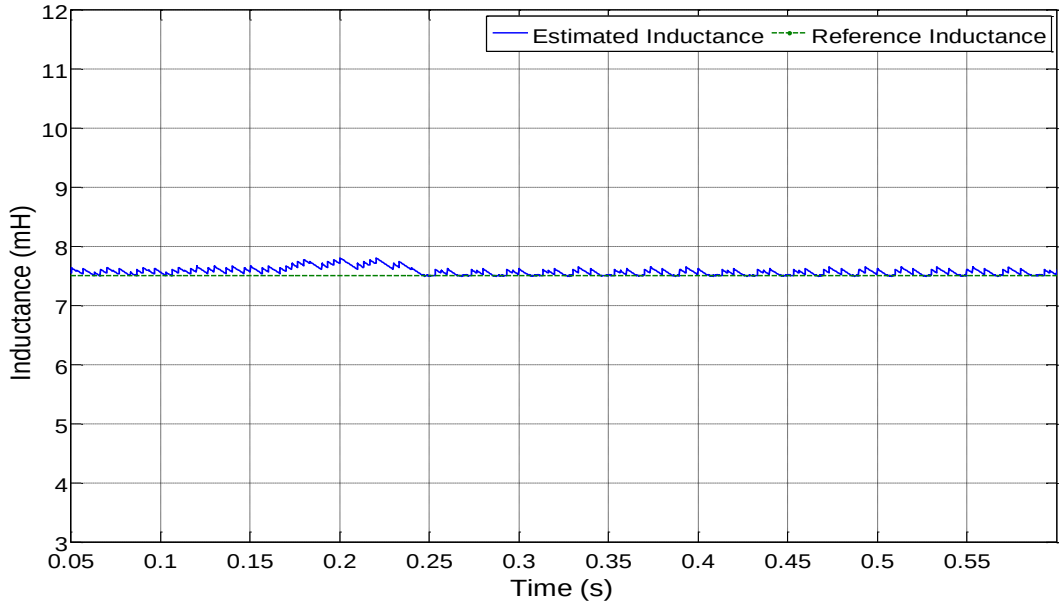
(a1)


Estimated Inductance
Reference Inductance
Inductance (mH)
Time (s)
12
11
10
9
8
7
6
5
4
3
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55

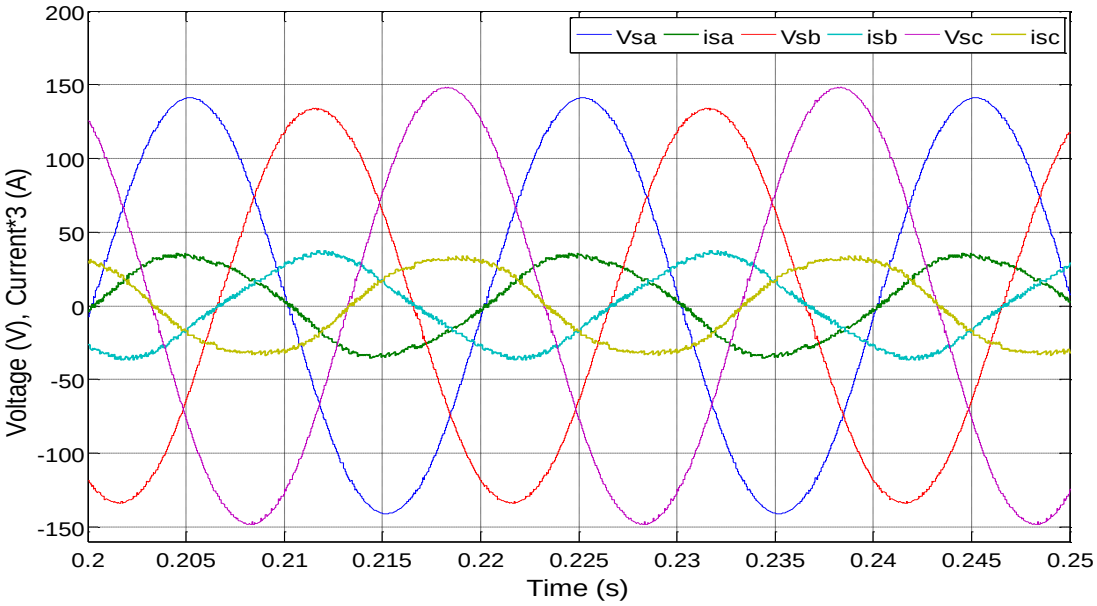
(a2)


Vsa
isa
Vsb
isb
Vsc
isc
Voltage (V), Current*3 (A)
Time (s)
200
150
100
50
0
-50
-100
-150
0.2
0.205
0.21
0.215
0.22
0.225
0.23
0.235
0.24
0.245
0.25

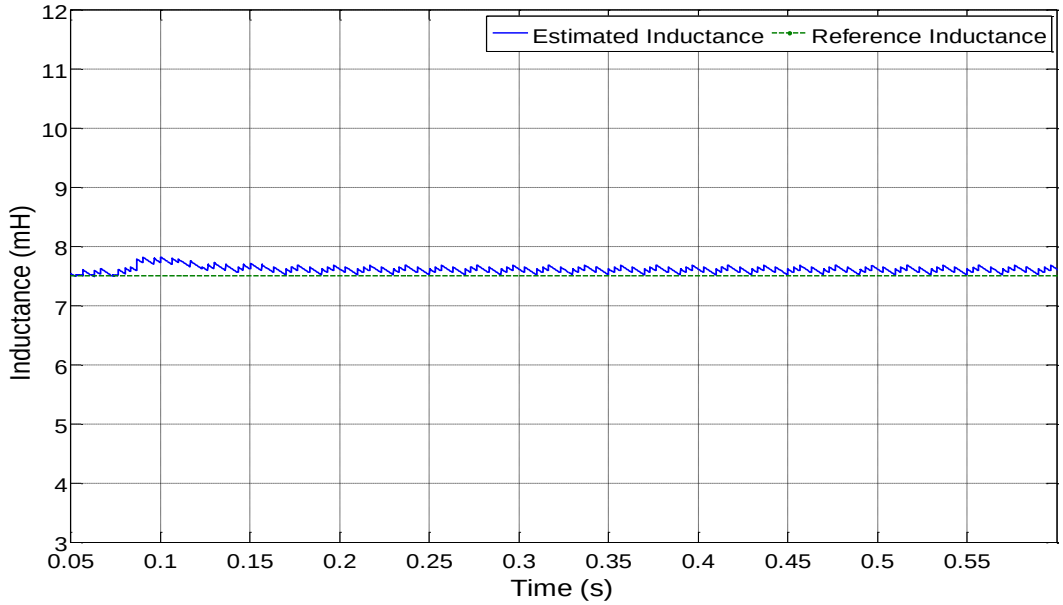
(b1)


Estimated Inductance
Reference Inductance
Inductance (mH)
Time (s)
12
11
10
9
8
7
6
5
4
3
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55

(b2)



(c1)



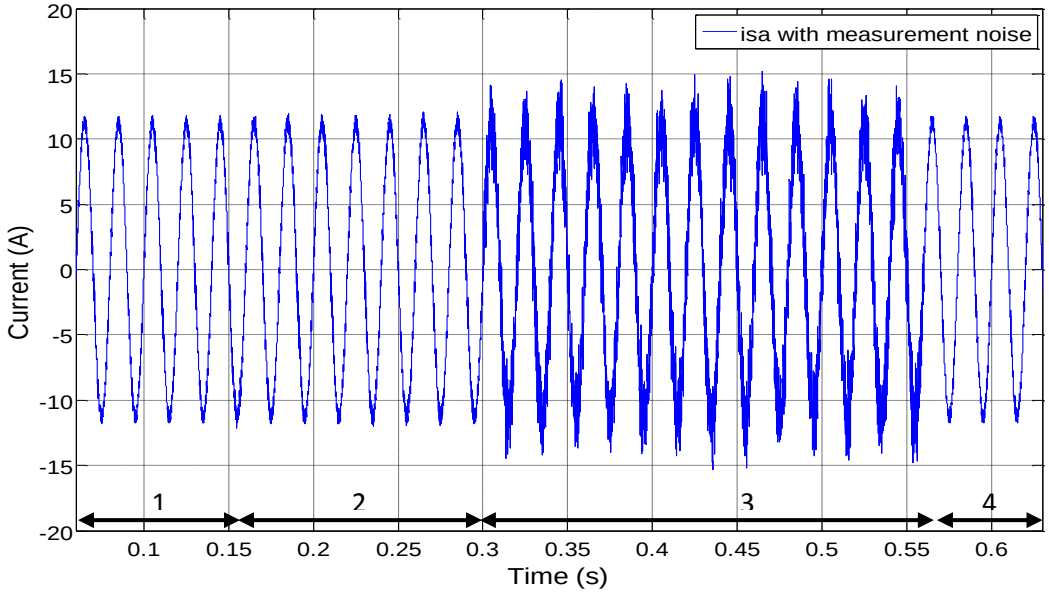
(c2)

Figure 5.33: (a1) 2% unbalance grid voltages with respective supply currents, (a2) Total estimated inductance to 2% grid voltage unbalance. (b1) 5% unbalance grid voltages with respective supply currents, (b2) Total estimated inductance to 5% grid voltage unbalance. (c1) 10% unbalance grid voltages with respective supply currents, (c2) Total estimated inductance to 10% grid voltage unbalance

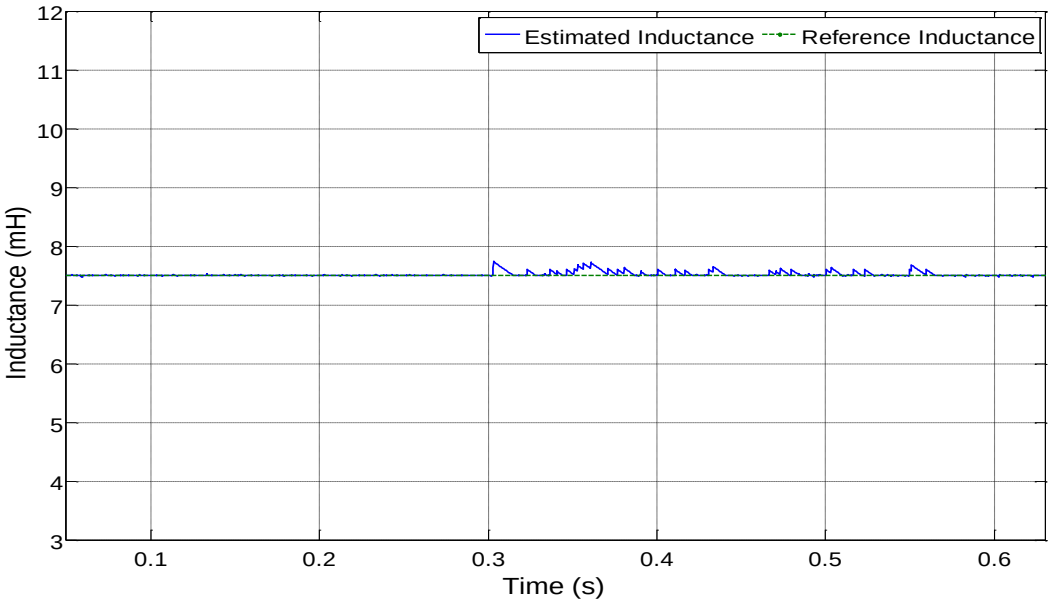
As the grid voltage unbalance increased, it was observed that the steady state error on the total estimated inductance also increased. This is due to the assumption made in derivation of algorithm that states a constant grid voltage magnitude between two consecutive sampling instants. Also, since the unbalanced grid voltages were not compensated in the control process, this affected the control performance and resulted in supply current THD of 3.9%, 4.93% and 6.7%, respectively, for the three test conditions.

5.4.7. Effect of measurement noise

The results presented in this section show the effect of measurement noise on the estimation algorithm. The effect of measurement noise was introduced in controller measurements by using a Band-Limited White Noise Block in Matlab Simulink. As the noise intensity was increased, the supply current THD increased and the total inductance estimation was affected as well. The noise was varied in 4 steps as can be seen in figure 5.34(a) that shows the current waveform.



(a)



(b)

Figure 5.34: Estimation Method 1 (a) Effect of noise on measured supply current, (b) Total estimated inductance in presence of noise

Table 5.4 shows the effect on supply current THD or 4 difference noise values arbitrarily used in the Matlab Noise block.

Table 5.4: Estimation Method 1 - Effect of measurement noise on supply current THD

	Noise Intensity in Matlab Block	**THD_i**
1	$1e^{-9}$	3.4%
2	$1e^{-7}$	3.7%
3	$1e^{-4}$	17.6%
4	$1e^{-9}$	3.4%

With reference to table 5.4 and figure 5.34, the peak-peak ripple amplitude on supply current in case of test condition 1 of measurement noise was 0.7A while in case of test condition 3 the peak-peak ripple amplitude increased to 7A.

5.5. Model based Predictive Direct Power Control with online predictive model fitting algorithm for online grid inductance estimation

5.5.1. Online estimation using Method 2

This section presents the test results for the estimation method proposed and explained in section 4.4.3 of chapter 4. This approach estimates the variation in grid inductance, as opposed to total inductance estimation in method 1, based on a "cost-function optimization" criterion as explained in section 4.4.3. Similar to the estimation method 1, the estimated grid inductance in method 2 is used to update the model inductance value in the MP-DPC.

Figures 5.35 and 5.36 show results for the estimated grid inductance, supply current, PCC voltage and grid voltage estimation for $L_S=50\%L_C$ and $L_S=100\%L_C$, respectively.

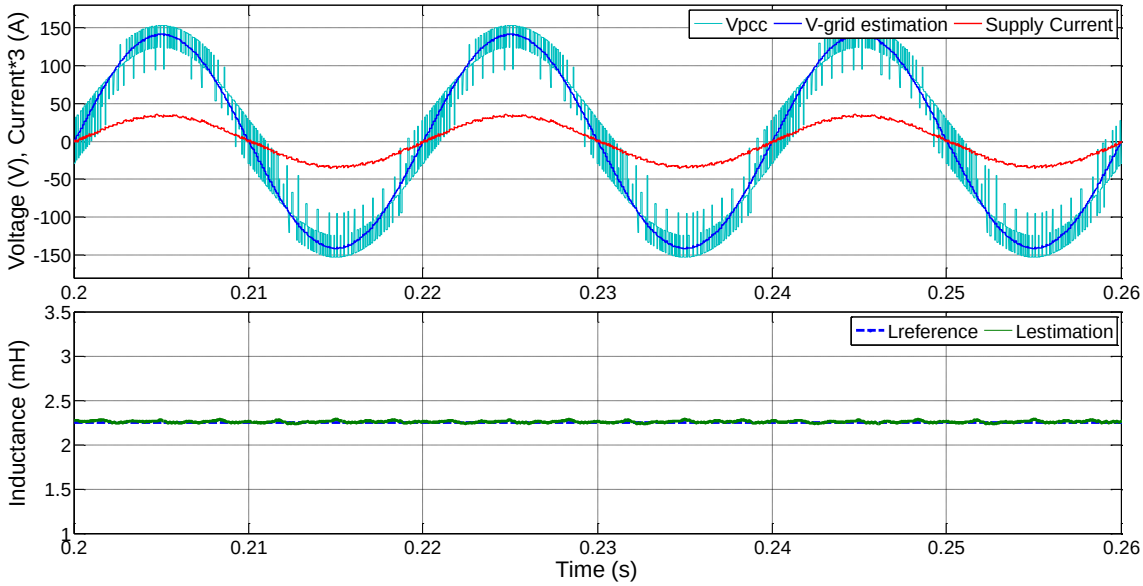


Figure 5.35: Grid voltage estimation, PCC voltage, supply current and grid inductance estimation with $L_S=50\%L_C$ (L_S = 2.25mH) as compared to L_C

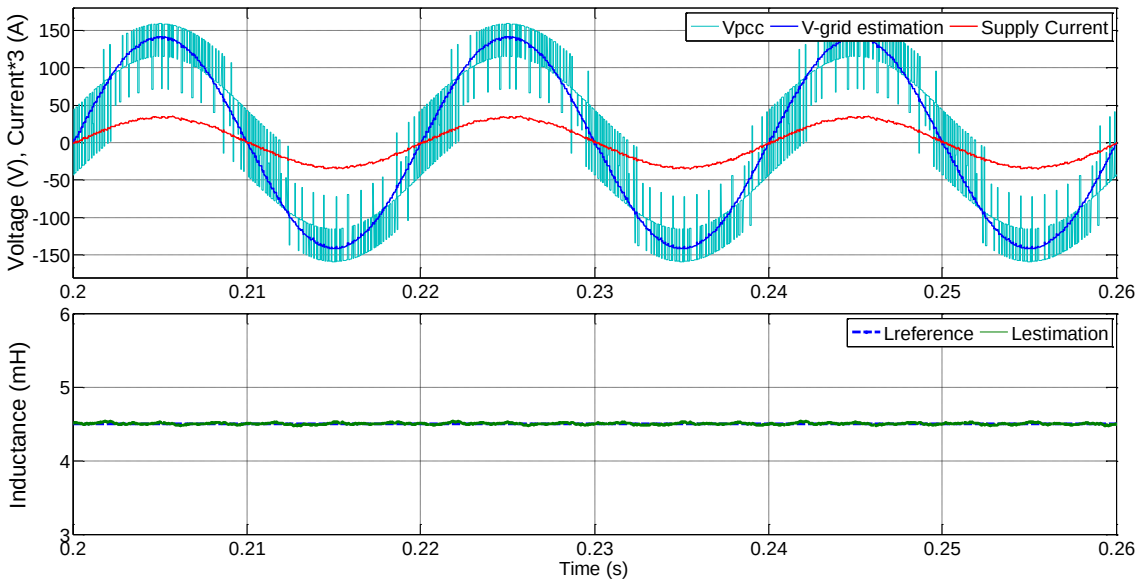


Figure 5.36: Grid voltage estimation, PCC voltage, supply current and grid inductance estimation with L_S=100%L_C

In figure 5.36 for L_S equal to L_C, the grid inductance is again estimated without any significant steady state error giving a supply current THD of 3.43%, estimated grid voltage THD of 1.36% for a PCC voltage THD of 31.3%. Comparing these results with that of figure 5.22, a very negligible difference in supply current THD of ~0.2% is observed whereas the estimated grid voltage maintains its THD value around ~1.4%. Therefore, the results for the two proposed methods match each other for similar cases without showing any drastic differences.

5.5.2. Frequent step variation in grid inductance

It is important to check the performance of the estimator integrated within the predictive control to a frequent step variation in grid inductance. The grid inductance estimation has been tested for a variation in grid inductance from 0.5mH to 4.5mH, i.e. L_S=*10%*L_C and L_S=*100%*L_C. In figure 5.37 the estimation algorithm responds quite accurately to a frequent variation in L_S.

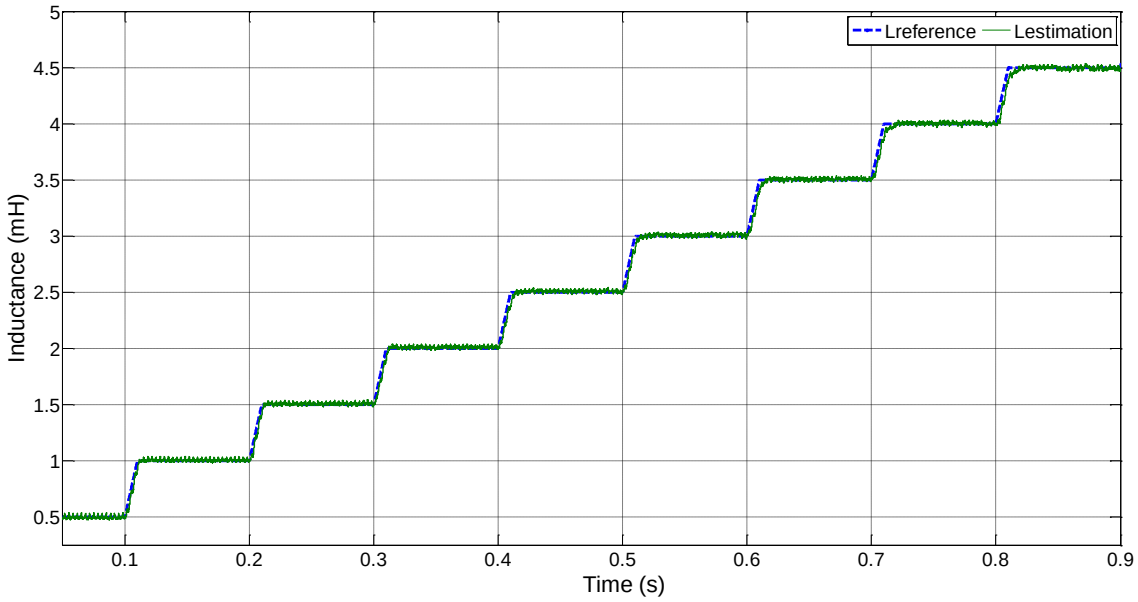


Figure 5.37: Grid inductance estimation with frequent variation

On the other hand, figure 5.38 shows the corresponding active and reactive powers with respect to their references for the frequent step variation in the grid inductance as presented in 5.37. It can be observed, that the powers follow their respective references quite accurately without any significant steady state error. Moreover, as expected, due to a smaller ripple on the supply current and correct estimation of the grid voltage the ripple on the active and reactive powers decrease with an increasing grid inductance. The dc-link voltage also maintains its stability around its reference value. However, for higher values of grid inductance, as shown in figure 5.39, the estimator starts showing a steady state error. In order to overcome this steady state error, the estimators' tuning parameters *n* and *i* need to be properly tuned or auto-tuning algorithm needs be derived. This is an on-going work and the further work of this estimation algorithm aims to highlight this important issue under very high grid inductance values.

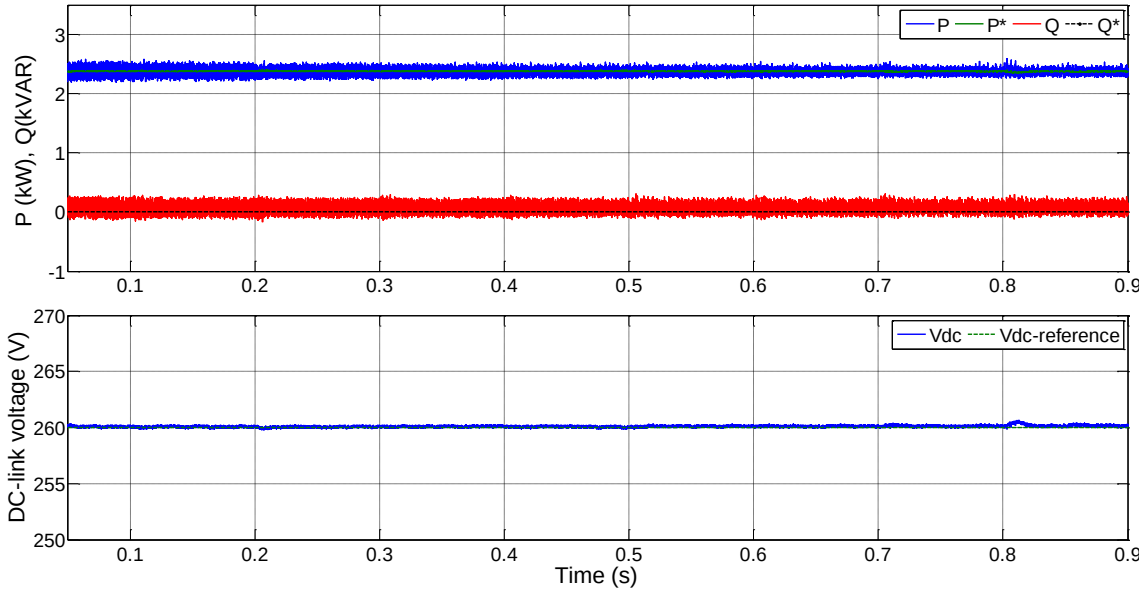


Figure 5.38: Active and reactive powers, DC-link voltage with references to a frequent variation in L_S

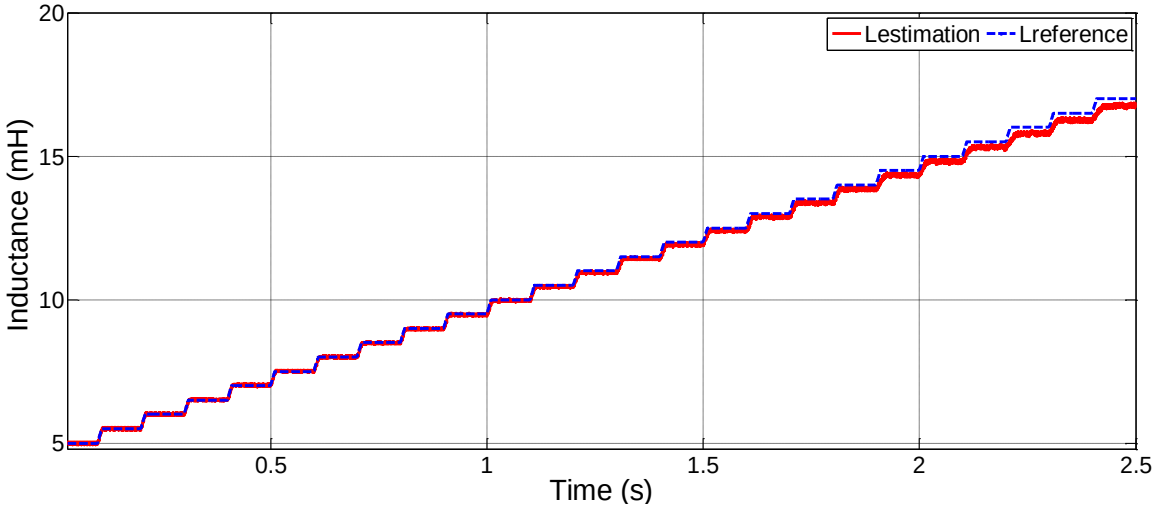


Figure 5.39: Grid inductance estimation for high grid inductance values

5.5.3. Online estimation in case of a large step in grid inductance

Figure 5.40 shows the performance of the estimator and the predictive controller to a large step of 3.0mH in the grid inductance. For an L_S value of 0.5mH from 0.08s-0.1s, the supply current has a THD value of 5.56% whereas the estimated grid voltage has a THD of 0.576% for a PCC voltage THD of 6.23%. When the step is introduced the

controller significantly deteriorates its performance resulting in supply current THD of 24.16% and estimated grid voltage THD of 15.9% for a PCC voltage THD of 31.54%. Unlike estimating the correct value in approximately one fundamental cycle using estimation method 1, method 2 takes approximately 3 fundamental cycles to reach the desired value of 3.5mH and after that greatly improving the supply current THD to 3.81% and estimated grid voltage THD to 1.8% when the PCC voltage has a THD value of 27.8%.

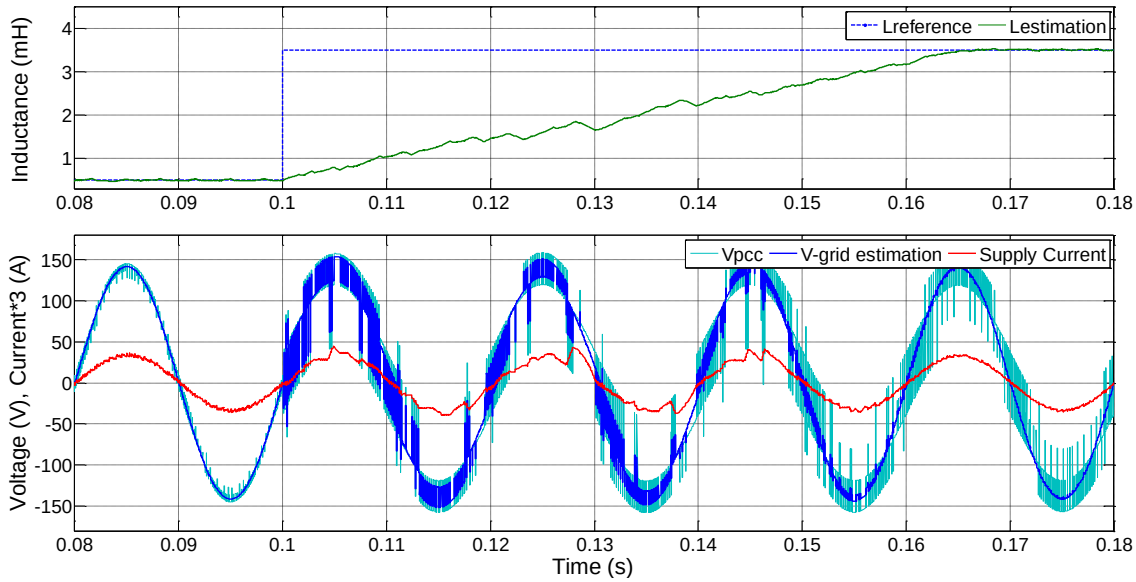


Figure 5.40: L_S estimation, supply current, PCC voltage, and grid voltage estimation with 67% step in L_S value (L_S = 0.5mH – 3.0mH) when L_C = 4.5mH

Therefore, to compare the two estimation methods for the same large variation in grid inductance, the supply current and estimated grid voltage have similar THD values, despite a larger settling time of method 2.

5.5.4. Online estimation with reactive power variation

Figure 5.41 presents grid inductance estimation results for the case when reactive power is varied from 0VAR to 1000VAR, 1000VAR to 500VAR and 500VAR to 0VAR. The

estimation algorithm, similar to the case in figure 5.27 using method 1, does not seem to get significantly affected by this variation and maintains its estimation around the reference value without giving noticeable steady state errors. Moreover, due to an accurate estimation of the grid inductance, the active and reactive powers also do not loose their performance and maintain close to their respective reference values. Since estimation method 2 highly depends on the tuning of the upper and lower limits, *n*, of the integer step, *i*, if these tuning parameters are not accurately designed it can result in a ripple on the estimated inductance as opposed to almost ripple-less estimation results using method 1. The tuning procedure of *n* and *i* is purely based on empirical methods and further work in this regard will be needed in order to establish a formal and rigorous methodology.

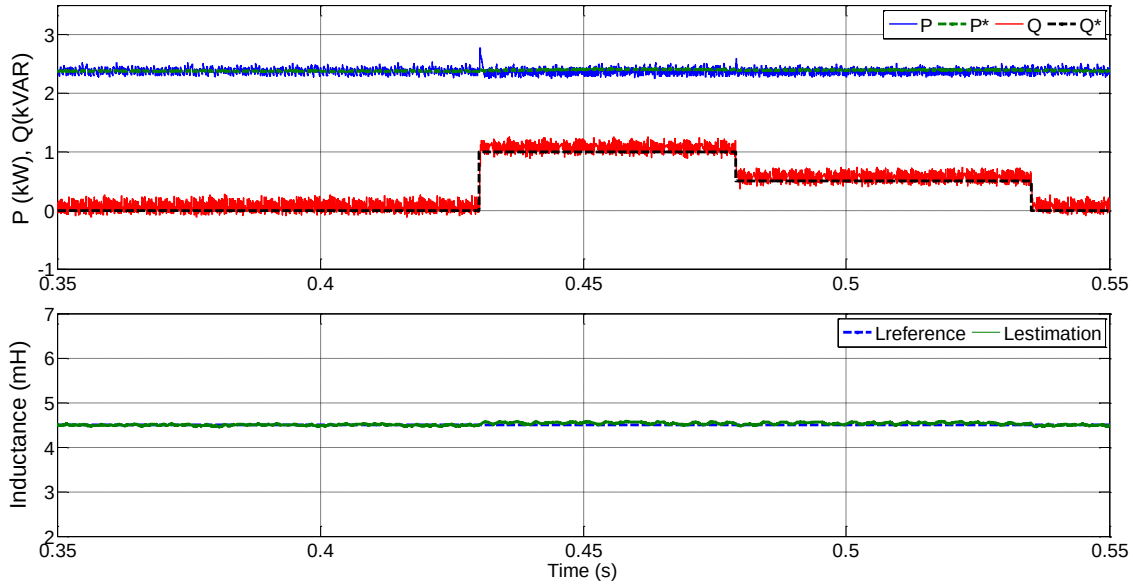


Figure 5.41: Active and Reactive powers with steps in reactive power reference and L_S inductance with L_S=100%L_C

5.5.5. Online estimation in the presence of a grid capacitance

A similar test to the one carried out in figure 5.32 for an equivalent grid model of figure 5.31 is here performed and figure 5.42 shows the results for grid inductance estimation

using method 2 when same value of grid capacitance of 100µF with a step in grid inductance from 0mH to 3.0mH grid inductance takes place. Comparing the result in figure 5.42 to the result in figure 5.32 for the grid impedance parameters, the estimated inductance follows the reference value quite accurately in both cases. However, a slight presence of ripple is seen for method 2 in figure 5.42 which can be improved with careful tuning of its parameters *n* and *i*.

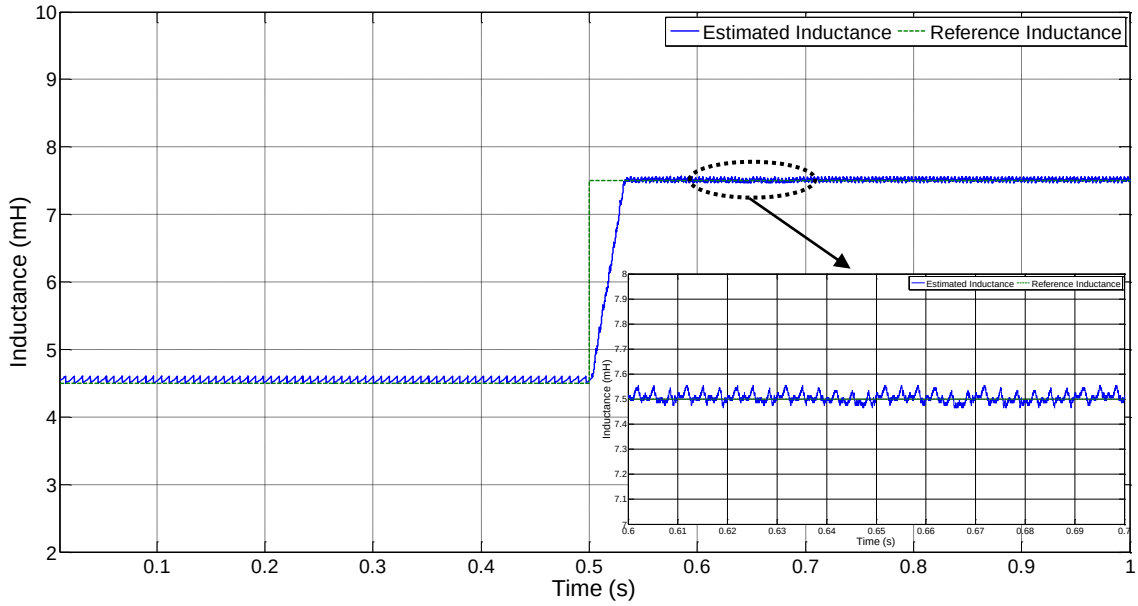


Figure 5.42: Grid inductance estimation with a presence of 100µF grid capacitance

5.5.6. Online estimation with unbalanced grid voltages

The results in this section present the performance of the inductance estimator in presence of unbalanced grid voltages. In figure 5.43 an unbalance between the three phase voltages was set such that phase *B* and *C* had a difference of 10V in amplitude with respect to phase *A*. Thus, while the phase *A* amplitude was set to $100V_{rms}$, the amplitude of phase *B* and *C* were $90V_{rms}$ and $110V_{rms}$, respectively. Even though there is a significant unbalance in the grid voltage amplitudes, the supply currents manage to

retain their synchronization with the grid voltage and maintain a close to unity power factor operation.

Figure 5.44, on the other hand, shows the total inductance (grid inductance + converter input filter inductance) estimation results. The estimation has a good reference tracking even for the case when the grid inductance has the same value as the converter input filter inductance of 4.5mH. Moreover, as compared to the estimation results of method 1, the estimation results in method 2 show a slight ripple on it. This ripple can be further reduced by adjusting the upper and lower integer limits as mentioned when explaining the proposed method in chapter 4.

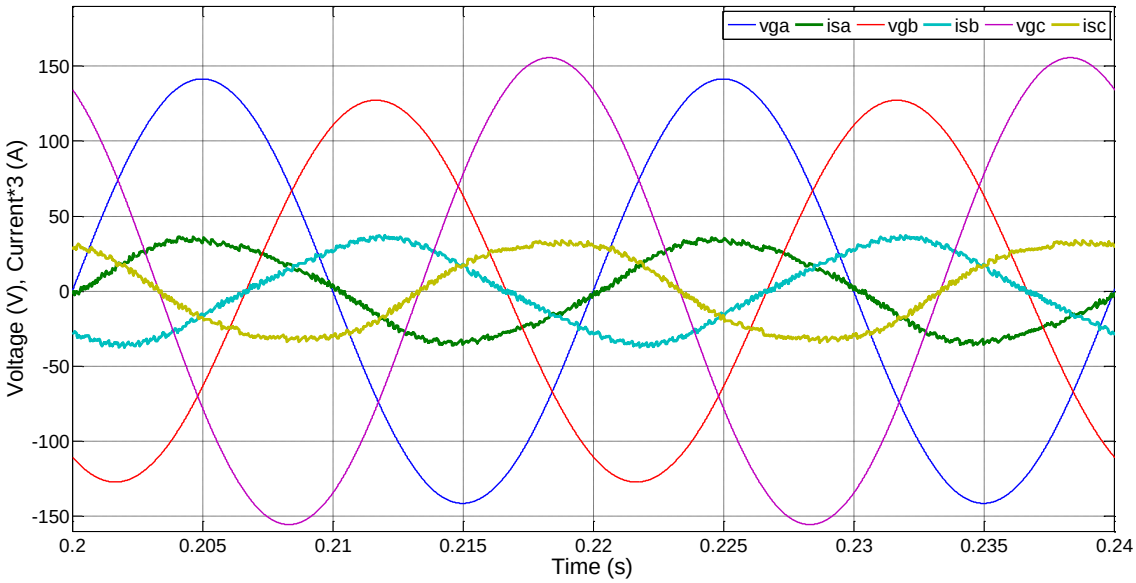


Figure 5.43: 3-phase unbalance grid voltages and respective supply currents

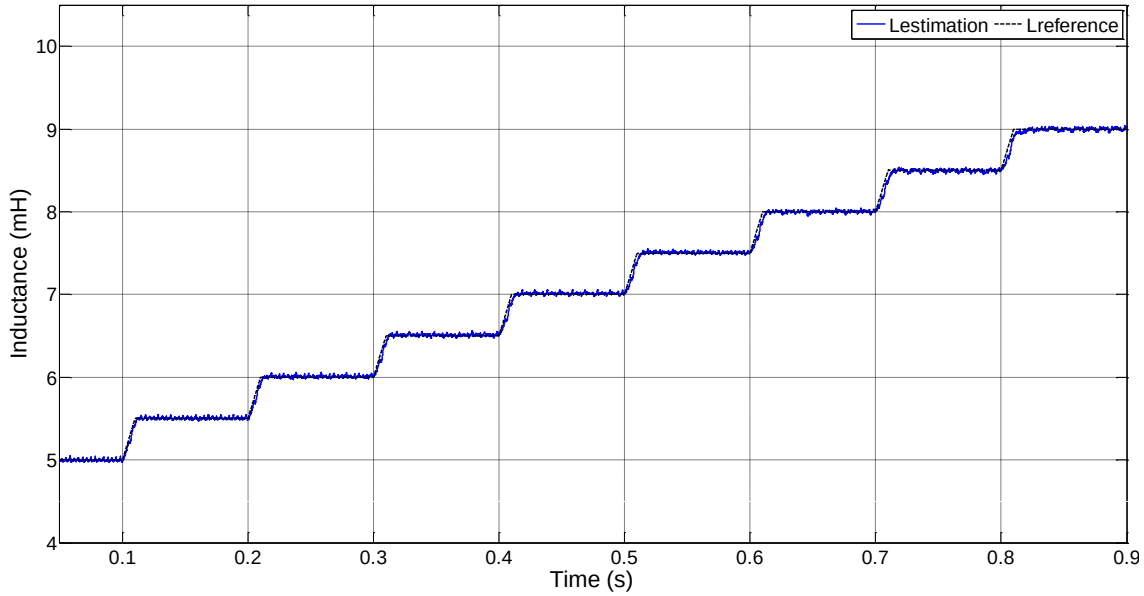


Figure 5.44: Total inductance estimation for unbalance grid voltage condition

Figure 5.45 shows the grid voltage estimation, supply current and the PCC voltage for a 100% grid inductance value compared to the converter input filter inductance in case of a significant unbalance between the grid voltages.

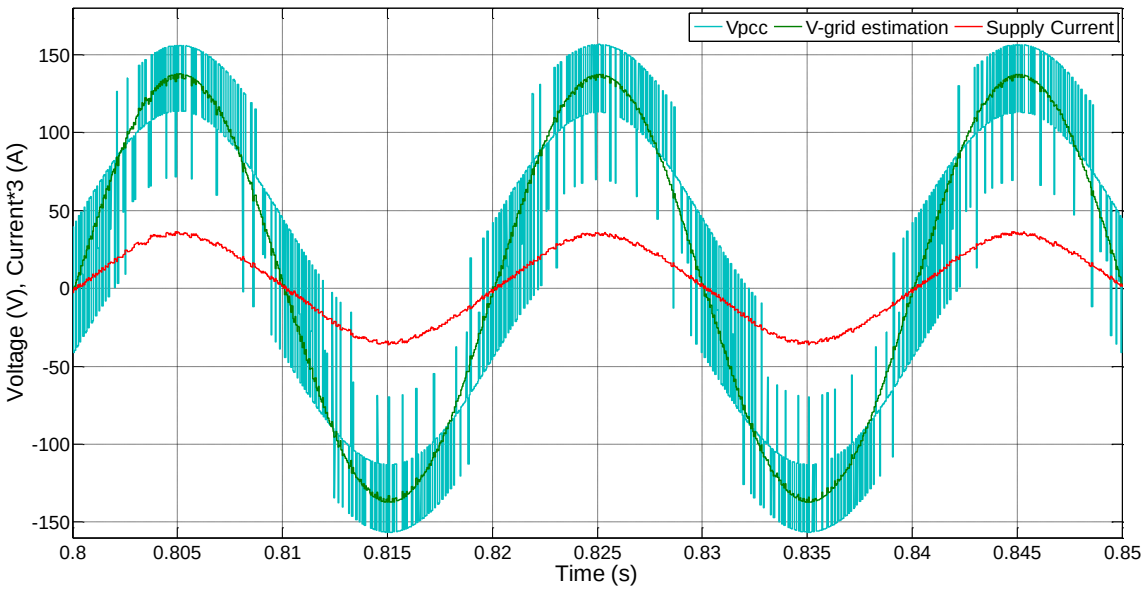


*Figure 5.45: Grid voltage estimation, PCC voltage and supply current*3 for phase A with unbalanced grid voltage condition and L_S=100%L_C, L_S=4.5mH, L_C = 4.5mH*

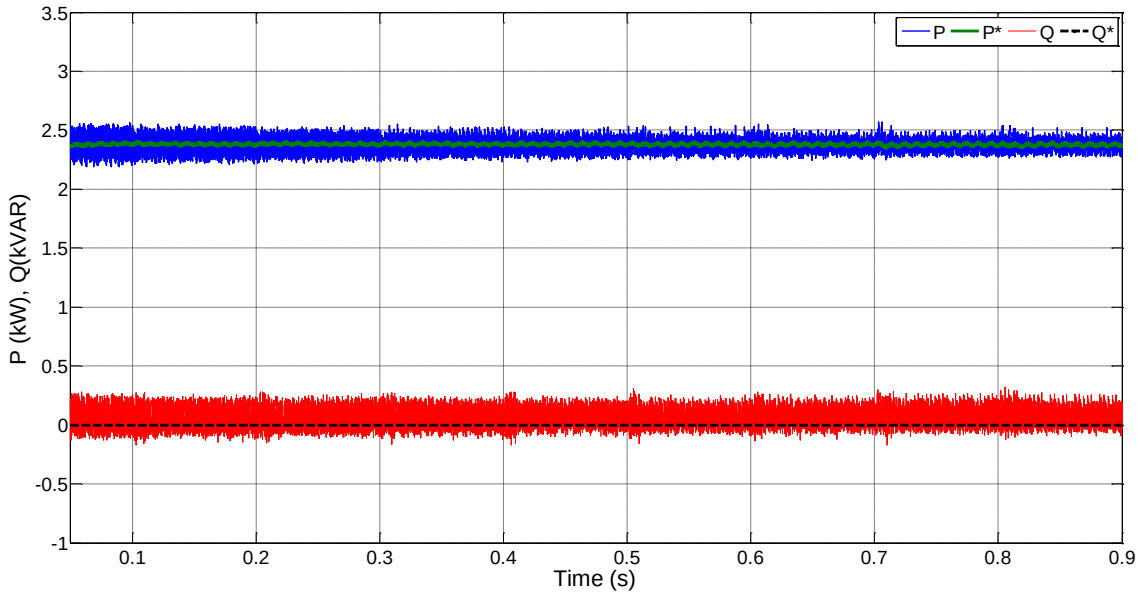


Figure 5.46: Active and reactive powers with their respective references for unbalanced grid voltage condition

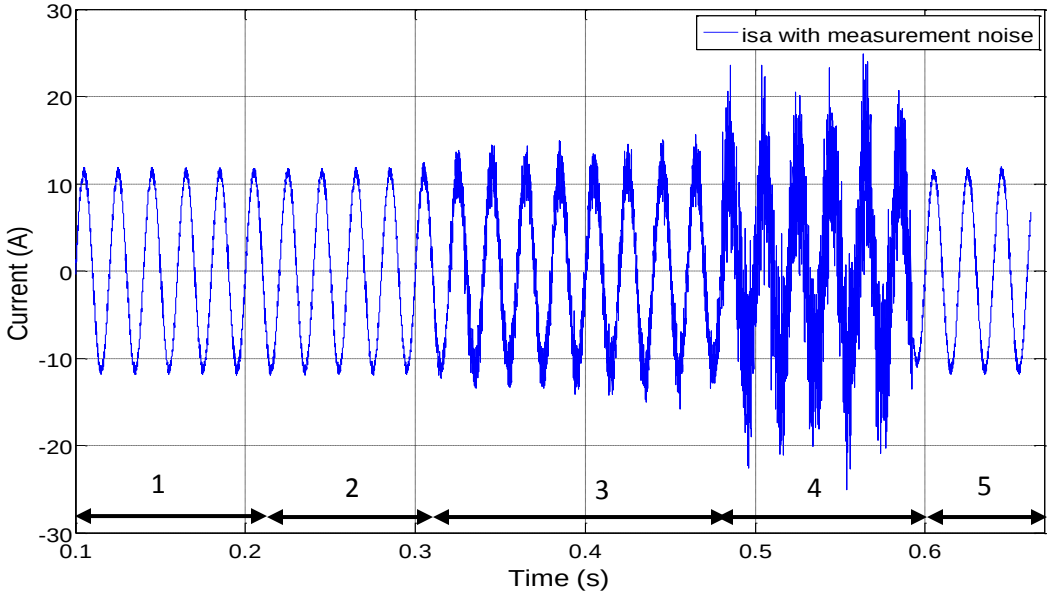
Figure 5.46 shows the active and reactive powers along with their respective references for the unbalanced grid voltage. A small steady state error is seen on the reactive power and that is due to the presence of ripple on the estimated inductance. This is currently an on-going challenge associated with this approach where under very low SCR values, the ripple on the estimated inductance increases and starts to affect the control performance. In order to solve this issue, an online tuning of the integer parameter used in the cost-function optimization for optimum grid inductance value generation needs to be carried out so the estimator is automatically corrected and updated once the SCR reaches a low value. This is an on-going work and the further work section of this project will address this issue.

Overall, the results presented in this section show a good reference tracking for the inductance estimation, active and reactive powers and show a high quality current waveform with THD below 4% even in case of an unbalanced grid voltage.

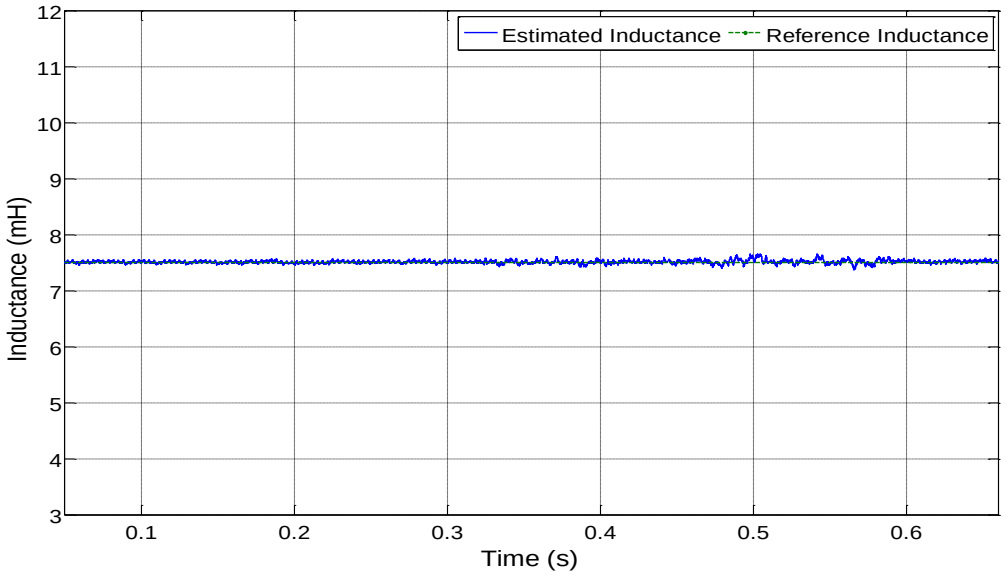
Furthermore, the impedance estimation in the presence of voltage unbalance is only possible with method 2 as it does not rely on a constant grid voltage magnitude.

5.5.7. Effect of measurement noise

In this section the effect of measurement noise was observed on estimation method 2 as shown in figure 5.47 using 5 test conditions. The Band-Limited White Noise Block in Matlab/Simulink was used at the input of the controller.



(a)



(b)

Figure 5.47: Estimation Method 2 (a) Effect of noise on measured supply current, (b) Total estimated inductance in presence of noise

Table 5.5 shows the effect on supply current THD for 5 difference noise values arbitrarily used in the Matlab Noise block.

Table 5.5: Estimation method 2 - Effect of measurement noise on supply current THD

	Noise Intensity in Matlab Block	**THD_i**
1	$1e^{-9}$	3.38%
2	$1e^{-7}$	3.47%
3	$1e^{-4}$	17.6%
4	$1e^{-3}$	51.6%
5	$1e^{-9}$	3.38%

With reference to table 5.5 and figure 5.47, the peak-peak ripple amplitude on supply current in case of test condition 1 of measurement noise was 0.7A while in case of test condition 4 the peak-peak ripple amplitude increased to 14A. Also, in comparison to figure 5.34, estimation method 2 in this section seemed to be less susceptible to

measurement noise as it showed lesser or negligible steady state error on the estimated inductance to introduction of measurement noise.

5.6. Conclusion

This chapter started with a presentation of simulation results for the MP-DPC and showed its performance under variations of the dc-link voltage reference and the reactive power reference. To show the sensitivity of MP-DPC to parameter mismatches, 2 cases of results with grid inductance, when not compensated, were presented. The results showed that the performance of the MP-DPC is greatly affected due to the presence of these unknown grid parameters. Therefore, estimation and integration of these parameters within the predictive controller for grid-connected converters becomes extremely important.

Sections 5.4 and 5.5 presented results for the two proposed grid inductance estimation methods that can be easily integrated within the MP-DPC giving it a much robust and stable performance under low Short Circuit Ratio value, representing a Weak Grid scenario. Results for both the proposed estimation algorithms present good tracking to grid inductance variations even under reactive power variation or when a large step in grid inductance takes place. Both the proposed estimation methods were also tested under cases of grid voltage unbalance and also in presence of noise. It was observed that method 1 was more prone to effect voltage unbalance and noise as compared to method 2 that did not show significant steady state errors.

For method 2, a suitable value of ΔL_s and n had to be chosen that was computationally feasible. The estimation algorithm took larger time to converge to the right value when the ΔL_s value was of the order 0.001mH as compared to a larger value of 0.1mH that

resulted in faster convergance, for example. However, once the estimated value reached its steady state, the estimation result with a small value of ΔL_s was more affected by noise as compared to a larger value of ΔL_s. Therefore, a tradeoff between the convergance rate and presence of noise needs to be taken in consideration while designing the parameters of estimation method 2. The stability limits of estimation algorithms using predictive control were not investigated in this project but further work can look into the stability margins [38], [63], [74].

The next chapter presents the experimental results for the proposed estimation methods applied on a three phase two-level grid connected converter prototype.

Chapter 6: Experimental Setup and Results

6.1. Introduction

In order to validate the simulation work carried out in chapter 5, this chapter presents the experimental results in support of the Model based Predictive Direct Power Control (MP-DPC) and line inductance estimation algorithms proposed in this work tested on a 3-phase 2-level rectifier prototype. An equivalent representation of the experimental setup is explained in chapter 5 and is also shown in figure 6.1. Tests have been conducted supplying the active rectifier circuit both by means of a three-phase Programmable Voltage Source (PVS) manufactured by CHROMA[109] and also by using an autotransformer (VARIAC) [6], one at a time respectively.

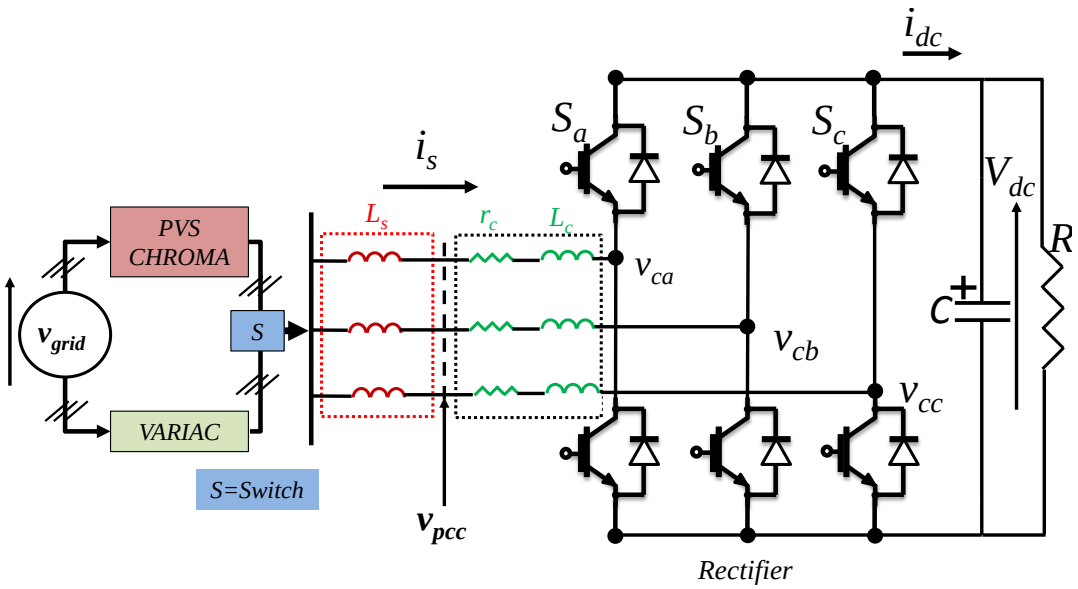


Figure 6.1: Experimental arrangement circuit diagram

Using the PVS, three operating conditions have been tested and the results are presented in sections 6.2.1, 6.2.2 and 6.2.3 respectively, where the inductance estimator and the model predictive controller are tested with a constant DC-link reference value, a step in the dc-link voltage reference and by varying the reactive power reference.

In section 6.3, results using the VARIAC are presented where the performance of the predictive controller and the inductance estimator is analyzed to a sudden variation in the VARIAC voltage. The reason to use an autotransformer VARIAC is to estimate its built-in inductance together with the grid inductance L_S, as shown in figure 6.1, in order to test the estimation algorithm under more practical operating test conditions.

6.1.1 Experimental setup

Figure 6.2 shows the experimental setup for testing the proposed control algorithms. The experimental setup has been made such as to replicate a real grid scenario where there is a presence of grid inductance. In figure 6.2, an autotransformer (connected to the mains of the laboratory) is used as a voltage source. A power supply protection circuit is also used to isolate the experimental system in case of over current or a short circuit.

6.1.1.1. Voltage and Current measurement

Measurements of the three phase PCC voltages and the dc-link voltage are taken by voltage transducers for control processing. Voltage hall-effect transducers with model number LEM LV25-P have been used that can measure up to 500V as mentioned in the datasheet [110]. The supply currents are measured using three LEM LA55-P transducers that have a maximum bandwidth of 200kHz and a maximum current capacity of 50A [111]. The output of both the transducers is a current value that is proportional to the primary side signal at the input of the respective transducers. A burden resistor is used to convert these current signals into voltage signals to be used by the interface card for control processing.

6.1.1.2. System Parameters

A grid inductance L_S of 3mH is used with one end connected to the autotransformer and the other end connected to the point of common coupling (PCC) while a converter input filter inductance L_C of 4.5mH has been used that is connected between the PCC and the converter input, as shown in figure 6.2 of the experimental setup. The dc-link consists of two 1100µF electrolytic capacitors connected in parallel, resulting in a total dc-link capacitance of 2200µF that acts like a filter to reduce the voltage ripples due to the rectification process on the output dc-link voltage. Two resistors of 58.6Ω are connected in parallel to give a 28.8Ω load with a total power of approximately 2.5kW.

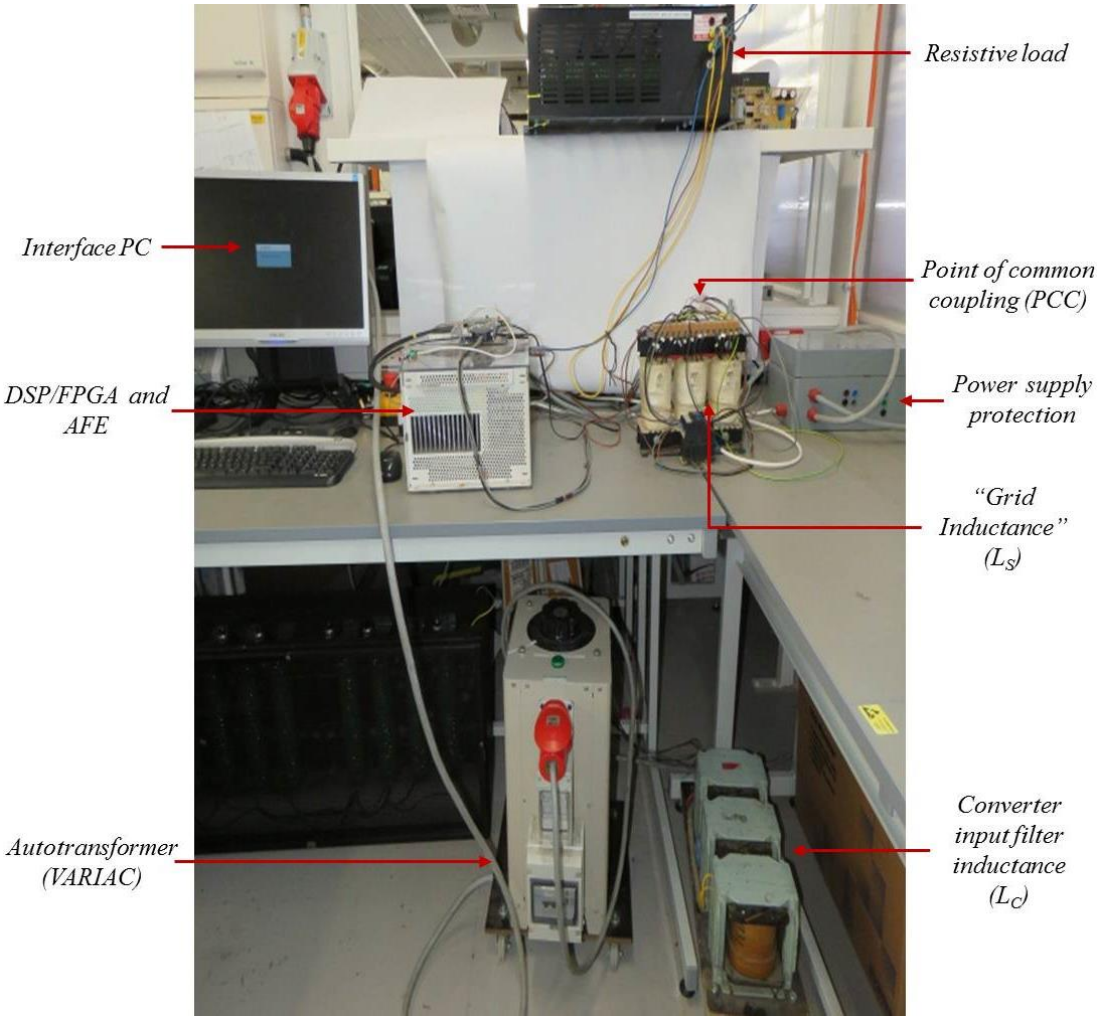


Figure 6.2: Experimental set-up

6.1.2. Control board and AFE

Figure 6.3 shows the details of the power electronics converter. The three legs of the rectifier, labeled as *a*, *b* and *c* consists of two Semikron SK30GH123 IGBT modules per leg rated at 1200V and 30A, as in figure 6.1, and receive the optimum switching signals through fiber optic cables.

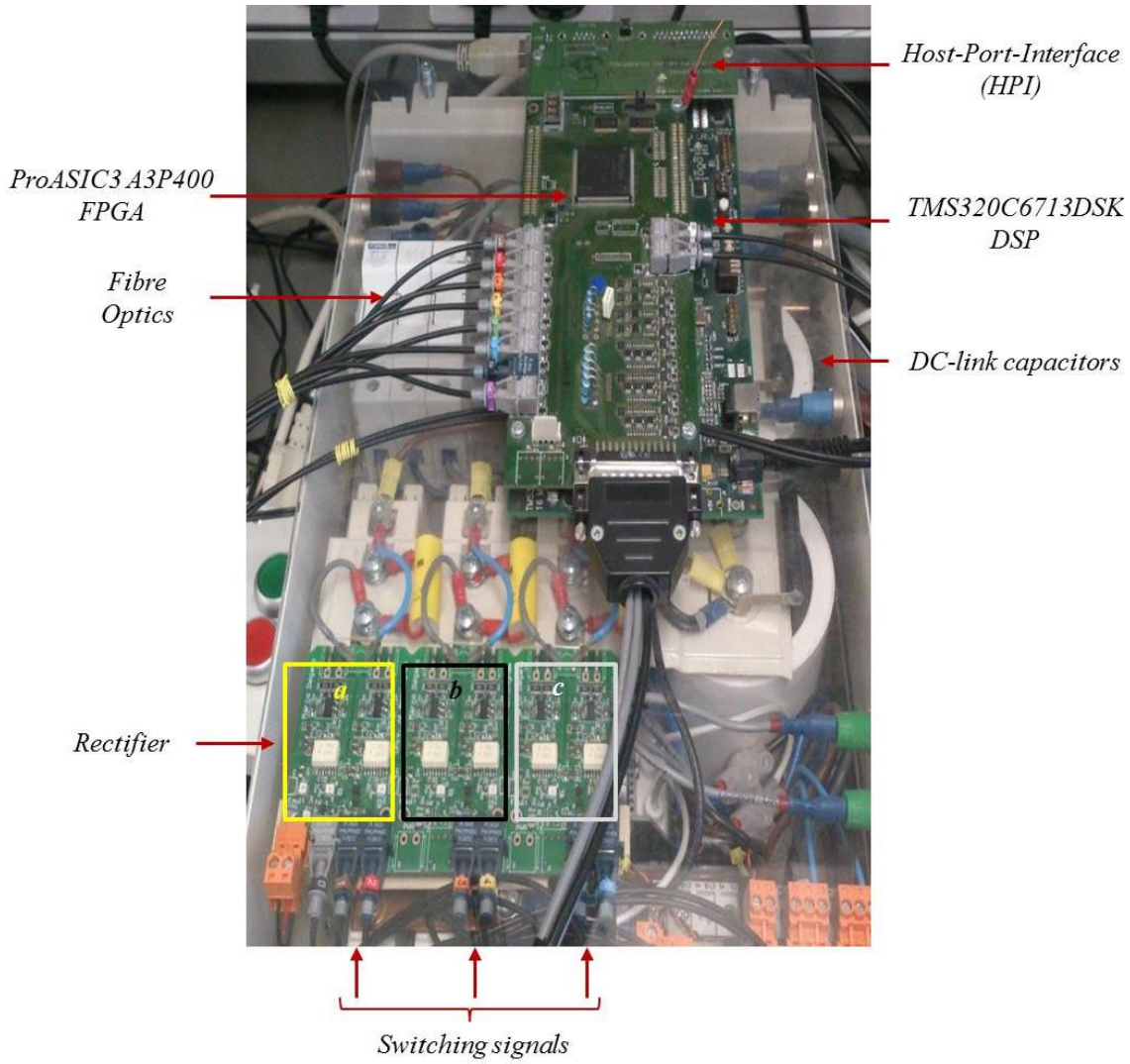


Figure 6.3: Three phase active two-level rectifier set-up

The features of these IGBT modules include compact design, operation in temperatures ranging from -20° to greater than 120°C, one screw mounting onto the PCB board, can be used in switch mode power supplies and also in uninterrupted power supplies [112].

A dead-time circuit is integrated in the system to ensure that two switches in each leg are not turned ON or OFF simultaneously in order to avoid short-circuit of the dc-link capacitor. Also, hardware device protection circuits are mounted onto the PCB board to protect the IGBTs from over-current or in case of short-circuit. The IGBT modules are driven by gate drive signals generated from the *Actel ProASIC3 A3P400* field programmable gate array (FPGA) board with a clock frequency of 50MHz. The FPGA board designed by the University of Nottingham PEMC Group is mounted on to a Texas Instruments *TMS320C6713DSK* digital signal processor (DSP) board that has a clock frequency of 225MHz and a 32-bit wide external memory interface for communication with the FPGA. Both the DSP and FPGA boards work together such that the interrupt time for DSP operation, at the user-defined sampling frequency (clock frequency) of 20kHz, is generated by the FPGA that also triggers the conversion of the 10 Analogue to Digital channels (ADC) on the FPGA. Once the ADC conversions are completed, the digital measurements from the ADC on FPGA are mapped into the memory of the DSP that gives the DSP access to measurements in real-time. These measurements are processed within the MP-DPC control algorithm written in C-language that is compiled and transferred into the DSP memory by Code Composer Studio 5.5.1 to obtain the optimum switching signals through cost-function optimization. The DSP then sends the optimum switching signals to the FPGA board that transforms them into gating signals and through optic fiber cables drives the power converter IGBTs. In order to minimize the effect of measurement noise, Anti-aliasing filters are added before the ADC channels. Anti-aliasing filters are also known as Low Pass filters that satisfy the Nyquist Sampling Theorem which states that the cut-off frequency of the filter should be less

than or half of the sampling frequency. In this project, the sampling frequency was 20kHz so the cut-off of the anti-aliasing filters was designed to 10kHz and less. The advantage of anti-alisaing filters is that it allows low frequency signals to pass through while it attenuates high frequency signals. A Host-Port-Interface (HPI) Daughter Card is mounted on the FPGA and DSP boards, as shown in figure 6.3. HPI board allows the acquisition of data from the DSP to be processed on software such as Maltab/SIMULINK in order to plot and provide additional commands for the control of desired variables. Figure 6.4 shows a block diagram of control implementation on the experimental system setup as shown in figure 6.2 and figure 6.3.

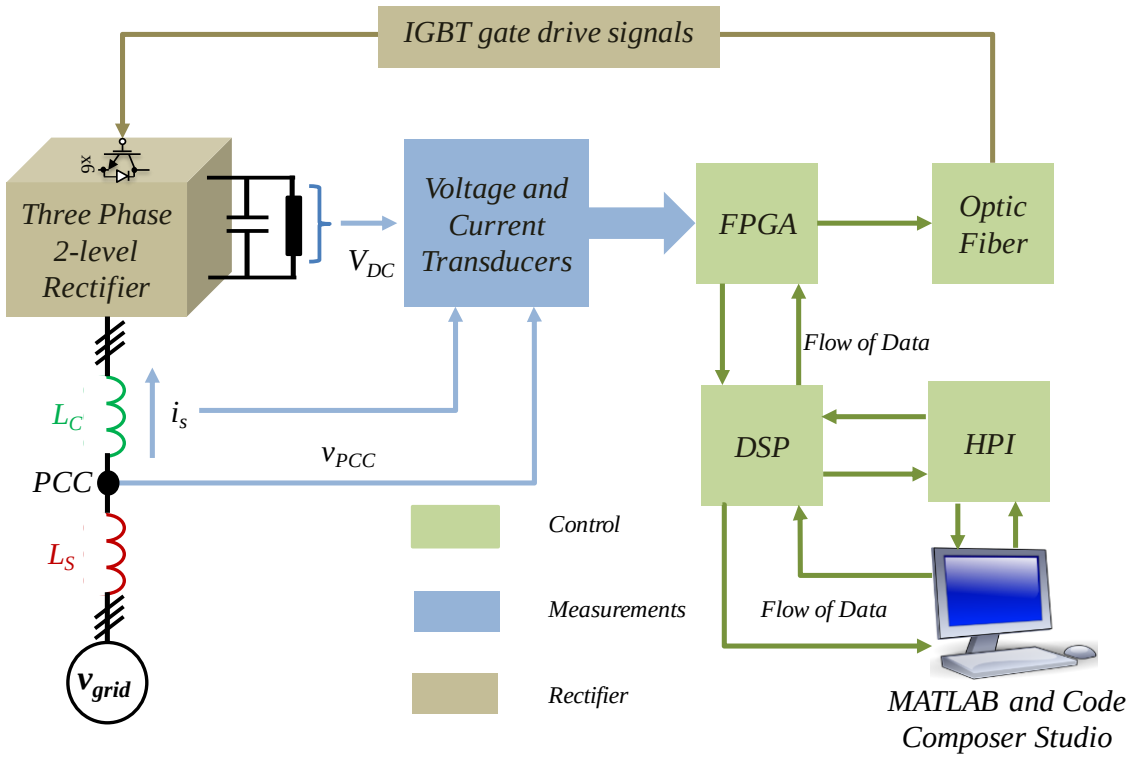


Figure 6.4: Block diagram of the control implementation

6.2. Experimental Results using a Programmable Voltage Source

Figures 6.5-6.16 in this section show results for the real-time grid inductance estimation method 1 as proposed in chapter 4 when tested using a programmable voltage source manufactured by CHROMA that also takes into account an online power switching devices dead-time compensation method. With reference to figure 6.1, the grid inductance has been set to 3.0mH and the usually known converter input filter inductance value at 4.5mH. Therefore, the total expected estimation of line inductance is 7.5mH. Using the MP-DPC, the power factor is maintained close to unity by directly controlling the active and reactive powers, thus keeping the voltage and current synchronized with each other and avoiding the use of a PLL. This can be seen in figure 6.5 where the estimated grid voltage and the supply current are in synchronization despite having a large grid inductance value that is estimated correctly as shown in figure 6.6. Effect of digital noise and high switching of power converter can be seen in figure 6.5 and methods to minimize this, like inclusion of anti-aliasing filters, have been developed [7], [8], [20]. It was observed that though anti-aliasing filters can filter out noise seen on the PCC voltage as seen in figure 6.5, a small delay can also be introduced if value of grid impedance is large. Thus, another reason associated with presence of noise on PCC for phase *A* in figure 6.5 is due to a high value of grid impedance that results in a highly distorted PCC voltage. Moreover, anti-aliasing filters can be used but their tuning parameters need to be carefully designed so they can perform well under any value of grid impedance. With reference to figure 6.1, the distortion on the PCC voltage can be justified in equation (6.1) below:

$$v_{pcc}(t) = v_{grid}(t) - L_S \cdot \frac{di(t)}{dt} \tag{6.1}$$

Where, the v_{pcc} gets distorted because of the distorted voltage drop $L_S \cdot \frac{di(t)}{dt}$. As the value of grid inductance L_S increases the distortion on the PCC voltage increases.

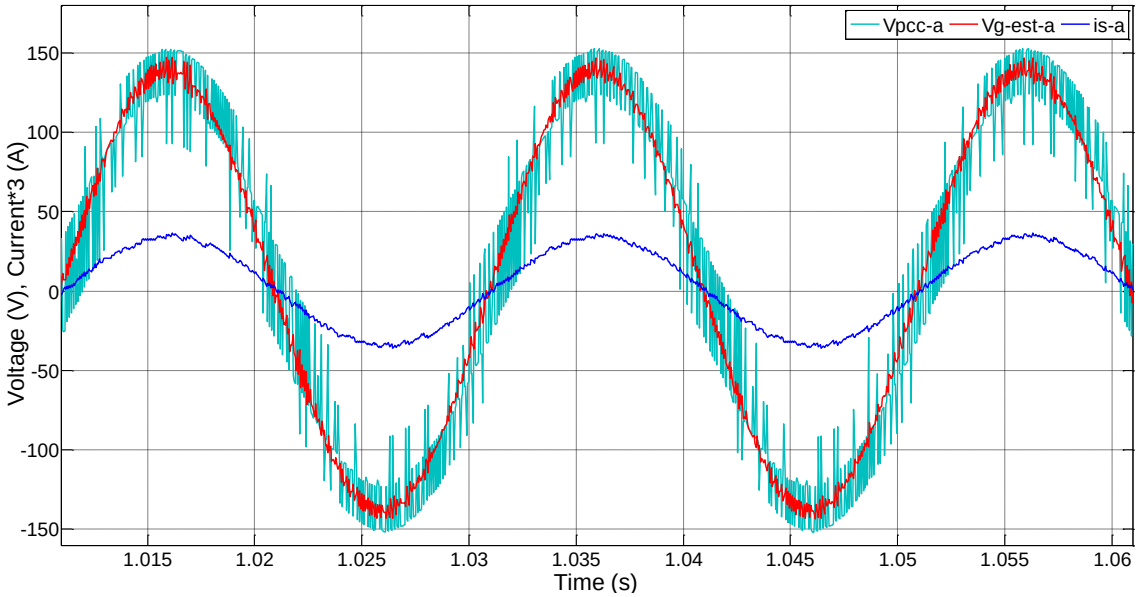


Figure 6.5: PCC voltage, supply current and grid voltage estimation – phase A

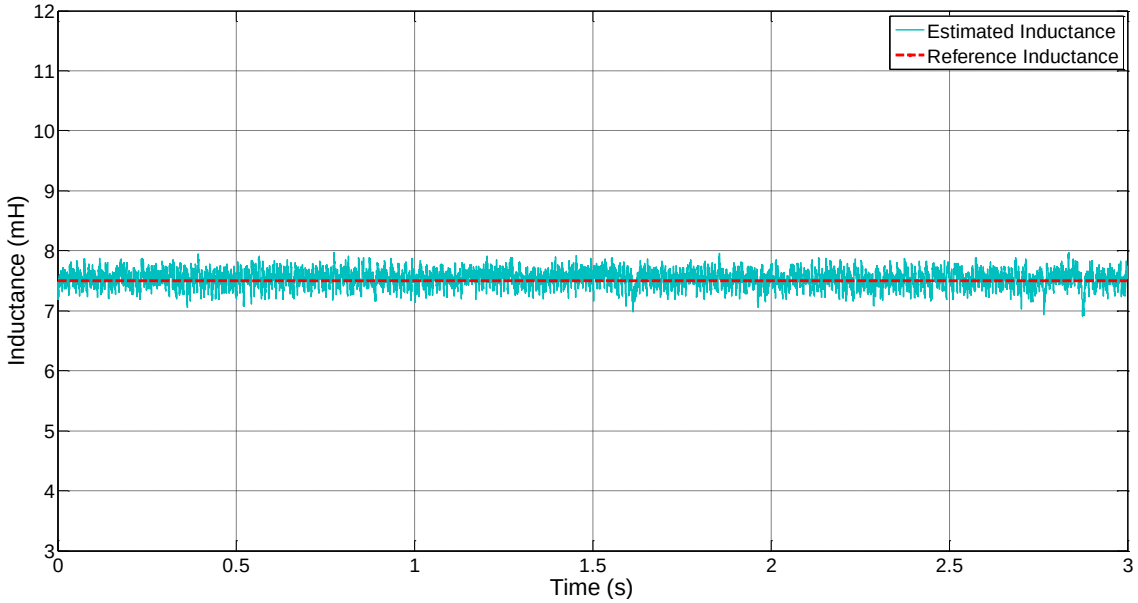


Figure 6.6: Total Inductance estimation – L_S = 3.0mH, L_C = 4.5mH

6.2.1. DC-Link voltage regulation procedure

The dc-link voltage and its reference are shown in figure 6.7 along with the active and reactive powers in figure 6.8. The reference calculations for the active power and dc-link voltage are explained in sections 4.2.5 and 4.2.6 in chapter 4, whereas, the reactive power reference is set to 0VAR to achieve a unity power factor.

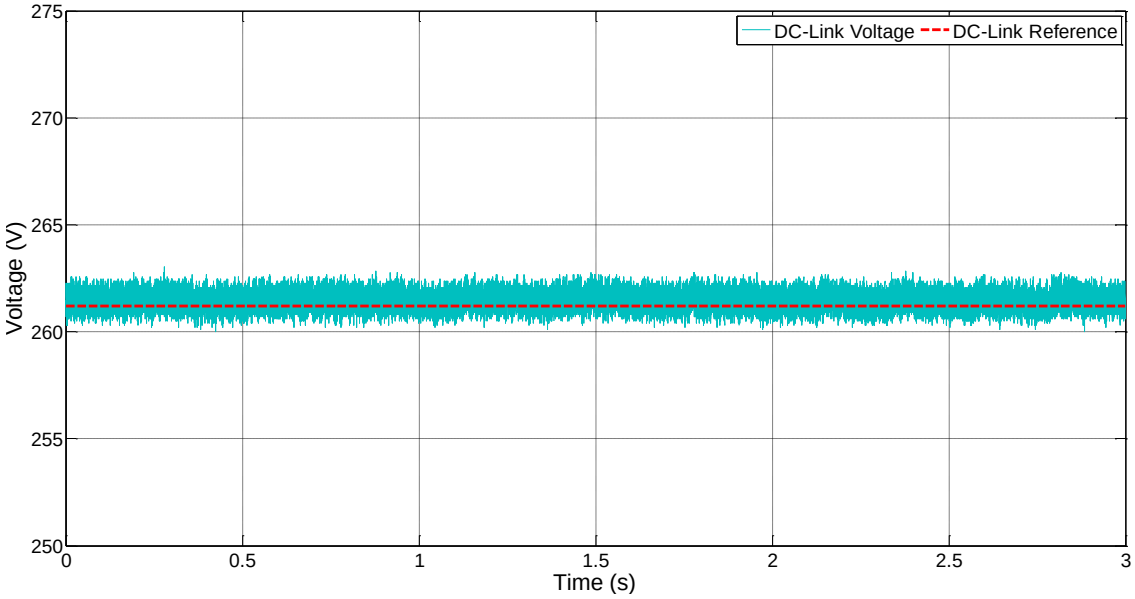


Figure 6.7: DC-Link Voltage with reference

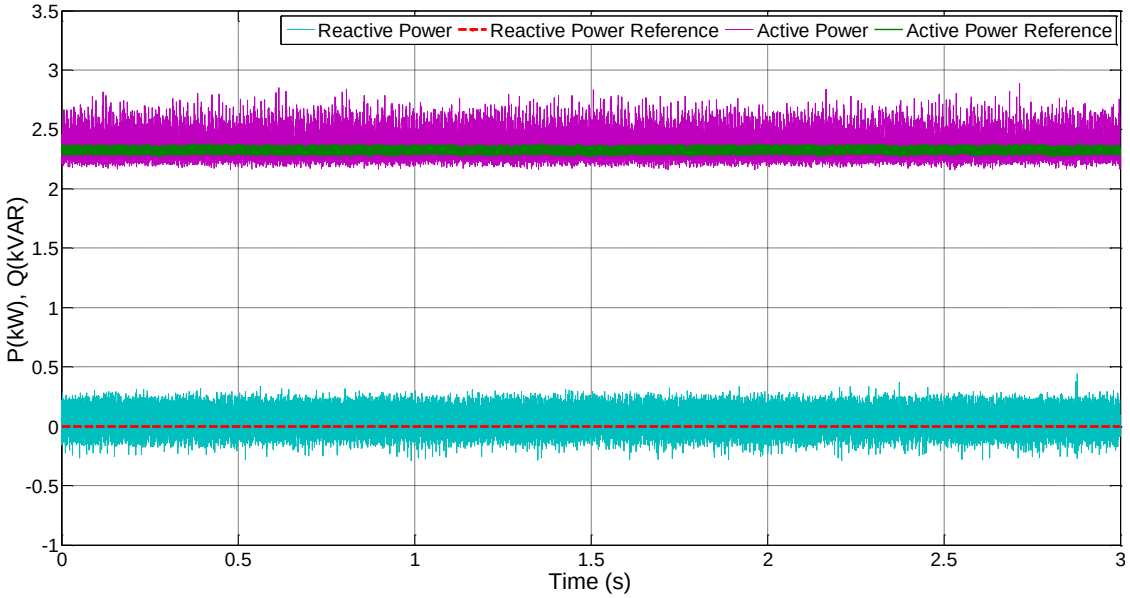


Figure 6.8: Active and Reactive power with reference

The dc-link voltage reference is equal to ~261V while the active power reference and the reactive power reference are equal to ~2.4kW and 0kVAR, respectively. The results in figure 6.7 and figure 6.8 show a good reference tracking of the dc-link voltage, active power and reactive powers, respectively.

6.2.2. Step in dc-link voltage reference

It becomes of utmost importance to observe how a variation in active power demand affects the proposed grid inductance estimation method. Figure 6.9 shows a step of approximately 35V, 182V to 217V, on the dc-link voltage reference. As expected, the dc-link voltage follows the reference accurately.

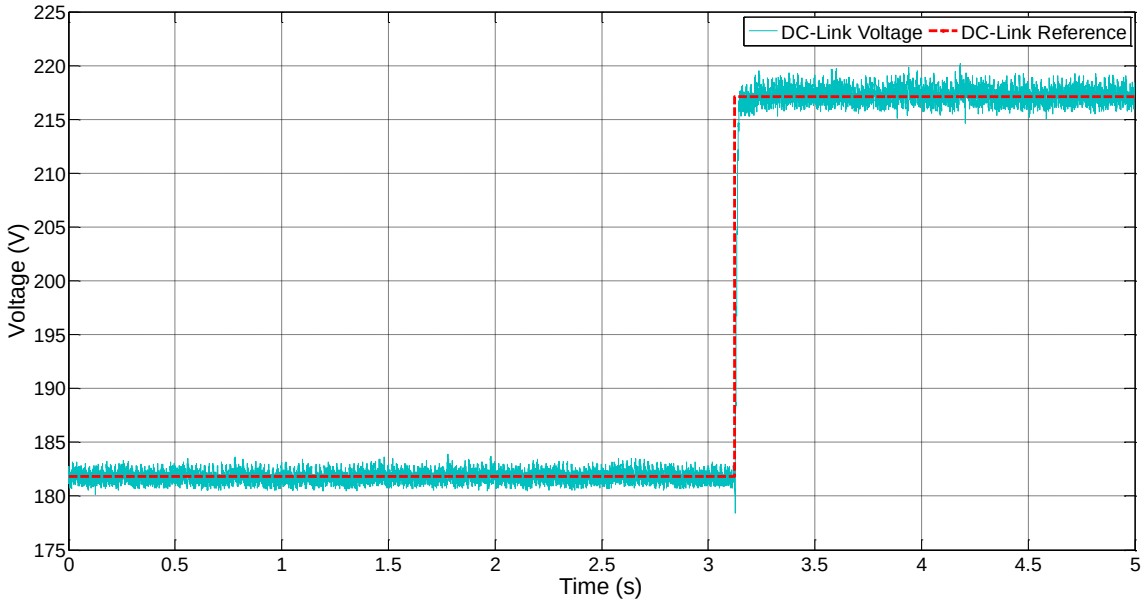


Figure 6.9: DC-link voltage with a step of 35V in dc-link voltage reference

The response of active power with respect to its reference variation is seen in figure 6.10 where even for a large step in active power, the reactive power does not get affected and maintains close to unity power factor by staying at ~0VAR.

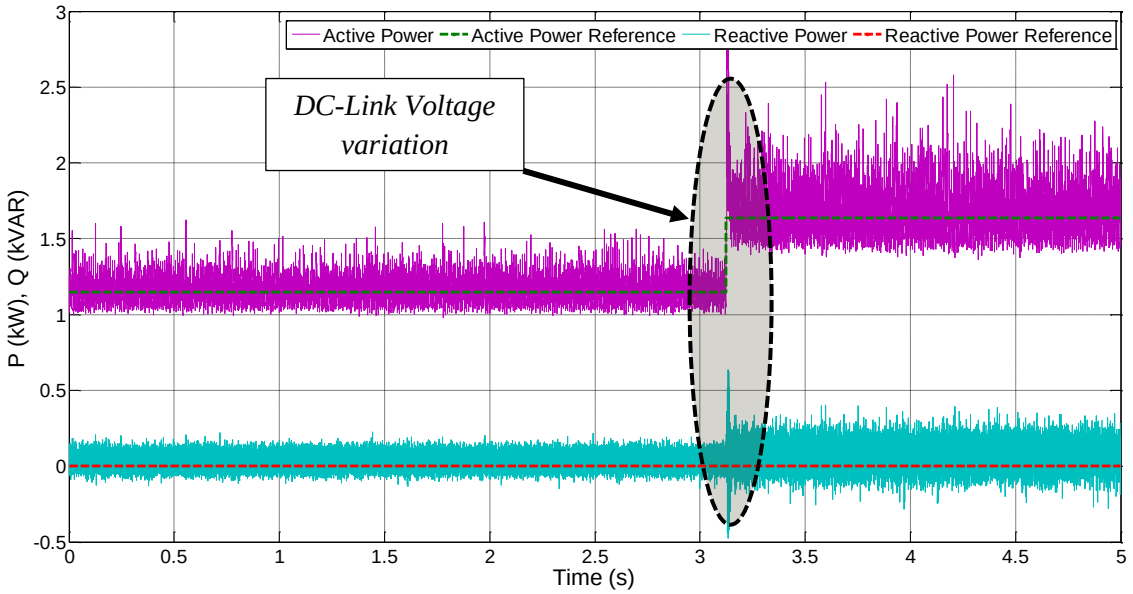


Figure 6.10: Active power and reactive power with their respective references with a step of 35V in dc-link voltage reference

At time 3.2s a large spike can be observed on the active and reactive power to a step variation in dc-link voltage reference in figure 6.10. This is due to a high demand of supply current during that instant and also due to the small calculation time required by the inductance estimator to reach its desired value. Though the active and reactive powers are calculated using the estimated grid voltage, a larger ripple on the PCC voltage will in turn induce a ripple on the estimated grid voltage. The MP-DPC takes less than 0.01s to respond to this variation.

Figure 6.11 shows the corresponding supply current, PCC voltage and the grid voltage estimation to a variation in the dc-link voltage. The supply current amplitude increases, as expected and the THD value shows a slight increase from 5.1% to 5.9%.

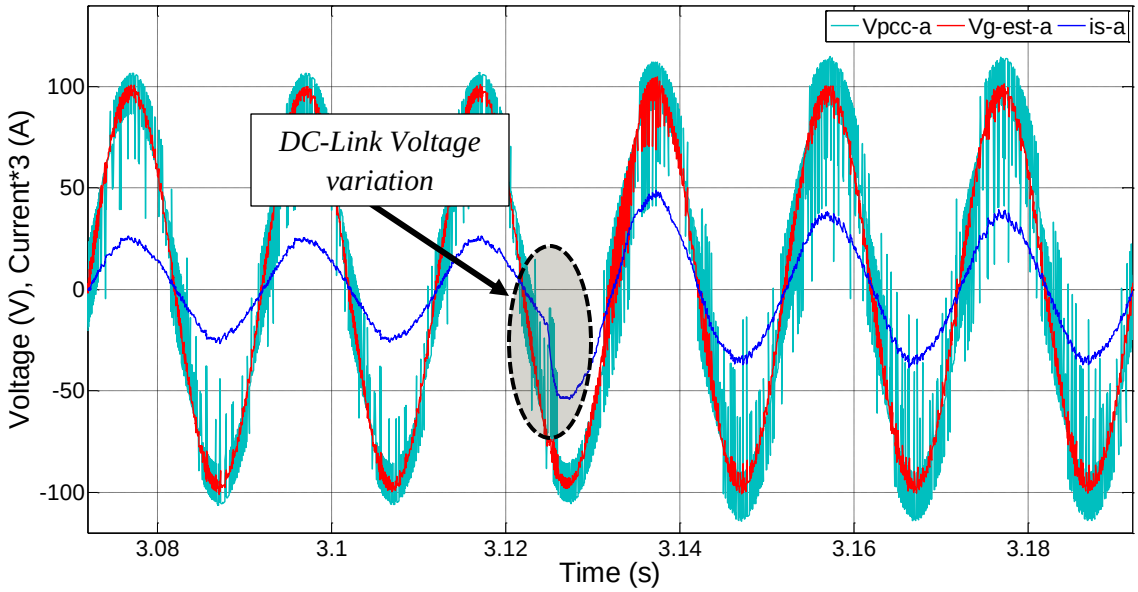


Figure 6.11: PCC voltage, supply current and grid voltage estimation for a step of 35V in dc-link voltage reference– phase A

An important point to highlight in figure 6.11 is the grid voltage estimation that maintains its quasi-sinusoidal waveform even for a large step in dc-link voltage as the inductance estimation algorithm does not lose its performance even after the step in the dc-link voltage.

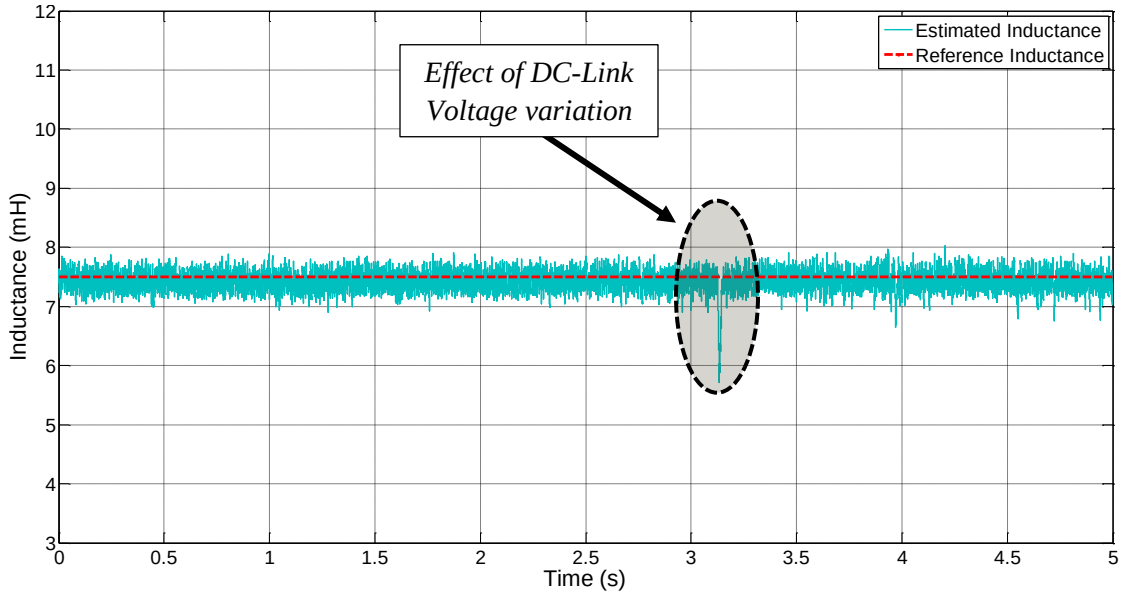


Figure 6.12: Total Inductance estimation with a step in dc-link voltage reference, L_S = 3.0mH, L_C = 4.5mH

At time ~3.1s in figure 6.12, a small variation in estimation due to a large step in dc-link voltage can be seen. This is because the estimator depends on the supply current samples. As the current increases, the estimator gets disturbed briefly, but becomes stable again as soon as the dc-link voltage reaches its required reference value, resulting in a steady current waveform.

6.2.3. Step in reactive power reference

The results in this section present the performance of predictive controller and the inductance estimation to a variation of 500VAR in reactive power reference.

Figure 6.13 shows the variation in reactive power and its reference. Also, it can be observed that even though a large variation in reactive power is seen, the active power reference is unaffected by it. Moreover, the tracking of reactive power to its reference variation does not show any significant steady state error.

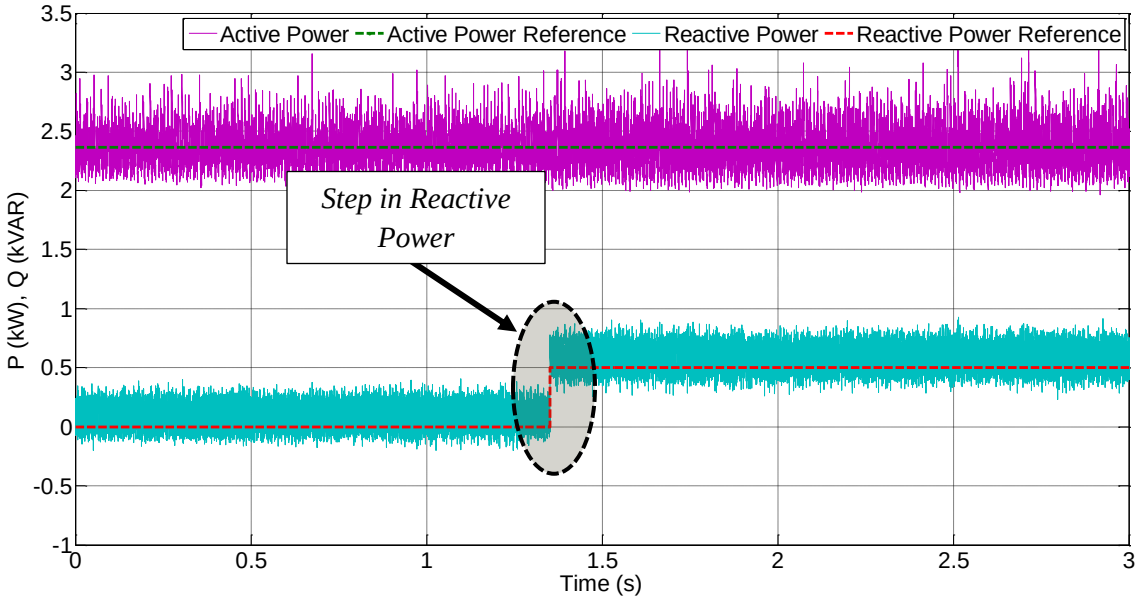


Figure 6.13: Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference

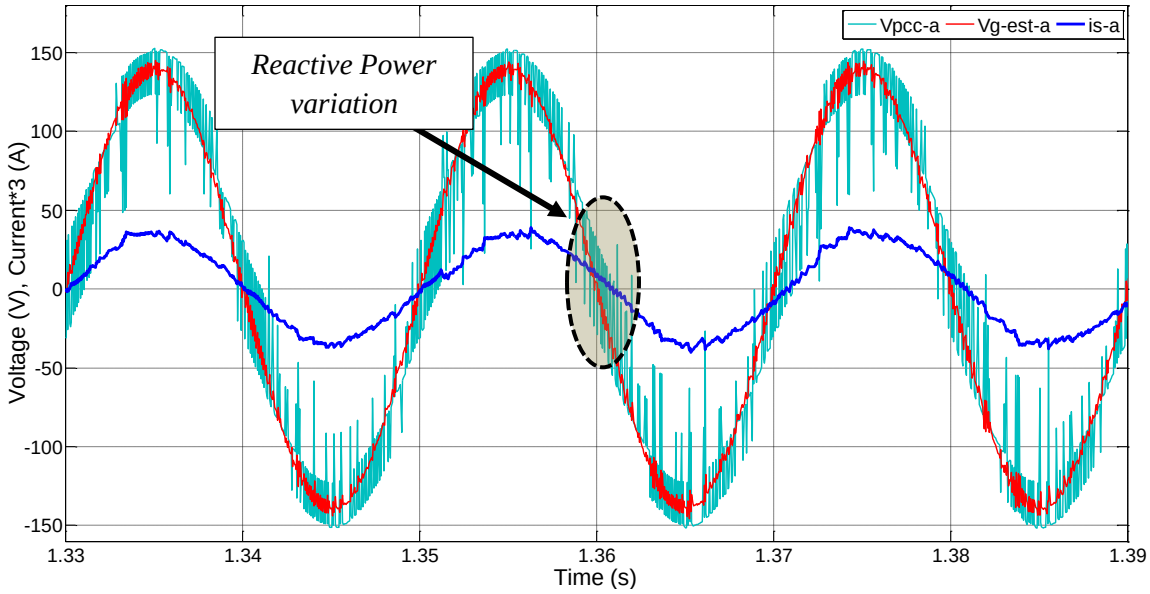


Figure 6.14: PCC voltage, supply current and grid voltage estimation – phase A for a step of 500VAR in reactive power reference

Figure 6.14 shows the supply current, voltage at the PCC and the grid voltage estimation. The effect of reactive power variation can be seen at time ~1.36s where the supply current leads the supply voltage due to a positive variation in reactive power.

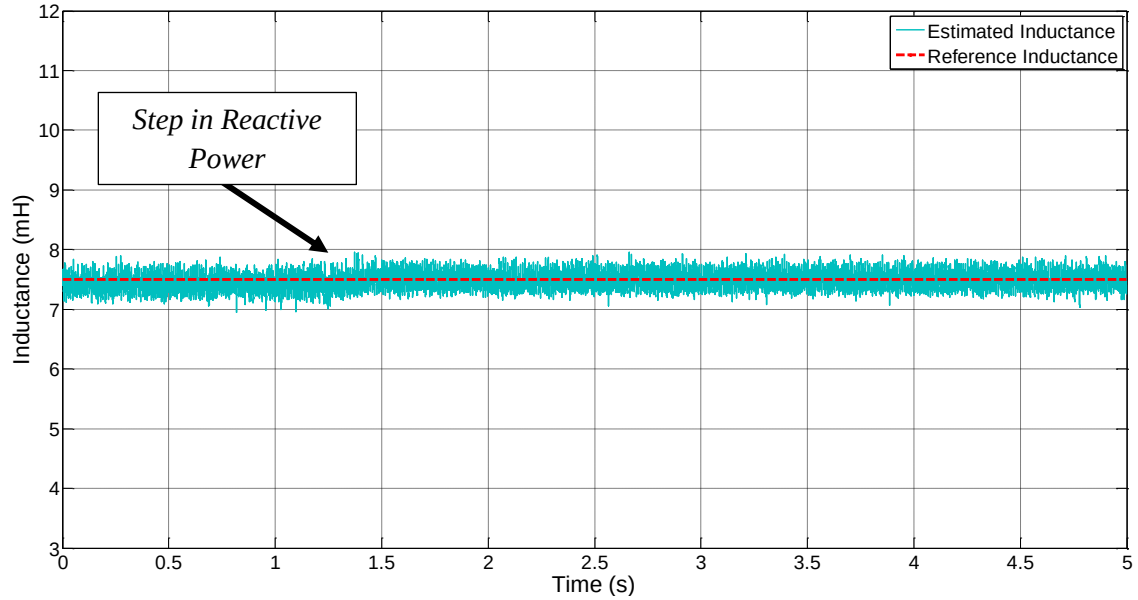


Figure 6.15: Total Inductance estimation with a step of 500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH

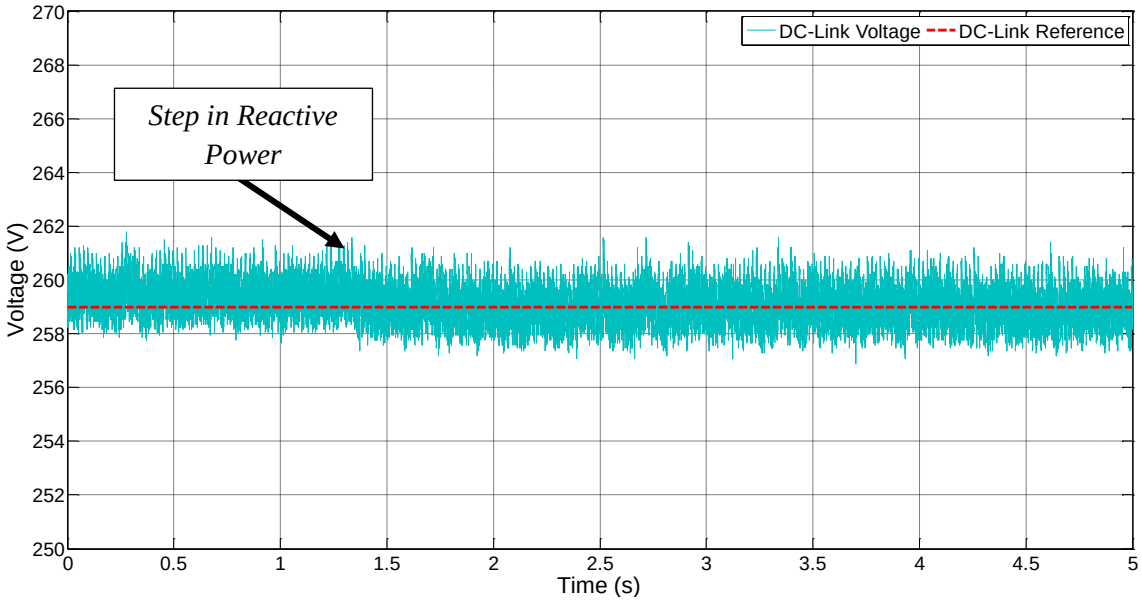


Figure 6.16: DC-Link voltage with reference for a step of 500VAR in reactive power reference

The total inductance estimation can be seen in figure 6.15 for a 500VAR step in reactive power. The inductance estimation responds to this variation without showing any noticeable errors. DC-link voltage response to a variation in reactive power is shown in figure 6.16 where the dc-link voltage shows a good reference tracking.

6.3. Experimental Results using a VARIAC

6.3.1. Model Predictive Control with grid inductance estimation in the presence of a step of supply voltage

This chapter presents results for the inductance estimation technique integrated within the predictive controller when a VARIAC, connected to the mains, was used. The VARIAC is an autotransformer and takes as input the voltage coming from the mains connection in the laboratory, stepping it up gradually from 0V to the user demand.

Since the VARIAC has copper windings wrapped around a steel core, it has inductive properties[113]. Figure 6.17 shows an equivalent representation of the VARIAC where *N* represents the number of coils in the autotransformer; *Input* is the VARIAC side

connected to the mains and *Output* refers to the regulated voltage used for the power converter[113]. *Sliding brush*, also called as *Carbon brush*, works such that when the regulating dial on the VARIAC is moved in a clockwise motion, the *Output* increases thus increasing the number of turns of the coil on the *Output*. Similarly, when the regulating dial is moved in an anti-clockwise motion, the *Output* decreases resulting in a decrease in the number of coils[6].

By increasing the voltage on the *Output*, due to an increase in the number of coils the inductance increases as well [113]. This effect can be seen in figures 6.18-6.23 where a sudden variation of ~66V amplitude in the VARIAC *Output* was introduced. The results show adaptability of the MP-DPC and the inductance estimator to a sudden variation in the supply voltage. Consequently, the PVS manufactured by CHROMA could have been used to carry out the same tests by setting the parameters; however, a VARIAC was preferred as it gives a more realistic transmission line condition with presence of inductance, resistance and capacitance.

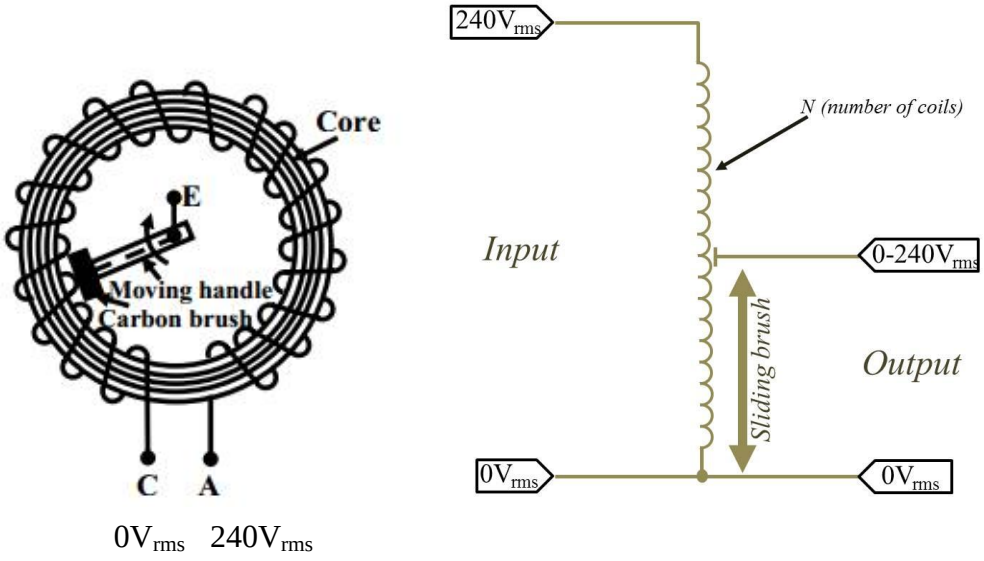


Figure 6.17: Equivalent representation of a VARIAC [113]

Figure 6.18 shows the PCC voltage, supply current and grid voltage estimation. For simplicity of explanation of the results in the text ahead, the two test regions have been labeled as ***A*** and ***B*** respectively. Where, ***A*** is for the case when the VARIAC *Output* voltage is ~33V and ***B*** for ~100V. The corresponding THD values are presented in table 6.1.

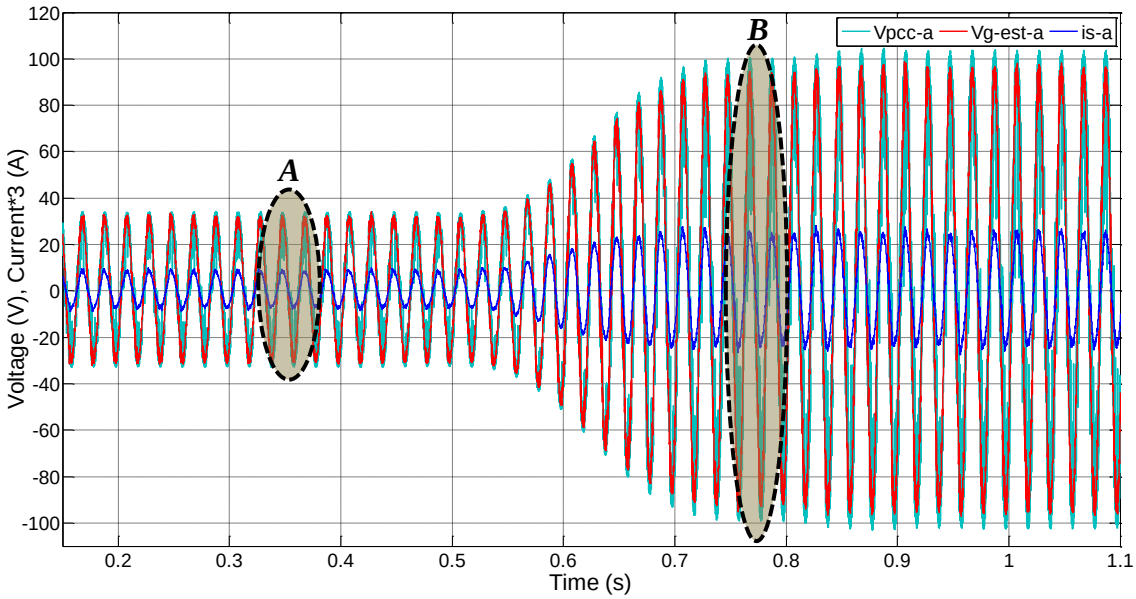


Figure 6.18: Step from ~33V to ~100V PCC voltage, supply current and grid voltage estimation – phase A

Figure 6.19 shows the case when the VARIAC *Output* was ~33V. Since the inductance estimation estimates the total line inductance correctly, the grid voltage estimation with a THD value of 3.3% can be seen to be much less distorted than the PCC voltage and the supply current maintains its quasi-sinusoidal pattern with a THD value of 8.6%.

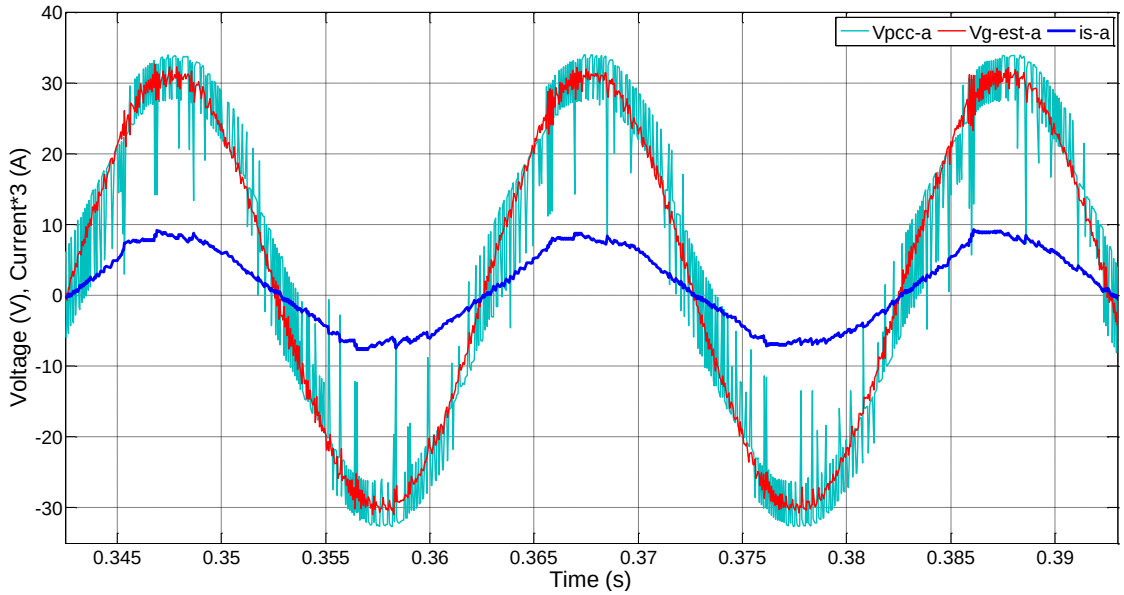


*Figure 6.19: **A** - ~33V in VARIAC. PCC voltage, supply current and grid voltage estimation – phase A*

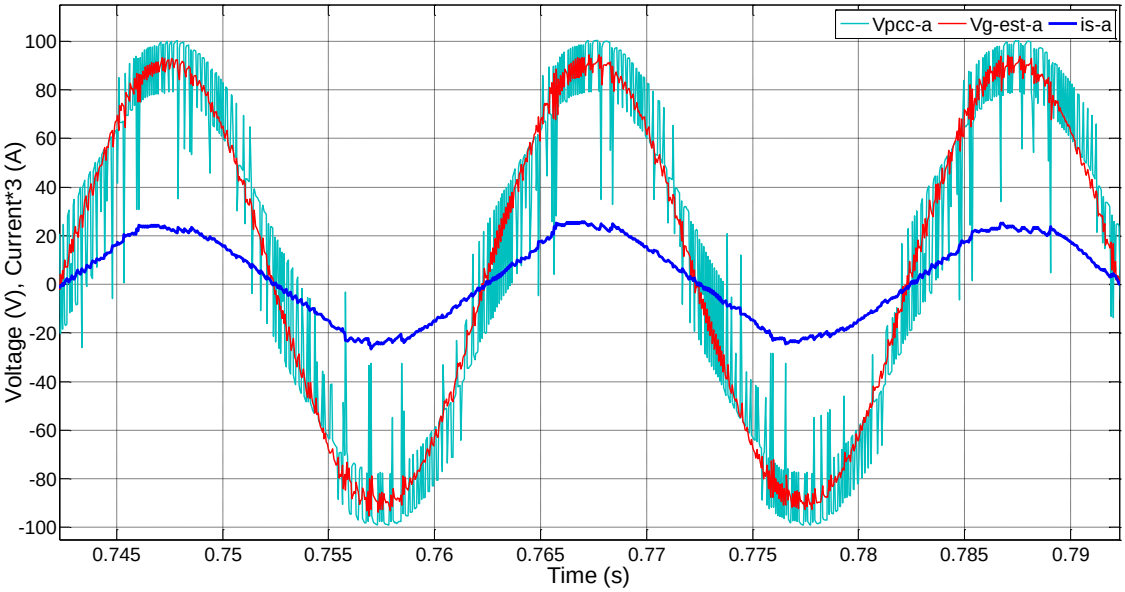


*Figure 6.20: **B** - ~100V in VARIAC. PCC voltage, supply current and grid voltage estimation – phase A*

Figure 6.20 shows case ***B*** when the VARIAC *Output* was varied to ~100V. Even after a sudden variation in the voltage as shown in figure 6.18, in figure 6.20 the estimator responds correctly by estimating the grid voltage with a THD value of 3.5% where the

PCC voltage shows more distortion than case ***A***. Since the total inductance on the line increases, the supply current THD reduces to 6.8% from 8.6% as in case ***A***.

The total inductance estimation is presented in figure 6.21. The variation takes place at ~0.55s. Since it takes about 0.15s for the VARIAC *Output* voltage to be stable, the inductance estimator gets stable around 0.7s in figure 6.21, giving an estimation of around 8.1mH. The physical 'grid inductance' installed on the practical system was 3.0mH, therefore, it can be seen that by varying the VARIAC *Output* voltage, the grid inductance increased by ~0.6mH. This shows that the VARIAC internal inductance can also be estimated. It can also be said that varying the VARIAC *Output* voltage increased the total grid inductance from 66.67% to 80% of converter input filter inductance, which is quite significant.

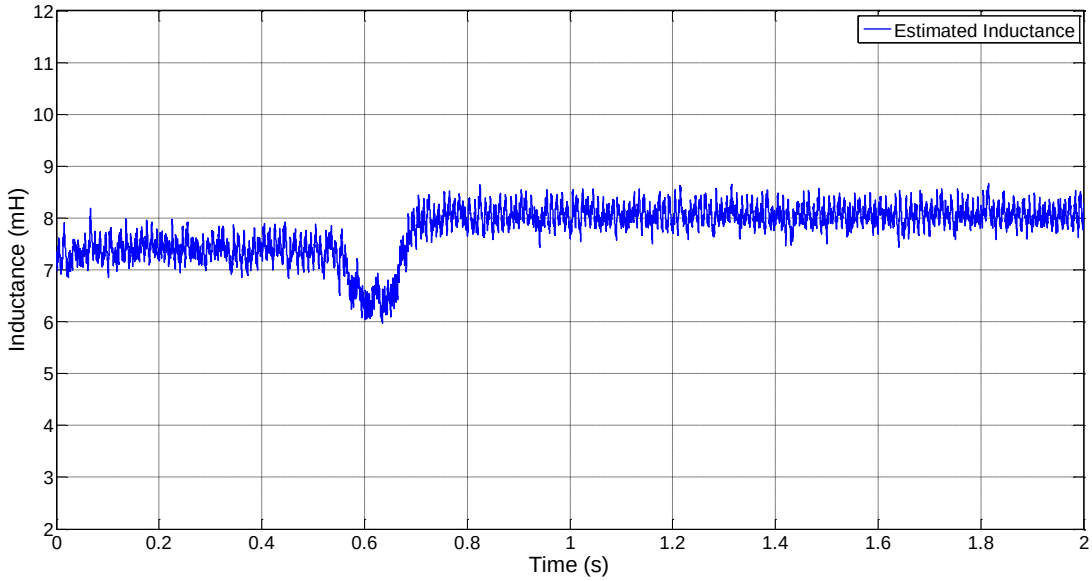


Figure 6.21: Step from ~33V to ~100V in VARIAC, Inductance estimation, $L_{estimation} = L_S + L_{VARIAC}$

Due to power limitations in the experimental setup, the supply voltage was not further increased to check the performance of inductance estimator. However, the presented results support the idea that even for a larger variation in grid inductance the estimator

will estimate the total inductance correctly and update the predictive controller in real-time.

Figure 6.22 shows the response of the dc-link voltage to this variation and figure 6.23 shows the corresponding active and reactive powers. Table 6.1 shows the relevant waveforms THD values for VARIAC operating points ***A*** and ***B***. An increase in the VARIAC *Output* inductance increases the THD of the PCC voltage; however, the grid voltage estimation maintains its THD to less than 4%.

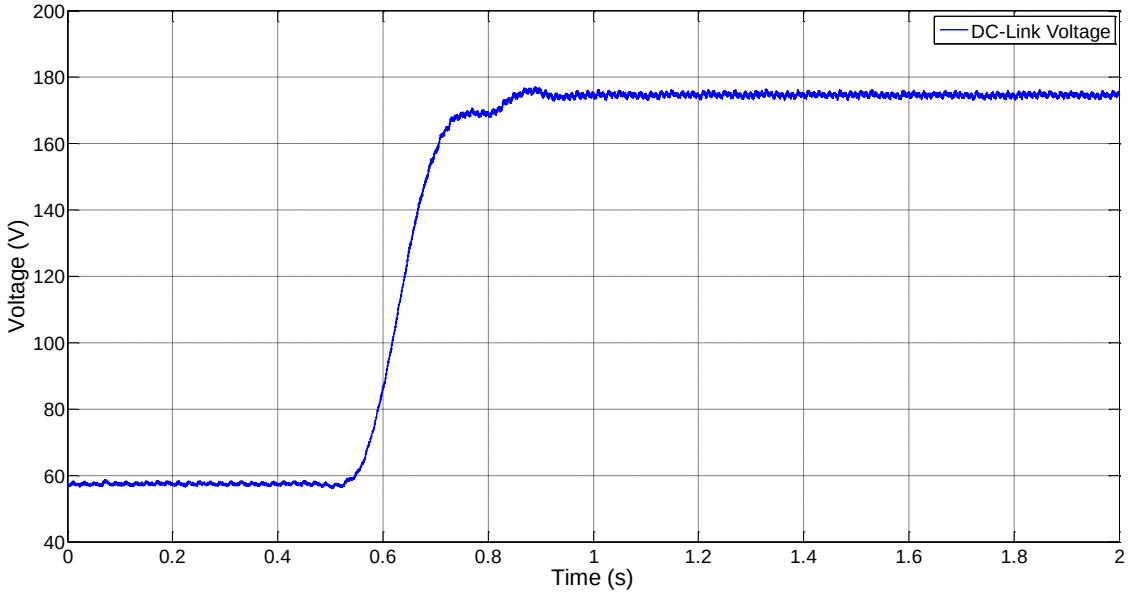


Figure 6.22: Step from 33V to 100V in VARIAC, DC-Link Voltage

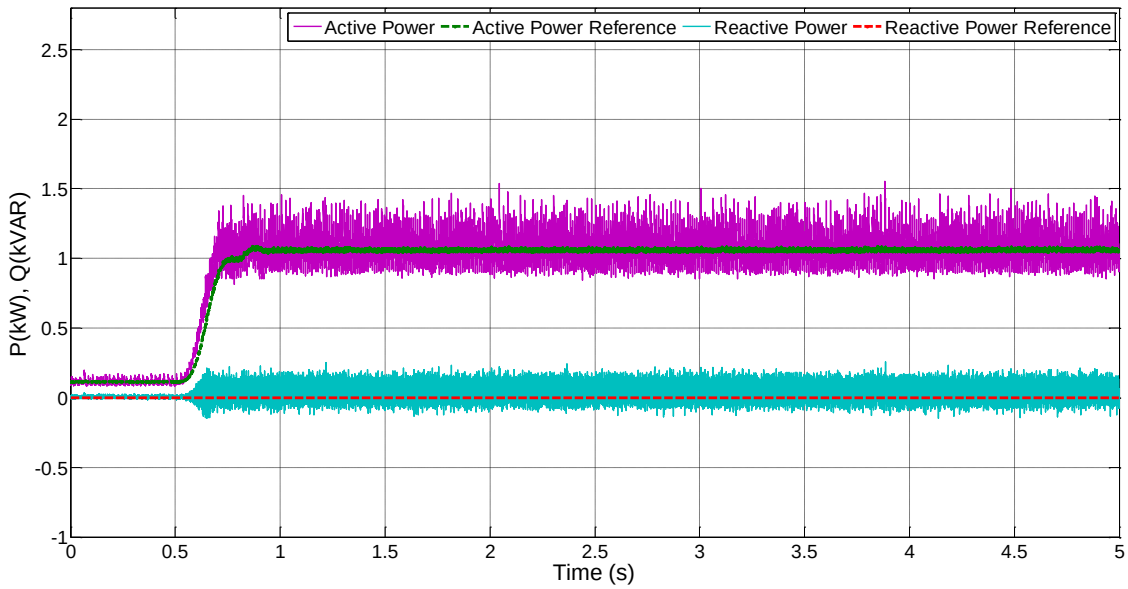


Figure 6.23: Step from ~33V to ~100V in VARIAC, Active and Reactive Power with reference

TABLE 6.1: THD values for 2 VARIAC operating conditions

L_S(mH), L_C (mH)	VARIAC Operating Points	THD_i (%)	THD_{Vpcc} (%)	$THD_{Vg\text{-}est}$ (%)
(3.0+L_{VARIAC}), 4.5	A	8.6	17.4	3.3
(3.0+L_{VARIAC}), 4.5	B	6.8	18.6	3.5

The results presented in sections 6.2 and 6.3 have been carried out using the estimation method 1 tested using MP-DPC on a three phase two level rectifier.

6.4. Comparison between the simulation and experimental results using estimation method 1

Table 6.2 shows a comparison between the THD values of the simulation results and the experimental results for the tests conducted in section 6.2. The proposed estimation method has only been tested with a 3.0mH supply inductance due to limitations on the practical system. However, referring to the simulation results in chapter 5, the estimation method can also be applied in cases when the grid inductance is more than 3.0mH; even for cases when the SCR is less than 4.

TABLE 6.2: Comparison of THD values between simulation results and experimental results using programmable voltage source

L_S(mH), L_C (mH)	Operating Conditions	$THD_{i-Exp.}$ (%)	$THD_{i-Sim.}$ (%)	$THDv_{g-est\ Exp.}$ (%)	$THDv_{g-est-Sim.}$ (%)
3.0, 4.5	V_{dc}* = 261	3.77	3.67	2.9	1.14
3.0, 4.5	Q* = 0VAR	5.31	3.91	2.66	1.16
3.0, 4.5	Q* = 500VAR	5.62	4.08	2.9	1.18

For a constant value of dc-link voltage reference equal to 261V_{dc}, the supply current has a THD value, $THD_{i\text{-}Exp.}$, of 3.77% while the estimated grid voltage has a THD value, $THD_{Vg\text{-}est\text{-}Exp.}$ of 2.9% respectively. For the same test conditions, the simulation results show a supply current THD, referred as $THD_{i\text{-}Sim}$, with similar results as in experiment whereas the estimated grid voltage THD is reduced in simulations as compared to experimental results as there is a higher ripple present on the PCC voltage in the experimental system. Table 6.2 also shows results for a step variation in the reactive power reference from 0VAR to 500VAR. Since the supply current amplitude does not change and only the phase shift occurs between the supply voltage and supply current, the THD values before and after the reactive power variation do not change significantly. It is observed from the above analysis and results presented in table 6.2 that the MP-DPC responds well by maintaining synchronization between the supply voltage and supply current unless a positive reactive power was deliberately injected that resulted in the supply current leading the supply voltage. Moreover, the integration of the proposed grid inductance estimation method within the predictive controller does not lose its stability and estimation when tested under different scenarios.

For ease of noticing the comparison between simulation and experimental results, figures 6.24-6.31 show experimental results using the programmable voltage source and simulation results together to observe the response of the dc-link voltage to a step variation of ~35V in its reference value, active power, reactive power to a step variation of 500VAR in its reference value and the response of inductance estimator to these variations.

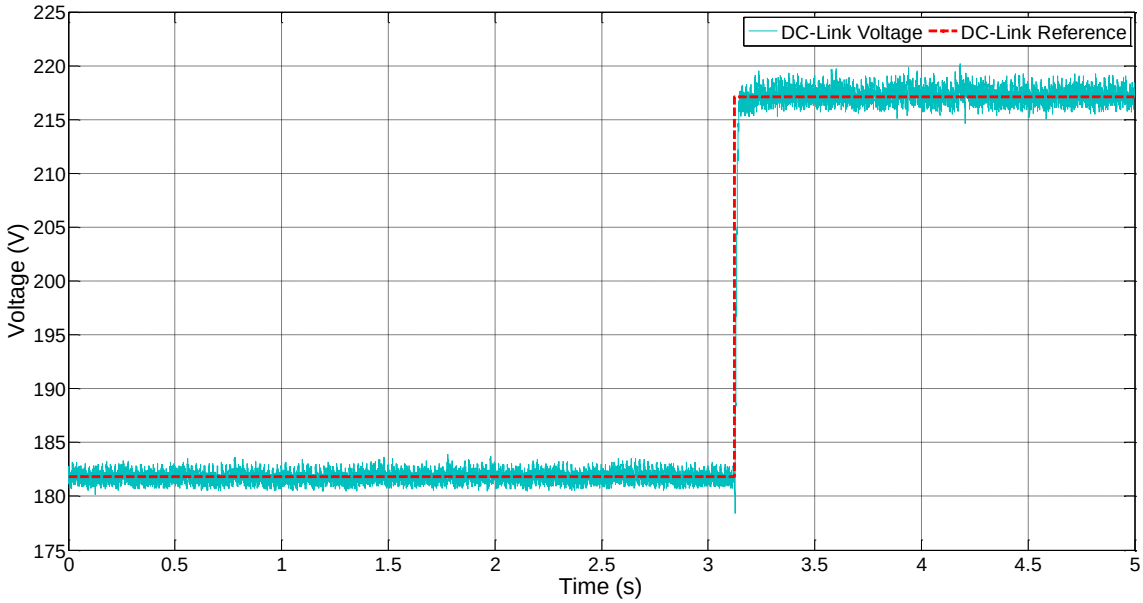


Figure 6.24: DC-link voltage response to 35V step in DC-link voltage reference – experimental result using a programmable voltage source

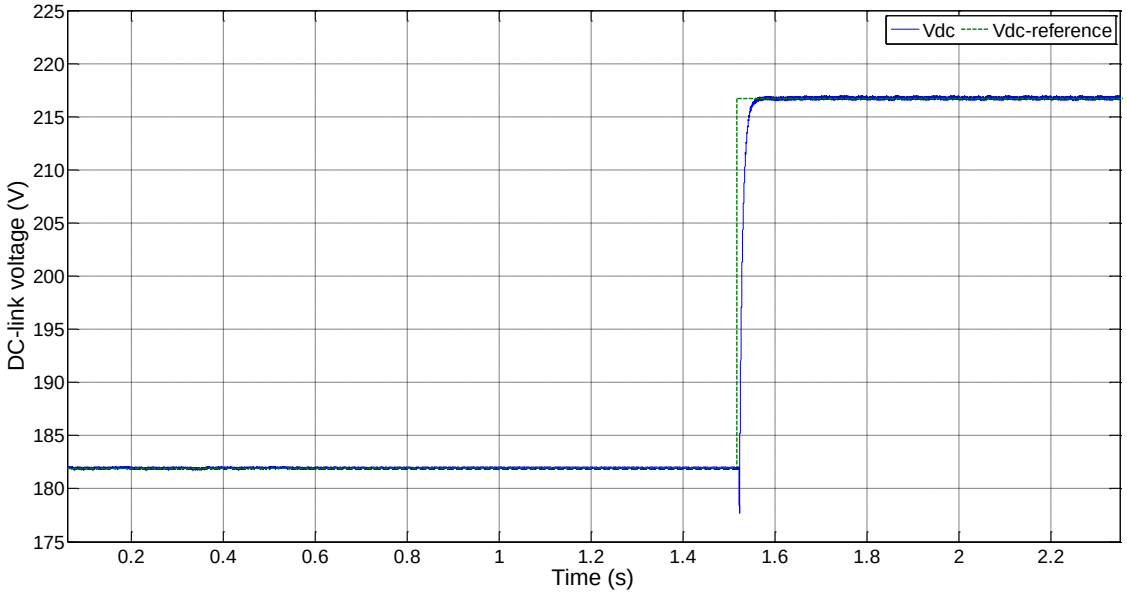


Figure 6.25: DC-link voltage response to 35V step in DC-link voltage reference – simulation result

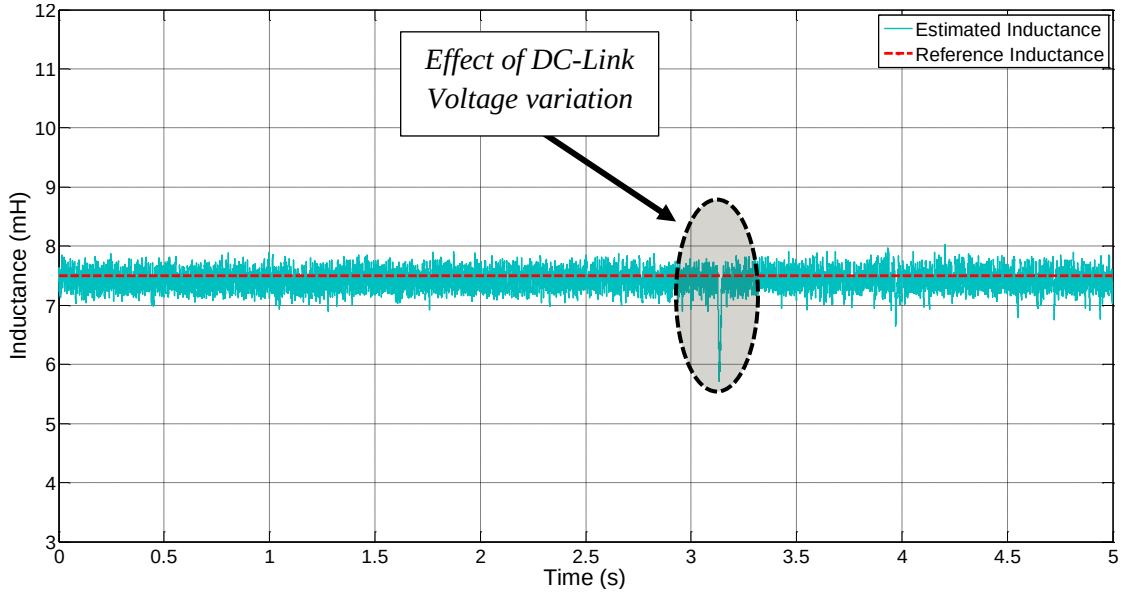


Figure 6.26: Total Inductance estimation with 35V step in dc-link voltage reference – experimental result using a programmable voltage source. L_S = 3.0mH, L_C = 4.5mH

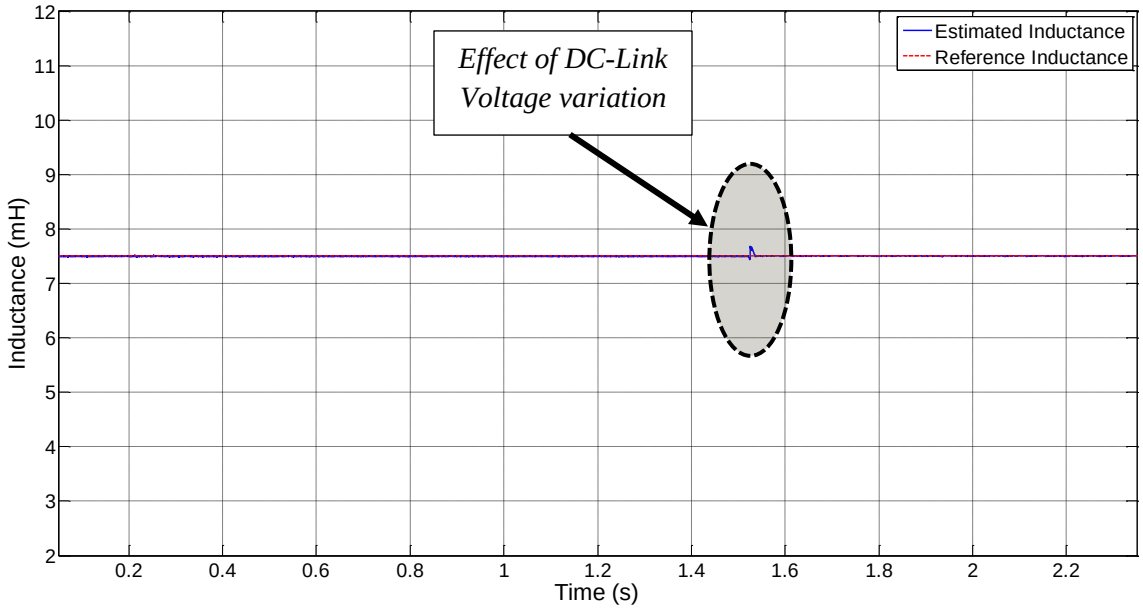


Figure 6.27: Total Inductance estimation with 35V step in dc-link voltage reference – simulation result. L_S = 3.0mH, L_C = 4.5mH

The results shown in figures 6.24-6.27 show a good comparison between the simulation and experimental results for a 35V step in the dc-link voltage reference. Moreover, the total inductance estimation remains stable around 7.5mH. The major difference between the experimental and simulation results that has been observed is the additional presence of the ripple on the experimental results that is due to measurement noise. Further improvement, if needed in the experimental system, can be added by designing low pass filters for cancellation of noise in the estimation.

Results in figures 6.28-6.31 show a comparison between the experimental and simulation results to a 500VAR step in the reactive power. The experimental results for the active and reactive power and the estimated total inductance show a larger ripple as compared to the simulation result.

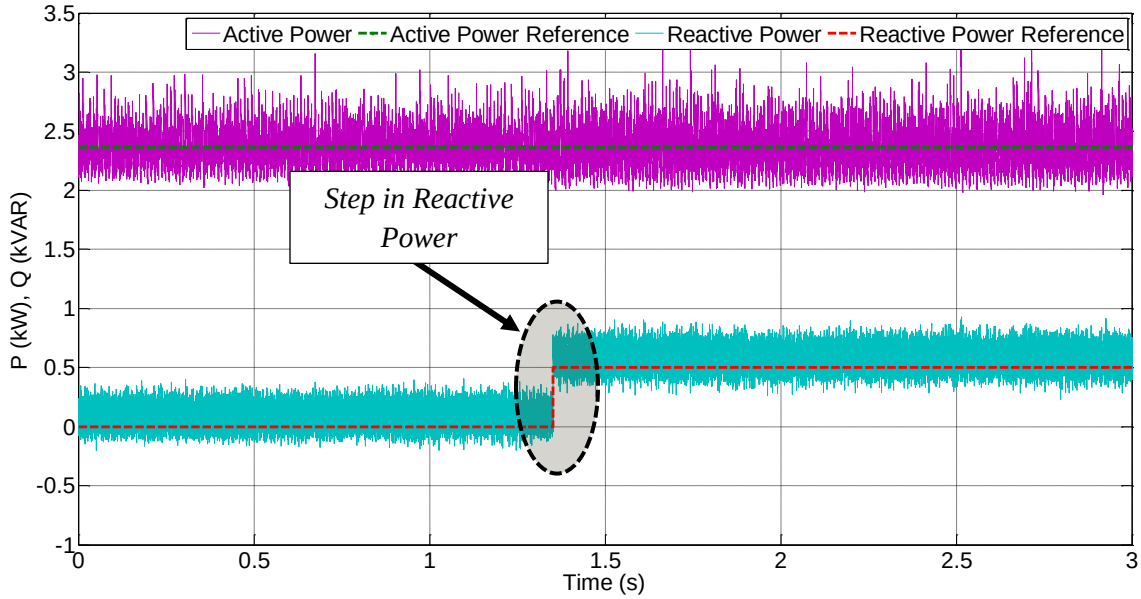


Figure 6.28: Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference – experimental result using a programmable voltage source

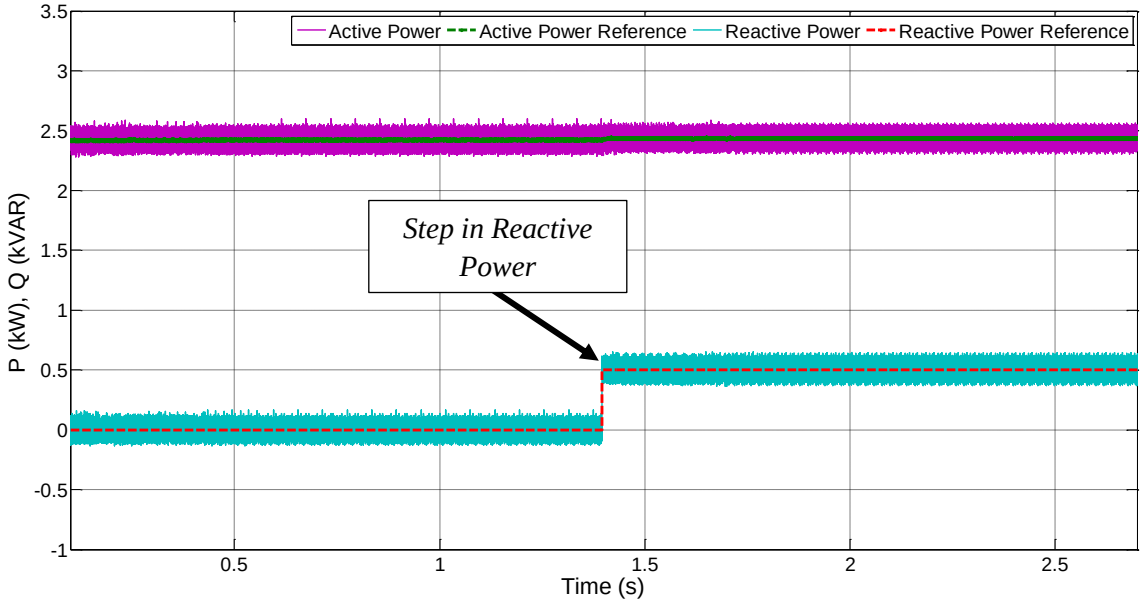


Figure 6.29: Active power and reactive powers with their respective references for a step of 500VAR in reactive power reference – simulation result

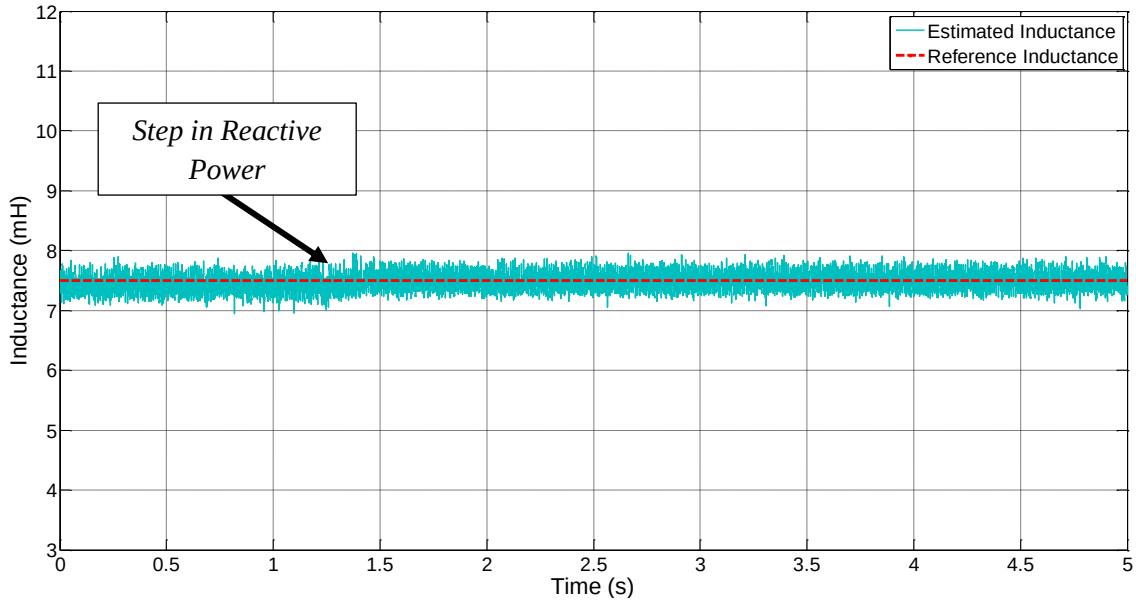


Figure 6.30: Total Inductance estimation with a step of 500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH – experimental result using a programmable voltage source

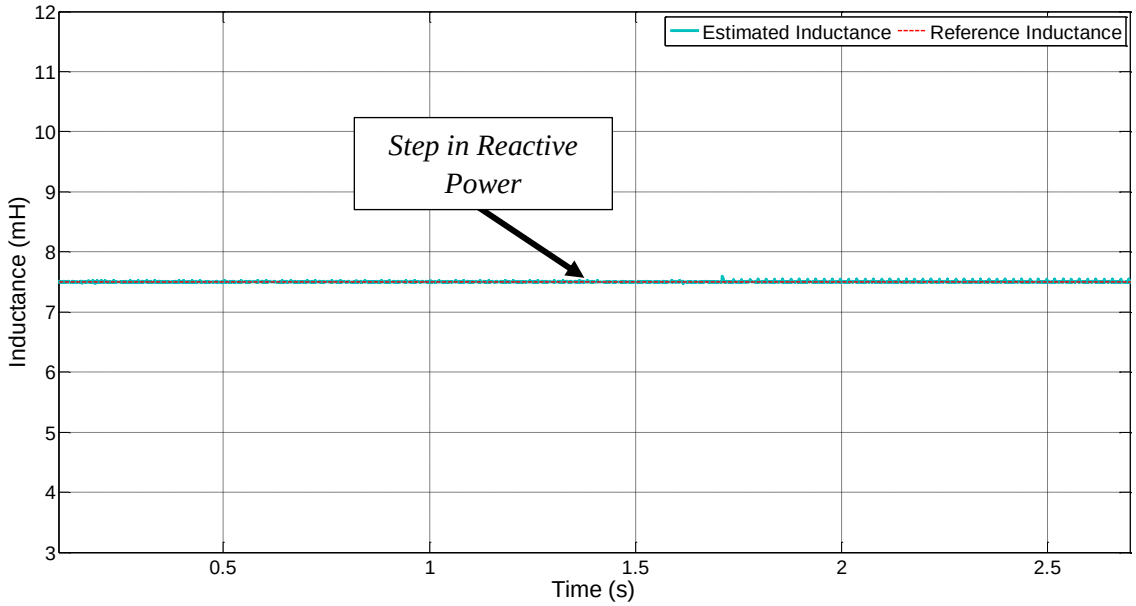


Figure 6.31: Total Inductance estimation with a step of 500VAR in reactive power reference, L_S = 3.0mH, L_C = 4.5mH – simulation result

Apart from the presence of ripple, the simulation and experimental results match each other and respond accurately to a 500VAR variation in reactive power reference.

So far, results have been presented using the inductance estimation method 1 on MP-DPC. The next section shows experimental results for inductance estimation method 2.

6.5. Comparison between the simulation and experimental results using estimation method 2

The figures presented in this section show a comparison between the experimental and simulation results under the same operating conditions. Estimation method 2 has been tested in the experimental system using a 0.5mH grid inductance such that the grid inductance has been varied from 0.5mH to approximately 0mH and then back to 0.5mH using a bypass switch, thus showing a transient behavior of grid inductance variation. Figure 6.32 and figure 6.33 show the experimental and simulation results for a variation of 0.5mH in grid inductance.

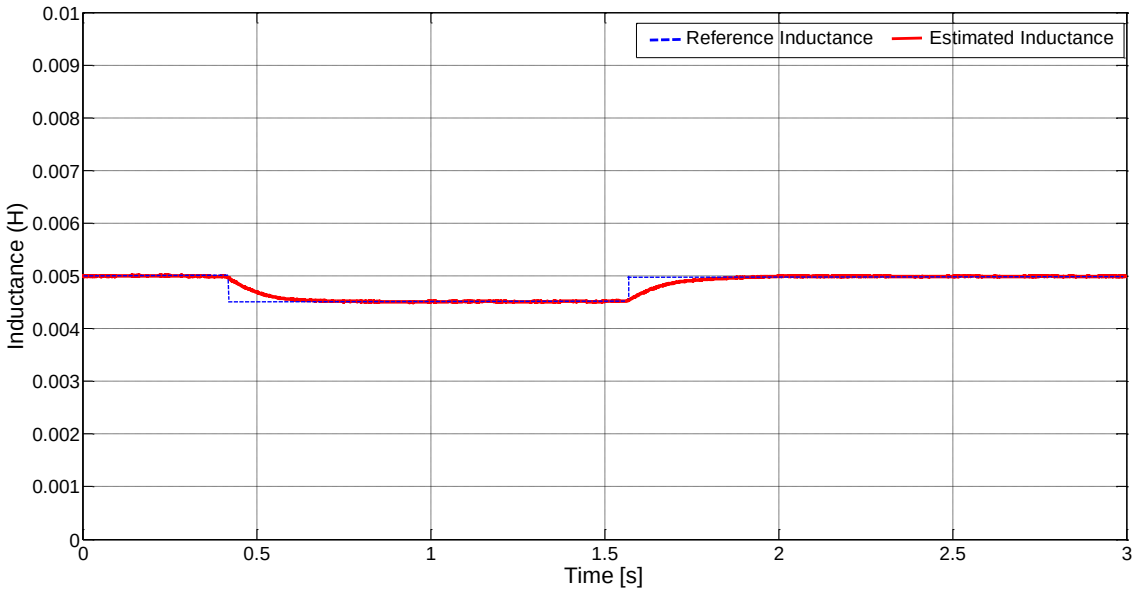


Figure 6.32: Total Inductance estimation with a 0.5mH step in grid inductance, L_S = 0.5mH, L_C = 4.5mH – experimental result using a programmable voltage source

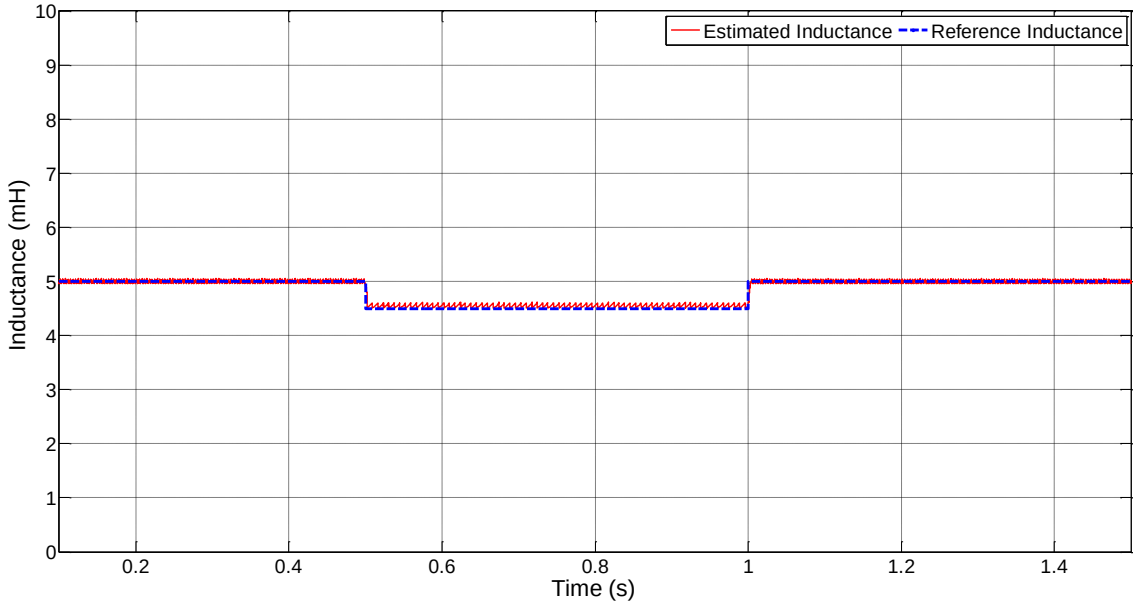


Figure 6.33: Total Inductance estimation with a 0.5mH step in grid inductance, L_S = 0.5mH, L_C = 4.5mH – simulation result

Both in simulation and experimental results the estimated inductance responds accurately to the actual variation in grid inductance. However, the estimated inductance in the experiment test took slightly longer to reach the desired value due to the practical computational effort of the DSP involved in the estimation algorithm. In order to test the experimental performance of estimation method 2 to a higher value of grid inductance, results in figure 6.34 show the total estimated inductance when a grid inductance of 3.0mH was used.

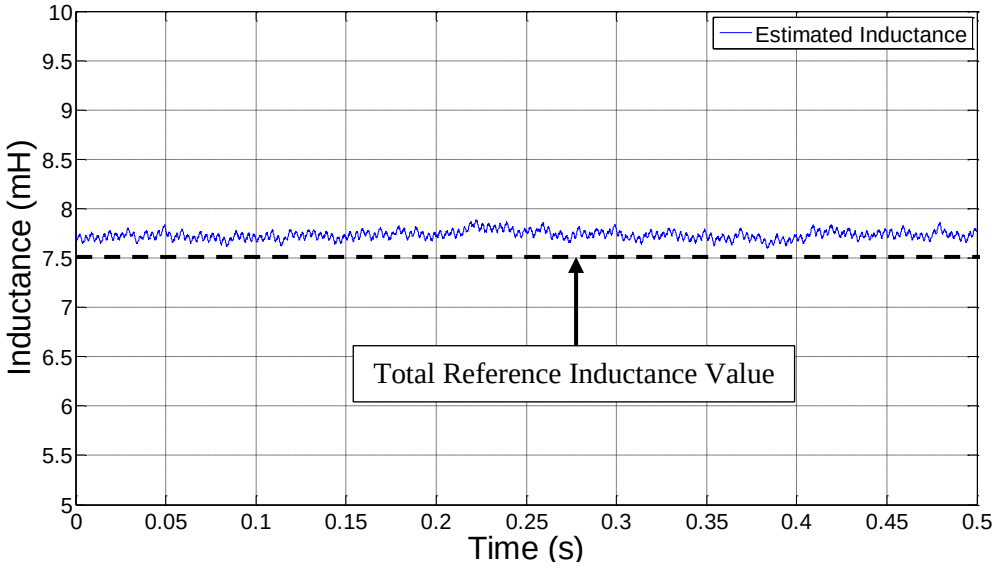


Figure 6.34: Total Inductance estimation, L_S = 3.0mH, L_C = 4.5mH, experimental result

It was observed in figure 6.34 that when a higher value of grid inductance was used,estimation method 2 resulted in a steady state error of approximately 0.5mH. In figure 6.35, the supply current, grid voltage estimation and PCC voltage are shown. As the total estimated inductance is erroneous, it is reflected in a ripple dominated grid voltage estimation and supply current with THD greater than 4%.

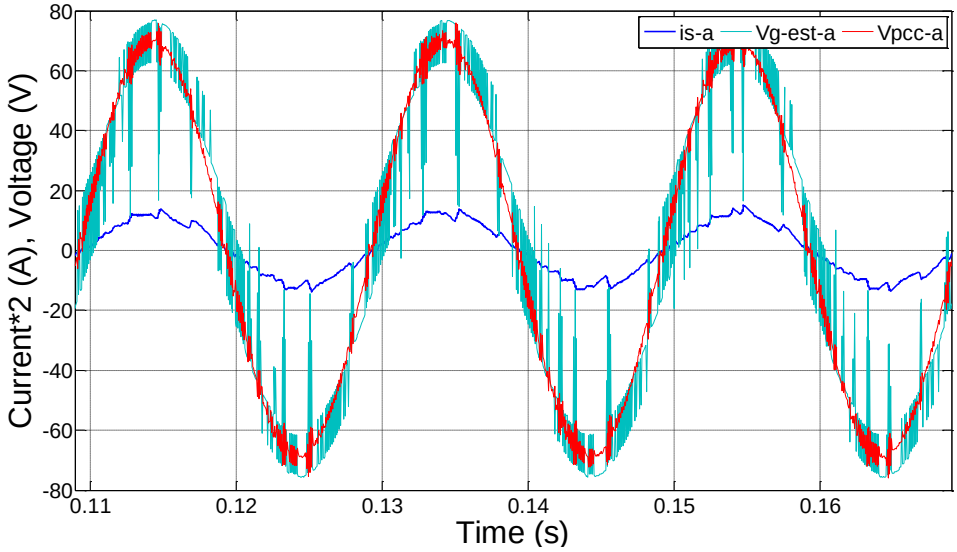


Figure 6.35: Grid voltage estimation, supply current and PCC voltage, L_S = 3.0mH, L_C = 4.5mH, – experimental result

The simulation results presented in section 5.5 for estimation method 2 when the grid inductance is varied to high values show better results as compared to when applied on the experimental setup. It is observed that when applied on the practical system, estimation method 2 is sensitive to hardware delays present on DSP/FPGA. The proposed estimation method 2 does not take into account these delays. For further improvement and implementation of this method, it is suggested that all measurement delays are taken into account.

6.6. Conclusion

This chapter started by briefly explaining the experimental setup and then presented experimental test for the proposed inductance estimation method 1 integrated within the MP-DPC using on the supply side of the converter both a Programmable Voltage Source manufactured by Chroma and an Autotransformer (VARIAC), one at a time. The estimation method shows good performance under different operating conditions that included tests with a constant dc-link voltage reference, with variation of the dc-link voltage reference, variation of the reactive power and under a large step (~67V) in the input supply voltage.

A grid inductance of 3.0mH was physically installed in the practical system to emulate actual grid impedance, thus making the total line inductance equal to 7.5mH. The inductance estimation algorithm estimated the total inductance on the line without exceeding 1% steady state error. The point of measurement for the voltage and supply current, as explained in figure 6.1, were at the PCC after the grid inductance.

A 67V step in VARIAC resulted in the total grid inductance to increase from ~67% to 80% of the converter input filter inductance. Moreover, the method used for estimation

of the grid voltage presents an advantage by avoiding the use of complex low pass filtering techniques to achieve the estimation of fundamental voltage at the PCC that may require higher computational efforts on the DSP. Though the estimation algorithm and the MP-DPC have been tested on the practical system using only a 3.0mH grid inductance due to practical system limitations, the proposed estimation algorithm can be tested for higher values as supported by the simulation results of Chapter 5. Appendix E shows the oscilloscope captured results carried out using the *Programmable Voltage Source* for method 1 and method 2 estimation algorithms using MP-DPC.

The next chapter presents concluding remarks for the work carried out in this project and makes suggestions on further improvements to the work.

Chapter 7: Discussion, Conclusion and Further Work

7.1. Background

In recent years, grid-connected converters have gained popularity for renewable energy systems integration, distributed generation connection and other applications. It is very frequent that the grid to which these systems are connected is not stiff, like micro grids for example. Small grid parameter variations in these systems can substantially affect the performance of the converter control. This grid parameter variation can be regarded as a variation in grid impedance that is mostly dominated by variation in grid inductance. For classical grid-connected converter control strategies that include the use of PLLs for phase synchronization, the tuning of the PI controller inside the PLL gets affected by a variation in grid impedance when this is significant compared to converter impedance. Hence, this affects the control performance for SCR values lower than 10. It is possible to re-tune the PI controller on the basis of the value of grid impedance once it is known, however, this value can vary with time and grid operative condition, therefore large look-up tables and gain scheduling techniques are need for controller tuning. Earlier methods that have been proposed in the literature present some solutions to solve this challenging task, but do not show promising results in case of a Weak Grid scenario. However, most methods that have been proposed to estimate variation in grid impedance have been executed offline and the controller does not get updated in real-time with the latest variation in grid impedance.

Therefore, taking the above issues related to grid-connected converters into consideration, the work presented in this thesis chose to use a Model Based Predictive Direct Power Control (MP-DPC) and also presented two grid impedance estimation methods. A comparison between the performances of the two estimation techniques

when integrated within the MP-DPC has been given in the thesis and will be summarized in the following sections.

Model predictive control approaches to control power electronics systems have recently captured the attention of the international research community due to their easier concepts and the advantages they provide: inclusion of nonlinearities in the control system and also multivariable control within a single control structure thus avoiding the use of cascaded control loops such as external and internal PI/PID controllers in case of a voltage oriented control. Moreover, model predictive control provides a fast dynamic response responding to system transient variations quickly.

As mentioned in chapters 2 and 3, for grid synchronization and reference calculations when the required phase angle is calculated with the help of PLL techniques, the control performance gets affected in case of a low SCR and it becomes particularly challenging to modify control and PLL parameters to adapt to different grid conditions. For this reason direct power control, in conjunction with the model predictive control has been used as it provides control of the power factor (grid synchronization) by directly controlling active and reactive powers and avoids the use of PLLs. On the other hand, predictive control also has a drawback. If there is a model parameter mismatch, i.e. the value of the parameter used in the model is different than its actual value, the control performance deteriorates. Hence, while using predictive control for grid connected converters, we have to ensure that the grid impedance is known, above all if its value is substantial compared to the converter input impedance. This is the reason why in this project MP-DPC has been proposed in conjunction with two novel impedance

estimation methods so the control can be updated online by providing fast and robust operation.

7.2. Grid impedance estimation techniques

In this project two grid impedance estimation techniques have been proposed in chapter 4 that have been referred to as *Method 1* and *Method 2*, respectively. Both these novel methods estimate the variation in grid impedance in real-time and update the MP-DPC in real-time with the latest variation in its value, thus providing a good control performance under low SCR values as well.

Method 1 works by imposing a constant grid voltage magnitude at two consecutive sampling instants. The grid voltage in this case was referred to as the voltage at the low-voltage substation while the grid impedance is considered between the low-voltage substation and the point of common coupling (PCC) where the measurements are taken for the converter input.

The grid voltage magnitude at the AC-side of the grid-connected converter was modeled for two sampling instants, *k-1* and *k*, such that it included the supply currents at the *present* and *past* instants, grid impedance term, converter input filter impedance and converter input voltage at the *present* and *past* instants. The latter values are evaluated by means of the dc-link voltage and the optimum switching signals obtained from the minimization of the cost-function.

Once the grid voltage magnitudes were modeled, the total line inductance was equated such that the total line inductance comprised of the usually known converter input filter inductance and the variations in grid inductance. Though only grid inductance has been

considered in the proposed estimation algorithm, this can be modified to take into consideration also the variation in grid resistance.

The simulation and experimental results using ***method 1*** show a robust performance of the estimator to a frequent variation in grid inductance value. The tests were first conducted for fixed values of grid inductance with values of 50%, 100% and 200% of the converter input filter inductance. The estimator response was excellent and showed hardly any significant steady state errors. The predictive control was updated as well and maintained a sinusoidal current waveform with a THD value less than 5% even in cases when the grid inductance has the same value as the converter input filter inductance. Furthermore, the tests were then conducted for a frequent variation in the grid inductance value. The grid inductance was varied from 0.5mH up to 17.5mH while the converter input filter inductance was fixed at 4.5mH, meaning up to SCR values less than 3. Even for such large variation in grid inductance, the estimator did not loose its effectiveness and estimated the total inductance accurately while still updating the predictive controller in real-time. The control variables, i.e. active power, reactive power and the dc-link voltage, followed their respective references with less than 1% steady state error. As the grid inductance increased, the total inductance on the line increased as well. Thus, the ripple on the supply current and its THD value decreased to less than 3% even under SCR values less than 3.

Another highlight of the proposed method was the grid voltage estimation. Once the variation in grid inductance was known, the grid voltage was estimated to replace the PCC voltage being used in the MP-DPC. The advantage of using the estimated grid voltage instead of the PCC voltage is that the need of advanced low pass filtering

techniques to filter out the high frequency ripples on the PCC voltage were not needed anymore.

The drawback of estimation *method 1*, however, is that it cannot work under unbalanced grid voltages since the estimator operating condition requires a constant grid voltage magnitude. Though the results with unbalanced grid voltage have not been included in the thesis, it can be very well understood that under unbalanced grid voltages the estimator would loose its performance.

For this reason, the inductance estimation *method 2* was proposed to estimate the variation in grid inductance with the knowledge of supply currents and not the magnitude of the grid voltage. The working principle of the estimation *method 2* is based on the minimization of the error between the estimated supply current and the actual current; the grid inductance value that minimizes the error is selected as the optimum value to be used to update the MP-DPC. This calculation takes place at every sampling instant. The minimization of the difference between the actual current and the estimated current is referred to as the "cost-function optimization", in similar way to the process in MP-DPC for optimum switching signal generation. The estimation *method 2* not only works in cases of low SCR values, but the results show that it even works under unbalanced grid voltage conditions as shown in section 5.4.6 in chapter 5. However, the presence of a larger ripple in the estimation is seen in *method 2* as compared to the estimation results of *method 1*. The reason for this is because the upper and lower integer limits need to be re-tuned in cases of high grid inductance values. Currently, the tuning of these parameters are purely based on empirical methods,

however, further work will investigate methods to provide auto-tuning of these bands to provide better quality estimation under low SCR cases.

7.3. Further work suggestions

The work presented in this thesis is focused on two grid impedance estimation techniques used in conjunction with a Model based Predictive Direct Power Control. The proposed methods have been implemented on a standard three phase two level converter topology used as a grid connected AFE. The reason for using a two-level converter was to prove the proposed techniques on a simple system before progressing onto a more advance multilevel converter topology, most commonly used in these applications, such as Cascaded H-Bridge multilevel or Modular Multilevel Converter, for example. Further research may be based on the following topics:

1. *Including a grid resistance term*

   The proposed estimation techniques have considered the grid impedance model to be significantly dominated by inductance; hence the estimation for a variation in grid inductance has only been carried out. The variation in grid resistance, as suggested in the literature, is not as significant as compared to the variation in inductance. While the presence of resistance affects the magnitude of the voltage at the PCC, the presence of inductance not only affects the magnitude, but also introduces a phase shift. Thus, the variation in grid inductance becomes more important to compensate. The proposed estimation methods can be modified such that the total grid impedance can be estimated collectively instead of grid inductance and its resistance separately. Though this may give a better representation of the grid model, it may also introduce more complex algorithm and higher computational time. Chapter 4.4.4 gives an

insight into how the estimation algorithm can be modified with inclusion of the resistive term.

2. *Use of a modulation scheme within the MPC*

In the work presented, the control strategy used for the control of power converter is a traditional Finite Set Model Predictive Direct Power Control. The switching signals are generated based on the optimization of a pre-defined cost-function such that at each sampling interval the switching combination that gives the minimum difference between the reference value and the predicted value of the control variable is selected to be applied as the optimum switching signal. It is possible that the same switching signal gives the least error for three or more sampling intervals, thus resulting in a variable switching frequency of the power converter.

In order to overcome the problem of variable switching frequency and instead provide the converter with a fixed switching frequency for improved power quality, a modulation strategy integrated within the MP-DPC needs to be further researched and tested in conjunction with the proposed grid impedance estimation algorithms.

A modulated model predictive direct power control has been implemented on a three phase two level converter as proposed in [92], however the estimation of grid impedance becomes challenging. The modulated predictive control has the same working principle as a space vector modulation, with the difference that the predictions and references of the control variable are used in a cost function to generate the switching signals instead of using a modulation signal. The switching signals are applied for the calculated application times, thus providing the converter with a fixed switching frequency.

The impedance estimation algorithms rely on the optimum switching signals generated by optimization of the cost function and are applied according to each of the active vectors' application times as calculated in [92]. Therefore, it was observed that it becomes computationally challenging to apply the estimation algorithms with a modulated predictive control as there are 7 switching transitions within a sampling period (see chapter 2.3.3.) as compared to only one transition in case of a finite set model predictive control. The work in this case is currently on-going to suggest methods for improvements in the control system.

3. *Application on a multilevel topology*

Multilevel converters such as cascaded H-bridge or other topologies are mostly used for grid connected applications since they are capable to handle high power reducing the stress on the devices and modular multilevel converter provide an improved power quality to the converter operation as compared to a classical two-level converter. Now that the proposed grid impedance estimation algorithms have proven to give a robust performance using MP-DPC on a three-phase two-level converter, the idea can be expanded on multilevel converters as well. The impedance estimation algorithm would just need to be updated with converter input voltages that would consist of a higher number of converter voltage levels (5 in case of a 5-level converter or 7 in case of a 7-level converter). A challenging task associated with the control of multilevel converters is the control of independent dc-link voltages, particularly in case of a Cascaded H-Bridge converter.

4. *Performance under a distribution network*

   The proposed methods have been tested for a single converter connected on a transmission line. To further support the efficacy of the proposed methods it would be desirable to explore the performance of the controller and the impedance estimation algorithm in presence of non-linear loads or other loads connected on the distribution bus.

To conclude, the work presented in this thesis has presented a good base for further exploration in this highly demanding task as the future electrical grid in the coming years would demand a better control structure. With the inclusion of more electrical energy sources onto the transmission line and an increased presence of non-linear loads, the knowledge of variation in grid parameters become critical for the control of power converters. The above mentioned suggestions for further work in this topic can be explored to further improve performance of grid connected converters.

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Appendix A: Short Circuit Ratio (SCR) Calculations

Short circuit ratio is defined as the ratio of the short circuit power (SCP) to the base power (S_{base}). The SCP at the point of common coupling in a three phase system (equivalent weak grid circuit diagram shown in figure A1) is defined as:

$$SCP = i_S \cdot v_{grid(LL)} \tag{A1}$$

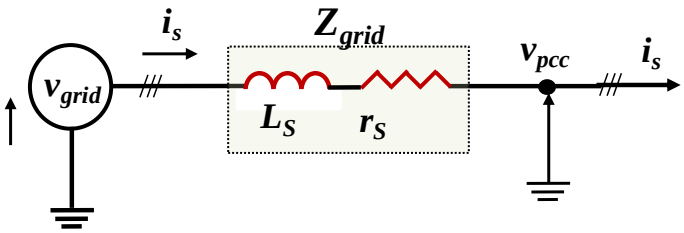

Figure A1: Equivalent circuit diagram of a weak grid

Where, i_s refers to the supply current and the $v_{grid(LL)}$ is the line to line grid voltage. The line to line grid voltage in a three phase system is equal to $\sqrt{3} \cdot v_{grid(PH.)}$. Furthermore, the SCP can be rewritten by transforming the supply current in terms of line to line grid voltage and grid impedance as:

$$SCP = \frac{v_{grid(LL)}}{Z_{grid}} \cdot v_{grid(LL)} \tag{A2}$$

$$\rightarrow SCP = \frac{\left(v_{grid(LL)}\right)^2}{Z_{grid}} \tag{A3}$$

Where, Z_{grid} is the grid impedance calculated as:

$$Z_{grid} = r_S + j\omega L_S \tag{A4}$$

The base power, S_{base}, for a three phase system is the rated power at the point of common connection and is calculated as:

Appendix A: Short Circuit Ratio (SCR) Calculations

$$S_{base} = \frac{3}{2} \cdot i_S \cdot v_{PCC} \tag{A5}$$

Hence, the short circuit ratio (SCR) is calculated as:

$$SCR = \frac{SCP}{S_{base}} \tag{A6}$$

The grid impedance model considered in this thesis is dominated by inductance, hence:

$$Z_{grid} = \omega L_S$$

Where, ω is the angular frequency equal to *2*pi*f (f = 50Hz)*.

For table 5.3 in the thesis, the SCR values have been calculated as demonstrated with the help of examples of different values of grid inductance as below:

1) L_S = 2.0mH:

$$Z_{grid} = \omega L_S = 2 * pi * 50 * 2.0 * 10^{-3} = 0.628\ \Omega$$

$$SCP = \frac{\left(100\sqrt{3}\right)^2}{0.628} = 47.77\ kVA$$

$$S_{base} = \frac{3}{2} \cdot (11.2) \cdot \left(100\sqrt{2}\right) \approx 2.4\ kW$$

$$\boldsymbol{SCR = \frac{47.77\ kVA}{2.4\ kW} = 19.9 \rightarrow Strong\ grid}$$

2) L_S = 4.0mH:

$$Z_{grid} = \omega L_{grid} = 2 * pi * 50 * 4.0 * 10^{-3} = 1.257\ \Omega$$

$$SCP = \frac{\left(100\sqrt{3}\right)^2}{1.257} = 23.87\ kVA$$

Appendix A: Short Circuit Ratio (SCR) Calculations

$$S_{base} = \frac{3}{2} \cdot (11.2) \cdot \left(100\sqrt{2}\right) \approx 2.4\ kW$$

$$\boldsymbol{SCR} = \frac{23.87\ kVA}{2.4\ kW} = \mathbf{9.95} \rightarrow \boldsymbol{Reasonably\ Weak\ grid}$$

3) L_S = 8.0mH:

$$Z_{grid} = \omega L_{grid} = 2 * pi * 50 * 8.0 * 10^{-3} = 2.513\ \Omega$$

$$SCP = \frac{\left(100\sqrt{3}\right)^2}{2.513} = 11.94\ kVA$$

$$S_{base} = \frac{3}{2} \cdot (11.2) \cdot \left(100\sqrt{2}\right) \approx 2.4\ kW$$

$$\boldsymbol{SCR} = \frac{11.94\ kVA}{2.4\ kW} = \mathbf{4.98} \rightarrow \boldsymbol{Weak\ grid}$$

4) L_S = 12.0mH:

$$Z_{grid} = \omega L_{grid} = 2 * pi * 50 * 12.0 * 10^{-3} = 3.77\ \Omega$$

$$SCP = \frac{\left(100\sqrt{3}\right)^2}{3.77} = 7.958\ kVA$$

$$S_{base} = \frac{3}{2} \cdot (11.2) \cdot \left(100\sqrt{2}\right) \approx 2.4\ kW$$

$$\boldsymbol{SCR} = \frac{7.958\ kVA}{2.4\ kW} = \mathbf{3.32} \rightarrow \boldsymbol{Very\ weak\ grid}$$

1) L_S = 16.0mH:

$$Z_{grid} = \omega L_{grid} = 2 * pi * 50 * 16.0 * 10^{-3} = 5.027\ \Omega$$

$$SCP = \frac{\left(100\sqrt{3}\right)^2}{5.027} = 5.968\ kVA$$

Appendix A: Short Circuit Ratio (SCR) Calculations

$$S_{base} = \frac{3}{2} \cdot (11.2) \cdot \left(100\sqrt{2}\right) \approx 2.4\ kW$$

$$\boldsymbol{SCR} = \frac{5.968\ kVA}{2.4\ kW}\ = \mathbf{2.49} \rightarrow \boldsymbol{Very\ weak\ grid}$$

Therefore, the above examples show how the SCR values have been calculated based on a weak grid that is dominated by inductance. The proposed inductance estimation methods manage to estimate the weak grid inductance in real time up to the values of SCR equal to 2, after which the estimated value starts showing a steady state error.

The SCR values have been calculated using [27].

Appendix B: Mathematical model of the system

MPC approaches are applicable to SISO (Single Input Single Output) systems and works on the information of the present and past sampling instants to make predictions at the future sampling instants. Therefore, it becomes necessary to have discrete-time system model that makes it easy to include the different sampling instants. Using the Forward Euler Discretization method (First Order mostly), the continuous-time state-space representation of Time-Invariant system model can be transformed into a Discrete model [5]. Equations (B1) and (B2) explain the state space model of a system:

$$\frac{d}{dt}\boldsymbol{x}(\boldsymbol{t}) = Ax(t) + Bu(t) \qquad (B1)$$

$$y(t) = Cx(t) \qquad (B2)$$

Where, *A*, *B* and *C* are the system matrices. The terms *x*, *u* and *y* are such that,

x = State Vector

u = Input Vector

y = Output Vector

The left side of (B2) can be explained using first order Forward Euler Discretization method, such that [74], [76],

$$\frac{d}{dt}\boldsymbol{x}(\boldsymbol{t}) = \frac{x(k+1) - x(k)}{\Delta t} \qquad (B3)$$

Where,

x(k+1)= Future instant

x(k) = Present instant where measurements are made

Appendix B: Mathematical model of the system

Δt = *Sample time (Time different between two consecutive sampling instants)*

Therefore, substituting (B3) in (B2):

$$x(k+1) - x(k) = \Delta t \cdot [A \cdot x(k) + B \cdot u(k)] \quad (B4)$$

$$y(k) = C \cdot x(k) \quad (B5)$$

Taking *x(k)* to the right hand side in (B4),

$$x(k+1) = x(k) \cdot (A \cdot \Delta t + 1) + (B \cdot \Delta t) \cdot u(k) \quad (B6)$$

$$y(k) = C \cdot x(k) \quad (B7)$$

For simplicity of the state-space models in (B6) and (B7) we can say that

$$A \cdot \Delta t + 1 = A_D$$

$$B \cdot \Delta t = B_D$$

$$C = C_D$$

Hence, the State-Space model in Discrete-time domain (used for MPC) derived from a Continuous-time domain is represented as

$$x(k+1) = A_D \cdot x(k) + B_D \cdot u(k) \quad (B8)$$

$$y(k) = C_D \cdot x(k) \quad (B9)$$

Equations (B8) and (B9) represent the case for One-Step Ahead predictions in MPC. Since one of the issues related to MPC control is that the computation effort is high during large

calculations for the system model. In order to compensate for the computational delays, two-steps-ahead predictions are usually carried out, such that instead of using predictions at *k+1* for optimization of the cost functions, predictions at *k+2* are used. This modifies (B8) and (B9) to

$$x(k+2) = A_D \cdot x(k+1) + B_D \cdot u(k+1) \quad (B10)$$

$$y(k+1) = C_D \cdot x(k+1) \quad (B11)$$

Appendix C: Clarke's Transformation

Since a large number of calculations are involved in this control approach, therefore, the computational effort can be very high for the MPC. For simplicity of the control algorithm, the three phase representation of the grid-connected converter is transformed to its respective *α-β* components using the Clarke's transformation [114]. The Clarke's transformation states that for a three phase signal X_a, X_b, and X_c, the equivalent *α-β* representation is such that

$$X_\alpha = \frac{2}{3} * \left(X_a - \frac{1}{2} * (X_b + X_c) \right) \quad (C1)$$

$$X_\beta = \frac{\sqrt{3}}{2} * (X_b - X_c) \quad (C2)$$

The equivalent transformation of the three phase voltage vectors to their respective *α-β* vectors is presented in figure 4.4 where instead of being 120° apart, the voltages are 90° apart and move in the stationary axis with an angular speed of ωt.

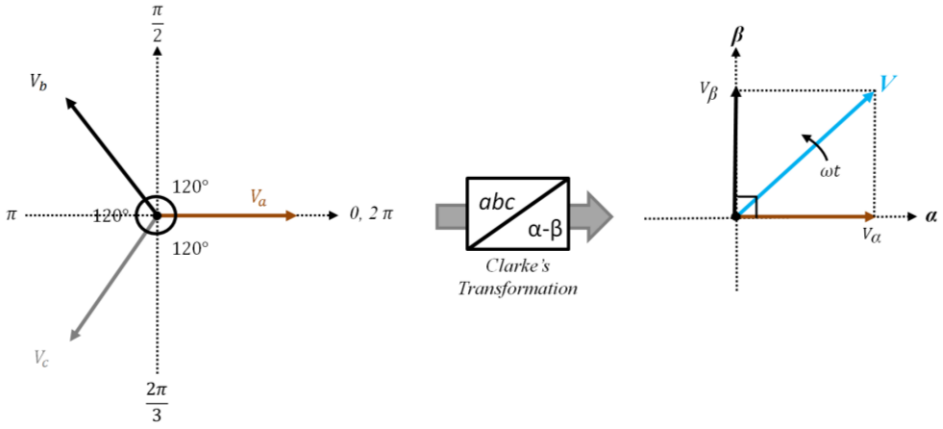

Figure C1: Three phase to α-β voltage transformation

Appendix D: Dead-Time block in MATLAB/SIMULINK

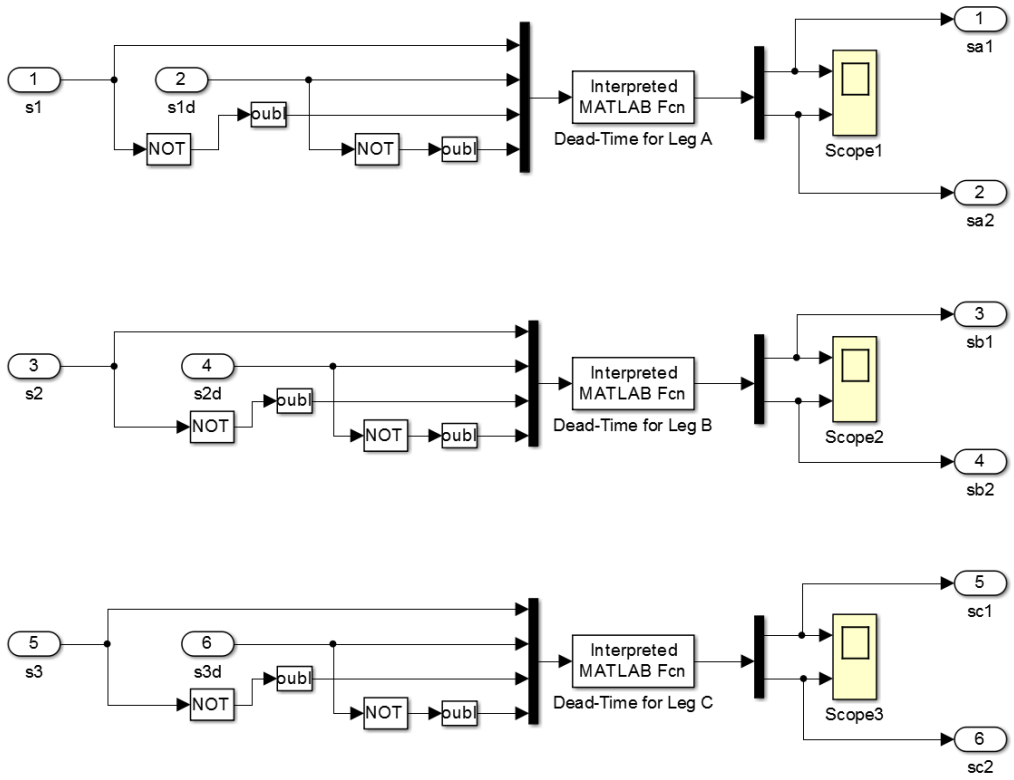

Figure D1: Dead-Time Generation block in Matlab/SIMULINK

Appendix D.1: Dead-Time generation code

The following code for dead-time generation is written in "m.file" with respect to figure 4.10 and figure 4.11 in chapter 4.

```
function out = dead_time1(u)


s1 = u(1);    % top switch - leg A
s1d = u(2);   % top switch delayed - leg A
s1n = u(3);   % bottom switch - leg A
s1nd = u(4); % bottom switch delayed - leg A
```

Appendix D: Dead-Time block in MATLAB/SIMULINK

```
 if (s1 == 0 && s1d == 0),
    s1x = 0;
end
if (s1 == 1 && s1d == 0),
    s1x = 0;
end
if (s1 == 1 && s1d == 1),
    s1x = 1;
end
if (s1 == 0 && s1d == 1),
    s1x = 0;
end
 if (s1n == 1 && s1nd == 1),
    s1nx = 1;
end
if (s1n == 0 && s1nd == 1),
    s1nx = 0;
end
if (s1n == 0 && s1nd == 0),
    s1nx = 0;
end
if (s1n == 1 && s1nd == 0),
    s1nx = 0;
end


out = [s1x, s1nx]; % Output switching signals for upper and lower
                     switches in each leg with dead-time.
```

Appendix E: Experimental results from oscilloscope for MP-DPC with estimation methods

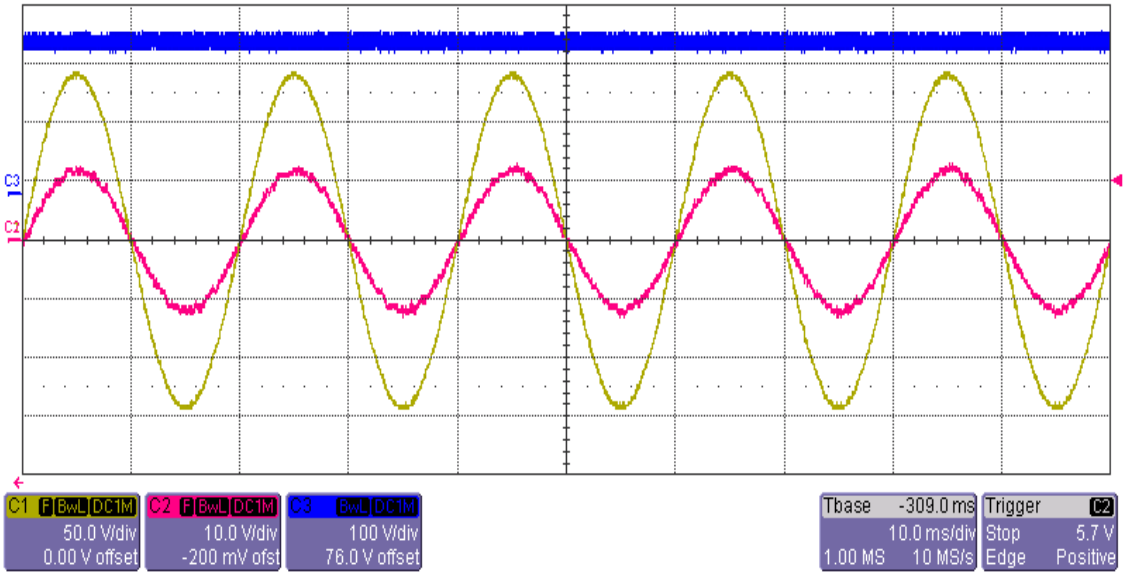

Figure E1: Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage (blue) using PVS using method 1

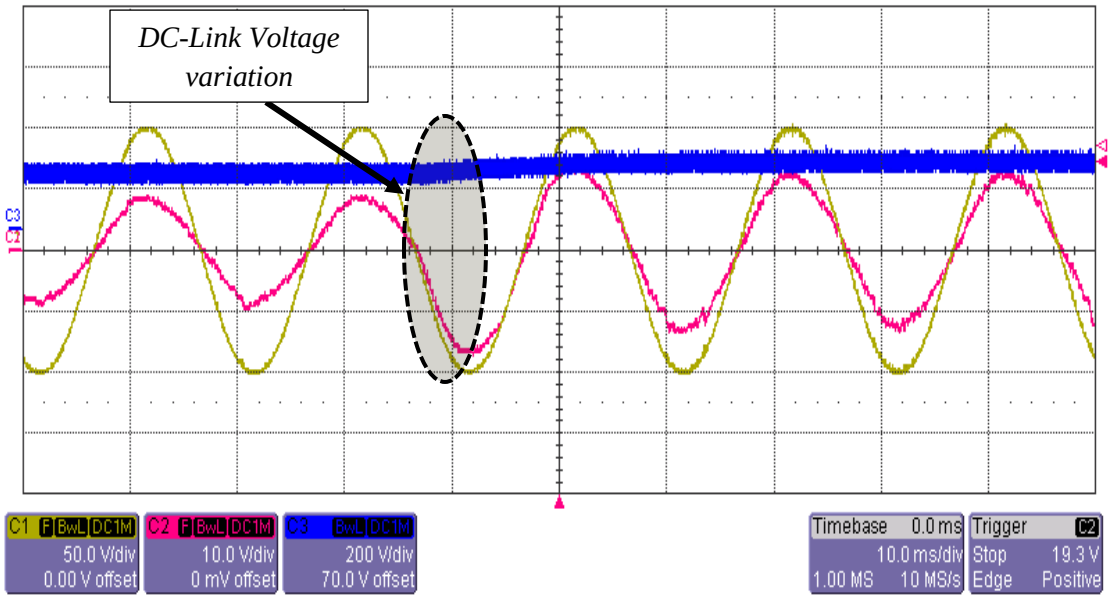

Figure E2: Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage with a step (blue) using PVS using method 1

Appendix E: Experimental results from oscilloscope for MP-DPC with estimation methods

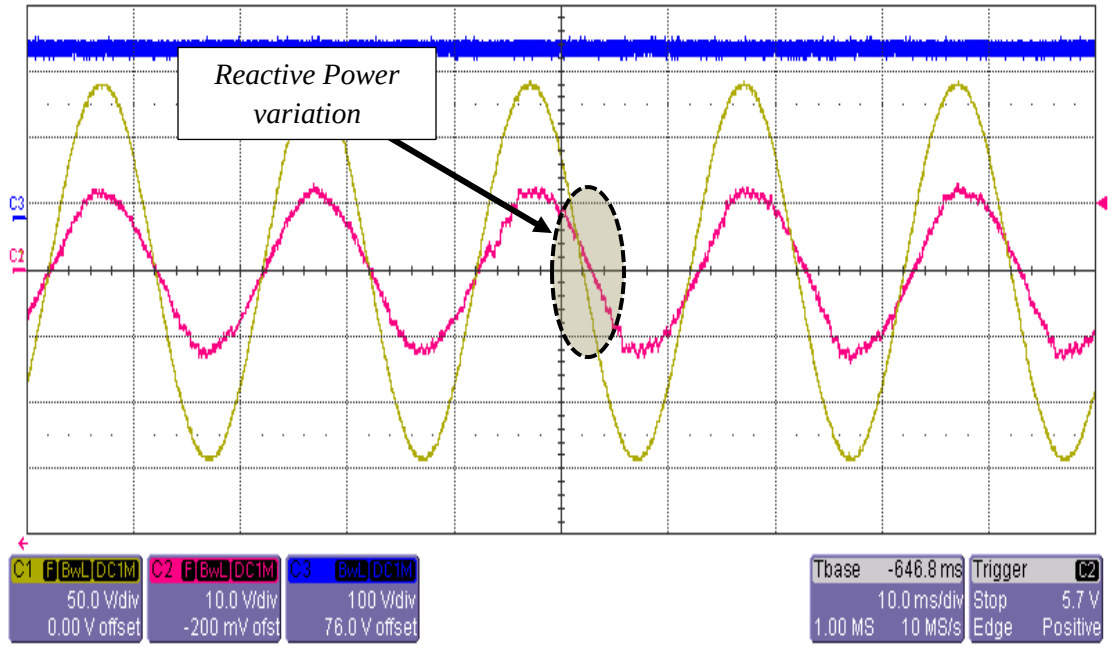

Figure E3: Oscilloscope results for supply voltage (yellow), supply current (pink) and dc-link voltage (blue) with a variation in reactive power reference using PVS using method 1

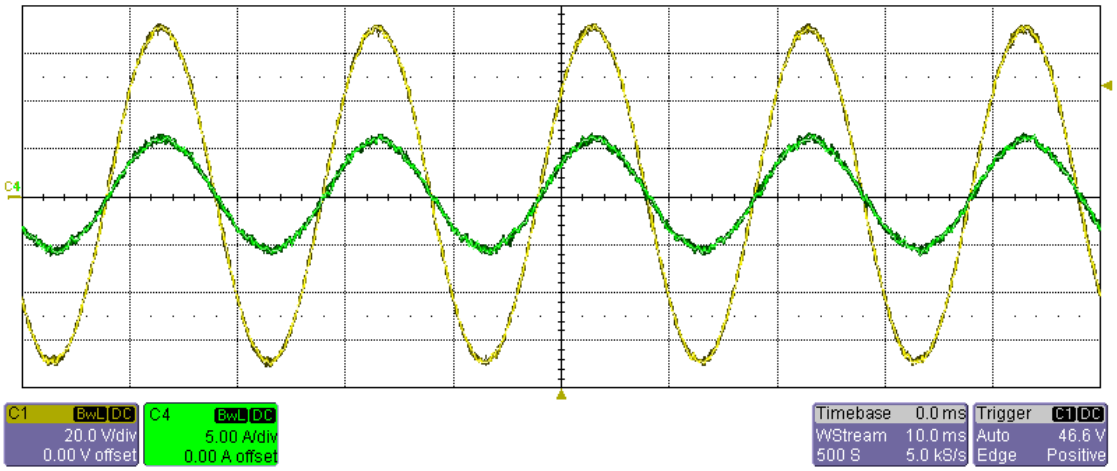

Figure E4: Oscilloscope results for supply voltage (yellow) and supply current (pink) using PVS using method 2

Appendix E: Experimental results from oscilloscope for MP-DPC with estimation methods

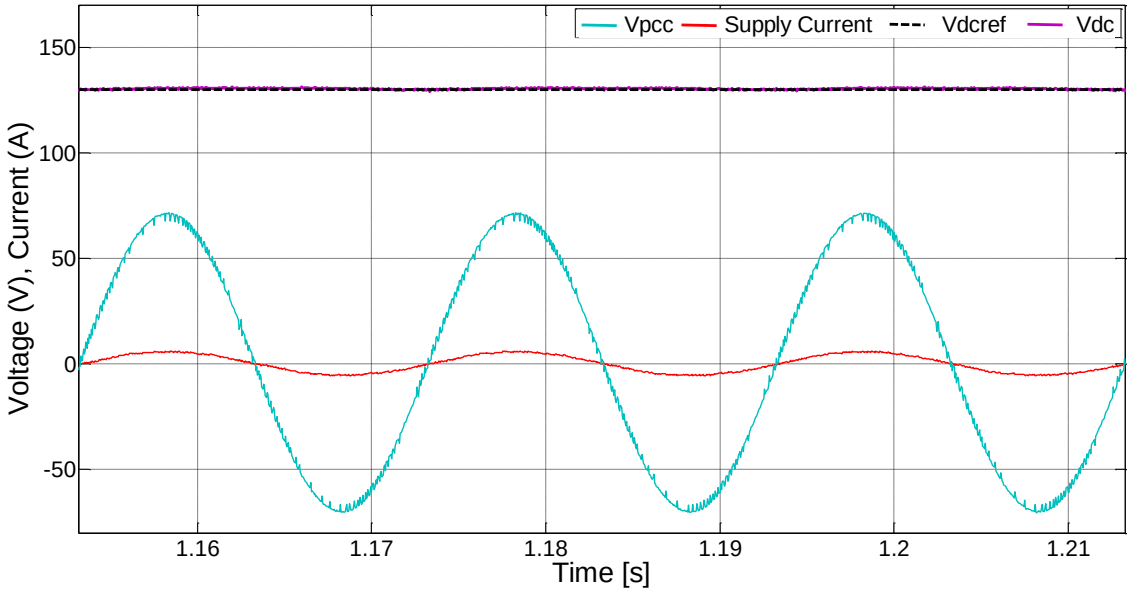

Figure E5: Experimental results for supply voltage, supply current and dc-link voltage using PVS using method 2