Predictive Control of a Direct Series Resonant Converter with Active Output Voltage Compensation

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Abstract

Modern high power supplies are based on resonant converters in order to use high frequency reactive elements (for reduced size) without sacrificing converter efficiency. In an effort to achieve compact high power supplies, direct power converter topologies have been considered, since these are mainly characterised by their high power density. A direct resonant converter topology combines matrix converters with conventional resonant converters.

This work focused on achieving high quality input/output power and high efficiency. Thus, this thesis presents the research on the control of a direct series resonant converter. Since the resonant converter allows a sinusoidal high frequency output current to be generated, zero current switching (ZCS) was considered to reduce the power losses. Hence, since the converter is switched at every zero crossing of the output current (fixed period), model predictive control was considered.

Different predictive approaches for controlling the input and output currents were developed and analysed, however, owing to the characteristics of the topology, these strategies resulted in a suboptimal control. Therefore, in order to improve the input and output qualities (reduce distortion), an output voltage compensation strategy was proposed. This compensation approach is based on adding an H-bridge converter in series between the matrix converter and the resonant tank. This converter improves the voltage applied to the resonant tank, thus, reducing the distortion at the output and, as a consequence, also the distortion at the input. The H-bridge converter utilises only a small capacitor on the dc side in comparison with conventional resonant converters and operates at a low voltage.

Simulations were carried out using MATLAB/Simulink and an experimental prototype was built to validate the strategies proposed, achieving a reduction of the input current THD from 4.4% to 2.7%, a reduction of the output current distortion of approximately 40% and an analytically derived efficiency of 89.5%.

Acknowledgements

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Introduction

1.1 Introduction

Several applications in different sectors such as industrial and scientific research require high-voltage high-power supplies. Among these, the use of high power radio frequency for mineral extraction, industrial heating and particle accelerators are examples. Traditional power supplies are based on line frequency (50/60Hz) topologies which utilise large reactive components and can present a low quality power [1-4]. In order to optimise size, efficiency and power quality, modern power supplies are based on different topologies of resonant power converters. Resonant converters are used to operate at high frequency, which allows reducing the size of the reactive elements and, as a result, compact power supplies can be developed. In addition, owing to the high frequency operation, soft-switching techniques are employed for minimising the switching power loss, thus, leading to a high efficiency [5-7].

In industrial high power radio frequency (RF) applications, high voltage power supplies are used to drive microwave devices such as magnetrons, klystrons and travelling wave tubes. These power supplies are known as modulators and can be divided into two types, namely pulse modulators and continuous wave (CW) modulators. A pulse modulator can produce a high power pulse, some examples of long-pulse modulator based on resonant dc-dc converters are presented in [1, 2].

Unlike pulse modulators, a CW modulator continuously supplies power to the microwave device. In [3], a CW modulator for use in high energy physics applications

was considered. This power supply is based on a direct resonant converter in an effort to achieve a high power density CW modulator. Different control strategies for this power supply were developed in [4]. This power supply utilises a three-phase to single-phase direct (matrix) converter feeding a series resonant parallel loaded circuit connected, via a high frequency transformer, to a high voltage inductively smoothed rectifier.

In this thesis, a research on the control of a new power supply based on a direct power converter is presented. This power supply, a CW modulator, is based on a series resonant circuit driving an industrial magnetron. The direct power converter, loaded with a series resonant tank, is denominated a direct series resonant converter. Since this research focuses on the control of a direct series resonant converter, for simplicity, an equivalent resistive load is considered to replace the dc output stage, i.e. transformer, rectifier, output filter and load.

In order to reduce power losses, a direct resonant converter is switched using soft-switching techniques, particularly, zero current switching (ZCS). To achieve ZCS operation, the converter is only switched at every zero crossing of the high frequency output current, hence, in this work, Model Predictive Control (MPC) is considered to control the direct series resonant converter since this control technique optimises the selection of the converter switching state.

Unlike [3, 4], where a series resonant parallel loaded (SRPL) tank is utilised, in this work, a series tank is considered for a magnetron, as it is more suitable to control the current supplied to the device. A series resonant circuit presents some advantages when compared with a SRPL circuit, namely:

- Since the output current depends on the load, the power losses are variable and are reduced for a low load current.
- The dc output stage of a series resonant converter is composed of a capacitively smoothed rectifier, thus, only a capacitor is needed, unlike a SRPL circuit, where an inductor and a capacitor are necessary.

1.2 Project objectives

The aim of this project was to study the control of a direct series resonant converter with focus on the power quality. Thus, this project considered the following objectives:

- Develop control strategies in order to have input current with low harmonic content and low distortion at the output.
- Study and analyse improvements to the converter topology.
- Verify the performance of the system through simulations.
- Experimental validation of the strategies and/or improvements.

1.3 Thesis plan

Chapter two presents an overview of resonant power converters. This chapter focuses on dc-dc resonant converters which are used to create high voltage power supplies. The structure and control of these converters are discussed in this chapter.

Chapter three provides an overview of model predictive control of power converters. This chapter introduces the predictive control with finite control set, which is a control strategy based on the model of a power electronics system. The basic components of a predictive algorithm are described, such as the cost function, weighting factors and prediction equations. As the main part of a predictive control with finite control set algorithm, the switching model of a power converter is also described. Finally, a compensation approach for the delay associated to the digital implementation is presented.

Chapter four describes the structure and main characteristics of a direct resonant converter. Two direct resonant topologies are considered in this chapter, the direct parallel resonant converter (DPRC) which was used in previous work, and the direct series resonant converter (DSRC) which is the topology utilised in this research. Both topologies are analysed considering zero current switching operation.

Chapter five presents new predictive control strategies for a direct series resonant converter. Three predictive approaches are described, namely input current predictive control, output current predictive control and input-output predictive control.

Chapter six presents a new voltage compensation strategy for a direct series resonant converter in order to overcome the issues related to input-output control. This compensation approach is based on the inclusion of an H-bridge converter connected in series between the direct converter and the resonant tank. The voltage provided by the H-bridge improves the voltage applied to the resonant tank and is controlled by expanding the input-output predictive control algorithm.

Chapter seven describes the entire experimental system, including power converters, control platform, resonant tank and the DSP control program.

Chapter eight presents the experimental results obtained during the experimental validation of the proposed control and compensation strategies.

Finally, chapter nine gives the conclusions for this work.

Chapter 2

Overview of Resonant Power Converters

2.1 Introduction

The operation of conventional pulse-width modulated (PWM) power converters presents several drawbacks such as switching power losses associated with hard switching, and electromagnetic interference (EMI) problems [5-7]. These shortcomings become more significant when high frequency operation is being considered in an effort to increase the power density (size reduction); hence, different converter topologies have been developed to overcome these issues. One approach is the use of resonant converters, which are based on an LC circuit (resonant tank) which produces a high frequency oscillatory voltage and/or current, allowing the semiconductor devices to switch with zero voltage (zero voltage switching, ZVS) and/or zero current (zero current switching, ZCS), thus, reducing the switching power losses and stress [5-7]. ZVS and ZCS are called soft-switching techniques.

There are different types of resonant converters: load resonant converters, quasi-resonant converters, multi-resonant converters, resonant dc-link inverter, amongst others [5-7]. Quasi- and multi-resonant converters, also called resonant-switch converters [7], are basically PWM power converters employing auxiliary resonant circuits, which include parasitic elements, with the power switches (called resonant switches) in order to achieve soft-switching operation [5-7]. Figure 2.1 and 2.2 show ZVS and ZCS resonant switches, and resonant topologies for a buck converter, respectively.

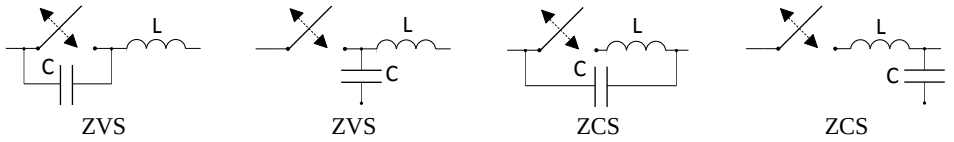


Fig. 2.1 Resonant switches: ZVS and ZCS configurations.

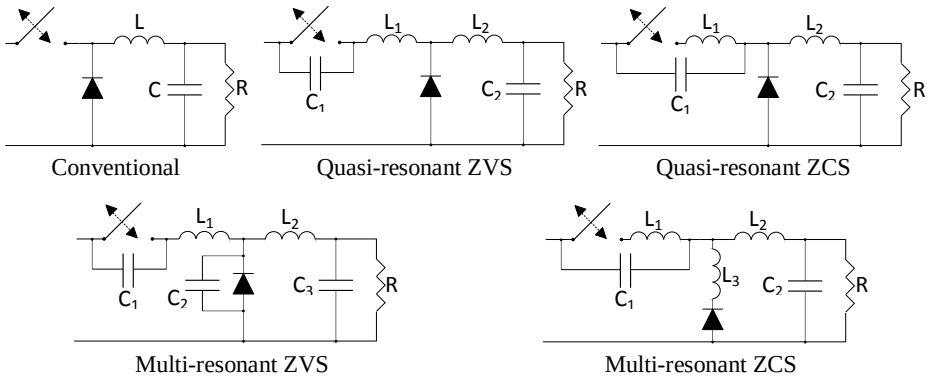


Fig. 2.2 Buck converter topologies.

A resonant dc-link inverter, as that shown in figure 2.3, is an inverter that utilises a resonant circuit at the input to produce a pulsating voltage, instead of a constant dc voltage, to allow soft commutation of the inverter switching devices [5, 7].

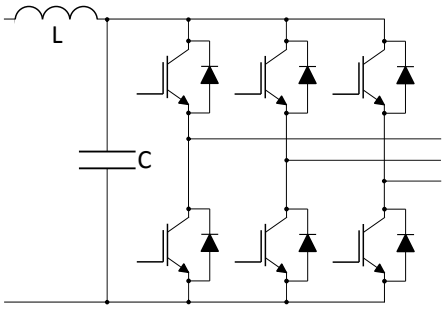


Fig. 2.3 Resonant dc-link inverter.

Load resonant dc-dc converters are composed of a resonant inverter and a high frequency rectifier [5-7]. Essentially, a resonant inverter consists of a high frequency inverter feeding a resonant tank. High frequency sinusoidal waveforms and soft-switching operation can be achieved via suitable design and control. A high frequency rectifier is connected to the resonant tank to obtain the dc output. In figure 2.4, a diagram of a load resonant converter is depicted. A high frequency transformer is employed, as shown in figure 2.4, if isolation and/or voltage/current scaling is required [5-7].

There are several types of load resonant converters, usually characterised by the configuration of the resonant circuit, such as series, parallel, series-parallel and current source parallel resonant converters [5-7]. Among the series-parallel

topologies, various configurations can be found, such as LCC and CLL, where L and C refer to the number of inductors and capacitors used in the resonant tank. Figure 2.5 shows several topologies of resonant tanks used in load resonant converters [5-7].

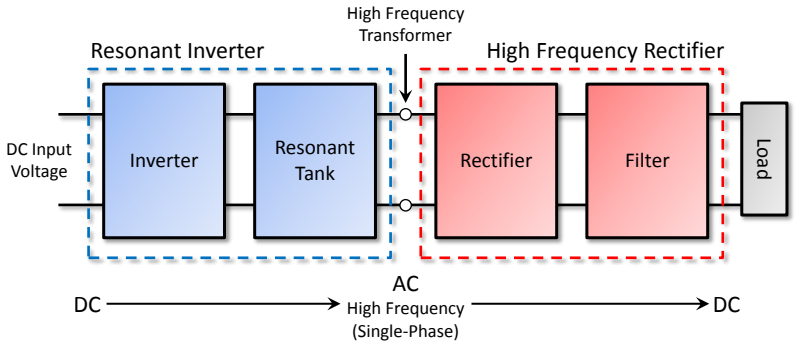


Fig. 2.4 Diagram of a load resonant dc-dc converter.

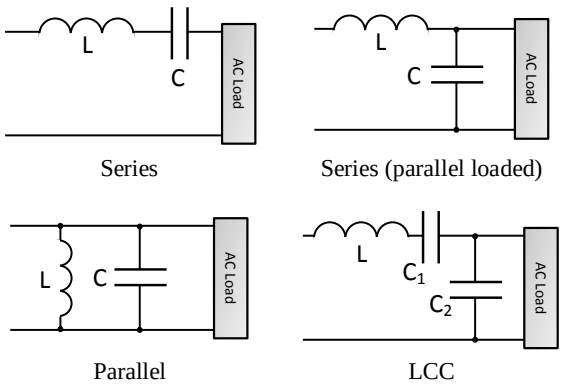


Fig. 2.5 Resonant tank topologies.

High frequency operation without sacrificing converter efficiency makes load resonant converters suitable for compact high power applications [5]. This chapter focuses on the characteristics of these types of resonant converters.

In high power applications, owing to voltage/current levels involved, IGBTs are the typical semiconductor devices utilised in load resonant converters.

2.2 Resonant tank configurations

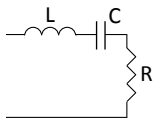
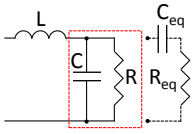
Various configurations of resonant circuits are employed in resonant converters. In order to design and control these converters, several parameters must be considered, such as corner frequency, resonant frequency, characteristic impedance and loaded quality factor, which are defined as follows [6]:

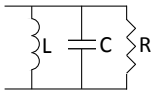
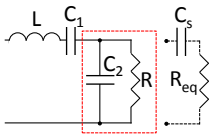
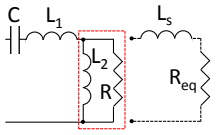
- Corner frequency or undamped natural frequency (f_o). This frequency is defined by the main tank reactive components without considering resistive elements.
- Resonant frequency (f_r). This is defined as the frequency which cancels out the inductive and capacitive impedances, hence, input voltage and current are in phase.
- Characteristic impedance (Z_o). This corresponds to the absolute value of the inductive impedance or of the capacitive impedance calculated at the corner frequency.
- Loaded quality factor (Q). This parameter provides a measure of the energy stored in the resonant tank at the corner frequency compared with the energy dissipated at the corner frequency. Thus, the loaded quality factor is defined by (2.1), where the reactive power corresponds to the inductive reactive power or the capacitive reactive power at the corner frequency, and the active power is the average power dissipated by the load.

$$Q = 2\pi \frac{Peak\ energy\ stored}{Energy\ dissipated\ per\ cycle} = \frac{Reactive\ power}{Active\ power} \tag{2.1}$$

Table 2.1 summarises the expressions of corner frequency (or undamped natural frequency), resonant frequency, characteristic impedance and loaded quality factor for different resonant circuit topologies [6].

Table 2.1 Resonant circuit topologies and their parameters.

Resonant circuit	Corner frequency ω_o	Resonant frequency ω_r	Characteristic impedance Z_o	Loaded quality factor Q
 Series (series loaded)	$\frac{1}{\sqrt{LC}}$	$\frac{1}{\sqrt{LC}}$	$\sqrt{\frac{L}{C}}$	$\frac{Z_o}{R}$
 Series (parallel loaded)	$\frac{1}{\sqrt{LC}}$	$\frac{1}{\sqrt{LC_{eq}}}$	$\sqrt{\frac{L}{C}}$	$\frac{R}{Z_o}$

 Parallel	$\frac{1}{\sqrt{LC}}$	$\frac{1}{\sqrt{LC}}$	$\sqrt{\frac{L}{C}}$	$\frac{R}{Z_o}$
 LCC	$\frac{1}{\sqrt{LC}}$ $\left(C = \frac{C_1 C_2}{C_1 + C_2}\right)$	$\frac{1}{\sqrt{LC_{eq}}}$ $\left(C_{eq} = \frac{C_1 C_s}{C_1 + C_s}\right)$	$\sqrt{\frac{L}{C}}$ $\left(C = \frac{C_1 C_2}{C_1 + C_2}\right)$	$\frac{R}{Z_o}$
 CLL	$\frac{1}{\sqrt{LC}}$ $(L = L_1 + L_2)$	$\frac{1}{\sqrt{L_{eq}C}}$ $\left(L_{eq} = L_1 + L_s\right)$	$\sqrt{\frac{L}{C}}$ $(L = L_1 + L_2)$	$\frac{R}{Z_o}$

Expressions for the total impedance of series and parallel resonant circuit are given in table 2.2. In addition, in order to show the impedance variation considering different operating frequencies and quality factor values, figure 2.6, 2.7 and 2.8 show magnitude (normalised) and angle (phase) of the total impedance as functions of the quotient $\frac{f}{f_o}$ (normalised frequency) and quality factor. In these figures, it can be seen the effect of the quality factor on the resonant circuit behaviour as well as the effect of the operating frequency.

Table 2.2 Total impedance of resonant circuits.

Resonant circuit	Impedance Z(f)	
	Magnitude |Z| (Ω)	Angle φ (rad)
Series (series loaded)	$Z_o\sqrt{\frac{1}{Q^2}+\left[\left(\frac{f}{f_o}\right)-\left(\frac{f_o}{f}\right)\right]^2}$	$tan^{-1}\left\{Q\left[\left(\frac{f}{f_o}\right)-\left(\frac{f_o}{f}\right)\right]\right\}$
Series (parallel loaded)	$Z_o\sqrt{\frac{Q^2\left[1-\left(\frac{f}{f_o}\right)^2\right]^2+\left(\frac{f}{f_o}\right)^2}{1+\left[Q\left(\frac{f}{f_o}\right)\right]^2}}$	$tan^{-1}\left\{Q\left(\frac{f}{f_o}\right)\left[\left(\frac{f}{f_o}\right)^2+\left(\frac{1}{Q^2}\right)-1\right]\right\}$
Parallel	$Z_o\frac{1}{\sqrt{\frac{1}{Q^2}+\left[\left(\frac{f}{f_o}\right)-\left(\frac{f_o}{f}\right)\right]^2}}$	$-tan^{-1}\left\{Q\left[\left(\frac{f}{f_o}\right)-\left(\frac{f_o}{f}\right)\right]\right\}$

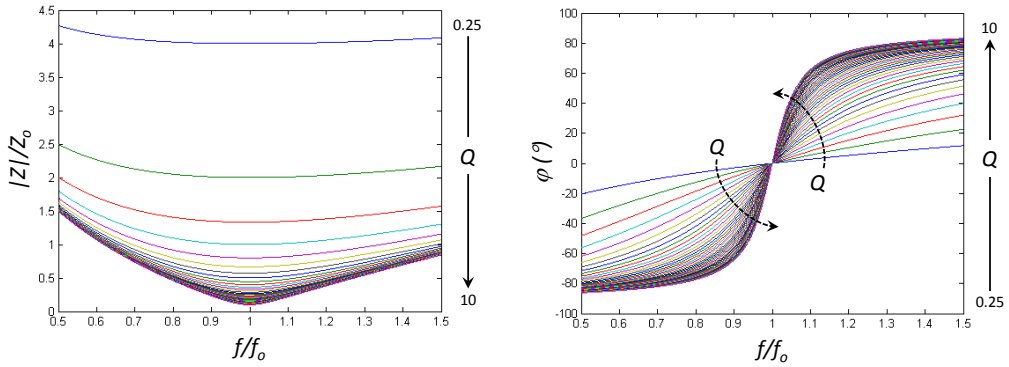


Fig. 2.6 Magnitude and angle of the total impedance of a series resonant circuit.

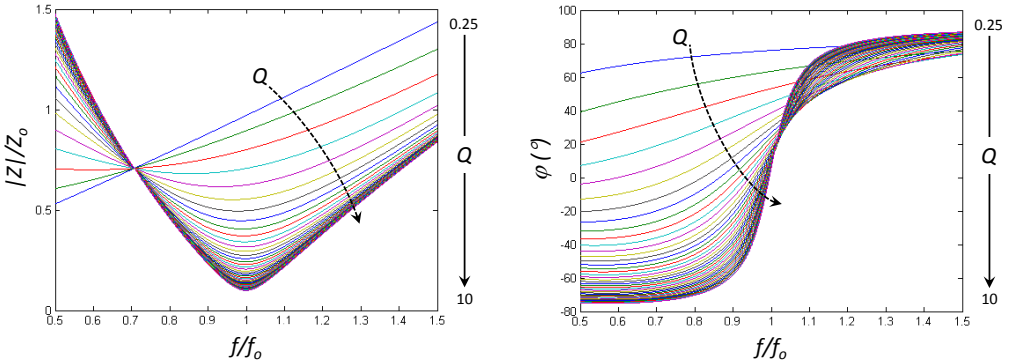


Fig. 2.7 Magnitude and angle of the total impedance of a series (parallel loaded) resonant circuit.

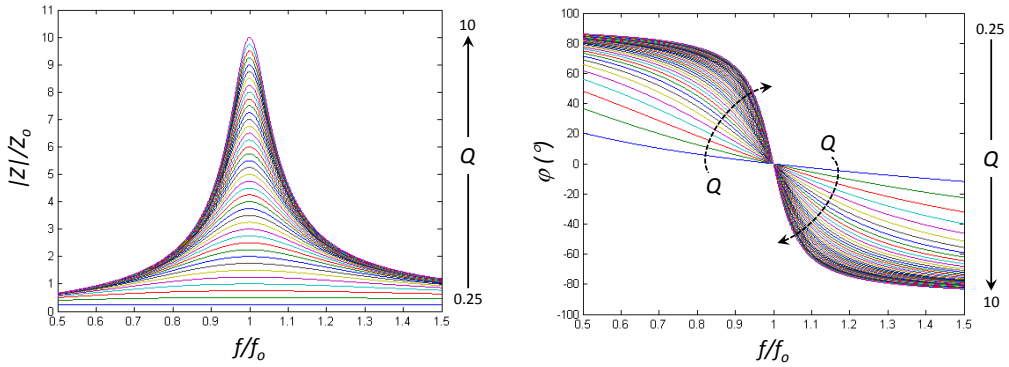


Fig. 2.8 Magnitude and angle of the total impedance of a parallel resonant circuit.

2.3 Load resonant dc-dc converters

This section presents the structure and control techniques for series and parallel resonant converters. The quality factor of the resonant tank is assumed to be high enough such that the currents through the tank components are sinusoidal. Furthermore, an operating frequency about the resonant frequency is also considered.

2.3.1 Series resonant converter

A series resonant converter (SRC) [5, 6], also called series-loaded resonant (SLR) converter [7], consists of a resonant inverter and a capacitively smoothed rectifier as output stage [5-7]. The resonant tank configuration is that depicted in figure 2.5(a). A diagram of this converter is shown in figure 2.9.

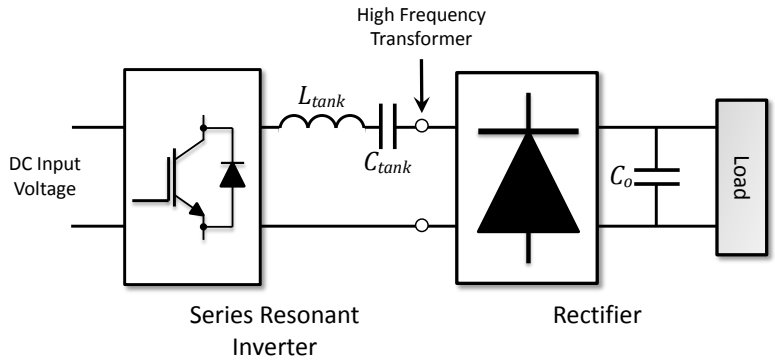


Fig. 2.9 Schematic diagram of the topology of a series resonant converter.

Considering a sinusoidal tank current, a series resonant converter behaves as a current source, thus, as shown in figure 2.10, since the output stage is connected in series with the resonant tank, the rectifier input voltage (v_o) is a square wave voltage whose magnitude depends on the dc output voltage (V_o), which corresponds to the output filter capacitor voltage.

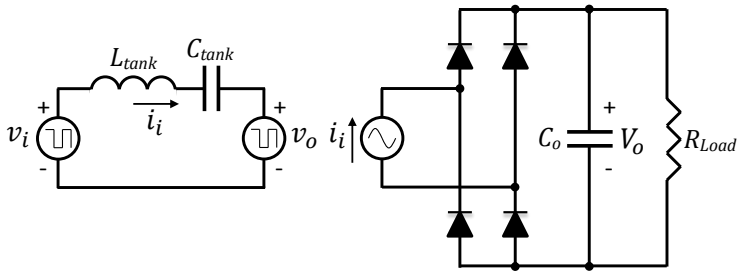


Fig. 2.10 Equivalent circuit of a series resonant converter.

2.3.2 Parallel resonant converter

As in a series resonant converter, a parallel resonant converter (PRC) [5, 6] is composed of a resonant inverter supplying a series resonant (parallel loaded) circuit or SRPL tank [1-2, 8], shown in figure 2.5(b). In this case, the output stage is based on an inductively smoothed rectifier [5-7]. A schematic diagram of a parallel resonant

converter is shown in figure 2.11. This converter is also called parallel-loaded resonant (PLR) converter [7].

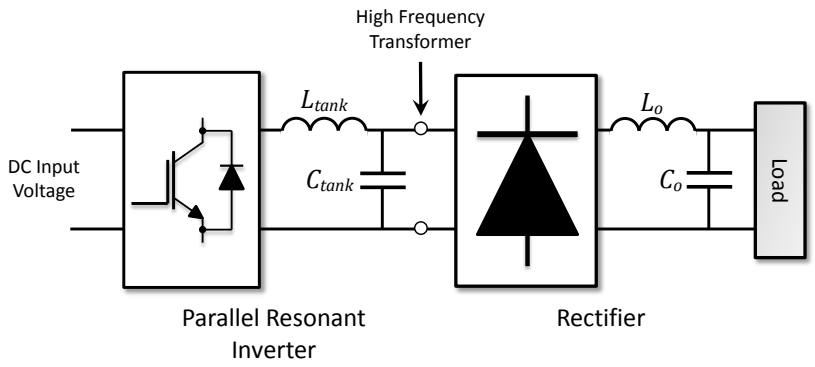


Fig. 2.11 Schematic diagram of the topology of a parallel resonant converter.

Assuming a sinusoidal tank capacitor voltage, unlike series resonant converters, the output stage (load) is in parallel with the resonant tank capacitor, which acts as a voltage source. In this case, as illustrated in figure 2.12, the rectifier input current (i_o) is a square wave current, whose peak magnitude is equal to the current through the output filter inductor (I_o).

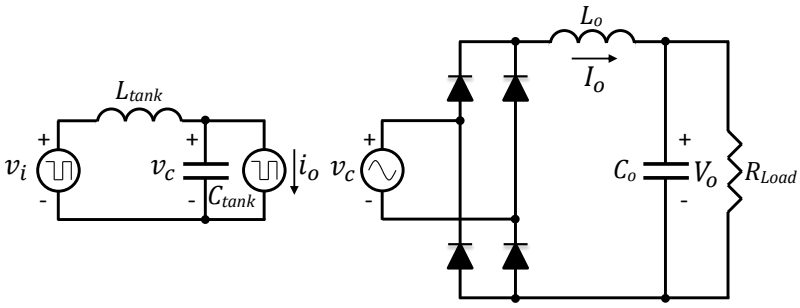


Fig. 2.12 Equivalent circuit of a parallel resonant converter.

2.3.3 Control of load resonant converters

To regulate the output dc voltage (load voltage in figure 2.9 and 2.11), it is necessary to control the current through the resonant tank (series loaded) or the voltage across the tank capacitor (parallel loaded). Therefore, considering the previous assumptions (high Q, etc.) and steady-state operation, an equivalent ac load (R_{AC}) is calculated [1-2, 8-10], as shown in figure 2.13, in order to define the relationship between the voltage applied to the resonant tank (v_{in}) and the load voltage (v_{out}).

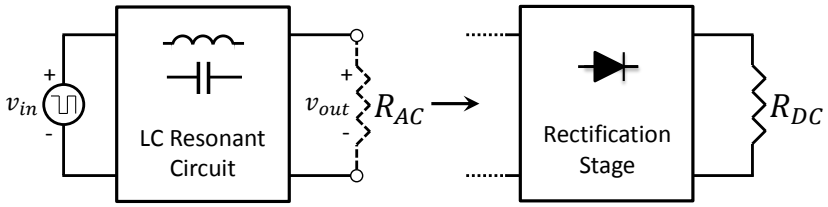


Fig. 2.13 Equivalent ac load.

This equivalent ac load is determined by considering the fundamental component of voltages and currents (fundamental mode approximation, FMA). Table 2.3 gives, for both resonant converters, the relationship between the peak value of the voltage applied to the resonant tank ($\hat{v}_{in}$) and the peak value of the load voltage ($\hat{v}_{out}$) as well as the equivalent ac load. The switching frequency (f_s) corresponds to the frequency of the voltage applied to the resonant tank, i.e. operating frequency. Figure 2.14 shows the input/output voltage relationship as a function of the switching frequency.

Table 2.3 Input/output voltage relationship and equivalent ac load.

	Series Resonant Converter	Parallel Resonant Converter
$\frac{\hat{v}_{out}}{\hat{v}_{in}}$	$\frac{1}{\sqrt{1+Q^2\left[\left(\frac{f_s}{f_o}\right)-\left(\frac{f_o}{f_s}\right)\right]^2}}$	$\frac{1}{\sqrt{\left[1-\left(\frac{f_s}{f_o}\right)^2\right]^2+\left[\left(\frac{1}{Q}\right)\left(\frac{f_s}{f_o}\right)\right]^2}}$
R_{AC}	$\frac{8}{\pi^2}R_{DC}$	$\frac{\pi^2}{8}R_{DC}$

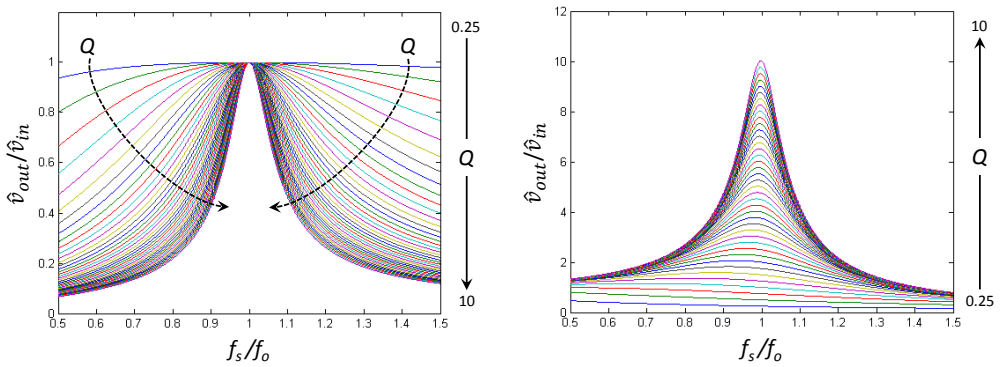


Fig. 2.14 Input/output voltage relationship: (a) series and (b) parallel converter.

The voltage applied to the resonant tank by the inverter is a square wave voltage or a quasi-square wave voltage [1-2, 8-12]. The fundamental component is determined by

means of the Fourier series of the quasi-square wave signal illustrated in figure 2.15. This series is given by:

$$f(\theta) = \sum_{n=1}^{\infty} \left\{ \frac{2A}{n\pi} [1 - \cos(n\pi)] \cos(n\alpha) \right\} \sin(n\theta) \tag{2.2}$$

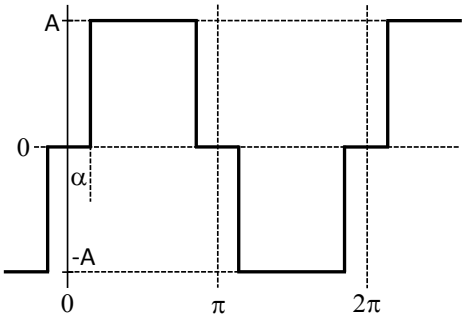


Fig. 2.15 Quasi-square wave signal.

From (2.2), the peak value of the fundamental component of a full square wave signal, i.e. α=0, is:

$$\hat{f}_1 = \frac{4A}{\pi} \tag{2.3}$$

Considering the input/output voltage relationship (table 2.3) and a square/quasi-square wave input voltage, three control strategies for load resonant converters may be considered [1-2, 8-12]:

- Frequency control.
- Phase control.
- Combined frequency and phase control.

2.3.3.1 Frequency control

Since the behaviour of a resonant tank depends on the operating frequency, the inverter may be controlled by varying the switching frequency (f_s) [2-10]. In this case, the voltage applied to the resonant tank, which depends on the dc input voltage (V_{DC}), is a square wave voltage whose fundamental component, from (2.3), is:

$$\hat{v}_{in} = \frac{4V_{DC}}{\pi} \tag{2.4}$$

The modulation index can be determined by using the input/output voltage relationship given in table 2.3. Thus, considering that the maximum value of the

input/output voltage relationship is $\frac{\hat{v}_{out}}{\hat{v}_{in}} = 1$, for a series converter, and $\frac{\hat{v}_{out}}{\hat{v}_{in}} \approx Q$, for a parallel converter, the modulation index for each converter is given by:

$$M_{FC(series)}\left(\frac{f_s}{f_o}\right) = \frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{1}{\sqrt{1 + Q^2\left[\left(\frac{f_s}{f_o}\right) - \left(\frac{f_o}{f_s}\right)\right]^2}} \tag{2.5}$$

$$M_{FC(parallel)}\left(\frac{f_s}{f_o}\right) = \frac{1}{Q}\frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{1}{\sqrt{Q^2\left[1 - \left(\frac{f_s}{f_o}\right)^2\right]^2 + \left(\frac{f_s}{f_o}\right)^2}} \tag{2.6}$$

Figure 2.16 shows the modulation index for different levels of quality factor. The switching of the inverter for frequency control is depicted in figure 2.17, which shows the voltage applied to the resonant tank and its fundamental component.

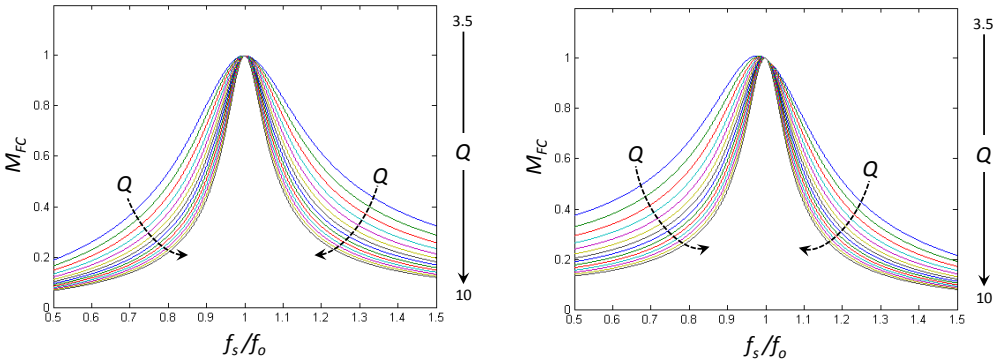


Fig. 2.16 Modulation index for frequency control: (a) series and (b) parallel converter.

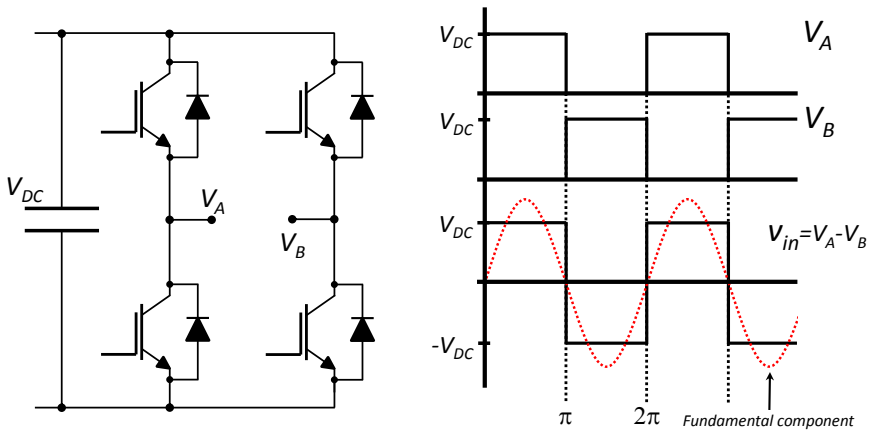


Fig. 2.17 Voltage applied to the resonant tank by employing frequency control.

Waveforms for a series and a parallel resonant converter regulated by frequency control are illustrated in figure 2.18. In both cases, the power converter is operating at

the corner frequency, which is approximately equal to the resonant frequency for a high value of quality factor.

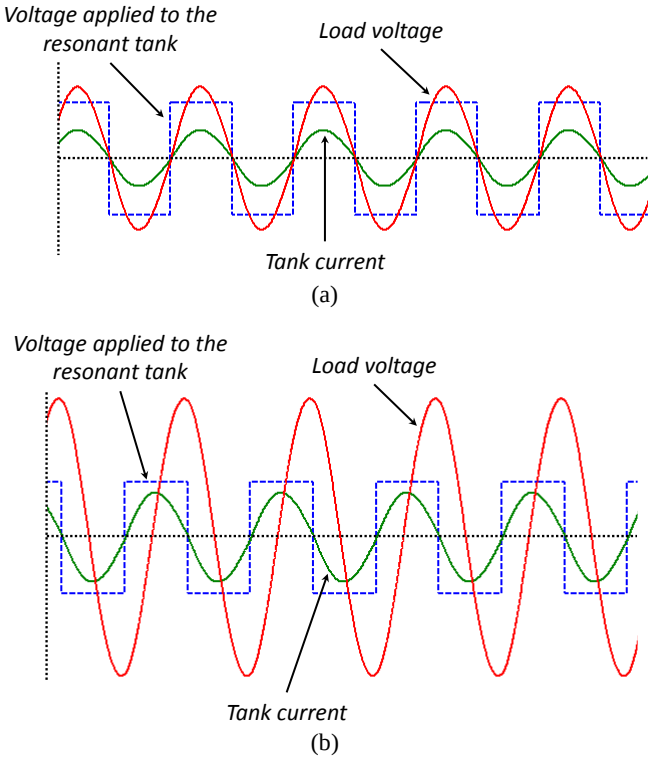


Fig. 2.18 Waveforms using frequency control: (a) series and (b) parallel converter.

Since the angle between tank input voltage and tank input current depends on the operating frequency, this control technique achieves full soft-switching operation (ZCS) when the switching frequency corresponds to the resonant frequency.

2.3.3.2 Phase control

If the switching frequency is maintained fixed (generally operating at the corner frequency), the output voltage may be controlled by modifying the angle α in equation (2.2), thus, a quasi-square wave voltage is applied to the resonant tank [1-2,8-12]. Hence, the fundamental value of the input voltage and the input/output voltage relationship are given by (2.7) and table 2.4, respectively.

$$\hat{v}_{in} = \frac{4V_{DC}}{\pi}\cos(\alpha) \tag{2.7}$$

Considering ϕ as the phase shift between the switching of each inverter leg (where $\alpha = \frac{\phi}{2}$), as shown in figure 2.19, the modulation index for both resonant

converters can be determined by (2.8). Waveforms for phase control of both converters are shown in figure 2.20.

$$M_{PC(series)}(\phi) = M_{PC(parallel)}(\phi) = cos\left(\frac{\phi}{2}\right) \quad (2.8)$$

Table 2.4 Input/output voltage relationship.

	Series Resonant Converter	Parallel Resonant Converter
$\frac{\hat{v}_{out}}{\hat{v}_{in}}$	$\cos(\alpha)$	Q $\cos(\alpha)$

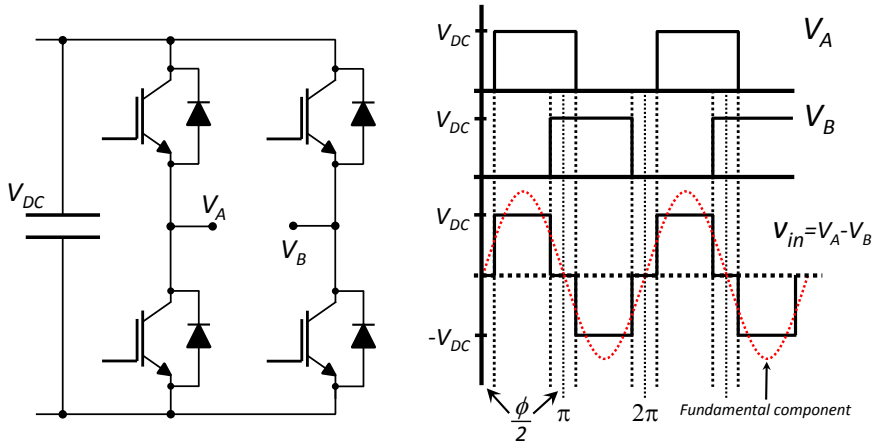


Fig. 2.19 Voltage applied to the resonant tank by using phase control.

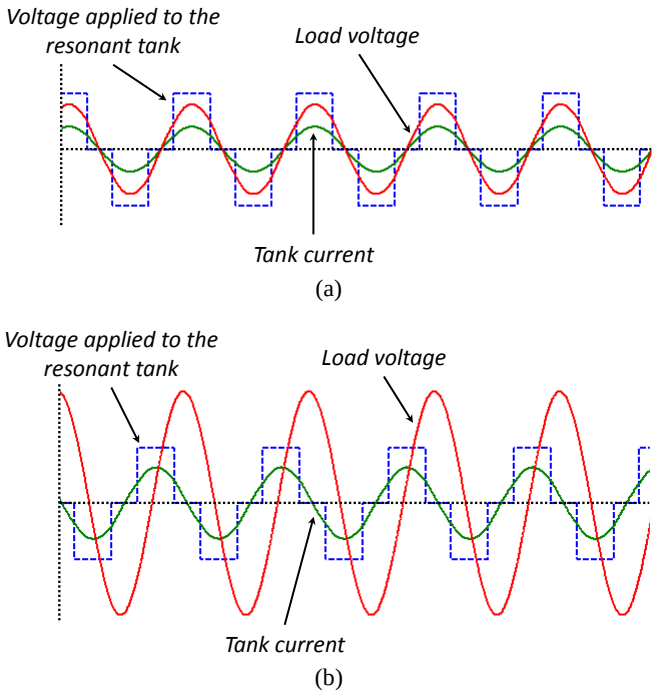


Fig. 2.20 Waveforms using phase control: (a) series and (b) parallel converter.

Although this control strategy allows the output voltage to be regulated without varying the switching frequency, full soft-switching operation may be lost even when operating at the resonant frequency.

2.3.3.3 Frequency-Phase control

In order to regulate the output voltage under soft-switching operation (ZCS and ZVS), reducing losses, frequency and phase control can be combined [1-2, 8-12]. In addition, this control strategy allows the control of the output voltage to be more flexible in terms of operating range (quality factor and frequency). Thus, the phase shift between input voltage and tank current (φ) is considered as:

$$\varphi = \frac{\phi}{2} \tag{2.9}$$

As a result, from (2.8) and table 2.2, the modulation index for each converter considering phase control is:

$$M_{PC(series)}\left(\frac{f_s}{f_o}\right) = cos\left(tan^{-1}\left\{Q\left[\left(\frac{f_s}{f_o}\right)-\left(\frac{f_o}{f_s}\right)\right]\right\}\right) \tag{2.10}$$

$$M_{PC(parallel)}\left(\frac{f_s}{f_o}\right) = cos\left(tan^{-1}\left\{Q\left(\frac{f_s}{f_o}\right)\left[\left(\frac{f_s}{f_o}\right)^2+\left(\frac{1}{Q^2}\right)-1\right]\right\}\right) \tag{2.11}$$

Therefore, from (2.5)-(2.6) and (2.10)-(2.11), the modulation index for both converters using frequency-phase control is given by:

$$M_{FPC(series)} = M_{FC(series)} \times M_{PC(series)} \tag{2.12}$$

$$M_{FPC(parallel)} = M_{FC(parallel)} \times M_{PC(parallel)} \tag{2.13}$$

Hence, the final expressions for (2.12) and (2.13) are:

$$M_{FPC(series)}\left(\frac{f_s}{f_o}\right) = \frac{\left(\frac{f_s}{f_o}\right)^2}{\left[Q^2\left(\frac{f_s}{f_o}\right)^4 + \left(\frac{f_s}{f_o}\right)^2 + Q^2 - 2Q^2\left(\frac{f_s}{f_o}\right)^2\right]} \tag{2.14}$$

$$M_{FPC(parallel)}\left(\frac{f_s}{f_o}\right) = \frac{Q}{\left[Q^2\left(\frac{f_s}{f_o}\right)^4 + \left(\frac{f_s}{f_o}\right)^2 + Q^2 - 2Q^2\left(\frac{f_s}{f_o}\right)^2\right]\sqrt{Q^2\left(\frac{f_s}{f_o}\right)^2 + 1}} \tag{2.15}$$

The modulation index, for series and parallel converters, utilising frequency-phase control as function of $\frac{f_s}{f_o}$ is shown in figure 2.21. In addition, the switching of the inverter and typical waveforms for this strategy can be seen in figures 2.22 and 2.23, respectively.

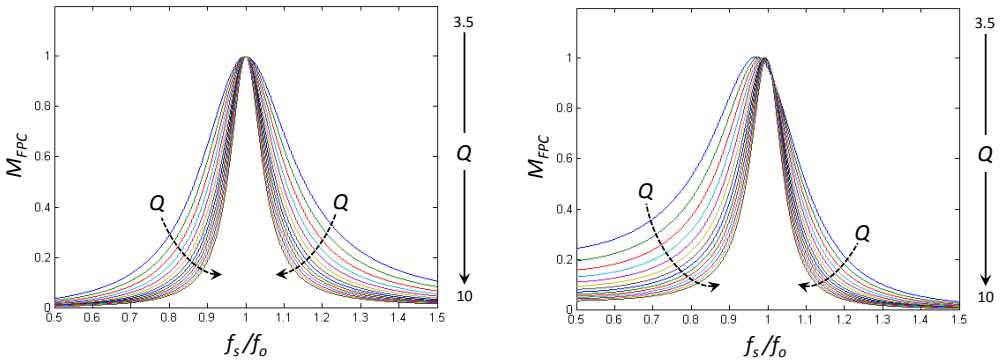


Fig. 2.21 Modulation index for frequency-phase control: (a) series and (b) parallel converter.

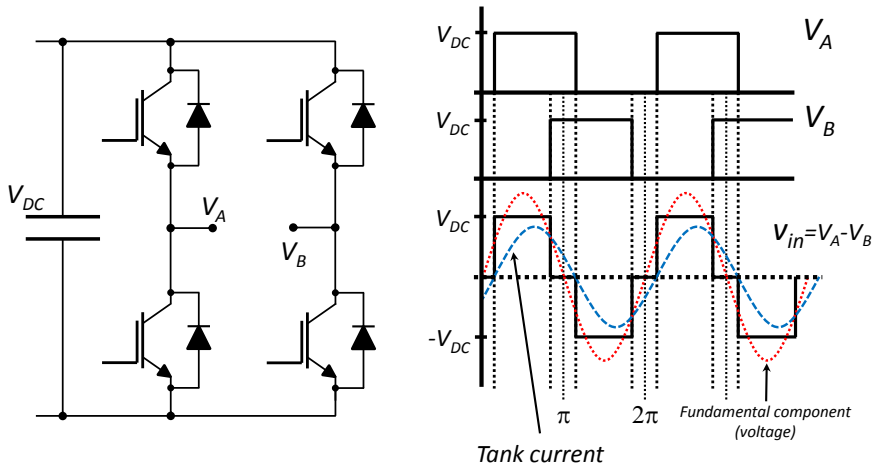


Fig. 2.22 Voltage applied to the resonant tank by using frequency-phase control.

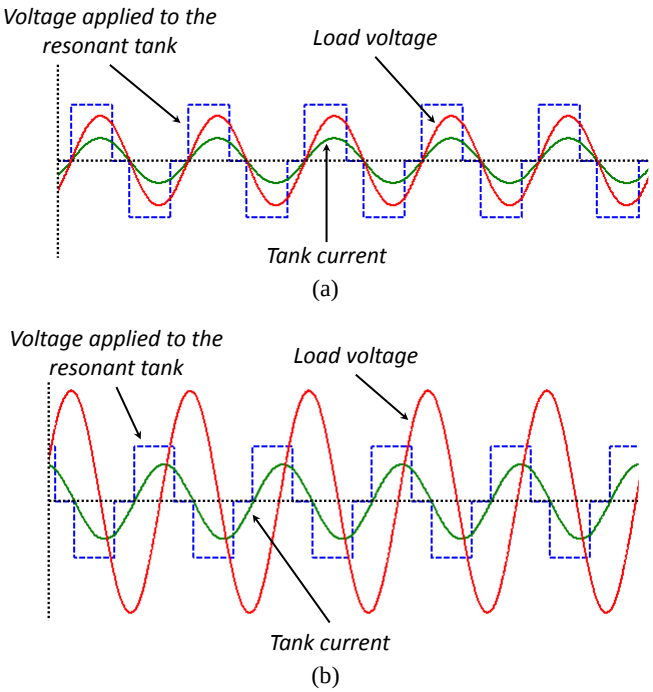


Fig. 2.23 Waveforms using frequency-phase control: (a) series and (b) parallel converter.

With this control strategy, one inverter leg (leg A) switches at zero crossing of the tank current (ZCS), whereas the other leg (leg B) presents hard switching, as shown in figure 2.22. In order to achieve ZVS operation for leg B, snubber capacitors can be utilised across the semiconductor devices [1-2, 8-12].

To implement frequency-phase control, it is necessary to determine the switching frequency for a defined modulation index, thus, the switching frequency may be considered as a function of the modulation index (M_{FPC}) and, for instance, a polynomial approximation may be employed [1-2, 8-10], as given by (2.16).

$$f_s = \sum_{k=0}^{n} a_k \, (M_{FPC})^{\,k} \tag{2.16}$$

This polynomial approximation is calculated by considering a fixed quality factor, i.e. constant load (R_{AC}). In order to implement this control strategy with a variable quality factor (variable load), a different approximation approach must be considered, for example, a surface fitting approximation as is used in [11, 12].

2.4 Summary

This chapter has briefly introduced some conventional resonant converter topologies. In addition, several resonant circuit configurations and their main parameters have been presented. Among the converter topologies, load resonant converters have been considered in more detail, describing the structure, operation and control.

Specifically, two load resonant converter topologies, series and parallel, have been considered in this chapter. For these converters, three control strategies, namely frequency control, phase control and frequency-phase control, have been described.

Chapter 3

Predictive Control of Power Converters

3.1 Introduction

Model Predictive Control (MPC) has been continuously researched over a number of recent decades and for a wide range of applications [13, 14]. MPC employs a model of the process to be controlled, thus, the future behaviour of the plant may be pre-calculated or predicted in order to determine an optimum value for the control signal [13-16]. There are several predictive control strategies which are currently used in industry, such as Dynamic Matrix Control (DMC), Generalised Predictive Control (GPC) and Predictive Functional Control (PFC), which are based on different models that include constraints and/or disturbances [13, 14].

In a MPC strategy [13-16], the model is utilised to predict the outputs at future instants according to the prediction horizon (N_p), which determines the number of samples ahead which must be predicted. To calculate the optimal control signal, an objective function, usually called a cost function, must be defined and minimised. Generally, this is based on the error between the predicted output and the reference, and takes the form of a quadratic function. In addition, it may also include the control effort. After optimising the cost function, a set of samples for the control signal is obtained. The number of samples is defined by the control horizon (N_c), however, only the first value of the control signal set is applied to the system since the future values will be recalculated considering more information (measurements, calculations, etc.) over future sampling periods. This process of applying a single control signal and carrying out the calculation of a new control signal value every sampling instant is

known as a receding horizon strategy [13-16]. A scheme for MPC, considering $N_p=N_c=1$, is depicted in figure 3.1.

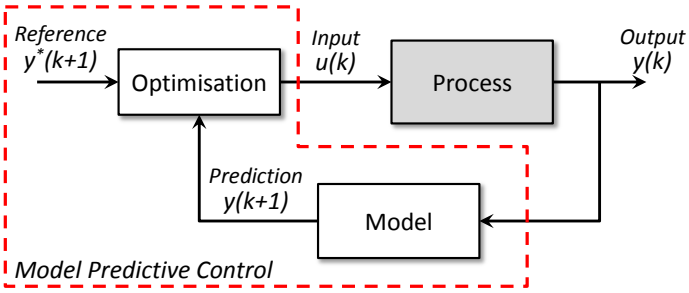


Fig. 3.1 Scheme for model predictive control ($N_p=N_c=1$).

Some advantages of MPC are [13-16]:

- It is relatively easy to understand and implement.
- It can be easily expanded to multivariable control.
- It is fairly simple to consider nonlinearities and constraints in the control system.

However, its dependency on parameter values and the potential requirement for a significant computational effort are some of the main drawbacks associated with this control strategy.

Since MPC needs to perform various calculations, it has been mainly utilised to control 'slow' processes. During recent decades, chiefly owing to the development of fast processors, MPC has become a control method applied to electrical systems such as power electronics and drives [15, 16]. Several characteristics of power converters and electrical drives make MPC a suitable control option [16]. These characteristics are depicted in figure 3.2.

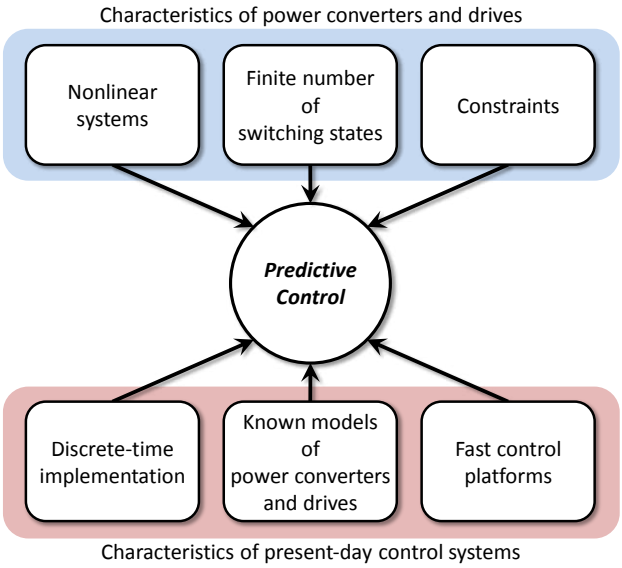


Fig. 3.2 Characteristics of power electronic systems which make MPC a suitable control option.

3.2 MPC for a SISO system

A simple MPC-based controller can be designed for a single-input/single-output (SISO) system. This controller calculates the input of the system by minimising a cost function based on the output error and the control effort [13, 14]. Considering the SISO system given by (3.1), where $\underline{x_o}$ is the state vector, u is the input and y is the output:

$$\begin{aligned} \underline{x_o}(k+1) &= A_o\underline{x_o}(k) + B_o u(k) \\ y(k) &= C_o\underline{x_o}(k) \end{aligned} \tag{3.1}$$

Then, defining the increments $\Delta\underline{x_o}(k)$, $\Delta u(k)$ and $\Delta y(k)$ as:

$$\Delta\underline{x_o}(k) = \underline{x_o}(k) - \underline{x_o}(k-1) \tag{3.2}$$

$$\Delta u(k) = u(k) - u(k-1) \tag{3.3}$$

$$\Delta y(k) = y(k) - y(k-1) \tag{3.4}$$

From (3.1)-(3.4), the increment of the state vector and of the output at t_{k+1} may be written as:

$$\Delta\underline{x_o}(k+1) = \underline{x_o}(k+1) - \underline{x_o}(k) \Rightarrow \Delta\underline{x_o}(k+1) = A_o\Delta\underline{x_o}(k) + B_o\Delta u(k) \tag{3.5}$$

$$\Delta y(k+1) = y(k+1) - y(k) \Rightarrow \Delta y(k+1) = C_o\Delta\underline{x_o}(k+1) \tag{3.6}$$

Considering a new vector given by [14]:

$$\underline{x}(k) = \begin{bmatrix} \Delta\underline{x_o}(k) \\ y(k) \end{bmatrix} \tag{3.7}$$

And, from (3.5)-(3.7), arranging a new system:

$$\begin{aligned} \begin{bmatrix} \Delta\underline{x_o}(k+1) \\ y(k+1) \end{bmatrix} &= \begin{bmatrix} A_o & 0 \\ C_oA_o & 1 \end{bmatrix}\begin{bmatrix} \Delta\underline{x_o}(k) \\ y(k) \end{bmatrix} + \begin{bmatrix} B_o \\ C_oB_o \end{bmatrix}\Delta u(k) \\ y(k) &= [0 \quad 1]\begin{bmatrix} \Delta\underline{x_o}(k) \\ y(k) \end{bmatrix} \end{aligned} \tag{3.8}$$

Equation (3.8) may be rewritten as:

$$\begin{aligned} \underline{x}(k+1) &= A\underline{x}(k) + B\Delta u(k) \\ y(k) &= C\underline{x}(k) \end{aligned} \tag{3.9}$$

In order to implement a predictive controller for the SISO system given by (3.1), a control horizon (N_c) and a prediction horizon (N_p) must be defined, thus, the sequences given by (3.10)-(3.12) are obtained [13, 14].

$$\Delta u(k) \quad \Delta u(k+1) \quad \cdots \quad \Delta u(k+N_c-1) \tag{3.10}$$

$$\underline{x}(k+1) \quad \underline{x}(k+2) \quad \cdots \quad \underline{x}(k+N_p) \tag{3.11}$$

$$y(k+1) \quad y(k+2) \quad \cdots \quad y(k+N_p) \tag{3.12}$$

Considering $N_p = N_c = 1$, to simplify calculations, and equation (3.9), the prediction of the output is:

$$y(k+1) = CA\underline{x}(k) + CB\Delta u(k) \tag{3.13}$$

Therefore, for a given reference output value (y^*), a cost function (G) to minimise the error of the output is given by (3.14), which includes the input increment (Δu) to consider the magnitude of the input variation (control effort), i.e. how fast the input variable can change or how large the input variable can be between two consecutive sampling periods [13, 14]. A coefficient λ is used to make Δu more or less important, thus, when λ=0, the controller does not consider how the input varies.

$$G = [y^* - y(k+1)]^2 + \lambda[\Delta u(k)]^2 \tag{3.14}$$

When minimising the cost function [13, 14], i.e. $\frac{\partial G}{\partial \Delta u} = 0$, equation (3.15) is obtained from (3.13) and (3.14):

$$\frac{\partial G}{\partial \Delta u} = \frac{\partial}{\partial \Delta u}\left\{\left[y^* - \left(CA\underline{x}(k) + CB\Delta u(k)\right)\right]^2 + \lambda[\Delta u(k)]^2\right\} = 0 \tag{3.15}$$

Thus, Δu is given by:

$$\Delta u(k) = \frac{CB}{(CB)^2 + \lambda}\left[y^* - CA\underline{x}(k)\right] \tag{3.16}$$

Rewriting (3.16) by using (3.8):

$$\Delta u(k) = \frac{C_o B_o}{(C_o B_o)^2 + \lambda}\left[y^* - y(k) - C_o A_o \Delta \underline{x}_o(k)\right] \tag{3.17}$$

As a result, from (3.2) and (3.3), the predictive controller equation is:

$$u(k) = u(k-1) + \frac{C_o B_o}{(C_o B_o)^2 + \lambda}\left[y^* - y(k) - C_o A_o \underline{x}_o(k) + C_o A_o \underline{x}_o(k-1)\right] \tag{3.18}$$

3.3 Predictive control methods for power converters

Different predictive strategies have been used in power electronics and drives [15-17], namely deadbeat control, hysteresis-based predictive control, trajectory-based predictive control and model predictive control. Table 3.1 summarises the main characteristics of each method [16, 17].

Deadbeat control aims to make the output reach the reference value (error equal to zero) in the next sampling instant. Hysteresis-based strategy maintains the output within a tolerance band (hysteresis area), whereas trajectory-based control forces the system to follow predefined trajectories. With regard to MPC strategies, there are two methods: with a continuous control set and with a finite control set. The first strategy generates a continuous control variable, therefore, this requires a modulator to control the power converter. Unlike this, a MPC with finite control set method is based on the limited number of switching states of a power converter, hence, this approach controls directly the converter without employing any modulation strategy.

Table 3.1 Predictive control strategies used in power electronics and drives.

Predictive control method		Characteristics
Deadbeat control		▪ Uses a modulator ▪ Fixed switching frequency ▪ Low computations ▪ Constraints not included
Hysteresis-based		▪ No modulator ▪ Variable switching frequency ▪ Simple concepts
Trajectory-based		▪ No modulator ▪ Variable switching frequency ▪ No cascaded structure
Model Predictive Control	MPC with continuous control set	▪ Needs a modulator ▪ Fixed switching frequency ▪ Constraints may be included
	MPC with finite control set	▪ No modulator ▪ Variable switching frequency ▪ Online optimisation ▪ Low complexity (N_p= N_c=1) ▪ Constraints may be included

3.4 MPC applied to power converters

From table 3.1, there are several predictive control strategies employed in power electronics and drives. This section is focused on model predictive control with finite control set or also called finite control set model predictive control (FCS-MPC) [16-18], which is based on the switching model of a power converter and considers the control signal of every power switch as a control variable. As previously mentioned, FCS-MPC does not need a modulator since the switching signals are the output of the controller and these are directly applied to the power converter. Since the switching

signals do not necessarily follow a defined pattern, this strategy produces a variable switching frequency. For this approach, the optimisation is carried out online at every sampling period and, generally, a prediction and a control horizon equal to one are used [16-18]. Figures 3.3 and 3.4 show an example of an FCS-MPC scheme when implemented on a power electronic system and the concept of this control strategy, respectively.

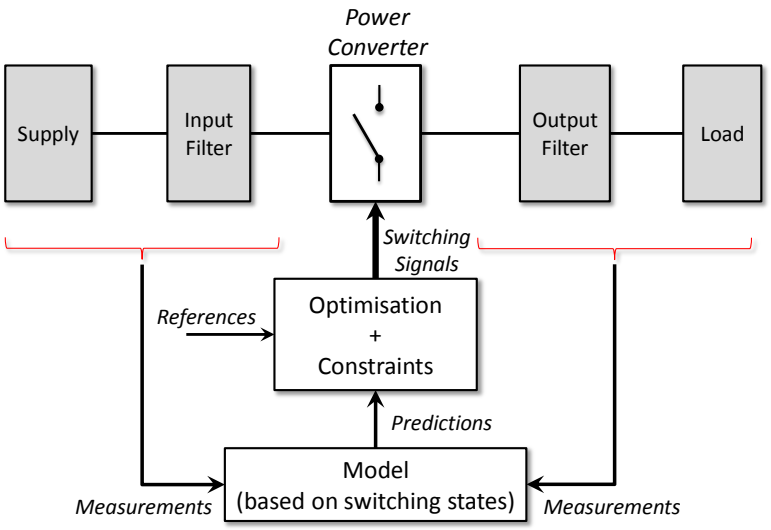


Fig. 3.3 Scheme of FCS-MPC for a power electronic system.

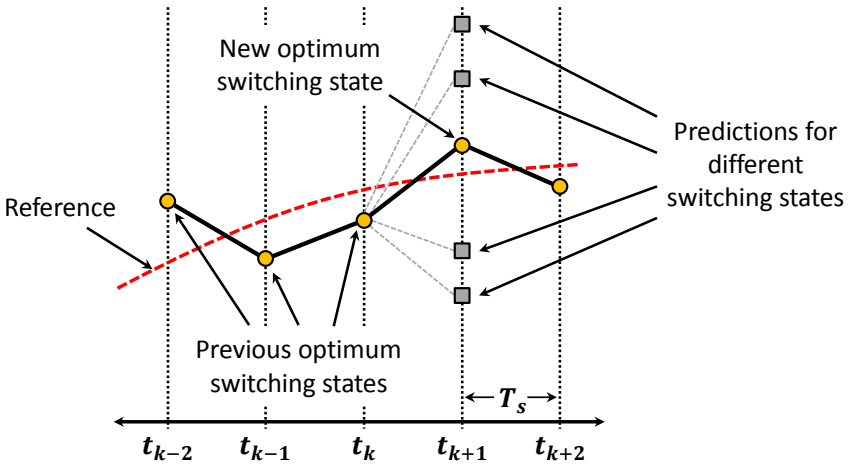


Fig. 3.4 Concept of FCS-MPC.

3.4.1 Switching model of a power converter

A power converter can be considered as a set of power switches, which correspond to power semiconductor devices such as IGBT, MOSFET, diodes, etc. For a switched mode converter, these semiconductor devices operate in two states, namely saturation and cut-off, which function as ‘on’ and ‘off’ states, respectively. To analyse the

behaviour of a power converter, a power switch is considered to be ideal, appearing as a short circuit (zero impedance) when on and as an open circuit (infinite impedance) when off [7, 19]. In addition, every change between states, from ‘on’ to ‘off’ and vice versa, is considered to be instantaneous, incurring zero loss during the transition.

Although an ideal switch operation is considered when analysing a power converter, in reality, when a switch is ‘on’, there is a small voltage drop across the terminals whose value depends on the semiconductor device employed and the operational state of the circuit. Similarly, during an ‘off’ state, there is a small leakage current [7, 19]. Furthermore, the process of turning a device on and off does not occur instantaneously, thus, the current through the device increases or decreases gradually. Figure 3.5 shows an ideal power switch and some configurations of power switches based on IGBTs utilised in different converter topologies.

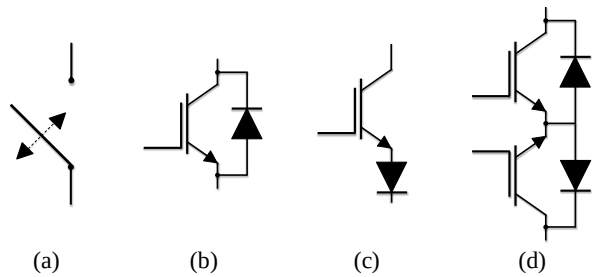


Fig. 3.5 Some power switches using IGBTs: (a) ideal switch, (b) unidirectional switch (current can flow in both directions/only positive voltage across the device can be blocked), (c) unidirectional switch (current can flow in one direction/positive and negative voltage across the device can be blocked) and (d) bidirectional switch (common emitter configuration).

The switching model of a power converter is based on the on-off operation of a power switch, which is defined by a switching function. An example of a switching function is given in (3.19). Therefore, using this function, voltages and currents of the power converter may be obtained. Generally, the switching functions are result of a modulation strategy, such as pulse width modulation (PWM).

$$S(t) = \begin{cases} 1, \text{ when power switch is 'on'} \\ 0, \text{when power switch is 'off'} \end{cases} \tag{3.19}$$

Some strategies to control power converters, such as space vector modulation (SVM), are based on all possible allowed combinations of switching elements. Each combination [16-18, 20], called a switching state, produces different input and output voltages/currents, hence, the behaviour of a power converter can be determined by these states. In order to determine the switching states of a power converter, it is necessary to consider some restrictions related to the converter operation. Thus, depending on whether the power converter has a voltage or current source, the

switching states for a similar power converter structure, considering ideal switches, are different in order to ensure that Kirchhoff's voltage and current laws are maintained. In figure 3.6, a schematic diagram of a three-phase inverter with ideal switches is illustrated. Figure 3.7 shows a three-phase voltage source inverter (VSI) and a three-phase current source inverter (CSI), both using IGBTs. In addition, table 3.2 presents the switching states for both inverters.

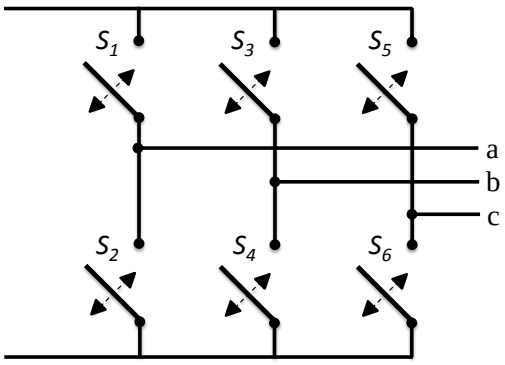
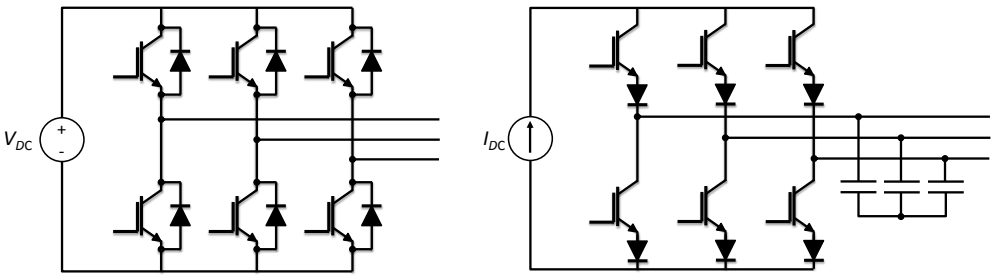


Fig. 3.6 Three-phase inverter with ideal switches.



(a) (b)

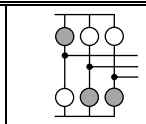
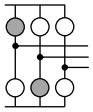
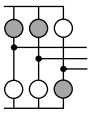
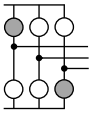
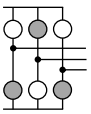
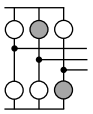
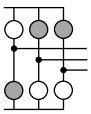
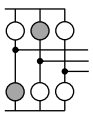
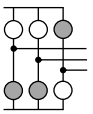
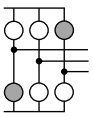
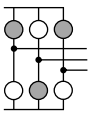
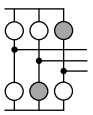
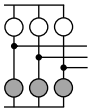
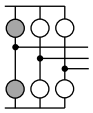
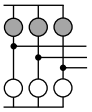
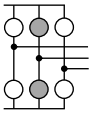
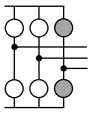
Fig. 3.7 Three-phase inverter: (a) VSI and (b) CSI.

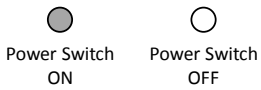
Consequently, a switching model may be represented by matrices, such as equations (3.20) and (3.21) for both inverter topologies [7, 20].

$$\begin{bmatrix} V_{ab}(t) \\ V_{bc}(t) \\ V_{ca}(t) \end{bmatrix} = \begin{bmatrix} \frac{\{S_1(t)-S_2(t)\}-\{S_3(t)-S_4(t)\}}{2} \\ \frac{\{S_3(t)-S_4(t)\}-\{S_5(t)-S_6(t)\}}{2} \\ \frac{\{S_5(t)-S_6(t)\}-\{S_1(t)-S_2(t)\}}{2} \end{bmatrix} V_{DC} \tag{3.20}$$

$$\begin{bmatrix} I_a(t) \\ I_b(t) \\ I_c(t) \end{bmatrix} = \begin{bmatrix} \{S_1(t) - S_2(t)\} \\ \{S_3(t) - S_4(t)\} \\ \{S_5(t) - S_6(t)\} \end{bmatrix} I_{DC} \tag{3.21}$$

Table 3.2 Switching states for three-phase inverters (VSI and CSI).

Voltage Source Inverter (VSI)					Current Source Inverter (CSI)				
	Switching state	V_{ab}	V_{bc}	V_{ca}		Switching state	I_a	I_b	I_c
Active switching states		V_{DC}	0	$-V_{DC}$	Active switching states		I_{DC}	$-I_{DC}$	0
		0	V_{DC}	$-V_{DC}$			I_{DC}	0	$-I_{DC}$
		$-V_{DC}$	V_{DC}	0			0	I_{DC}	$-I_{DC}$
		$-V_{DC}$	0	V_{DC}			$-I_{DC}$	I_{DC}	0
		0	$-V_{DC}$	V_{DC}			$-I_{DC}$	0	I_{DC}
		V_{DC}	$-V_{DC}$	0			0	$-I_{DC}$	I_{DC}
Zero switching states		0	0	0	Zero switching states		0	0	0
		0	0	0			0	0	0
							0	0	0



3.4.2 Prediction equations

For the FCS-MPC strategy, prediction equations of every variable to be controlled are needed, hence, to control a power electronic system, a model including power converter, load, filters, etc. must be defined. From the previous section, a power converter may be represented by a switching model, thus, in order to obtain the prediction equations, the model of every component of the system (load, filter, etc.) must be combined with the switching model, which provides output and input voltages/currents of the power converter. Prediction equations are usually derived

using a first order approximation of the derivative, as given in (3.22), or a discrete-time state-space representation, as in (3.23) [16, 17].

$$\frac{d}{dt}x(t) = \frac{x(k+1) - x(k)}{T_s} \tag{3.22}$$

$$\begin{aligned} \underline{x}(k+1) &= A\underline{x}(k) + B\underline{u}(k) \\ \underline{y}(k+1) &= C\underline{x}(k+1) \end{aligned} \tag{3.23}$$

3.4.3 Cost function and optimisation

The controller output (switching state) is determined by minimising the error between the reference and the prediction of the variable to be controlled. The expression to be optimised is denominated cost function (G) and it may include several variables (multivariable control). Normally, this is implemented via the absolute value or the square of the error [16-18], as given by (3.24), where x^* is a reference value and x^p is the corresponding prediction.

$$\begin{aligned} G &= |x^* - x^p| \\ G &= (x^* - x^p)^2 \end{aligned} \tag{3.24}$$

Optimisation of the cost function is carried out by evaluating the cost function using every switching state and selecting the one which achieves the minimum value. Since this procedure depends on the number of switching states, it may demand a significant number of calculations. A flowchart of the optimisation process is shown in figure 3.8, where N is the number of switching states, x_i^{k+1} is the prediction at t_{k+1} for the i-th switching state ($1 \leq i \leq N$), x^k is the value of x at t_k, S_i^k is the i-th switching state, and S_{opt}^k is the switching state to be applied at t_k.

As previously mentioned, the cost function can contain different terms, such as another variable to be controlled, some additional terms related to the control effort or some constraints, for instance, minimisation of switching frequency, reduction of the switching losses and voltage/current limitations [16-18]. When the cost function is composed of several terms, in order to consider the significance of each term, coefficients known as weighting factors are employed [16-18], which allow tuning of the cost function. Equation (3.25) gives an example of a cost function with two variables to be controlled and an additional term (F), where λ_1, λ_2 and λ_3 are weighting factors.

$$G = \lambda_1 \left| x_1^* - x_1^p \right| + \lambda_2 \left| x_2^* - x_2^p \right| + \lambda_3 F \tag{3.25}$$

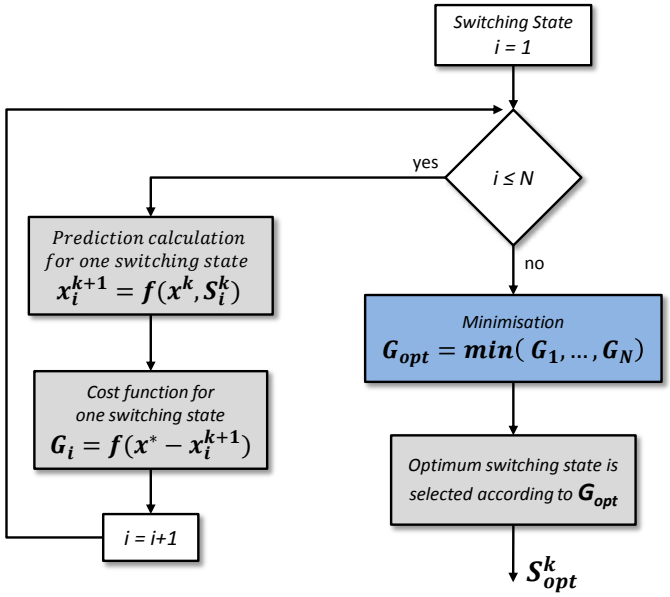


Fig. 3.8 Optimisation process.

Furthermore, when two or more variables have to be regulated, the error of each variable can be normalised [16-18], resulting in per-unit values, which leads to a homogeneous cost function. An example is given by (3.26), where x_1^n, x_2^n and x_3^n are the corresponding nominal values.

$$G = \lambda_1 \frac{|x_1^* - x_1^p|}{x_1^n} + \lambda_2 \frac{|x_2^* - x_2^p|}{x_2^n} + \lambda_3 \frac{|x_3^* - x_3^p|}{x_3^n} \tag{3.26}$$

3.4.4 Delay compensation

Ideally, a predictive control strategy can minimise the error at t_{k+1} by applying a new switching state (S_{opt}) at t_k, as shown in figure 3.9.

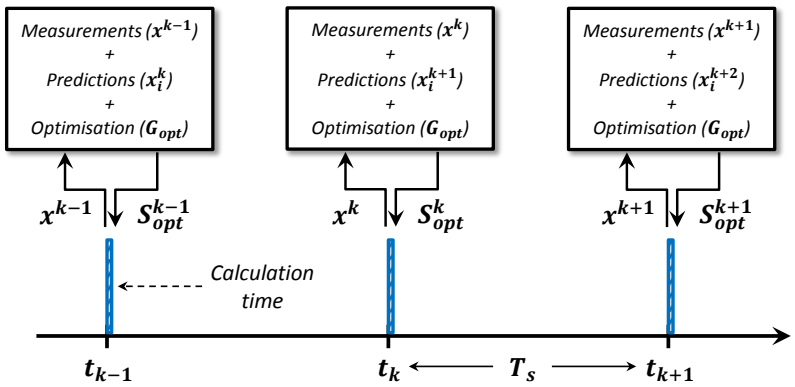


Fig. 3.9 Ideal implementation of FCS-MPC.

Since FCS-MPC is digitally implemented, every calculation consumes time, as a consequence, this generates a predictable delay which must be compensated. One compensation approach is based on optimising the cost function at t_{k+2} and applying the optimum switching state at t_{k+1} [16, 17]. In order to implement this approach, it is necessary to obtain every variable at t_{k+1} instead of measurements at t_k, therefore, a simple option is to estimate the values at t_{k+1} using the optimum switching state applied at t_k (previous result of optimisation), measurements and the model of the system. In figures 3.10 and 3.11, a flowchart of the optimisation process taking into account the calculation delay and a diagram of FCS-MPC implemented in a digital control platform are depicted, respectively.

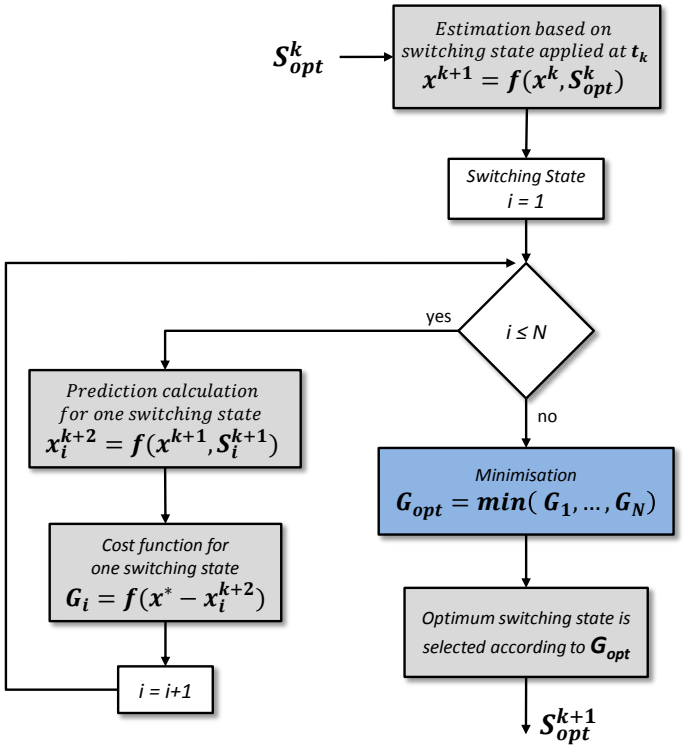


Fig. 3.10 Optimisation process with calculation delay.

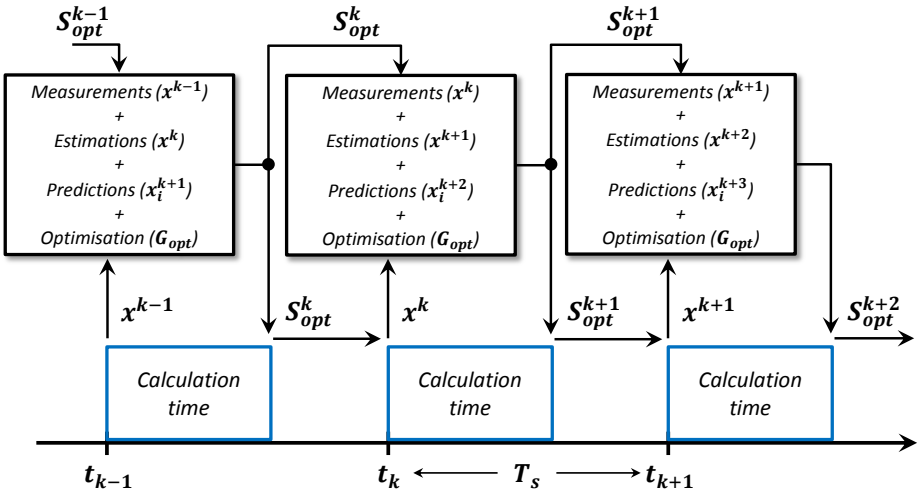


Fig. 3.11 Actual implementation of FCS-MPC.

3.4.5 Predictive control implementation

There are four basic stages in the implementation of an FCS-MPC algorithm: measurements, estimations, predictions and optimisation. Each of these stages is explained as follows:

- Measurements: In this stage, all of the variables needed are measured, either variables to be controlled or any state variable. If it is not possible to measure some variable, an observer may be utilised in order to estimate its value.
- Estimations: Owing to the calculation delay generated (actual digital implementation), it is not feasible to minimise the error at t_{k+1} and apply the optimal switching state at t_k, therefore, the entire process is shifted from t_k to t_{k+1}, and, as a result, the model is employed to estimate the variables at t_{k+1} as well as to predict the variables at t_{k+2}. In order to calculate the estimations at t_{k+1}, the previous optimum switching state calculated at t_{k-1} but applied at t_k, $S_{opt}(k)$, is used.
- Predictions: The predictions at t_{k+2} are calculated by using the estimated values of every variable at t_{k+1} and every switching state. These predicted values are used to obtain the errors at t_{k+2} which are included in the cost function.
- Optimisation: After calculating the predicted values for every switching state at t_{k+2}, a cost function is defined (one value for each switching state), mainly, based on each error at t_{k+2}. Then, the optimisation (minimisation) is performed online, i.e. it is carried out during every sampling period, and, according to the minimum value of the cost function, the optimal switching state to be applied at t_{k+1} is determined.

In figures 3.12 and 3.13, flowcharts of FCS-MPC implementation with and without delay compensation are depicted. In these, a general system is considered, hence, a multi-input/multi-output (MIMO) state-space model is used. Outputs and inputs are measured, and the output predictions are calculated based on the state vector predictions, which depend on the converter switching states. The cost function (G_i) is also given in a general form, where Λ is a diagonal matrix, given in (3.27), that contains the weighting factors, and F is an additional term which represents some constraint or other variable to be taken into account during optimisation. The optimisation process compares every value of the cost function in order to determine the switching state that minimises it. Finally, the optimal switching state is applied to

the power converter. The MIMO system considered is given by (3.28), where $\underline{x}$ is the state vector, $\underline{v}$ is an input vector (related to the power converter), S is a matrix of switching functions, which is different for each switching state, $\underline{y}$ is the output vector and N is the number of switching states. In (3.27) and (3.28), n, m, q and r are used to indicate the dimension of every element.

$$[\Lambda]_{rxr} = \begin{bmatrix} \lambda_1 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \lambda_r \end{bmatrix} \tag{3.27}$$

$$\begin{aligned} \left[\underline{x}(k+1)\right]_{nx1} &= [A]_{nxn}\left[\underline{x}(k)\right]_{nx1} + [B]_{nxm}\left\{[S(k)]_{mxq}\left[\underline{v}(k)\right]_{qx1}\right\} \\ \left[\underline{y}(k+1)\right]_{rx1} &= [C]_{rxn}\left[\underline{x}(k+1)\right]_{nx1} \end{aligned} \tag{3.28}$$

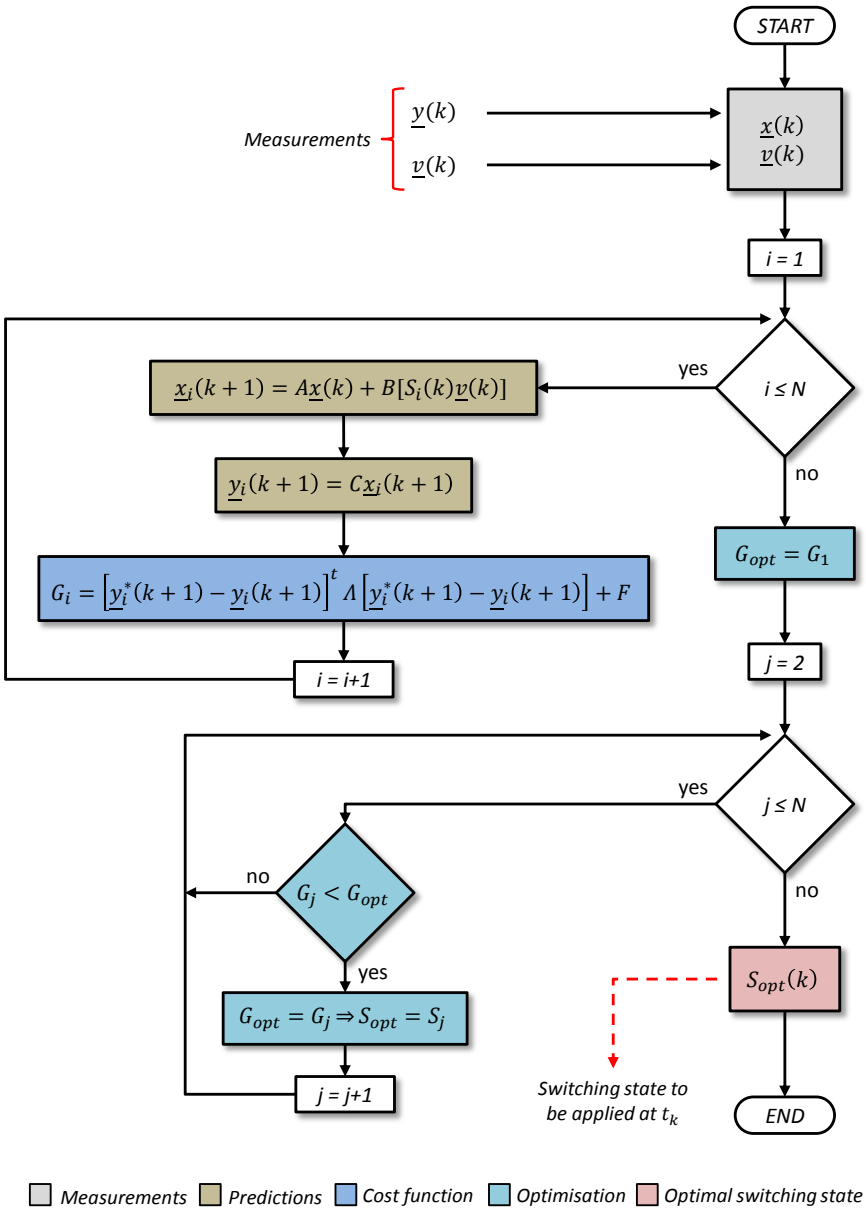


Fig. 3.12 Flowchart of FCS-MPC without delay compensation.

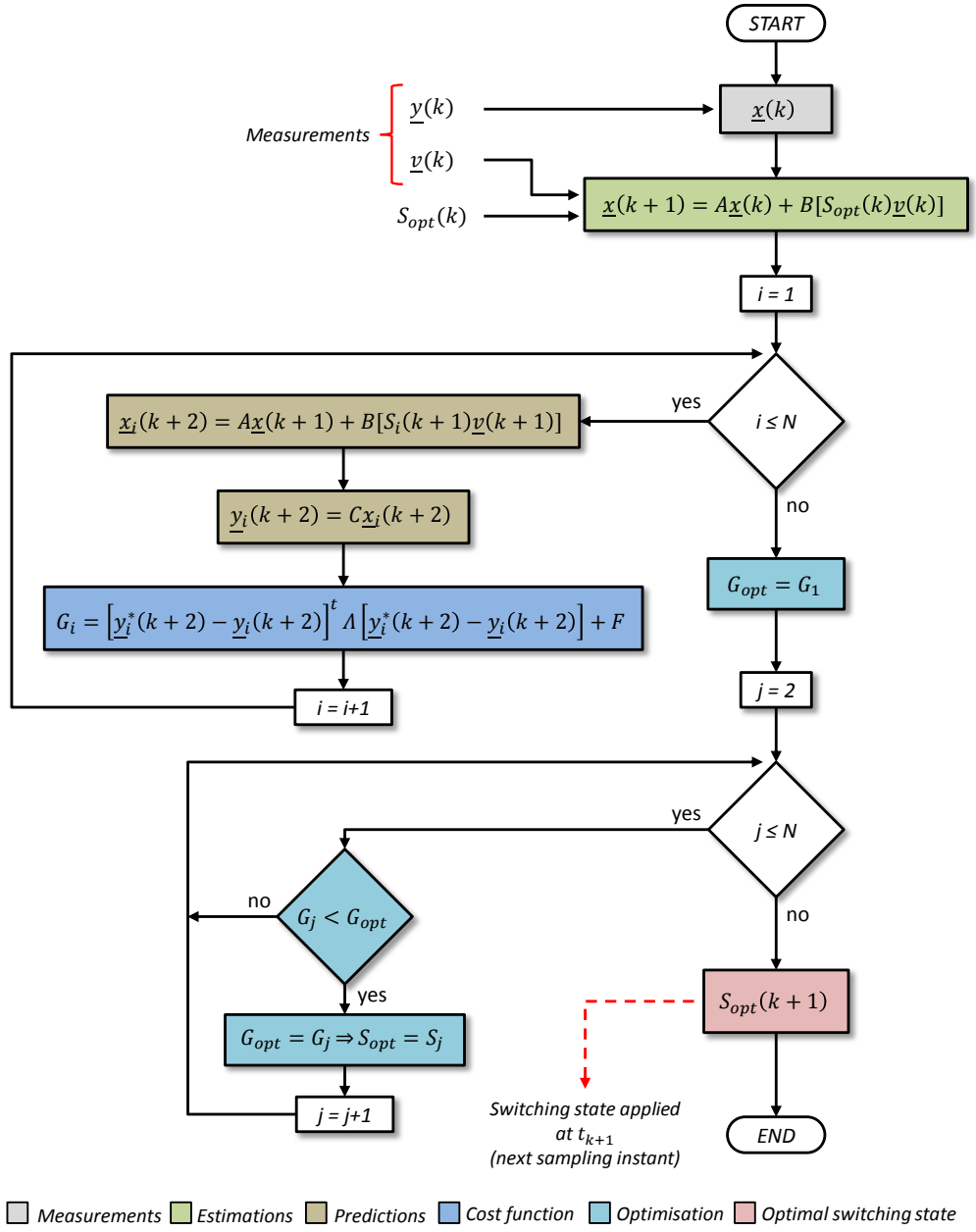


Fig. 3.13 Flowchart of FCS-MPC with delay compensation.

3.5 Summary

This chapter has introduced Model Predictive Control (MPC) applied to power electronic systems and has focused on FCS-MPC (model predictive control with finite control set) that allows controlling a power converter by applying directly a switching state during a sampling period. This switching state is the result of the predictive control strategy. Implementation with/without calculation delay compensation has been presented. In addition, other predictive control approaches used in power electronics and drives have also been considered.

Chapter 4

Direct Resonant Power Converter

4.1 Introduction

This chapter introduces the direct resonant converter (DRC) and considers two DRC topologies, namely the direct parallel resonant converter (DPRC) and the direct series resonant converter (DSRC). A DPRC has been utilised in previous work, whereas a DSRC is the topology that this research focuses on. Since this work focused on the control of a DRC, a resistive load is considered. The structure, main characteristics, model and switching states are described. Furthermore, an analysis of the zero current switching (ZCS) operation and voltage/current limitations for both DRC topologies is carried out.

4.2 Direct resonant converter

In a direct resonant converter (DRC), the inverter of a load resonant converter is replaced by a matrix converter which connects the three-phase input directly to the resonant tank. This converter has been considered for use in high voltage applications [3-4, 21-24] as seen in figure 4.1, where a diagram of a high voltage DC power supply based on a DRC is shown. A DRC presents several potential advantages [3, 4]:

- High power density. Since there is no dc-link capacitor and the size of reactive components can be reduced owing to the high frequency operation.
- High quality input power. Sinusoidal input current may be obtained by using a suitable control strategy and input filter design.
- Unity power factor operation. When employing a proper control strategy.

- High efficiency. The losses are reduced by switching the semiconductor devices at every zero crossing of the output current (ZCS).

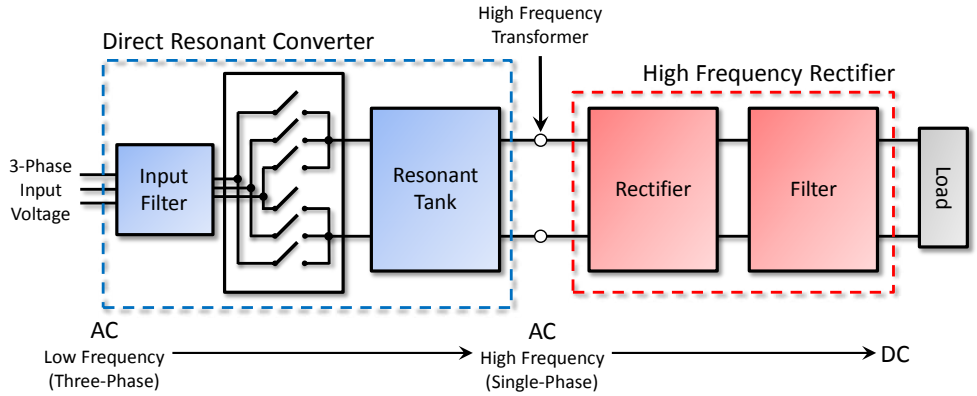


Fig. 4.1 Diagram of a high voltage DC power supply based on a direct resonant converter.

As a combination of matrix and load resonant converters, the DRC is composed of three main parts: an input filter, a three-phase to single-phase array of power switches and a resonant tank, as depicted in figure 4.1. The input filter consists of an LCR filter, which allows current filtering as well as smoothing of the input converter voltage. The three-phase to single-phase array of semiconductor devices is composed of six bidirectional power switches which are configured such that any output can be connected to any input. Finally, the resonant tank comprises inductive and capacitive elements which, when being fed with a voltage at a defined frequency by the converter, can generate a high frequency sinusoidal output voltage/current. Different resonant circuits configurations were discussed in chapter 2. In addition, to achieve safe operation of a DRC, an overvoltage protection circuit must be implemented [3-4, 25-26].

4.2.1 Resonant tank

As a load resonant converter, different configurations of resonant circuits can be used in a DRC, such as series, series resonant parallel loaded (SRPL) or LCC circuits. In previous work [3-4, 21-24], a SRPL tank is utilised, therefore, the load voltage is the voltage across the tank capacitor. In contrast, this work employs a series resonant tank, where the load current corresponds to the converter output current. Figure 4.2 illustrates both direct resonant converter topologies with a resistive load, a direct parallel resonant converter (DPRC) and a direct series resonant converter (DSRC), respectively.

Since the magnitude of the voltage provided by a DRC is intrinsically variable, in order to avoid significant distortion at the output, a higher quality factor, when

compared with a conventional resonant inverter, is needed. Values of quality factor between 4 and 10 can make the resonant tank less susceptible to the output converter voltage variations [3, 4].

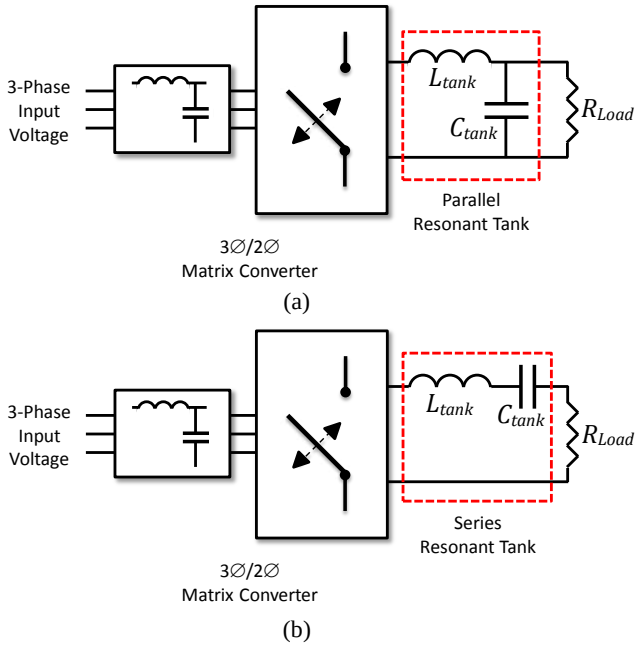


Fig. 4.2 Scheme of a DRC with resistive load: (a) DPRC and (b) DSRC.

4.2.2 Model and switching states

The three-phase to single-phase matrix converter with ideal switches is depicted in figure 4.3. This circuit can be modelled by equations (4.1) and (4.2), where S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn} and S_{cn} are the switching functions for each power switch.

$$\begin{bmatrix} v_p(t) \\ v_n(t) \end{bmatrix} = \begin{bmatrix} S_{ap}(t) & S_{bp}(t) & S_{cp}(t) \\ S_{an}(t) & S_{bn}(t) & S_{cn}(t) \end{bmatrix} \begin{bmatrix} v_{ia}(t) \\ v_{ib}(t) \\ v_{ic}(t) \end{bmatrix} \Rightarrow [v_{pn}] = [S][v_{iabc}] \tag{4.1}$$

$$\begin{bmatrix} i_{ia}(t) \\ i_{ib}(t) \\ i_{ic}(t) \end{bmatrix} = \begin{bmatrix} S_{ap}(t) & S_{an}(t) \\ S_{bp}(t) & S_{bn}(t) \\ S_{cp}(t) & S_{cn}(t) \end{bmatrix} \begin{bmatrix} i_p(t) \\ i_n(t) \end{bmatrix} \Rightarrow [i_{iabc}] = [S]^t [i_{pn}] \tag{4.2}$$

From (4.1) and (4.2), the output converter voltage and the output current, which correspond to the voltage applied to the resonant tank (v_{tank}) and the tank current (i_{tank}), are given by:

$$v_{tank} = v_p - v_n = (S_{ap} - S_{an})v_{ia} + (S_{bp} - S_{bn})v_{ib} + (S_{cp} - S_{cn})v_{ic} \tag{4.3}$$

$$i_{tank} = i_p = -i_n \tag{4.4}$$

Using (4.4), the input converter currents are calculated by:

$$i_{ia} = S_{ap}i_p + S_{an}i_n \Rightarrow i_{ia} = (S_{ap} - S_{an})i_{tank} \tag{4.5}$$

$$i_{ib} = S_{bp}i_p + S_{bn}i_n \Rightarrow i_{ib} = (S_{bp} - S_{bn})i_{tank} \tag{4.6}$$

$$i_{ic} = S_{cp}i_p + S_{cn}i_n \Rightarrow i_{ic} = (S_{cp} - S_{cn})i_{tank} \tag{4.7}$$

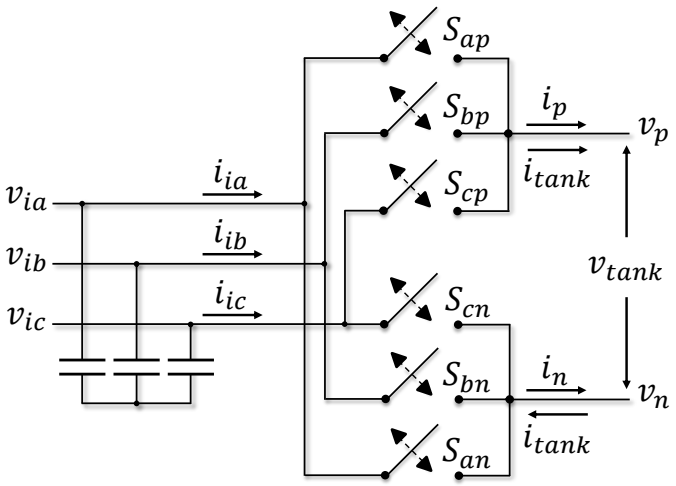


Fig. 4.3 Three-phase to single-phase matrix converter with ideal switches.

In order to prevent a short circuit between input phases and/or interrupting the output current path, the switching functions are constrained by [25]:

$$\begin{aligned} S_{ap} + S_{bp} + S_{cp} &= 1 \\ S_{an} + S_{bn} + S_{cn} &= 1 \end{aligned} \tag{4.8}$$

By considering (4.8), nine switching states, six active states and three zero states, can be defined. Each switching state and the corresponding input current and output voltage are given in table 4.1. Moreover, these switching states are shown in figure 4.4.

Table 4.1 Switching states for a DRC.

	Switching state	Switches ON		Input current			Output voltage
				i_{ia}	i_{ib}	i_{ic}	v_{tank}
Active states	1	S_{ap}	S_{bn}	i_{tank}	$-i_{tank}$	0	v_{iab}
	2	S_{ap}	S_{cn}	i_{tank}	0	$-i_{tank}$	v_{iac}
	3	S_{bp}	S_{cn}	0	i_{tank}	$-i_{tank}$	v_{ibc}
	4	S_{bp}	S_{an}	$-i_{tank}$	i_{tank}	0	v_{iba}
	5	S_{cp}	S_{an}	$-i_{tank}$	0	i_{tank}	v_{ica}
	6	S_{cp}	S_{bn}	0	$-i_{tank}$	i_{tank}	v_{icb}
Zero states	7	S_{ap}	S_{an}	0	0	0	0
	8	S_{bp}	S_{bn}	0	0	0	0
	9	S_{cp}	S_{cn}	0	0	0	0

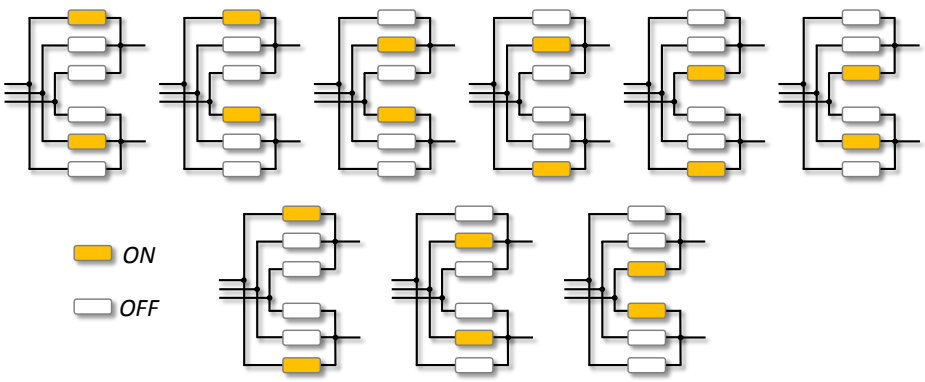


Fig. 4.4 Switching states for a DRC.

Finally, a switching model for a DRC based on equations (4.3)-(4.7) is depicted in figure 4.5.

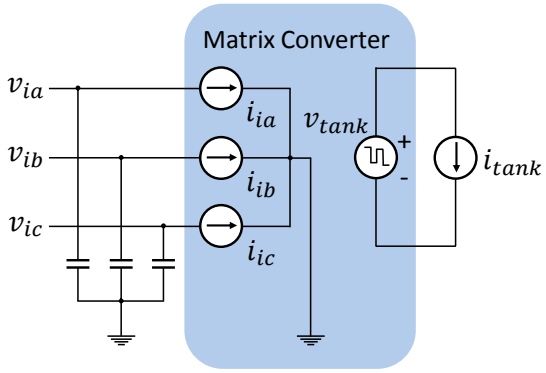
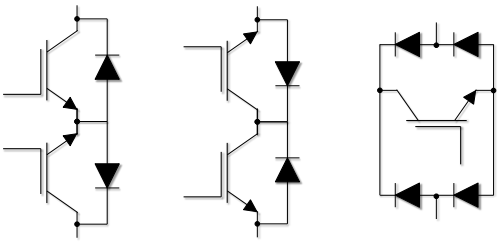


Fig. 4.5 Switching model of a DRC.

4.2.3 Bidirectional switches and commutation strategies

A bidirectional power switch allows current to circulate in both directions and can block voltage in both directions. There are several configurations for a bidirectional power switch [25, 26], such as common emitter, common collector and diode bridge arrangements. These power switch arrangements, using IGBTs, are shown in figure 4.6. The main differences between configurations reside in conduction power losses and the number of gate drive circuit power supplies needed [7, 8]. Specifically, in this work, a common emitter bidirectional switch is employed.



(a) (b) (c)

Fig. 4.6 Bidirectional switch configurations using IGBTs: (a) common emitter, (b) common collector, and (c) diode bridge.

The commutation strategy for bidirectional switches is a crucial process for any matrix-converter-based topology. This allows the power converter to operate safely without causing a short circuit at the input and/or an output open circuit when switches are turned on/off. Thus, for a bidirectional switch formed of two unidirectional semiconductor arrangements, the commutation process specifies the correct sequence to turn on/off every active device. A strategy widely used is that denominated four-step commutation [25], which can be controlled by the output current direction (current-based commutation), where the output current sign is measured, or by the relative magnitudes of the input voltages (voltage-based commutation), where the line-to-line input voltage sign is employed. Figure 4.7 illustrates both commutation methods considering a simple two-phase to single-phase circuit and a defined commutation time (t_c).

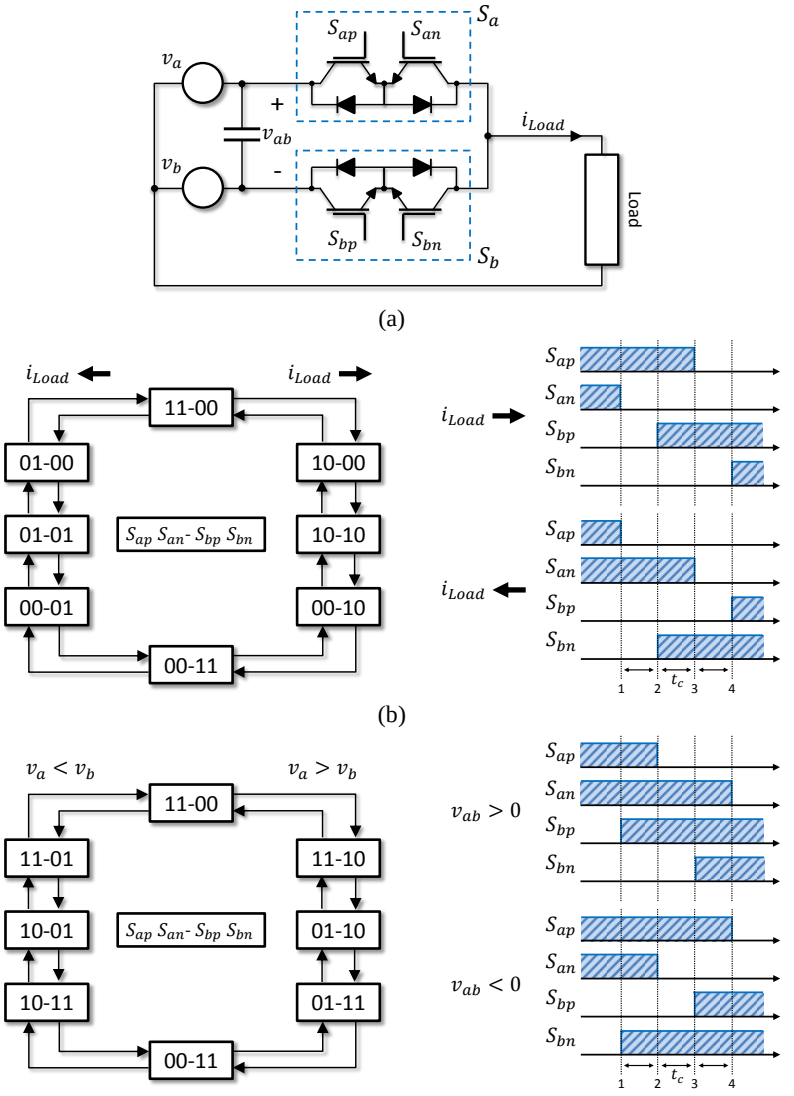


Fig. 4.7 Four-step commutation strategy: (a) circuit with two bidirectional switches, (b) current-based commutation, and (c) voltage-based commutation.

4.2.4 Input filter

In order to filter the high frequency components of the current generated by the converter at the input, a filter circuit is connected between the supply and the converter power circuit. Normally, as in matrix converters, a second order LCR circuit can be used, figure 4.8(a), however, depending on the characteristics of the system, for example, the resulting harmonic content or implemented control strategy, an optimised filter might be needed as in [3, 24], where the filter shown in figure 4.8(b) was implemented in order to reduce the power loss in the input filter.

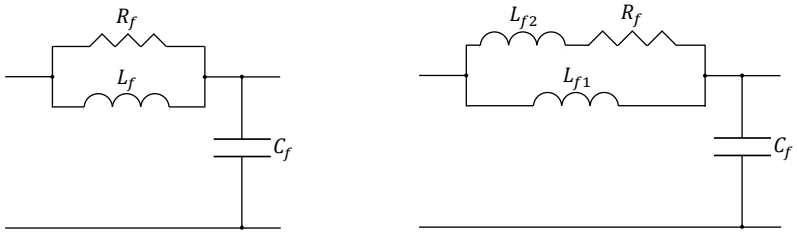


Fig. 4.8 Input filter configurations: (a) input filter with damping resistor in parallel with the inductor (typical filter used in matrix converters), and (b) input filter implemented in [3, 24].

Since the output is a high frequency current and soft-switching operation is expected, the input filter design could become a laborious task. Thus, different factors must be taken into account, such as:

- Current harmonics at the input.
- Quality of the input capacitor voltage.
- Cut-off frequency.
- Size of the reactive elements.
- Power losses.

4.2.5 Overvoltage protection

The overvoltage protection circuit, also called clamp circuit, is used to protect the power converter from overvoltages produced by, for instance, line perturbations, commutation failure or a device failure [25, 26]. The purpose of this circuit is to create a path for the output current (tank current) in order to absorb the energy stored at the input or output when a fault condition occurs and the converter is turned off. The clamp circuit for a DRC is composed of a RC circuit and 10 fast-recovery diodes, as shown in figure 4.9. Since the energy stored in the resonant tank is small, a low rating clamp circuit with a small capacitor is required.

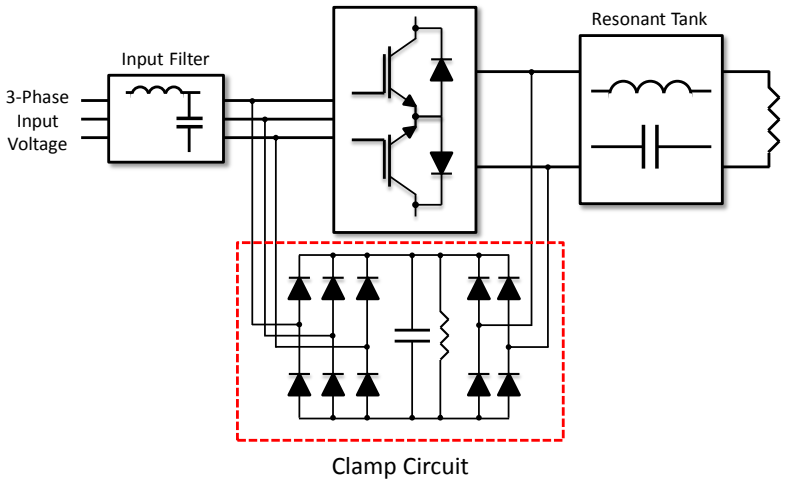


Fig. 4.9 Clamp circuit for a DRC.

4.3 Zero current switching operation

Considering that the tank loaded quality factor is sufficiently high, the resonant tank can produce a high frequency sinusoidal current when the converter supplies a voltage whose frequency is close to the tank resonant frequency. The voltage applied to the resonant circuit is produced by connecting the output to a line-to-line input voltage, as shown in figure 4.10. Therefore, considering the output frequency is much greater than the input frequency, the voltage applied to the resonant tank can be considered as a variable magnitude square wave voltage.

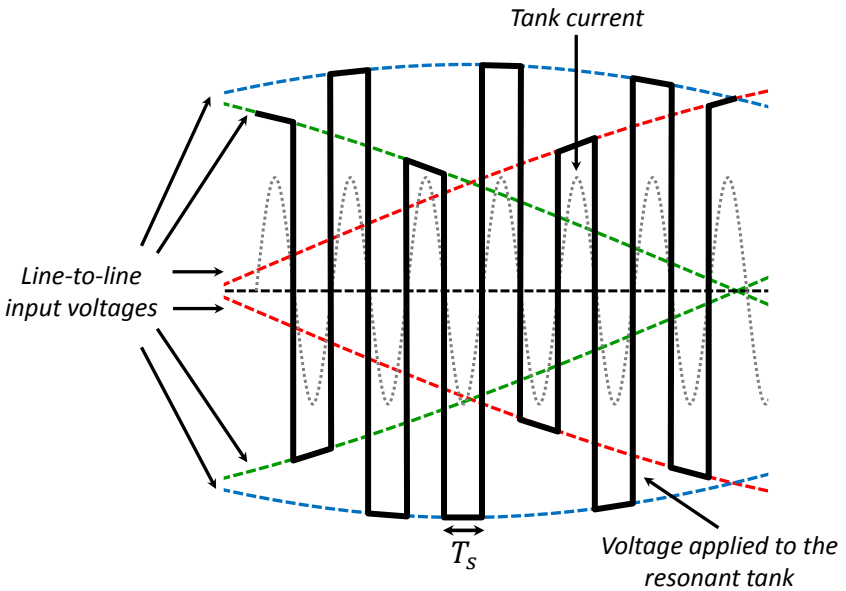


Fig. 4.10 Voltage applied to the resonant tank.

When the operating frequency is equal to the resonant frequency (f_r), the converter can be switched at every zero crossing of the output current, i.e. zero current switching, since the voltage and current are in phase. Hence, a ZCS control strategy must operate at a sampling/switching frequency of twice the resonant frequency, i.e. $T_s = (2f_r)^{-1}$.

4.3.1 Input converter current under ZCS

As discussed in section 4.2.2, the input converter current is determined by the converter switching and the output current, thereby, under ZCS, it consists of multiple fixed-width current pulses which correspond to half cycles of the resonant tank current, as illustrated in figure 4.11, where the input converter current for a switching state (switching state 1 in table 4.1) is shown. As a result, a low frequency sinusoidal input current (i_{in}) (supply frequency) can be synthesised by achieving a sinusoidal current pulse distribution. Thus, in order to control the input current, an equivalent rectangular pulse can be considered, as depicted in figure 4.12. Figures 4.13 and 4.14 show the input converter current and the equivalent input current, respectively.

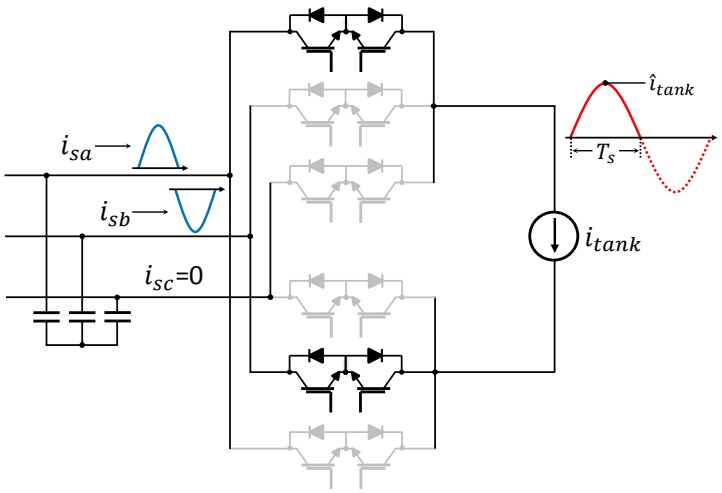


Fig. 4.11 Input converter current for a switching state ($\boldsymbol{S_{ap}}$ and $\boldsymbol{S_{bn}}$ are switched on).

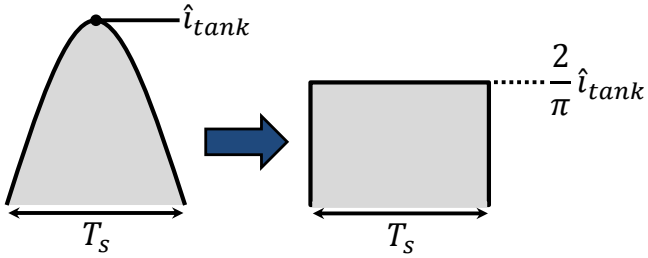


Fig. 4.12 Equivalent current pulse.

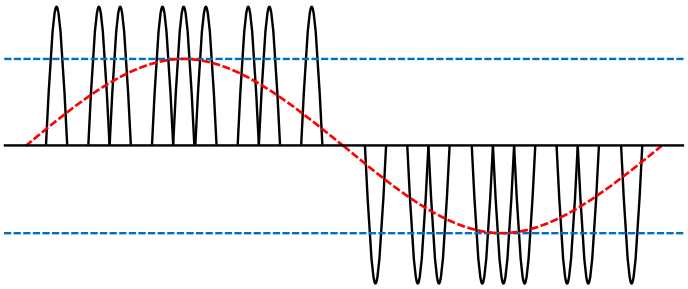


Fig. 4.13 Input converter current.

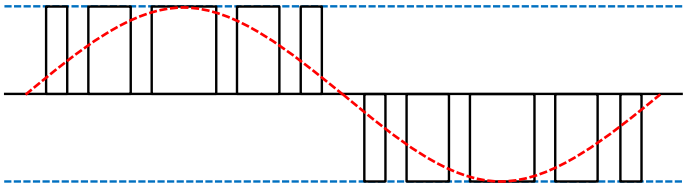


Fig. 4.14 Equivalent input converter current (average).

As observed in figure 4.14, the maximum value of the low frequency input current is given by the average value of the output current (maximum magnitude of an equivalent rectangular pulse). Therefore, the low frequency input current is limited by:

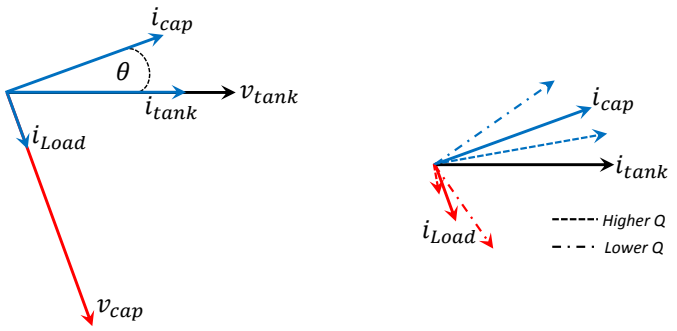
$$\hat{\imath}_{in} \leq \frac{2}{\pi}\hat{\imath}_{tank} \tag{4.9}$$

Furthermore, if the constraint given by (4.9) is not satisfied, the input converter current will be composed of a large number of successive pulses, leading to overmodulation of the DRC.

4.3.2 Parallel resonant tank under ZCS

In a SRPL circuit, the phase shift between the resonant tank current (i_{tank}, current through the inductor) and the tank capacitor voltage (v_{cap}, which corresponds to the voltage across the load) depends on the loaded quality factor (Q). For high values of Q, the load current becomes small in comparison with the tank current, resulting in a phase shift of, approximately, 90° and a resonant frequency (ω_r) close to the natural frequency (ω_o). On the other hand, for low values of the quality factor, the load current becomes more significant, leading to a smaller phase shift and a lower resonant frequency. Equations (4.10) and (4.11) show the resonant frequency and the current relationship as a function of the quality factor, where $\hat{\imath}_{cap}$ and $\hat{\imath}_{Load}$ are the peak value of the tank capacitor and load current, respectively. From the phasor diagram in figure 4.15, the value of the tank capacitor voltage when the tank current is

zero can be calculated by (4.13), where $\hat{v}_{cap}$ is the peak capacitor voltage. Figure 4.16 shows voltage and current waveforms for a SRPL tank under ZCS.



(a) (b)

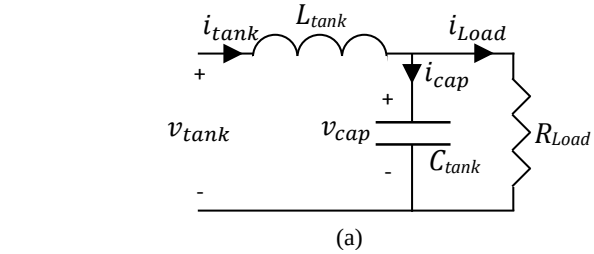
Fig. 4.15 Phasor diagram for a SRPL tank under ZCS: (a) voltages and currents and (b) currents for different values of loaded quality factor.

$$\omega_r = \omega_o \sqrt{1 - \frac{1}{Q^2}} \tag{4.10}$$

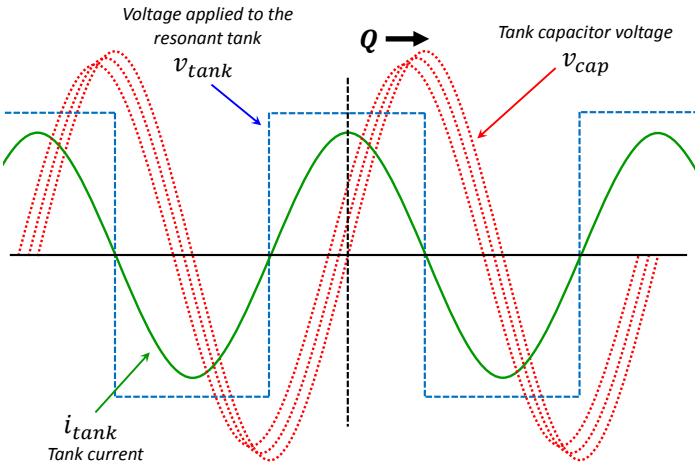
$$\hat{\imath}_{cap} = \hat{\imath}_{Load}\sqrt{Q^2 - 1} \Rightarrow \hat{\imath}_{tank} = \hat{\imath}_{Load} Q = \hat{\imath}_{cap} \left(\sqrt{1 - \frac{1}{Q^2}} \right)^{-1} \tag{4.11}$$

$$\theta = tan^{-1}\left(\frac{\hat{\imath}_{Load}}{\hat{\imath}_{cap}}\right) = tan^{-1}\left(\frac{1}{\sqrt{Q^2 - 1}}\right) \tag{4.12}$$

$$v_{cap}(t_{i_{tank}=0}) = \pm \hat{v}_{cap} cos(\theta) \tag{4.13}$$



(a)



(b)

Fig. 4.16 SRPL tank under ZCS: (a) SRPL circuit, and (b) waveforms for a SRPL tank.

4.3.3 Series resonant tank under ZCS

In a series resonant tank, soft switching can be achieved when operating at the natural frequency since this is equal to the resonant frequency. Thus, the tank current leads the capacitor voltage by 90°. Voltage and current waveforms for a series resonant tank operating under ZCS are shown in figure 4.17.

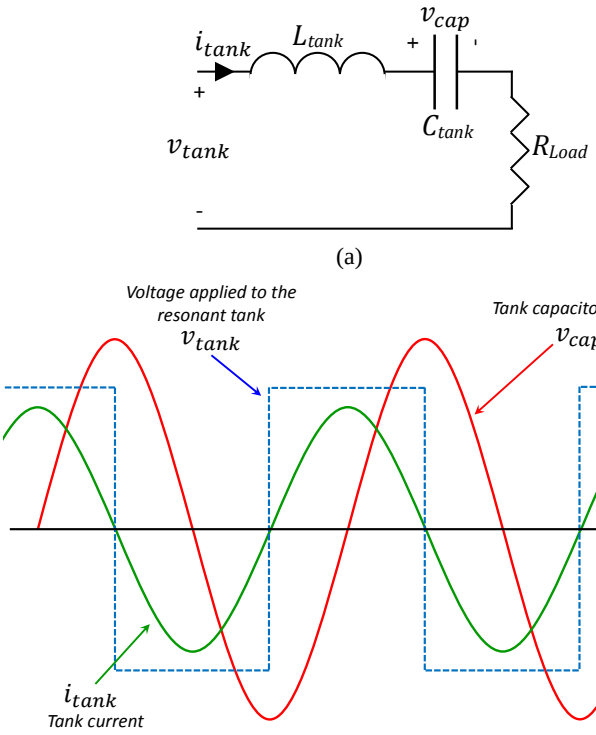


Fig. 4.17 Series resonant tank under ZCS: (a) series resonant circuit, and (b) waveforms for a series resonant tank.

4.4 Limitations under ZCS

In this section, the limitations for the input current and output voltage are defined. The restriction for the input current is determined for each DRC topology by taking into account operation at unity power factor and the resonant tank characteristics. For the output converter voltage, a study of the resulting distortion considering the output voltage waveform is carried out.

4.4.1 Input current limitation

Under ZCS, the restriction given by (4.9) must be satisfied in order to avoid input current saturation (overmodulation), which entails low frequency distortion. Therefore, considering that the input filter removes the high frequency components of

the input converter current, the constraint (4.9) can be rewritten as in (4.14), where $\hat{\imath}_s$ is the peak supply current.

$$\hat{\imath}_s \leq \frac{2}{\pi}\hat{\imath}_{tank} \tag{4.14}$$

Thus, from (4.14), expressions for the input current limit, for a DPRC and a DSRC, in terms of the loaded quality factor and input voltage can be obtained.

4.4.1.1 Input current limitation for a DPRC

In a DPRC operating under ZCS, hence, operating at the resonant frequency, and considering (4.10), the tank capacitor voltage (load voltage) is given by:

$$\hat{v}_{cap} = \frac{1}{\omega_r C_{tank}}\hat{\imath}_{cap} \Rightarrow \hat{v}_{cap} = \left(\sqrt{1-\frac{1}{Q^2}}\right)^{-1} Z_o \hat{\imath}_{cap} \tag{4.15}$$

Then, neglecting power losses, an expression for the tank capacitor voltage can be determined from the power balance equation:

$$P_{in} = P_{Load} \Rightarrow \frac{3}{2}\hat{v}_s\hat{\imath}_s = \frac{1}{2}\frac{\hat{v}_{cap}^2}{R_{Load}} \Rightarrow \hat{v}_{cap} = \sqrt{3\hat{v}_s\hat{\imath}_s R_{Load}} \tag{4.16}$$

By using (4.11), (4.15) and (4.16), the tank current can be calculated by:

$$\hat{\imath}_{tank} = \frac{\hat{v}_{cap}}{Z_o}\sqrt{1-\frac{1}{Q^2}}\left(\sqrt{1-\frac{1}{Q^2}}\right)^{-1} \Rightarrow \hat{\imath}_{tank} = \sqrt{\frac{3\hat{v}_s\hat{\imath}_s R_{Load}}{Z_o^2}} \tag{4.17}$$

Therefore, replacing the tank current in (4.14) by (4.17), the constraint given by (4.14) becomes:

$$\sqrt{\frac{3\hat{v}_s\hat{\imath}_s R_{Load}}{Z_o^2}} \geq \frac{\pi}{2}\hat{\imath}_s \tag{4.18}$$

Since $Q = \frac{R_{Load}}{Z_o}$, then the supply current limit is:

$$\hat{\imath}_s \leq \frac{12}{\pi^2}\frac{\hat{v}_s}{Z_o}Q \tag{4.19}$$

4.4.1.2 Input current limitation for a DSRC

Following an identical process as that carried out for a DPRC, the output current for a DSRC is given by:

$$P_{in} = P_{Load} \Rightarrow \frac{3}{2}\hat{v}_s\hat{\imath}_s = \frac{1}{2}R_{Load}\hat{\imath}_{tank}^2 \Rightarrow \hat{\imath}_{tank} = \sqrt{\frac{3\hat{v}_s\hat{\imath}_s}{R_{Load}}} \quad (4.20)$$

Therefore, in this case, (4.14) is transformed into:

$$\hat{\imath}_s \leq \frac{12}{\pi^2}\frac{\hat{v}_s}{R_{Load}} \quad (4.21)$$

Then, since $Q = \frac{Z_o}{R_{Load}}$ for a series resonant circuit, (4.21) results in the same constraints defined by (4.19):

$$\hat{\imath}_s \leq \frac{12}{\pi^2}\frac{\hat{v}_s}{Z_o}Q \quad (4.22)$$

4.4.1.3 Input current limitation in terms of converter voltage ratio

The maximum voltage that can be applied to the resonant tank is determined by the line-to-line input voltage. Therefore, considering the fundamental frequency component of the square wave voltage applied to the resonant tank (section 4.3), the maximum voltage applied to the resonant tank ($\hat{v}_{o,max}$, maximum output converter voltage) is given by (4.23), where $\hat{v}_s$ is the peak value of the phase input voltage.

$$\hat{v}_{o,max} = \frac{4}{\pi}\sqrt{3}\hat{v}_s \quad (4.23)$$

Thus, a converter voltage ratio (M_v) can be defined by:

$$M_v = \frac{\hat{v}_o}{\hat{v}_{o,max}} \quad (4.24)$$

From (4.23) and (4.24), the fundamental component of the voltage applied to the resonant tank (output converter voltage) as a function of the converter voltage ratio is:

$$\hat{v}_o = \frac{4}{\pi}\sqrt{3}M_v\hat{v}_s \; ; \; 0 \leq M_v \leq 1 \quad (4.25)$$

In addition, calculating the tank current, where the total impedance, for both resonant circuits, is:

$$|Z| = \frac{Z_o}{Q} \quad (4.26)$$

$$\hat{\imath}_{tank} = \frac{\hat{v}_o}{|Z|} = \frac{(Q\hat{v}_o)}{Z_o} \quad (4.27)$$

Therefore, considering equation (4.17), the input current for a DPRC is given by:

$$\hat{\imath}_s = \frac{(Q\hat{v}_o)^2}{3\hat{v}_s R_{Load}} \tag{4.28}$$

From (4.20), the input current for a DSRC is:

$$\hat{\imath}_s = \frac{(Q\hat{v}_o)^2 R_{Load}}{3\hat{v}_s Z_o^2} \tag{4.29}$$

Then, from (4.28), (4.29) and (4.14), the voltage applied to the resonant tank, for both converters, is constrained by:

$$\hat{v}_o \leq \frac{6}{\pi}\hat{v}_s \tag{4.30}$$

Thus, from (4.30) and (4.25), the voltage ratio for both converters is limited by:

$$M_v \leq \frac{\sqrt{3}}{2} \tag{4.31}$$

4.4.2 Output converter voltage limitation

Ideally, the converter should supply a square wave voltage to the resonant tank, however, the output converter voltage (v_o) is formed by applying a line-to-line input voltage at every switching instant. Therefore, in order to determine the maximum output converter voltage, an analysis is carried out by considering the output voltage waveforms and the resulting distortion.

From figure 4.18, four different levels for a required voltage magnitude, where $\hat{v}_{LL}$ is the peak line-to-line input voltage, can be defined as follows:

A. $\frac{\sqrt{3}}{2}\hat{v}_{LL} < \hat{v}_o < \hat{v}_{LL}$

B. $\frac{1}{2}\hat{v}_{LL} < \hat{v}_o < \frac{\sqrt{3}}{2}\hat{v}_{LL}$

C. $0 < \hat{v}_o < \frac{1}{2}\hat{v}_{LL}$

D. $\hat{v}_o = \frac{\sqrt{3}}{2}\hat{v}_{LL}$

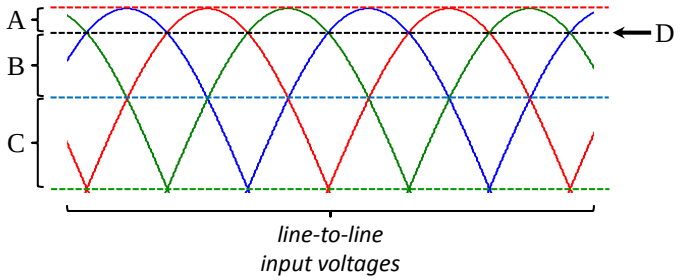


Fig. 4.18 Voltage levels considered for output converter voltage analysis.

For a required voltage in 'A', the output converter voltage will be given by $|v_o(t)| \geq \frac{\sqrt{3}}{2}\hat{v}_{LL}$, as shown in figure 4.19, leading to a voltage saturation. For a voltage in 'B', the converter voltage will be mainly limited by $\frac{1}{2}\hat{v}_{LL} \leq |v_o(t)| \leq \frac{\sqrt{3}}{2}\hat{v}_{LL}$, whereas for 'C', the resulting restriction will be $0 < |v_o(t)| \leq \frac{\sqrt{3}}{2}\hat{v}_{LL}$ (see figure 4.19). As a result, a significant distortion at the resonant tank could be generated. In 'D', a required output converter voltage equal to $\frac{\sqrt{3}}{2}\hat{v}_{LL}$ is considered, thus, in this case, the instantaneous output voltage will be restricted by $\frac{1}{2}\hat{v}_{LL} \leq |v_o(t)| \leq \hat{v}_{LL}$, as can be seen in figure 4.19. Despite the variation of the resulting voltage for 'D', the distortion at the resonant tank is minimised when operating at this voltage level, and, therefore, $\hat{v}_o = \frac{\sqrt{3}}{2}\hat{v}_{LL}$ corresponds to the optimal output converter voltage.

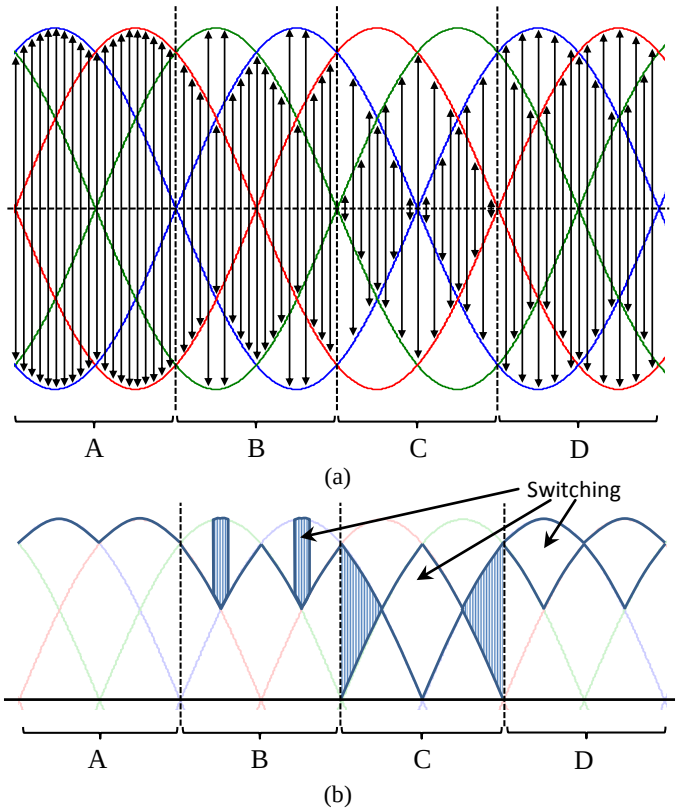


Fig. 4.19 Output converter voltage: (a) resulting output voltage, and (b) magnitude variation of (a).

Since the output converter voltage is constrained by $\hat{v}_o \leq \frac{\sqrt{3}}{2}\hat{v}_{LL}$, the fundamental frequency component of the voltage applied to the resonant tank and the converter voltage ratio are limited by (4.30) and (4.31), respectively. In addition, the optimal operating condition, only considering the converter output, is given by:

$$\hat{v}_o^{opt} = \frac{6}{\pi}\hat{v}_s \quad ; \quad M_v^{opt} = \frac{\sqrt{3}}{2} \tag{4.32}$$

4.5 Control of a DRC

Owing to the high frequency operation, control approaches based on pulse density modulation (PDM) have been investigated in previous research, such as area comparison pulse density modulation (AC-PDM) in [4]. Other attractive control techniques for a DRC are based on model predictive control (MPC). Predictive strategies for a direct parallel resonant converter were studied in [3, 4], whereas for a series topology, which is the subject of this work, predictive control approaches are considered in the next chapter.

4.6 Summary

The structure and main characteristics of a direct resonant converter (DRC) have been described in this chapter. The switching states and model, which will be used in the next chapters, have been presented. The DPRC have been considered since this topology has been studied in previous research.

This chapter has also included an analysis of the ZCS operation, where the limitations for the input current and output voltage have been studied. This analysis has been carried out for both DRC topologies, series and parallel, in an effort to generalise the voltage/current limitations.

Finally, in order to introduce the control of a DRC, some control strategies for a DPRC which were studied in previous work were cited. Predictive control strategies for a DSRC, which is the topic of this research, will be presented in the next chapters.

Chapter 5

Predictive Control Strategies for a Direct Series Resonant Converter

5.1 Introduction

This chapter presents the ZCS predictive control strategies developed during this research for a direct series resonant converter (DSRC). Since this research focuses on the control of a DSRC, a resistive load is considered, as shown in figure 5.1. Three predictive approaches are described in detail, namely input current predictive control (ICPC), output current predictive control (OCPC) and input-output predictive control (IOPC). The aims of these control strategies are:

- Sinusoidal three-phase input current (reduction of low order harmonics).
- Unity power factor.
- Sinusoidal resonant tank current (reduction of current oscillations).

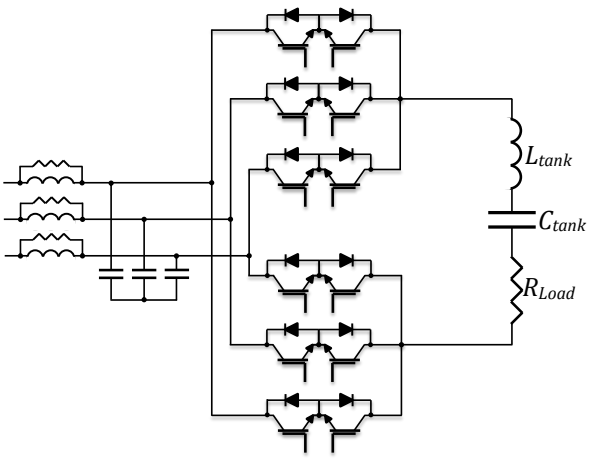


Fig. 5.1 Direct series resonant converter with resistive load.

This chapter also includes the approach for compensating the delay associated with the digital implementation, previously discussed in chapter 3, and simulation results for each control approach.

5.2 Input current predictive control (ICPC)

The purpose of this approach is to achieve supply currents with low harmonic content as well as unity power factor. Essentially, to obtain input sinusoidal currents, the control strategy must switch the converter in order to synthesise a sinusoidal fundamental component at the input.

In order to have an accurate prediction and control of the input current, this strategy is based on the state-space model of the input filter. The filter utilised in this research is a second order filter with a damping resistor in parallel with the inductance, as seen in figure 5.2, where the model employed for this approach is depicted. The model of a DSRC corresponds to the switching model presented in chapter 4.

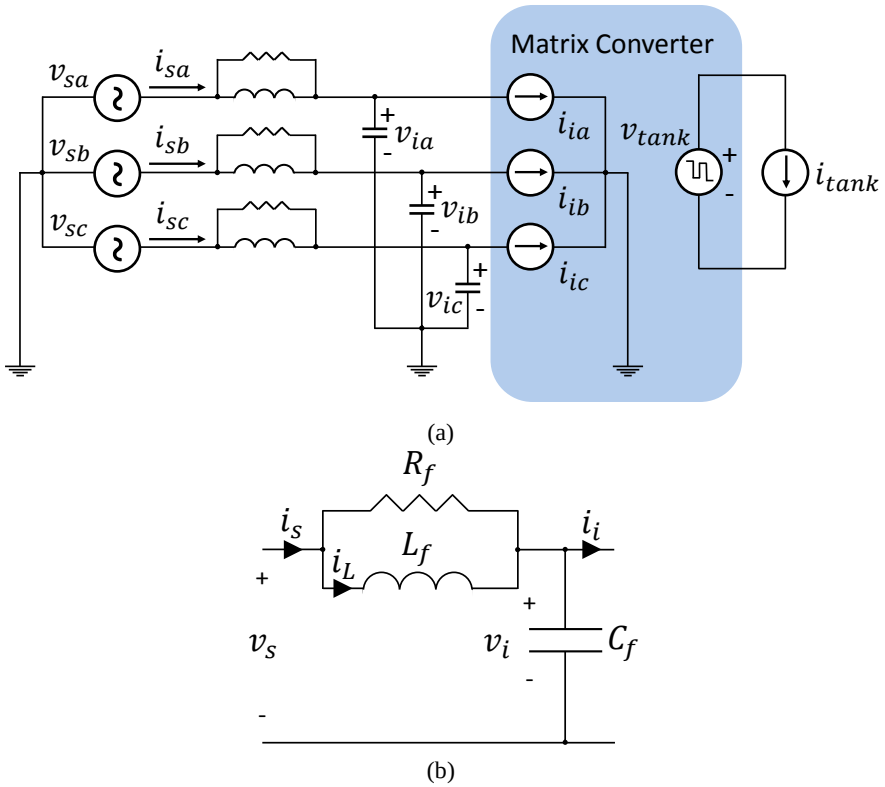


Fig. 5.2 Model for ICPC: (a) model of a DSRC and (b) input filter circuit.

The dynamic behaviour of the input filter is given by (5.1)-(5.2), where v_s, v_i, i_s, i_i and i_L are the input voltage, the capacitor voltage, the input current, the input converter current and the inductor current, respectively. In this model, the input converter current is considered independent of the input capacitor voltage and only

depends on the output converter current (i_{tank}) and the converter switching, as explained later in this chapter.

$$\begin{bmatrix} \frac{d}{dt} i_L(t) \\ \frac{d}{dt} v_i(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & -\frac{1}{R_f C_f} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_i(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_f} \\ -\frac{1}{C_f} & \frac{1}{R_f C_f} \end{bmatrix} \begin{bmatrix} i_i(t) \\ v_s(t) \end{bmatrix} \tag{5.1}$$

$$\begin{bmatrix} i_s(t) \\ v_i(t) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{R_f} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_i(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{R_f} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_i(t) \\ v_s(t) \end{bmatrix} \tag{5.2}$$

Prediction equations for the supply current and input capacitor voltage can be defined by discretising (5.1)-(5.2) [16] (see appendix A). Hence, the discrete-time model of the input filter is as follows:

$$\begin{bmatrix} i_L(k+1) \\ v_i(k+1) \end{bmatrix} = \begin{bmatrix} E_{in11} & E_{in12} \\ E_{in21} & E_{in22} \end{bmatrix} \begin{bmatrix} i_L(k) \\ v_i(k) \end{bmatrix} + \begin{bmatrix} F_{in11} & F_{in12} \\ F_{in21} & F_{in22} \end{bmatrix} \begin{bmatrix} i_i(k) \\ v_s(k) \end{bmatrix} \tag{5.3}$$

Then, from (5.2) and (5.3), the predictions of the supply current and input capacitor voltage can be written as:

$$i_s(k+1) = H_1 i_s(k) + H_2 v_i(k) + H_3 v_s(k) + \frac{1}{R_f} v_s(k+1) + H_4 i_i(k) \tag{5.4}$$

$$v_i(k+1) = E_{in21} i_s(k) + H_5 v_i(k) + H_6 v_s(k) + F_{in21} i_i(k) \tag{5.5}$$

Where:

$$H_1 = E_{in11} - \frac{E_{in21}}{R_f} \tag{5.6}$$

$$H_2 = E_{in12} + \frac{E_{in11}}{R_f} - \frac{E_{in21}}{R_f^2} - \frac{E_{in22}}{R_f} \tag{5.7}$$

$$H_3 = F_{in12} - \frac{E_{in11}}{R_f} + \frac{E_{in21}}{R_f^2} - \frac{F_{in22}}{R_f} \tag{5.8}$$

$$H_4 = F_{in11} - \frac{F_{in21}}{R_f} \tag{5.9}$$

$$H_5 = E_{in22} + \frac{E_{in21}}{R_f} \tag{5.10}$$

$$H_6 = F_{in22} - \frac{E_{in21}}{R_f} \tag{5.11}$$

Both predictions, (5.4) and (5.5), include the input converter current which, under ZCS operation, i.e. $T_s = t_{k+1} - t_k = (2f_r)^{-1}$ (f_r, resonant frequency), is composed

of current pulses (half cycles of the output current). Therefore, as previously explained in chapter 4, the average value of the input converter current over a sampling period is considered. Using table 5.1, the input converter current is given by:

$$i_i(k) = K_i \frac{2}{\pi} \hat{\imath}_{tank}(k) \tag{5.12}$$

In addition, the prediction of the supply current (5.4) contains the future value of the supply voltage. This value can be estimated, for instance, by considering the supply voltage variation over a sampling period is negligible, i.e. $v_s(k+1) = v_s(k)$, or by using (5.13) which is based on Lagrange polynomial extrapolation [16]:

$$v_s(k+1) = \sum_{i=0}^{n} (-1)^{n-i} \left[\frac{(n+1)!}{(n+1-i)!\, i!} \right] v_s(k+i-n) \tag{5.13}$$

Table 5.1 Input converter current (K_i) and output converter voltage for each switching state.

Switching state	j	Input converter current			Output converter voltage
		$K_{ia,j}$	$K_{ib,j}$	$K_{ic,j}$	$v_{tank,j}$
1	1	1	-1	0	v_{iab}
2	2	1	0	-1	v_{iac}
3	3	0	1	-1	v_{ibc}
4	4	-1	1	0	v_{iba}
5	5	-1	0	1	v_{ica}
6	6	0	-1	1	v_{icb}
7-8-9	7	0	0	0	0

Consequently, from (5.4) and (5.12), the prediction of the supply current per phase is given by:

$$i_{s,j}^{p} = H_1 i_s(k) + H_2 v_i(k) + H_3 v_s(k) + \frac{1}{R_f} v_s(k+1) + \cdots$$

$$\cdots + H_4 K_{i,j} \frac{2}{\pi} \hat{\imath}_{tank}(k) \quad ; \quad j = 1, \ldots, 7 \tag{5.14}$$

Since a balanced three-phase power supply is considered, control of the three-phase supply current can be achieved by regulating only two currents. Another option is to transform the three-phase current into alpha-beta or d-q current components. Accordingly, the cost function can be defined by:

$$G_{ICPC,j} = \left(i_{sa}^{*} - i_{sa,j}^{p} \right)^2 + \left(i_{sb}^{*} - i_{sb,j}^{p} \right)^2 \quad ; \quad j = 1, \ldots, 7 \tag{5.15}$$

Note that the cost function (5.15) must be evaluated for each switching state and then, the minimum value must be determined. A scheme of ICPC is shown in figure 5.3.

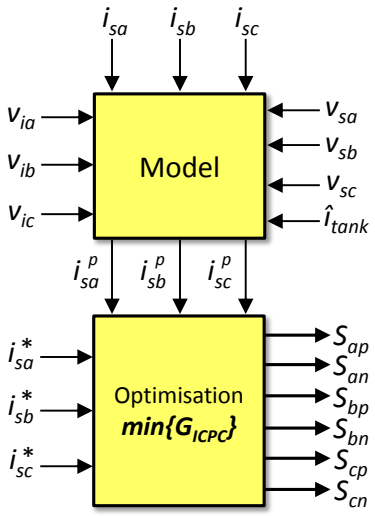


Fig. 5.3 Scheme of ICPC strategy.

5.3 Output current predictive control (OCPC)

This approach aims to control the output converter current, which corresponds to the load current in a DSRC. Figure 5.4 shows a series resonant circuit whose state-space model can be given by:

$$\begin{bmatrix} \frac{d}{dt} i_{tank}(t) \\ \frac{d}{dt} v_{cap}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{Load}}{L_{tank}} & -\frac{1}{L_{tank}} \\ \frac{1}{C_{tank}} & 0 \end{bmatrix} \begin{bmatrix} i_{tank}(t) \\ v_{cap}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{tank}} \\ 0 \end{bmatrix} v_{tank}(t) \tag{5.16}$$

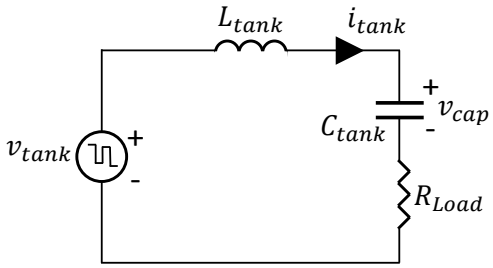


Fig. 5.4 Series resonant tank.

Discretising (5.16) (see appendix B), the discrete-time model of the resonant tank is given by (5.17). Since the converter is switched at every zero crossing of the tank current, i.e. $i_{tank}(k) = i_{tank}(k+1) = 0$ and $T_s = t_{k+1} - t_k = (2f_r)^{-1}$, in order to control this current, the prediction of the tank capacitor voltage, equation (5.18), is

utilised to determine the prediction of the magnitude of the tank current for each sampling/switching period.

$$\begin{bmatrix} i_{tank}(k+1) \\ v_{cap}(k+1) \end{bmatrix} = \begin{bmatrix} E_{out11} & E_{out12} \\ E_{out21} & E_{out22} \end{bmatrix} \begin{bmatrix} i_{tank}(k) \\ v_{cap}(k) \end{bmatrix} + \begin{bmatrix} F_{out1} \\ F_{out2} \end{bmatrix} v_{tank}(k) \tag{5.17}$$

$$v_{cap}(k+1) = E_{out22} v_{cap}(k) + F_{out2} v_{tank}(k) \tag{5.18}$$

The coefficients E_{out22} and F_{out2} are given by (5.19) and (5.20), where ω_o^{out}, ω_d^{out}, Z_o^{out}, δ_{out} and ψ_{out} correspond to the corner frequency, the damped natural frequency, the characteristic impedance, the damping factor and the angle defined by the poles of the resonant circuit, respectively.

$$E_{out22} = \frac{e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s + \psi_{out}) \tag{5.19}$$

$$F_{out2} = 1 - \frac{e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s + \psi_{out}) \tag{5.20}$$

$$\omega_o^{out} = \frac{1}{\sqrt{L_{tank}C_{tank}}} \quad ; \quad Z_o^{out} = \sqrt{\frac{L_{tank}}{C_{tank}}} \quad ; \quad \delta_{out} = \frac{R_{Load}}{2Z_o^{out}} \tag{5.21}$$

$$\omega_d^{out} = \omega_o^{out}\sqrt{1-\delta_{out}^2} \quad ; \quad \psi_{out} = tan^{-1}\left(\frac{\sqrt{1-\delta_{out}^2}}{\delta_{out}}\right) \tag{5.22}$$

Thus, considering a sinusoidal tank current and (5.16), the tank current magnitude, see figure 5.5, can be calculated by:

$$i_{tank}(t) = C_{tank}\frac{d}{dt}v_{cap}(t) \Rightarrow \hat{\imath}_{tank}(k) = (\omega_d^{out}C_{tank})v_{cap}(k) \tag{5.23}$$

Therefore, considering (5.18) and (5.23), the magnitude of the tank current at every sampling period can be predicted by:

$$\hat{\imath}_{tank}(k+1) = E_{out22}\hat{\imath}_{tank}(k) + (\omega_d^{out}C_{tank}F_{out2})v_{tank}(k) \tag{5.24}$$

Thus, the prediction of the tank current magnitude is given by:

$$\hat{\imath}_{tank,j}^{p} = E_{out22}\hat{\imath}_{tank}(k) + (\omega_d^{out}C_{tank}F_{out2})v_{tank,j}(k) \quad ; \quad j = 1, \dots, 7 \tag{5.25}$$

Finally, the cost function for OCPC is given by (5.26), where the voltage applied to the resonant tank must be evaluated for each switching state according to table 5.1, and $\hat{\imath}_{tank}^{*}$ is the tank current magnitude reference. A scheme for OCPC approach is depicted in figure 5.6.

$$G_{OCPC,j} = \left(\hat{\imath}_{tank}^{*} - \hat{\imath}_{tank,j}^{p}\right)^2 \quad ; \quad j = 1, \dots, 7 \tag{5.26}$$

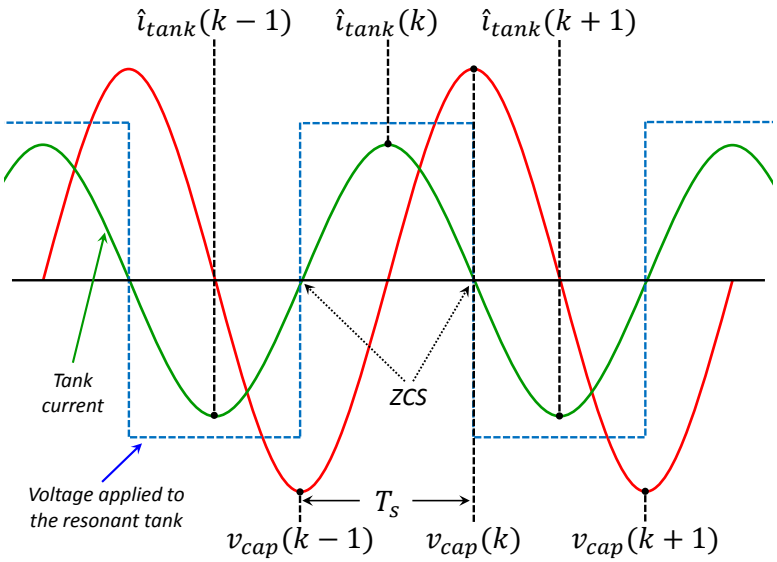


Fig. 5.5 Concept of OCPC strategy.

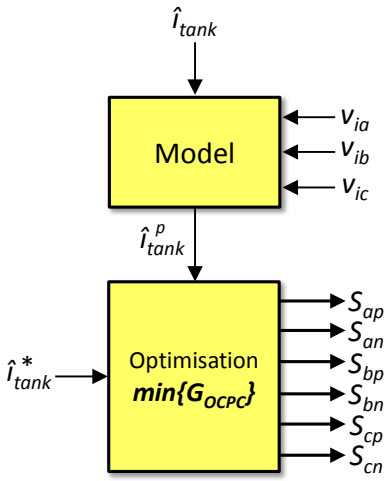


Fig. 5.6 Scheme of OCPC strategy.

5.3.1 Output current prediction as a function of Q

From (5.19)-(5.22), the coefficients E_{out22} and F_{out2} can be expressed as a function of the quality factor, which, for a series resonant tank, is defined by:

$$Q = \frac{Z_o^{out}}{R_{Load}} \tag{5.27}$$

By using (5.27), the damping factor (δ_{out}), the angle defined by the poles (ψ_{out}) and the natural frequency (ω_d^{out}) are given by:

$$\delta_{out}(Q) = \frac{R_{Load}}{2Z_o^{out}} = \frac{1}{2Q} \tag{5.28}$$

$$\psi_{out}(Q) = tan^{-1}\left(\frac{\sqrt{1-\delta_{out}^2}}{\delta_{out}}\right) = tan^{-1}\left(\sqrt{4Q^2-1}\right) \tag{5.29}$$

$$\omega_d^{out}(Q) = \omega_o^{out}\sqrt{1-\delta_{out}^2} = \omega_o^{out}\left(\frac{\sqrt{4Q^2-1}}{2Q}\right) \tag{5.30}$$

In addition, since the converter operates under ZCS, from (5.30), the sampling time can be defined by:

$$T_s(Q) = \frac{\pi}{\omega_d^{out}} = \frac{\pi}{\omega_o^{out}}\left(\frac{2Q}{\sqrt{4Q^2-1}}\right) \tag{5.31}$$

Therefore, using (5.28)-(5.31), equations (5.19) and (5.20) can be rewritten:

$$E_{out22}(Q) = -\frac{2Qe^{-\left(\frac{\pi}{\sqrt{4Q^2-1}}\right)}}{\sqrt{4Q^2-1}}sin\{\psi_{out}(Q)\} \tag{5.32}$$

$$F_{out2}(Q) = 1 - E_{out22}(Q) = 1 + \frac{2Qe^{-\left(\frac{\pi}{\sqrt{4Q^2-1}}\right)}}{\sqrt{4Q^2-1}}sin\{\psi_{out}(Q)\} \tag{5.33}$$

Thus, from (5.25), (5.32) and (5.33), the output current prediction is given by:

$$\hat{\imath}_{tank,j}^{p} = E_{out22}(Q)\hat{\imath}_{tank}(k) + \left(\frac{\sqrt{4Q^2-1}}{2QZ_o^{out}}F_{out2}(Q)\right)v_{tank,j}(k)\ ;\ j = 1,\dots,7 \tag{5.34}$$

5.4 Input-Output predictive control (IOPC)

In order to control the input and output currents, the previous control approaches can be combined. As a result, a new strategy denominated input-output predictive control (IOPC), which integrates ICPC with OCPC, can be defined. For this approach, from (5.15) and (5.26), a cost function can be defined by (5.35), where λ_i and λ_o are weighting factors, and $\hat{\imath}_{sn}$ and $\hat{\imath}_{on}$ are the nominal input current and the nominal output current, respectively.

$$G_{IOPC,j} = \frac{\lambda_i}{\hat{\imath}_{sn}^2}G_{ICPC,j} + \frac{\lambda_o}{\hat{\imath}_{on}^2}G_{OCPC,j}\ \ ;\ \ j = 1,\dots,7 \tag{5.35}$$

The weighting factors can be determined by considering a defined criterion for analysing the input and output responses. In order to simplify the adjustment process of the weighting factors, the input or output current control can be selected as the primary control, thus, the corresponding weighting factor can be defined as equal to

one. For instance, if the output current control is chosen as the primary control, then, from (5.35), the cost function is given by (5.36), and only λ_i needs to be determined.

$$G_{IOPC,j} = \frac{G_{OCPC,j}}{\hat{\imath}_{on}^2} + \lambda_i \frac{G_{ICPC,j}}{\hat{\imath}_{sn}^2} \quad ; \quad j = 1, \dots, 7 \tag{5.36}$$

5.4.1 Calculation of the input current reference

To achieve a correct correlation between the input and output control, the input current reference can be calculated by estimating the power losses. Assuming ZCS operation, the switching losses can be neglected in order to simplify the analysis. Thus, the power balance equation is given by (5.37), where P_{in} is the input power, P_{Load} is the power absorbed by the load, P_{matrix} corresponds to the matrix converter conduction losses, P_{tank} is the power dissipated in the resonant tank, and P_{filter} corresponds to the power dissipated in the input filter.

$$P_{in} = \underbrace{P_{Load}}_{Output\ power} + \underbrace{\left(P_{matrix} + P_{tank} + P_{filter}\right)}_{Power\ losses} \tag{5.37}$$

As shown in figure 5.1 and described in chapter 7, the matrix converter used in this work employs bidirectional power switches based on IGBTs, hence, to estimate the conduction losses of the matrix converter, the on-state voltage drop of the semiconductor devices can be calculated by (5.38) and (5.39), where V_{CE0}, R_{CE}, i_C, V_{F0}, R_F and i_F are the initial IGBT saturation voltage, the on-state IGBT resistance, the collector IGBT current, the initial forward diode voltage, the forward diode resistance and the forward diode current, respectively.

$$V_{on\_igbt} = R_{CE} i_C + V_{CE0} \tag{5.38}$$

$$V_{on\_diode} = R_F i_F + V_{F0} \tag{5.39}$$

Since the converter is switched at every zero crossing of the output current (i_{tank}), the current through each device corresponds to an entire half cycle of the output current. Therefore, the conduction power loss for every device is given by:

$$P_{cond_{igbt}} = \frac{1}{T_s} \int_0^{T_s} [R_{CE} i_C(t) + V_{CE0}] i_C(t)\, dt = \frac{R_{CE} \hat{\imath}_{tank}^2}{2} + \frac{2}{\pi} (V_{CE0} \hat{\imath}_{tank}) \tag{5.40}$$

$$P_{cond_{diode}} = \frac{1}{T_s} \int_0^{T_s} [R_F i_F(t) + V_{F0}] i_F(t)\, dt = \frac{R_F \hat{\imath}_{tank}^2}{2} + \frac{2}{\pi} (V_{F0} \hat{\imath}_{tank}) \tag{5.41}$$

Owing to the matrix converter utilises bidirectional switches, the output current circulates through two IGBTs and two diodes, thus, the conduction losses of the matrix converter corresponds to:

$$P_{matrix} = 2(P_{cond_{igbt}} + P_{cond_{diode}}) \tag{5.42}$$

With respect to the resonant tank, the power loss is mainly caused by the internal resistance of the tank inductor ($R_{L_{tank}}$). Thus, the tank power loss can be calculated by:

$$P_{tank} = \frac{R_{L_{tank}} \hat{\imath}_{tank}^2}{2} \tag{5.43}$$

The power loss in the input filter can be estimated by (5.44), considering the equivalent resistance at 50Hz (supply frequency) calculated by (5.45), where R_f, R_{L_f}, L_f and ω correspond to the parallel damping resistor, the internal resistance of the filter inductor, the filter inductance and the input angular frequency (supply angular frequency), respectively.

$$P_{filter} = \frac{3}{2} R_{eq} \hat{\imath}_s^2 \tag{5.44}$$

$$R_{eq} = \frac{R_f \left[R_{L_f} \left(R_f + R_{L_f} \right) + \left(\omega L_f \right)^2 \right]}{\left(R_f + R_{L_f} \right)^2 + \left(\omega L_f \right)^2} \tag{5.45}$$

Therefore, from the power balance equation (5.37), the following equation can be obtained:

$$P_{in} = P_{Load} + P_{Losses} \Rightarrow \underbrace{\frac{3}{2} \hat{v}_s \hat{\imath}_s}_{\substack{Input \\ power}} - \underbrace{\frac{3}{2} R_{eq} \hat{\imath}_s^2}_{\substack{Input\ filter \\ losses}} = P_{Load} + \underbrace{\Delta P}_{\substack{Converter\ losses \\ + \\ Tank\ losses}} \tag{5.46}$$

Finally, calculating the input current from (5.46) and considering (5.40)-(5.45) and the tank current reference, the magnitude for the input current reference can be determined by (5.47), where P_{Load} and ΔP are given by (5.48) and (5.49), respectively. However, since the input current reference is based on an approximation of the power losses, the output current control can have steady-state error. In order to improve the input current reference, a feedback approach could be implemented.

$$\hat{\imath}_s^* = \frac{\left(\frac{3}{2} \hat{v}_s \right) - \sqrt{\left(\frac{3}{2} \hat{v}_s \right)^2 - 6 R_{eq} (P_{Load} + \Delta P)}}{3 R_{eq}} \tag{5.47}$$

$$\Delta P = \underbrace{2\left\{\left[\frac{R_{CE}}{2}(\hat{\imath}^*_{tank})^2 + \frac{2}{\pi}(V_{CE0}\hat{\imath}^*_{tank})\right] + \left[\frac{R_F}{2}(\hat{\imath}^*_{tank})^2 + \frac{2}{\pi}(V_{F0}\hat{\imath}^*_{tank})\right]\right\}}_{Matrix\ converter} + \cdots$$

$$\cdots + \underbrace{\frac{R_{L_{tank}}(\hat{\imath}^*_{tank})^2}{2}}_{Tank\ inductor} \quad (5.48)$$

$$P_{Load} = \frac{R_{Load}(\hat{\imath}^*_{tank})^2}{2} \quad (5.49)$$

5.5 Delay compensation

To compensate the delay associated with the digital implementation, the error between the reference and the predicted value at t_{k+2} is considered, as discussed in chapter 3. Thus, the predictive algorithms minimise the error at t_{k+2} and apply the optimum switching state at t_{k+1}. Hence, the cost functions for ICPC and OCPC are redefined and given by:

$$G_{ICPC,j} = \left(i^*_{sa} - i^{k+2}_{sa,j}\right)^2 + \left(i^*_{sb} - i^{k+2}_{sb,j}\right)^2 \;\; ; \;\; j = 1, \dots, 7 \quad (5.50)$$

$$G_{OCPC,j} = \left(\hat{\imath}^*_{tank} - \hat{\imath}^{k+2}_{tank,j}\right)^2 \;\; ; \;\; j = 1, \dots, 7 \quad (5.51)$$

For ICPC, from (5.14), the prediction of the supply current per phase at t_{k+2} can be calculated by:

$$i^{k+2}_{s,j} = H_1 i_s(k+1) + H_2 v_i(k+1) + H_3 v_s(k+1) + \frac{1}{R_f} v_s(k+2) + \cdots$$

$$\cdots + H_4 K_{i,j} \frac{2}{\pi} \hat{\imath}_{tank}(k+1) \;\; ; \;\; j = 1, \dots, 7 \quad (5.52)$$

It can be seen that prediction (5.52) includes the value at t_{k+1} of the supply current, the supply voltage, the input capacitor voltage and the tank current magnitude as well as the value at t_{k+2} of the supply voltage. From equations (5.4), (5.5), (5.12) and (5.24), the future values of the supply current per phase, the input capacitor voltage per phase and the magnitude of the tank current can be determined by (5.53)-(5.55) when considering the optimum switching state applied at t_k (result of the previous optimisation, see chapter 3).

$$i_s(k+1) = H_1 i_s(k) + H_2 v_i(k) + H_3 v_s(k) + \frac{1}{R_f} v_s(k+1) + \cdots$$

$$\cdots + H_4 K_{i,opt} \frac{2}{\pi} \hat{\imath}_{tank}(k) \quad (5.53)$$

$$v_i(k+1) = E_{in21} i_s(k) + H_5 v_i(k) + H_6 v_s(k) + F_{in21} K_{i,opt} \frac{2}{\pi} \hat{\imath}_{tank}(k) \quad (5.54)$$

$$\hat{\imath}_{tank}(k+1) = E_{out22} \hat{\imath}_{tank}(k) + (\omega_d^{out} C_{tank} F_{out2}) v_{tank,opt}(k) \quad (5.55)$$

The future values of the supply voltage can be estimated by using (5.13), where $n = 2$ is sufficient to estimate the values of a sinusoidal function accurately [16]. Thus, the supply voltage at t_{k+1} and t_{k+2} can be calculated by:

$$v_s(k+1) = 3v_s(k) - 3v_s(k-1) + v_s(k-2) \quad (5.56)$$

$$v_s(k+2) = 6v_s(k) - 8v_s(k-1) + 3v_s(k-2) \quad (5.57)$$

For OCPC approach, the prediction equation for the tank current magnitude at t_{k+2} is given by (5.58), where $\hat{\imath}_{tank}(k+1)$ is calculated by (5.55).

$$\hat{\imath}_{tank,j}^{k+2} = E_{out22} \hat{\imath}_{tank}(k+1) + (\omega_d^{out} C_{tank} F_{out2}) v_{tank,j}(k+1) \; ; \; j = 1, \ldots, 7 \quad (5.58)$$

5.6 Simulation results

Simulations for ICPC, OCPC and IOPC strategies were carried out in MATLAB/Simulink. The parameters employed, table 5.2, are based on the experimental system implemented in this work, which is detailed in a later chapter.

Table 5.2 Simulation parameters for ICPC, OCPC and IOPC.

Supply		$\hat{v}_s$	170V
		f	50Hz
		P_{in}	2.1kW
Input filter		L_f	1.75mH
		C_f	14μF
		R_f	50Ω
Resonant tank		L_{tank}	929.6μH
		$R_{L_{tank}}$	0.578Ω
		C_{tank}	72.54nF
		f_o	19.3kHz
		Q	5.78
Load		R_{Load}	19Ω
Matrix Converter	IGBTs	V_{CE0}/R_{CE}	1.2V/26mΩ
	Diodes	V_{F0}/R_F	1.0V/16mΩ

The simulation results shown in this section include the delay compensation approach and the input current reference calculation. For IOPC strategy, results with different values of weighting factors are depicted. In addition, the magnitude of the load current (tank current) is obtained by using the filtering approach experimentally implemented (detailed in chapter 7).

5.6.1 Simulation results for ICPC

Simulation results for ICPC strategy considering an output current of $10A_{rms}$ are shown in figures 5.7-5.12. The input current reference value is $5.66A_{rms}$. As expected, the ICPC approach achieve sinusoidal input currents, however, considerable distortion is produced at the output as seen in figure 5.7

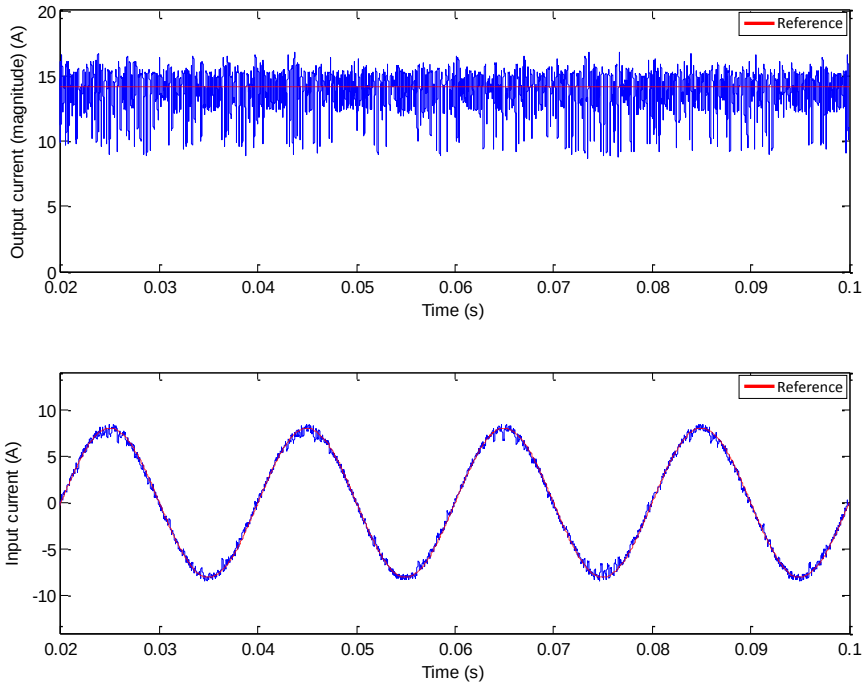


Fig. 5.7 Simulation results for ICPC strategy: output current magnitude and input current control.

In figure 5.8, input power factor and ZCS operation can be seen. The input converter current (unfiltered current) and the input current are depicted in figure 5.9. This figure also includes the frequency spectrum of both currents, whereas figure 5.10 shows the frequency spectrum of the input current in more detail in order to observe the low order harmonics.

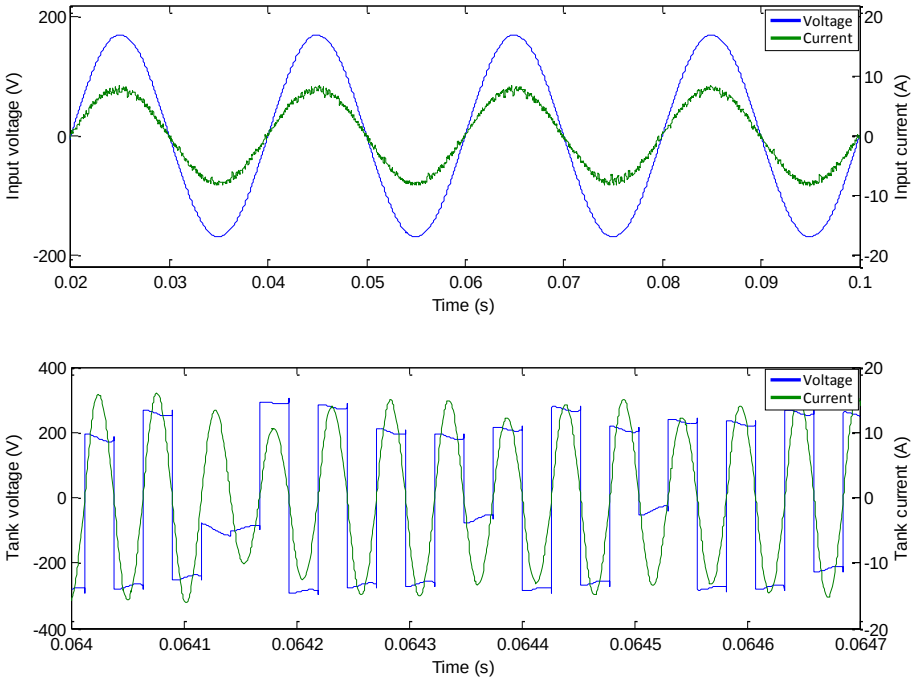


Fig. 5.8 Simulation results for ICPC strategy: input voltage/current, voltage applied to the resonant tank and output current.

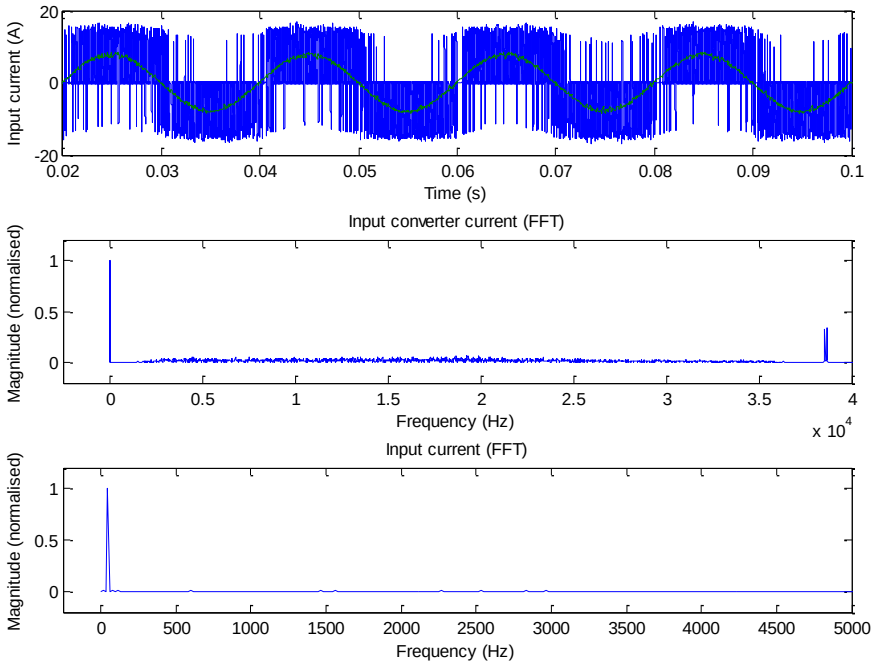


Fig. 5.9 Simulation results for ICPC strategy: input converter current, FFT of the input converter current and FFT of the input current.

Figure 5.10 shows the frequency spectrum of the input current to observe the low order harmonics. The distortion generated at the output due to the input current control can be seen in figure 5.11, where the tank current and the voltage applied to the resonant tank are shown. In order to mitigate the effects of the ICPC strategy on

the output current (oscillations of the tank current), a higher quality factor can be utilised, nevertheless, this results in a significant increase of the voltage requirements of the resonant tank components.

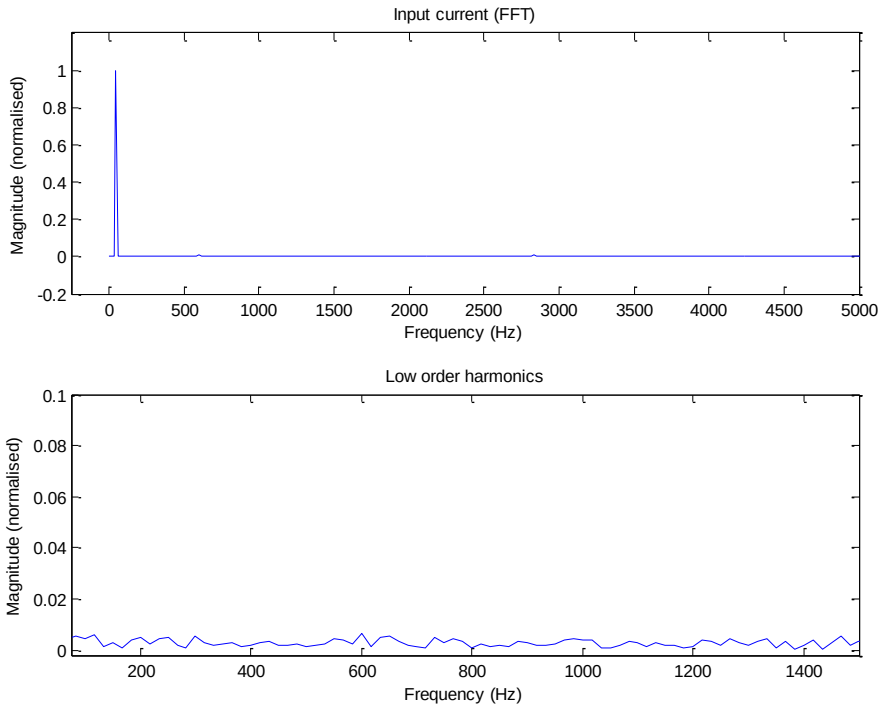


Fig. 5.10 Simulation results for ICPC strategy: FFT of the input current (low order harmonics).

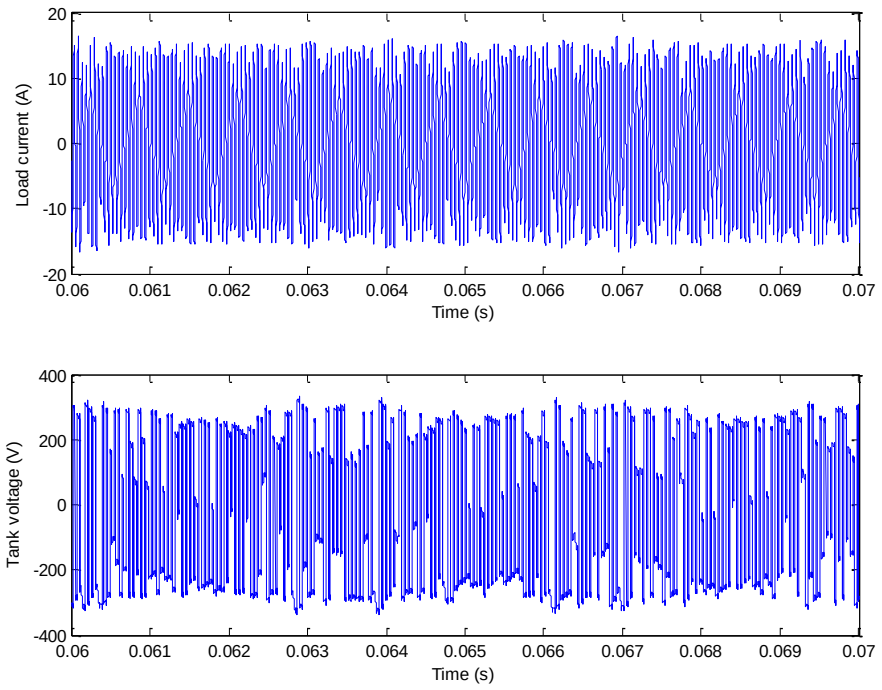


Fig. 5.11 Simulation results for ICPC strategy: output current and voltage applied to the resonant tank.

Figure 5.12 shows the supply voltage, the input filter capacitor voltage (input converter voltage) and the supply current (input current).

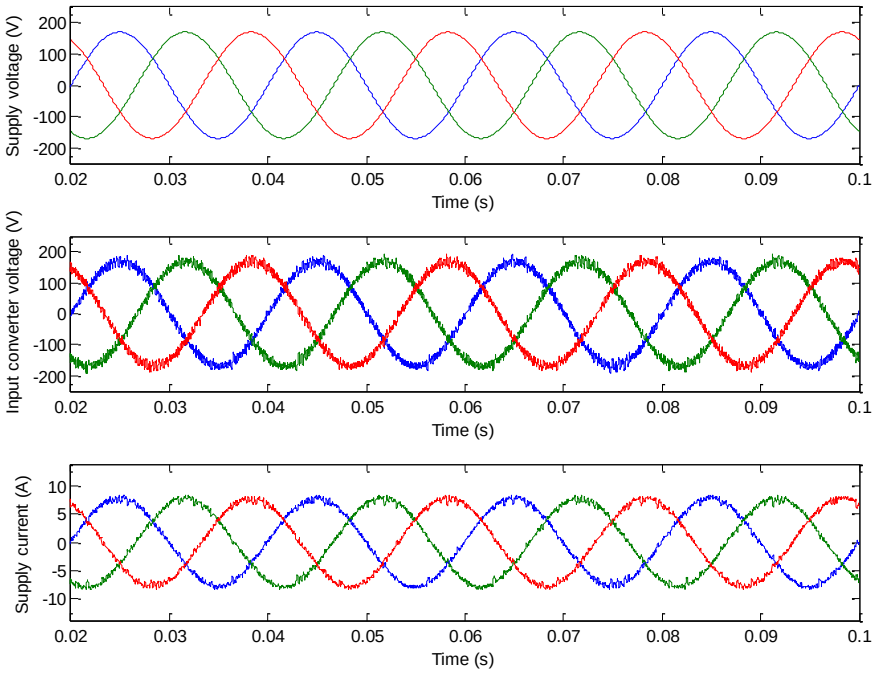


Fig. 5.12 Simulation results for ICPC strategy: input voltage, input converter voltage and input current.

Figures 5.13 and 5.14 depict waveforms for ICPC with a reference of $8A_{rms}$ (output current $12A_{rms}$) which is equivalent to a converter voltage ratio of $M_v \approx 0.89$. The effect of overmodulation on the input and output currents can clearly be observed.

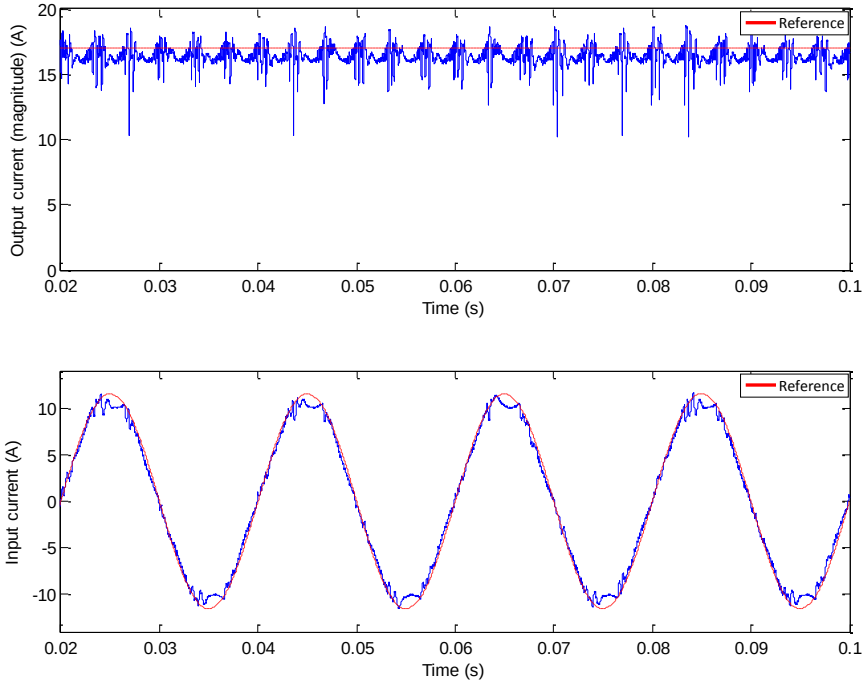


Fig. 5.13 Simulation results for ICPC strategy: output current magnitude and input current control for a reference value above the limit $\boldsymbol{M_v = \frac{\sqrt{3}}{2}}$.

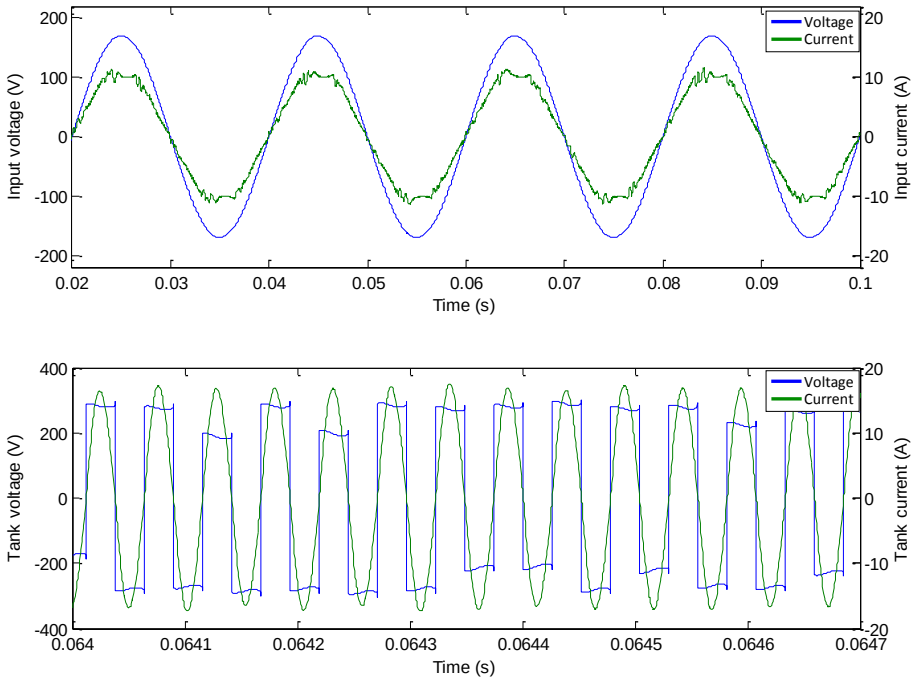


Fig. 5.14 Simulation results for ICPC strategy: input voltage/current, voltage applied to the resonant tank and output current for a reference value above the limit $\boldsymbol{M_v = \frac{\sqrt{3}}{2}}$.

5.6.2 Simulation results for OCPC

The main issue for the OCPC strategy is the input filtering. Since the output current is regulated, the input current can become highly distorted, which leads to a distorted input converter voltage as well. This effect on the input side directly affects the output waveforms as shown in figures 5.15-5.18, where the output current reference corresponds to the optimum value (≈11.6A_{rms}), i.e. $M_v = \frac{\sqrt{3}}{2}$. In order to overcome the high distortion of the input converter voltage, the input filter can be modified, reducing the parallel damping resistor (R_f), however, this entails an increase of the power loss in the input filter.

Waveforms for a damping resistor equal to 5Ω and an optimum output current reference, as in figures 5.15-5.18, are depicted in figures 5.19-5.23. Results for a load current reference below the optimum value, output current reference equal to 10A_{rms}, and a damping resistor of 5Ω are shown in figures 5.24-5.25. In figures 5.16 and 5.20, it can be observed that the unity displacement power factor is an intrinsic characteristic of the OCPC approach.

Figures 5.15 and 5.16 show the input and output currents for a damping resistor of 50Ω and a converter voltage ratio equal to $\frac{\sqrt{3}}{2}$.

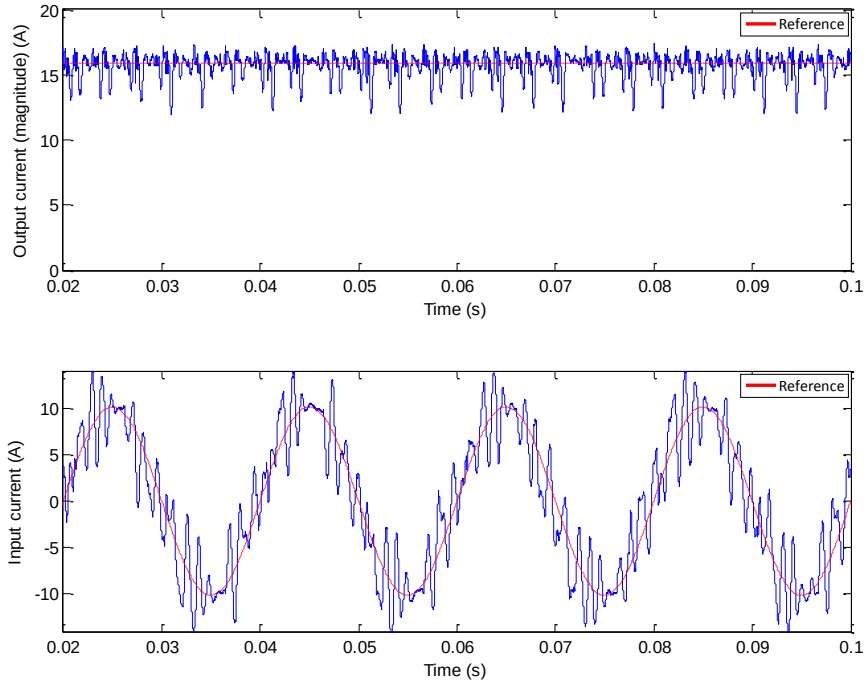


Fig. 5.15 Simulation results for OCPC strategy: output current magnitude control and input current ($\boldsymbol{R_f}$=50Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

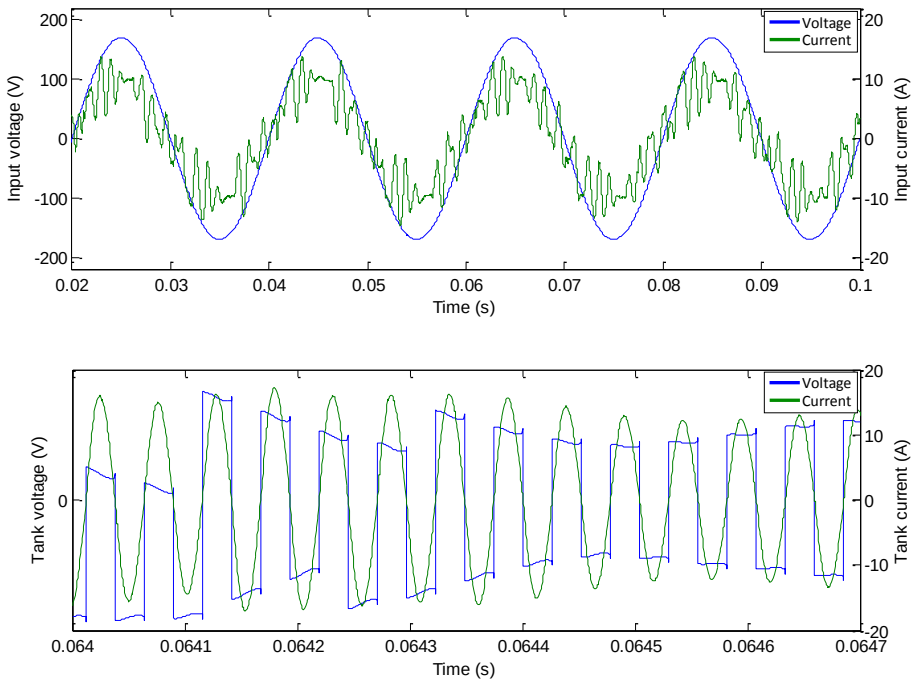


Fig. 5.16 Simulation results for OCPC strategy: input voltage/current, voltage applied to the resonant tank and output current ($\boldsymbol{R_f}$=50Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

Figure 5.17 depicts the output current and the voltage applied to the resonant tank (R_f=50Ω and $M_v = \frac{\sqrt{3}}{2}$), whereas figure 5.18 shows the supply voltage, the input filter capacitor voltage (input converter voltage) and supply current (input current).

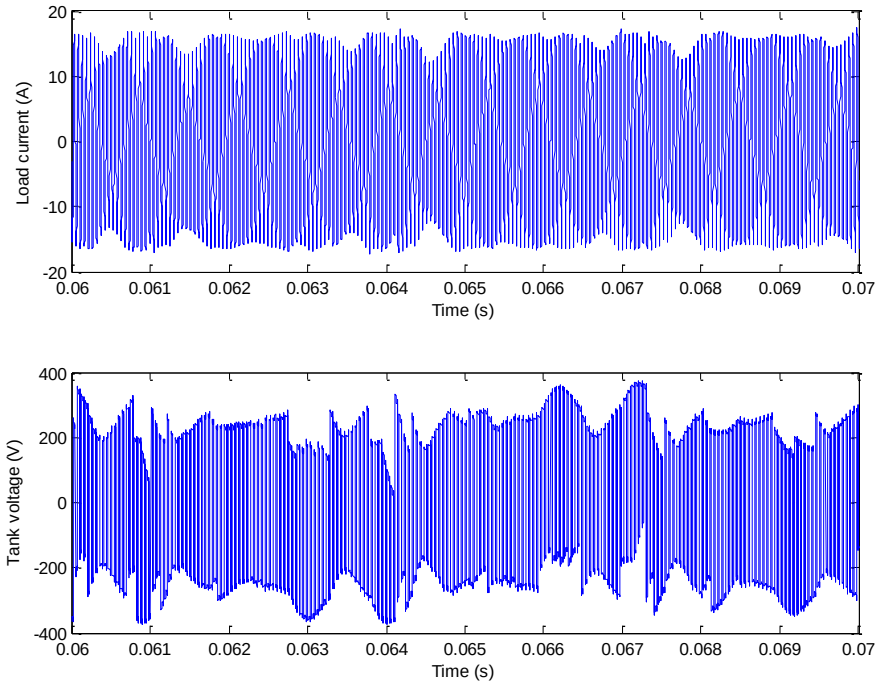


Fig. 5.17 Simulation results for OCPC strategy: output current and voltage applied to the resonant tank ($\boldsymbol{R_f}$=50Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

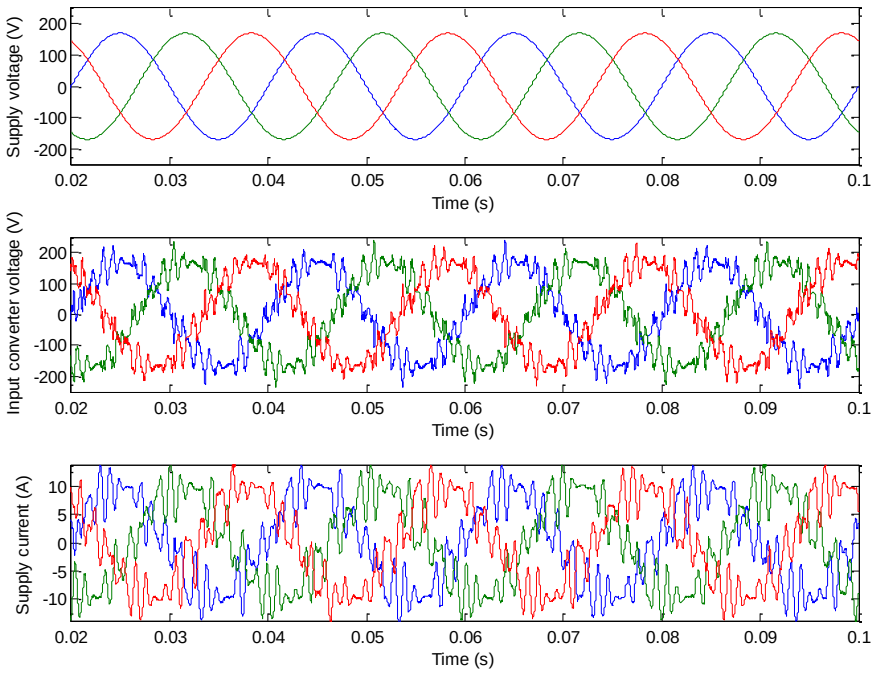


Fig. 5.18 Simulation results for OCPC strategy: input voltage, input converter voltage and input current ($\boldsymbol{R_f}$=50Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

The input and output currents for a damping resistor of 5Ω are shown in figures 5.19 and 5.20.

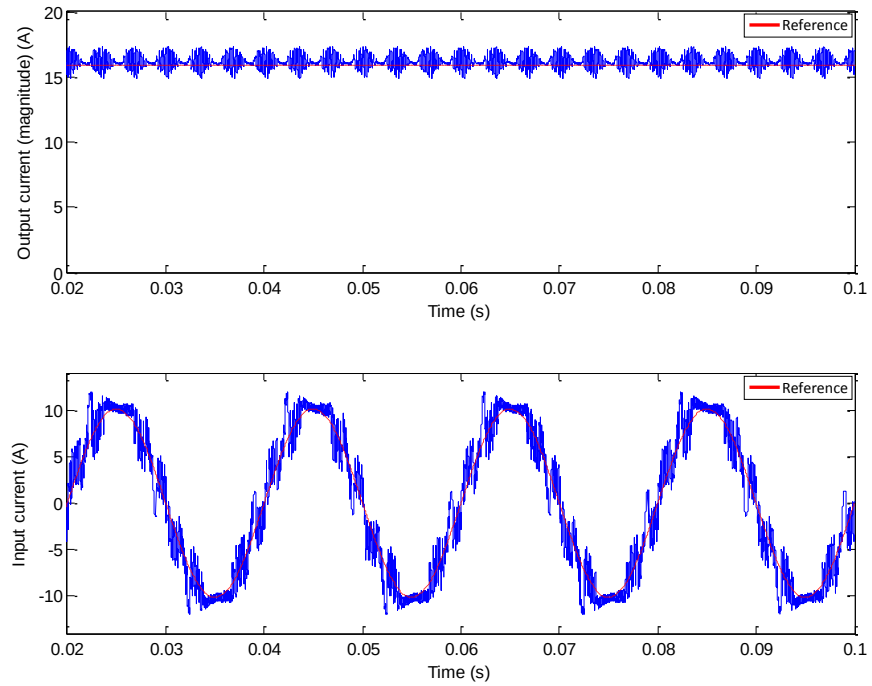


Fig. 5.19 Simulation results for OCPC strategy: output current magnitude control and input current ($\boldsymbol{R_f}$=5Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

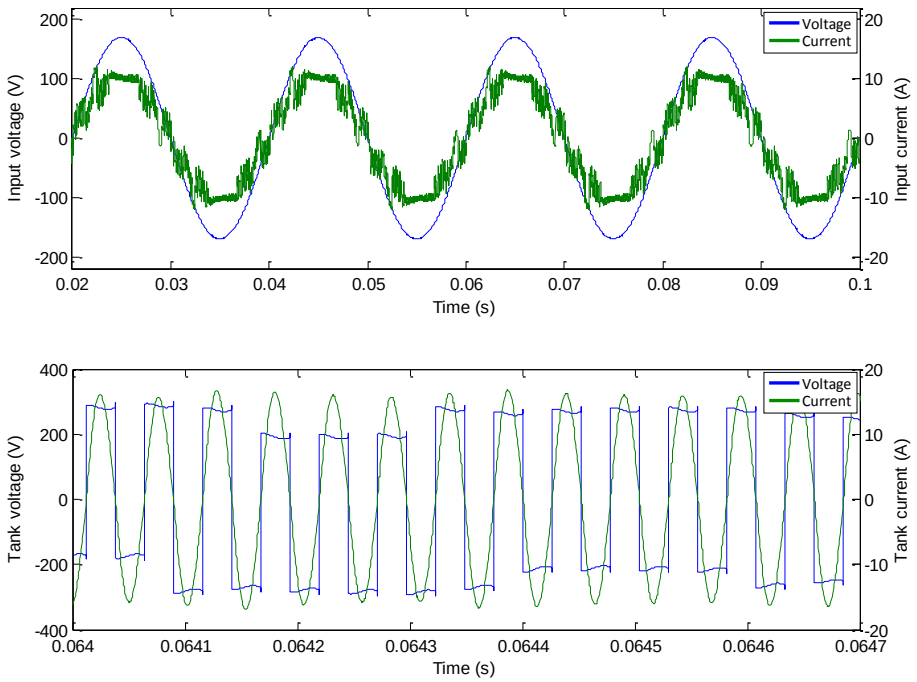


Fig. 5.20 Simulation results for OCPC strategy: input voltage/current, voltage applied to the resonant tank and output current ($\boldsymbol{R_f}$=5Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

In figure 5.21, the frequency spectrum of the input current is shown in order to observe the harmonic content. Figure 5.22 shows the output current and the voltage applied to the resonant tank.

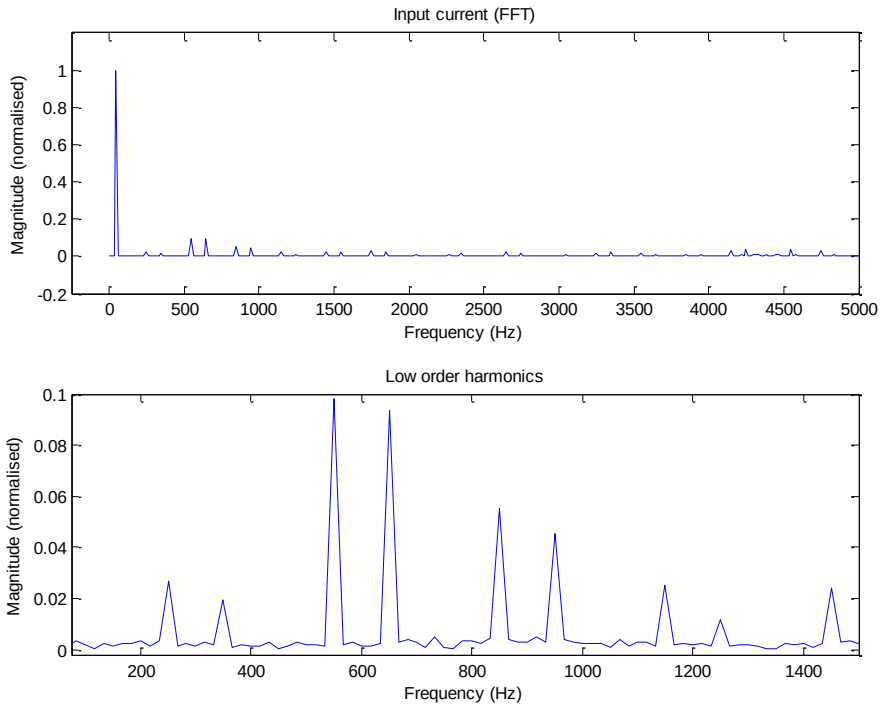


Fig. 5.21 Simulation results for OCPC strategy: FFT of the input current (low order harmonics) ($\boldsymbol{R_f}$=5Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

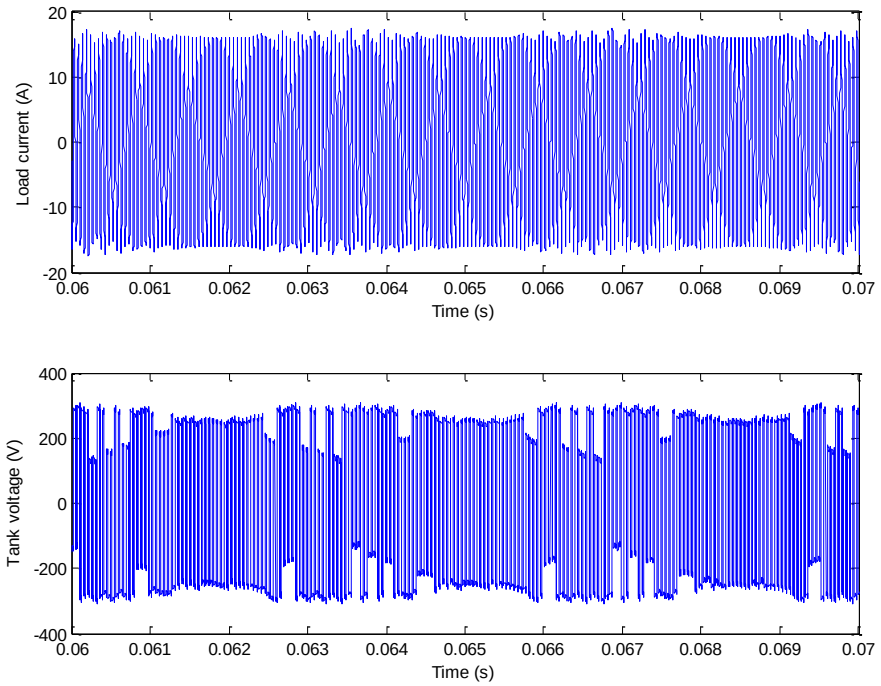


Fig. 5.22 Simulation results for OCPC strategy: output current and voltage applied to the resonant tank ($\boldsymbol{R_f}$=5Ω, $\boldsymbol{M_v} = \frac{\sqrt{3}}{2}$).

Figure 5.23 shows the supply voltage, the input converter voltage and input current (R_f=5Ω and $M_v = \frac{\sqrt{3}}{2}$). In figures 5.24, the output current magnitude and the input current for a reference below the optimum value are depicted (R_f=5Ω). The frequency spectrum of the input current in figure 5.24 is shown in figure 5.25.

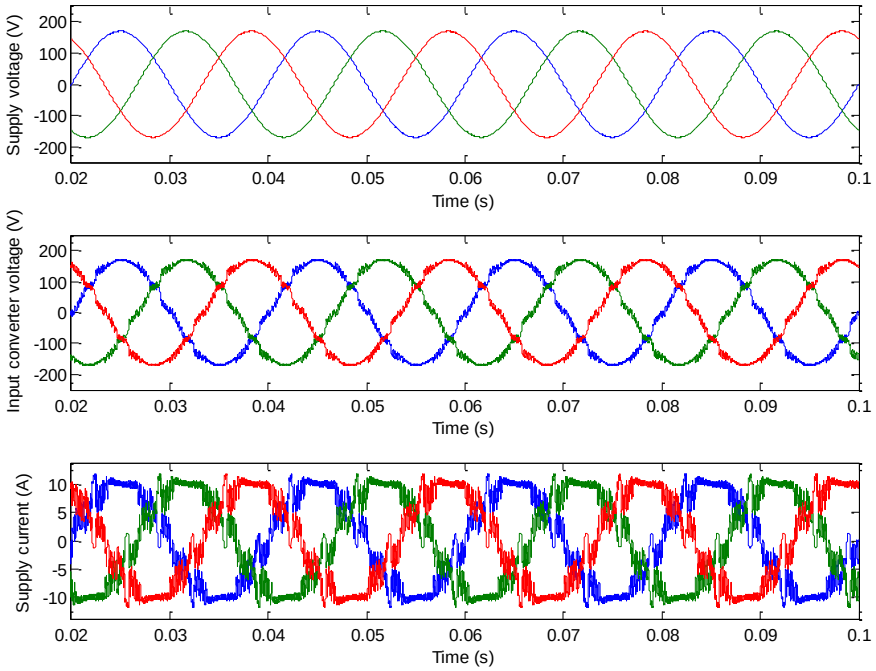


Fig. 5.23 Simulation results for OCPC strategy: input voltage, input converter voltage and input current ($\boldsymbol{R_f}$=5Ω, $\boldsymbol{M_v = \frac{\sqrt{3}}{2}}$).

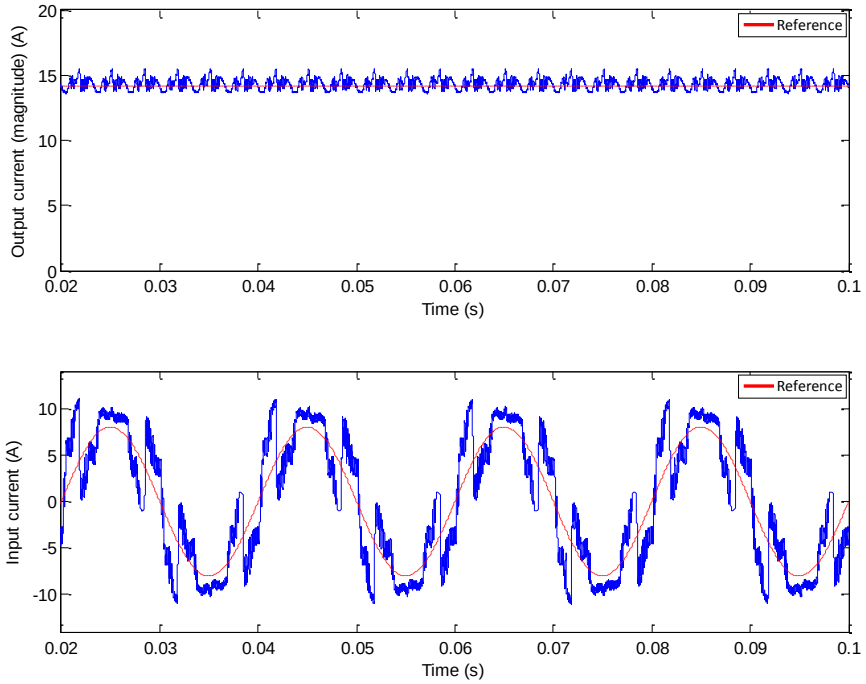


Fig. 5.24 Simulation results for OCPC strategy: output current magnitude control and input current for a reference below the optimum value ($\boldsymbol{R_f}$=5Ω).

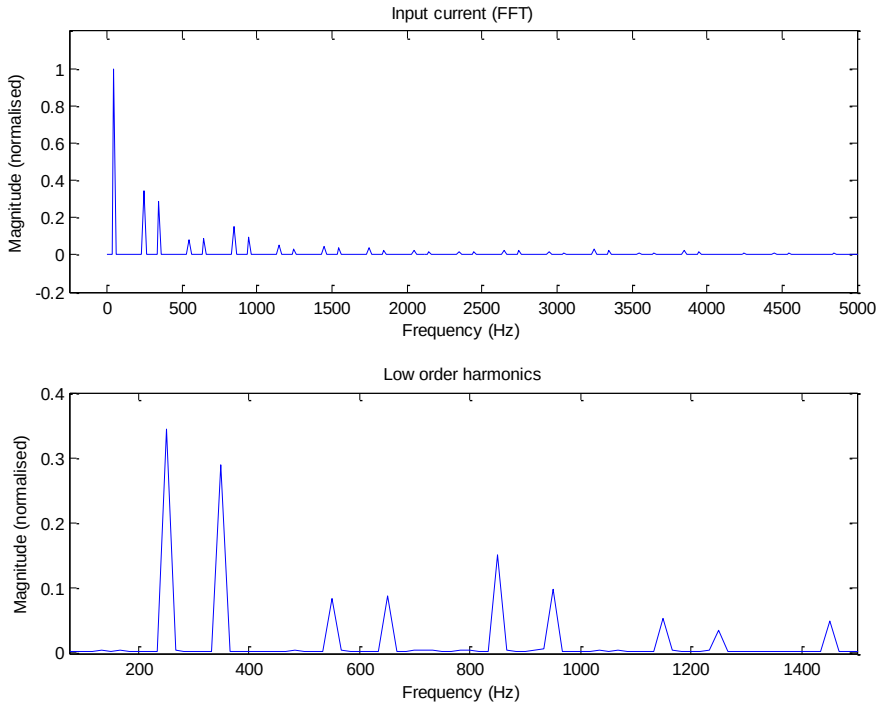


Fig. 5.25 Simulation results for OCPC strategy: FFT of the input current (low order harmonics) for a reference below the optimum value ($\boldsymbol{R_f}$=5Ω).

5.6.3 Simulation results for IOPC

Results for IOPC strategy considering different values of weighting factors are shown. The damping resistor of the input filter corresponds to 50Ω. These results can be divided into two parts. First, the output current control is selected as the primary control, with λ_i=0.25. Figure 5.26 depicts waveforms for IOPC for an output reference of approximately 11.6A_{rms}, which corresponds to the optimum value given by $M_v = \frac{\sqrt{3}}{2}$. In figure 5.27, the output current reference is 10A_{rms}.

In figure 5.26, it can be seen the input control reduces the distortion at the input in comparison with figure 5.15 (OCPC). Nonetheless, when the output current reference is a value below the optimal operating point, as shown in figure 5.27, the distortion at the input side becomes significantly high.

Figures 5.28 and 5.29 show the results for IOPC with input current control as the main control, i.e. λ_i=1.0 and λ_o=0.25, for an output current reference equal to and below the output optimal operation point, respectively. As seen in these figures, although the input control is improved, the oscillation of the output current (ripple of the output current magnitude) is increased.

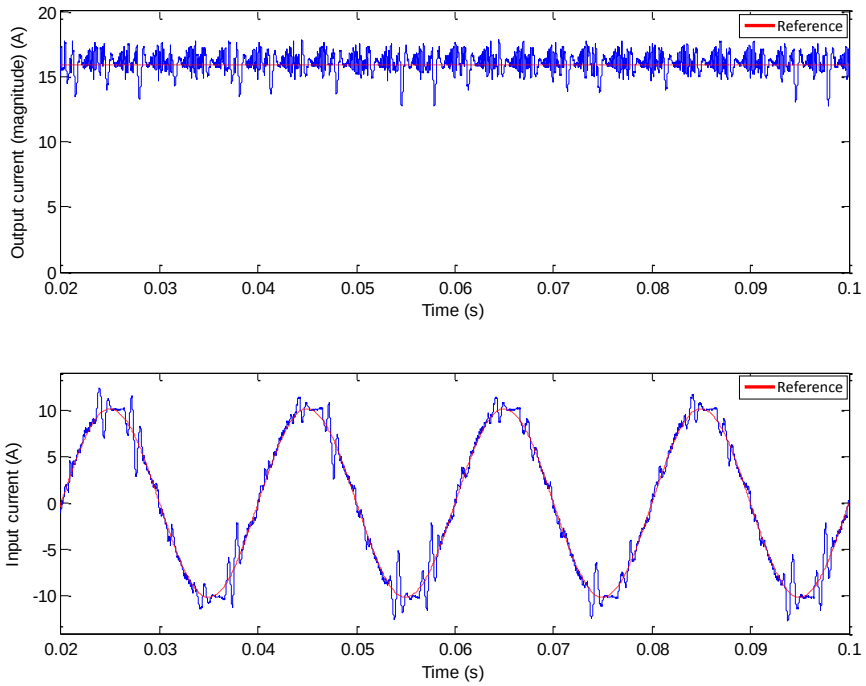


Fig. 5.26 Simulation results for IOPC strategy ($\boldsymbol{\lambda_i = 0.25}$, $\boldsymbol{\lambda_o = 1.0}$, $\boldsymbol{M_v = \frac{\sqrt{3}}{2}}$): output and input control.

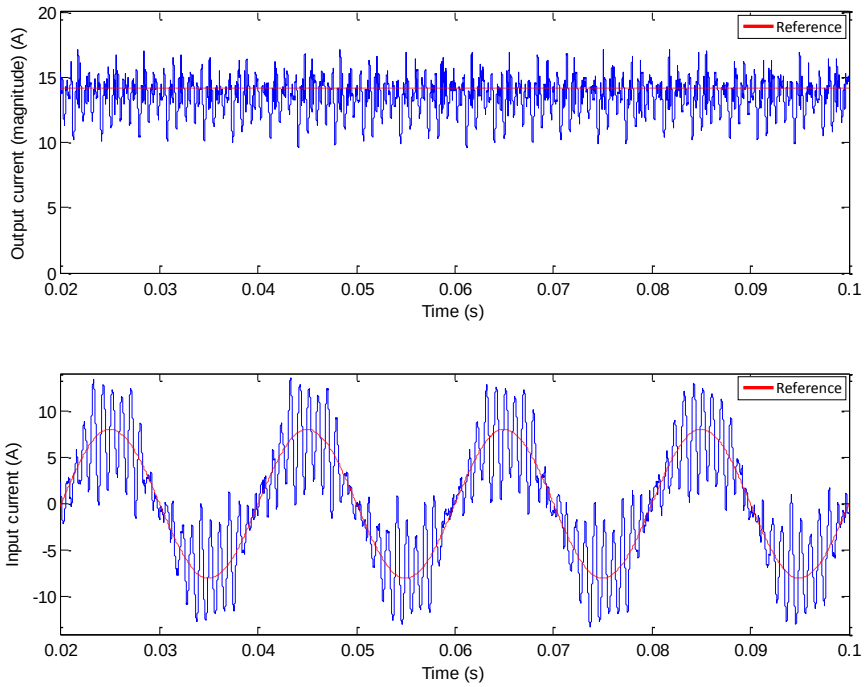


Fig. 5.27 Simulation results for IOPC strategy ($\boldsymbol{\lambda_i = 0.25}$, $\boldsymbol{\lambda_o = 1.0}$, $\boldsymbol{M_v < \frac{\sqrt{3}}{2}}$): output and input control.

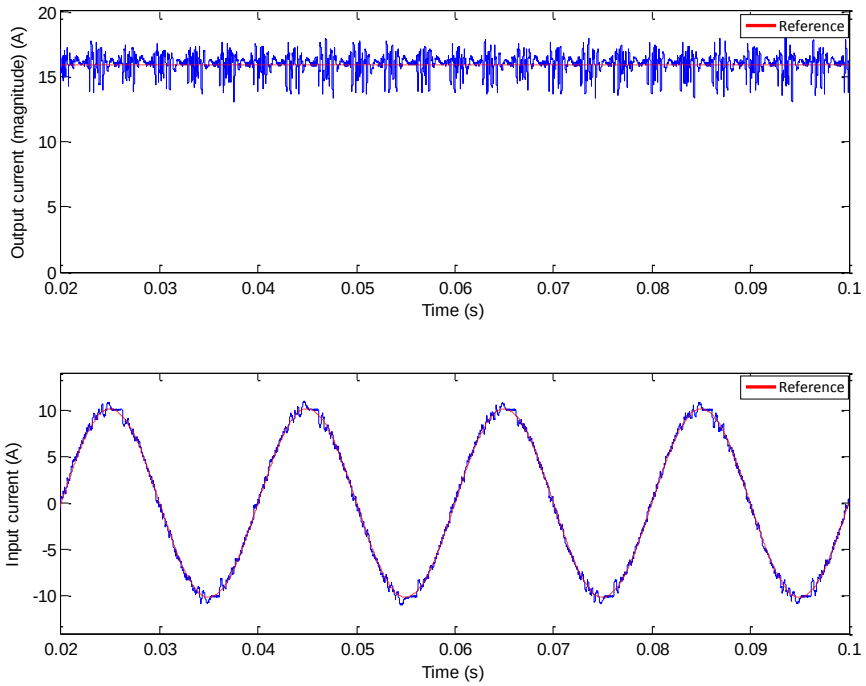


Fig. 5.28 Simulation results for IOPC strategy ($\boldsymbol{\lambda_i = 1.0}$, $\boldsymbol{\lambda_o = 0.25}$, $\boldsymbol{M_v = \frac{\sqrt{3}}{2}}$): output and input control.

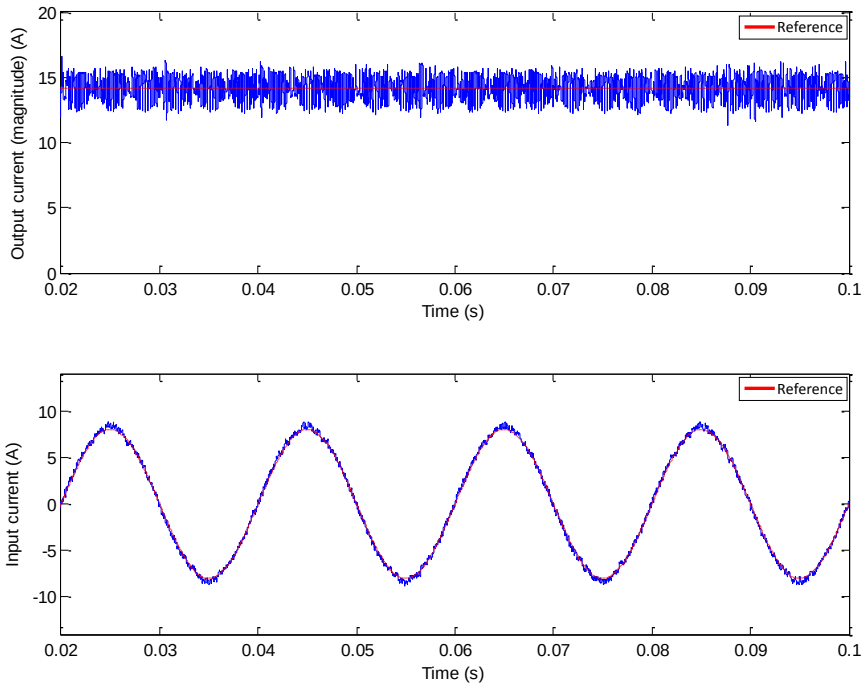


Fig. 5.29 Simulation results for IOPC strategy ($\boldsymbol{\lambda_i = 1.0}$, $\boldsymbol{\lambda_o = 0.25}$, $\boldsymbol{M_v < \frac{\sqrt{3}}{2}}$): output and input control.

Since the optimal operating point for OCPC corresponds to the limit operating condition for ICPC, as previously discussed in chapter 4, both approaches are

practically mutually exclusive, and, as a result, the combination of both strategies leads to a suboptimal control.

Consequently, to improve IOPC, a strategy for mitigating the effect of controlling the output current on the input current and vice versa must be considered. Hence, in this work, a modification to the converter structure to compensate the output converter voltage (voltage applied to the resonant tank) is proposed. This new compensation approach, which combines IOPC strategy with output voltage compensation, is presented in the next chapter.

5.7 Summary

New ZCS predictive control strategies for a DSRC developed during this work, ICPC and OCPC, have been presented in this chapter. The ICPC approach controls the input current, achieving sinusoidal current and unity power factor, whereas OCPC regulates the magnitude of the high frequency output current. As observed in the simulation results, significant distortion can be generated when only input or output current is controlled.

In order to have input and output control, a new strategy (IOPC) which integrates both control approaches was investigated. However, owing to the characteristics of ICPC and OCPC, IOPC cannot accomplish a satisfactory control. Hence, to enhance the control of the DSRC, a modification to the converter is proposed, which will be discussed in the next chapter.

Predictive control strategies depend on the model of the system (parameters) and the measurements, therefore, the behaviour of the control approaches can be affected by errors in the model parameters and/or measurement noise. In the next chapter, the effect of model parameter errors is evaluated. However, the effect of measurement noise and a stability analysis are considered beyond of the scope of this work.

Chapter 6

Direct Series Resonant Converter with Output Voltage Compensation

6.1 Introduction

As discussed in chapter 5, since the optimal operation conditions for ICPC and OCPC are different, the combination of both strategies (IOPC) leads to a suboptimal control, resulting in distortion of the input and output current. Thus, in order to overcome the issues of controlling both sides, a method for modifying the voltage applied to the resonant tank is proposed in this chapter. The purpose of this approach is to improve the voltage applied to the resonant tank, reducing the voltage variation produced when IOPC is implemented. Figure 6.1 summarises the effects of the ICPC and OCPC approaches.

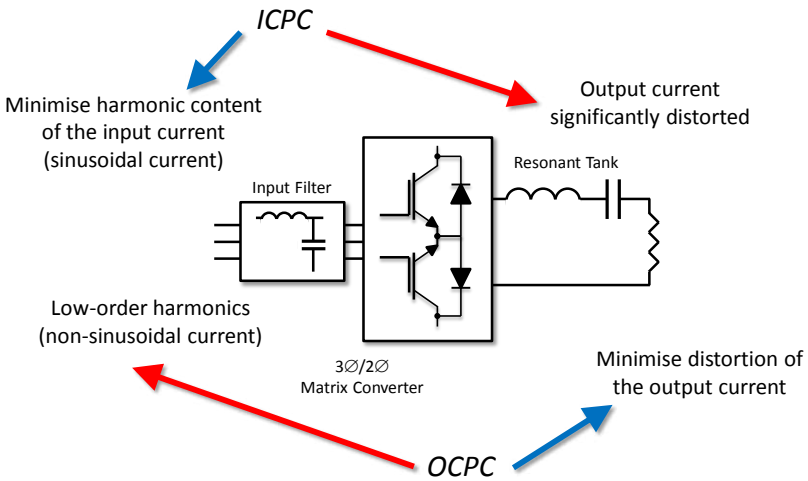


Fig. 6.1 Effects of the ICPC and OCPC strategies.

The implementation of the output voltage compensator considers the following objectives:

- Provide different voltage values.
- ZCS operation (reduce the effect on the converter efficiency).
- Reduced size of the reactive components.

6.2 Concept of the output voltage compensation

The voltage compensation consists of a modification to the output converter voltage by connecting an extra voltage source in series with the resonant tank. This additional voltage source must be capable of providing different voltages in order to mitigate the variation of the output converter voltage and, as a result, decrease the distortion of the load current. Figure 6.2 shows the principle of this voltage compensation method, where v_{matrix} and v_{comp} are the output converter voltage and the compensation voltage, respectively.

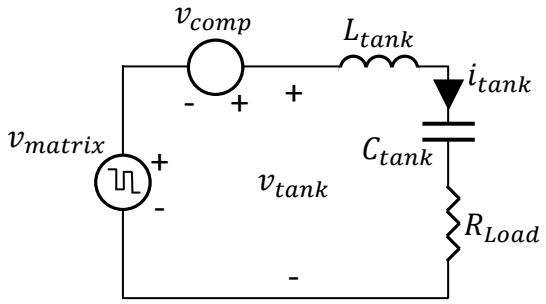


Fig. 6.2 Concept of the output voltage compensation.

The dynamic equation for the circuit depicted in figure 6.2 is:

$$v_{tank}(t) = L_{tank}\frac{d}{dt}i_{tank}(t) + \frac{1}{C_{tank}}\int_0^t i_{tank}(\tau)d\tau + R_{Load}i_{tank}(t) \tag{6.1}$$

In (6.1), the voltage applied to the resonant tank is given by:

$$v_{tank}(t) = v_{matrix}(t) + v_{comp}(t) \tag{6.2}$$

6.3 Implementation of the output voltage compensator

Since the voltage compensator needs to supply a variable voltage, the use of an H-bridge converter is suitable for this purpose. In [27-30], an H-bridge converter has been employed for improving the voltage ratio of an indirect matrix converter. Thus,

as in [27-30], the voltage compensator in this work is implemented by using an H-bridge converter which is not externally supplied. In figure 6.3, a scheme of the DSRC with voltage compensator is depicted.

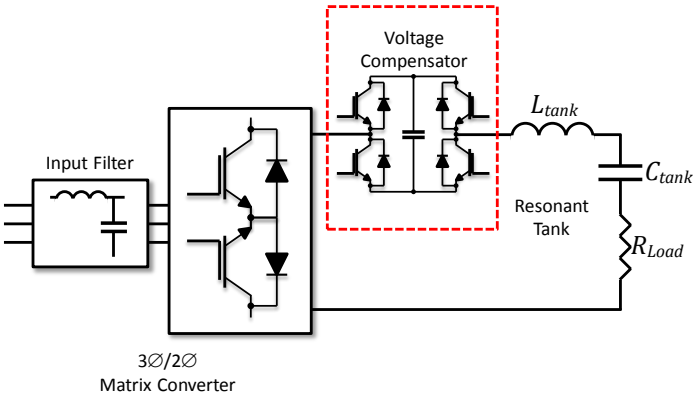


Fig. 6.3 Scheme of the DSRC with output voltage compensator.

The compensator can provide three different voltages, as shown in figure 6.4. The compensation voltage is defined by the capacitor voltage which, owing to the compensator is placed in series between the converter and the resonant tank, depends on the output current (load current).

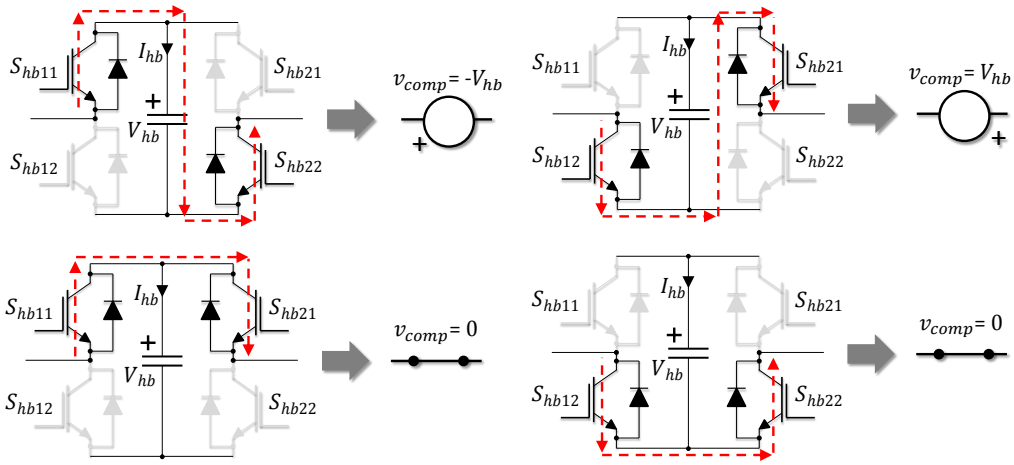


Fig. 6.4 Operation of the voltage compensator.

From figure 6.4, the switching states for the voltage compensator are given in table 6.1. Furthermore, the compensator switching model is defined by (6.3) and (6.4), where S_{hb11}, S_{hb12}, S_{hb21} and S_{hb22} are the switching functions for each switch.

$$v_{comp}(t) = -\frac{1}{2}\{[S_{hb11}(t) - S_{hb12}(t)] - [S_{hb21}(t) - S_{hb22}(t)]\}V_{hb}(t) \tag{6.3}$$

$$I_{hb}(t) = \frac{1}{2}\{[S_{hb11}(t) - S_{hb12}(t)] - [S_{hb21}(t) - S_{hb22}(t)]\}i_{tank}(t) \tag{6.4}$$

Table 6.1 Switching states for the voltage compensator.

Switches ON		n	$K_{hb,n}$	$v_{comp,n}$	$I_{hb,n}$
S_{hb11}	S_{hb22}	1	1	$-V_{hb}$	i_{tank}
S_{hb12}	S_{hb21}	2	-1	V_{hb}	$-i_{tank}$
S_{hb11}	S_{hb21}	3	0	0	0
S_{hb12}	S_{hb22}				

6.4 Predictive control of the compensator capacitor voltage

In order to avoid reducing the efficiency of the system considerably, the voltage compensator switching is synchronised with the switching of the main converter (ZCS). The switching of the voltage compensator allows regulation of the dc capacitor voltage and, also, compensation of the output converter voltage.

This predictive strategy regulates the capacitor voltage by minimising the future voltage error. The future value of the dc voltage prediction equation is obtained from the dynamic equation of the compensator capacitor voltage:

$$C_{hb}\frac{d}{dt}V_{hb}(t) = I_{hb}(t) \Rightarrow V_{hb}(k+1) = V_{hb}(k) + \frac{1}{C_{hb}}\int_{kT_s}^{(k+1)T_s} I_{hb}(t)dt \qquad (6.5)$$

The integral of the current through the capacitor (I_{hb}) is given by (6.6), where K_{hb} is defined by each switching state in table 6.1.

$$\int_{kT_s}^{(k+1)T_s} I_{hb}(t)dt = K_{hb}T_s\frac{2}{\pi}\hat{\imath}_{tank}(k) \qquad (6.6)$$

Therefore, from (6.5) and (6.6), the prediction of the compensator capacitor voltage is calculated by:

$$V_{hb,n}^{p} = V_{hb}(k) + K_{hb,n}\frac{T_s}{C_{hb}}\frac{2}{\pi}\hat{\imath}_{tank}(k) \quad ; \quad n = 1,2,3 \qquad (6.7)$$

Then, the cost function is defined by:

$$G_{hb,n} = \left(V_{hb}^{*} - V_{hb,n}^{p}\right)^2 \quad ; \quad n = 1,2,3 \qquad (6.8)$$

6.5 Control of a DSRC with output voltage compensation

The control of the converter with compensation of the output voltage is carried out by using input-output predictive control. When the compensation is included in this

control strategy, only the output current control is affected, since the H-bridge compensator increases the available output voltage levels from 7 to 21 different values. In other words, 21 switching states, which are the result of combining the switching states of the matrix converter and the H-bridge compensator, i.e. 7×3=21, can be considered for controlling the output current. However, the zero switching states of the matrix converter are not suitable for the control of the output current as these do not transfer power from the input to the load, instead, the energy stored by the resonant tank is consumed. Hence, this can lead to a significant distortion of the output current. Consequently, only active switching states of the matrix converter are taken into account, resulting in 18 switching states for the output control, 6 for the input control and 3 for the compensator capacitor voltage control. These switching states are defined in table 6.2.

Table 6.2 Switching states for the DSRC with output voltage compensator.

j	Input converter current			Output converter voltage	n	Capacitor current	Compensation voltage	m	Output voltage
	$K_{ia,j}$	$K_{ib,j}$	$K_{ic,j}$	$v_{matrix,j}$		$K_{hb,n}$	$v_{comp,n}$		$v_{tank,m}$
1	1	-1	0	v_{iab}	1	-1	$-V_{hb}$	1	$v_{iab}-V_{hb}$
					2	1	V_{hb}	2	$v_{iab}+V_{hb}$
					3	0	0	3	v_{iab}
2	1	0	-1	v_{iac}	1	-1	$-V_{hb}$	4	$v_{iac}-V_{hb}$
					2	1	V_{hb}	5	$v_{iac}+V_{hb}$
					3	0	0	6	v_{iac}
3	0	1	-1	v_{ibc}	1	-1	$-V_{hb}$	7	$v_{ibc}-V_{hb}$
					2	1	V_{hb}	8	$v_{ibc}+V_{hb}$
					3	0	0	9	v_{ibc}
4	-1	1	0	v_{iba}	1	-1	$-V_{hb}$	10	$v_{iba}-V_{hb}$
					2	1	V_{hb}	11	$v_{iba}+V_{hb}$
					3	0	0	12	v_{iba}
5	-1	0	1	v_{ica}	1	-1	$-V_{hb}$	13	$v_{ica}-V_{hb}$
					2	1	V_{hb}	14	$v_{ica}+V_{hb}$
					3	0	0	15	v_{ica}
6	0	-1	1	v_{icb}	1	-1	$-V_{hb}$	16	$v_{icb}-V_{hb}$
					2	1	V_{hb}	17	$v_{icb}+V_{hb}$
					3	0	0	18	v_{icb}

6.5.1 Compensator capacitance calculation

Since the voltage compensator is switched at every zero crossing of the tank current (ZCS operation), the capacitance can be determined by considering the voltage variation over a sampling period (ΔV_{hb}) and the nominal output current ($\hat{\imath}_{on}$). Thus, from (6.5), the compensator capacitance is given by:

$$C_{hb} = \frac{1}{\Delta V_{hb}} \int_{kT_s}^{(k+1)T_s} I_{hb}(t)dt \Rightarrow C_{hb} = \frac{2}{\pi} \frac{T_s}{\Delta V_{hb}} \hat{\imath}_{on} \tag{6.9}$$

6.5.2 Compensator capacitor voltage reference

To determine the reference value for the compensator capacitor voltage control, the output converter voltage must be analysed. In order to avoid saturation of the input current control, a voltage ratio equal to 0.75, i.e. $M_v = \frac{3}{4}$, is considered. Thus, the voltage applied to the resonant tank when the converter is controlled by IOPC is shown in figure 6.5.

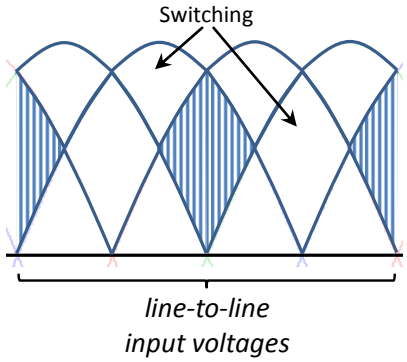


Fig. 6.5 Voltage applied to the resonant tank for IOPC strategy, $\boldsymbol{M_v = 0.75}$ (magnitude variation).

Since the compensator (H-bridge) can only provide a constant magnitude voltage (positive, negative or zero), the voltage reference is determined by considering the magnitude of the voltage applied to the resonant tank. In figure 6.6, the voltage compensation is illustrated. In this figure, it can be seen that if the magnitude of the voltage applied to the resonant tank is considered equal to a 75% of the line-to-line input voltage ($M_v = \frac{3}{4}$), the voltage variation between $\hat{v}_{LL}$ and $\frac{1}{2}\hat{v}_{LL}$ can be reduced if a voltage equal to $\pm\frac{1}{4}\hat{v}_{LL}$ is added. Hence, the reference for the compensator capacitor voltage can be selected as:

$$V_{hb}^{*} = \frac{1}{4}\hat{v}_{LL} \tag{6.10}$$

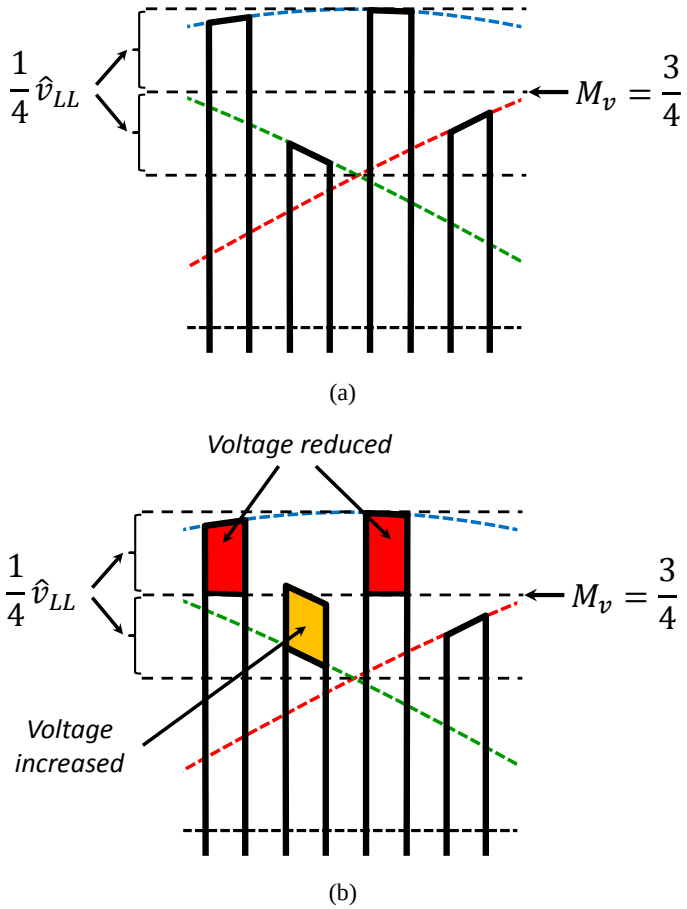


Fig. 6.6 Output voltage compensation: (a) voltage applied to the resonant tank and (b) compensated voltage applied to the resonant tank (negative output voltage is omitted for clarity).

6.5.3 IOPC with output voltage compensation

In this strategy, the control of the voltage compensator is combined with IOPC algorithm. Thus, from (5.14), (5.25), (6.2) and table 6.2, the output current prediction, the input current prediction and the compensator capacitor voltage prediction are calculated by:

$$\hat{\imath}^{p}_{tank,m} = E_{out22}\hat{\imath}_{tank}(k) + (\omega_d^{out} C_{tank} F_{out2}) v_{tank,m}(k) \quad ; \quad m = 1, \dots, 18 \qquad (6.11)$$

$$v_{tank,m}(k) = v_{matrix,j}(k) + v_{comp,n}(k) \quad ; \quad j = 1, \dots, 6 \quad n = 1, 2, 3 \qquad (6.12)$$

$$i^{p}_{s,j} = H_1 i_s(k) + H_2 v_i(k) + H_3 v_s(k) + \frac{1}{R_f} v_s(k+1) + \cdots$$

$$\cdots + H_4 K_{i,j} \frac{2}{\pi} \hat{\imath}_{tank}(k) \quad ; \quad j = 1, \dots, 6 \qquad (6.13)$$

$$V^{p}_{hb,n} = V_{hb}(k) + K_{hb,n} \frac{T_s}{C_{hb}} \frac{2}{\pi} \hat{\imath}_{tank}(k) \quad ; \quad n = 1, 2, 3 \qquad (6.14)$$

Considering the cost function for IOPC, equation (5.35), the cost function for this strategy is defined by (6.15), where λ_{hb} is the weighting factor related to the compensator capacitor voltage control. A scheme of this approach is shown in figure 6.7.

$$G_{IOPC,m} = \frac{\lambda_i}{\hat{\imath}_{sn}^2} G_{ICPC,j} + \frac{\lambda_o}{\hat{\imath}_{on}^2} G_{OCPC,m} + \frac{\lambda_{hb}}{(V_{hb}^*)^2} G_{hb,n} \; ; \; \begin{matrix} j = 1,\dots,6 \\ m = 1,\dots,18 \\ n = 1,2,3 \end{matrix} \tag{6.15}$$

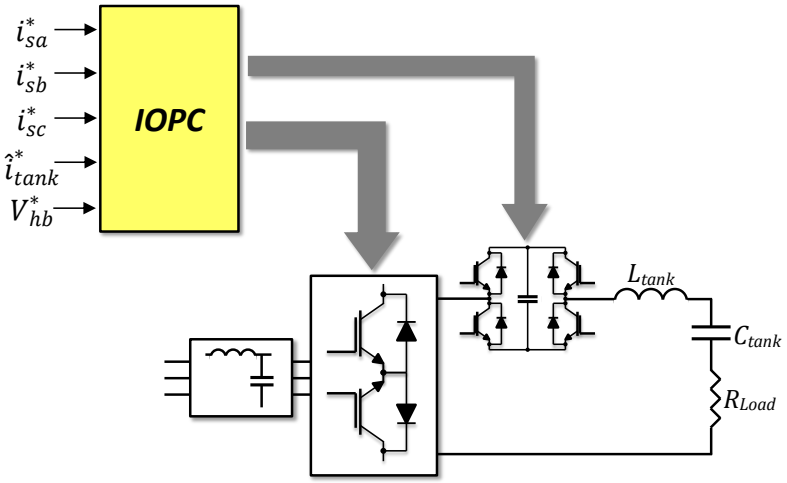


Fig. 6.7 Scheme of IOPC strategy with predictive control of the compensator capacitor voltage.

In this case, the process to determine the weighting factors of (6.15) can be a laborious task. As described in chapter 5, a primary control can be selected and, as a consequence, only two weighting factors need to be calculated. In order to simplify the process, in this work, both input and output control were chosen as primary control ($\lambda_i = \lambda_o = 1$), therefore, only the value of λ_{hb} was determined, as described in a later chapter.

6.5.4 Input current reference

As described in the previous chapter, the input current reference for IOPC is calculated by considering the power losses. Since the compensator operates under ZCS, in order to determine this reference, the conduction losses in the compensator are included in (5.48). As depicted in figure 6.3 and described later in chapter 7, the output voltage compensator utilised in this work is based on IGBTs, thus, the conduction losses of the H-bridge converter can be calculated by using (5.38)-(5.41):

$$P_{HB_{igbt}} = \frac{R_{CE\_hb}\hat{\imath}_{tank}^2}{2} + \frac{2}{\pi}\left(V_{CE0\_hb}\hat{\imath}_{tank}\right) \tag{6.16}$$

$$P_{HB_{diode}} = \frac{R_{F\_hb}\hat{\imath}_{tank}^2}{2} + \frac{2}{\pi}\left(V_{F0\_hb}\hat{\imath}_{tank}\right) \tag{6.17}$$

Since the devices of the H-bridge in the current path depend on the switching state applied and the tank current direction, as can be seen in figure 6.4, the compensator conduction losses can be determined by considering the highest power loss between semiconductor devices. Thus, the power loss owing to the voltage compensator can be estimated by:

$$P_{HB} = 2P_{HB_{igbt}} \tag{6.18}$$

Then, including (6.18) in (5.48):

$$\Delta P = \underbrace{2\left\{\left[\frac{R_{CE}}{2}(\hat{\imath}_{tank}^*)^2 + \frac{2}{\pi}(V_{CE0}\hat{\imath}_{tank}^*)\right] + \left[\frac{R_F}{2}(\hat{\imath}_{tank}^*)^2 + \frac{2}{\pi}(V_{F0}\hat{\imath}_{tank}^*)\right]\right\}}_{Matrix\ converter} + \cdots$$

$$\cdots + \underbrace{2\left\{\frac{R_{CE\_hb}}{2}(\hat{\imath}_{tank}^*)^2 + \frac{2}{\pi}\left(V_{CE0\_hb}\hat{\imath}_{tank}^*\right)\right\}}_{H-bridge} + \underbrace{\frac{R_{L_{tank}}(\hat{\imath}_{tank}^*)^2}{2}}_{Tank\ inductor} \tag{6.19}$$

Therefore, the input current reference can be calculated by (6.20), as discussed in chapter 5.

$$\hat{\imath}_s^* = \frac{\left(\frac{3}{2}\hat{v}_s\right) - \sqrt{\left(\frac{3}{2}\hat{v}_s\right)^2 - 6R_{eq}(P_{Load} + \Delta P)}}{3R_{eq}} \tag{6.20}$$

6.5.5 Delay compensation

In order to compensate the delay associated with the algorithm calculations, the approach presented in the previous chapter is considered. Thus, the estimation of the tank current magnitude at t_{k+1} is calculated by using equation (6.21) and the prediction of the compensator capacitor voltage at t_{k+2} is determined by (6.22) and (6.23).

$$v_{tank,opt}(k) = v_{matrix,opt}(k) + v_{comp,opt}(k) \tag{6.21}$$

$$V_{hb}(k+1) = V_{hb}(k) + K_{hb,opt}\frac{T_s}{C_{hb}}\frac{2}{\pi}\hat{\imath}_{tank}(k) \tag{6.22}$$

$$V_{hb,n}^{k+2} = V_{hb}(k+1) + K_{hb,n}\frac{T_s}{C_{hb}}\frac{2}{\pi}\hat{\imath}_{tank}(k+1) \quad ; \quad n = 1,2,3 \tag{6.23}$$

Finally, the cost function for the control of the compensator capacitor voltage is given by:

$$G_{hb,n} = \left(V_{hb}^{*} - V_{hb,n}^{k+2}\right)^2 \quad ; \quad n = 1,2,3 \tag{6.24}$$

6.6 Simulation results

Simulations for IOPC strategy with output voltage compensation were carried out in MATLAB/Simulink. The parameters used are based on the experimental implementation and given in tables 5.2 and 6.3. The weighting factor for the compensation voltage is 0.25 as used in the experimental validation. The selection of this value is explained in chapter 8.

The compensator capacitance and voltage reference are calculated using (6.9) and (6.10), respectively. For the capacitance calculation, the following parameters are considered: T_s=25.9µs, $\hat{\imath}_{on}$=14.14A and ΔV_{hb}=5V.

Thus, the compensator capacitance and the voltage reference are given by:

$$C_{hb} = \frac{2}{\pi}\frac{T_s}{\Delta V_{hb}}\hat{\imath}_{on} = 46.6\mu F \approx 50\mu F \tag{6.25}$$

$$V_{hb}^{*} = \frac{1}{4}\hat{v}_{LL} = \frac{1}{4}170\sqrt{3} \approx 73.6V \tag{6.26}$$

Table 6.3 Simulation parameters for IOPC with output voltage compensation.

Voltage compensator		C_{hb}	50µF
		V_{hb}^{*}	73.6V
H-bridge	IGBTs	V_{CE0_hb}/R_{CE_hb}	1.2V/52mΩ
	Diodes	V_{F0_hb}/R_{F_hb}	1.0V/32mΩ
Weighting factors		λ_i	1.0
		λ_o	1.0
		λ_{hb}	0.25

Figures 6.8-6.14 show the results for an output current reference of $10A_{rms}$. In figures 6.8 and 6.9, the control of the input current, output current and compensator capacitor voltage are shown.

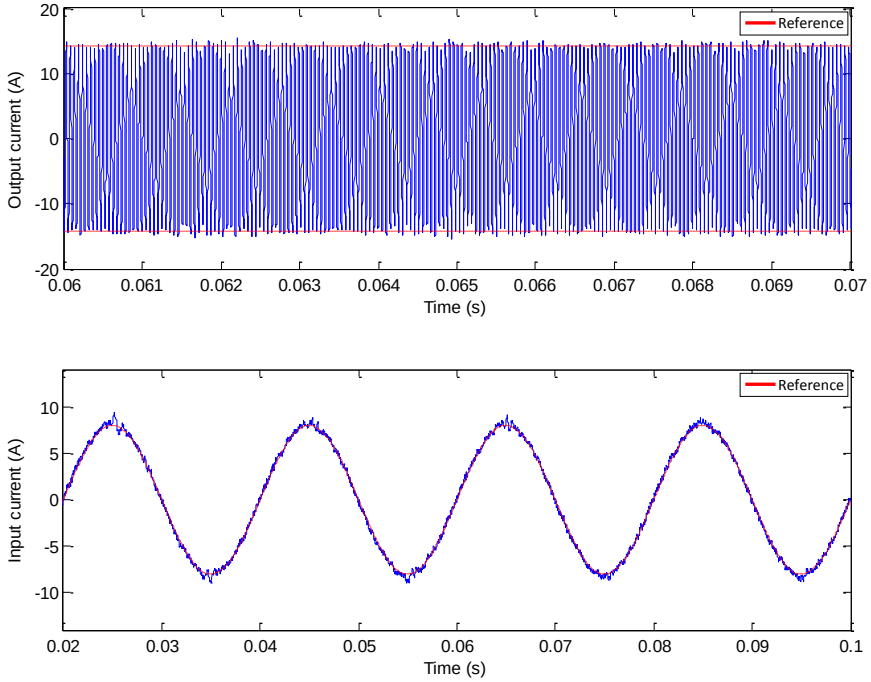


Fig. 6.8 Simulation results for IOPC with voltage compensation: input and output control.

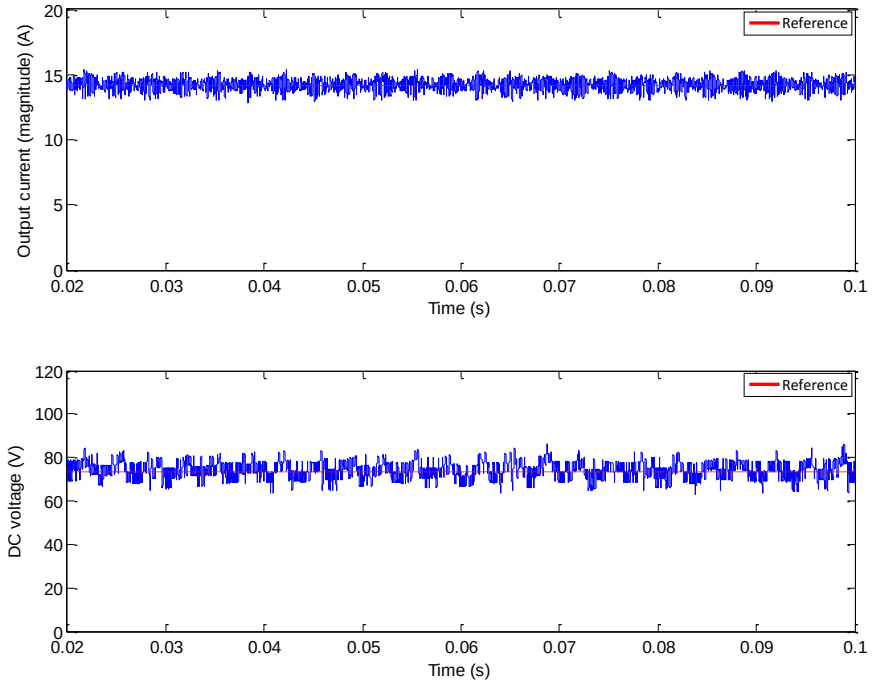


Fig. 6.9 Simulation results for IOPC with voltage compensation: output current magnitude and compensator capacitor voltage control.

The compensation voltage can be observed in figures 6.10 and 6.11, where the output matrix converter voltage, the voltage applied to the resonant tank and the output compensator voltage are depicted.

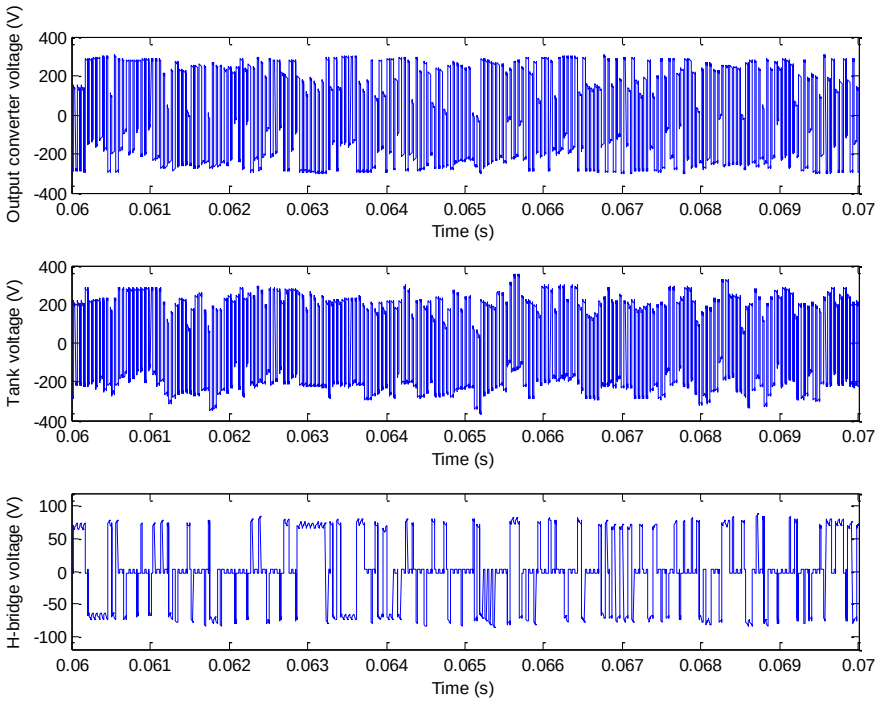


Fig. 6.10 Simulation results for IOPC with voltage compensation: output matrix converter voltage, voltage applied to the resonant tank and output compensator voltage.

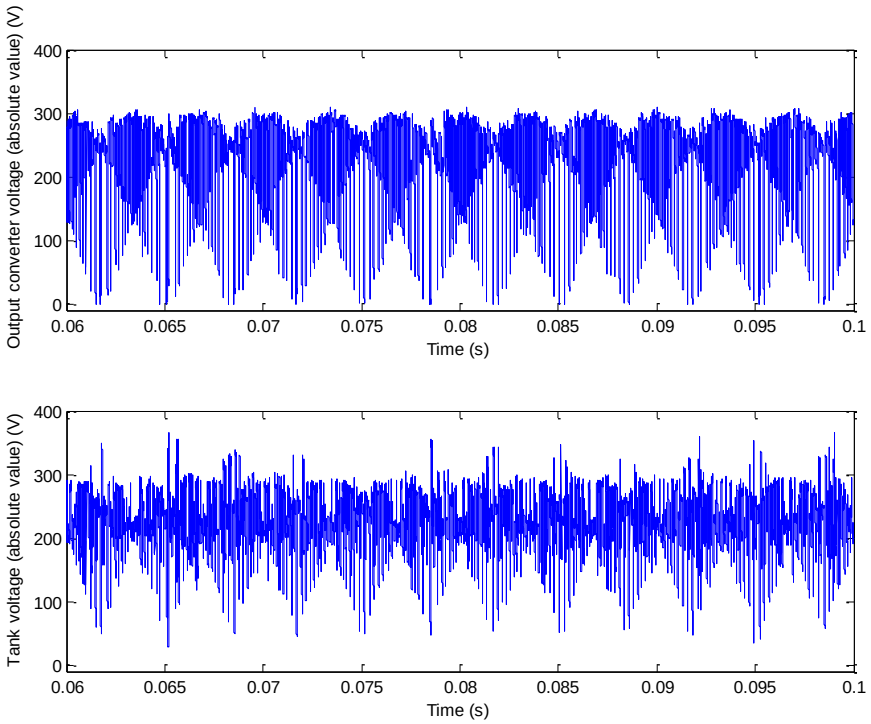


Fig. 6.11 Simulation results for IOPC with voltage compensation: output matrix converter voltage and voltage applied to the resonant tank (magnitude variation).

The unity power factor and the resonant tank waveforms are shown in figure 6.12. In addition, the frequency spectrum of the input current and the input waveforms are depicted in figures 6.13 and 6.14, respectively.

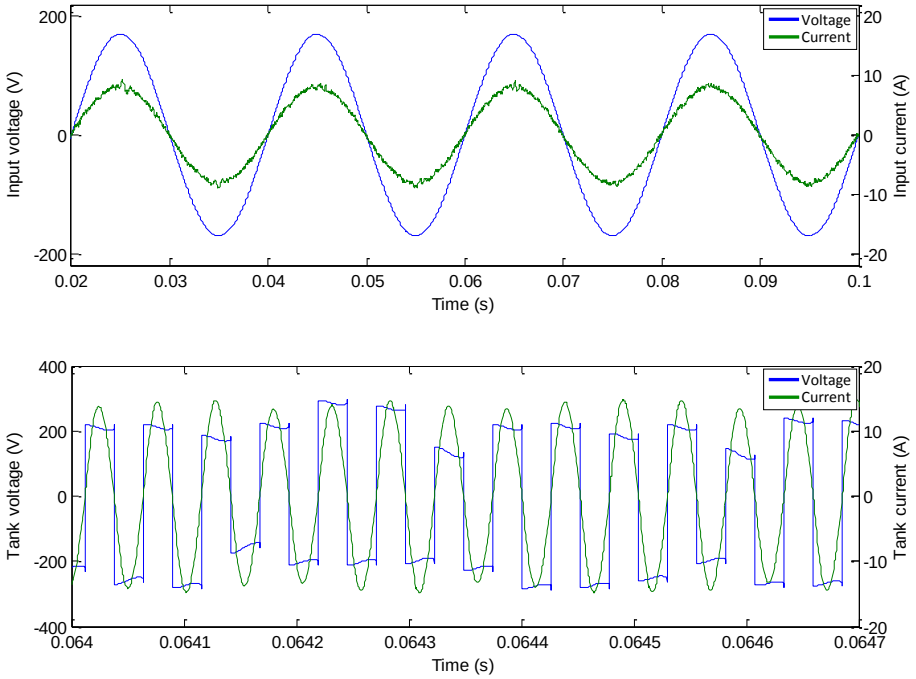


Fig. 6.12 Simulation results for IOPC with voltage compensation: input voltage/current, voltage applied to the resonant tank and tank current.

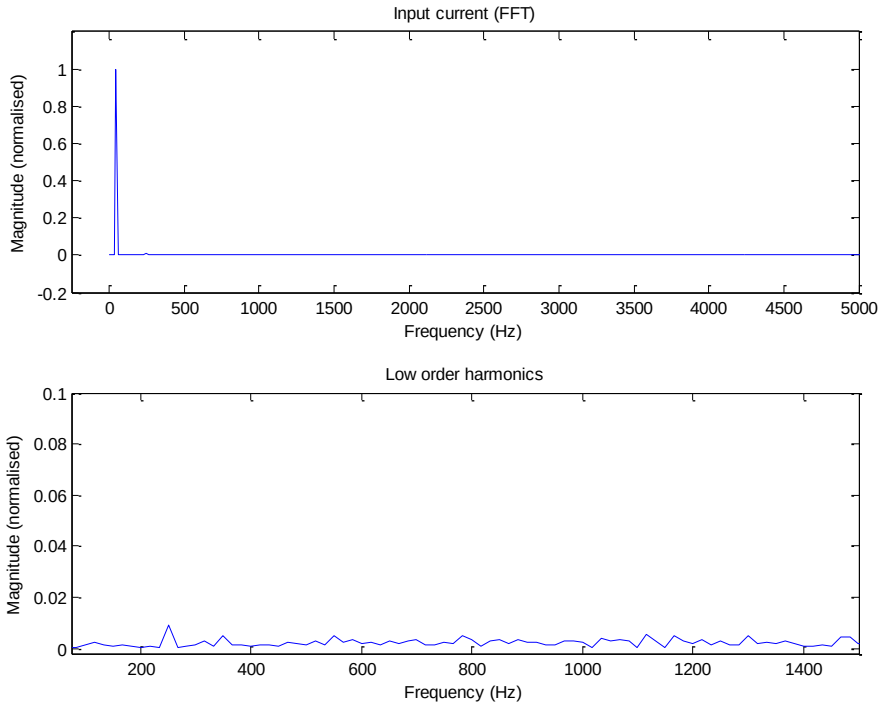


Fig. 6.13 Simulation results for IOPC with voltage compensation: FFT of the input current.

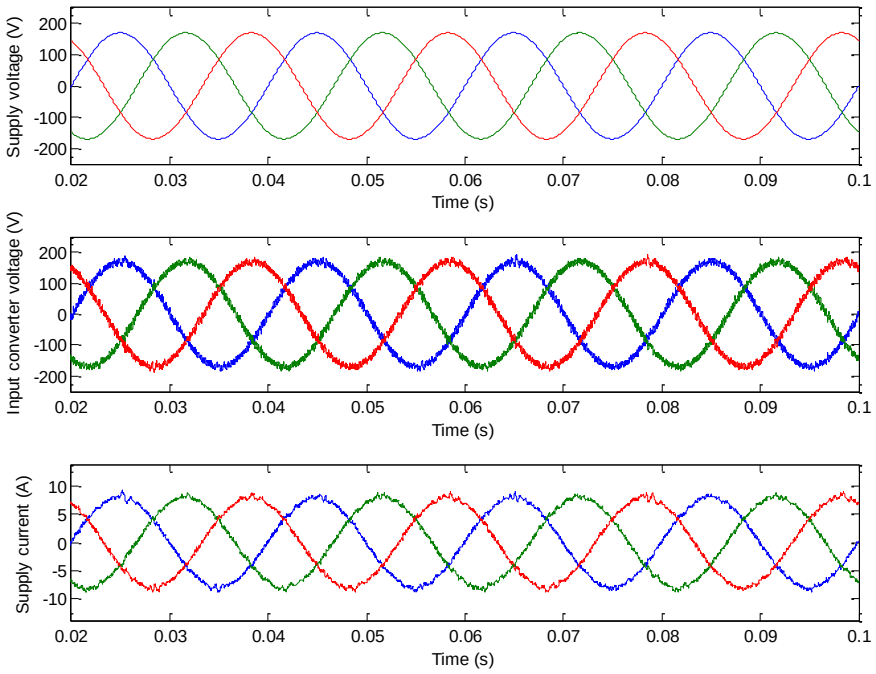


Fig. 6.14 Simulation results for IOPC with voltage compensation: input voltage, input capacitor voltage and input current.

Results considering an output current reference of 11.3A$_{rms}$ ($M_v \approx \frac{\sqrt{3}}{2}$) are shown in figures 6.15-6.18. In figures 6.17 and 6.18, it can be seen the voltage compensation, whereas the effects of overmodulation on the input current can be observed in figure 6.15.

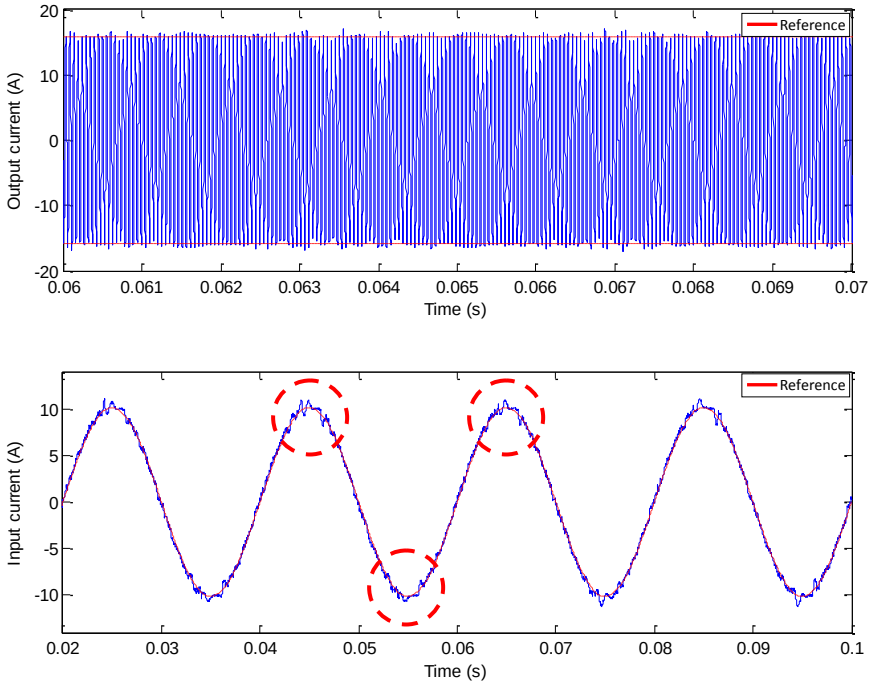


Fig. 6.15 Simulation results for IOPC with voltage compensation ($\boldsymbol{M_v \approx \frac{\sqrt{3}}{2}}$): input and output control.

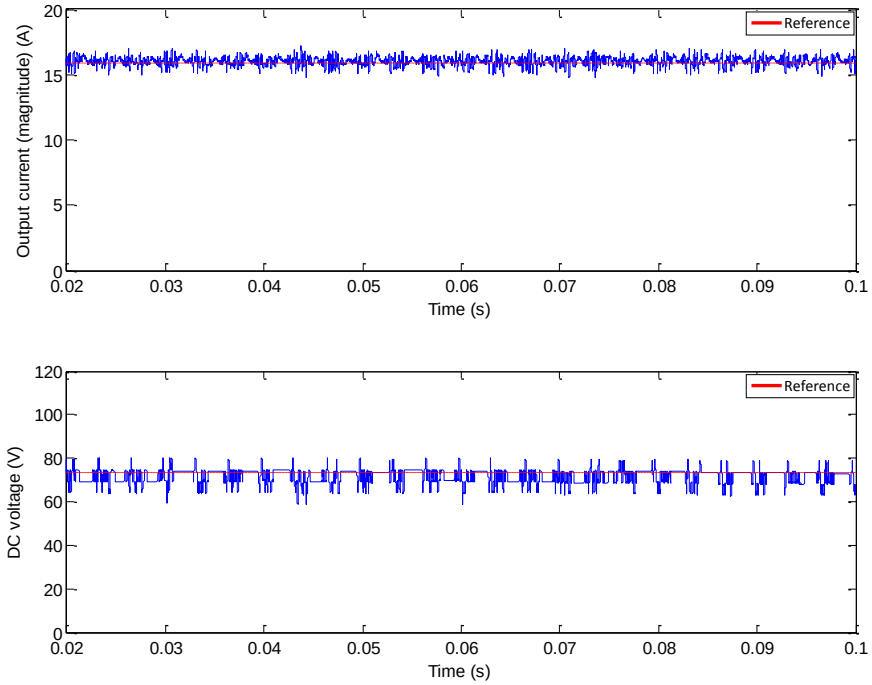


Fig. 6.16 Simulation results for IOPC with voltage compensation ($\boldsymbol{M_v} \approx \frac{\sqrt{3}}{2}$): output current magnitude and compensator capacitor voltage control.

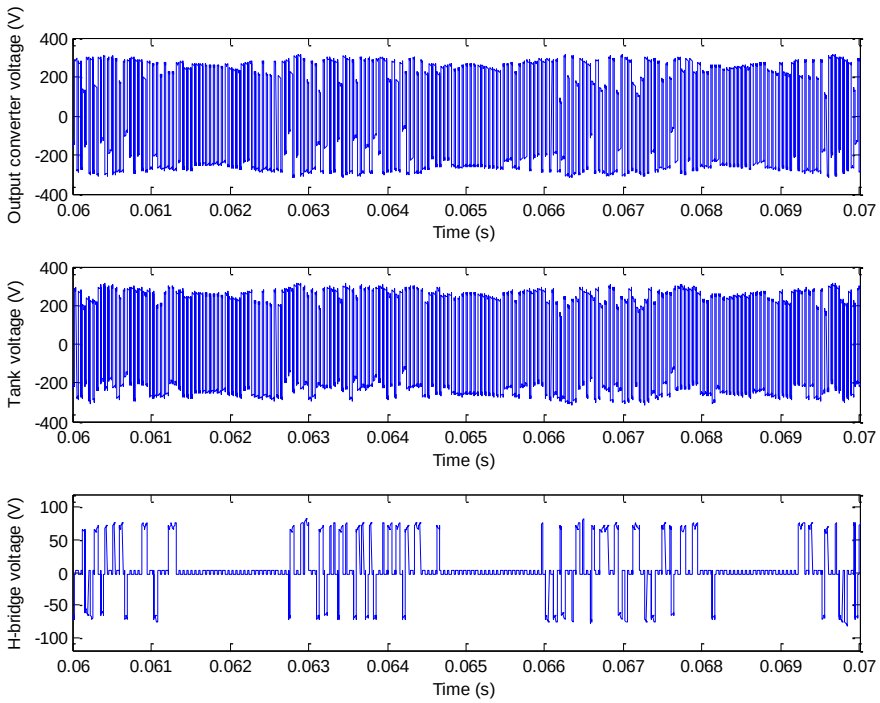


Fig. 6.17 Simulation results for IOPC with voltage compensation ($\boldsymbol{M_v} \approx \frac{\sqrt{3}}{2}$): output matrix converter voltage, voltage applied to the resonant tank and output compensator voltage.

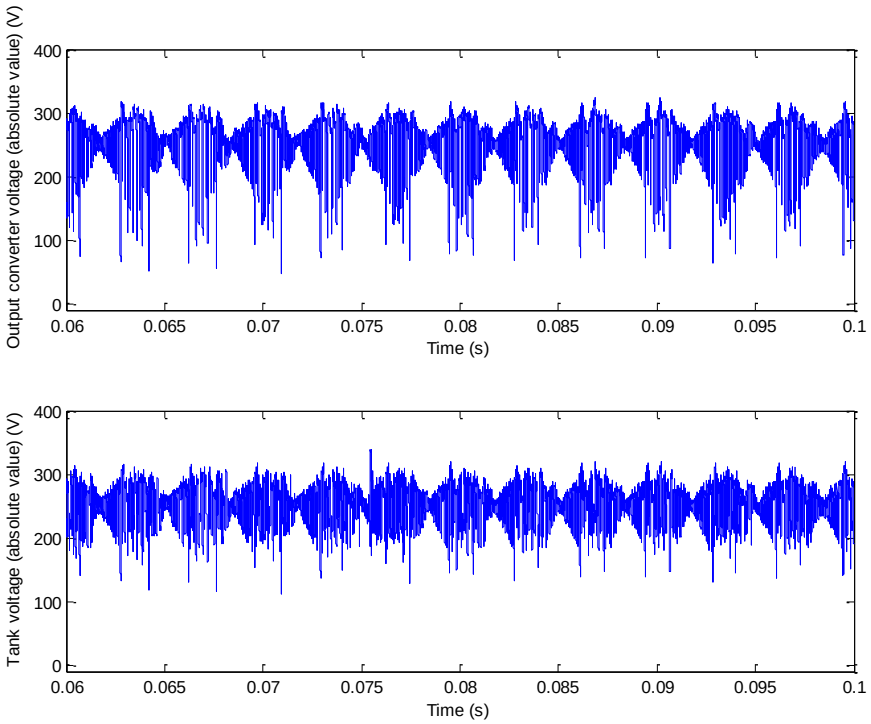


Fig. 6.18 Simulation results for IOPC with voltage compensation ($\boldsymbol{M_v} \approx \frac{\sqrt{3}}{2}$): output matrix converter voltage and voltage applied to the resonant tank (magnitude variation).

Figures 6.19-6.22 show the control responses when a step change reference is applied to the output current control and the compensator capacitor voltage control.

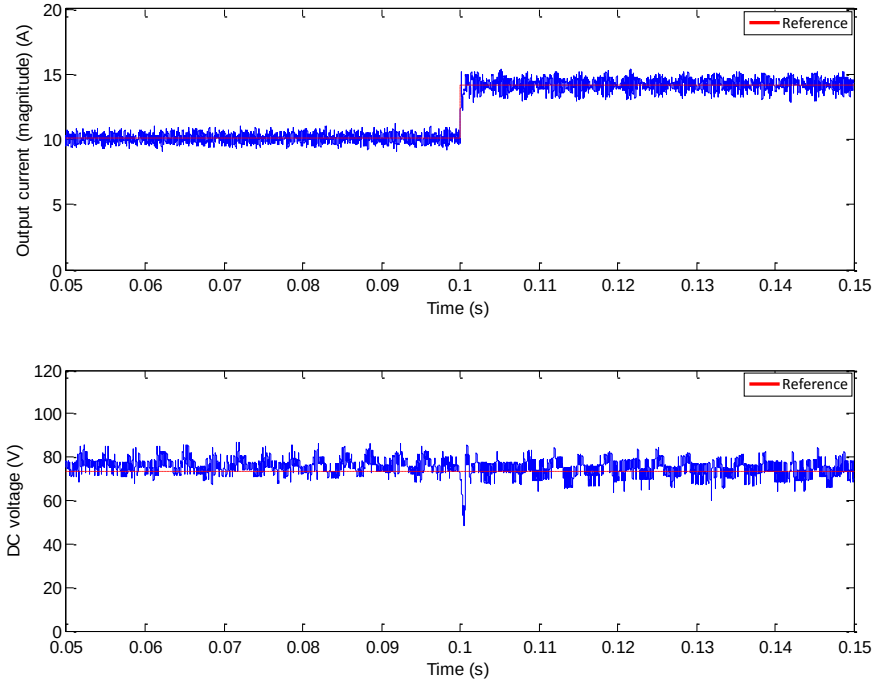


Fig. 6.19 Simulation results for IOPC with voltage compensation: output current magnitude and compensator capacitor voltage control for a step change in the output current reference from 10A to 14A at time 0.1s.

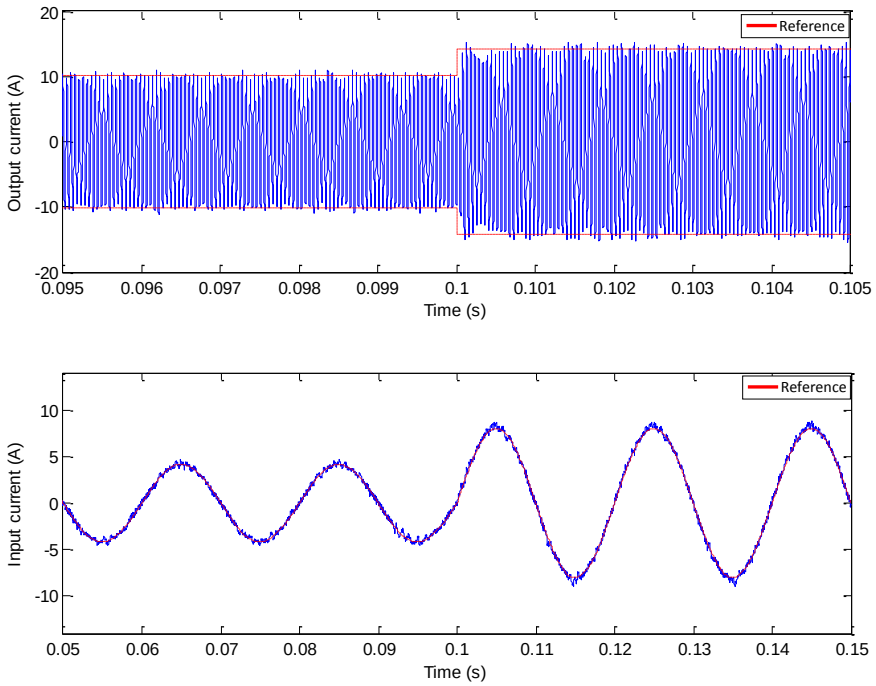


Fig. 6.20 Simulation results for IOPC with voltage compensation: input and output control for a step change in the output current reference from 10A to 14A at time 0.1s.

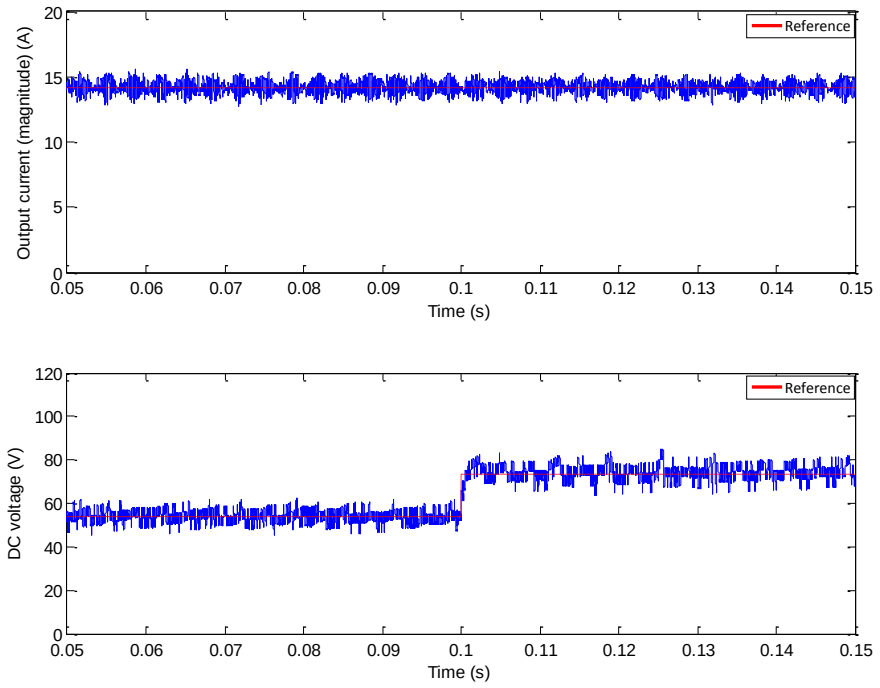


Fig. 6.21 Simulation results for IOPC with voltage compensation: output current magnitude and compensator capacitor voltage control for a step change in the compensator capacitor voltage reference from 53.6V to 73.6V at time 0.1s.

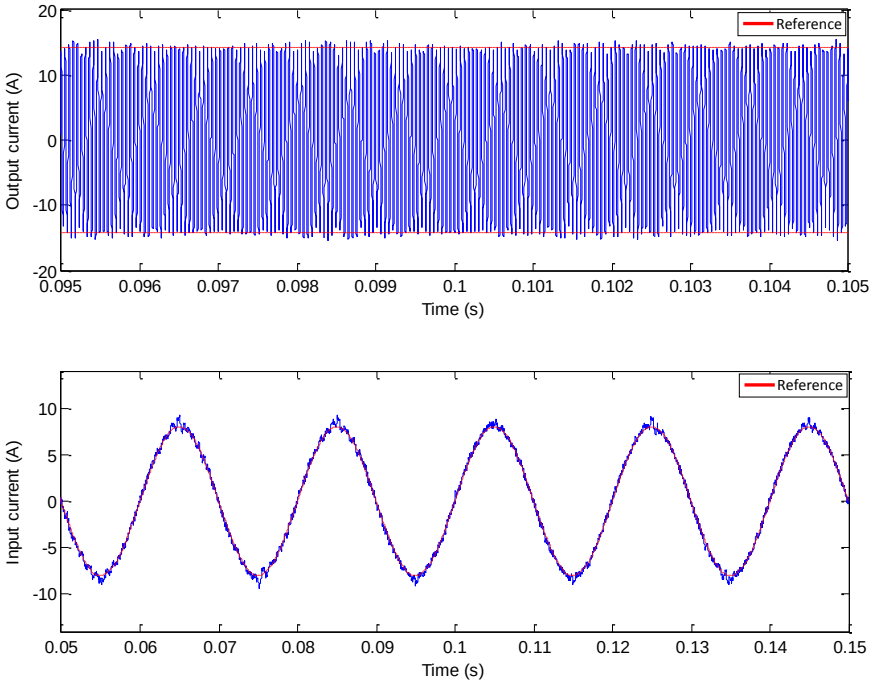


Fig. 6.22 Simulation results for IOPC with voltage compensation: input and output control for a step change in the compensator capacitor voltage reference from 53.6V to 73.6V at time 0.1s.

In figures 6.23-6.25, results considering a supply impedance (1mH/1mΩ) are depicted. Since the ripple of the supply voltage can affect the control algorithm calculations, an input voltage filter based on the d-q axis is implemented. This filter is described in chapter 7.

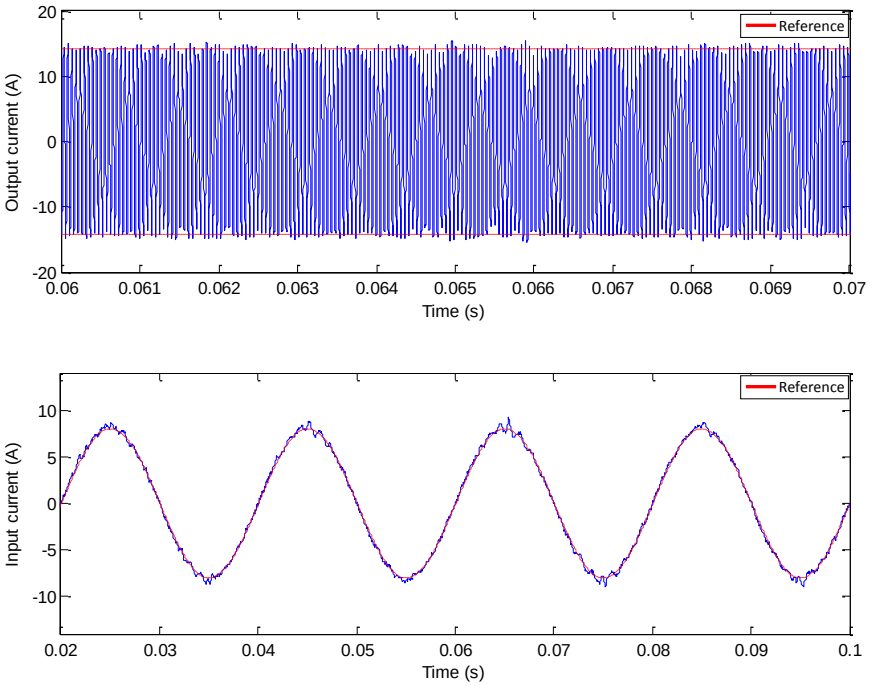


Fig. 6.23 Simulation results for IOPC with voltage compensation considering a supply impedance: input and output current.

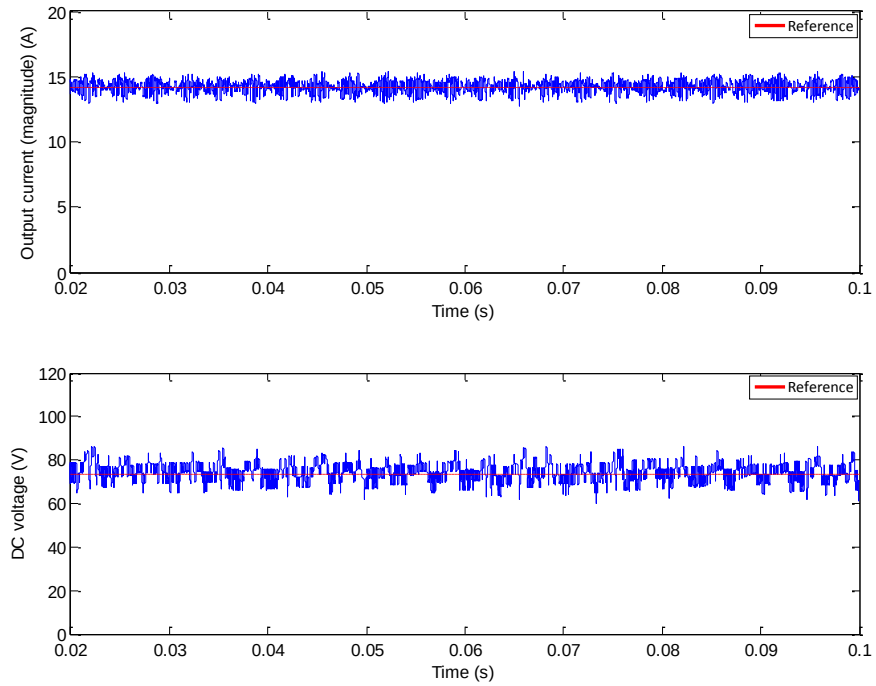


Fig. 6.24 Simulation results for IOPC with voltage compensation considering a supply impedance: output current magnitude and compensator capacitor voltage control.

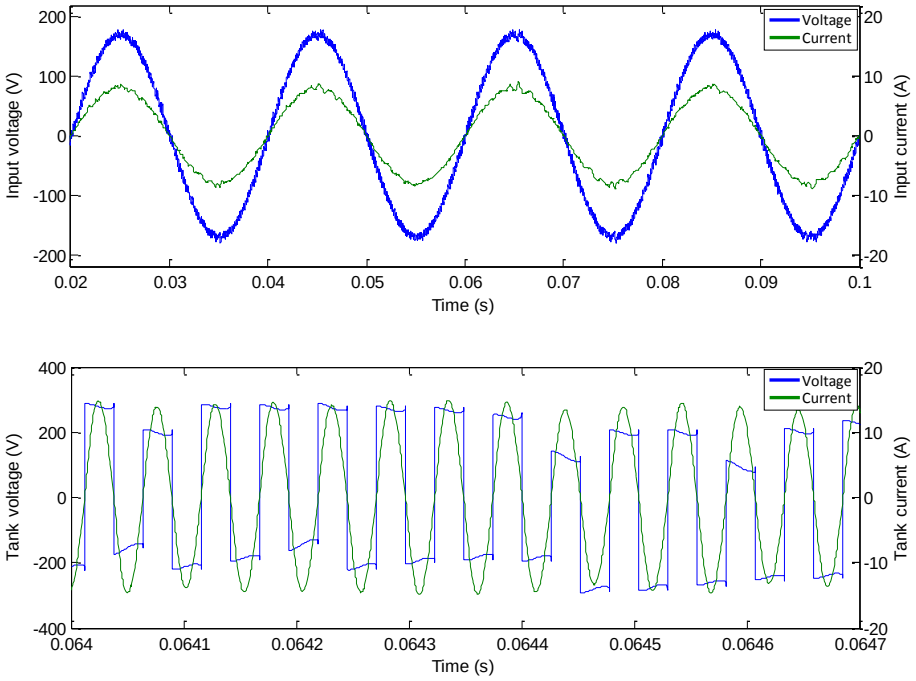


Fig. 6.25 Simulation results for IOPC with voltage compensation considering a supply impedance: input voltage/current, voltage applied to the resonant tank and output current.

6.6.1 Effect of model parameter errors

Since the predictive control algorithm is directly based on the discrete-time model of the system, it is important to evaluate the behaviour of the predictive control considering errors in the model parameters. Tables 6.4-6.6 give the RMS error of each controlled variable for different parameter errors.

Table 6.4 Effects of the errors in the input filter model.

	L_f/C_f						
	-50%	-20%	-10%	+0%	+10%	+20%	+50%
RMS error Input current	1.154	0.870	0.834	0.812	0.802	0.799	0.817
RMS error Output current	1.226	0.975	0.924	0.879	0.856	0.824	0.779
RMS error DC capacitor voltage	25.565	15.137	13.646	11.976	10.643	9.551	8.435

Table 6.5 Effects of the errors in the resonant tank inductance value.

	L_{tank}						
	-20%	-10%	-5%	+0%	+5%	+10%	+20%
RMS error Input current	1.675	0.962	0.831	0.812	0.811	0.884	1.186
RMS error Output current	1.564	0.976	0.889	0.879	0.890	0.929	1.180
RMS error DC capacitor voltage	10.378	10.677	12.081	11.976	11.590	10.407	9.391

Table 6.6 Effects of the errors in the compensator capacitance value.

	C_{hb}				
	-50%	-20%	+0%	+20%	+50%
RMS error Input current	0.854	0.806	0.812	0.803	0.804
RMS error Output current	0.948	0.901	0.879	0.848	0.857
RMS error DC capacitor voltage	7.512	10.004	11.976	14.038	16.488

In figures 6.26-6.27, the results obtained considering L_f±20% and C_f±20% (both parameters are simultaneously modified) are shown.

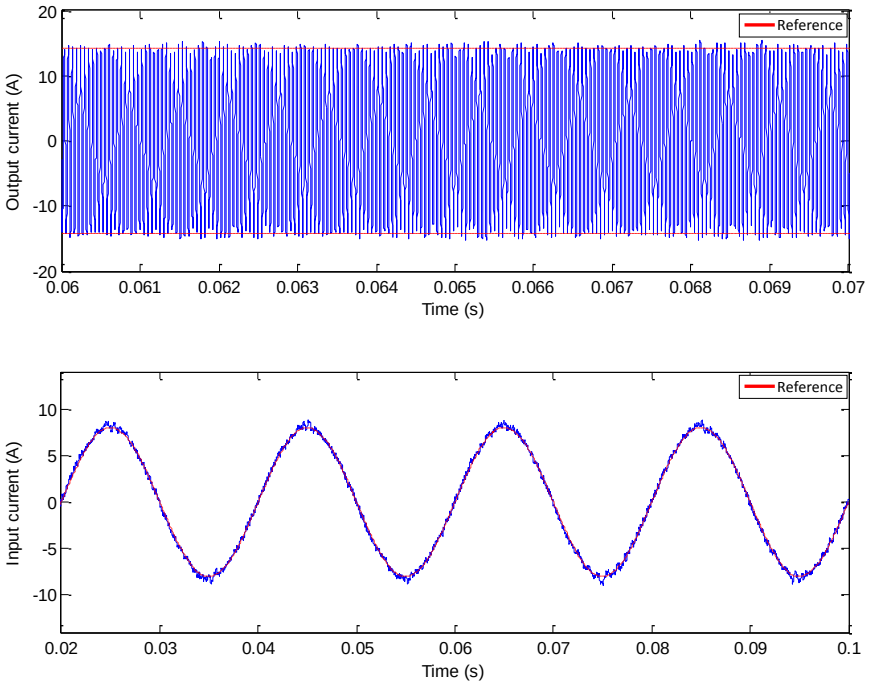


Fig. 6.26 Model parameter errors ($\boldsymbol{L_f}$/$\boldsymbol{C_f}$-20%): input and output current control.

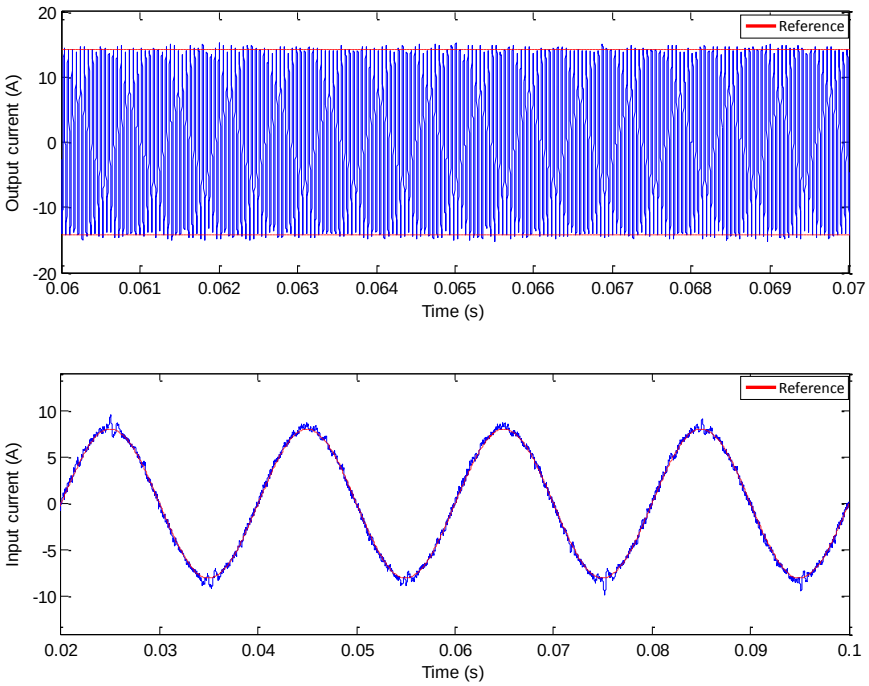


Fig. 6.27 Model parameter errors ($\boldsymbol{L_f}$/$\boldsymbol{C_f}$+20%): input and output current control.

In order to show the effects of a significant parameter error, figures 6.28-6.29 depict the results when the error in the tank inductance value corresponds to -20%.

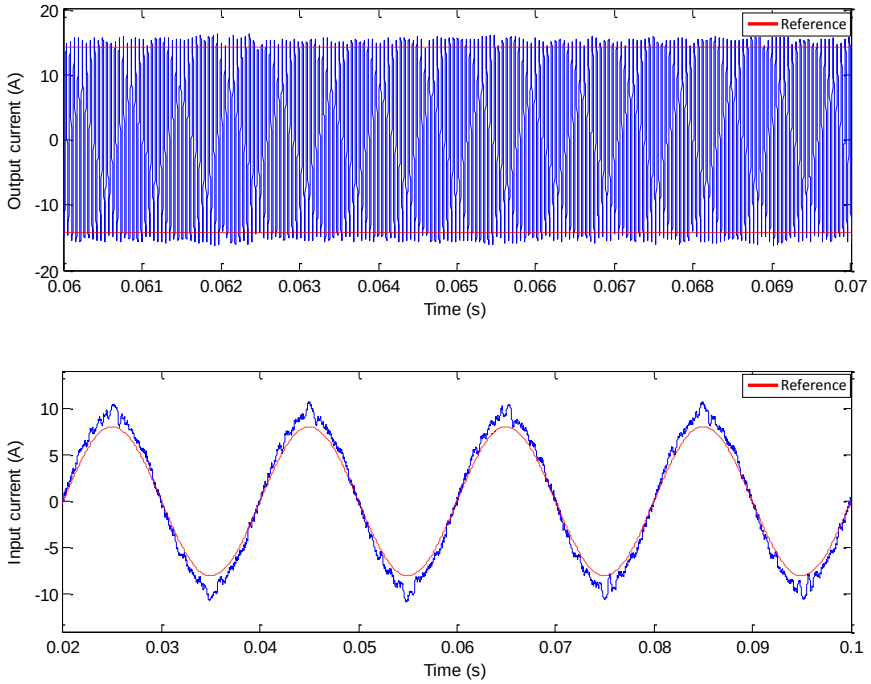


Fig. 6.28 Model parameter errors (L_{tank}-20%): input and output current control.

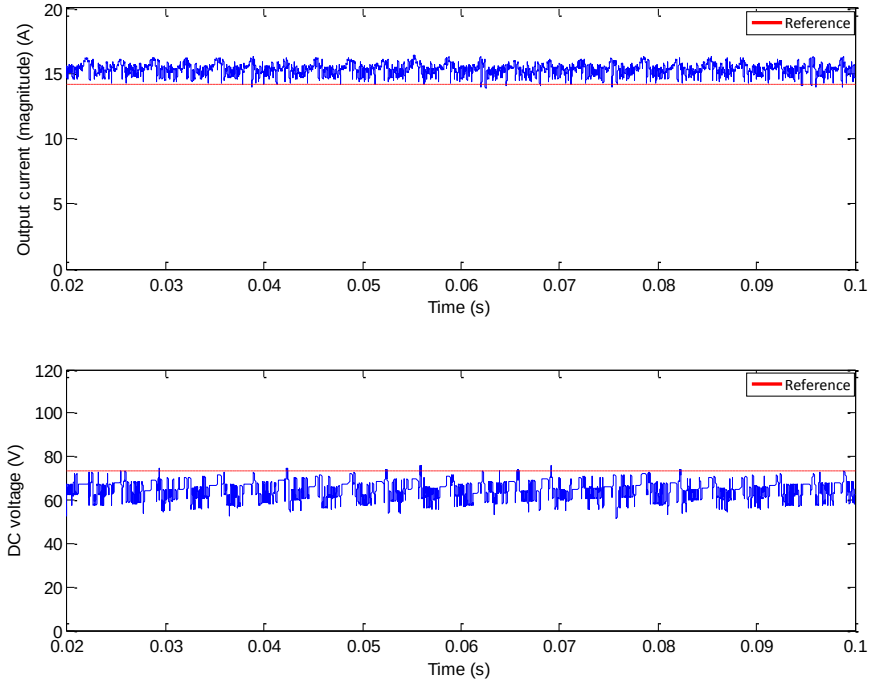


Fig. 6.29 Model parameter errors (L_{tank}-20%): output current magnitude and compensator capacitor voltage control.

From tables 6.4-6.6, it can be seen that for a parameter error range of ±5%, the predictive algorithm can perform with no significant error in the calculations. For a range higher than 10%, especially in the resonant tank parameters, the correct performance of the predictive algorithm cannot be ensured.

6.7 Summary

This chapter has discussed a new voltage compensation strategy for a direct resonant converter. This compensation approach is based on connecting an H-bridge converter in series between the matrix converter and the resonant tank in order to mitigate the effects of controlling the input current on the output matrix converter voltage. This voltage compensator operates under ZCS in an effort to reduce the effects of the compensator on the converter efficiency.

In order to control the compensator capacitor voltage, the IOPC strategy has been expanded. In addition, the calculations of the compensator capacitance and voltage reference have been discussed. Finally, simulation results and a brief analysis of the effects of the model parameter errors on the control performance have been presented.

Chapter 7

Experimental Implementation

7.1 Introduction

In this chapter, the experimental system used to verify and validate the operation and control of a direct series resonant converter is described. The main components of this system are:

- Three-phase to single-phase matrix converter.
- H-bridge converter.
- C6713 DSK development board (part of the control platform).
- FPGA board (part of the control platform).
- HPI board (part of the control platform).
- Resonant tank.
- Resistive load.
- Three-phase autotransformer.
- Voltage and current measurement boards.
- Output current magnitude measurement board.

Figures 7.1 and 7.2 show the experimental rig and a simplified diagram of the system, respectively. In figure 7.2, the dc power supplies for the measurement boards and converters (gate drive circuits), ±15V and +5V, are omitted for clarity.

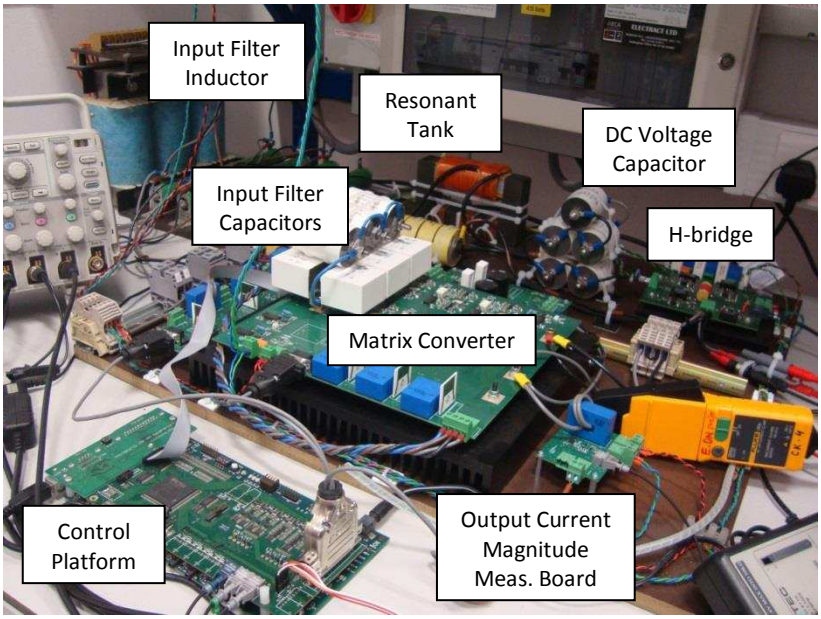


Fig. 7.1 Experimental system.

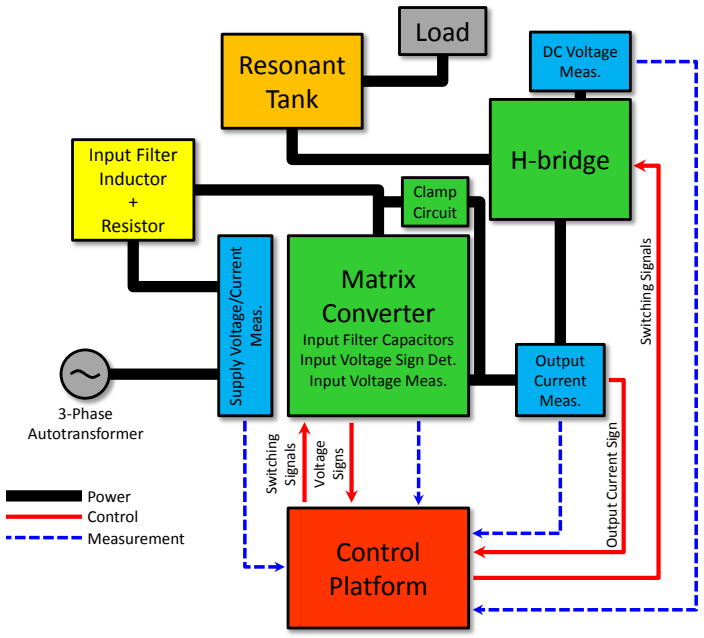


Fig. 7.2 Connection diagram of the experimental system.

7.2 Matrix converter

The three-phase to single-phase matrix converter employed in this work is depicted in figure 7.3. This converter is a 7.5kW six-layer PCB prototype which is designed for use in different matrix converter applications in the PEMC Group, University of Nottingham. This prototype consists of six IGBT power modules and their gate drive

circuits, three circuits for input voltage sign detection and three voltage transducers for measuring the input voltage. Since this prototype has been utilised in several topologies of two-stage matrix converters, a clamp circuit is included in the design, however, particularly for the application in this research, an external clamp circuit was implemented.

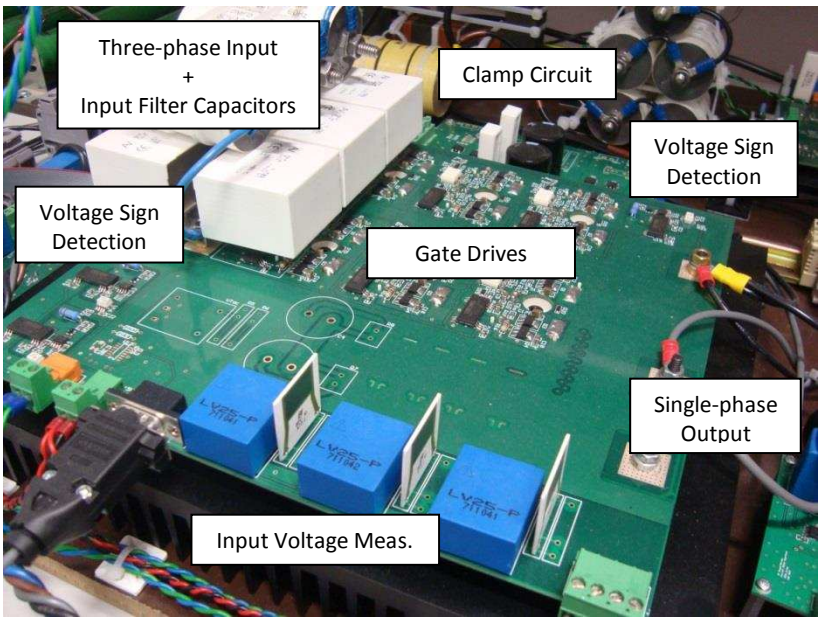
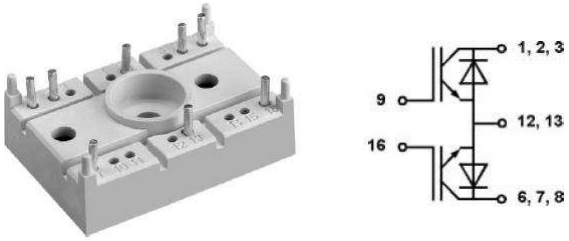


Fig. 7.3 Three-phase to single-phase matrix converter.

The control platform supplies the switching signals to the matrix converter via a Samtec FFSD IDC ribbon cable. This cable also includes the input voltage sign signals, which are sent from the matrix converter to the control platform, for the commutation strategy.

7.2.1 Power modules

The 3Ø/2Ø matrix converter uses six SEMIKRON SK60GM123 (1200V/60A) bidirectional power modules, shown in figure 7.4. These IGBT modules consist of two unidirectional power switches connected in common emitter configuration.



(a) (b)

Fig. 7.4 SEMIKRON SK60GM123: (a) power module and (b) pin configuration.

7.2.2 Gate drive circuits

Each power module requires a gate drive circuit, which allows control of every active semiconductor device. The matrix converter prototype used in this work has six isolated gate drive circuits, one for every IGBT module. Since the bidirectional switch is a common emitter arrangement, each gate drive circuit is powered by a single DCP020515 miniature isolated 2W unregulated dc-dc converter, which can provide an output voltage of ±15V from an input of +5V.

The gate signals (from the control platform) for each module are connected to an HCPL-315J dual IGBT gate drive optocoupler (0.5A peak output current) via two SN74LVC1G07 open-drain buffers/drivers. In order to ensure a fast switching of the semiconductor devices, the dual gate drive optocoupler drives two push-pull amplifiers which are composed of two transistors, an NPN FZT690B and a PNP FZT790A. In addition, for each IGBT, a resistor is connected between gate and the common point to prevent the device undesirably turning on owing to the charge stored in the parasitic capacitance when a gate drive circuit fault occurs or the control board is switched off and the main power supply is on. A schematic diagram of the gate drive circuit for an IGBT module is depicted in figure 7.5.

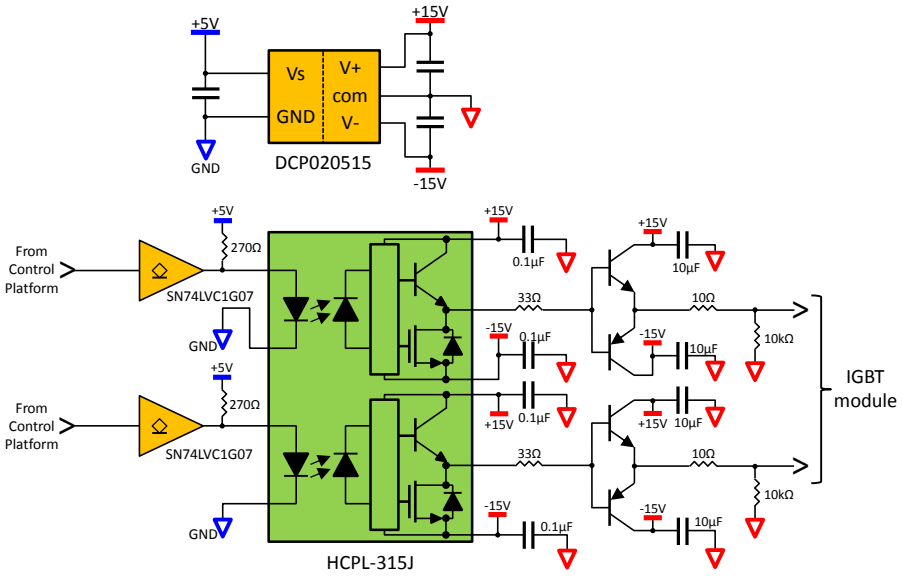


Fig. 7.5 Schematic diagram of the gate drive circuit for a power module of the matrix converter.

7.2.3 Input voltage sign detection

To switch the matrix converter safely, a voltage-based four-step commutation strategy, which is described in chapter 4, is employed. This strategy utilises the sign of the line-to-line input voltage to control the switching sequence of the

semiconductor devices. To detect the input voltage sign, three isolated circuits are included in the matrix converter. A schematic diagram of the sign detection circuit for the input voltage V_{ab} is shown in figure 7.6.

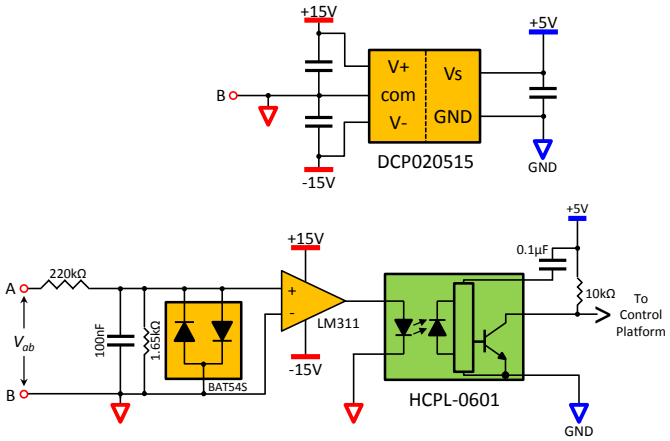


Fig. 7.6 Schematic diagram of the voltage sign detection circuit for V_{ab}..

A series resistor (220kΩ/1W) limits the current through the input diodes (to less than 200mA), which restrict the comparator input voltage to a value less than ±0.8V. Since the converter input voltage (input capacitor voltage) contains some ripple, a capacitor is used for filtering purposes and to avoid problems associated with the sign signal generation at the zero crossing of the input voltage. The voltage sign detection circuits are connected to the control platform through the optocouplers.

7.2.4 Clamp circuit

The clamp circuit, described in chapter 4, used in this work corresponds to a design intended to be employed in different matrix converter applications, therefore, this is oversized for the converter of this research. This circuit is composed of two rectifiers, which utilise a total of ten VS-8EWF12SPBF 8A/1200V fast soft recovery diodes. These rectifiers are connected to two 150µF/450V capacitors in parallel with two 47kΩ/7W resistors. The clamp circuit is depicted in figure 7.7.

Fig. 7.7 Clamp circuit.

7.2.5 Input filter

The input filter is composed of a 1.75mH per phase three-phase inductor connected in parallel with three 50Ω resistors. The input capacitors, 14μF/500V per phase, are depicted in figure 7.3, whilst figure 7.8 shows the input filter inductor.

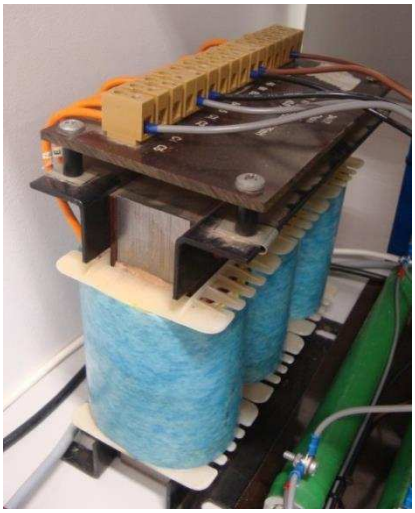


Fig. 7.8 Input filter inductor.

7.3 H-bridge converter

The H-bridge converter corresponds to a two-layer PCB prototype which is designed for use in multi-level converter applications in the PEMC Group, University of Nottingham. This prototype uses an H-bridge IGBT module and includes the gate drive circuits for every semiconductor device. To avoid turning on two devices in one leg at the same time, each gate drive contains an analogue dead-time circuit. In addition, only two switching signals (top IGBTs) are needed to control the converter, since the switching pulses for the bottom devices are generated inverting these signals. Figures 7.9 shows the H-bridge converter employed in the experimental rig.

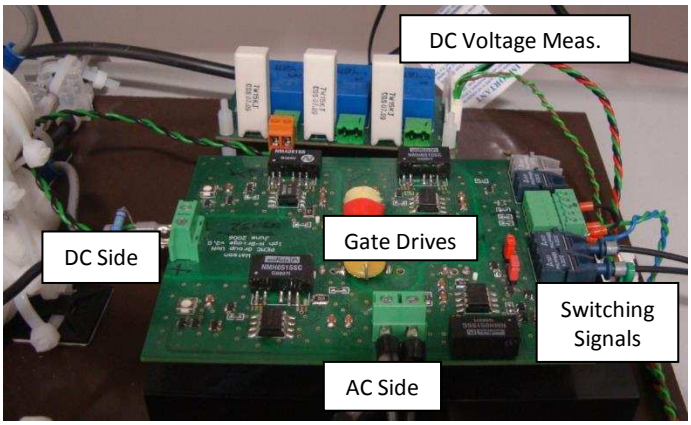
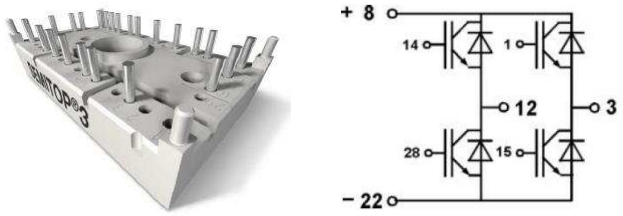


Fig. 7.9 H-bridge converter.

The connection between the control platform and the H-bridge converter is through Avago Technologies HFBR-1521Z /HFBR-2521Z fibre optic transmitters/receivers. A 50μF/500V capacitor is connected to the dc side.

7.3.1 H-bridge power module

The H-bridge converter is based on a SEMIKRON SK30GH123 (1200V/30A) power module which contains four IGBTs. This power module is depicted in figure 7.10.



(a) (b)

Fig. 7.10 SEMIKRON SK30GH123: (a) power module and (b) pin configuration.

7.3.2 Gate drive circuits

The H-bridge converter has four gate drive circuits, one for every IGBT of the power module. Each circuit uses an HCPL-3120 gate drive optocoupler (2A peak output current) and an NMH0515SC isolated 2W dc-dc converter (+5V to ±15V). In addition, an SN74LVC1G06 open-drain single inverter buffer/driver is employed to drive the optocoupler and two Zener diodes are used to limit the gate-emitter voltage to ±15V. Also, to prevent the IGBTs turning on as a result of the charge stored in the device parasitic capacitance in the event of, for example, power or control board failure, a resistor is connected between the gate and emitter connections. As previously mentioned, every gate drive includes an analogue dead-time circuit, which is described in the next section. Furthermore, since the H-bridge converter is designed for different applications, an enable signal (EN in figure 7.11) is used to ensure the bottom IGBTs are not switched on in the absence of switching signals. A schematic diagram of a gate drive circuit of the H-bridge converter is shown in figure 7.11.

7.3.3 Dead-time implementation

The analogue dead-time circuit implemented allows a low-to-high transition to be delayed through an RC circuit. The delay is adjustable by modifying the time constant of the RC network. Figure 7.12 illustrates a diagram of the dead-time circuit.

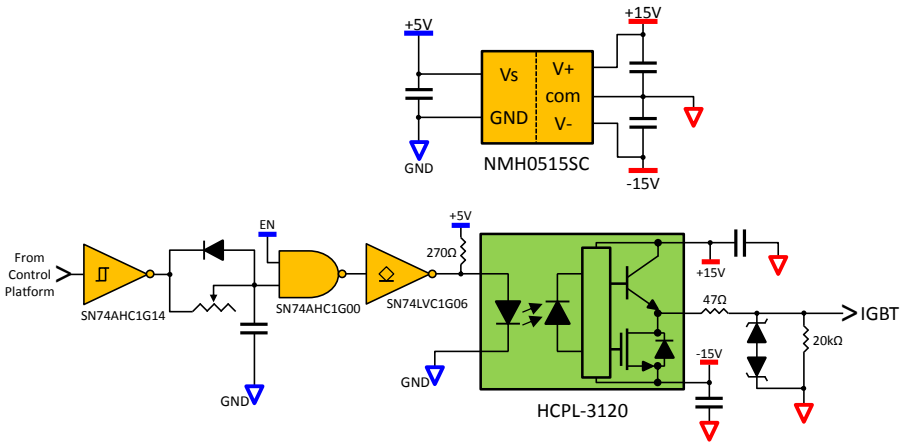


Fig. 7.11 Schematic diagram of a gate drive circuit of the H-bridge converter.

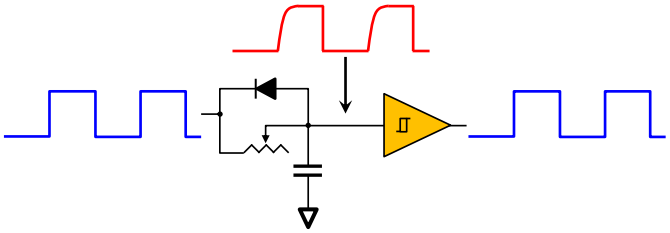


Fig. 7.12 Circuit for the dead-time implementation.

7.4 Control platform

The control platform is composed of a C6713 DSK board, an FPGA board and an HPI card. A diagram of the control platform is depicted in figure 7.13. This platform allows the system to be controlled and monitored, and performs different processes such as:

- Control algorithm calculations.
- Analogue to digital conversion.
- Generation of the switching signals for the power converters.
- Generation of trip signals to switch the power converters off in case of a fault or unsafe condition.

7.4.1 C6713 DSK board

The C6713 DSK (DSP Starter Kit), shown in figure 7.14, is a Texas Instruments development board based on a TMS320C6713 floating-point DSP. A diagram of the

C6713 DSK board is depicted in figure 7.15 [31]. The main characteristics of this DSK board are [32]:

- A DSP operating at 225MHz.
- 1800/1350 MIPS/MFLOPS.
- 512KB of Flash memory.
- 16MB of synchronous DRAM (SDRAM).
- 32-bit External Memory Interface (EMIF).
- A Host Port Interface (HPI).

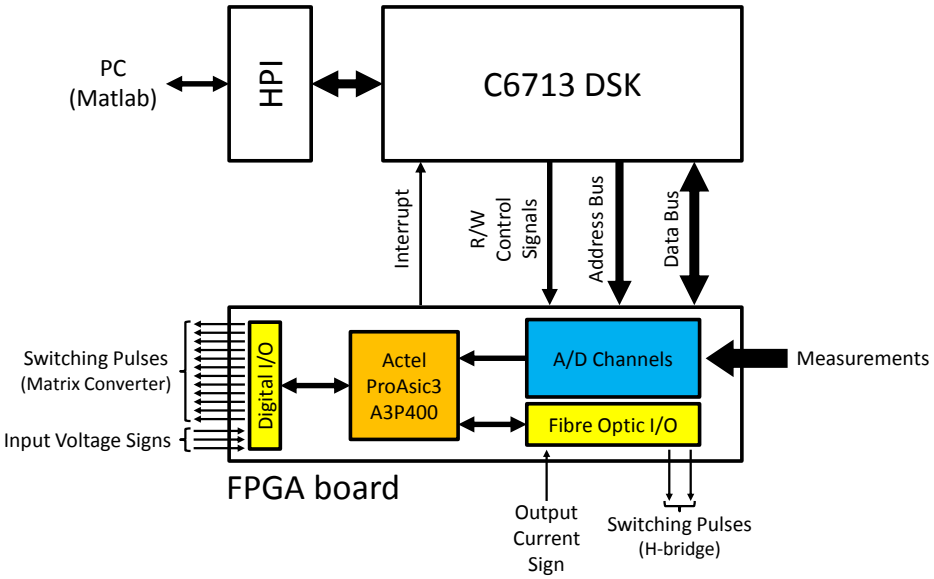


Fig. 7.13 Control platform diagram.

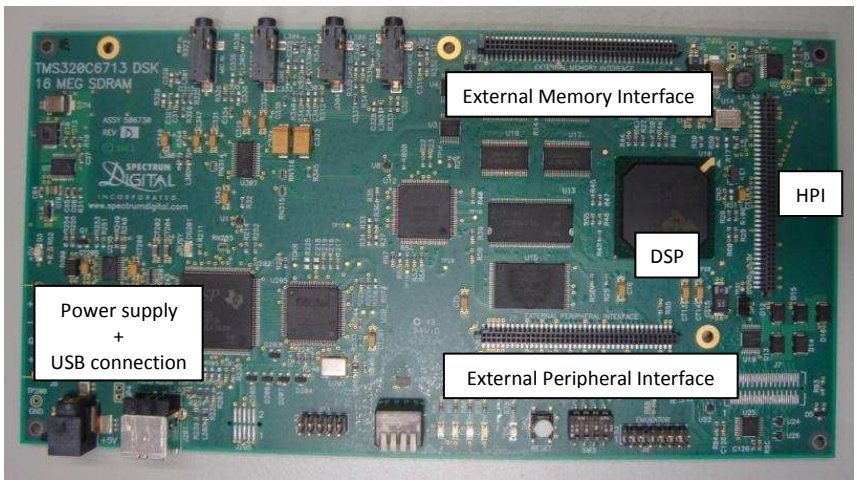


Fig. 7.14 C6713 DSK board.

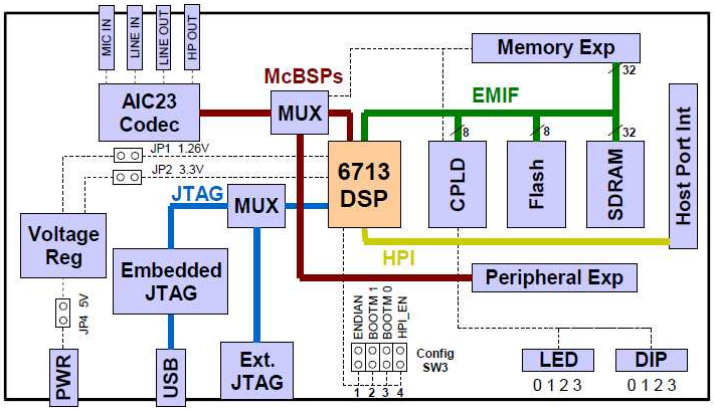


Fig. 7.15 Diagram of the C6713 DSK board [31].

The DSP can be programmed by using Code Composer Studio (CCS) from Texas Instruments. In this work, this software is utilised to develop and compile the control program (C language), which is loaded into the DSK board by employing an HPI daughter card, which is described in the next section, and MATLAB.

In order to ensure the entire control program could run within an interrupt cycle (about 25μs), the DSP was programmed to operate at 350MHz, i.e. it is overclocked.

7.4.2 HPI card

The HPI daughter card, developed by Educational DSP and shown in figure 7.16, allows the control program to be loaded into the DSK board and the reading/writing of variables when the control program is running from a PC via a USB connection. In this work, MATLAB is used to monitor the system via the HPI card by implementing an interface which is described later in section 7.10.

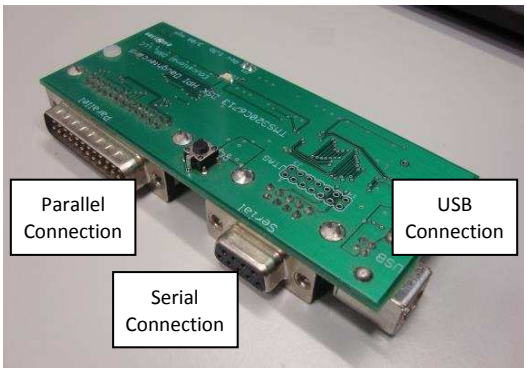


Fig. 7.16 HPI card.

7.4.3 FPGA board

The FPGA board, developed by the PEMC Group of the University of Nottingham for use in power electronics applications, is depicted in figure 7.17. This card is based on an ACTEL ProASIC3 A3P400 FPGA. This board is mainly characterised by:

- 50MHz clock.
- 10 12-bit A/D channels (conditioning and protection circuits).
- 2 high-density connectors (26-pin and 30-pin) for digital inputs/outputs.
- 10 inputs/outputs through fibre optic or current mirrors.

The communication between the DSK board and the FPGA card is carried out through the DSK 80-pin EMIF connectors (memory expansion connector and peripheral expansion connector). These connectors allow a daughter card to have access to the DSP data and address buses, power supply, reading/writing control signals, timers, clocks and interrupts.

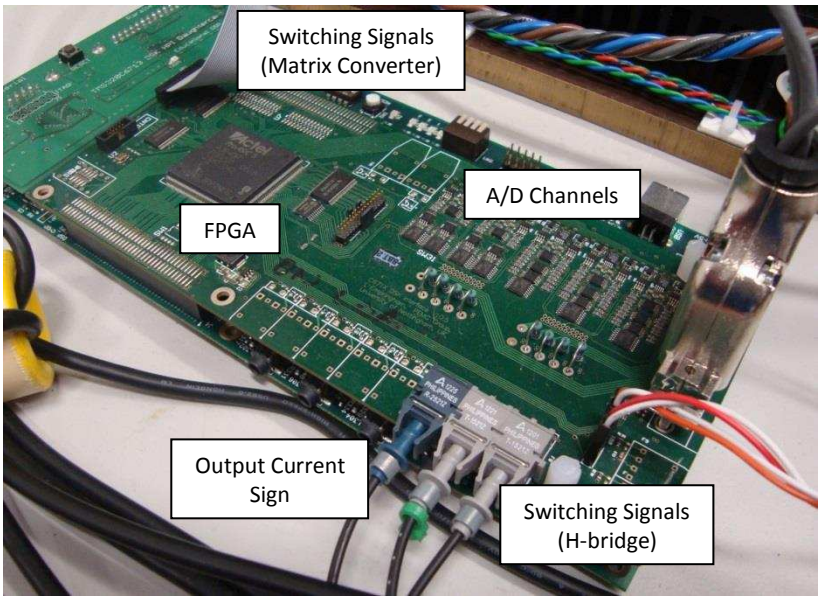


Fig. 7.17 FPGA board.

Particularly in this work, the FPGA board generates an interrupt at a frequency defined by the resonant tank in order to achieve ZCS operation. This interrupt drives the routine (DSP program) which contains the control algorithm.

7.5 Resonant tank

The resonant tank, shown in figure 7.18, consists of two elements: the tank capacitor and the tank inductor. The tank capacitor, whose required capacitance value corresponds to 70nF, is composed of five 350nF (±10%) $500V_{ac}/1500V_{dc}$ capacitors

connected in series. These capacitors were designed and manufactured by ICW Capacitors as required, and are characterised by their low losses and low inductance. With respect to the tank inductor, the required inductance value for a resonant frequency of about 20kHz was 905μH. This inductor was designed and built by using an EPCOS UU-93/152/30 soft ferrite core and litz wire. The final measured values (at 20kHz) of the tank resonant components are 72.54nF and 929.6μH, respectively.

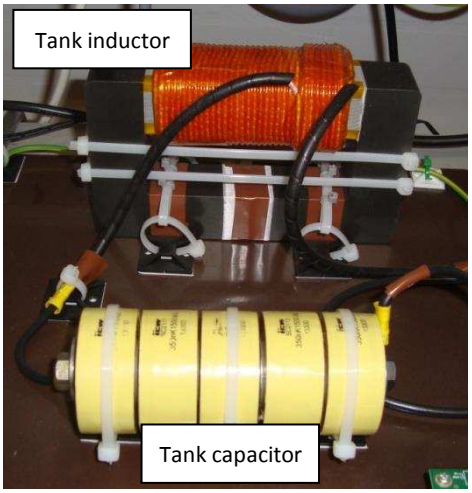
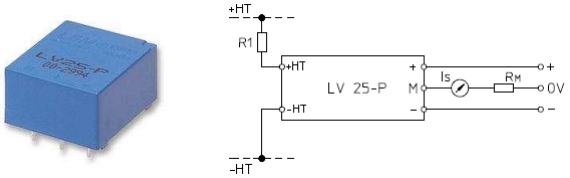


Fig. 7.18 Resonant tank.

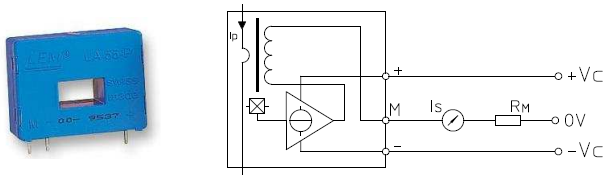
7.6 Voltage and current measurements

To measure the voltages and currents which are needed to implement the control algorithm, LEM transducers LV25-P (voltage) and LA55-P (current), shown in figures 7.19 and 7.20, are used. The nominal values for both transducers are 500V and 50A, respectively. The converter input voltages (input capacitor voltage) are measured by three transducers placed in the matrix converter, whilst the supply voltages and currents are measured using a PCB based circuit depicted in figure 7.21. The H-bridge capacitor dc voltage is measured by employing an available PCB voltage measurement board (previously used in other systems). Another measurement board, which is described later, has been designed to measure the magnitude of the high frequency output current.



(a) (b)

Fig. 7.19 LV25-P voltage transducer: (a) transducer and (b) connection diagram.



(a) (b)

Fig. 7.20 LA55-P current transducer: (a) transducer and (b) connection diagram.

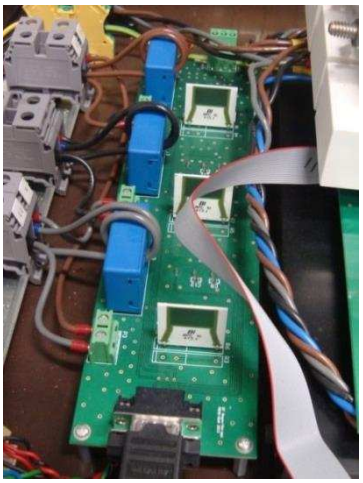


Fig. 7.21 Supply voltage/current measurement board (voltage transducers are underneath).

7.6.1 Output current magnitude measurement

To measure the magnitude of the high frequency output current, a PCB board was designed. This board is shown in figure 7.22 and consists of the following elements:

- A current transducer to measure the output current.
- A rectification stage.
- A Notch filter (designed to filter frequencies about 40kHz).
- A low-pass filter (cut-off frequency of 10kHz).
- Output current sign detection circuit.

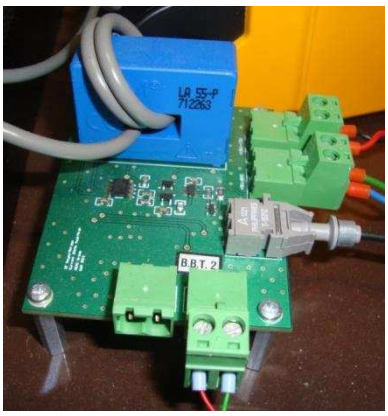


Fig. 7.22 Output current measurement board.

In order to avoid using a low-pass filter with a relative low cut-off frequency, and, as a consequence, losing information about the variation of the output current magnitude, a filtering scheme with two filters was implemented. The Notch filter is used to attenuate the high frequency component, then, the low-pass filter allows obtaining the average value, leading to the peak value of the output current. Since the high frequency component (about 40kHz) is reduced by the Notch filter, a cut-off frequency of 10kHz for the low-pass filter was selected. In addition, a circuit to detect the sign of the output current was also implemented in this board. This circuit is based on a very fast comparator ADCMP600 and the digital output sign signal is sent to the FPGA card via fibre optic. To implement the rectification stage and the active filters, operational amplifiers ADA4000 (single and dual) were utilised. Figures 7.23 and 7.24 show the schematic diagrams of the circuits included in this board.

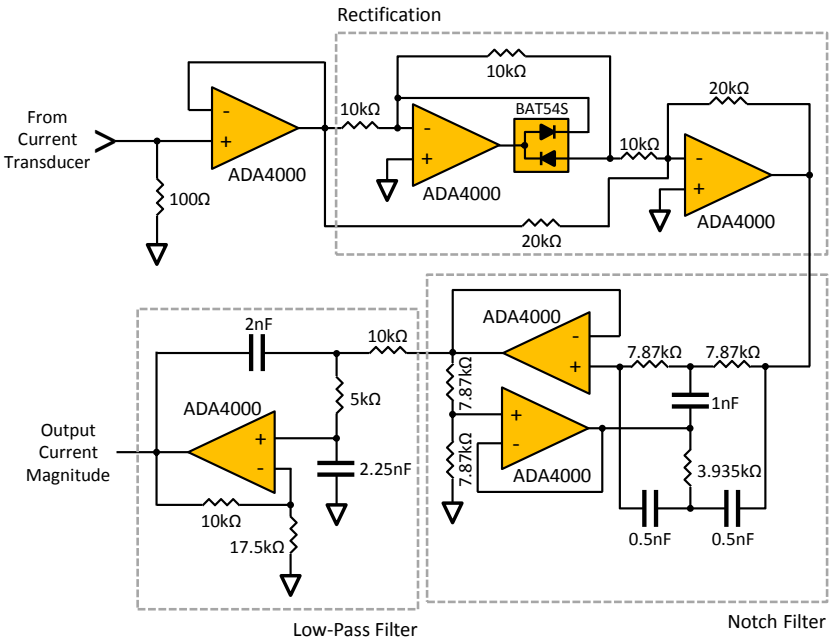


Fig. 7.23 Schematic diagram of the output current magnitude measurement circuit.

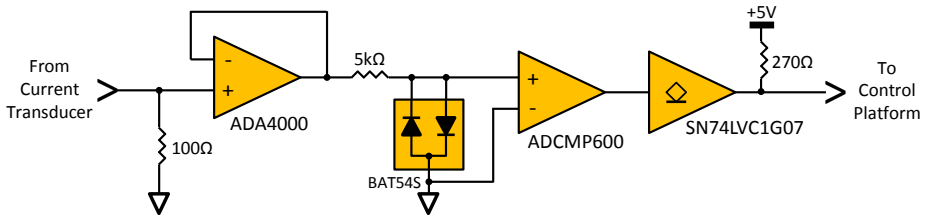


Fig. 7.24 Schematic diagram of the output current sign detection circuit.

7.7 Autotransformer and load

A 415V/10A three-phase autotransformer is used and the load is composed of three HVR Pentagon 57Ω/1kW high-power resistors connected in parallel, resulting in a total resistance of 19Ω/3kW. The autotransformer and the load resistors are shown in figure 7.25.

(a) (b)

Fig. 7.25 (a) Autotransformer and (b) load resistors.

7.8 Control program

The control program is developed and compiled in Code Composer Studio and can be divided into two main sections: initialisation and interrupt routine.

7.8.1 Initialisation

The initialisation includes the declaration of variables, switching vectors definition and the configuration values related to the FPGA board, such as interrupt frequency, commutation time for the matrix converter (four-step commutation strategy) and control of the A/D conversion.

7.8.2 Interrupt routine

This routine, which is driven by the interrupt signal generated by the FPGA board, contains the main code section of the control program. This code includes A/D channels reading, filtering of the supply voltage, the predictive control algorithm and a data storage routine. A flowchart of the interrupt routine is depicted in figure 7.26.

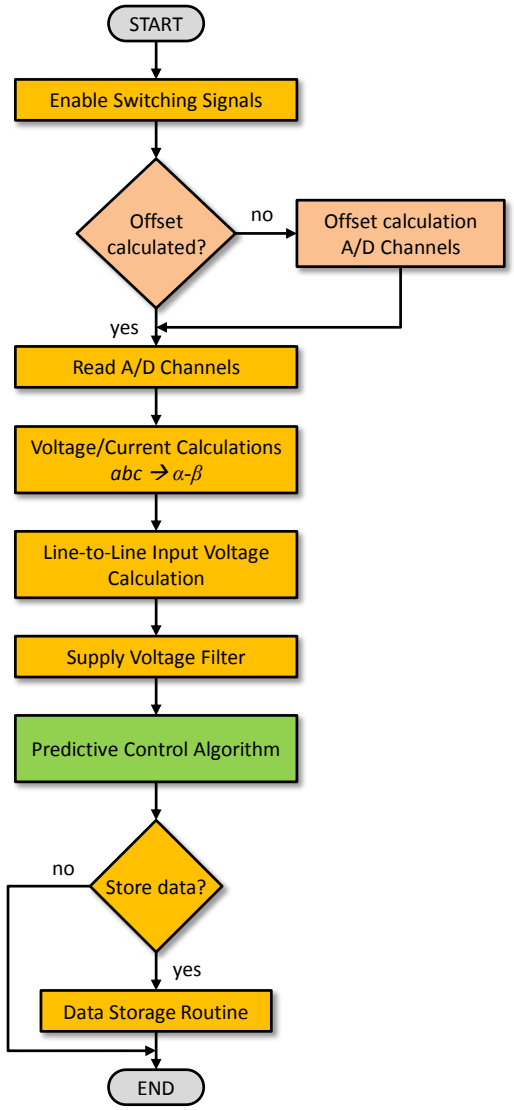


Fig. 7.26 Flowchart of the interrupt routine.

7.8.2.1 A/D channels offset calculation

Before reading the A/D channels from the DSK, a number of interrupt cycles are utilised to calculate the offset for each channel. Thus, when every offset is obtained, the entire interrupt routine is performed.

7.8.2.2 Supply voltage filtering

In order to calculate the phase of the supply voltage, a filter designed in the d-q axis (rotating frame) is employed. This filter corresponds to a low-pass filter applied to the d-q voltage components, thus, avoiding the generation of a phase shift between the original signal and the filtered one. A cut-off frequency of 25Hz was selected for the low-pass filter. Moreover, the filtered supply voltage is used in the predictive control

algorithm to prevent the voltage distortion affecting the algorithm calculations. A diagram of the supply voltage filter is shown in figure 7.27.

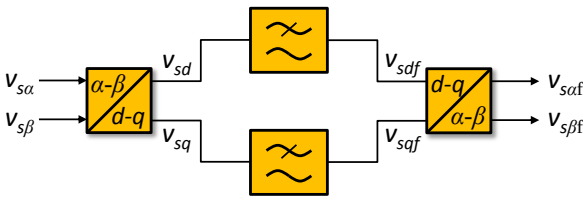


Fig. 7.27 Diagram of the supply voltage filter.

7.8.2.3 Predictive control algorithm

This code section within the interrupt routine corresponds to the predictive control algorithm described in chapter 6. This contains the prediction equations, considering delay compensation, and the optimisation process. The minimisation of the cost function selects a switching vector which is stored in a FIFO register in the FPGA that is driven by the interrupt signal. A flowchart of this code section is shown in figure 7.28.

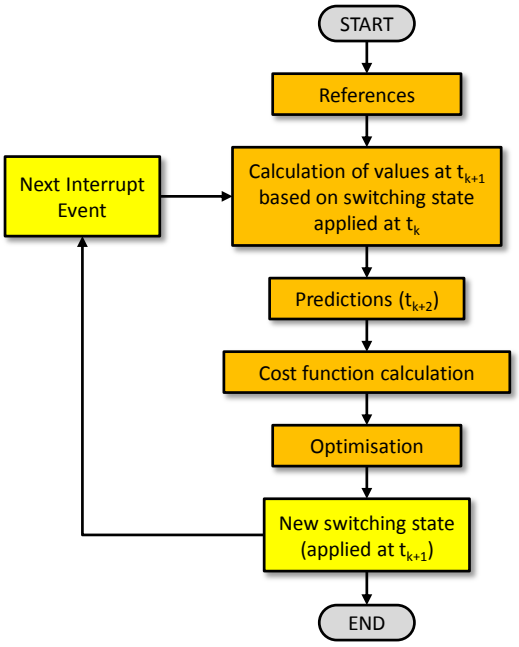


Fig. 7.28 Flowchart of the predictive control algorithm.

7.8.2.4 Data storage

To store data from the control program, a routine which utilises vectors of 10000 data values is implemented. These vectors can be transferred to MATLAB for monitoring the control program.

7.9 FPGA program

The program used is based on an FPGA program developed in the PEMC Group, University of Nottingham, for matrix converter applications. Modifications were made for this particular direct resonant converter.

The memory registers programmed in the FPGA are mapped into the CE2 region of the DSK external memory (EMIF CE2). This memory region is for use with daughter cards and comprises the hexadecimal address range A000 0000-AFFF FFFF. To communicate with the DSP, the FPGA program uses the address bus (only seven bits, EA[8:14]), the 32-bit data bus (ED[0:31]), the chip enable 2 signal (CE2), the asynchronous output enable signal (AOE), the asynchronous write enable signal (AWE) and the asynchronous read enable signal (ARE).

Different processes/blocks are programmed in the FPGA, such as a FIFO memory for switching signals generation (originally used to implement space vector modulation), an interrupt timer (to generate the interrupt signal), A/D conversion block (to transform the serial data from the A/D converters into 12-bit numbers), and the four-step commutation block (to implement the commutation strategy for the matrix converter). A schematic diagram of the FPGA program is depicted in figure 7.29, where VSAB, VSBC and VSCA are voltage sign signals.

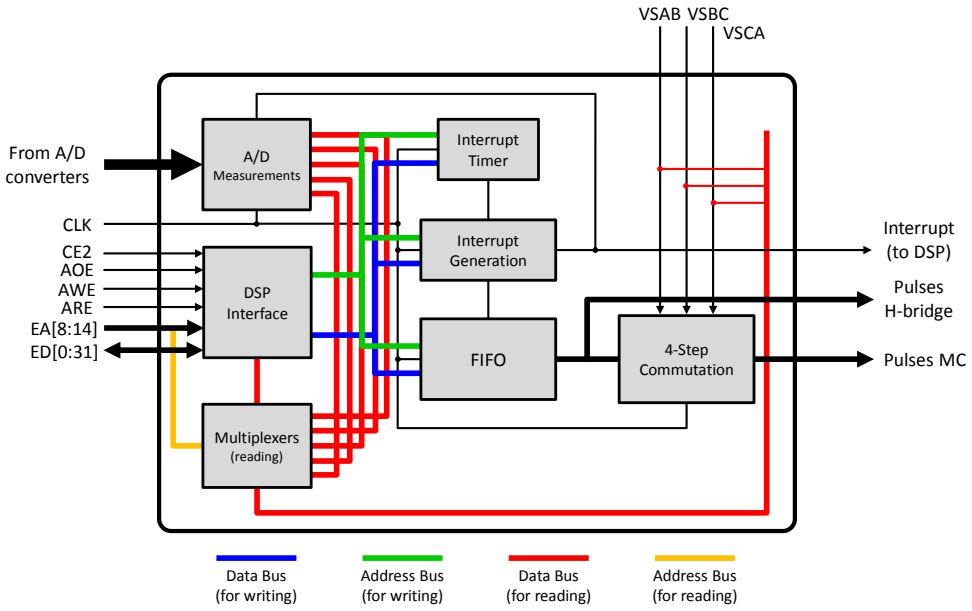


Fig. 7.29 Schematic diagram of the FPGA program.

7.10 MATLAB Interface

A MATLAB interface, shown in figure 7.30, was developed in order to operate the system. This interface allows modifying reference values, control strategy and plotting different waveforms. The data transference from/to the DSK board is carried out by the HPI card as previously explained. To load the program and read/write variables, a set of functions (C8X_DEBUG), developed by Educational DSP, is used.

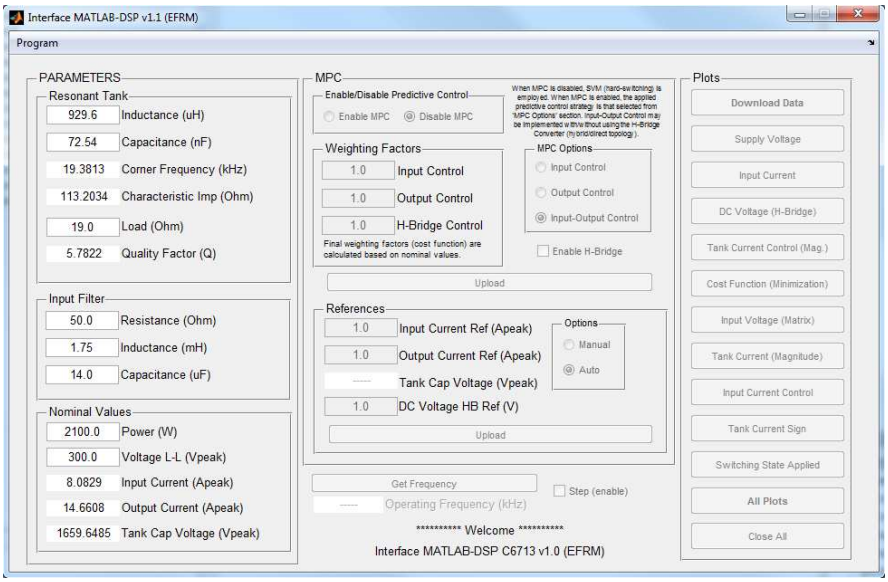


Fig. 7.30 Matlab interface.

7.11 Summary

The entire experimental system used to implement a direct series resonant converter with output voltage compensation has been described in this chapter. The power converters, the control platform, the resonant tank and the measurement boards have been described. Hence, emphasis has been placed on the main circuits included in each component (gate drives, sign detection, filters, etc.) as well as on the DSP and FPGA programs utilised to validate the proposed control strategy.

Chapter 8

Experimental Results

8.1 Introduction

This chapter presents the results obtained with the experimental system described in chapter 7 in order to validate the proposed converter and the control strategies. The parameters of the system correspond to those previously given in tables 5.2 and 6.3.

In this chapter, the selection of the weighting factor for the compensation voltage control, as discussed in chapter 6, is experimentally demonstrated. With regard to the experimental results, waveforms for the DSRC with voltage compensation operating at nominal conditions are presented. In addition, although this research focuses on the steady-state operation of the converter, results considering a step change reference for the output current and compensator capacitor voltage are shown in order to verify the control responses.

Finally, experimental results for the DSRC without voltage compensation are presented and an estimate of the converter efficiency is calculated.

8.2 Selection of the weighting factor λ_{hb}

In order to select the weighting factor related to the control of the voltage compensator, experimental results for different values of λ_{hb} were obtained. Then, the RMS error of the output current, input current and compensator capacitor voltage were calculated. Figure 8.1 depicts the RMS error against λ_{hb}, where the initial value corresponds to $\lambda_{hb} = 0$, i.e. without voltage compensation. The system is operated at

nominal current ($10A_{rms}$). Figure 8.2 shows the data in detail, where it can be seen that for $\lambda_{hb} = 0.25$ the error of the output current is minimised. Owing to the importance of the distortion at the output, this value was selected.

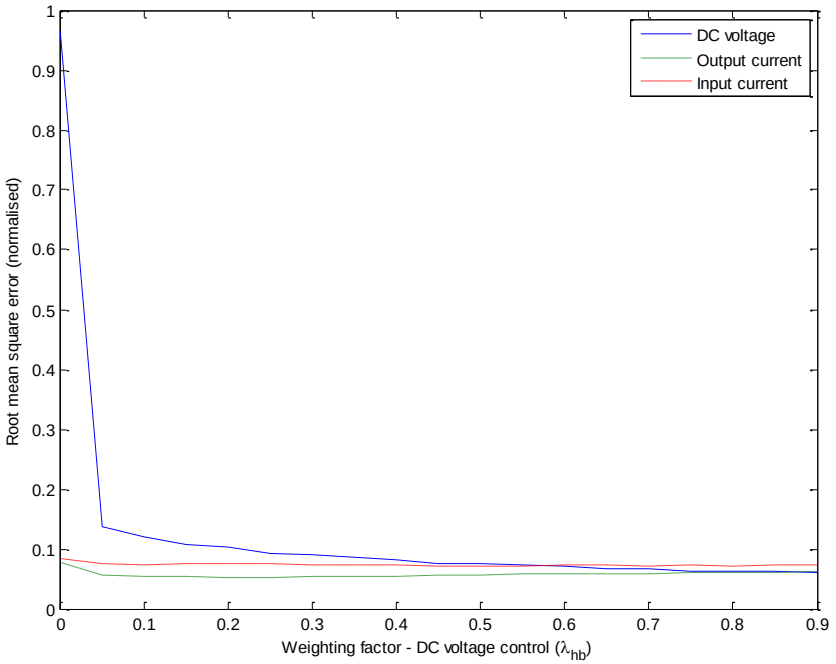


Fig. 8.1 RMS error against $\boldsymbol{\lambda_{hb}}$.

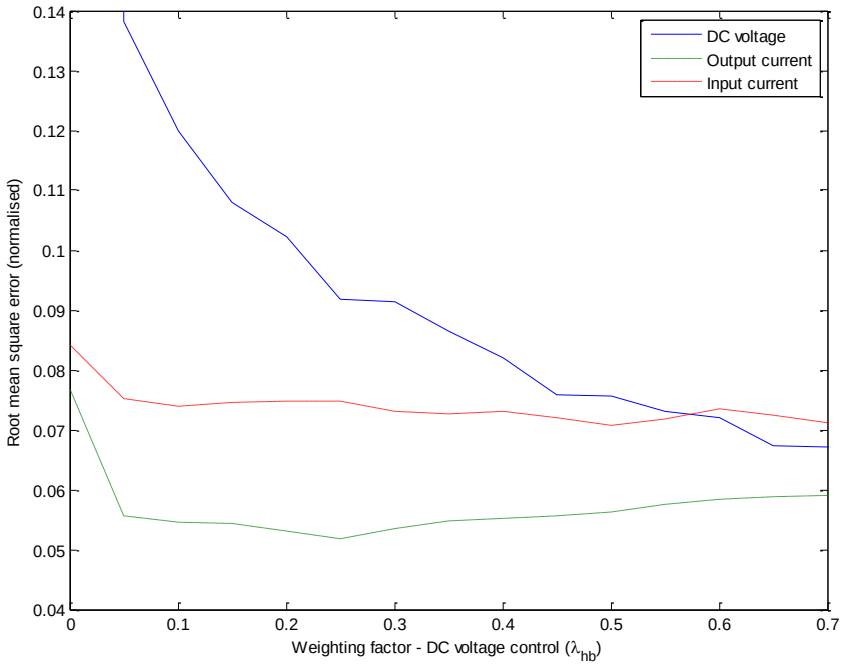


Fig. 8.2 RMS error against $\boldsymbol{\lambda_{hb}}$ (detailed).

8.3 Experimental results at nominal output current

Waveforms for the DSRC with output compensation operating at nominal current ($10A_{rms}$) are shown in figures 8.4-8.10. The high frequency waveforms were reconstructed using MATLAB and the data acquired via the control platform, such as input capacitor voltage, output current magnitude and switching state applied. Figure 8.3 explains the reconstruction concept considering the sinusoidal output current.

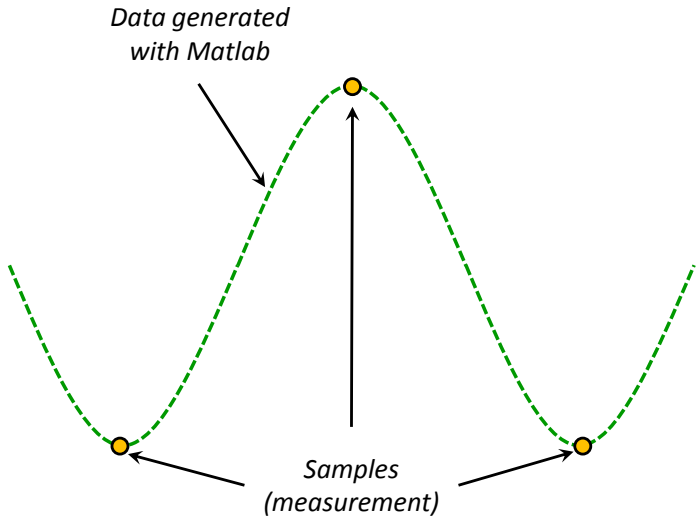


Fig. 8.3 Reconstruction concept: high frequency output current.

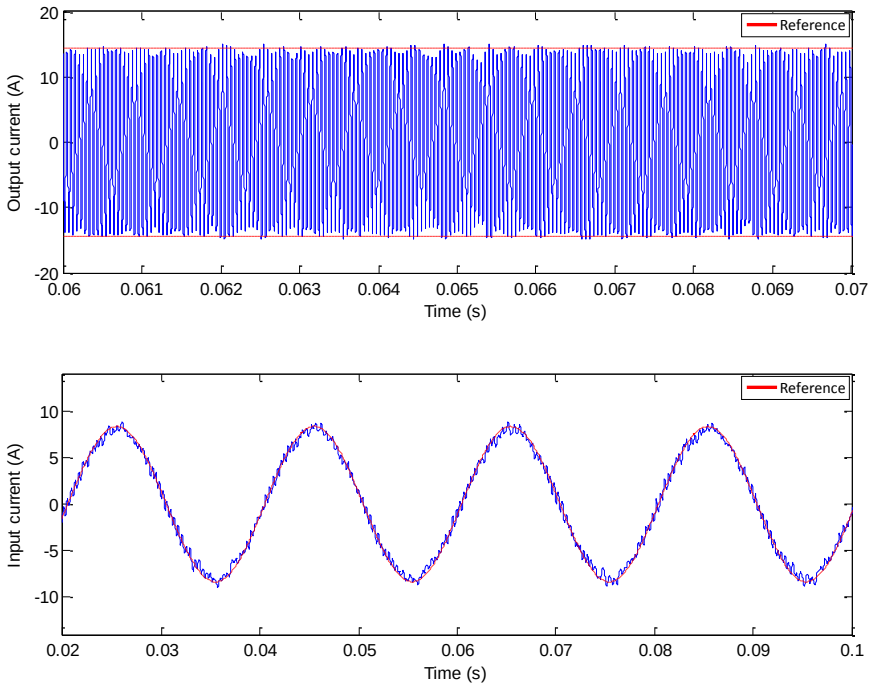


Fig. 8.4 Input and output current control (experimental).

Figure 8.5 shows the control of the output current (magnitude) and the compensator capacitor voltage. Figure 8.6 depicts input waveforms, input voltage and current, and also output waveforms, voltage applied to the resonant tank and tank current (load current).

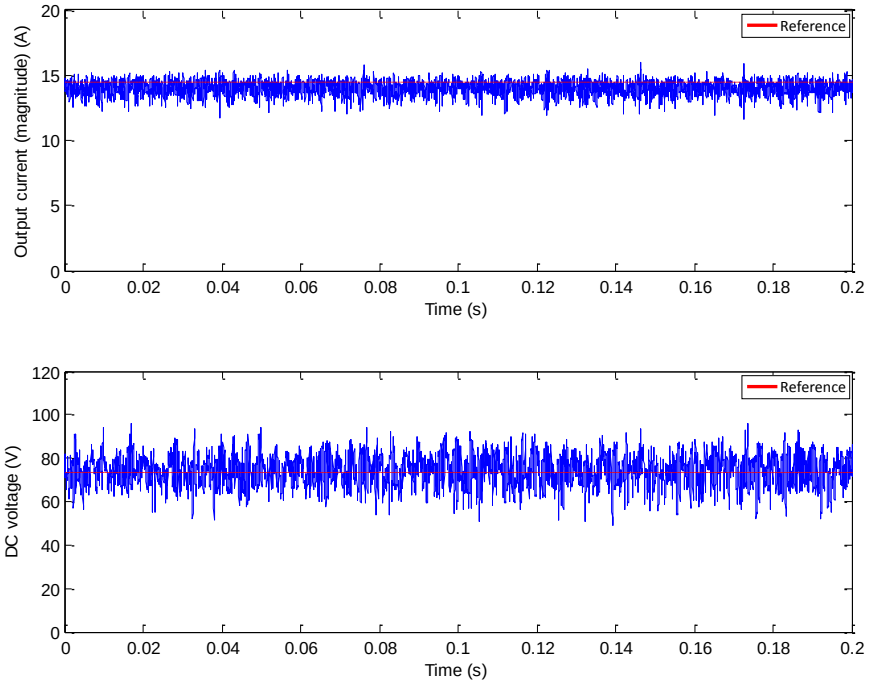


Fig. 8.5 Output current magnitude and compensator capacitor voltage control (experimental).

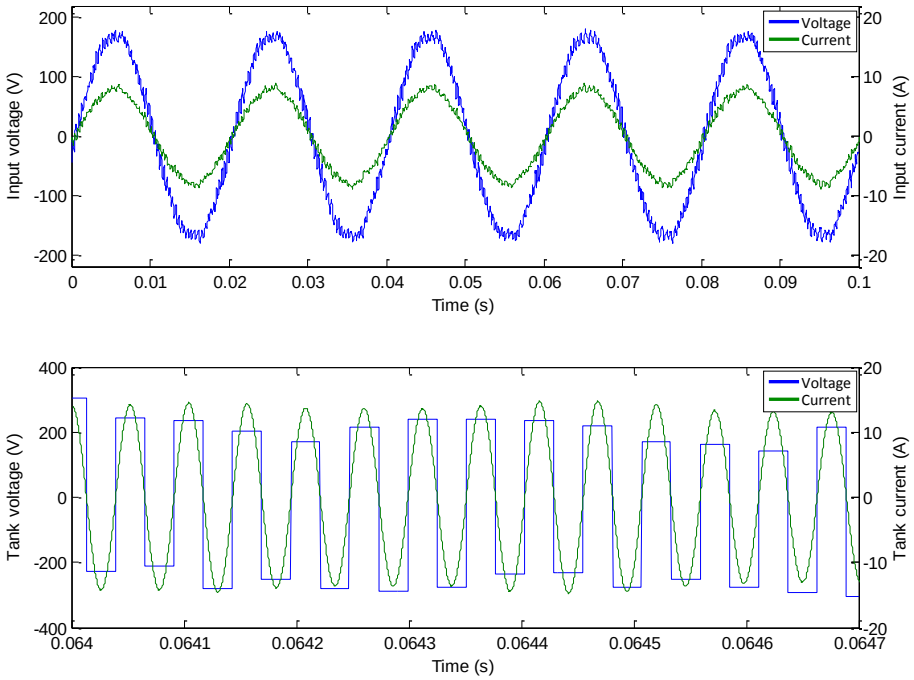


Fig. 8.6 Input voltage/current, voltage applied to the resonant tank and tank current (experimental).

In figure 8.7, the output matrix converter voltage, the compensator voltage and the voltage applied to the resonant tank are depicted. In order to observe the voltage compensation, figure 8.8 illustrates the magnitude variation of the matrix converter output voltage and the voltage applied to the resonant tank.

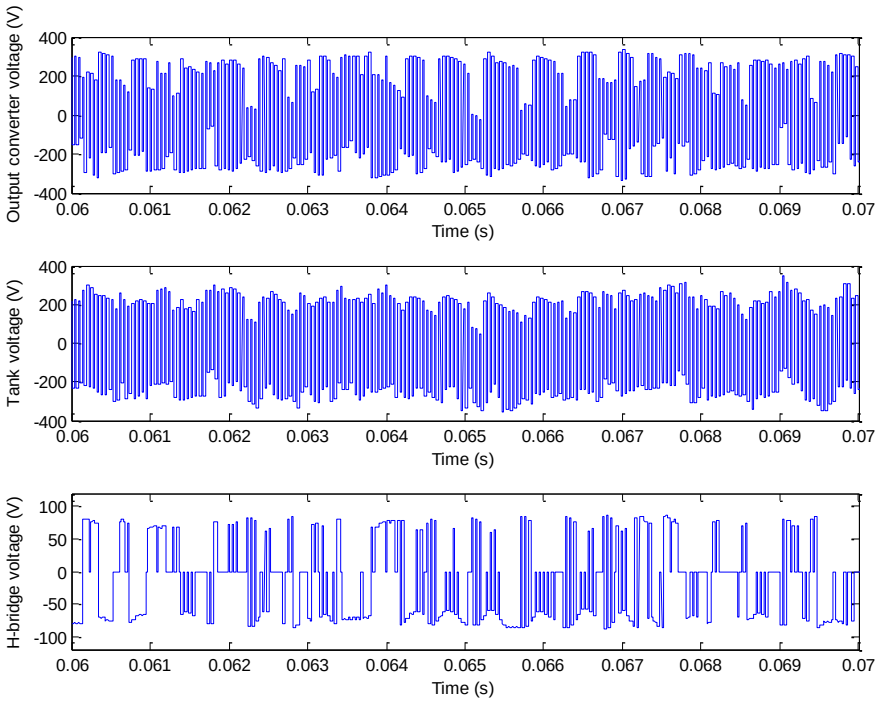


Fig. 8.7 Output matrix converter voltage, voltage applied to the resonant tank and output compensator voltage (experimental).

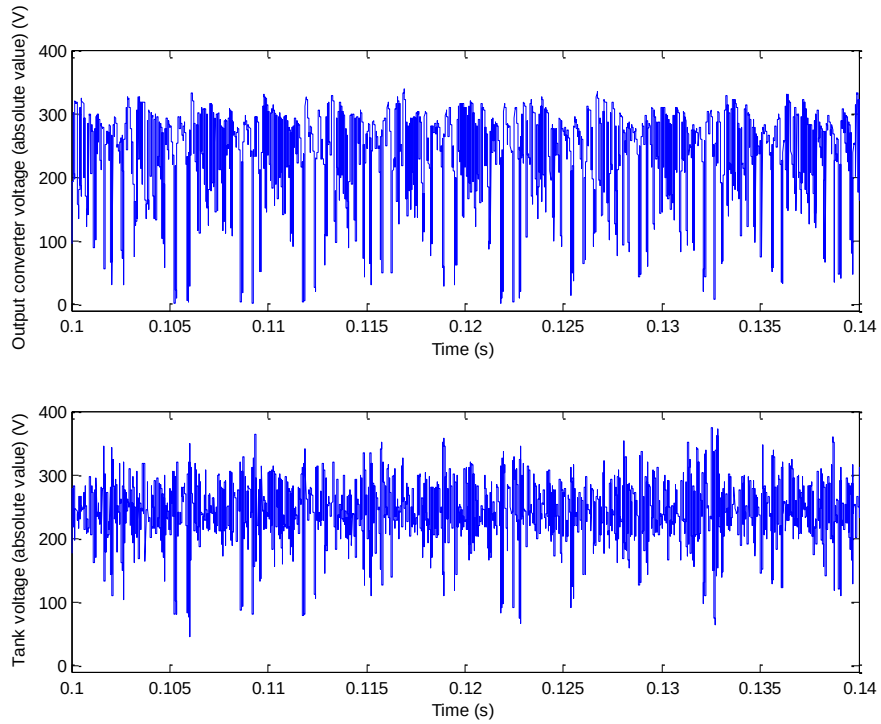


Fig. 8.8 Output matrix converter voltage and voltage applied to the resonant tank (magnitude variation) (experimental).

Figure 8.9 shows supply voltage, input capacitor voltage (input converter voltage) and supply current, whereas figure 8.10 shows the cost function value (result of the minimisation) and the switching state applied to the converter (matrix converter and compensator).

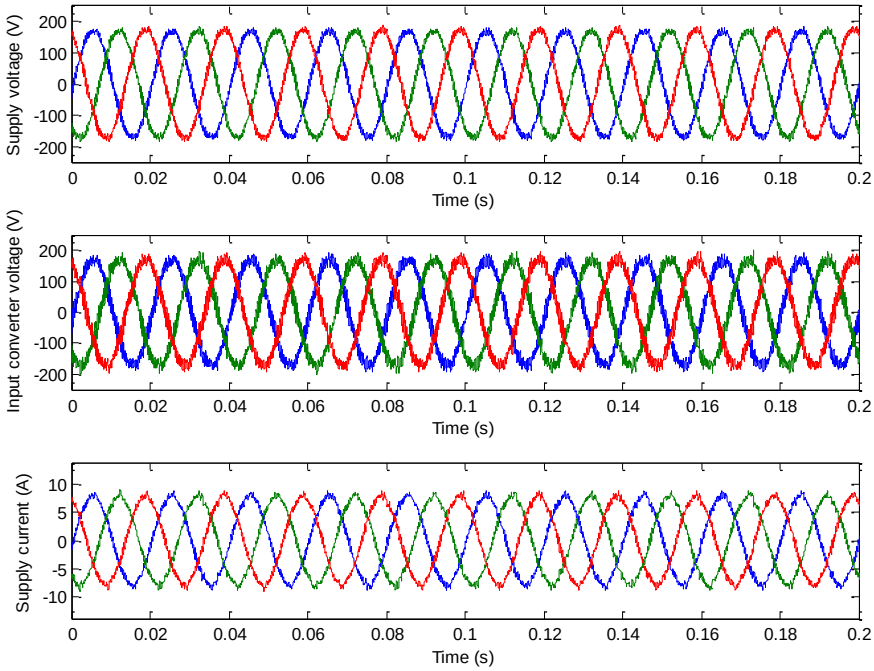


Fig. 8.9 Supply voltage, input capacitor voltage and supply current (experimental).

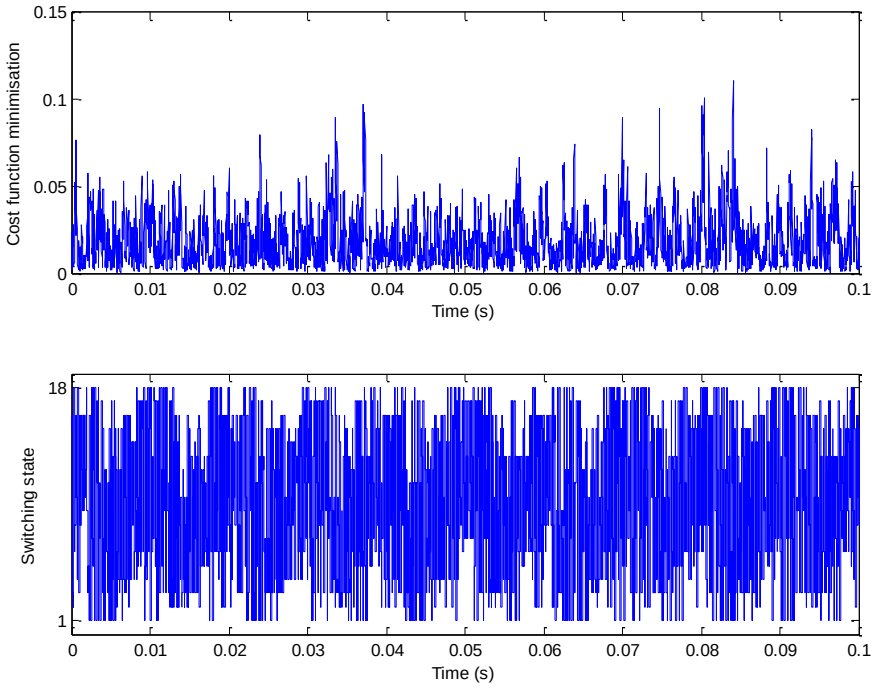


Fig. 8.10 Cost function minimisation (result of the optimisation) and switching state applied to the converter (experimental).

Figures 8.11-8.15 show waveforms for operation at nominal output current acquired from the oscilloscope utilised.

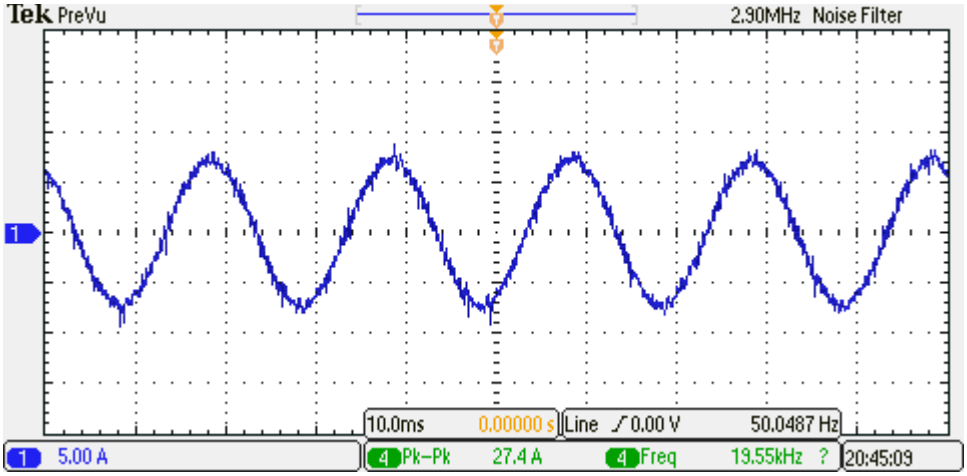


Fig. 8.11 Input current.

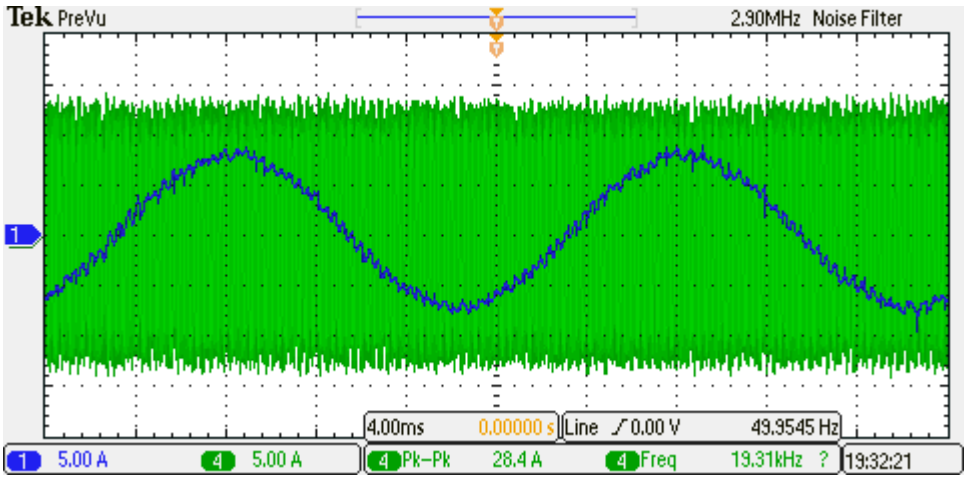


Fig. 8.12 Input and output current.

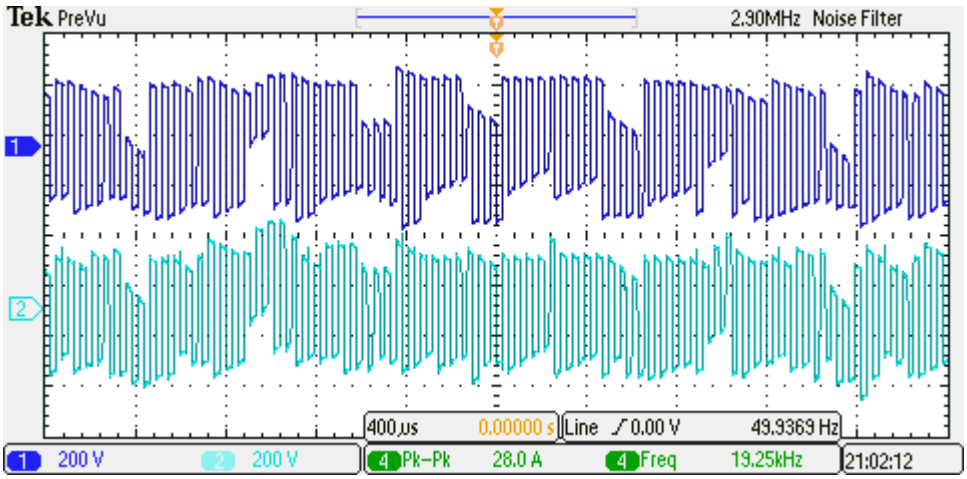


Fig. 8.13 Output matrix converter voltage (top) and voltage applied to the resonant tank (bottom).

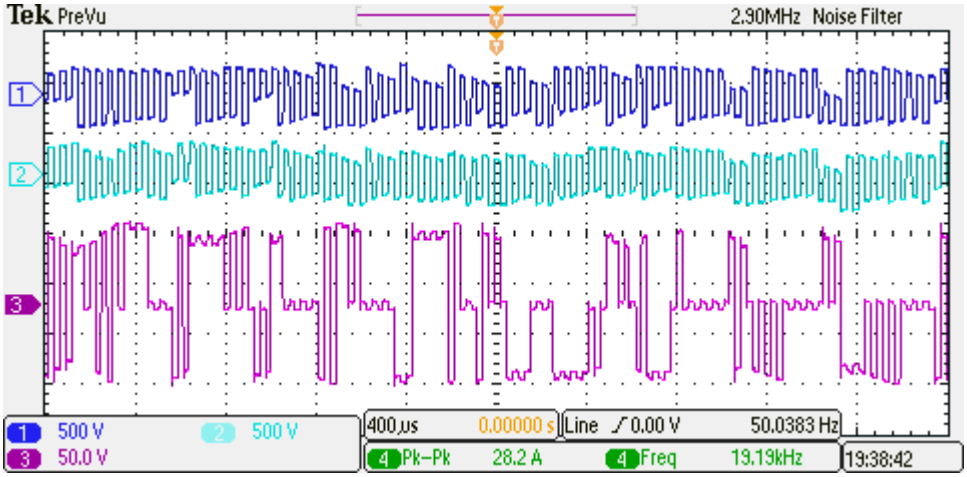


Fig. 8.14 Output matrix converter voltage (top), voltage applied to the resonant tank (middle) and output compensator voltage (bottom).

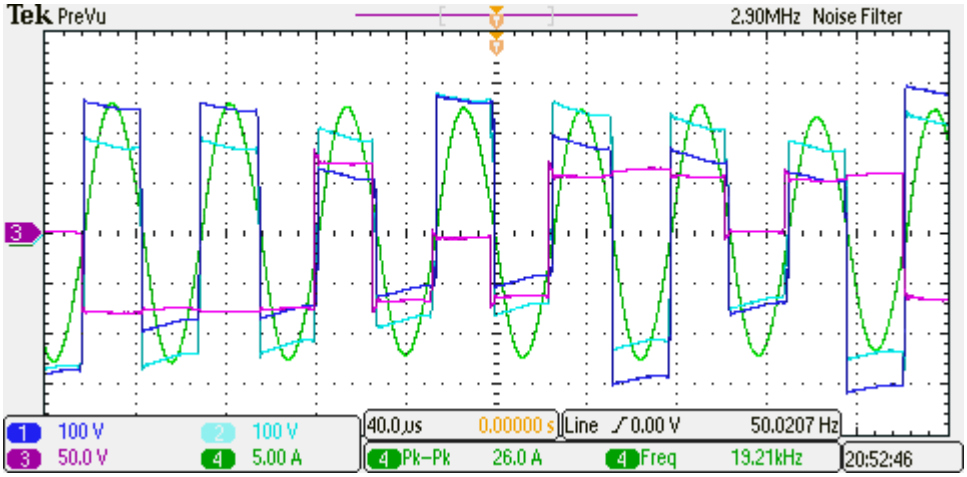


Fig. 8.15 Output matrix converter voltage (blue), output compensator voltage (purple), voltage applied to the resonant tank (cyan) and tank current (green).

In figures 8.4-8.15, correct operation of the DSRC with voltage compensation can be observed operating at nominal output current, achieving sinusoidal input and output current and unity power factor. In figures 8.7, 8.8, 8.13 and 8.15, the voltage compensation process can be seen. In addition, ZCS operation is evident in figure 8.15.

8.4 Control responses under step change references

In order to test the transient behaviour of the predictive control algorithm, step changes of the output current reference and the compensator capacitor voltage reference were utilised. In figures 8.16-8.19, the output current reference is varied, whereas the compensator capacitor voltage reference was changed in figures 8.20-8.23.

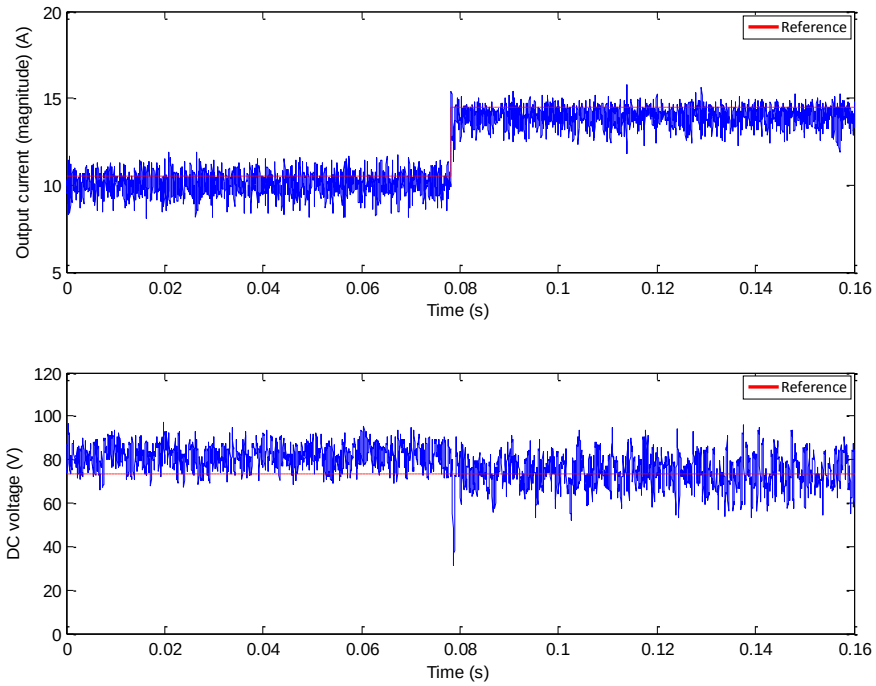


Fig. 8.16 Output current magnitude and compensator capacitor voltage control for a step change in the output current reference from 10.5A to 14.5A at time 0.078s (experimental).

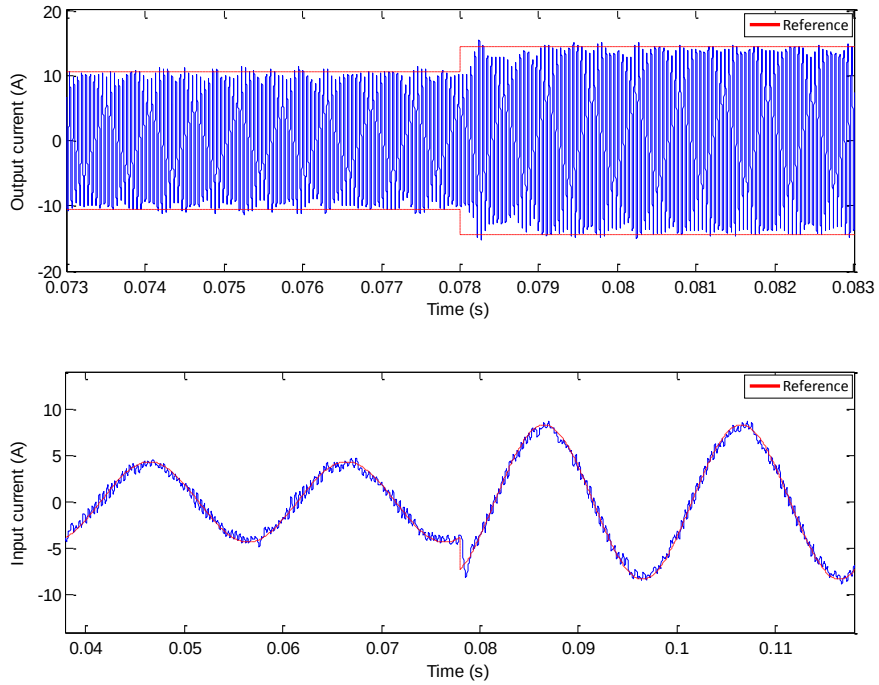


Fig. 8.17 Input and output control for a step change in the output current reference from 10.5A to 14.5A at time 0.078s (experimental).

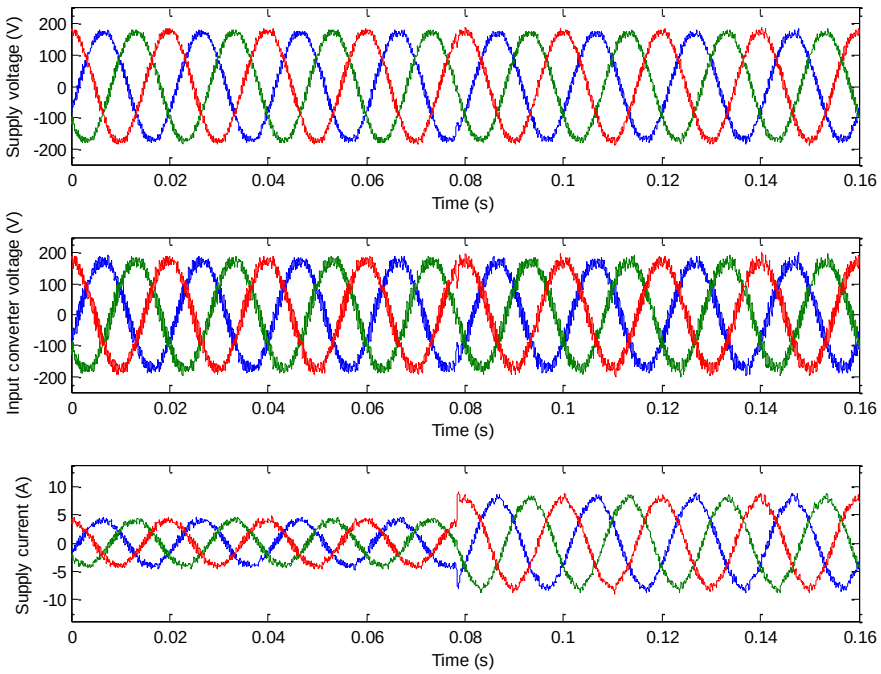


Fig. 8.18 Supply voltage, input capacitor voltage and supply current for a step change in the output current reference from 10.5A to 14.5A at time 0.078s (experimental).

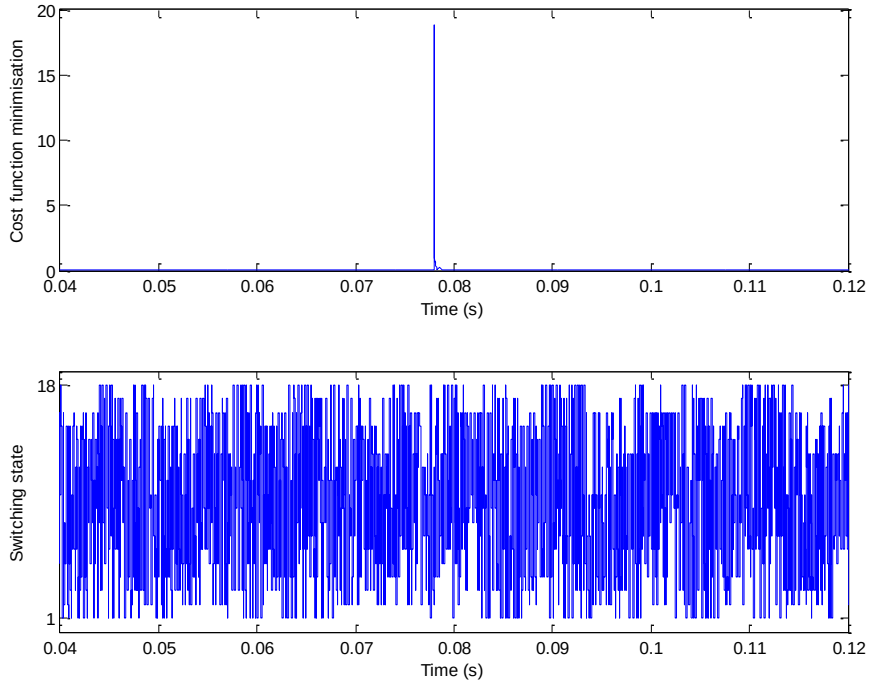


Fig. 8.19 Cost function minimisation and switching state applied to the converter for a step change in the output current reference from 10.5A to 14.5A at time 0.078s (experimental).

In figures 8.20-8.23, the compensator capacitor voltage reference is varied. Figure 8.20 shows the control response.

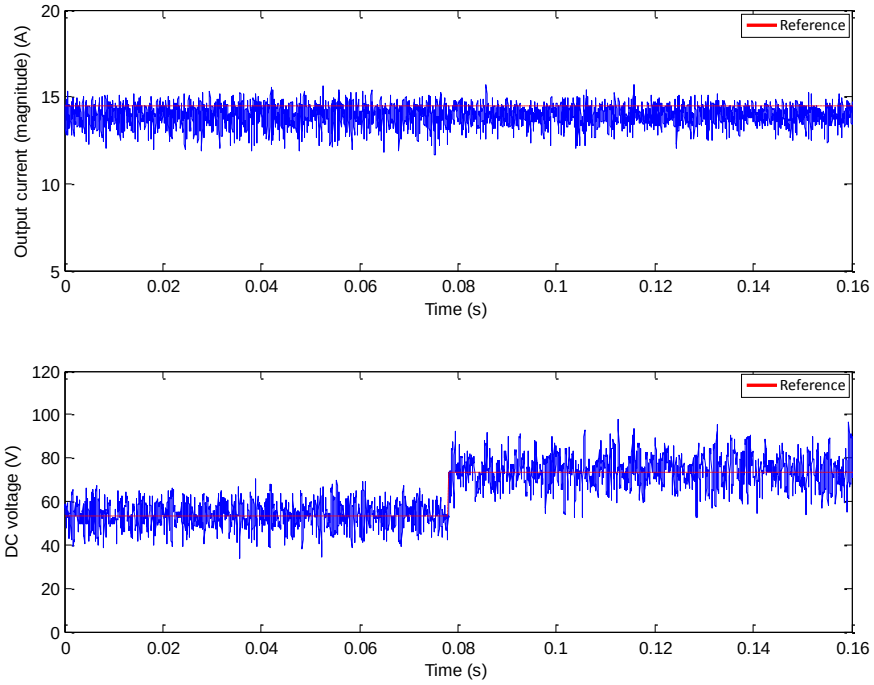


Fig. 8.20 Output current magnitude and compensator capacitor voltage for a step change in the compensator capacitor voltage reference from 53.5V to 73.5V at time 0.078s (experimental).

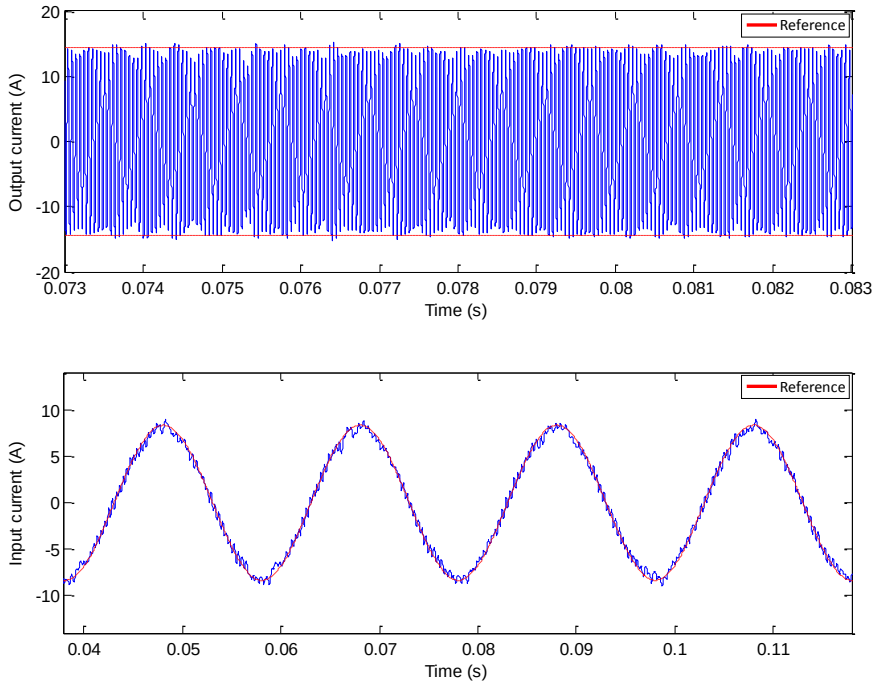


Fig. 8.21 Input and output current control for a step change in the compensator capacitor voltage reference from 53.5V to 73.5V at time 0.078s (experimental).

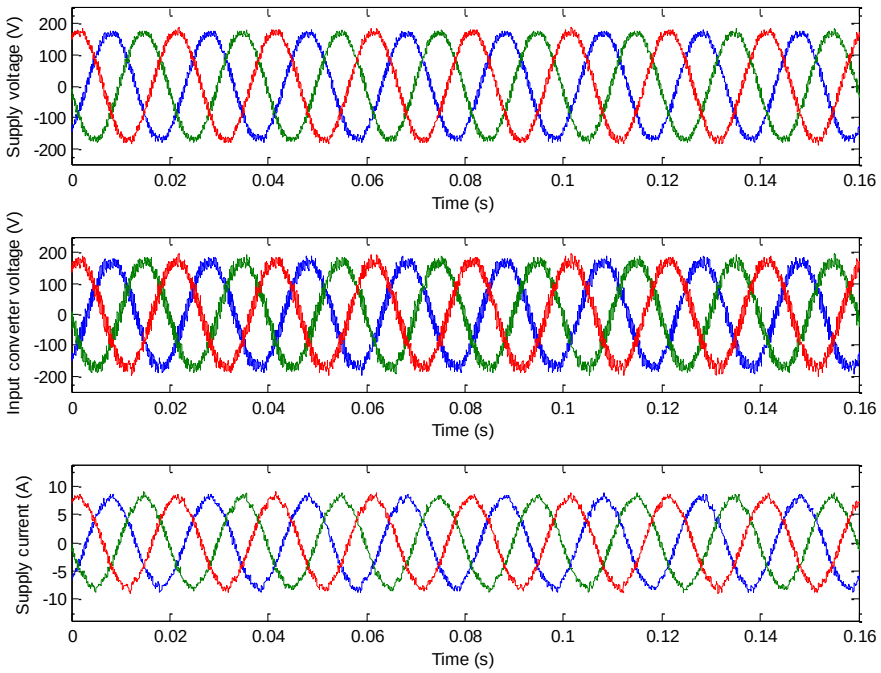


Fig. 8.22 Supply voltage, input capacitor voltage and supply current for a step change in the compensator capacitor voltage reference from 53.5V to 73.5V at time 0.078s (experimental).

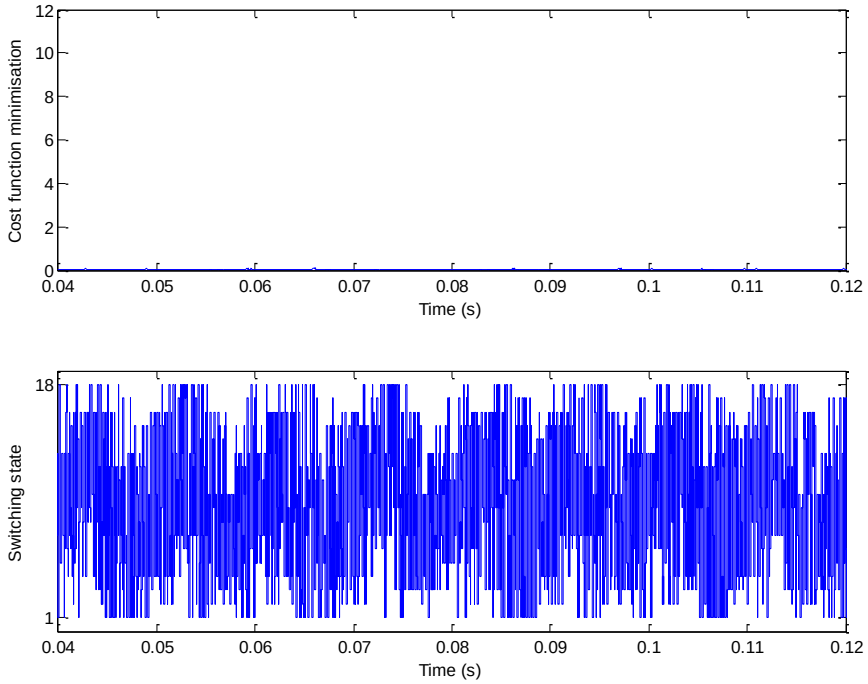


Fig. 8.23 Cost function minimisation and switching state applied to the converter for a step change in the compensator capacitor voltage reference from 53.5V to 73.5V at time 0.078s (experimental).

Since the compensator capacitor voltage depends on the output current, for a change in this current, the control algorithm modifies the switching of the H-bridge in order to regulate the compensator capacitor voltage. This action can be seen in figure 8.16.

On the other hand, when a change of the compensator capacitor voltage occurs, there is no significant effect on the output current control since the control algorithm regulates the compensator voltage via switching of the H-bridge converter. Furthermore, in figures 8.16-8.19, the effect of the different dynamics present in this converter topology (input filter, resonant tank and compensator capacitor) on the output current control can be observed. Moreover, the cost function minimisation for a step change of the compensator capacitor voltage is shown in figure 8.23 in order to compare this with figure 8.19. As seen in figure 8.23, the control algorithm does not need much effort to control the compensator capacitor voltage compared to that for the output current control (figure 8.19).

8.5 Effects of the converter overmodulation

As discussed in chapter 4, a DRC has the same limitations as a conventional matrix converter considering input current control, i.e. the voltage ratio is limited to 87% in order to achieve good quality input currents. Figures 8.24-8.27 show results for M_v≈87%. In figure 8.28, the low frequency distortion of the input current due to overmodulation can be observed.

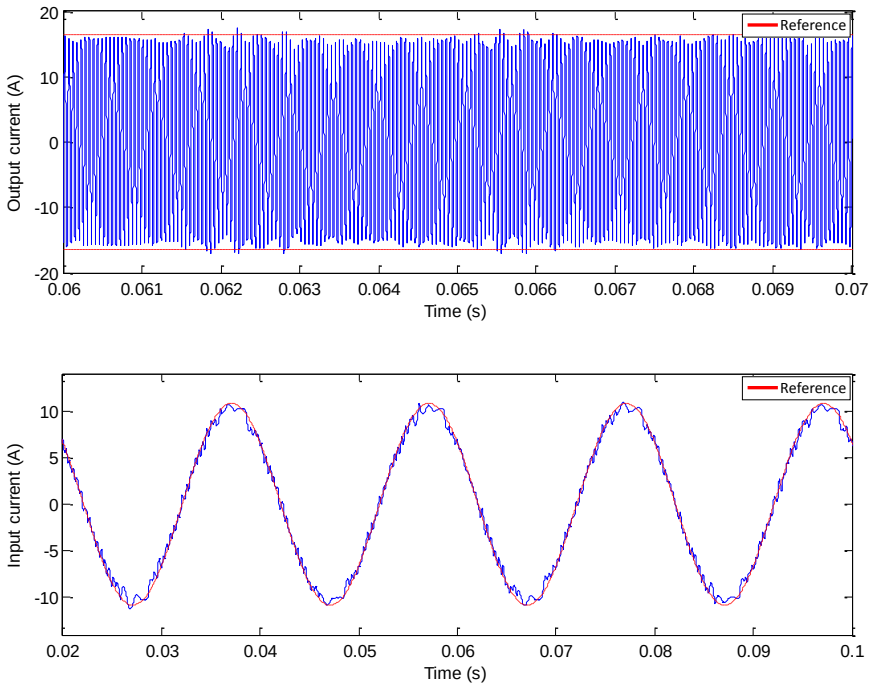


Fig. 8.24 Input and output current control for $\boldsymbol{M_v}$≈87% (experimental).

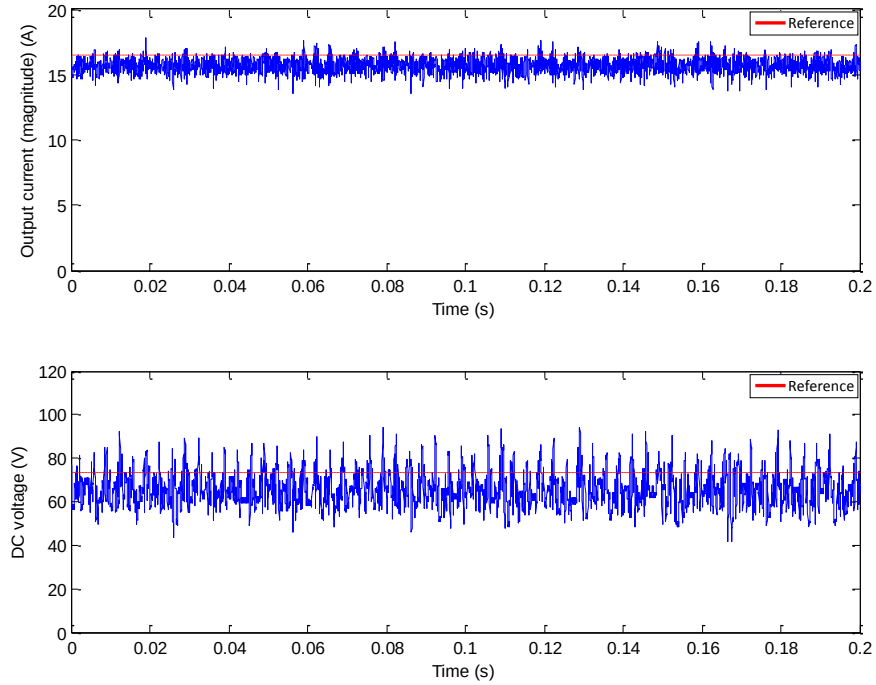


Fig. 8.25 Output current magnitude and compensator capacitor voltage control for $\boldsymbol{M_v}$≈87% (experimental).

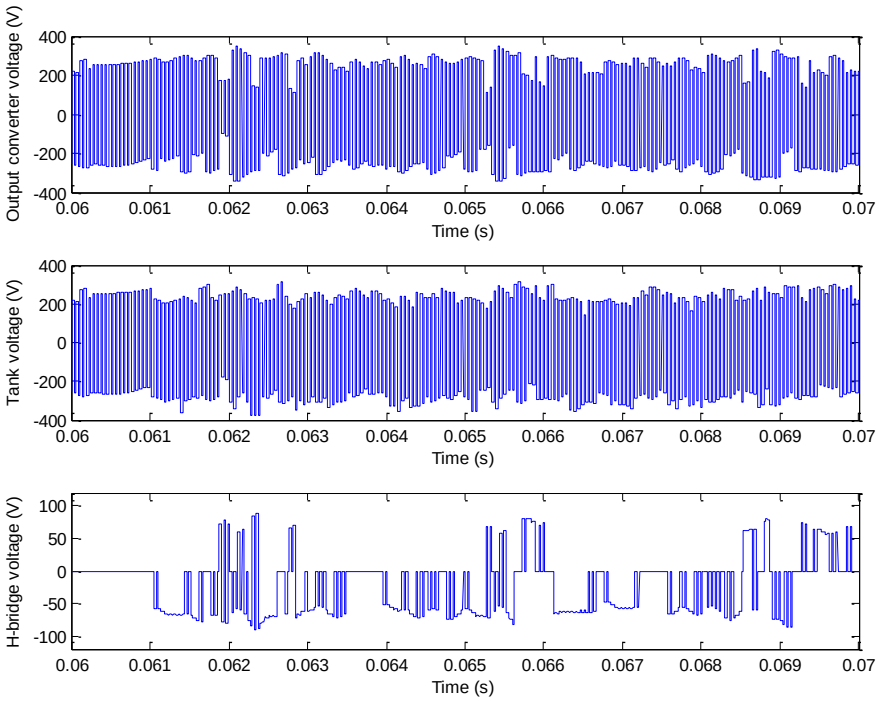


Fig. 8.26 Output matrix converter voltage, voltage applied to the resonant tank and output compensator voltage for $\boldsymbol{M_v}$≈87% (experimental).

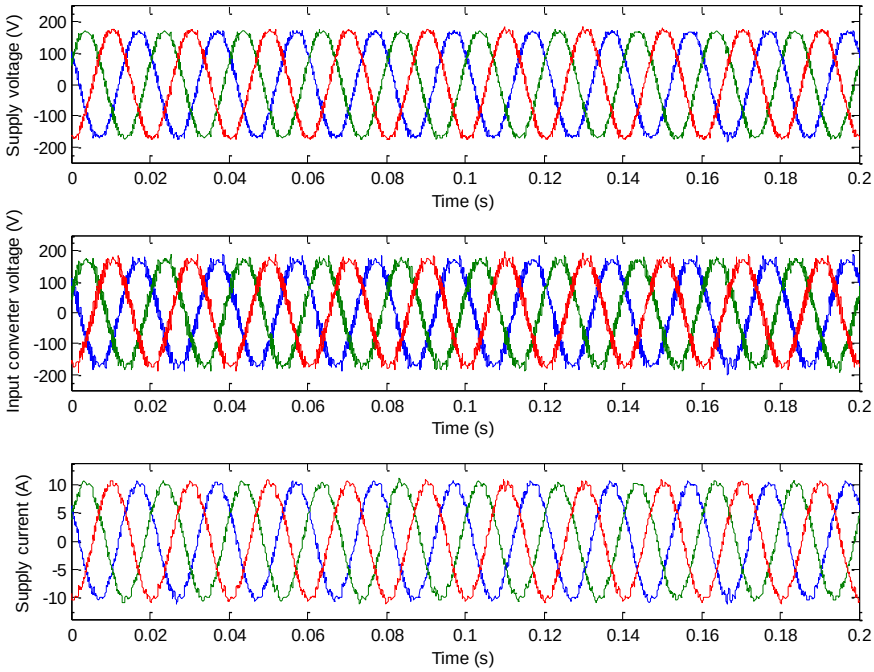


Fig. 8.27 Supply voltage, input capacitor voltage and supply current for M_v≈87% (experimental).

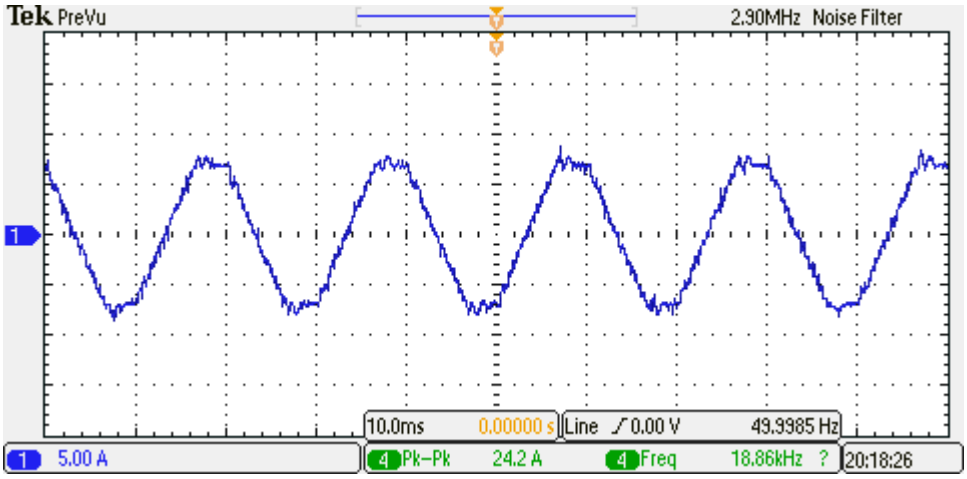


Fig. 8.28 Input current distortion owing to overmodulation.

8.6 Results without voltage compensation

Experimental results without voltage compensation are shown in figures 8.29-8.31. In this case, λ_{hb}=0 and the H-bridge is disabled, except for two permanently on switches which allow the current to flow between the matrix converter and the resonant tank.

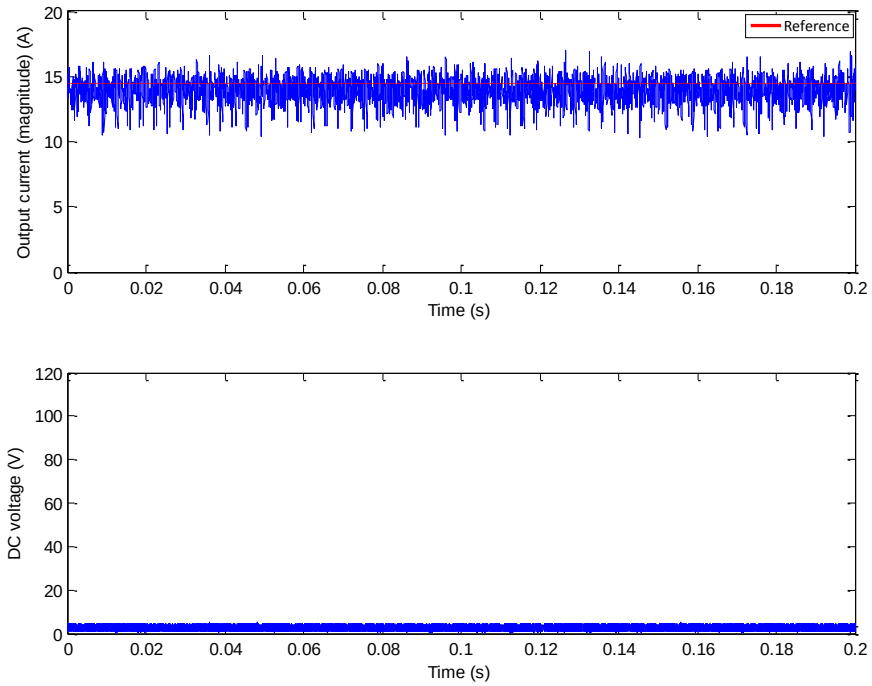


Fig. 8.29 DSRC without voltage compensation: output current magnitude and compensator capacitor voltage (experimental).

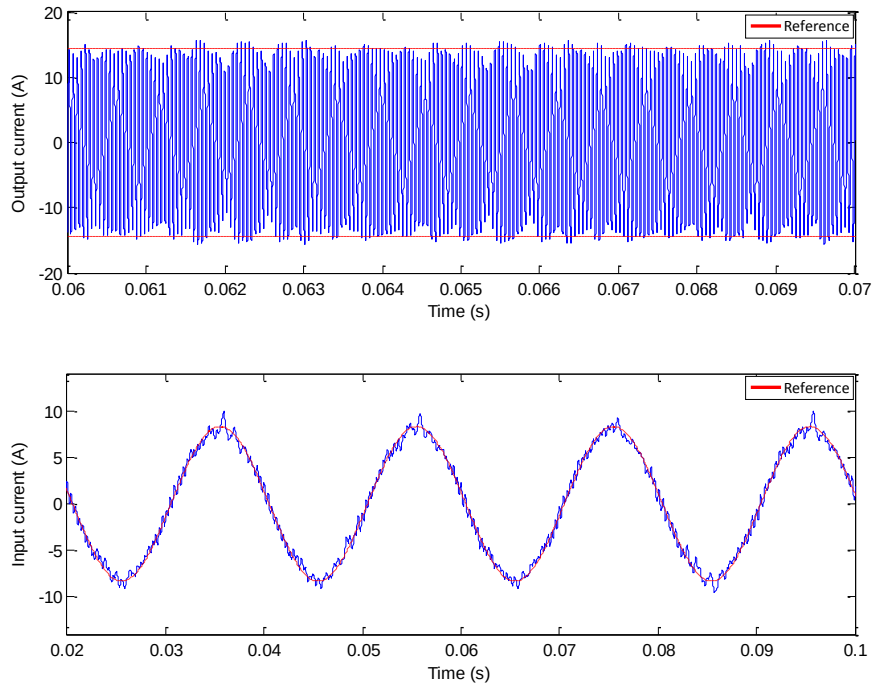


Fig. 8.30 DSRC without voltage compensation: input and output current control (experimental).

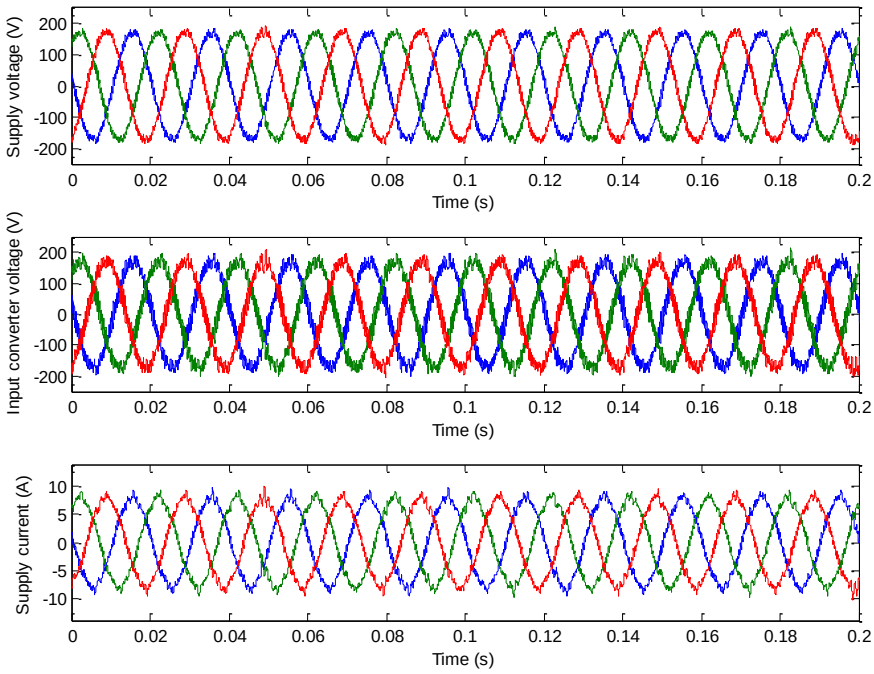


Fig. 8.31 DSRC without voltage compensation: supply voltage, input capacitor voltage and supply current (experimental).

In figure 8.32, the output current magnitude and input current without and with voltage compensation are shown. As can be seen, the distortion of the output current (magnitude ripple) is reduced by approximately 40%.

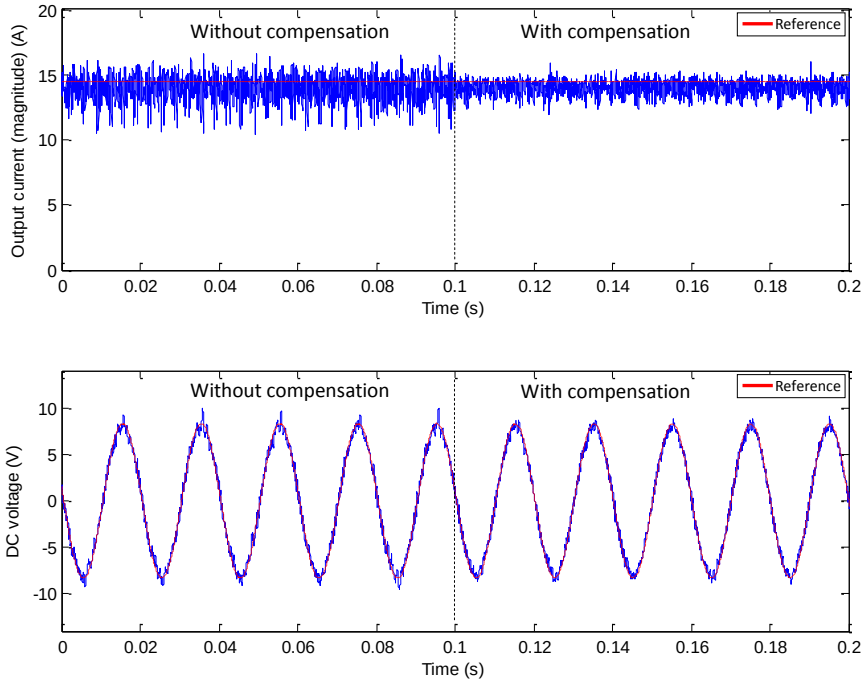


Fig. 8.32 DSRC without/with voltage compensation: output current magnitude and input current (experimental).

In figures 8.33 and 8.34, the frequency spectra of the input current for the DSRC with and without voltage compensation (respectively) are shown. The total harmonic distortion (THD) calculated, for both cases, corresponds to 2.7% (with compensation) and 4.4% (without compensation).

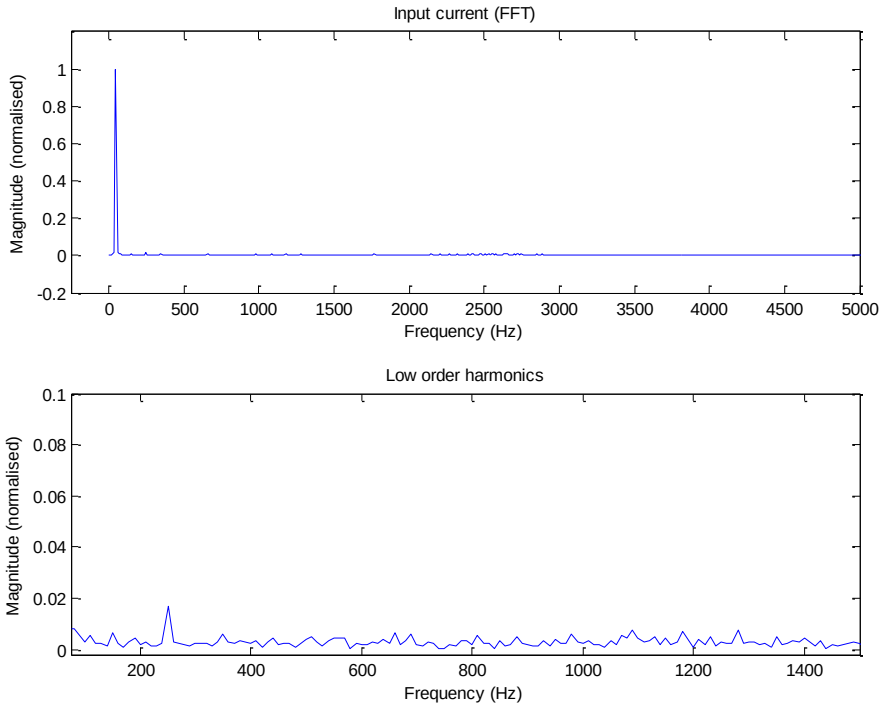


Fig. 8.33 DSRC with voltage compensation: FFT of the input current (experimental).

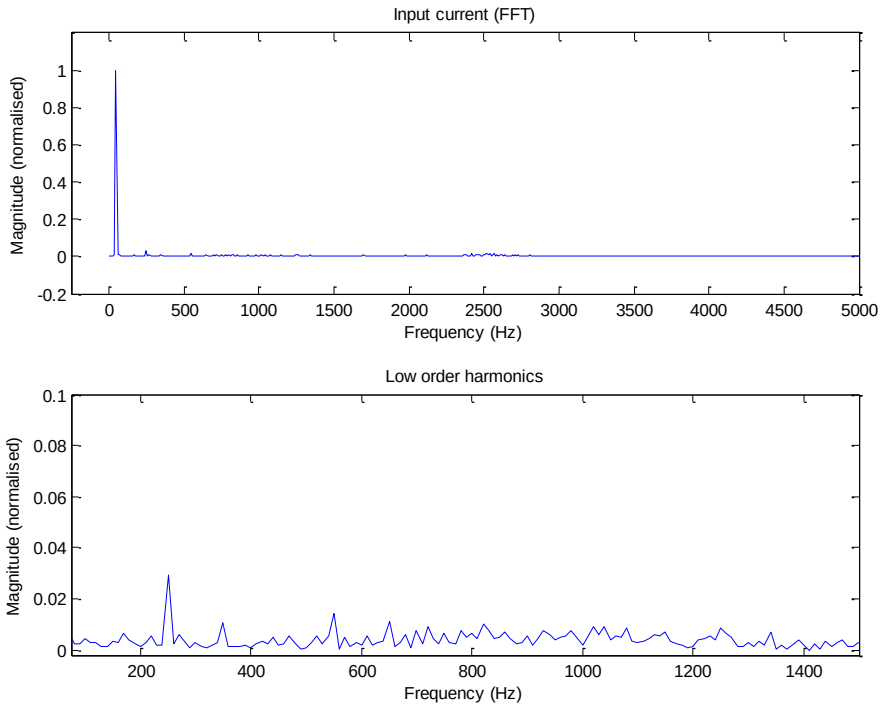


Fig. 8.34 DSRC without voltage compensation: FFT of the input current (experimental).

8.7 Power losses and efficiency estimations

The main focus of this work has been on control of the DSRC and, therefore, experimental investigation of the converter losses has not been attempted because of time constraints. Direct electrical measurement of losses via an input-output approach is extremely difficult due to the complex waveforms (with significant high frequency components) at both the input and output sides. Calorimetry [33, 34] would provide a feasible way of evaluating overall losses, but requires significant experimental development, and time consuming calibration and testing. However, it is still instructive and valuable to estimate the expected losses, particularly, for the extra losses associated with the compensator. In this section, losses are estimated using the methodology developed earlier in section 6.5.4.

In order to estimate the power losses and the efficiency of the power converter, a nominal output current ($10A_{rms}$) is considered. The power losses calculated using the parameters given in tables 5.2 and 6.3 are shown in table 8.1. Table 8.2 gives the efficiency of the DSRC with and without voltage compensator. Since the converters operate under ZCS, the switching losses are not considered.

Table 8.1 Power losses of the DSRC with voltage compensation.

Matrix Converter	H-Bridge Converter	Resonant Tank Inductor	Input Filter	Total Losses
48.01W (33.89%)	32.01W (22.59%)	57.80W (40.79%)	3.87W (2.73%)	141.69W (100%)

Table 8.2 Efficiency with/without H-bridge converter (voltage compensator).

	Output Power (Load: 19Ω)	Input Power	Efficiency
With H-Bridge	1.9kW	2.04kW	93.1%
Without H-Bridge	1.9kW	2.01kW	94.6%

Table 8.3 and 8.4 give the estimation of the power losses and efficiency based on measurements carried out in the experimental system. The output current considered for calculations is $9.82A_{rms.}$

Table 8.3 Estimated experimental power losses.

Resonant Tank Inductor	Other losses	Total Losses
55.72W (25.81%)	160.16W (74.19%)	215.88W (100%)

Table 8.4 Estimated experimental efficiency.

Output Power (Load: 19Ω)	Input Power	Efficiency
1.83kW	2.05kW	89.5%

From table 8.1, the power loss associated with the H-bridge compensator (conduction losses) corresponds to 22.59% of the total losses. Thus, this power loss reduces the converter efficiency by 1.5% approximately, as shown in table 8.2. In order to decrease the compensator losses, different semiconductor devices, such as MOSFETs, can be considered to implement the H-bridge converter.

8.8 Summary

This chapter has presented the results obtained with the experimental converter. The selection of the weighting factor related to the compensator capacitor voltage control has been described. Various results for the converter operating at nominal output current and considering output voltage compensation have been depicted. These results have shown the correct operation for the proposed voltage compensation strategy and for the proposed control strategies generally.

In addition, step changes in reference have been utilised in order to verify the operation of the control approach described in chapter 6. Waveforms for an output current reference above the limits previously defined in chapter 4 have been depicted to show the distortion generated at the input in order to verify the analysis given in section 4.4. Results for the converter operating with and without voltage compensation have been presented to demonstrate the effects of the voltage compensation proposed in chapter 6. Thus, the distortion of the output current

(magnitude ripple) and the input current THD have been reduced by approximately 40%; the input current THD being decreased from 4.4% to 2.7%.

The power losses and the efficiency of the experimental converter have been calculated in order to estimate the effect of the voltage compensation strategy on the converter efficiency. The efficiency of the experimental system reaches 89.5% (with voltage compensation) and the power loss due to the H-bridge compensator is about 22.6% of the total losses. Owing to the inclusion of the voltage compensator, the converter efficiency is reduced by 1.5% approximately.

Chapter 9

Conclusions

One of the main desirable characteristics of direct power converter topologies is the potential increase in power density in comparison with conventional converters. This characteristic has been the reason for using direct converters in various applications, such as electrical drives. Another application which can utilise the high power density characteristic to advantage is in high power supplies. Modern high power supplies utilise resonant converters, which avoids significant power loss when operating at high frequencies. These resonant converters are usually based on an inverter topology whose dc input voltage is stabilised by the input capacitor, which often occupies a significant proportion of the volume of the power supply. Therefore, in order to achieve compact high power supplies, research on employing a direct topology in a power supply is interesting. Thus, a resonant converter based on a direct topology has been investigated in this work.

A direct resonant converter (DRC) allows the direct connection of a three-phase power supply to a resonant circuit and a load. As in loaded resonant converters, the resonant circuit is used for generating a high frequency sinusoidal waveform. Since a DRC is operated at high frequency, in order to achieve a power supply as compact as possible, the control strategy of a DRC must consider minimising the power losses. Hence, a DRC, like a conventional resonant converter, is expected to operate under zero current switching (ZCS) and/or zero voltage switching (ZVS).

In this thesis, control strategies for a direct series resonant converter (DSRC) were investigated. Since the converter operates at high frequency, model predictive control was considered. This control technique allows application of an optimum switching

state to the power converter. In order to minimise the switching power losses, the control strategies developed in this research switch the converter at every zero crossing of the output current.

Three predictive control strategies were developed in this research, namely input current predictive control (ICPC), output current predictive control (OCPC) and input-output predictive control (IOPC). ICPC strategy achieves sinusoidal input currents, however, considerable distortion can be produced at the output since the predictive algorithm does not include the output side in the optimisation process. In contrast, OCPC allows the control of the output current, however, the input current becomes highly distorted. As a consequence, it is necessary to control both sides of the converter. Hence, a predictive algorithm that includes both the input and output currents was analysed. Although, the IOPC approach controls both currents, owing to the difference between the input and output optimal operating conditions, distortion of both currents is generated. In order to reduce the distortion at the output, a new voltage compensation approach was proposed in this thesis.

The voltage compensation approach introduces an H-bridge converter connected in series between the matrix converter and the resonant tank. Since the H-bridge converter (compensator) can provide three different voltages (positive, negative and zero), the output voltage of the matrix converter can be compensated, resulting in a decrease in the distortion of the voltage applied to the resonant tank. The voltage across the H-bridge capacitor is controlled by including it in the predictive algorithm. This voltage is regulated via the switching of the H-bridge compensator, since the current through the capacitor corresponds to the output current, i.e. no separate dc supply is needed to feed the capacitor. In order to reduce the power losses due to the compensator, the H-bridge converter operates under ZCS. In addition, the compensator capacitance value needed is small in comparison with the capacitance utilised in conventional resonant converters.

In order to validate the proposed control and compensation strategies, simulations were developed and an experimental prototype was constructed. Comprehensive results were shown in the thesis. In the simulation and experimental results, the expected operation of the converter, including the compensation approach, was demonstrated. Good performance of the predictive control strategies developed was also demonstrated.

Finally, the achievements of this research are summarised as follows:

- Predictive control strategies for a direct series resonant converter have been developed.
- A voltage compensation approach to improve the control and performance of the converter has been developed.
- The current/voltage limitations for a direct resonant converter have been analysed in detail.
- Simulations of the proposed control and compensation strategies have been carried out in order to verify the performance of the system.
- A direct series resonant converter with an output voltage compensator has been built in order to experimentally validate the proposed control and compensation strategies.

9.1 Further work

To continue the research on this topic, some suggestions are given:

- Apply the compensation approach to a direct series resonant converter with unbalance supply voltage.
- Consider a direct series resonant converter with dc output stage (rectifier and output filter).
- Verify the compensation approach for a higher power level.
- Investigate operation with a magnetron load.

9.2 Published papers

E. F. Reyes, A. J. Watson, J. C. Clare and P. W. Wheeler, "Comparison of Predictive Control Strategies for Direct Resonant High Voltage DC Power Supply," PEMD Conference, Bristol, UK, 2012.

E. Reyes-Moraga, A. Watson, J. Clare and P. Wheeler, "Predictive Control of a Direct Resonant Converter with Output Voltage Compensation for High Voltage DC Power Supply Applications," EPE Conference, Lille, France, 2013.

Appendix A

Input Filter Model

The input filter utilised in this work is depicted in figure A.1.

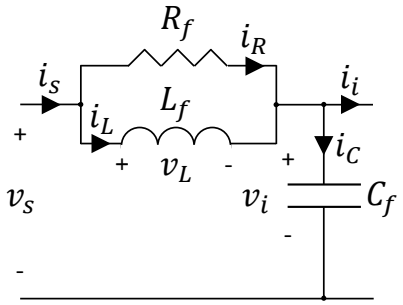


Fig. A.1 Input filter.

The dynamic equations of the input filter are given by (A.1)-(A.3), where v_s, v_L, v_i, i_s, i_C and i_i are the input voltage, the inductor voltage, the capacitor voltage, the input current, the capacitor current and the input converter current, respectively.

$$v_s(t) = v_L(t) + v_i(t) \Rightarrow v_s(t) = L_f \frac{d}{dt} i_L(t) + v_i(t) \qquad (A.1)$$

$$i_s(t) = i_C(t) + i_i(t) \Rightarrow i_s(t) = C_f \frac{d}{dt} v_i(t) + i_i(t) \qquad (A.2)$$

$$i_s(t) = i_L(t) + i_R(t) \Rightarrow i_s(t) = i_L(t) + \frac{[v_s(t) - v_i(t)]}{R_f} \qquad (A.3)$$

Thus, the second order filter can be modelled by:

$$\begin{bmatrix} \frac{d}{dt} i_L(t) \\ \frac{d}{dt} v_i(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & -\frac{1}{R_f C_f} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_i(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_f} \\ -\frac{1}{C_f} & \frac{1}{R_f C_f} \end{bmatrix} \begin{bmatrix} i_i(t) \\ v_s(t) \end{bmatrix} \qquad (A.4)$$

The output variables (i_s and v_i) are given by:

$$\begin{bmatrix} i_s(t) \\ v_i(t) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{R_f} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_i(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{R_f} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_i(t) \\ v_s(t) \end{bmatrix} \quad (A.5)$$

Thus, discretising (A.4), the discrete-time model of the input filter is given by:

$$\begin{bmatrix} i_L(k+1) \\ v_i(k+1) \end{bmatrix} = \begin{bmatrix} E_{in11} & E_{in12} \\ E_{in21} & E_{in22} \end{bmatrix} \begin{bmatrix} i_L(k) \\ v_i(k) \end{bmatrix} + \begin{bmatrix} F_{in11} & F_{in12} \\ F_{in21} & F_{in22} \end{bmatrix} \begin{bmatrix} i_i(k) \\ v_s(k) \end{bmatrix} \quad (A.6)$$

$$E_{in11} = \left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s + \psi_{in} \right) \quad (A.7)$$

$$E_{in12} = -\left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \sqrt{\frac{C_f}{L_f}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s \right) \quad (A.8)$$

$$E_{in21} = \left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \sqrt{\frac{L_f}{C_f}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s \right) \quad (A.9)$$

$$E_{in22} = -\left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s - \psi_{in} \right) \quad (A.10)$$

$$F_{in11} = 1 - \left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s + \psi_{in} \right) \quad (A.11)$$

$$F_{in12} = \left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \sqrt{\frac{C_f}{L_f}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s \right) \quad (A.12)$$

$$F_{in21} = -\left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \sqrt{\frac{L_f}{C_f}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s \right) \quad (A.13)$$

$$F_{in22} = 1 + \left(\frac{e^{-\delta_{in}\omega_o^{in}T_s}}{\sqrt{1-\delta_{in}^2}} \right) sin\left(\omega_o^{in}\sqrt{1-\delta_{in}^2}T_s - \psi_{in} \right) \quad (A.14)$$

Where ω_o^{in} is the cut-off frequency of the filter, and δ_{in} and ψ_{in} are given by:

$$\omega_o^{in} = \frac{1}{\sqrt{L_f C_f}} \quad ; \quad \delta_{in} = \frac{1}{2R_f}\sqrt{\frac{L_f}{C_f}} \quad ; \quad \psi_{in} = tan^{-1}\left(\frac{\sqrt{1-\delta_{in}^2}}{\delta_{in}}\right) \qquad (A.15)$$

Appendix B

Resonant Tank Model

Figure B.1 shows a series resonant circuit whose dynamic equation is given by:

$$v_{tank}(t) = L_{tank}\frac{d}{dt}i_{tank}(t) + \frac{1}{C_{tank}}\int_0^t i_{tank}(\tau)d\tau + R_{Load}i_{tank}(t) \qquad (B.1)$$

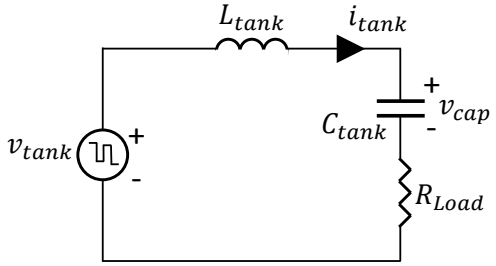


Fig. B.1 Series resonant tank.

This integro-differential equation can be represented by a pair of differential equations:

$$v_{tank}(t) = L_{tank}\frac{d}{dt}i_{tank}(t) + v_{cap}(t) + R_{Load}i_{tank}(t) \qquad (B.2)$$

$$i_{tank}(t) = C_{tank}\frac{d}{dt}v_{cap}(t) \qquad (B.3)$$

From (B.2) and (B.3), a state-space model for the series resonant circuit can be defined by:

$$\begin{bmatrix}\frac{d}{dt}i_{tank}(t)\\ \frac{d}{dt}v_{cap}(t)\end{bmatrix} = \begin{bmatrix}-\frac{R_{Load}}{L_{tank}} & -\frac{1}{L_{tank}}\\ \frac{1}{C_{tank}} & 0\end{bmatrix}\begin{bmatrix}i_{tank}(t)\\ v_{cap}(t)\end{bmatrix} + \begin{bmatrix}\frac{1}{L_{tank}}\\ 0\end{bmatrix}v_{tank}(t) \qquad (B.4)$$

Discretising (B.4), the discrete-time model of the resonant tank is given by (B.5)-(B.11), where ω_o^{out}, ω_d^{out}, Z_o^{out}, δ_{out} and ψ_{out} correspond to the corner frequency, the damped natural frequency, the characteristic impedance, the damping factor and the angle defined by the poles of the resonant circuit, respectively.

$$\begin{bmatrix} i_{tank}(k+1) \\ v_{cap}(k+1) \end{bmatrix} = \begin{bmatrix} E_{out11} & E_{out12} \\ E_{out21} & E_{out22} \end{bmatrix} \begin{bmatrix} i_{tank}(k) \\ v_{cap}(k) \end{bmatrix} + \begin{bmatrix} F_{out1} \\ F_{out2} \end{bmatrix} v_{tank}(k) \qquad (B.5)$$

$$E_{out11} = -\frac{e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s - \psi_{out}) \qquad (B.6)$$

$$E_{out12} = -\frac{e^{-\delta_{out}\omega_o^{out}T_s}}{Z_o^{out}\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s) \qquad (B.7)$$

$$E_{out21} = \frac{Z_o^{out}e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s) \qquad (B.8)$$

$$E_{out22} = \frac{e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s + \psi_{out}) \qquad (B.9)$$

$$F_{out1} = \frac{e^{-\delta_{out}\omega_o^{out}T_s}}{Z_o^{out}\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s) \qquad (B.10)$$

$$F_{out2} = 1 - \frac{e^{-\delta_{out}\omega_o^{out}T_s}}{\sqrt{1-\delta_{out}^2}} sin(\omega_d^{out}T_s + \psi_{out}) \qquad (B.11)$$

$$\omega_o^{out} = \frac{1}{\sqrt{L_{tank}C_{tank}}} \;\; ; \;\; Z_o^{out} = \sqrt{\frac{L_{tank}}{C_{tank}}} \;\; ; \;\; \delta_{out} = \frac{R_{Load}}{2Z_o^{out}} \qquad (B.12)$$

$$\omega_d^{out} = \omega_o^{out}\sqrt{1-\delta_{out}^2} \;\; ; \;\; \psi_{out} = tan^{-1}\left(\frac{\sqrt{1-\delta_{out}^2}}{\delta_{out}}\right) \qquad (B.13)$$

References

[1] F. Carastro, A. Castellazzi, J. Clare and P. Wheeler, "High-Efficiency High-Reliability Pulsed Power Converters for Industrial Processes," IEEE Trans. Power Electron., vol.27, no.1, pp.37-45, January 2012.

[2] H. Wang, P. Zanchetta, J. Clare and C. Ji, "Modelling and Control of a Zero Current Switching High-Voltage Resonant Converter Power Supply for Radio Frequency Sources," IET Power Electron., vol.5, no.4, pp.401-409, 2012.

[3] D. J. Cook, A Direct Resonant Converter for High Power RF Applications. PhD Thesis, University of Nottingham, 2007.

[4] M. Catucci, Control and Practical Implementation of a ZCS Direct Resonant Converter. PhD Thesis, University of Nottingham, 2006.

[5] S. Y. (Ron) Hui and Henry S. H. Chung, "Resonant and soft-switching converters," in Power Electronics Handbook: Devices, Circuits, and Applications, 3rd ed., M. H. Rashid, Ed. Oxford, UK: Elsevier, 2011, pp. 409-453.

[6] M. K. Kazimierczuk and D. Czarkowski, Resonant Power Converters, 2nd ed. Hoboken, New Jersey: Wiley, 2011.

[7] N. Mohan, T. M. Undeland and W. P. Robbins, Power Electronics: Converters, Applications, and Design, 2nd ed. New York: Wiley, 1995.

[8] H. Wang, Multivariable State Feedback Control for Resonant Long-pulse Modulator. PhD Thesis, University of Nottingham, 2008.

[9] F. Carastro, A. Goodman, J. Leach J. C. Clare and P. W. Wheeler, "Control and Implementation of a High Voltage Series Resonant Power Supply for Industrial Electrostatic Precipitators," IEEE ECCE Conference, Atlanta, USA, 2010.

[10] F. Carastro, J. Clare, A. Goodman, P. Wheeler, J. Leach and T. Hosking, "A 100kV Switch Mode Series Resonant Power Supply for Industrial Electrostatic Precipitators," IEEE IPMHVC Conference, Atlanta, USA, 2010.

[11] N. A. Abodhir, A. J. Watson, C. Ji and J. C. Clare, "Resonant Converter Based Modulator Control for Magnetron with Variable Load," EPE-ECCE Europe Conference, Lappeenranta, Finland, 2014.

[12] N. A. Abodhir, A. J. Watson and J. C. Clare, "Control of High Voltage Series Resonant Power Supply for Industrial Magnetrons," PEMD Conference, Manchester, UK, 2014.

[13] E. F. Camacho and C. Bordons, Model Predictive Control, 2nd ed. London: Springer-Verlag, 2007.

[14] L. Wang, Model Predictive Control System Design and Implementation Using MATLAB. London: Springer-Verlag, 2009.

[15] A. Linder, R. Kanchan, P. Stolze and R. Kennel, Model-based Predictive Control of Electric Drives. Göttingen: Cuvillier Verlag, 2010.

[16] J. Rodriguez and P. Cortes, Predictive Control of Power Converters and Electrical Drives. Chichester: Wiley, 2012.

[17] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo and J. Rodriguez, "Predictive Control in Power Electronics and Drives," IEEE Trans. Ind. Electron., vol.55, no.12, pp.4312-4324, Dec. 2008.

[18] P. Cortes, S. Kouro, B. La Rocca, R. Vargas, J. Rodriguez, J. I. Leon, S. Vasquez and L. G. Franquelo, "Guidelines for Weighting Factors Design in Model Predictive Control of Power Converters and Drives," International Conference on Industrial Technology, ICIT 2009, Churchill, Australia, 2009.

[19] I. Batarseh, "The power MOSFET," in Power Electronics Handbook: Devices, Circuits, and Applications, 3rd ed., M. H. Rashid, Ed. Oxford, UK: Elsevier, 2011, pp. 43-71.

[20] J. R. Espinoza, "Inverters," in Power Electronics Handbook: Devices, Circuits, and Applications, 3rd ed., M. H. Rashid, Ed. Oxford, UK: Elsevier, 2011, pp. 357-408.

[21] M. Catucci, J. Clare and P. Wheeler, "Predictive Control Strategies for ZCS Direct Converter HV Power Supply," EPE Conference, Dresden, Germany, 2005.

[22] M. Catucci, J. Clare and P. Wheeler, "ZCS Predictive Controllers for High Frequency AC-Link Resonant Converter," EPE-PEMC Conference, Portoroz, Slovenia, 2006.

[23] M. Catucci, J. Clare and P. Wheeler, "Predictive Control Strategy for ZCS Single Stage Resonant Converter," IECON Conference, Paris, France, 2006.

[24] D. J. Cook, M. Catucci, P. W. Wheeler, J. C. Clare, J. S. Przybyla and B. R. Richardson, "Development of a Predictive Controller for Use on a Direct Converter for High-Energy Physics Applications," IEEE Trans. Ind. Electron., vol.55, no.12, pp.4325-4334, December 2008.

[25] P. W. Wheeler, J. Rodríguez, J. C. Clare, L. Empringham and A. Weinstein, "Matrix Converters: A Technology Review," IEEE Trans. Ind. Electron., vol.49, no.2, pp.276-288, April 2002.

[26] L. Empringham, J. W. Kolar, J. Rodríguez, P. W. Wheeler and J. C. Clare, "Technological Issues and Industrial Application of Matrix Converters: A Review," IEEE Trans. Ind. Electron., vol.60, no.10, pp.4260-4271, October 2013.

[27] T. Wijekoon, New Improvements for the Two-stage Direct Power Converter Topology. PhD Thesis, University of Nottingham, 2007.

[28] C. Klumpner, "Hybrid Direct Power Converters with Increase/Higher than Unity Voltage Transfer Ratio and Improved Robustness against Voltage Supply Disturbances," IEEE PESC Conference, Recife, Brazil, 2005.

[29] C. Klumpner, T. Wijekoon and P. Wheeler, "A New Class of Hybrid AC/AC Direct Power Converters," IEEE IAS Conference, Hong Kong, 2005.

[30] S. Mariethoz, "A New Control Scheme for a Hybrid Two-stage Matrix Converter with Improved Efficiency," IEEE IECON Conference, Paris, France, 2006.

[31] TMS320C6713 DSK Technical Reference, Spectrum Digital, INC.

[32] TMS320C6713 Floating-Point Digital Signal Processor Datasheet, Texas Instruments.

[33] F. Carastro, J. C. Clare, M. J. Bland and P. W. Wheeler, "Calorimetric Loss Measurements and Optimization of High Power Resonant Converters for Pulsed Applications," EPE Conference, Barcelona, Spain, 2009.

[34] F. Carastro, J. C. Clare, P. W. Wheeler, D. Cook, M. Musallam and M. J. Bland, "High Speed Thermal Imaging applied to a Long Pulse Resonant Converter Modulator for Power device Reliability Assessment," IEEE International Power Modulators and High Voltage Conference, Las Vegas, USA, 2008.